# TMUX112x 5-V, Low-Leakage-Current, 1:1 (SPST), 2-Channel Precision Switches

## 1 Features

- Wide supply range: 1.08V to 5.5V
- Low leakage current: 3pA
- Low charge injection: –1.5pC
- Low on-resistance: 1.9Ω
- –40°C to +125°C operating temperature
- 1.8V Logic compatible
- Fail-safe logic
- Rail to rail operation
- Bidirectional signal path
- Break-before-make switching
- ESD protection HBM: 2000 V

## 2 Applications

- Sample-and-hold circuits
- Feedback gain switching
- Signal isolation
- Field transmitters
- Programmable logic controllers (PLC)
- Factory automation and control
- Ultrasound scanners
- Patient monitoring and diagnostics
- Electrocardiogram (ECG)
- Data acquisition systems (DAQ)
- Semiconductor test equipment
- Battery test equipment
- Instrumentation: lab, analytical, portable
- Ultrasonic smart meters: water and gas
- Optical networking
- Optical test equipment

## 3 Description

The TMUX1121, TMUX1122, and TMUX1123 are precision complementary metal-oxide semiconductor (CMOS) devices that have two independently selectable 1:1, single-pole, single-throw (SPST) switches. Wide operating supply of 1.08V to 5.5V allows for use in a broad array of applications from medical equipment to industrial systems. The device supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from GND to $V_{DD}$.

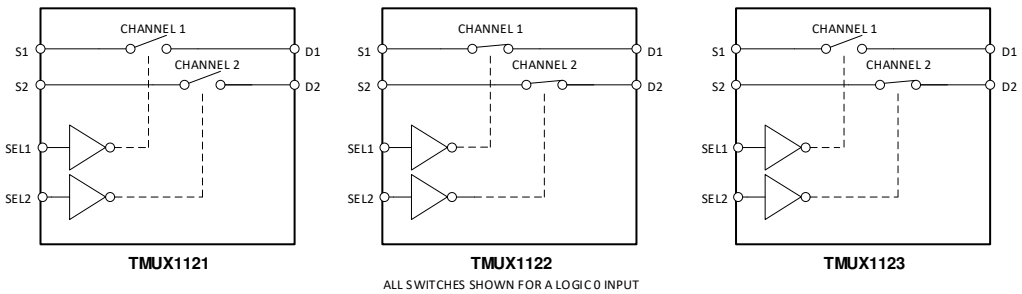
The switches of the TMUX1121 are turned on with Logic 1 on the appropriate logic control inputs, while Logic 0 is required to turn on switches in the TMUX1122. The two channels of the TMUX1123 are split with channel one supporting Logic 1, while channel two supports Logic 0. The TMUX1123 exhibits break-before-make switching, allowing the device to be used in cross-point switching applications.

The TMUX112x devices are part of the precision switches and multiplexers family. These devices have very low on and off leakage currents and low charge injection, allowing them to be used in high precision measurement applications. A low supply current of 7nA and small package options enable use in portable applications.

**Device Information**

| PART NUMBER(1) | CONTROL LOGIC(1) | PACKAGE(2) |
|---|---|---|
| TMUX1121<br>TMUX1122<br>TMUX1123 | Active High<br>Active Low<br>Mixed | DGK (VSSOP, 8) |

(1) See Device Comparison
(2) For more information, see Section 12




**TMUX112x Block Diagrams**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Device Comparison Table

| PRODUCT | DESCRIPTION |
|---|---|
| TMUX1121 | Low-Leakage-Current, 1:1 (SPST), 2-Channel Precision Switches (Active High) |
| TMUX1122 | Low-Leakage-Current, 1:1 (SPST), 2-Channel Precision Switches (Active Low) |
| TMUX1123 | Low-Leakage-Current, 1:1 (SPST), 2-Channel Precision Switches (Active High + Active Low) |


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# 5 Pin Configuration and Functions

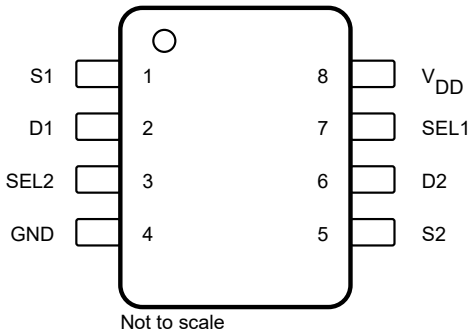



**Figure 5-1. DGK Package, 8-Pin VSSOP (Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION[2] |
|---|---|---|---|
| NAME | NO. | | |
| S1 | 1 | I/O | Source pin 1. Can be an input or output. |
| D1 | 2 | I/O | Drain pin 1. Can be an input or output. |
| SEL2 | 3 | I | Logic control select pin 2. Controls channel 2 state as shown in Truth Tables. |
| GND | 4 | P | Ground (0V) reference |
| S2 | 5 | I/O | Source pin 2. Can be an input or output. |
| D2 | 6 | I/O | Drain pin 2. Can be an input or output. |
| SEL1 | 7 | I | Logic control select pin 1. Controls channel 1 state as shown in Truth Tables. |
| $V_{DD}$ | 8 | P | Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between $V_{DD}$ and GND. |

(1) I = input, O = output, I/O = input and output, P = power
(2) Refer to Section 8.4 for what to do with unused pins

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | –0.5 | 6 | V |
| $V_{SEL}$ | Logic control input pin voltage (SELx) | –0.5 | 6 | V |
| $I_{SEL}$ | Logic control input pin current (SELx) | –30 | 30 | mA |
| $V_S$ or $V_D$ | Source or drain voltage (Sx, Dx) | –0.5 | $V_{DD}$+0.5 | V |
| $I_S$ or $I_{D\ (CONT)}$ | Source or drain continuous current (Sx, Dx) | $I_{DC}$ ± 10%(4) | $I_{DC}$ ± 10% (4) | mA |
| $I_S$ or $I_{D\ (PEAK)}$ | Source and drain peak current: (1ms period max, 10% duty cycle maximum) (Sx, D) | $I_{peak}$ ± 10 % (4) | $I_{peak}$ ± 10%(4) | mA |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |
| $P_{tot}$ | Total power dissipation(5) | | 300 | mW |
| $T_J$ | Junction temperature | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Refer to Recommended Operating Conditions for $I_{DC}$ and $I_{peak}$ ratings
(5) For DGK (VSSOP) package: $P_{tot}$ derates linearly above TA=88°C by 4.87mW/°C

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Positive power supply voltage | | 1.08 | | 5.5 | V |
| $V_S$ or $V_D$ | Signal path input/output voltage (source or drain pins: Sx, Dx) | | 0 | | $V_{DD}$ | V |
| $V_{SEL}$ | Logic control input pin voltage (SELx) | | 0 | | 5.5 | V |
| $T_A$ | Ambient temperature | | –40 | | 125 | °C |
| $I_{DC}$ | Signal path continuous current (source or drain pins: Sx, Dx) | Tj = 25°C | | 150 | | mA |
| | | Tj = 85°C | | 120 | | mA |
| | | Tj = 125°C | | 60 | | mA |
| | | Tj = 130°C | | 50 | | mA |
| $I_{peak}$ | Peak current through switch(1ms period max, 10% duty cycle maximum) | Tj = 25°C | | 300 | | mA |
| | | Tj = 85°C | | 300 | | mA |
| | | Tj = 125°C | | 180 | | mA |
| | | Tj = 130°C | | 160 | | mA |


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## 6.4 Thermal Information

| THERMAL METRIC[1] | | TMUX1121 / TMUX1122 / TMUX1123 DGK (VSSOP) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 205.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 91.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 127.0 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 25.9 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 125.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics ($V_{DD}$ = 5V ±10 %)

at $T_A$ = 25°C, $V_{DD}$ = 5V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0V to $V_{DD}$<br>$I_{SD}$ = 10mA<br>Refer to Section 7.1 | 25°C | | 1.9 | 4 | Ω |
| | | | –40°C to +85°C | | | 4.5 | Ω |
| | | | –40°C to +125°C | | | 4.9 | Ω |
| $\Delta R_{ON}$ | On-resistance matching between channels | $V_S$ = 0V to $V_{DD}$<br>$I_{SD}$ = 10mA<br>Refer to Section 7.1 | 25°C | | 0.13 | | Ω |
| | | | –40°C to +85°C | | | 0.4 | Ω |
| | | | –40°C to +125°C | | | 0.5 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0V to $V_{DD}$<br>$I_{SD}$ = 10mA<br>Refer to Section 7.1 | 25°C | | 0.85 | | Ω |
| | | | –40°C to +85°C | | | 1.6 | Ω |
| | | | –40°C to +125°C | | | 1.6 | Ω |
| $I_{S(OFF)}$ | Source off leakage current[1] | $V_{DD}$ = 5V<br>Switch Off<br>$V_D$ = 4.5V / 1.5V<br>$V_S$ = 1.5V / 4.5V<br>Refer to Section 7.2 | 25°C | –0.08 | ±0.003 | 0.08 | nA |
| | | | –40°C to +85°C | –0.3 | | 0.3 | nA |
| | | | –40°C to +125°C | –0.9 | | 0.9 | nA |
| $I_{D(OFF)}$ | Drain off leakage current[1] | $V_{DD}$ = 5V<br>Switch Off<br>$V_D$ = 4.5V / 1.5V<br>$V_S$ = 1.5V / 4.5V<br>Refer to Section 7.2 | 25°C | –0.08 | ±0.003 | 0.08 | nA |
| | | | –40°C to +85°C | –0.3 | | 0.3 | nA |
| | | | –40°C to +125°C | –0.9 | | 0.9 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 5V<br>Switch On<br>$V_D$ = $V_S$ = 4.5V / 1.5V<br>Refer to Section 7.3 | 25°C | –0.1 | ±0.003 | 0.1 | nA |
| | | | –40°C to +85°C | –0.35 | | 0.35 | nA |
| | | | –40°C to +125°C | –2 | | 2 | nA |
| **LOGIC INPUTS (SELx)** | | | | | | | |
| $V_{IH}$ | Input logic high | | –40°C to +125°C | 1.49 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | –40°C to +125°C | 0 | | 0.87 | V |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | 25°C | | ±0.005 | | µA |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | –40°C to +125°C | | | ±0.05 | µA |
| $C_{IN}$ | Logic input capacitance | | 25°C | | 1 | | pF |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | | 2 | pF |
| **POWER SUPPLY** | | | | | | | |

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## 6.5 Electrical Characteristics ($V_{DD}$ = 5V ±10 %) (continued)

at $T_A$ = 25°C, $V_{DD}$ = 5V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0V or 5.5V | 25°C | | 0.007 | | µA |
| | | | –40°C to +125°C | | | 1 | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $t_{TRAN}$ | Transition time between channels | $V_S$ = 3V<br>$R_L$ = 200Ω, $C_L$ = 15pF<br>Refer to Section 7.4 | 25°C | | 12 | | ns |
| | | | –40°C to +85°C | | | 17 | ns |
| | | | –40°C to +125°C | | | 18 | ns |
| $t_{OPEN}$ (BBM) | Break before make time (TMUX1123 Only) | $V_S$ = 3V<br>$R_L$ = 200Ω, $C_L$ = 15pF<br>Refer to Section 7.5 | 25°C | | 8 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $Q_C$ | Charge Injection | $V_S$ = 1V<br>$R_S$ = 0Ω, $C_L$ = 1nF<br>Refer to Section 7.6 | 25°C | | –1.5 | | pC |
| $O_{ISO}$ | Off Isolation | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 1MHz<br>Refer to Section 7.7 | 25°C | | –62 | | dB |
| | | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 10MHz<br>Refer to Section 7.7 | 25°C | | –40 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 1MHz<br>Refer to Section 7.8 | 25°C | | –100 | | dB |
| | | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 10MHz<br>Refer to Section 7.8 | 25°C | | –90 | | dB |
| BW | Bandwidth | $R_L$ = 50Ω, $C_L$ = 5pF<br>Refer to Section 7.9 | 25°C | | 300 | | MHz |
| $C_{SOFF}$ | Source off capacitance | f = 1MHz | 25°C | | 6 | | pF |
| $C_{DOFF}$ | Drain off capacitance | f = 1MHz | 25°C | | 10 | | pF |
| $C_{SON}$<br>$C_{DON}$ | On capacitance | f = 1MHz | 25°C | | 18 | | pF |

(1) When $V_S$ is 4.5V, $V_D$ is 1.5V or when $V_S$ is 1.5V, $V_D$ is 4.5V.

## 6.6 Electrical Characteristics ($V_{DD}$ = 3.3V ±10 %)

at $T_A$ = 25°C, $V_{DD}$ = 3.3V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0V to $V_{DD}$<br>$I_{SD}$ = 10mA<br>Refer to Section 7.1 | 25°C | | 3.7 | 8.8 | Ω |
| | | | –40°C to +85°C | | | 9.5 | Ω |
| | | | –40°C to +125°C | | | 9.8 | Ω |
| $\Delta R_{ON}$ | On-resistance matching between channels | $V_S$ = 0V to $V_{DD}$<br>$I_{SD}$ = 10mA<br>Refer to Section 7.1 | 25°C | | 0.13 | | Ω |
| | | | –40°C to +85°C | | | 0.4 | Ω |
| | | | –40°C to +125°C | | | 0.5 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0V to $V_{DD}$<br>$I_{SD}$ = 10mA<br>Refer to Section 7.1 | 25°C | | 1.9 | | Ω |
| | | | –40°C to +85°C | | 2 | | Ω |
| | | | –40°C to +125°C | | 2.2 | | Ω |


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## 6.6 Electrical Characteristics ($V_{DD}$ = 3.3V ±10 %) (continued)

at $T_A$ = 25°C, $V_{DD}$ = 3.3V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 3.3V<br>Switch Off<br>$V_D$ = 3V / 1V<br>$V_S$ = 1V / 3V<br>Refer to Section 7.2 | 25°C | –0.05 | ±0.001 | 0.05 | nA |
| | | | –40°C to +85°C | –0.2 | | 0.2 | nA |
| | | | –40°C to +125°C | –0.9 | | 0.9 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 3.3V<br>Switch Off<br>$V_D$ = 3V / 1V<br>$V_S$ = 1V / 3V<br>Refer to Section 7.2 | 25°C | –0.05 | ±0.001 | 0.05 | nA |
| | | | –40°C to +85°C | –0.2 | | 0.2 | nA |
| | | | –40°C to +125°C | –0.9 | | 0.9 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 3.3V<br>Switch On<br>$V_D$ = $V_S$ = 3V / 1V<br>Refer to Section 7.3 | 25°C | –0.1 | ±0.003 | 0.1 | nA |
| | | | –40°C to +85°C | –0.35 | | 0.35 | nA |
| | | | –40°C to +125°C | –2 | | 2 | nA |
| **LOGIC INPUTS (SELx)** | | | | | | | |
| $V_{IH}$ | Input logic high | | –40°C to +125°C | 1.35 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | 25°C | | ±0.005 | | µA |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | –40°C to +125°C | | | ±0.05 | µA |
| $C_{IN}$ | Logic input capacitance | | 25°C | | 1 | | pF |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | | 2 | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0V or 5.5V | 25°C | | 0.004 | | µA |
| | | | –40°C to +125°C | | | 1 | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $t_{TRAN}$ | Transition time between channels | $V_S$ = 2V<br>$R_L$ = 200Ω, $C_L$ = 15pF<br>Refer to Section 7.4 | 25°C | | 14 | | ns |
| | | | –40°C to +85°C | | | 20 | ns |
| | | | –40°C to +125°C | | | 22 | ns |
| $t_{OPEN}$ (BBM) | Break before make time (TMUX1123 Only) | $V_S$ = 2V<br>$R_L$ = 200Ω, $C_L$ = 15pF<br>Refer to Section 7.5 | 25°C | | 9 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $Q_C$ | Charge Injection | $V_S$ = 1V<br>$R_S$ = 0Ω, $C_L$ = 1nF<br>Refer to Section 7.6 | 25°C | | –1.5 | | pC |
| $O_{ISO}$ | Off Isolation | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 1MHz<br>Refer to Section 7.7 | 25°C | | –62 | | dB |
| | | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 10MHz<br>Refer to Section 7.7 | 25°C | | –40 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 1MHz<br>Refer to Section 7.8 | 25°C | | –100 | | dB |
| | | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 10MHz<br>Refer to Section 7.8 | 25°C | | –90 | | dB |
| BW | Bandwidth | $R_L$ = 50Ω, $C_L$ = 5pF<br>Refer to Section 7.9 | 25°C | | 300 | | MHz |
| $C_{SOFF}$ | Source off capacitance | f = 1MHz | 25°C | | 6 | | pF |
| $C_{DOFF}$ | Drain off capacitance | f = 1MHz | 25°C | | 10 | | pF |

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## 6.6 Electrical Characteristics ($V_{DD}$ = 3.3V ±10 %) (continued)

at $T_A$ = 25°C, $V_{DD}$ = 3.3V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{SON}$<br>$C_{DON}$ | On capacitance | f = 1MHz | 25°C | | 18 | | pF |

(1) When $V_S$ is 3V, $V_D$ is 1V or when $V_S$ is 1V, $V_D$ is 3V.

## 6.7 Electrical Characteristics ($V_{DD}$ = 1.8V ±10 %)

at $T_A$ = 25°C, $V_{DD}$ = 1.8V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0V to $V_{DD}$<br>$I_{SD}$ = 10mA<br>Refer to Section 7.1 | 25°C | | 40 | | Ω |
| | | | –40°C to +85°C | | | 80 | Ω |
| | | | –40°C to +125°C | | | 80 | Ω |
| $\Delta R_{ON}$ | On-resistance matching between channels | $V_S$ = 0V to $V_{DD}$<br>$I_{SD}$ = 10mA<br>Refer to Section 7.1 | 25°C | | 0.4 | | Ω |
| | | | –40°C to +85°C | | | 1.5 | Ω |
| | | | –40°C to +125°C | | | 1.5 | Ω |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 1.98V<br>Switch Off<br>$V_D$ = 1.62 V / 1V<br>$V_S$ = 1V / 1.62 V<br>Refer to Section 7.2 | 25°C | –0.05 | ±0.001 | 0.05 | nA |
| | | | –40°C to +85°C | –0.2 | | 0.2 | nA |
| | | | –40°C to +125°C | –0.9 | | 0.9 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 1.98V<br>Switch Off<br>$V_D$ = 1.62 V / 1V<br>$V_S$ = 1V / 1.62 V<br>Refer to Section 7.2 | 25°C | –0.05 | ±0.001 | 0.05 | nA |
| | | | –40°C to +85°C | –0.2 | | 0.2 | nA |
| | | | –40°C to +125°C | –0.9 | | 0.9 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 1.98V<br>Switch On<br>$V_D$ = $V_S$ = 1.62 V / 1V<br>Refer to Section 7.3 | 25°C | –0.1 | ±0.003 | 0.1 | nA |
| | | | –40°C to +85°C | –0.35 | | 0.35 | nA |
| | | | –40°C to +125°C | –2 | | 2 | nA |
| **LOGIC INPUTS (SELx)** | | | | | | | |
| $V_{IH}$ | Input logic high | | –40°C to +125°C | 1.07 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | –40°C to +125°C | 0 | | 0.68 | V |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | 25°C | | ±0.005 | | µA |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | –40°C to +125°C | | | ±0.05 | µA |
| $C_{IN}$ | Logic input capacitance | | 25°C | | 1 | | pF |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | | 2 | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0V or 5.5V | 25°C | | 0.001 | | µA |
| | | | –40°C to +125°C | | | 0.85 | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $t_{TRAN}$ | Transition time between channels | $V_S$ = 1V<br>$R_L$ = 200Ω, $C_L$ = 15pF<br>Refer to Section 7.4 | 25°C | | 25 | | ns |
| | | | –40°C to +85°C | | | 44 | ns |
| | | | –40°C to +125°C | | | 44 | ns |
| $t_{OPEN}$ (BBM) | Break before make time (TMUX1123 Only) | $V_S$ = 1V<br>$R_L$ = 200Ω, $C_L$ = 15pF<br>Refer to Section 7.5 | 25°C | | 17 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |


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## 6.7 Electrical Characteristics ($V_{DD}$ = 1.8V ±10 %) (continued)

at $T_A$ = 25°C, $V_{DD}$ = 1.8V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $Q_C$ | Charge Injection | $V_S$ = 1V<br>$R_S$ = 0Ω, $C_L$ = 1nF<br>Refer to Section 7.6 | 25°C | | –0.5 | | pC |
| $O_{ISO}$ | Off Isolation | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 1MHz<br>Refer to Section 7.7 | 25°C | | –62 | | dB |
| | | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 10MHz<br>Refer to Section 7.7 | 25°C | | –40 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 1MHz<br>Refer to Section 7.8 | 25°C | | –100 | | dB |
| | | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 10MHz<br>Refer to Section 7.8 | 25°C | | –90 | | dB |
| BW | Bandwidth | $R_L$ = 50Ω, $C_L$ = 5pF<br>Refer to Section 7.9 | 25°C | | 300 | | MHz |
| $C_{SOFF}$ | Source off capacitance | f = 1MHz | 25°C | | 6 | | pF |
| $C_{DOFF}$ | Drain off capacitance | f = 1MHz | 25°C | | 10 | | pF |
| $C_{SON}$<br>$C_{DON}$ | On capacitance | f = 1MHz | 25°C | | 18 | | pF |

(1) When $V_S$ is 1.62 V, $V_D$ is 1V or when $V_S$ is 1V, $V_D$ is 1.62 V.

## 6.8 Electrical Characteristics ($V_{DD}$ = 1.2V ±10 %)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0V to $V_{DD}$<br>$I_{SD}$ = 10mA<br>Refer to Section 7.1 | 25°C | | 70 | | Ω |
| | | | –40°C to +85°C | | | 105 | Ω |
| | | | –40°C to +125°C | | | 105 | Ω |
| $\Delta R_{ON}$ | On-resistance matching between channels | $V_S$ = 0V to $V_{DD}$<br>$I_{SD}$ = 10mA<br>Refer to Section 7.1 | 25°C | | 0.4 | | Ω |
| | | | –40°C to +85°C | | | 1.5 | Ω |
| | | | –40°C to +125°C | | | 1.5 | Ω |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 1.32 V<br>Switch Off<br>$V_D$ = 1V / 0.8V<br>$V_S$ = 0.8V / 1V<br>Refer to Section 7.2 | 25°C | –0.05 | ±0.001 | 0.05 | nA |
| | | | –40°C to +85°C | –0.2 | | 0.2 | nA |
| | | | –40°C to +125°C | –0.9 | | 0.9 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 1.32 V<br>Switch Off<br>$V_D$ = 1V / 0.8V<br>$V_S$ = 0.8V / 1V<br>Refer to Section 7.2 | 25°C | –0.05 | ±0.001 | 0.05 | nA |
| | | | –40°C to +85°C | –0.2 | | 0.2 | nA |
| | | | –40°C to +125°C | –0.9 | | 0.9 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 1.32 V<br>Switch On<br>$V_D$ = $V_S$ = 1V / 0.8V<br>Refer to Section 7.3 | 25°C | –0.1 | ±0.003 | 0.1 | nA |
| | | | –40°C to +85°C | –0.35 | | 0.35 | nA |
| | | | –40°C to +125°C | –2 | | 2 | nA |
| **LOGIC INPUTS (SELx)** | | | | | | | |
| $V_{IH}$ | Input logic high | | –40°C to +125°C | 0.96 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | –40°C to +125°C | 0 | | 0.36 | V |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | 25°C | | ±0.005 | | µA |

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## 6.8 Electrical Characteristics ($V_{DD}$ = 1.2V ±10 %) (continued)

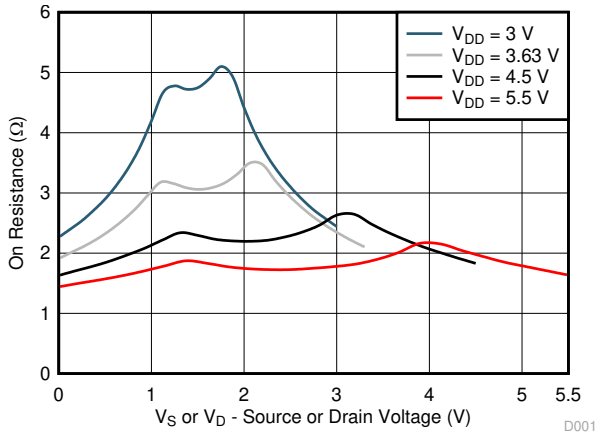
| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | –40°C to +125°C | | | ±0.05 | µA |
| $C_{IN}$ | Logic input capacitance | | 25°C | | 1 | | pF |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | | 2 | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0V or 5.5V | 25°C | | 0.001 | | µA |
| | | | –40°C to +125°C | | | 0.7 | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $t_{TRAN}$ | Transition time between channels | $V_S$ = 1V<br>$R_L$ = 200Ω, $C_L$ = 15pF<br>Refer to Section 7.4 | 25°C | | 55 | | ns |
| | | | –40°C to +85°C | | | 190 | ns |
| | | | –40°C to +125°C | | | 190 | ns |
| $t_{OPEN}$ (BBM) | Break before make time (TMUX1123 Only) | $V_S$ = 1V<br>$R_L$ = 200Ω, $C_L$ = 15pF<br>Refer to Section 7.5 | 25°C | | 28 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $Q_C$ | Charge Injection | $V_S$ = 1V<br>$R_S$ = 0Ω, $C_L$ = 1nF<br>Refer to Section 7.6 | 25°C | | –0.5 | | pC |
| $O_{ISO}$ | Off Isolation | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 1MHz<br>Refer to Section 7.7 | 25°C | | –62 | | dB |
| | | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 10MHz<br>Refer to Section 7.7 | 25°C | | –40 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 1MHz<br>Refer to Section 7.8 | 25°C | | –100 | | dB |
| | | $R_L$ = 50Ω, $C_L$ = 5pF<br>f = 10MHz<br>Refer to Section 7.8 | 25°C | | –90 | | dB |
| BW | Bandwidth | $R_L$ = 50Ω, $C_L$ = 5pF<br>Refer to Section 7.9 | 25°C | | 300 | | MHz |
| $C_{SOFF}$ | Source off capacitance | f = 1MHz | 25°C | | 6 | | pF |
| $C_{DOFF}$ | Drain off capacitance | f = 1MHz | 25°C | | 10 | | pF |
| $C_{SON}$<br>$C_{DON}$ | On capacitance | f = 1MHz | 25°C | | 18 | | pF |

(1) When $V_S$ is 1V, $V_D$ is 0.8V or when $V_S$ is 0.8V, $V_D$ is 1V.


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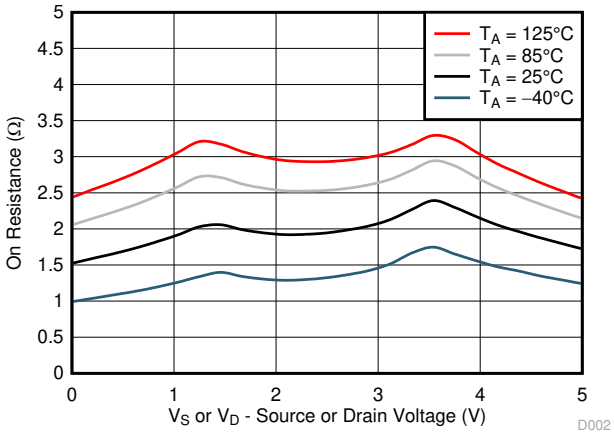
## 6.9 Typical Characteristics

at $T_A$ = 25°C, $V_{DD}$ = 5V (unless otherwise noted)



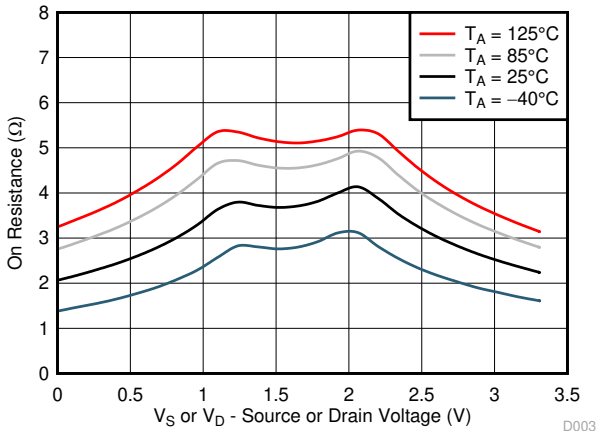

$T_A$ = 25°C

**Figure 6-1. On-Resistance vs Source or Drain Voltage**



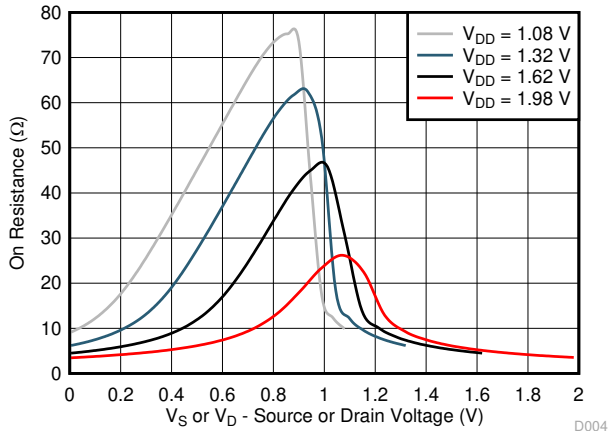

$V_{DD}$ = 5V

**Figure 6-2. On-Resistance vs Temperature**



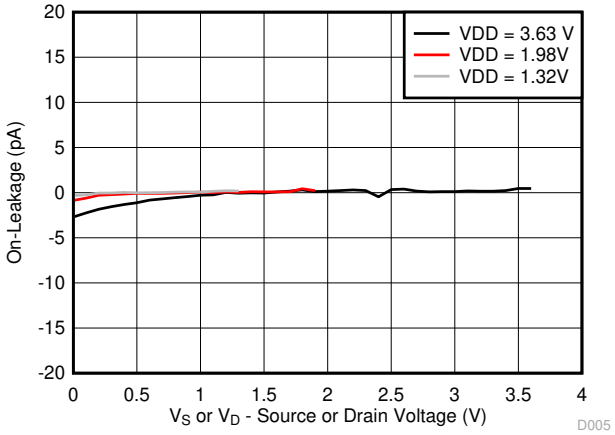

$V_{DD}$ = 3.3V

**Figure 6-3. On-Resistance vs Temperature**



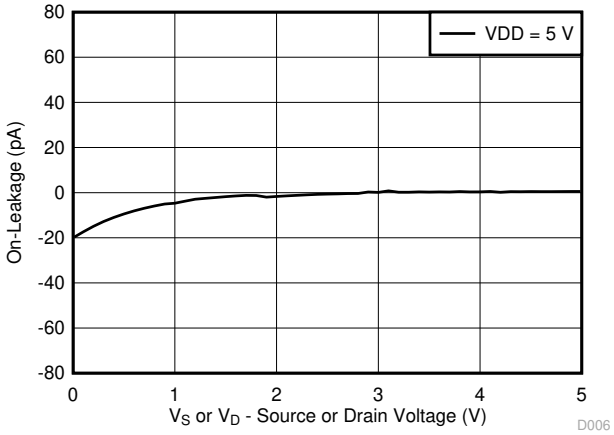

$T_A$ = 25°C

**Figure 6-4. On-Resistance vs Source or Drain Voltage**




$T_A$ = 25°C

**Figure 6-5. On-Leakage vs Source or Drain Voltage**



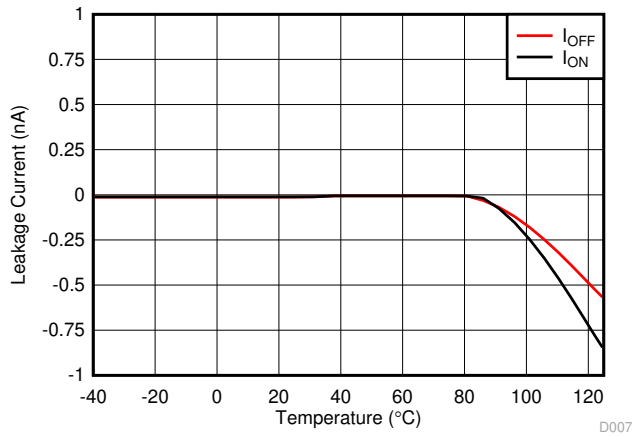

$T_A$ = 25°C

**Figure 6-6. On-Leakage vs Source or Drain Voltage**

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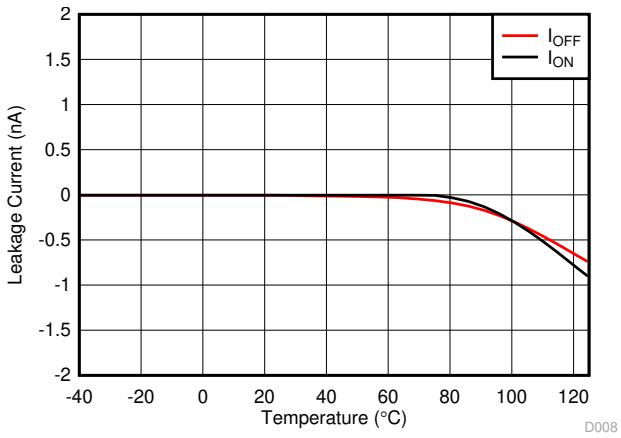
## 6.9 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_{DD}$ = 5V (unless otherwise noted)



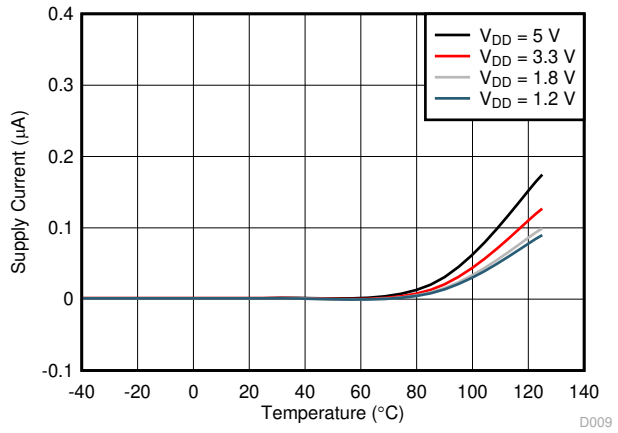

$V_{DD}$ = 3.3V

**Figure 6-7. Leakage Current vs Temperature**



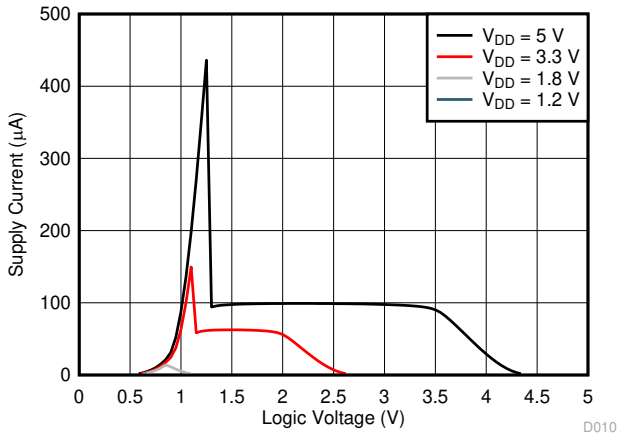

$V_{DD}$ = 5V

**Figure 6-8. Leakage Current vs Temperature**



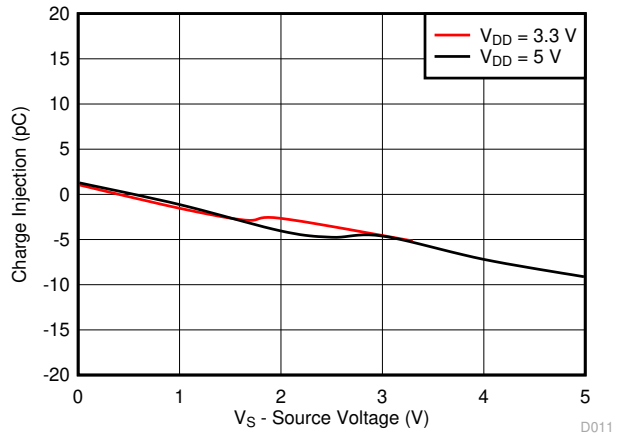

$V_{SEL}$ = 5.5V

**Figure 6-9. Supply Current vs Temperature**



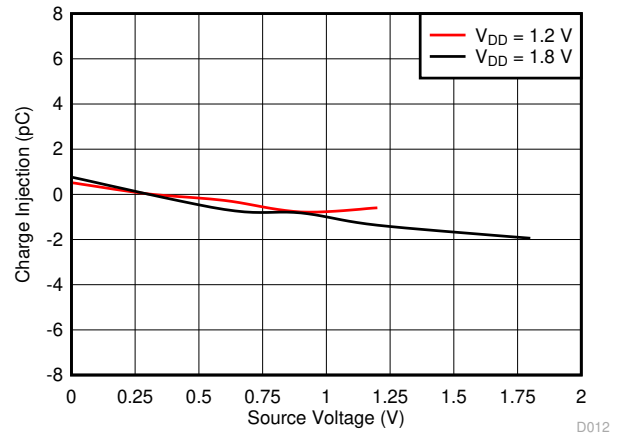

$T_A$ = 25°C

**Figure 6-10. Supply Current vs Logic Voltage**




$T_A$ = -40°C to 125°C

**Figure 6-11. Charge Injection vs Source Voltage**



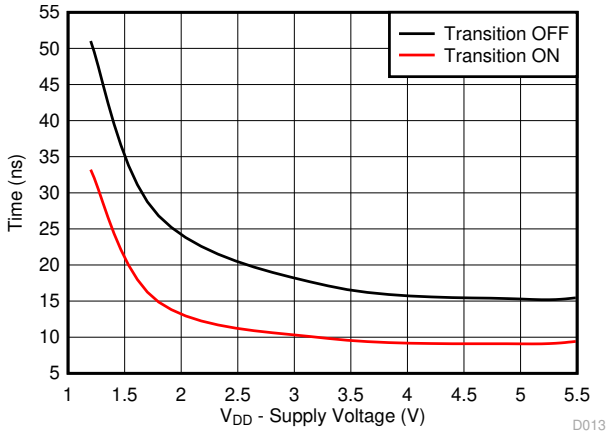

$T_A$ = –40°C to 125°C

**Figure 6-12. Charge Injection vs Source Voltage**


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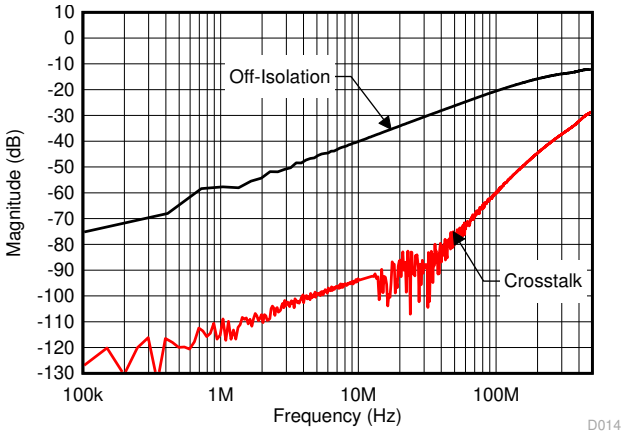
## 6.9 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_{DD}$ = 5V (unless otherwise noted)



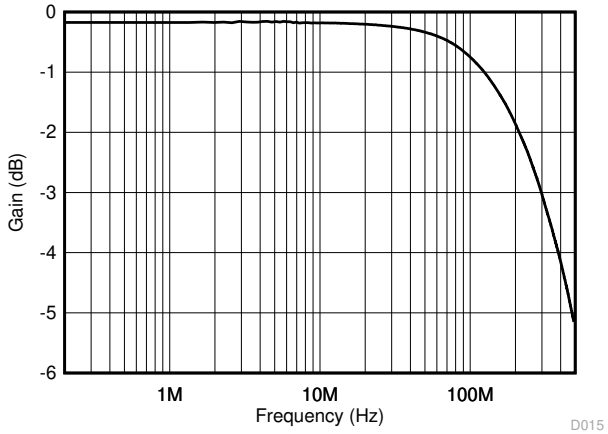

$T_A$ = -40°C to +125°C

**Figure 6-13. Output $T_{TRANSITION}$ vs Supply Voltage**




$T_A$ = -40°C to +125°C

**Figure 6-14. Off-Isolation vs Frequency**




$T_A$ = -40°C to +125°C

**Figure 6-15. On Response vs Frequency**

# 7 Parameter Measurement Information

## 7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol $R_{ON}$ is used to denote on-resistance. The measurement setup used to measure $R_{ON}$ is shown in Figure 7-1. Voltage (V) and current ($I_{SD}$) are measured using this setup, and $R_{ON}$ is computed with $R_{ON} = V / I_{SD}$:

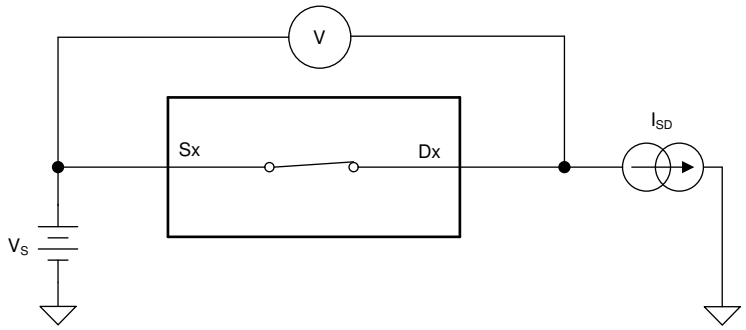



**Figure 7-1. On-Resistance Measurement Setup**

## 7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in Figure 7-2.

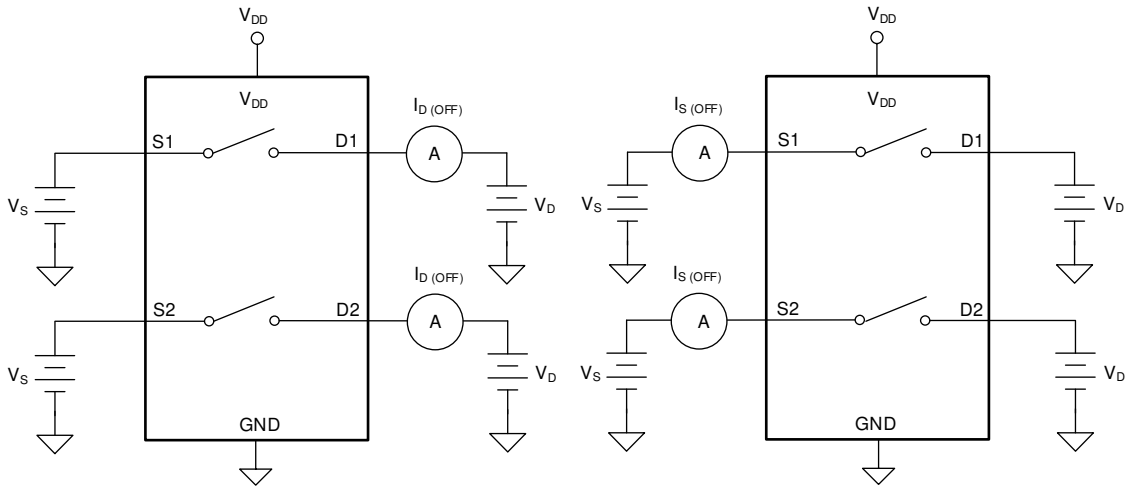



**Figure 7-2. Off-Leakage Measurement Setup**


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## 7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

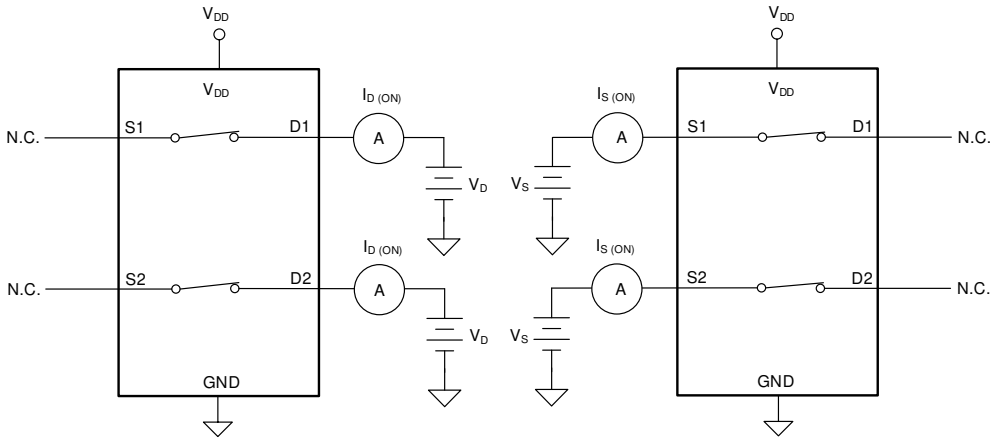



**Figure 7-3. On-Leakage Measurement Setup**

## 7.4 Transition time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

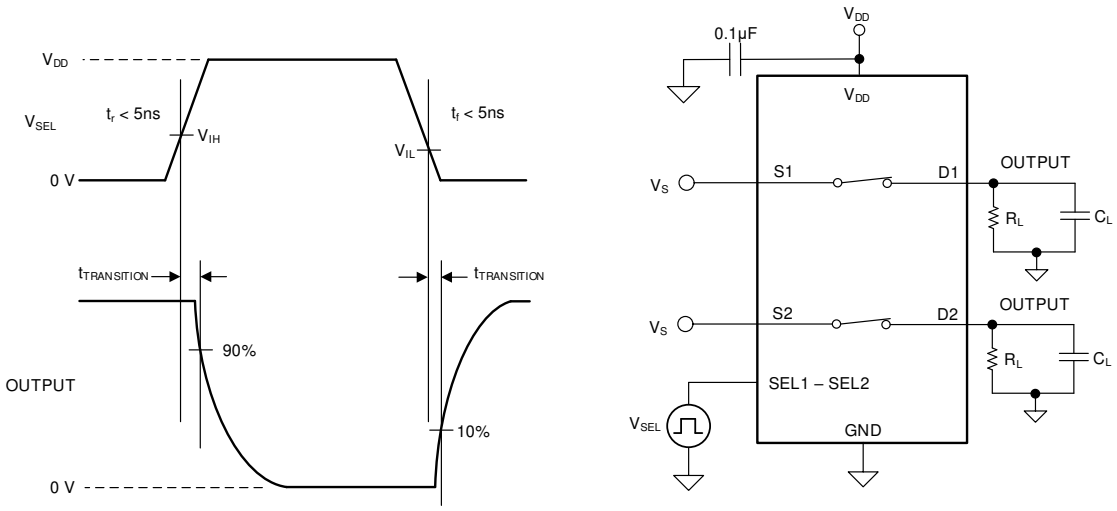



**Figure 7-4. Transition-Time Measurement Setup**

## 7.5 Break-Before-Make

The TMUX1123 has break-before-make delay which allows the device to be used in cross-point switching application. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 7-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

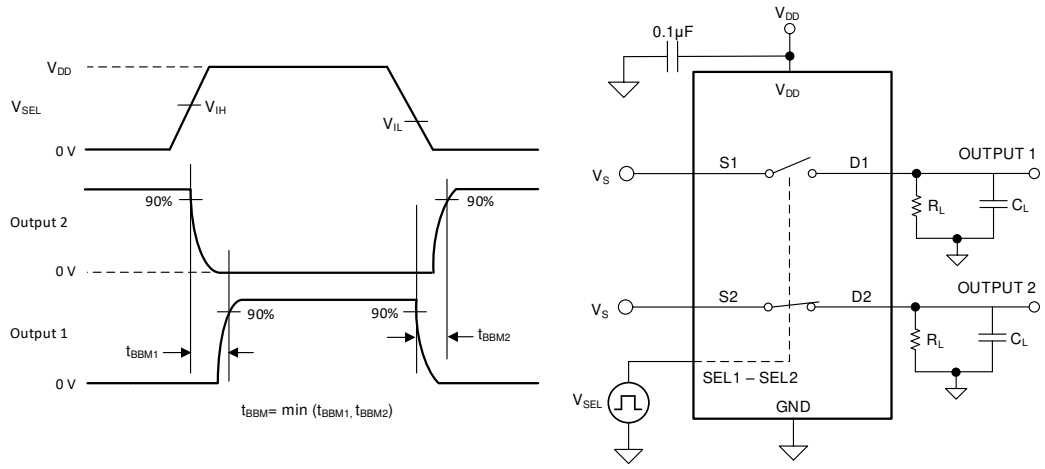



**Figure 7-5. Break-Before-Make Delay Measurement Setup**

## 7.6 Charge Injection

The TMUX112x devices have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol $Q_C$. Figure 7-6 shows the setup used to measure charge injection from source (Sx) to drain (Dx).

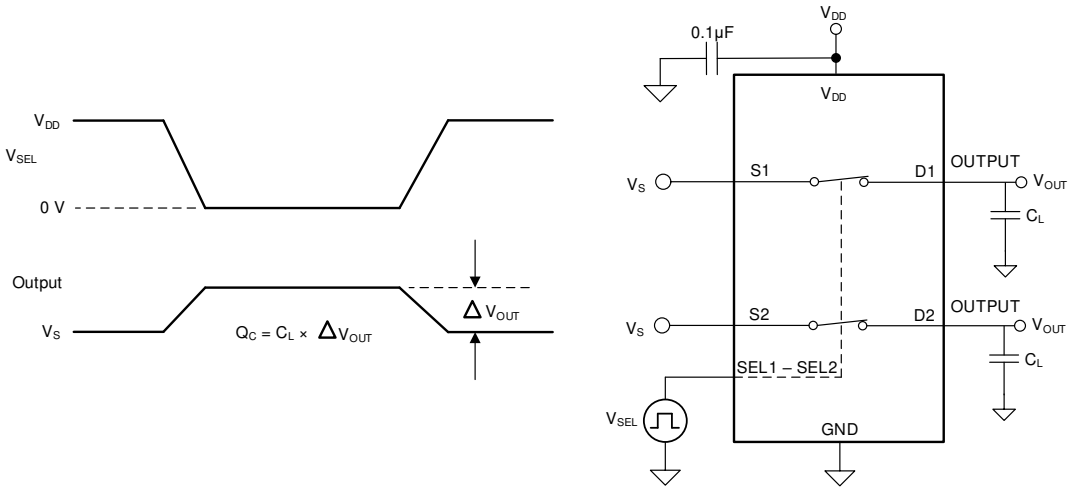



**Figure 7-6. Charge-Injection Measurement Setup**


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## 7.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, $Z_0$, for the measurement is 50Ω. Figure 7-7 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

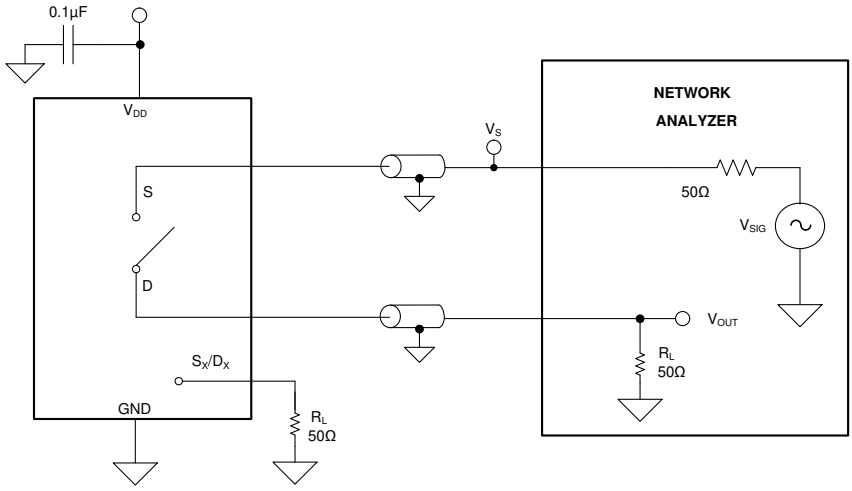



**Figure 7-7. Off Isolation Measurement Setup**

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

## 7.8 Channel-to-Channel Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, $Z_0$, for the measurement is 50Ω. Figure 7-8 shows the setup used to measure, and the equation used to compute crosstalk.

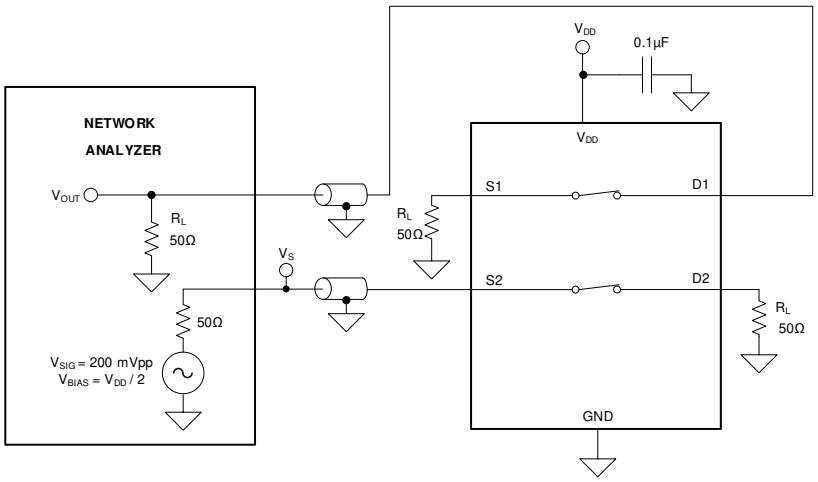



**Figure 7-8. Channel-to-Channel Crosstalk Measurement Setup**

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

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## 7.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, $Z_0$, for the measurement is 50Ω. Figure 7-9 shows the setup used to measure bandwidth.

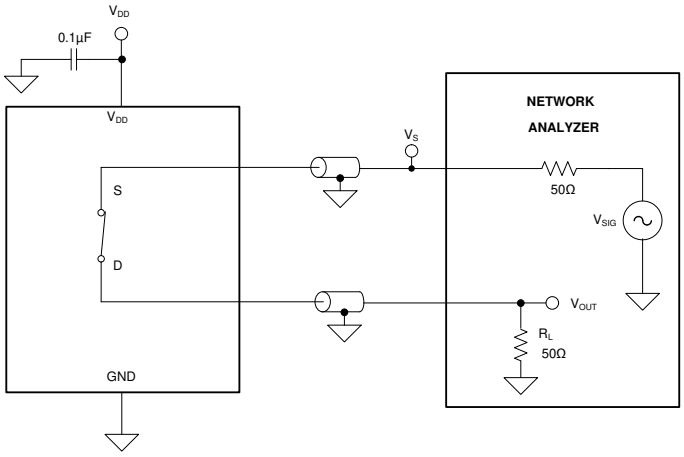



**Figure 7-9. Bandwidth Measurement Setup**

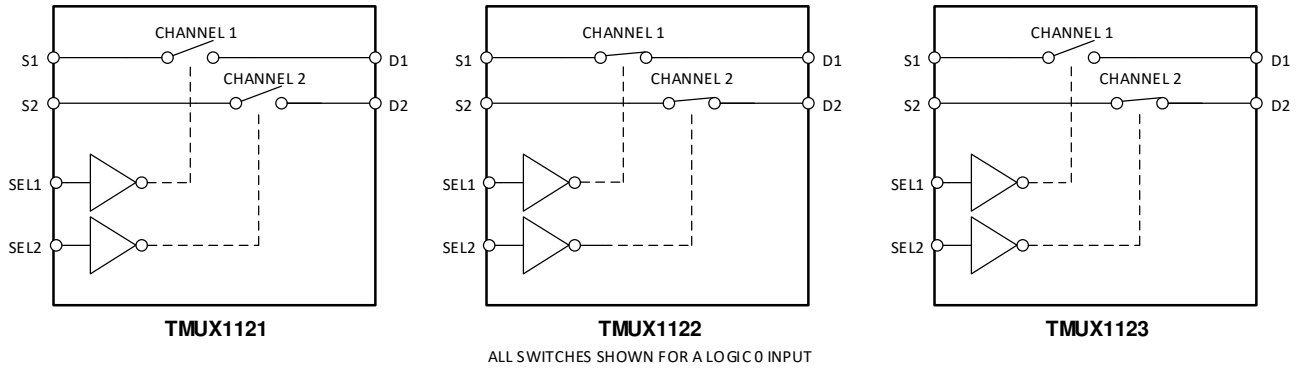

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# 8 Detailed Description

## 8.1 Overview

The TMUX1121, TMUX1122, and TMUX1123 are 1:1 (SPST), 2-Channel switches. The devices have two independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Bidirectional Operation

The TMUX112x conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

### 8.3.2 Rail-to-Rail Operation

The valid signal path input/output voltage for TMUX112x ranges from GND to $V_{DD}$.

### 8.3.3 1.8V Logic Compatible Inputs

The TMUX112x devices have 1.8V logic compatible control for all logic control inputs. The logic input thresholds scale with supply, but still provide 1.8V logic control when operating at 5.5V supply voltage. 1.8V logic level inputs allows the TMUX112x devices to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. The current consumption of the TMUX112x devices increase when using 1.8V logic with higher supply voltage as shown in Figure 6-10. For more information on 1.8V logic implementations refer to *Simplifying Design with 1.8V logic Muxes and Switches*

### 8.3.4 Fail-Safe Logic

The TMUX112x supports Fail-Safe Logic on the control input pins (EN, A0, A1) allowing for operation up to 5.5V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX112x to be ramped to 5.5V while $V_{DD}$ = 0V. Additionally, the feature enables operation of the TMUX112x with $V_{DD}$ = 1.2V while allowing the select pins to interface with a logic level of another device up to 5.5V.

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### 8.3.5 Ultra-Low Leakage Current

The TMUX112x devices provide extremely low on-leakage and off-leakage currents. The TMUX112x devices are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents. Figure 8-1 shows typical leakage currents of the TMUX112x devices versus temperature at $V_{DD}$ = 5V.

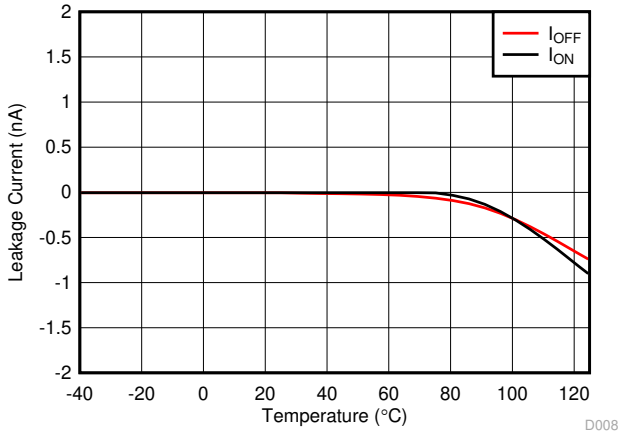



**Figure 8-1. Leakage Current vs Temperature**

### 8.3.6 Ultra-Low Charge Injection

The TMUX112x devices have a transmission gate topology, as shown in Figure 8-2. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

The TMUX112x devices have special charge-injection cancellation circuitry that reduces the source-to-drain charge injection to -1.5pC at $V_S$ = 1V as shown in Figure 8-3.

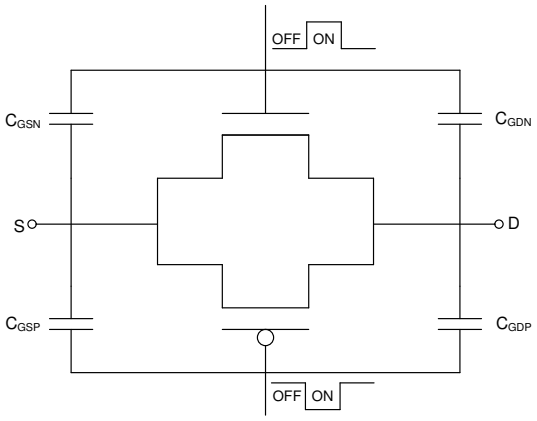



**Figure 8-2. Transmission Gate Topology**

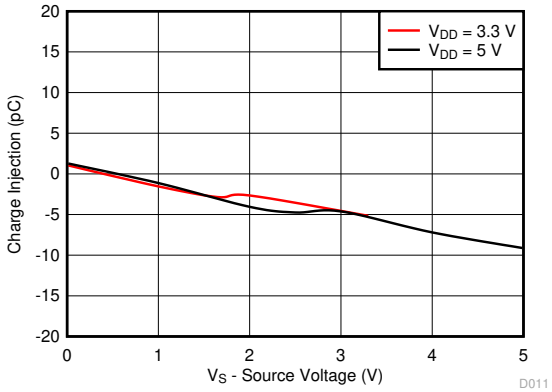



**Figure 8-3. Charge Injection vs Source Voltage**


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## 8.4 Device Functional Modes

The TMUX112x devices have two independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. The control pins can be as high as 5.5V.

The TMUX112x devices can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins should be tied to GND or $V_{DD}$ so that the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or Dx) should be connected to GND.

### 8.4.1 Truth Tables

Table 8-1, Table 8-2, and Table 8-3 list the truth tables for the TMUX1121, TMUX1122, and TMUX1123, respectively.

**Table 8-1. TMUX1121 Truth Table**

| SEL1(1) | SEL2 | CHANNEL STATE |
|---|---|---|
| 0 | X | Channel 1 OFF |
| 1 | X | Channel 1 ON |
| X | 0 | Channel 2 OFF |
| X | 1 | Channel 2 ON |

**Table 8-2. TMUX1122 Truth Table**

| SEL1 | SEL2 | CHANNEL STATE |
|---|---|---|
| 0 | X | Channel 1 ON |
| 1 | X | Channel 1 OFF |
| X | 0 | Channel 2 ON |
| X | 1 | Channel 2 OFF |

**Table 8-3. TMUX1123 Truth Table**

| SEL1 | SEL2 | CHANNEL STATE |
|---|---|---|
| 0 | X | Channel 1 OFF |
| 1 | X | Channel 1 ON |
| X | 0 | Channel 2 ON |
| X | 1 | Channel 2 OFF |

(1) X denotes *do not care*.

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# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The TMUX11xx family offers ultra-low input/output leakage currents and low charge injection. These devices operate up to 5.5V, and offer true rail-to-rail input and output of both analog and digital signals. The TMUX112x have a low on-capacitance which allows faster settling time when multiplexing inputs in the time domain. These features make the TMUX11xx devices a family of precision, high-performance switches and multiplexers for low-voltage applications.

## 9.2 Typical Application - Sample-and-Hold Circuit

One useful application to take advantage of the TMUX1121, TMUX1122, and TMUX1123 performance is the sample-and-hold circuit. A sample-and-hold circuit can be useful for an analog to digital converter (ADC) to sample a varying input voltage with improved reliability and stability. It can also be used to store the output samples from a single digital-to-analog converter (DAC) in a multi-output application. A simple sample-and-hold circuit can be realized using an analog switch such as the TMUX1121, TMUX1122, and TMUX1123 analog switches. Figure 9-1 shows a single channel sample-and hold circuit using only 1 of 2 channels in the TMUX112x devices.

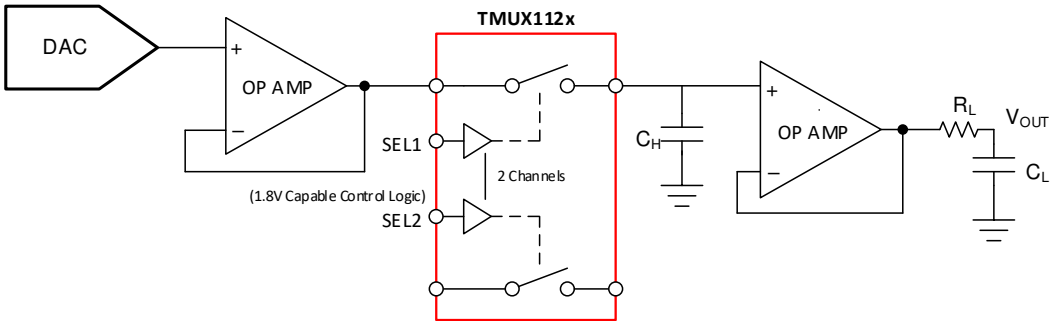



**Figure 9-1. Single Channel Sample-and-Hold Circuit Example**

An optional operational amplifier is used before the switch since buffered DACs typically have limitations in driving capacitive loads. The additional buffer stage is included following the DAC to prevent potential stability problems from driving a large capacitive load.

Ideally, the switch delivers only the input signals to the holding capacitors. However, when the switch gets toggled, some amount of charge also gets transferred to the switch output in the form of charge injection, resulting in a pedestal sampling error. The TMUX1121, TMUX1122, and TMUX1123 switches have excellent charge injection performance of only -1.5pC, making them an excellent choice for minimizing sampling errors in this implementation. The pedestal error voltage is indirectly related to the size of the capacitance on the output, for better precision a larger capacitor is required due to charge injection. Larger capacitance limits the system settling time which may not be acceptable in some applications. Figure 9-2 shows a TMUX112x device configured for a 2-channel sample-and-hold circuit with pedestal error compensation.


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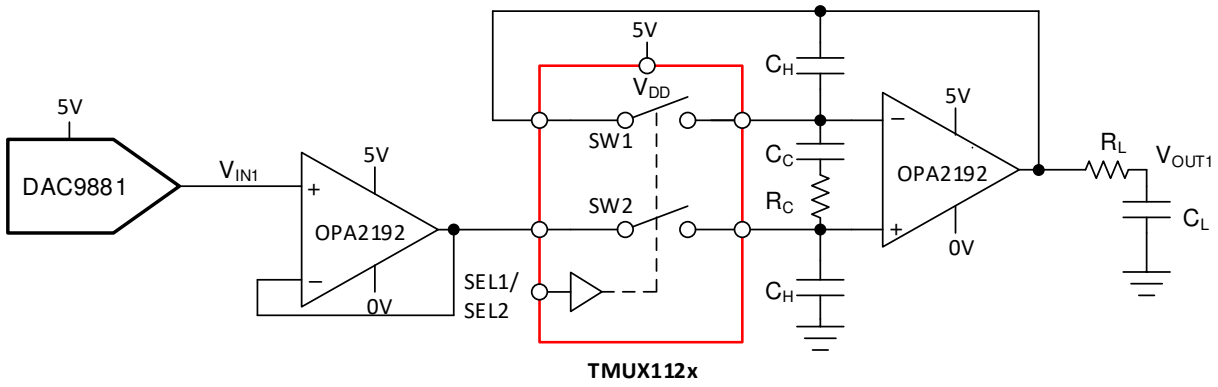



**Figure 9-2. 2-Channel Sample-and-Hold Circuit with Pedestal Error Compensation**

### 9.2.1 Design Requirements

The purpose of this precision design is to implement an optimized 2-output sample-and-hold circuit using a 2-channel 1:1 (SPST) switch. The sample and hold circuit needs to be capable of supporting high accuracy with minimized pedestal error and fast settling time.

### 9.2.2 Detailed Design Procedure

The TMUX1121, TMUX1122, or TMUX1123 switch is used in conjunction with the voltage holding capacitors ($C_H$) to implement the sample-and-hold circuit. The basic operation is:

1. When the switch (SW2) is closed, it samples the input voltage and charges the holding capacitors ($C_H$) to the input voltages values.
2. When the switch (SW2) is open, the holding capacitors ($C_H$) holds its previous value, maintaining stable voltage at the amplifier output ($V_{OUT}$).

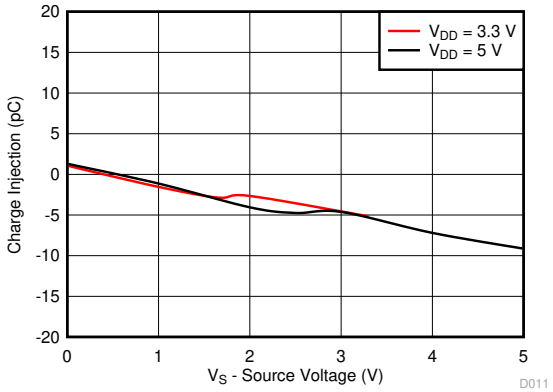
Due to switch and capacitor leakage current, as well as amplifier bias current, the voltage on the hold capacitors droops with time. The TMUX1121, TMUX1122, or TMUX1123 minimize the droops due to its ultra-low leakage performance. At 25°C, the TMUX1121, TMUX1122, and TMUX1123 have extremely low leakage current at 3pA typical.

A second switch SW1 is also included to operate in parallel with SW2 to reduce pedestal error during switch toggling. Because both switches are driven at the same potential, they act as common-mode signal to the op-amp, thereby minimizing the charge injection effects caused by the switch toggling action. Compensation network consisting of $R_C$ and $C_C$ is also added to further reduce the pedestal error, whiling reducing the hold-time glitch and improving the settling time of the circuit. Refer to *Sample and Hold Glitch Reduction for Precision Outputs Reference Design* for more information on sample-and-hold circuits.

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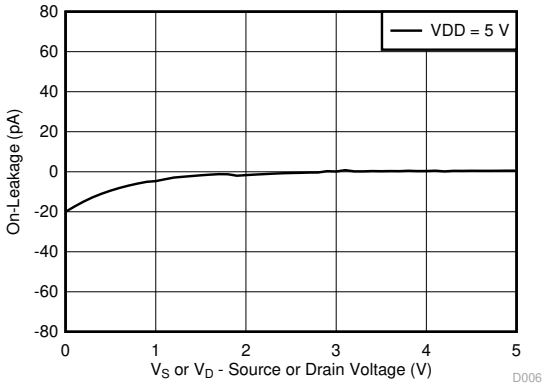
### 9.2.3 Application Curve

TMUX1121, TMUX1122, andTMUX1123 have excellent charge injection performance and ultra-low leakage current, making them ideal choices to minimize sampling error for the sample and hold application.




$T_A$ = -40°C to +125°C

**Figure 9-3. Charge Injection vs Source Voltage**




$V_{DD}$= 5V

**Figure 9-4. On-Leakage vs Source or Drain Voltage**

## 9.3 Typical Application - Switched Gain Amplifier

Switches and multiplexers are commonly used in the feedback path of amplifier circuits to provide configurable gain control. By using various resistor values on each switch path, the TMUX112x allows the system to have multiple gain settings. An external resistor, or utilizing 1 channel that is always closed, causes the amplifier to not operate in an open loop configuration. A transimpedance amplifier (TIA) for photodiode inputs is a common circuit that requires gain control using a multi-channel switch to convert the output current of the photodiode into a voltage for the MCU or processor. The leakage current, capacitance, and charge injection performance of the TMUX112x are key specifications to evaluate when selecting a device for gain control.

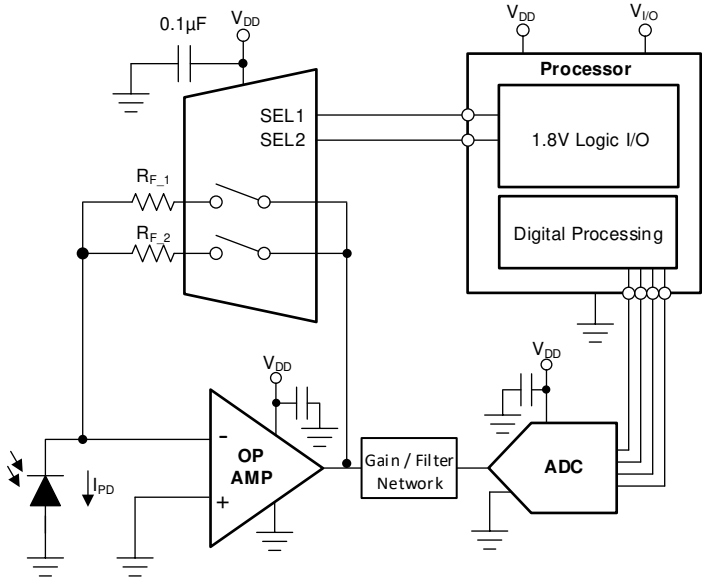



**Figure 9-5. Switching Gain Settings of a TIA Circuit**


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### 9.3.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

**Table 9-1. Design parameters**

| PARAMETERS | VALUES |
|---|---|
| Supply ($V_{DD}$) | 3.3V |
| Input / Output signal range | 0 µA to 10 µA |
| Control logic thresholds | 1.8V compatible |

### 9.3.2 Detailed Design Procedure

The TMUX112x devices can be operated without any external components except for the supply decoupling capacitors. All inputs signals passing through the switch must fall within the recommend operating conditions of the TMUX112x including signal range and continuous current. For this design example, with a supply of 3.3V, the signals can range from 0V to 3.3V when the device is powered. The maximum continuous current can be 30mA.

Photodiodes commonly have a current output that ranges from a few hundred picoamps to tens of microamps based on the amount of light being absorbed. The TMUX112x have a typical On-leakage current of less than 10pA which would lead to an accuracy well within 1% of a full scale 10 µA signal. The low ON and OFF capacitance of the TMUX112x improves system stability by minimizing the total capacitance on the output of the amplifier. Lower capacitance leads to less overshoot and ringing in the system which can cause the amplifier circuit to go unstable if the phase margin is not at least 45°. Refer to *Improve Stability Issues with Low $C_{ON}$ Multiplexers* for more information on calculating the phase margin versus percent overshoot.

### 9.3.3 Application Curve

The TMUX1121 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents.

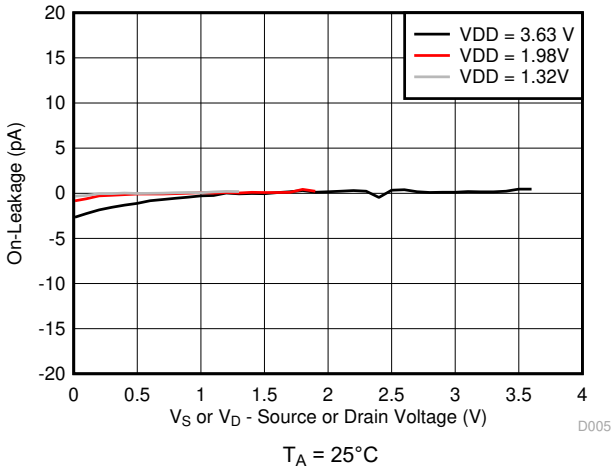



**Figure 9-6. On-Leakage vs Source or Drain Voltage**

## 9.4 Power Supply Recommendations

The TMUX112x operate across a wide supply range of 1.08V to 5.5V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the $V_{DD}$ supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF from $V_{DD}$ to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

## 9.5 Layout

### 9.5.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight, and therefore; some traces must turn corners. Figure 9-7 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

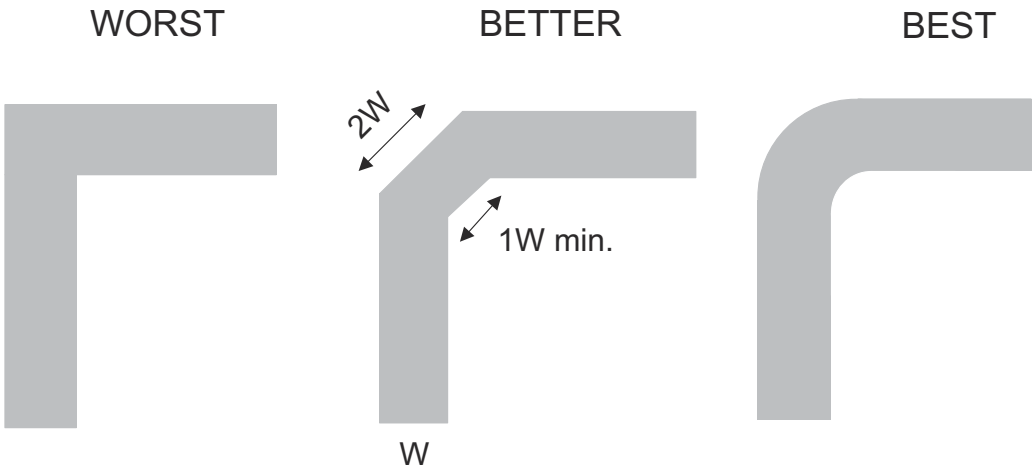



**Figure 9-7. Trace Example**

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.


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Figure 9-8 shows an example of a PCB layout with the TMUX112x. Some key considerations are:

- Decouple the $V_{DD}$ pin with a 0.1µF capacitor, placed as close to the pin as possible. Ensure that the capacitor voltage rating is sufficient for the $V_{DD}$ supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

### 9.5.2 Layout Example

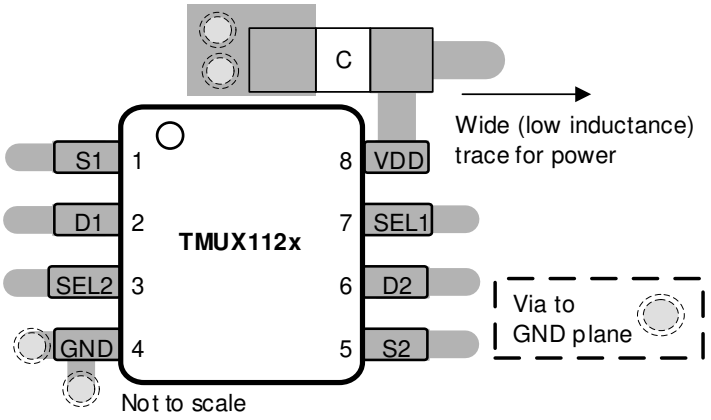



**Figure 9-8. TMUX112x Layout Example**

# 10 Device and Documentation Support

## 10.1 Documentation Support

### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Sample and Hold Glitch Reduction for Precision Outputs Reference Design*.
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit*.
- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.
- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches*.
- Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*.

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 10.4 Trademarks

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All trademarks are the property of their respective owners.

## 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (September 2019) to Revision B (February 2024) | Page |
|---|---|
| • Updated Is or Id (Continuous Current) values | 4 |
| • Added Ipeak values to *Recommended Operating Conditions* table | 4 |

| Changes from Revision * (August 2019) to Revision A (September 2019) | Page |
|---|---|
| • Changed the document From: *Advanced Information* To: *Production* data | 1 |


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## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TMUX1121DGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 121 |
| TMUX1121DGKR.A | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 121 |
| TMUX1122DGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 122 |
| TMUX1122DGKR.A | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 122 |
| TMUX1123DGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 123 |
| TMUX1123DGKR.A | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 123 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

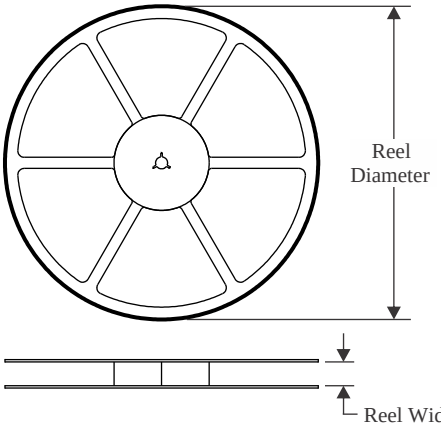
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

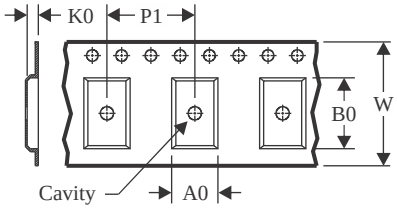
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

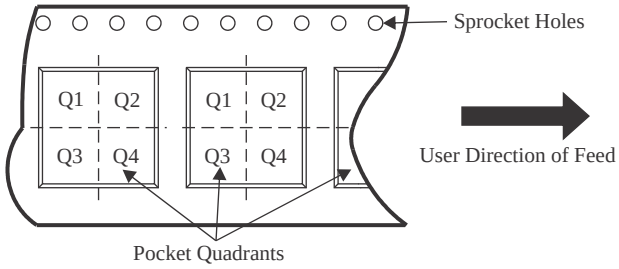



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

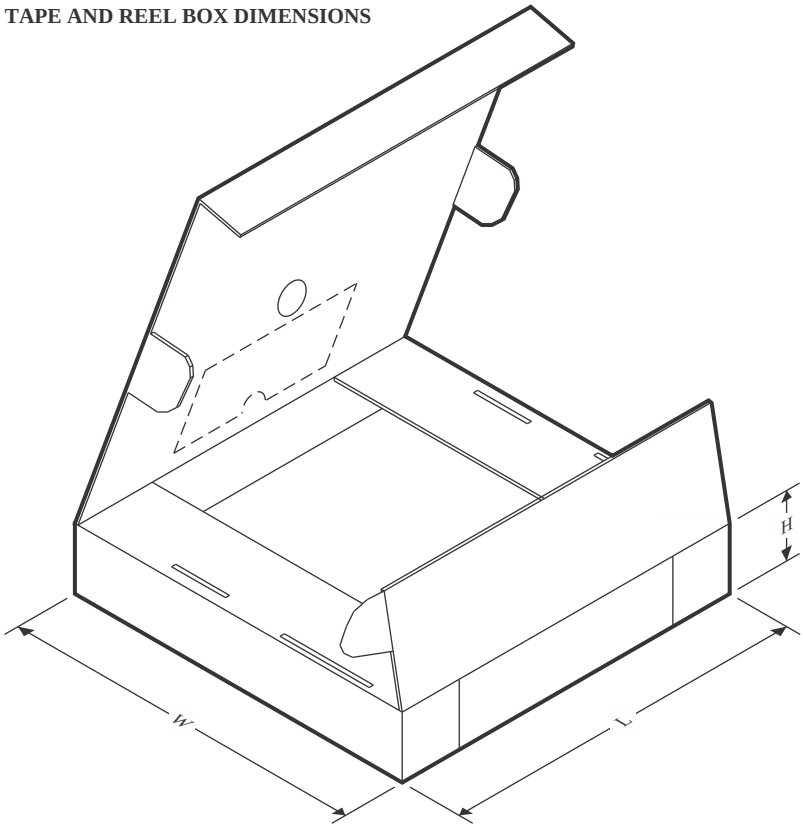
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMUX1121DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TMUX1121DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TMUX1122DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TMUX1123DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TMUX1123DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

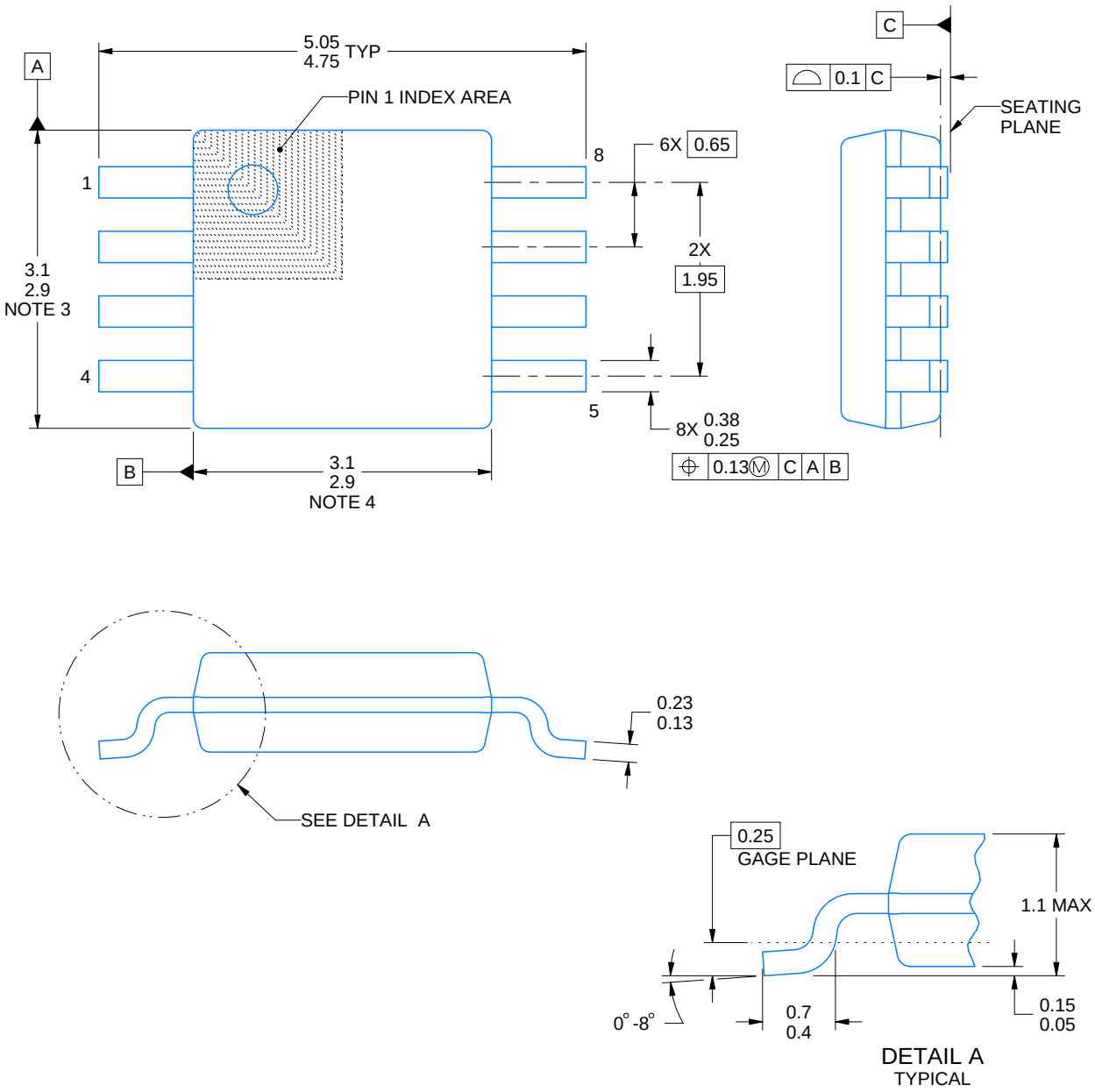
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMUX1121DGKR | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TMUX1121DGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TMUX1122DGKR | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TMUX1123DGKR | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TMUX1123DGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

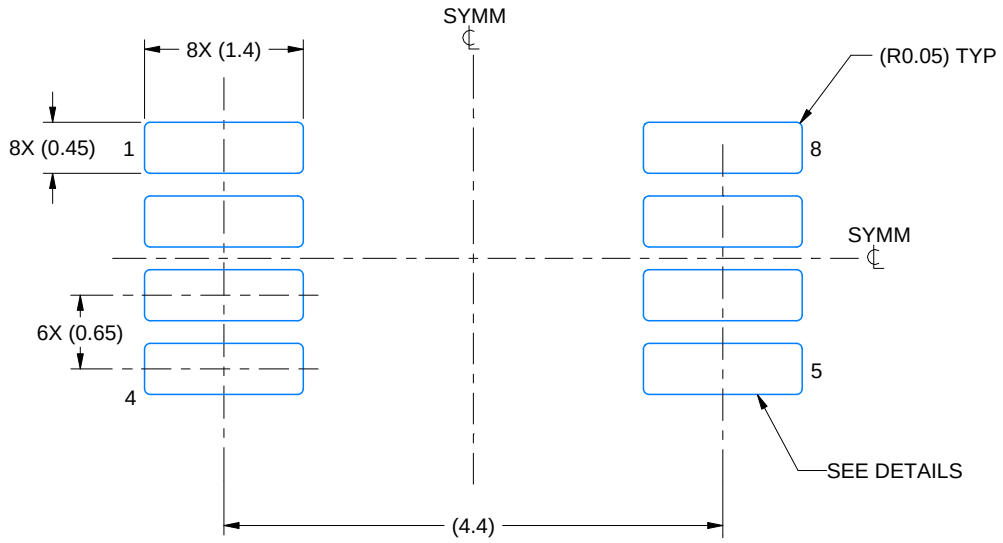
SMALL OUTLINE PACKAGE



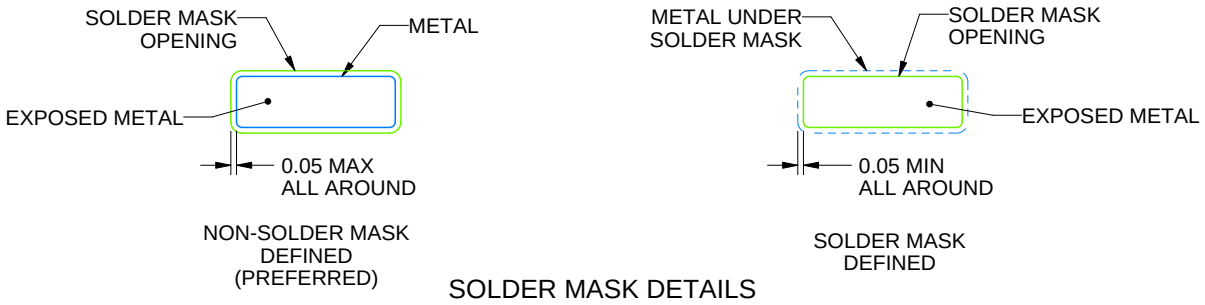

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

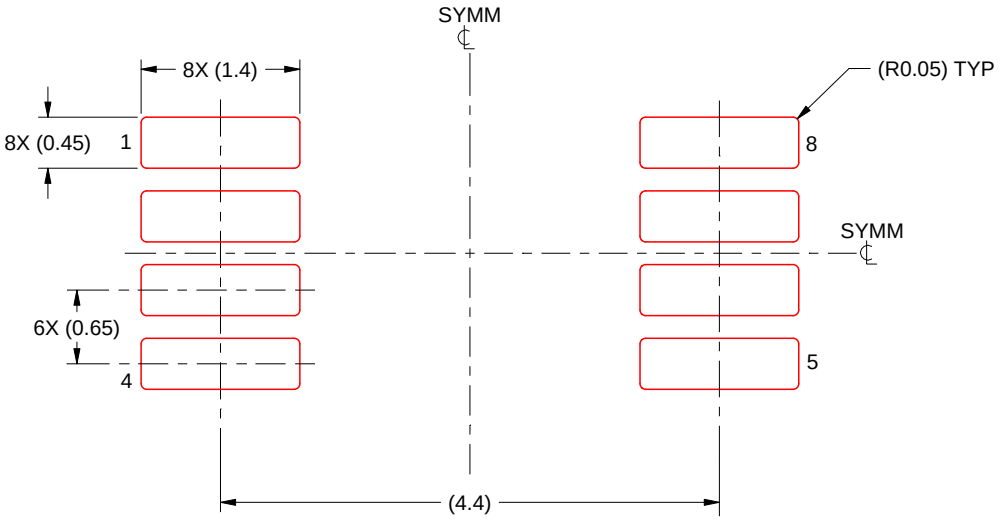



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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