One Output, Integrated VCO, Low-Jitter Clock Generator

Check for Samples: CDCM61001

FEATURES

- **One Crystal/LVCMOS Reference Input Including 24.8832 MHz, 25 MHz, and 26.5625 MHz**
- **Input Frequency Range: 21.875 MHz to 28.47 MHz**
- **On-Chip VCO Operates in Frequency Range of 1.75 GHz to 2.05 GHz**
- **1x Output Available:**
  - **Pin-Selectable Between LVPECL, LVDS, or 2-LVCMOS; Operates at 3.3 V**
- **LVCMOS Bypass Output Available**
- **Output Frequency Selectable by /1, /2, /3, /4, /6, /8 from the Output Divider**
- **Supports Common LVPECL/LVDS Output Frequencies:**
  - **62.5 MHz, 74.25 MHz, 75 MHz, 77.76 MHz, 100 MHz, 106.25 MHz, 125 MHz, 150 MHz, 155.52 MHz, 156.25 MHz, 159.375 MHz, 187.5 MHz, 200 MHz, 212.5 MHz, 250 MHz, 311.04 MHz, 312.5 MHz, 622.08 MHz, 625 MHz**
- **Supports Common LVCMOS Output Frequencies:**
  - **62.5 MHz, 74.25 MHz, 75 MHz, 77.76 MHz, 100 MHz, 106.25 MHz, 125 MHz, 150 MHz, 155.52 MHz, 156.25 MHz, 159.375 MHz, 187.5 MHz, 200 MHz, 212.5 MHz, 250 MHz**
- **Output Frequency Range: 43.75 MHz to 683.264 MHz (See Table 3)**
- **Internal PLL Loop Bandwidth: 400 kHz**
- **High-Performance PLL Core:**
  - **Phase Noise typically at –146 dBc/Hz at 5-MHz Offset for 625-MHz LVPECL Output**
  - **Random Jitter typically at 0.509 ps, RMS (10 kHz to 20 MHz) for 625-MHz LVPECL Output**
- **Output Duty Cycle Corrected to 50% (± 5%)**
- **Divider Programming Using Control Pins:**
  - **Two Pins for Prescaler/Feedback Divider**
  - **Three Pins for Output Divider**
  - **Two Pins for Output Select**
- **Chip Enable and Device Reset Control Pins Available**
- **3.3-V Core and I/O Power Supply**
- **Industrial Temperature Range: –40°C to +85°C**
- **5-mm × 5-mm, 32-pin, QFN (RHB) Package**
- **ESD Protection Exceeds 2 kV (HBM)**

APPLICATIONS

- **Low Jitter Clock Driver for High-End Datacom Applications Including SONET, Ethernet, Fibre Channel, Serial ATA, and HDTV**
- **Cost-Effective High-Frequency Crystal Oscillator Replacement**

DESCRIPTION

The CDCM61001 is a highly versatile, low-jitter frequency synthesizer that can generate low-jitter clock outputs, selectable between low-voltage positive emitter coupled logic (LVPECL), low-voltage differential signaling (LVDS), or low-voltage complementary metal oxide semiconductor (LVCMOS) outputs, from a low-frequency crystal or LVCMOS input for a variety of wireline and data communication applications. The CDCM61001 features an onboard PLL that can be easily configured solely through control pins. The overall output random jitter performance is less than 1ps, RMS (from 10 kHz to 20 MHz), making this device a perfect choice for use in demanding applications such as SONET, Ethernet, Fibre Channel, and SAN. The CDCM61001 is available in a small, 32-pin, 5-mm × 5-mm QFN package.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION, CONTINUED

The CDCM61001 is a high-performance, low phase noise, fully-integrated voltage-controlled oscillator (VCO) clock synthesizer with one universal output buffer that can be configured to be LVPECL, LVDS, or LVCMOS compatible. The universal output can also be converted to two LVCMOS outputs. Additionally, an LVCMOS bypass output clock is available in an output configuration which can help with crystal loading in order to achieve an exact desired input frequency. It has one fully-integrated, low-noise, LC-based VCO that operates in the 1.75 GHz to 2.05 GHz range.

The phase-locked loop (PLL) synchronizes the VCO with respect to the input, which can either be a low-frequency crystal. The output has an output divider sourced from the VCO core. All device settings are managed through a control pin structure, which has two pins that control the prescaler and feedback divider, three pins that control the output divider, two pins that control the output type, and one pin that controls the output enable. Any time the PLL settings (including the input frequency, prescaler divider, or feedback divider) are altered, a reset must be issued through the Reset control pin (active low for device reset). The reset initiates a PLL recalibration process to ensure PLL lock. When the device is in reset, the outputs and divider are turned off.

The output frequency (f_{OUT}) is proportional to the frequency of the input clock (f_{IN}). The feedback divider, output divider, and VCO frequency set f_{OUT} with respect to f_{IN}. For a configuration setting for common wireline and datacom applications, refer toTable 2. For other applications, use Equation 1 to calculate the exact crystal oscillator frequency required for the desired output.

$$f_{IN} = \left(\frac{\text{Output Divider}}{\text{Feedback Divider}}\right) f_{OUT} \tag{1}$$

The output divider can be chosen from 1, 2, 3, 4, 6, or 8 through the use of control pins. Feedback divider and prescaler divider combinations can be chosen from 25 and 3, 24 and 3, 20 and 4, or 15 and 5, respectively, also through the use of control pins. Figure 1 shows a high-level block diagram of the CDCM61001.

The device operates in a 3.3-V supply environment and is characterized for operation from –40°C to +85°C.

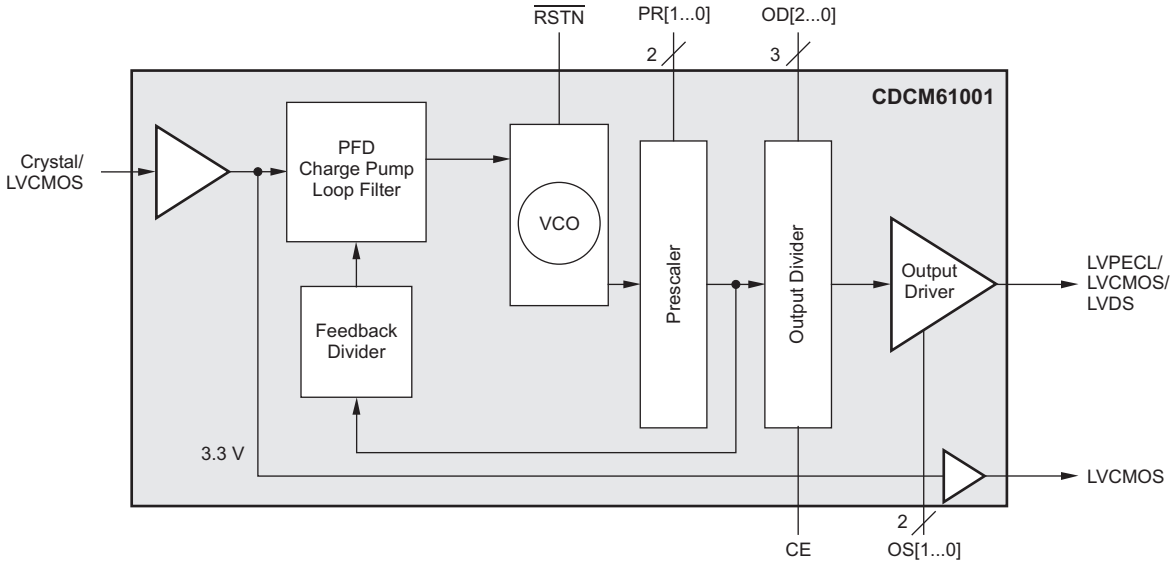

Figure 1. CDCM61001 Block Diagram

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AVAILABLE OPTIONS[1]

T_A	PACKAGED DEVICES	FEATURES[2]
–40°C to +85°C	CDCM61001RHBT	32-pin QFN (RHB) package, small tape and reel
	CDCM61001RHBR	32-pin QFN (RHB) package, tape and reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at ti.com.
(2) These packages conform to Lead (Pb)-free and green manufacturing specifications. Additional details including specific material content can be accessed at www.ti.com/leadfree. GREEN: TI defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1%of total product weight. N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree. Pb-FREE: TI defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		VALUE	UNIT
V_{CC_OUT}, V_{CC_PLL1}, V_{CC_PLL2}, V_{CC_VCO}, V_{CC_IN}	Supply voltage range[2]	–0.5 to +4.6	V
V_{IN}	Input voltage range[3]	–0.5 to (V_{CC_IN} + 0.5)	V
V_{OUT}	Output voltage range[3]	–0.5 to (V_{CC_OUT} + 0.5)	V
I_{IN}	Input current	20	mA
I_{OUT}	Output current	50	mA
T_{STG}	Storage temperature range	–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating condition* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All supply voltages must be supplied simultaneously.
(3) Input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC_OUT}	Output supply voltage	3.0	3.30	3.60	V
V_{CC_PLL1}	PLL supply voltage	3.0	3.30	3.60	V
V_{CC_PLL2}	PLL supply voltage	3.0	3.30	3.60	V
V_{CC_VCO}	On-chip VCO supply voltage	3.0	3.30	3.60	V
V_{CC_IN}	Input supply voltage	3.0	3.30	3.60	V
T_A	Ambient temperature	–40		+85	°C

DISSIPATION RATINGS[1][2]

PARAMETER		TEST CONDITIONS	VALUE 4 × 4 VIAS ON PAD	UNIT
θ_{JA}	Thermal resistance, junction-to-ambient	0 LFM	35	°C/W
θ_{JP}[3]	Thermal resistance, junction-to-pad		4	°C/W

(1) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC 2S2P (high-K board).
(2) Connected to GND with nine thermal vias (0.3-mm diameter).
(3) θ_{JP} (junction-to-pad) is used for the QFN package, because the primary heat flow is from the junction to the GND pad of the QFN package.

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ELECTRICAL CHARACTERISTICS

At V_{CC} = 3 V to 3.6 V and T_A = –40°C to +85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	CDCM61001 MIN	CDCM61001 TYP	CDCM61001 MAX	UNIT
Control Pin LVCMOS Input Characteristics						
V_{IH}	Input high voltage		$0.6V_{CC}$			V
V_{IL}	Input low voltage				$0.4V_{CC}$	V
I_{IH}	Input high current	V_{CC} = 3.6 V, V_{IL} = 0 V			200	µA
I_{IL}	Input low current	V_{CC} = 3 V, V_{IH} = 3.6 V			–200	µA
LVCMOS Output Characteristics(1) (See Figure 9 and Figure 10)						
f_{OSC_OUT}	Bypass output frequency		21.875		28.47	MHz
f_{OUT}	Output frequency		43.75		250	MHz
V_{OH}	Output high voltage	V_{CC} = min to max, I_{OH} = –100 µA	V_{CC} –0.5			V
V_{OL}	Output low voltage	V_{CC} = min to max, I_{OL} = 100 µA			0.3	V
t_{RJIT}	RMS phase jitter	250 MHz (10 kHz to 20 MHz)			0.85	ps, RMS
$t_{SLEW-RATE}$	Output rise/fall slew rate	20% to 80%	2.4			V/ns
ODC	Output duty cycle		45%		55%	
I_{CC}, LVCMOS	Device current, LVCMOS	f_{IN} = 25 MHz, f_{OUT} = 250 MHz, C_L = 5 pF		95	110	mA
LVPECL Output Characteristics(2) (See Figure 11 and Figure 12)						
f_{OUT}	Output frequency		43.75		683.264	MHz
V_{OH}	Output high voltage		V_{CC} –1.18		V_{CC} –0.73	V
V_{OL}	Output low voltage		V_{CC} –2		V_{CC} –1.55	V
$\|V_{OD}\|$	Differential output voltage		0.6		1.23	V
t_{RJIT}	RMS phase jitter	625 MHz (10 kHz to 20 MHz)			0.77	ps, RMS
t_R/t_F	Output rise/fall time	20% to 80%			175	ps
ODC	Output duty cycle		45%		55%	
I_{CC}, LVPECL	Device current, LVPECL	f_{IN} = 25 MHz, f_{OUT} = 625 MHz		100	115	mA
LVDS Output Characteristics(3) (See Figure 13 and Figure 14)						
f_{OUT}	Output frequency		43.75		683.264	MHz
$\|V_{OD}\|$	Differential output voltage		0.247		0.454	V
ΔV_{OD}	V_{DD} magnitude change				50	mV
V_{OS}	Common-mode voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} magnitude change				50	mV
t_{RJIT}	RMS phase jitter	625 MHz (10 kHz to 20 MHz)			0.73	ps, RMS
t_R/t_F	Output rise/fall time	20% to 80%			255	ps
ODC	Output duty cycle		45%		55%	
I_{CC}, LVDS	Device current, LVDS	f_{IN} = 25 MHz, f_{OUT} = 625 MHz		90	105	mA

(1) Figure 9 and Figure 10 show dc and ac test setups, respectively. Jitter measurements made using 25-MHz quartz crystal in.
(2) Figure 11 and Figure 12 show dc and ac test setups, respectively. Jitter measurements made using 25-MHz quartz crystal in.
(3) Figure 13 and Figure 14 show dc and ac test setups, respectively. Jitter measurements made using 25-MHz quartz crystal in.

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TYPICAL OUTPUT PHASE NOISE CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	CDCM61001 MIN	CDCM61001 TYP	CDCM61001 MAX	UNIT
250-MHz LVCMOS Output[(1)] (see Figure 10)						
phn_{100}	Phase noise at 100-Hz offset			–95		dBc/Hz
phn_{1k}	Phase noise at 1-kHz offset			–110		dBc/Hz
phn_{10k}	Phase noise at 10-kHz offset			–117		dBc/Hz
phn_{100k}	Phase noise at 100-kHz offset			–120		dBc/Hz
phn_{1M}	Phase noise at 1-MHz offset			–135		dBc/Hz
phn_{10M}	Phase noise at 10-MHz offset			–148		dBc/Hz
phn_{20M}	Phase noise at 20-MHz offset			–148		dBc/Hz
t_{RJIT}	RMS phase jitter from 10 kHz to 20 MHz			544		fs, RMS
t_{PJIT}	Total period jitter			27.4		ps, PP
$t_{STARTUP}$	Start-up time, power supply ramp time of 1 ms, final frequency accuracy of ±10 ppm			2.25		ms
625-MHz LVPECL Output[(2)] (see Figure 12)						
phn_{100}	Phase noise at 100-Hz offset			–81		dBc/Hz
phn_{1k}	Phase noise at 1-kHz offset			–101		dBc/Hz
phn_{10k}	Phase noise at 10-kHz offset			–109		dBc/Hz
phn_{100k}	Phase noise at 100-kHz offset			–112		dBc/Hz
phn_{1M}	Phase noise at 1-MHz offset			–129		dBc/Hz
phn_{10M}	Phase noise at 10-MHz offset			–146		dBc/Hz
phn_{20M}	Phase noise at 20-MHz offset			–146		dBc/Hz
t_{RJIT}	RMS phase jitter from 10 kHz to 20 MHz			509		fs, RMS
t_{PJIT}	Total period jitter			26.9		ps, PP
$t_{STARTUP}$	Start-up time, power supply ramp time of 1 ms, final frequency accuracy of ±10 ppm			2.25		ms
625-MHz LVDS Output[(3)] (see Figure 14)						
phn_{100}	Phase noise at 100-Hz offset			–88		dBc/Hz
phn_{1k}	Phase noise at 1-kHz offset			–102		dBc/Hz
phn_{10k}	Phase noise at 10-kHz offset			–109		dBc/Hz
phn_{100k}	Phase noise at 100-kHz offset			–112		dBc/Hz
phn_{1M}	Phase noise at 1-MHz offset			–129		dBc/Hz
phn_{10M}	Phase noise at 10-MHz offset			–146		dBc/Hz
phn_{20M}	Phase noise at 20-MHz offset			–146		dBc/Hz
t_{RJIT}	RMS phase jitter from 10 kHz to 20 MHz			510		fs, RMS
t_{PJIT}	Total period jitter			27		ps, PP
$t_{STARTUP}$	Start-up time, power supply ramp time of 1 ms, final frequency accuracy of ±10 ppm			2.25		ms

(1) Figure 10 shows test setup and uses 25-MHz quartz crystal in, V_{CC} = 3.3 V, T_A = +25°C, and C_L = 5 pF.
(2) Figure 12 shows test setup and uses 25-MHz quartz crystal in, V_{CC} = 3.3 V, and T_A = +25°C.
(3) Figure 14 shows test setup and uses 25-MHz quartz crystal in, V_{CC} = 3.3 V, and T_A = +25°C.

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TYPICAL OUTPUT JITTER CHARACTERISTICS(1)

OUTPUT FREQUENCY (MHz)	INPUT (MHz)	LVCMOS OUTPUT		LVPECL OUTPUT		LVDS OUTPUT	
		t_{RJIT} (fs, RMS)	t_{PJIT} (ps_{PP})	t_{RJIT} (fs, RMS)	t_{PJIT} (ps_{PP})	t_{RJIT} (fs, RMS)	t_{PJIT} (ps_{PP})
62.5	25	592	32.9	611	20.7	667	28.4
75	25	518	27.5	533	19.4	572	25.7
77.76	24.8832	506	29.2	526	20.9	567	26.9
100	25	507	24.5	510	20.7	533	26.5
106.25	26.5625	535	23.5	524	20.2	553	26.5
125	25	557	39.6	556	21.4	570	27.1
150	25	518	38.4	493	18.9	515	26.2
155.52	24.8832	498	36.9	486	19.8	502	26.7
156.25	25	510	37.7	503	20.7	518	26.5
159.375	26.5625	535	37.4	510	19.9	534	26.3
187.5	25	506	32.8	506	20.3	509	25.5
200	25	491	23.3	492	30	499	34.9
212.5	26.5625	520	47.8	509	30.8	530	37.3
250	25	544	27.4	541	21.4	550	27.5
311.04	24.8832			481	20.5	496	24.7
312.5	25			501	20.8	508	25.8
622.08	24.8832			492	27.2	500	27.2
625	25			515	26.9	509	27

(1) Figure 10, Figure 12, and Figure 14 show LVCMOS, LVPECL, and LVDS test setups (respectively) using appropriate quartz crystal in, V_{CC} = 3.3 V, and T_A = +25°C.

CRYSTAL CHARACTERISTICS

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
Mode of oscillation		Fundamental		MHz
Frequency	21.875		28.47	MHz
Equivalent series resistance (ESR)			50	Ω
On-chip load capacitance		8	10	pF
Drive level	0.1		1	mW
Maximum shunt capacitance			7	pF

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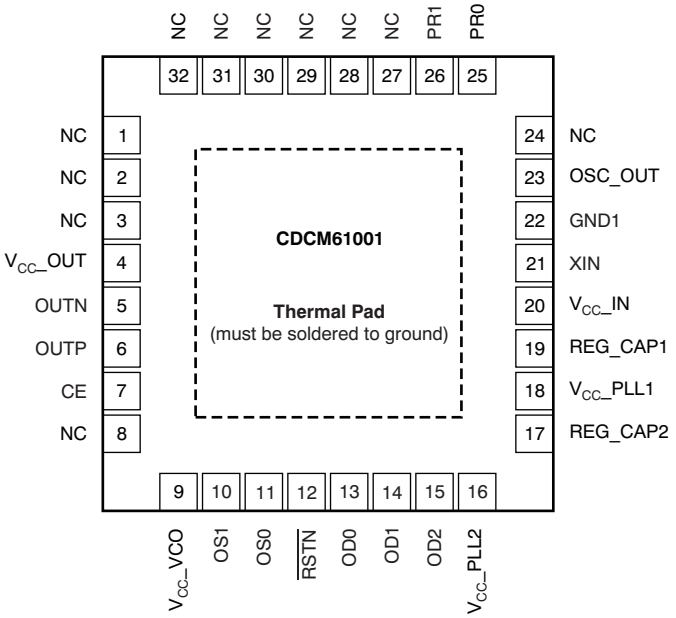
DEVICE INFORMATION

RHB PACKAGE
QFN-32
(TOP VIEW)



PIN FUNCTIONS

PIN		TYPE	DIRECTION (1)	DESCRIPTION
NAME	PAD NO.			
VCC_OUT	4	Power		3.3-V supply for the output buffer
VCC_PLL1	18	Power		3.3-V supply for the PLL circuitry
VCC_PLL2	16	Power		3.3-V supply for the PLL circuitry
VCC_VCO	9	Power		3.3-V supply for the internal VCO
VCC_IN	20	Power		3.3-V supply for the input buffers
GND1	22	Ground		Additional ground for device. (GND1 shorted on-chip to GND)
GND	Pad	Ground		Ground is on thermal pad; see *Thermal Management*
XIN	21	Input		Parallel resonant crystal or LVCMOS input
OUTN, OUTP	5, 6	Output		Differential output pair or two single-ended outputs
OSC_OUT	23	Output		Bypass LVCMOS output
REG_CAP1	19	Output		Capacitor for internal regulator (connect to a 10-μF Y5V capacitor to GND)
REG_CAP2	17	Output		Capacitor for internal regulator (connect to a 10-μF Y5V capacitor to GND)
PR0, PR1	25, 26		Pull-up	Prescaler and Feedback divider control pins (see Table 4)
OD0, OD1, OD2	13, 14, 15		Pull-up	Output divider control pins (see Table 5)
OS1, OS0	10, 11		Pull-up	Output type select control pin (see Table 6)
CE	7		Pull-up	Chip enable control pin (see Table 7)
$\overline{\text{RSTN}}$	12		Pull-up	Device reset (active low) (see Table 8)
NC	1-3, 8, 24, 27-32			No connection

(1) *Pull-up* refers to internal input resistors; see Pin Characteristics for typical values.

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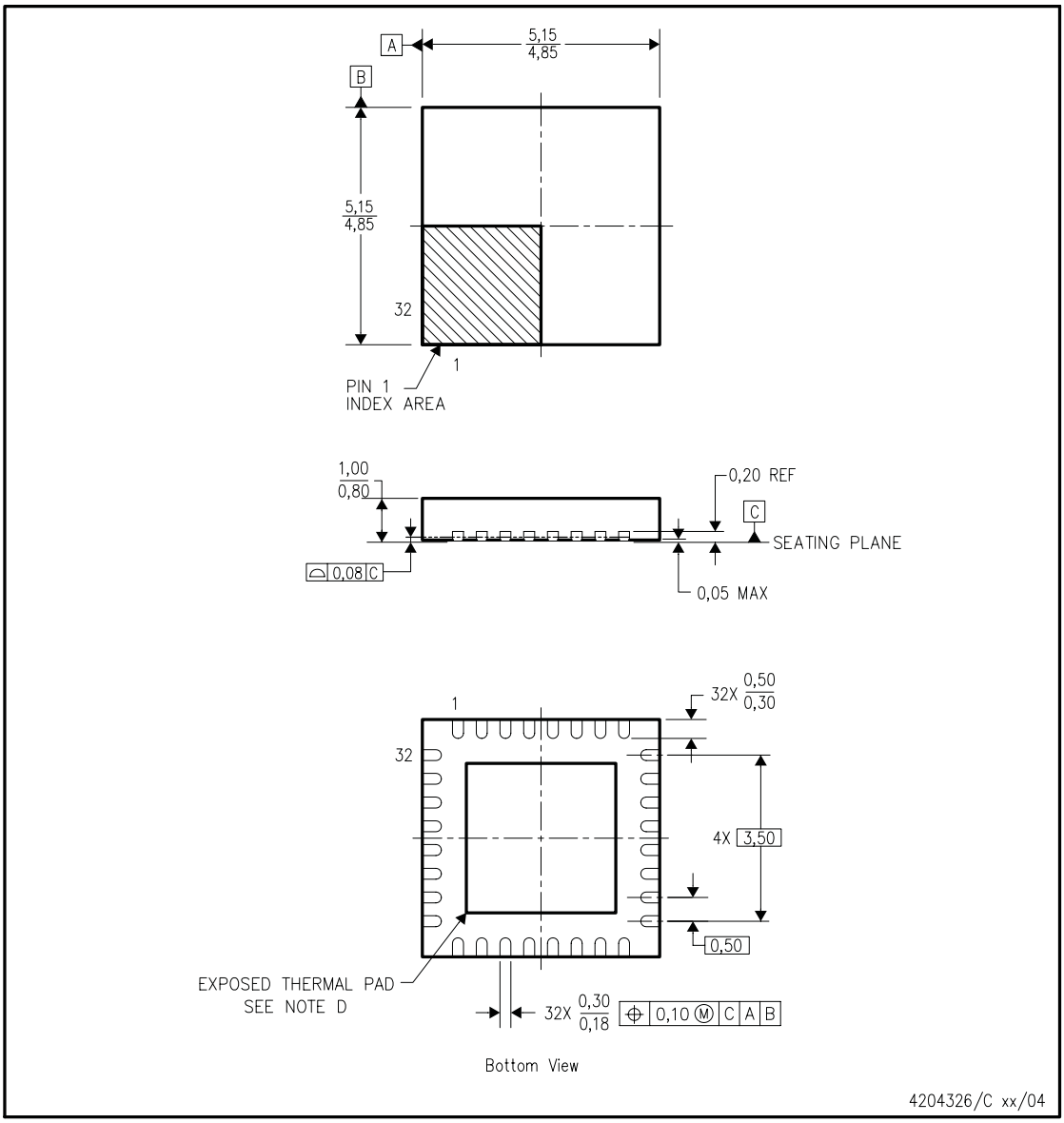
Table 1. PIN CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance		8	10	pF
R_{PULLUP}	Input pull-up resistor		150		kΩ

PACKAGE

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

Figure 2. RHB Package

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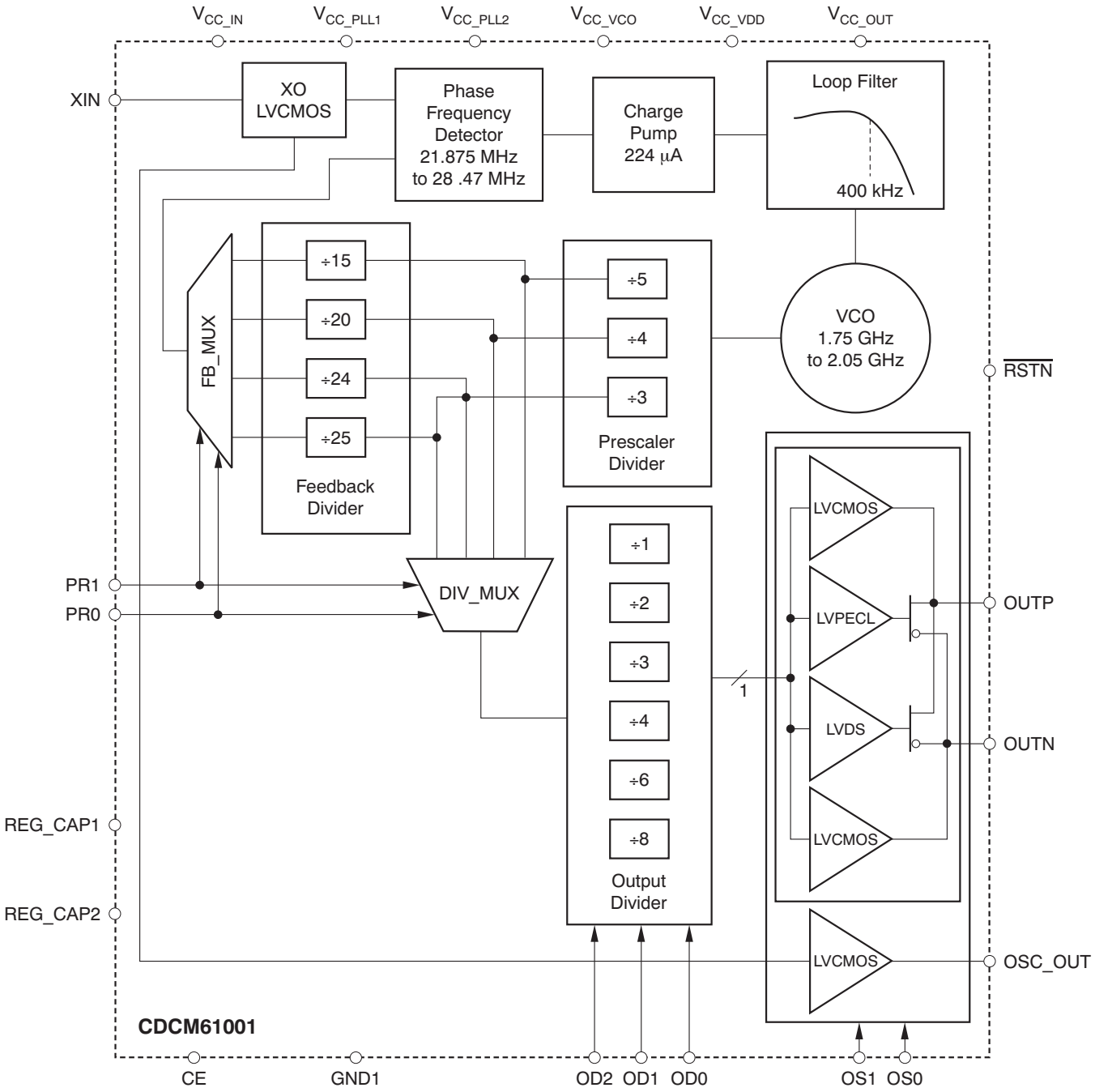
FUNCTIONAL BLOCK DIAGRAM



DEVICE CONFIGURATION

Table 2. Common Configuration

INPUT (MHz)	PRESCALER DIVIDER	FEEDBACK DIVIDER	VCO FREQUENCY (MHz)	OUTPUT DIVIDER	OUTPUT FREQUENCY (MHz)	APPLICATION
25	4	20	2000	8	62.5	GigE
24.75	3	24	1782	8	74.25	HDTV
25	3	24	1800	8	75	SATA
24.8832	3	25	1866.24	8	77.76	SONET
25	3	24	1800	6	100	PCI Express
26.5625	3	24	1912.5	6	106.25	Fibre Channel
25	4	20	2000	4	125	GigE
25	3	24	1800	4	150	SATA
24.8832	3	25	1866.24	4	155.52	SONET
25	3	25	1875	4	156.25	10 GigE
26.5625	3	24	1912.5	4	159.375	10-G Fibre Channel
25	5	15	1875	2	187.5	12 GigE
25	3	24	1800	3	200	PCI Express
26.5625	3	24	1912.5	3	212.5	4-G Fibre Channel
25	4	20	2000	2	250	GigE
24.8832	3	25	1866.24	2	311.04	SONET
25	3	25	1875	2	312.5	XGMII
24.8832	3	25	1866.24	1	622.08	SONET
25	3	25	1875	1	625	10 GigE

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Table 3. Generic Configuration

INPUT FREQUENCY RANGE (MHz)	PRESCALER DIVIDER	FEEDBACK DIVIDER	VCO FREQUENCY RANGE (MHz)	OUTPUT DIVIDER	OUTPUT FREQUENCY RANGE (MHz)
21.875 to 25.62	4	20	1750 to 2050	8	54.6875 to 64.05
21.875 to 25.62	4	20	1750 to 2050	6	72.92 to 85.4
21.875 to 25.62	4	20	1750 to 2050	4	109.375 to 128.1
21.875 to 25.62	4	20	1750 to 2050	3	145.84 to 170.8
21.875 to 25.62	4	20	1750 to 2050	2	218.75 to 256.2
21.875 to 25.62	4	20	1750 to 2050	1	437.5 to 512.4
23.33 to 27.33	3	25	1750 to 2050	8	72.906 to 85.408
23.33 to 27.33	3	25	1750 to 2050	6	97.21 to 113.875
23.33 to 27.33	3	25	1750 to 2050	4	145.812 to 170.816
23.33 to 27.33	3	25	1750 to 2050	3	194.42 to 227.75
23.33 to 27.33	3	25	1750 to 2050	2	291.624 to 341.632
23.33 to 27.33	3	25	1750 to 2050	1	583.248 to 683.264
23.33 to 27.33	5	15	1750 to 2050	8	43.75 to 51.25
23.33 to 27.33	5	15	1750 to 2050	6	58.33 to 68.33
23.33 to 27.33	5	15	1750 to 2050	4	87.5 to 102.5
23.33 to 27.33	5	15	1750 to 2050	3	116.66 to 136.66
23.33 to 27.33	5	15	1750 to 2050	2	175 to 205
23.33 to 27.33	5	15	1750 to 2050	1	350 to 410
24.305 to 28.47	3	24	1750 to 2050	8	72.915 to 85.41
24.305 to 28.47	3	24	1750 to 2050	6	97.22 to 113.88
24.305 to 28.47	3	24	1750 to 2050	4	145.83 to 170.82
24.305 to 28.47	3	24	1750 to 2050	3	194.44 to 227.76
24.305 to 28.47	3	24	1750 to 2050	2	291.66 to 341.64
24.305 to 28.47	3	24	1750 to 2050	1	583.32 to 683.28

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Table 4. Programmable Prescaler and Feedback Divider Settings

CONTROL INPUTS		PRESCALER DIVIDER	FEEDBACK DIVIDER	PFD FREQUENCY	
PR1	PR0			MINIMUM	MAXIMUM
0	0	3	24	24.305	28.47
0	1	5	15	23.33	27.33
1	0	3	25	23.33	27.33
1	1	4	20	21.875	25.62

Table 5. Programmable Output Divider

CONTROL INPUTS			OUTPUT DIVIDER
OD2	OD1	OD0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	Reserved
1	0	1	6
1	1	0	Reserved
1	1	1	8

Table 6. Programmable Output Type

CONTROL INPUTS		OUTPUT TYPE
OS1	OS0	
0	0	LVCMOS, OSC_OUT Off
0	1	LVDS, OSC_OUT Off
1	0	LVPECL, OSC_OUT Off
1	1	LVPECL, OSC_OUT On

Table 7. Output Enable

CONTROL INPUT	OPERATING CONDITION	OUTPUT
CE		
0	Power Down	Hi-Z
1	Normal	Active

Table 8. Reset

CONTROL INPUT	OPERATING CONDITION	OUTPUT
$\overline{\text{RSTN}}$		
0	Device Reset	Hi-Z
0 → 1	PLL Recalibration	Hi-Z
1	Normal	Active

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TYPICAL CHARACTERISTICS

Over operating free-air temperature range, unless otherwise noted.

TYPICAL CURRENT CONSUMPTION FOR LVPECL OUTPUT vs OUTPUT FREQUENCY

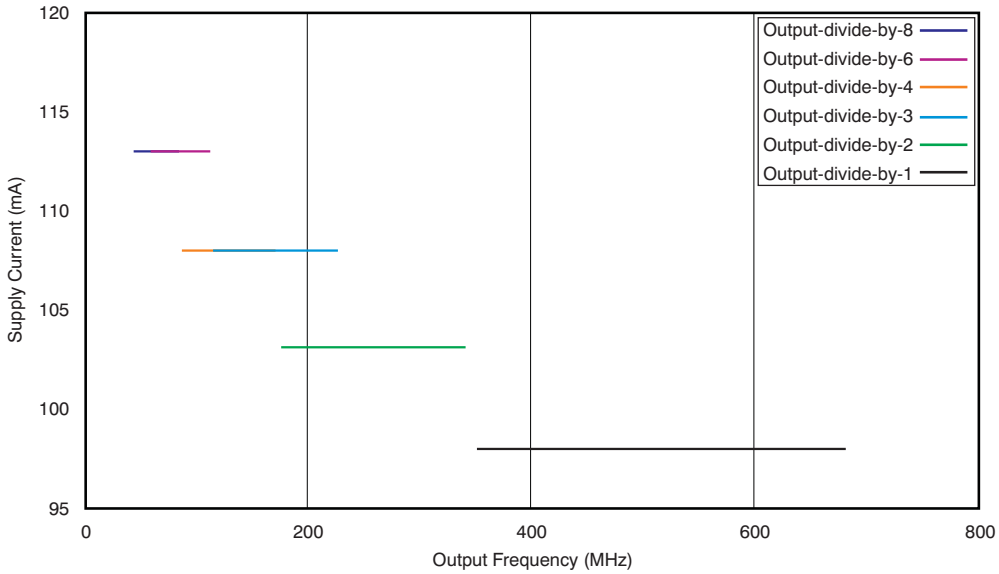

Figure 3.

TYPICAL CURRENT CONSUMPTION FOR LVDS OUTPUT vs OUTPUT FREQUENCY

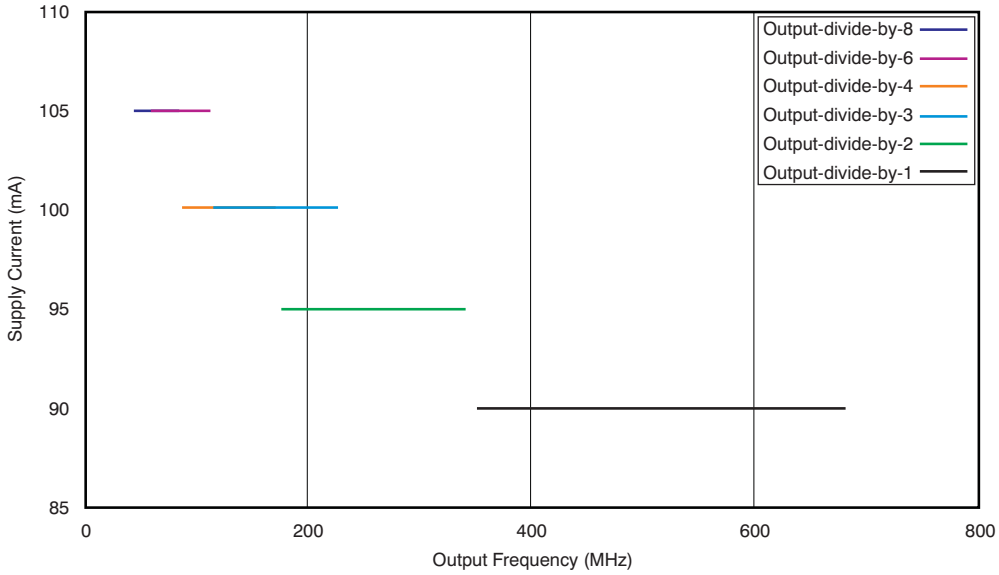

Figure 4.

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TYPICAL CHARACTERISTICS (continued)

Over operating free-air temperature range, unless otherwise noted.

TYPICAL CURRENT CONSUMPTION FOR LVCMOS OUTPUT WITH 5-pF LOAD vs OUTPUT FREQUENCY

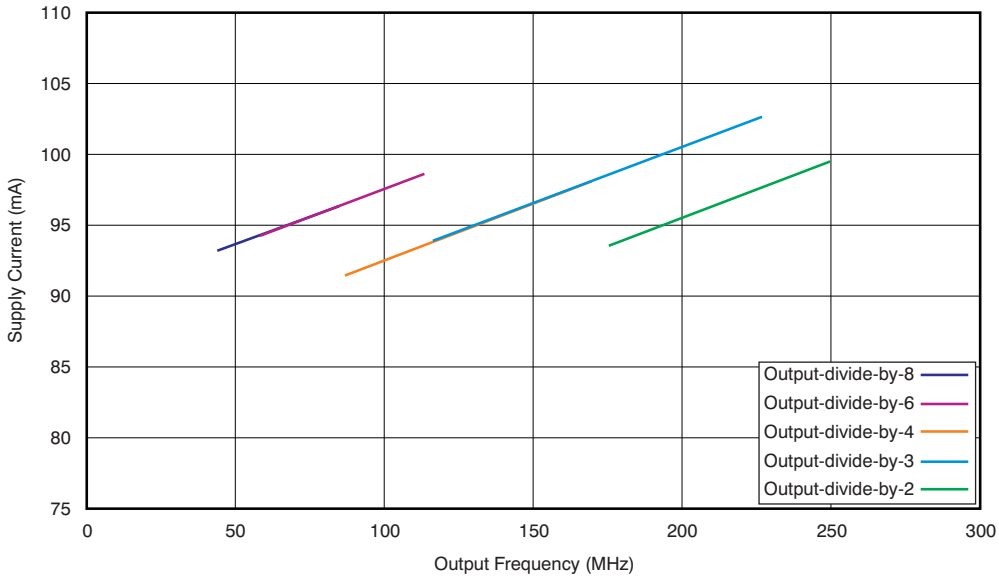

Figure 5.

TYPICAL LVPECL DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT FREQUENCY

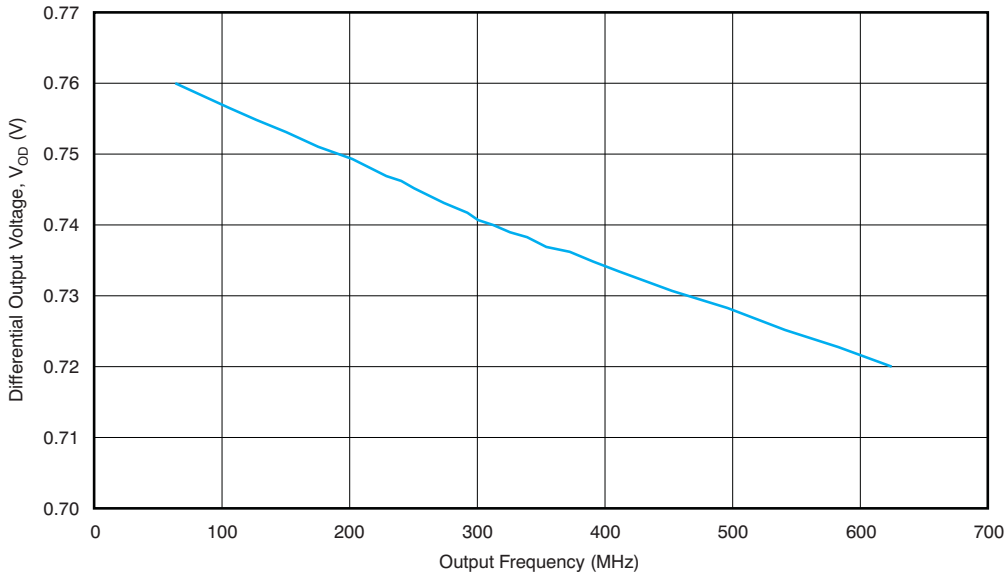

Figure 6.

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TYPICAL CHARACTERISTICS (continued)

Over operating free-air temperature range, unless otherwise noted.

TYPICAL LVDS DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT FREQUENCY

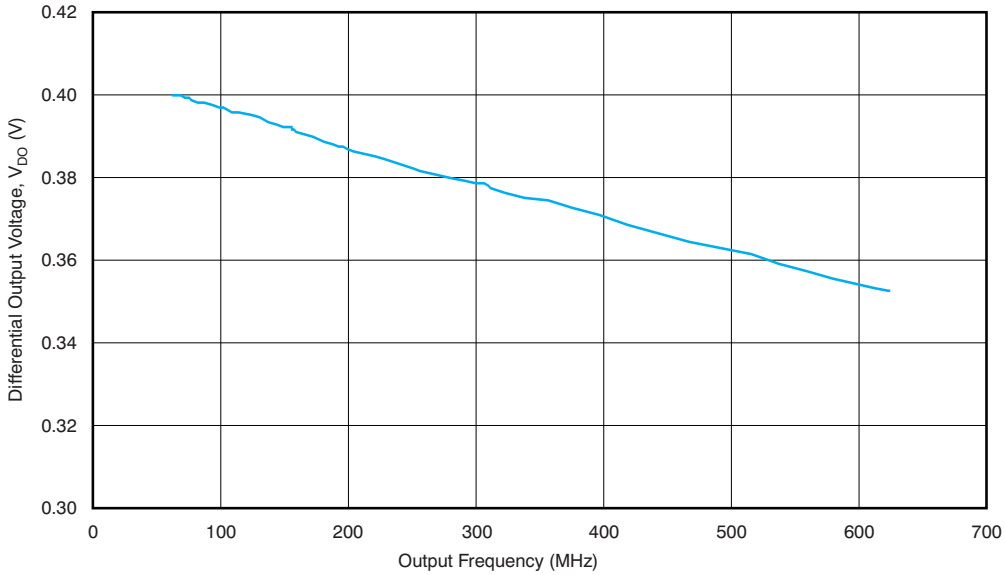

Figure 7.

TYPICAL LVCMOS OUTPUT VOLTAGE WITH 5-pF LOAD vs OUTPUT FREQUENCY

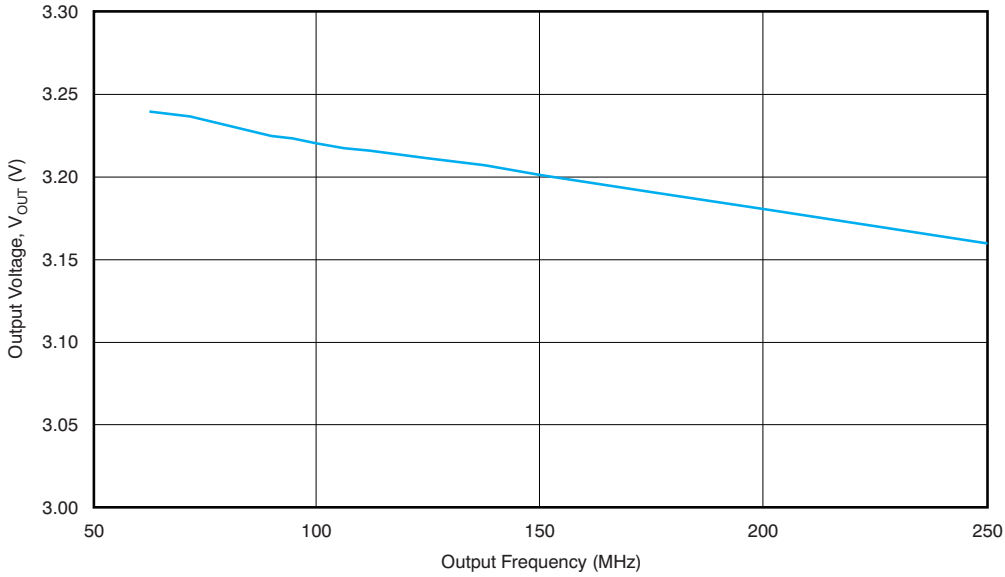

Figure 8.

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TEST CONFIGURATIONS

This section describes the function of each block for the CDCM61001. Figure 9 through Figure 15 illustrate how the device should be set up for a variety of output configurations.

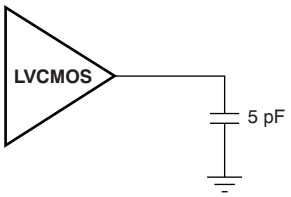

Figure 9. LVCMOS Output Loading During Device Test

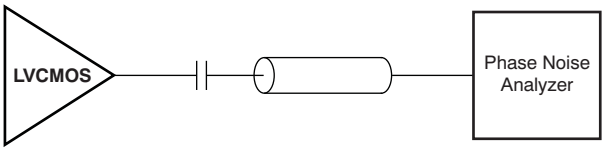

Figure 10. LVCMOS AC Configuration During Device Test

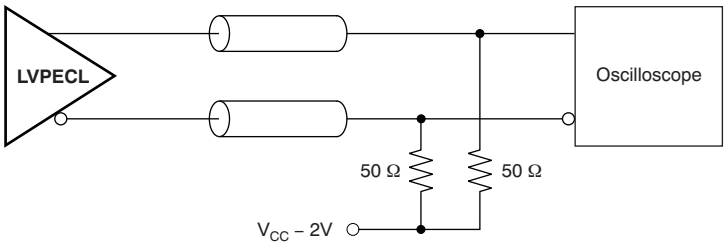

Figure 11. LVPECL DC Configuration During Device Test

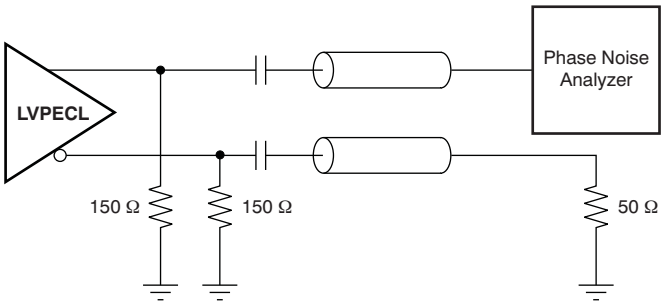

Figure 12. LVPECL AC Configuration During Device Test

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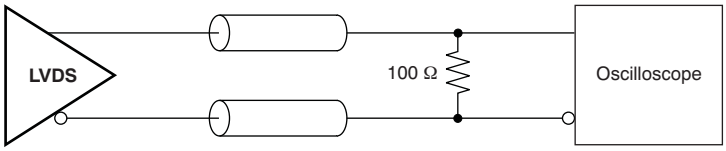

Figure 13. LVDS DC Configuration During Device Test

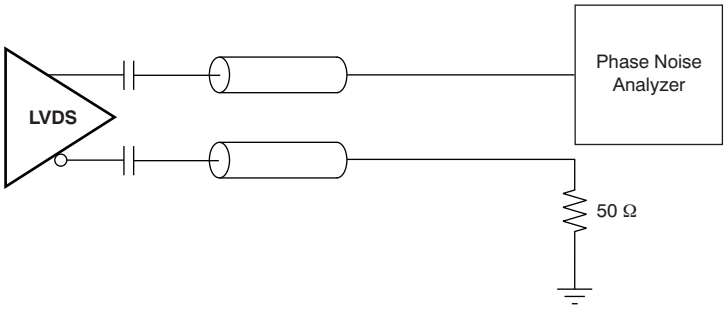

Figure 14. LVDS AC Configuration During Device Test

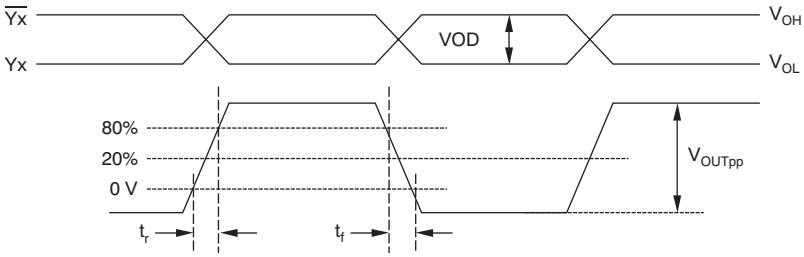

Figure 15. Output Voltage and Rise/Fall Times

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FUNCTIONAL DESCRIPTION

Phase-Locked Loop (PLL)

The CDCM61001 includes an on-chip PLL with an on-chip VCO. The PLL blocks consist of a crystal input interface, which can also accept an LVCMOS signal, a phase frequency detector (PFD), a charge pump, an on-chip loop filter, and prescaler and feedback dividers. Completing the CDCM61001 device are the output divider and universal output buffer.

The PLL is powered by on-chip, low-dropout (LDO) linear voltage regulators. The regulated supply network is partitioned such that the sensitive analog supplies are powered from separate LDOs rather than the digital supplies which use a separate LDO regulator. These LDOs provide isolation for the PLL from any noise in the external power-supply rail. The REG_CAP1 and REG_CAP2 pins should each be connected to ground by 10-µF capacitors to ensure stability.

Configuring the PLL

The CDCM61001 permits PLL configurations to accommodate the various input and output frequencies listed in Table 2 and Table 3. These configurations are accomplished by setting the prescaler divider, feedback divider and output divider. The various dividers are managed by setting the device control pins as shown in Table 4 and Table 5.

Crystal Input Interface

Fundamental mode is the recommended oscillation mode of operation for the input crystal and parallel resonance is the recommended type of circuit for the crystal.

A crystal load capacitance refers to all capacitances in the oscillator feedback loop. It is equal to the amount of capacitance seen between the terminals of the crystal in the circuit. For parallel resonant mode circuits, the correct load capacitance is necessary to ensure the oscillation of the crystal within the expected parameters.

The CDCM61001 implements an input crystal oscillator circuitry, known as the *Colpitts oscillator*, and requires one pad of the crystal to interface with the XIN pin; the other pad of the crystal is tied to ground. In this crystal interface, it is important to account for all sources of capacitance when calculating the correct value for the discrete capacitor component, C_L, for a design.

The CDCM61001 has been characterized with 10-pF parallel resonant crystals. The input crystal oscillator stage in the CDCM61001 is designed to oscillate at the correct frequency for all parallel resonant crystals with low-pull capability and rated with a load capacitance that is equal to the sum of the onchip load capacitance at the XIN pin (10-pF), crystal stray capacitance, and board parasitic capacitance between the crystal and XIN pin.

The normalized frequency error of the crystal, as a result of load capacitance mismatch, can be calculated as Equation 2:

$$\frac{\Delta f}{f} = \frac{C_S}{2(C_{L,R} + C_O)} - \frac{C_S}{2(C_{L,A} + C_O)} \tag{2}$$

Where:

C_S is the motional capacitance of the crystal,
C_0 is the shunt capacitance of the crystal,
$C_{L,R}$ is the rated load capacitance for the crystal,
$C_{L,A}$ is the actual load capacitance in the implemented PCB for the crystal,
Δf is the frequency error of the crystal,
and f is the rated frequency of the crystal.
The first three parameters can be obtained from the crystal vendor.

In order to minimize the frequency error of the crystal to meet application requirements, the difference between the rated load capacitance and the actual load capacitance should be minimized and a crystal with low-pull capability (low C_S) should be used.

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For example, if an application requires less than ±50 ppm frequency error and a crystal with less than ±50 ppm frequency tolerance is picked, the characteristics are as follows: C_0 = 7 pF, C_S = 10 fF, and $C_{L,R}$ = 12 pF. In order to meet the required frequency error, calculate $C_{L,A}$ using Equation 2 to be 17 pF. Subtracting $C_{L,R}$ from $C_{L,A}$, results in 5 pF; care must be taken during printed circuit board (PCB) layout with the crystal and the CDCM61001 to ensure that the sum of the crystal stray capacitance and board parisitic capacitance is less than the calculated 5 pF.

Good layout practices are fundamental to the correct operation and reliability of the oscillator. It is critical to locate the crystal components very close to the XIN pin to minimize routing distances. Long traces in the oscillator circuit are a very common source of problems. Do not route other signals across the oscillator circuit. Also, make sure power and high-frequency traces are routed as far away as possible to avoid crosstalk and noise coupling. Avoid the use of vias; if the routing becomes very complex, it is much better to use 0-Ω resistors as bridges to go over other signals. Vias in the oscillator circuit should only be used for connections to the ground plane. Do not share ground connections; instead, make a separate connection to ground for each component that requires grounding. If possible, place multiple vias in parallel for each connection to the ground plane. Especially in the Colpitts oscillator configuration, the oscillator is very sensitive to capacitance in parallel with the crystal. Therefore, the layout must be designed to minimize stray capacitance across the crystal to less than 5 pF total under all circumstances to ensure proper crystal oscillation. Be sure to take into account both PCB and crystal stray capacitance.

Table 9 lists several recommended crystals and the respective manufacturer of each.

Table 9. Recommended Crystal Manufacturers

MANUFACTURER	PART NUMBER
Vectron	VXC1-113
Fox	218-3
Saronix	FP2650002

Phase Frequency Detector (PFD)

The PFD takes inputs from the input interface and the feedback divider and produces an output that depends on the phase and frequency differences between the two inputs. The allowable range of frequencies at the PFD inputs is 21.875 MHz to 28.47 MHz.

Charge Pump (CP)

The charge pump is controlled by the PFD, which dictates either to pump up or down in order to charge or discharge the integrating section of the on-chip loop filter. The integrated and filtered charge pump current is then converted to a voltage that drives the control voltage node of the internal VCO through the on-chip loop filter. The charge pump current is preset to 224 µA and cannot be changed.

On-Chip PLL Loop Filter

Figure 16 shows the on-chip active loop filter topology implemented in the device. This design corresponds to a PLL bandwidth of 400 kHz for a PFD in the range of 21.875 MHz to 28.47 MHz, and a charge pump current of 224 µA.

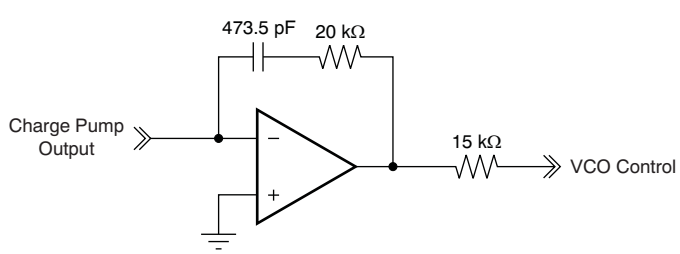

Figure 16. On-Chip PLL Loop Filter Topology

Prescaler Divider and Feedback Divider

The VCO output is routed to the prescaler divider and then to the feedback divider. The prescaler divider and feedback divider are set in tandem with each other, according to the control pin settings given in Table 4. The allowable combinations of the two dividers ensure that the VCO frequency and the PFD frequency are within the specified limits.

On-Chip VCO

The CDCM61001 includes an on-chip, LC oscillator-based VCO with low phase noise covering a frequency range of 1.75 GHz to 2.05 GHz. The VCO must be calibrated to ensure proper operation over the valid device operating conditions. This calibration requires that the PLL be set up properly to lock the PLL loop and that the reference clock input be present. During the first device initialization after power-up, which occurs after the Power-On-Reset is released (2.64 V or lower, over valid device operating conditions) or a device reset with the $\overline{\text{RSTN}}$ pin, a VCO calibration sequence is initiated after 16,384 × Reference Input Clock Cycles. The VCO calibration then takes about 20 µs over the allowable range of the reference clock input

The VCO calibration can also be reinitiated with a pulse on the $\overline{\text{RSTN}}$ pin at any time after POR is released on power-up; the $\overline{\text{RSTN}}$ pulse must be at least 100 ns wide.

For proper device operation, the reference input must be stable at the start of VCO calibration. Since inputs from crystals or crystal oscillators can typically take up to 1-2ms to be stable, it is recommended to establish a circuitry on the $\overline{\text{RSTN}}$ pin that ensures device initialization including VCO calibration after a delay of greater than 5ms compared to the power up ramp, as shown in Figure 17. A possible implementation of the delay circuitry on the $\overline{\text{RSTN}}$ pin would be a 47nF capacitor to GND, and this in tandem with the 150kΩ on-chip pull-up resistor ensures the appropriate delay. The CE pin has an internal 150kΩ pull-up resistor and can be left unconnected or pulled to high for proper device operation.

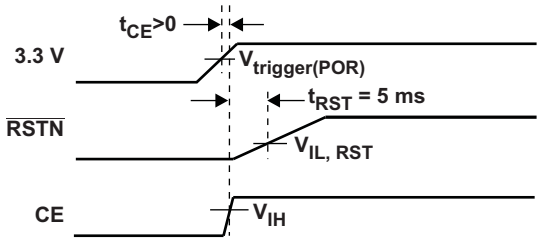

Figure 17. Suggested Timing Recommendation

LVCMOS INPUT INTERFACE

Alternately, the CDCM61001 can be operated with an external ac-coupled 2.5-V LVCMOS or dc-coupled 3.3-V LVCMOS reference input applied to the XIN pin. For proper operation, the LVCMOS reference should be available and fairly stable by the time the power supply voltages or the RSTN pin voltage on the CDCM61001 reaches 2.27V. Refer to application report SCAA111, available for download at ti.com, for more details about the LVCMOS input interface to the CDCM61001.

Output Divider

The output from the prescaler divider is also routed to the output divider. The output divider can be set with control pins according to Table 5.

Output Buffer

The output buffer can be set to LVPECL or LVDS or 2x LVCMOS, according to Table 6. OSC_OUT is an LVCMOS output that can be used to monitor proper loading of the input crystal in order to achieve the necessary crystal frequency with the least error. The OSC_OUT LVCMOS output turns on right at power up and is present during calibration. The output buffer is disabled during VCO calibration and is enabled only after calibration is complete.

The output buffer on the CDCM61001 can also be disabled, along with other sections of the device, using the CE pin according to Table 7.

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APPLICATION INFORMATION

Start-up Time Estimation

The CDCM61001 startup time can be estimated based on the parameters defined in Table 10 and graphically shown in Figure 18.

Table 10. Start-up Time Dependencies

PARAMETER	DEFINITION	DESCRIPTION	FORMULA/METHOD OF DETERMINATION
t_{REF}	Reference clock period	The reciprocal of the applied reference frequency in seconds.	$t_{REF} = \frac{1}{f_{REF}}$
t_{pul}	Power-up time (low limit)	Power-supply rise time to low limit of Power On Reset (POR) trip point	Time required for power supply to ramp to 2.27 V
t_{puh}	Power-up time (high limit)	Power supply rise time to high limit of POR trip point	Time required for power supply to ramp to 2.64 V
t_{rsu}	Reference start-up time	After POR releases, the Colpits oscillator is enabled. This start-up time is required for the oscillator to generate the requisite signal levels for the delay block to be clocked by the reference input.	500 µs best-case and 800 µs worst-case
t_{delay}	Delay time	Internal delay time generated from the reference clock. This delay provides time for the reference oscillator to stabilize.	$t_{delay} = 16384 \times t_{ref}$
t_{VCO_CAL}	VCO calibration time	VCO Calibration Time generated from the reference clock. This process selects the operating point for the VCO based on the PLL settings.	$t_{VCO_CAL} = 550 \times t_{ref}$
t_{PLL_LOCK}	PLL lock time	Time required for PLL to lock within ±10 ppm of f_{REF}	Based on the 400-kHz loop bandwidth, the PLL settles in 5τ or 12.5 µs.

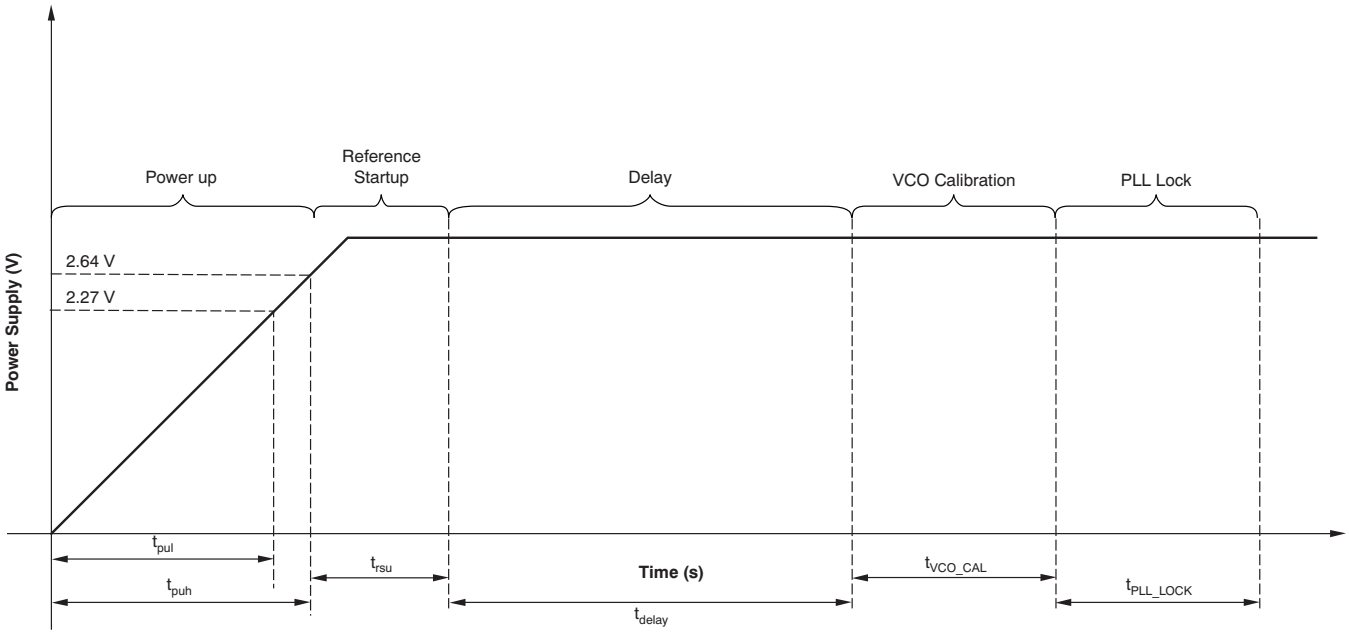

Figure 18. Start-up Time Dependencies

The CDCM61001 start-up time limits, t_{MAX} and t_{MIN}, can be calculated as follows:

$$t_{MAX} = t_{puh} + t_{rsu} + t_{delay} + t_{VCO_CAL} + t_{PLL_LOCK}$$

$$t_{MIN} = t_{pul} + t_{rsu} + t_{delay} + t_{VCO_CAL} + t_{PLL_LOCK}$$

Power Considerations

As a result of the different possible configurations of the CDCM61001, Table 11 is intended to provide enough information on the estimated current consumption of the device. Unless otherwise noted, V_{CC} = 3.3 V and T_A = +25°C.

Table 11. Estimated Block Power Consumption

BLOCK	CONDITION	CURRENT CONSUMPTION (mA)	IN-DEVICE POWER DISSIPATION (mW)	EXTERNAL RESISTOR POWER DISSIPATION (mW)
Entire device, core current	Output off, no termination resistors	65	214.5	
Output buffer	LVPECL output, active mode	28	42.4	50
	LVCMOS output pair, static	4.5	14.85	
	LVCMOS output pair, transient, 'C_L' load, 'f' MHz output frequency	$V \times f_{OUT} \times (C_L + 20 \times 10^{-12}) \times 10^3$	$V^2 \times f_{OUT} \times (C_L + 20 \times 10^{-12}) \times 10^3$	
	LVDS output, active mode	20	66	
Divide circuitry	Divide enabled, divide = 1	5	16.5	
	Divide enabled, divide = 2	10	33	
	Divide enabled, divide = 3, 4	15	49.5	
	Divide enabled, divide = 6, 8	20	66	

From Table 11, the current consumption can be calculated for any configuration. For example, the current for the entire device with one LVPECL output in active mode can be calculated by adding up the following blocks: core current, LVPECL output buffer current, and the divide circuitry current. The overall in-device power consumption can also be calculated by summing the in-device power dissipated in each of these blocks.

As an example scenario, let us consider the use case of a crystal input frequency of 25 MHz and device output frequency of 312.5 MHz in LVPECL mode. For this case, the typical overall power dissipation can be calculated as:

$$3.3\ V \times (65 + 28 + 10)\ mA = 339.9\ mW$$

Because the LVPECL output has external resistors and the power dissipated by these resistors is 50 mW, the typical overall in-device power dissipation is:

$$339.9\ mW – 50\ mW = 289.9\ mW$$

When the LVPECL output is active, the average voltage is approximately 1.9 V on each output as calculated from the LVPECL V_{OH} and V_{OL} specifications. Therefore, the power dissipated in each emitter resistor is approximately $(1.9\ V)^2/150\Omega$ = 25 mW.

When the LVCMOS output is active and drives a load capacitance, C_L, the overall LVCMOS output current consumption is the sum of a static pre-driver current and a dynamic switching current (which is a function of the output frequency and the load capacitance).

Let us consider another use case of a crystal input frequency of 26.5625 MHz and device output frequency of 212.5 MHz in LVCMOS mode and driving a 5-pF load capacitance. For this case, the typical overall power dissipation can be calculated as:

$$3.3\ V \times (65 + 15 + 21.4)\ mA = 334.62\ mW$$

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Thermal Management

Power consumption of the CDCM61001 can be high enough to require attention to thermal management. For reliability and performance reasons, the die temperature should be limited to a maximum of +125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times θ_{JA} should not exceed +125°C.

The device package has an exposed pad that provides the primary heat removal path as well as an electrical grounding to the printed circuit board (PCB). To maximize the removal of heat from the package, a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. See the mechanical data at the end of the data sheet for land and via pattern examples.

Power-Supply Filtering

PLL-based frequency synthesizers are sensitive to noise on the power supply, which can dramatically increase the jitter of the PLL. This characteristic is especially true for analog-based PLLs. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications. A PLL would have attenuated jitter as a result of power-supply noise at frequencies beyond the PLL bandwidth because of attenuation by the loop response.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use these bypass capacitors, they must be placed very close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1-μF) bypass capacitors as there are supply pins in the package.

The CDCM61001 power-supply requirements can be grouped into two sets: the analog supply line and the output/input supply line. The analog supply line consists of the following power-supply pins on the CDCM61001: VCC_PLL1, VCC_PLL2, and VCC_VCO. These pins can be shorted together. The output/input supply line consists of the VCC_OUT and the VCC_IN power-supply pins on the CDCM61001. These pins can be shorted together. Inserting a ferrite bead between the analog supply line and the output/input supply line isolates the high-frequency switching noises generated by the device input and output, preventing them from leaking into the sensitive analog supply line. Choosing an appropriate ferrite bead with very low dc resistance is important because it is imperative to provide adequate isolation between the sensitive analog supply line and the other board supply lines, and to maintain a voltage at the analog power-supply pins of the CDCM61001 that is greater than the minimum voltage required for proper operation.

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Figure 19 shows a general recommendation for decoupling the power supply.

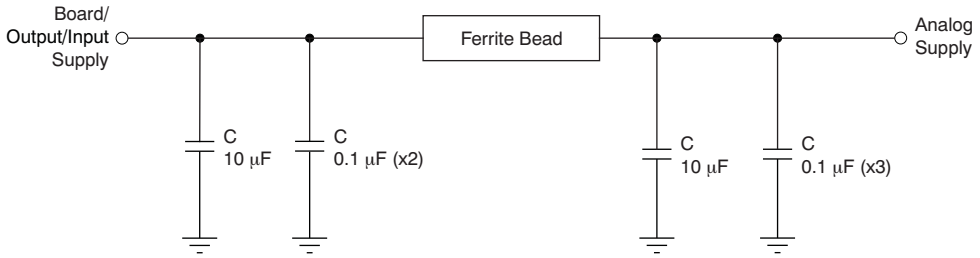

Figure 19. Recommended Power-Supply Decoupling

Output Termination

The CDCM61001 is a 3.3-V clock driver with the following output options: LVPECL, LVDS, or LVCMOS.

LVPECL Termination

The CDCM61001 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination are required to ensure correct operation of the device and to minimize signal integrity. The proper termination for LVPECL is 50 Ω to (V_{CC}–2) V, but this dc voltage is not readily available on most PCBs. Thus, a Thevenin equivalent circuit is worked out for the LVPECL termination in both direct-coupled (dc) and ac-coupled cases, as shown in Figure 20 and Figure 21. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltage of the driver and receiver are different, ac-coupling is required.

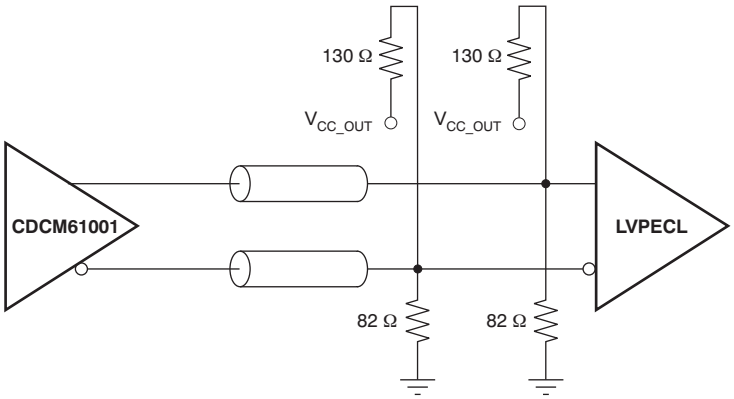

Figure 20. LVPECL Output DC Termination

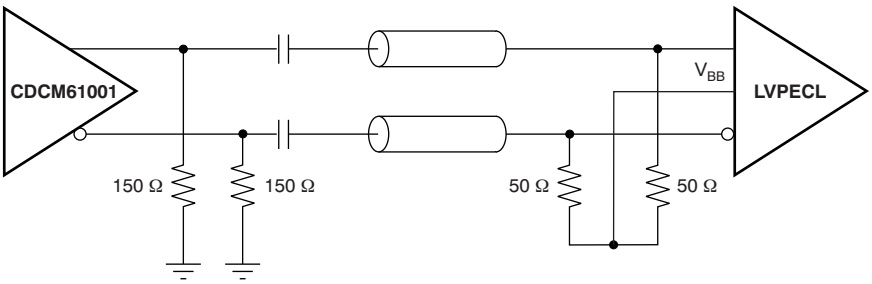

Figure 21. LVPECL Output AC Termination

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LVDS Termination

The proper LVDS termination for signal integrity over two 50 Ω lines is 100 Ω between the outputs on the receiver end. Either dc-coupled termination or ac-coupled termination can be used for LVDS outputs, as shown in Figure 22 and Figure 23. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltage of the driver and the receiver are different, ac-coupling is required.

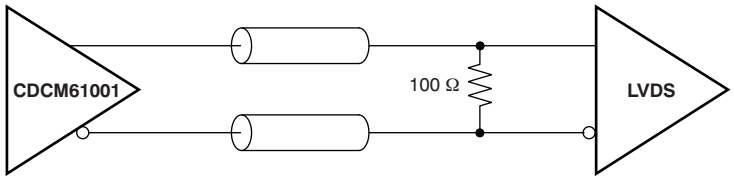

Figure 22. LVDS Output DC Termination

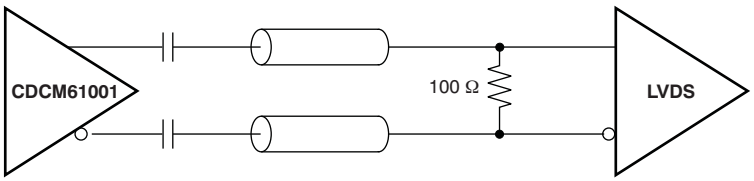

Figure 23. LVDS Output AC Termination

LVCMOS Termination

Series termination is a common technique used to maintain the signal integrity for LVCMOS drivers, if connected to a receiver with a high-impedance input with a pull-up or pull-down resistor. For series termination, a series resistor (R_S) is placed close to the driver, as shown in Figure 24. The sum of the driver impedance and R_S should be close to the transmission line impedance, which is usually 50 Ω. Because the LVCMOS driver in the CDCM61001 has an impedance of 30 Ω, R_S is recommended to be 22 Ω to maintain proper signal integrity.

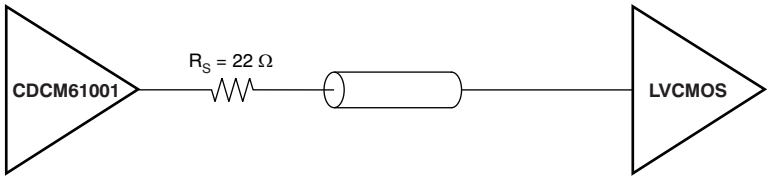

Figure 24. LVCMOS Output Termination

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Interfacing Between LVPECL and HCSL

Because the LVPECL common-mode voltage is different from the HCSL common-mode voltage, ac-coupled termination is used. The 150-Ω resistor ensures proper biasing of the CDCM61001 LVPECL output stage, while the 471-Ω and 56-Ω resistor network biases the HCSL receiver input stage, as shown in Figure 25.

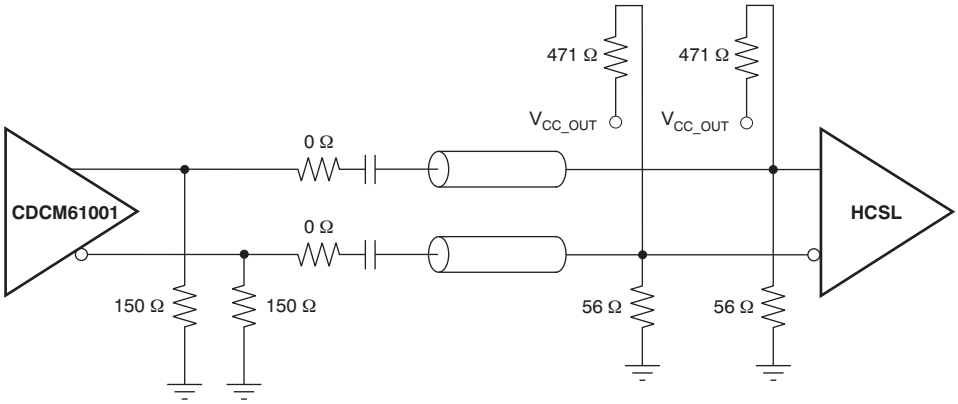

Figure 25. LVPECL to HCSL Interface

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July, 2009) to Revision C	Page
• Deleted all references to *Single-Ended* and *LVCMOS Inputs*	1
• Deleted parameters f_{IN}, ΔV/ΔT, and DutyREF from the Electrical Characteristics table	4
• Added *LVCMOS Input Interface* section	20

Changes from Revision C (February 2010) to Revision D	Page
• Changed *Crystal* to *Crystal/LVCMOS* in first bullet of Features list	1
• Changed first sentence of Description to include an LVCMOS input	1
• Updated Figure 1	2
• Changed title of *Control Pin LVCMOS Input Characteristics* section in Electrical Characteristics table	4
• Added minimum specification to *Drive level* parameter of Crystal Chatacteristics table	6
• Changed *crystal* to *crystal or LVCMOS* in XIN row of Pin Functions table	7
• Corrected order of OUTN and OUTP in Pin Functions table	7
• Changed description of *Crystal Input Interface* section	18
• Changed description of *LVCMOS Input Interface* section	20

Changes from Revision D (July 2010) to Revision E	Page
• Changed Note 1 of the Pin Functions table From: Pull-up and Pull-down refef to... To: Pull-up refers to	7
• Deleted $R_{PULLDOWN}$ from Table 1	8
• Changed values in row 24.75 of Table 2	10
• Changed the text of Configuring the PLL, deleted the last sentence	18
• Changed the On-Chip VCO section	20
• Changed the Output Buffer section	20
• Changed the power dissipation equation From: 3.3 V × (65 + 28 + 10) mA = 340.2 mW To: 3.3 V × (65 + 28 + 10) mA = 339.9 mW	22
• Changed the power dissipation equation From: 343.5 mW – 50 mW = 290.2 mW To: 339.9 mW – 50 mW = 289.9 mW	22
• Deleted figure "Recommended PCB Layout for CDCM61001" from the Thermal Management section. Added See the mechanical data at the end of the data sheet	23

Changes from Revision E (March 2011) to Revision F	Page
• Changed the On-Chip VCO section	20
• Changed Figure 17	20
• Moved the LVCMOS INPUT INTERFACE section prior to the Output Divider section	20

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCM61001RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CDCM 61001
CDCM61001RHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CDCM 61001
CDCM61001RHBR/2801	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CDCM 61001
CDCM61001RHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CDCM 61001
CDCM61001RHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CDCM 61001

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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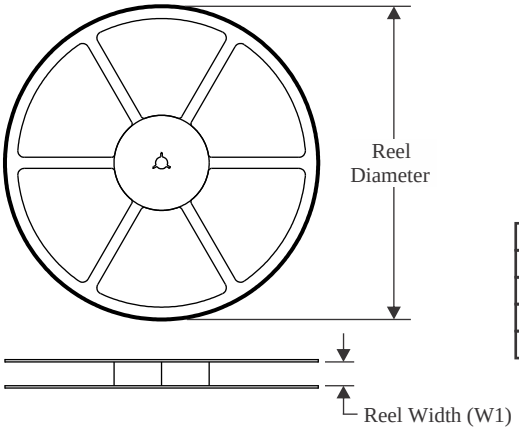
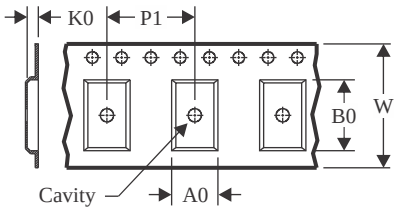
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

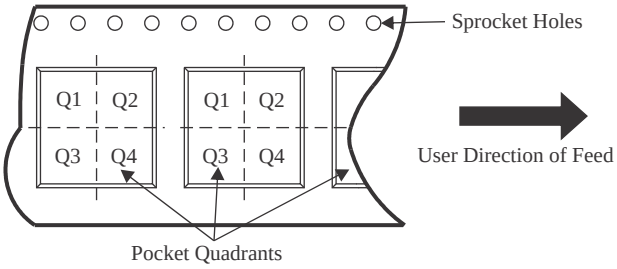


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

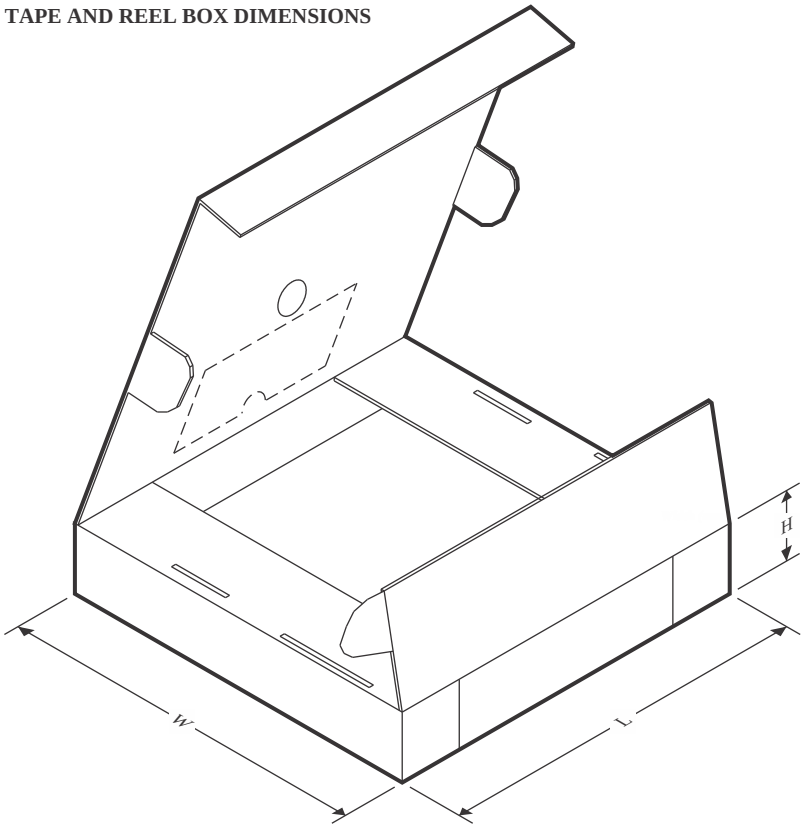
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCM61001RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CDCM61001RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCM61001RHBR	VQFN	RHB	32	3000	356.0	356.0	35.0
CDCM61001RHBT	VQFN	RHB	32	250	213.0	191.0	35.0

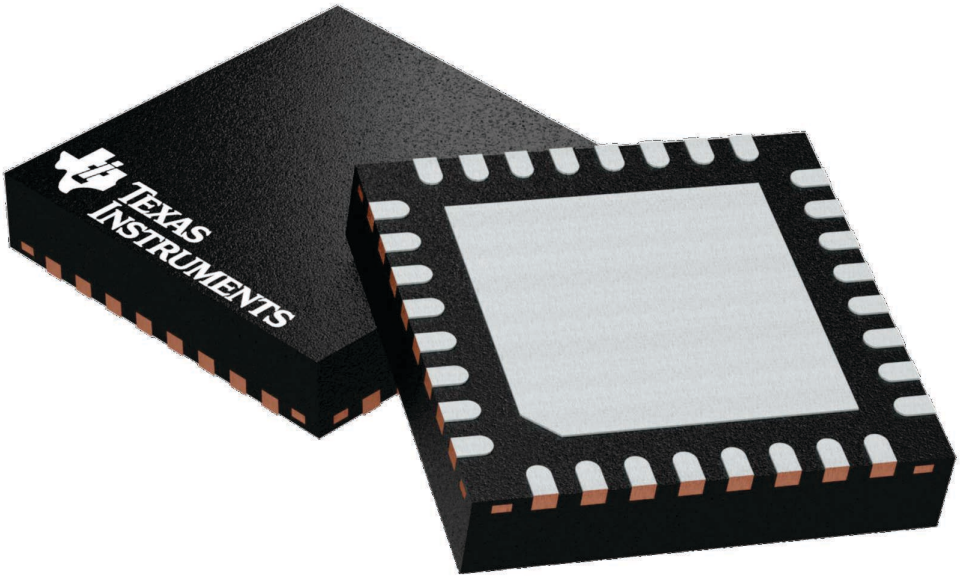
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

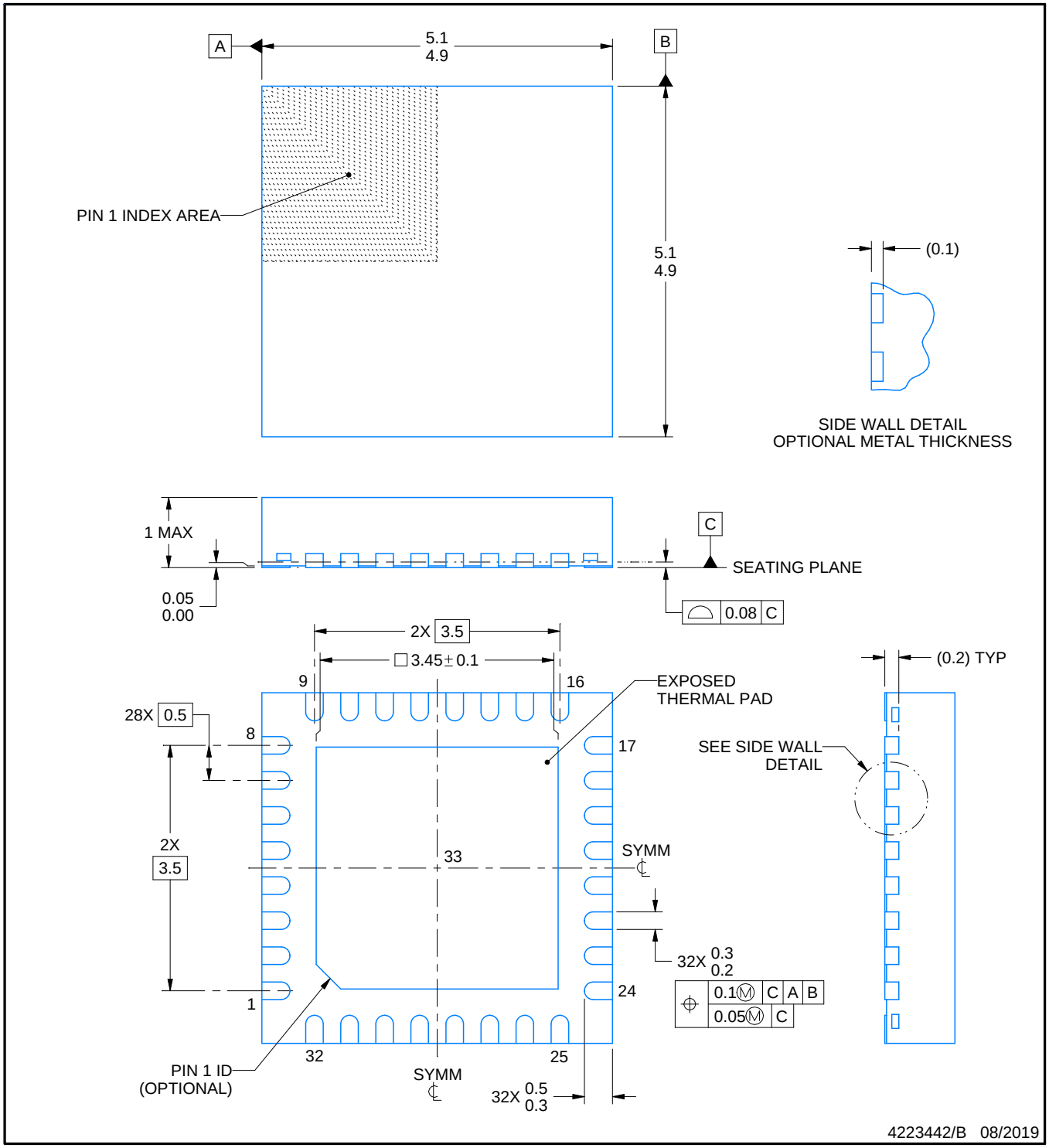
4224745/A

RHB0032E

PACKAGE OUTLINE

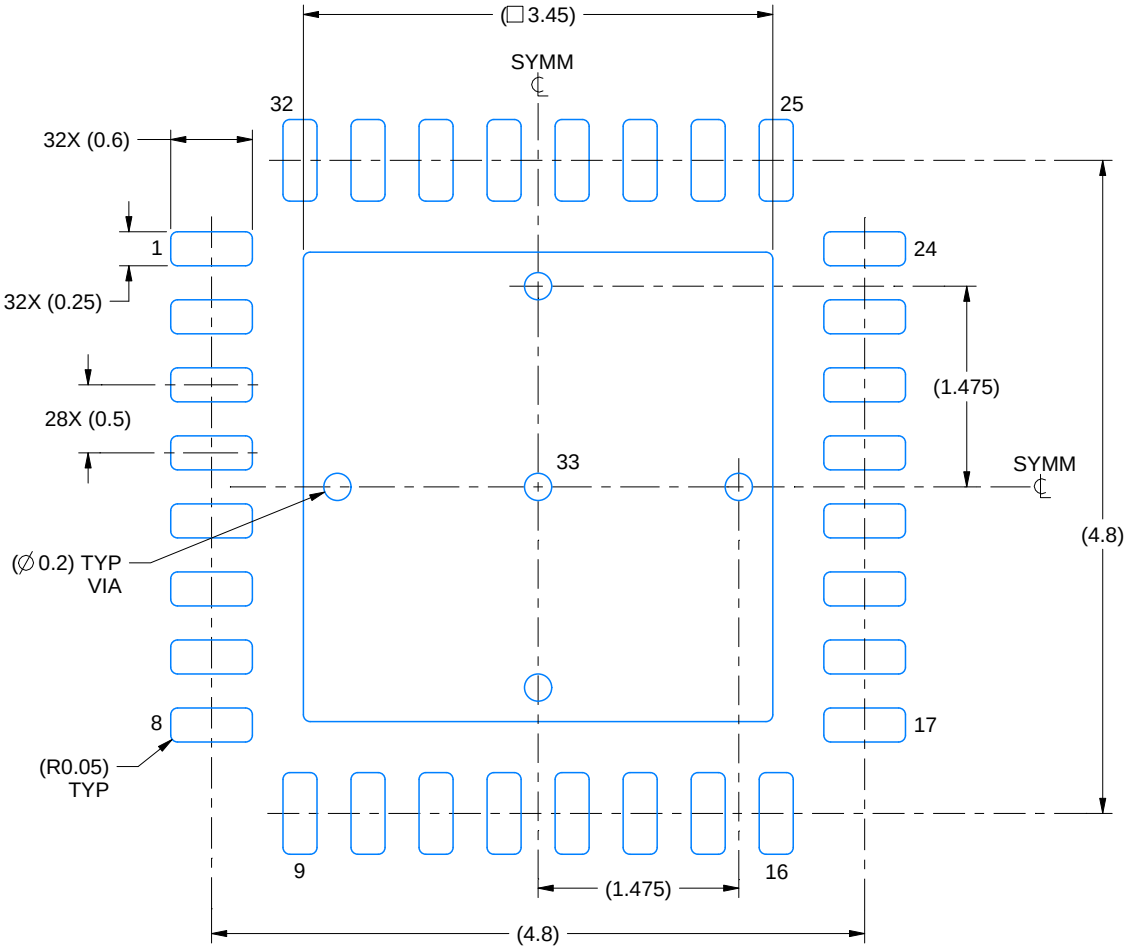
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

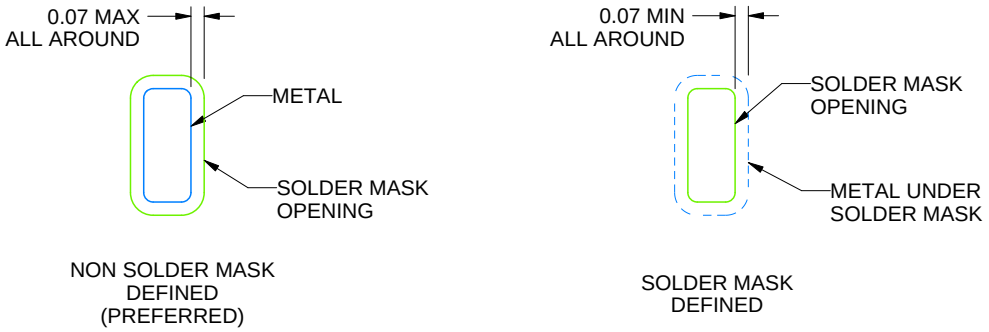


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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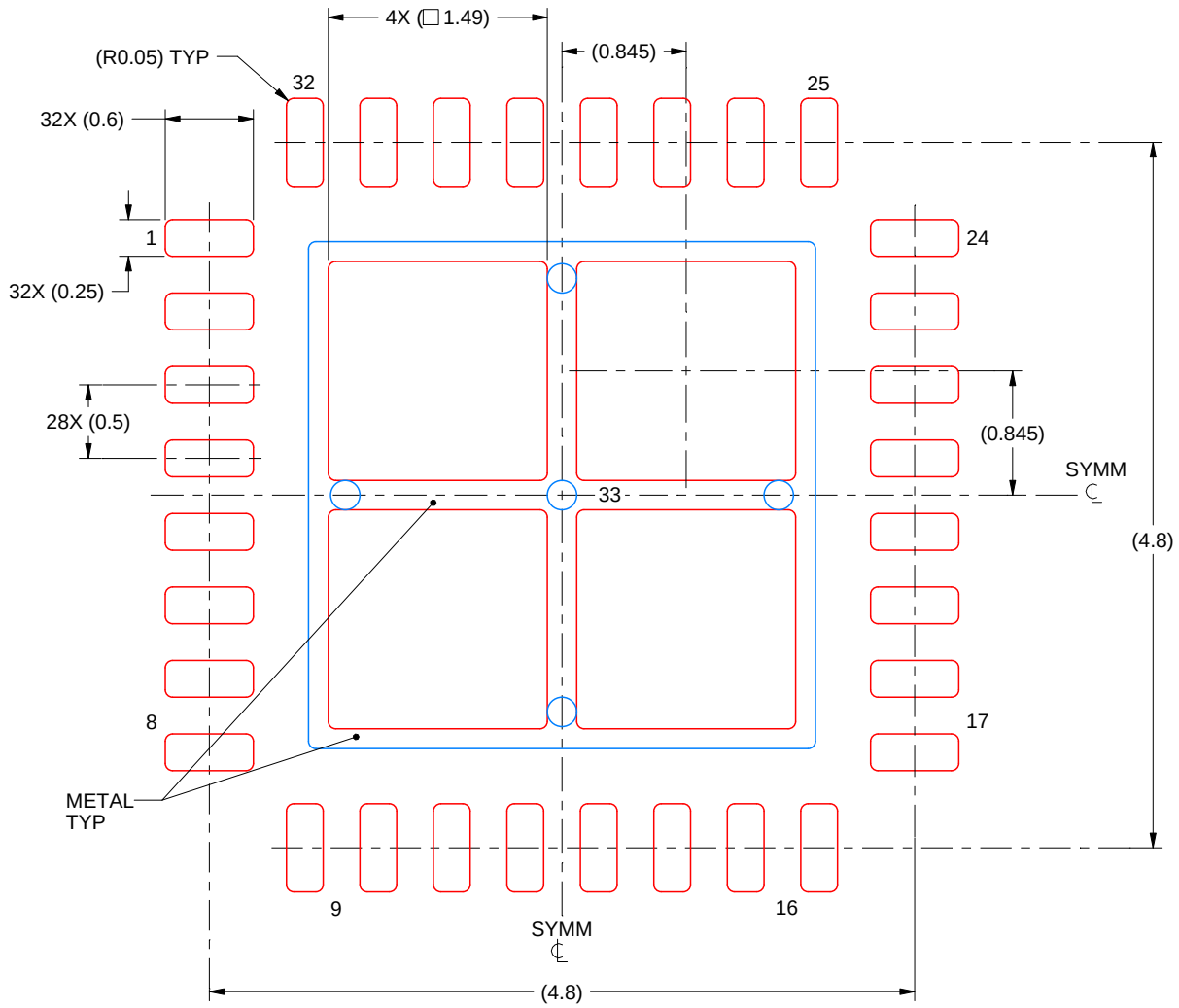
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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