

## Thunderbolt™ SUPPLY SELECTION IC

Check for Samples: [TPS22985](#)

### FEATURES

- 2.8 V to 19.8 V
- Auto Selects 3.3 V Supply
- > 10-mA Low Power Switch
- > 500-mA High Power Switch
- Reverse Current Blocking From OUT to VDD
- Wake on UART Input Activity
- UART RX and TX Buffers

### APPLICATIONS

- Thunderbolt™ Cables
- Notebook Computers
- Desktop Computers
- Power Management Systems

### DESCRIPTION

The TPS22985 is a supply selection device for active Thunderbolt™ cables. The device selects a supply that is at 3.3V from two supply inputs and connects this to two non-current limited outputs OUTA and OUTB. When 3.3V is not present at either supply, the outputs become high impedance.

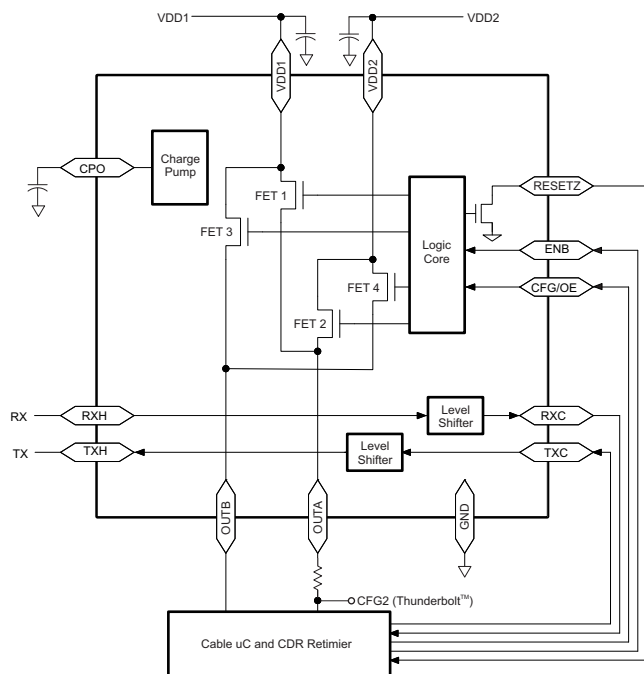
The TPS22985 has two modes of operation, Normal and Control.

In Normal Mode, OUTA is always on when a valid supply is present. OUTB is connected to a valid VDD when the ENB input is high.

In Control Mode, OUTA functions the same as Normal Mode and OUTB is controlled by a combination of monitored inputs and valid supplies on VDD1 and VDD2. When a valid VDD is available, the device waits for a rising input on ENB and then disconnects OUTB until the next falling RXH transition. Once the next falling RXH transition occurs, the device reconnects OUTB.

In either mode, when a valid VDD is not available, the TPS22985 opens all switches and the outputs OUTA and OUTB become high impedance. When the connected VDD exceeds a maximum voltage of 3.6V, it is disconnected from the outputs. VDD2 will only connect when it is in the valid range and VDD1 is greater than 3.6V

The TPS22985 is available in a 1.6mm x 1.6mm WCSP package.



**Figure 1. Typical Application**



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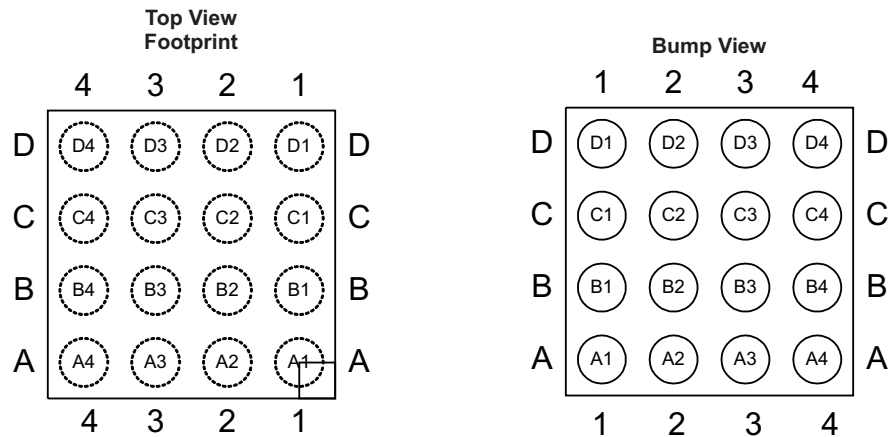


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION

| PART NUMBER | PACKAGE MARKING <sup>(1)</sup> | PACKAGE | DEVICE SPECIFIC FEATURES |
|-------------|--------------------------------|---------|--------------------------|
| TPS22985YFP | YMD9US                         | YFP     | WCSP                     |

(1) Y = Year, M = Month, D = Sequence Code, 9U = TPS22985 Device Code, S = Wafer Fab/Assembly Site Code



Die Size: 1.6mm x 1.6mm

Bump Size: 0.25mm

Bump Pitch: 0.4mm

**Table 1. TPS22985 Pin Mapping (Top View)**

|   | 4    | 3    | 2      | 1      |
|---|------|------|--------|--------|
| D | VDD1 | VDD1 | VDD2   | VDD2   |
| C | OUTA | OUTB | OUTB   | GND    |
| B | RXH  | TXH  | RESETZ | CPO    |
| A | RXC  | TXC  | ENB    | CFG/OE |

### DISSIPATION RATINGS

| PACKAGE | THERMAL RESISTANCE<br>$\theta_{JA}$ | THERMAL RESISTANCE <sup>(1)</sup><br>$\theta_{JB}$ | POWER RATING<br>$T_A = 25^\circ\text{C}$ | DERATING FACTOR<br>ABOVE <sup>(2)</sup><br>$T_A = 25^\circ\text{C}$ |
|---------|-------------------------------------|----------------------------------------------------|------------------------------------------|---------------------------------------------------------------------|
| YFP     | 95°C/W                              | 63°C/W                                             | 1050 mW                                  | 10.5 mW/°C                                                          |

(1) Simulated with high-K board

(2) Maximum power dissipation is a function of  $T_{J(\max)}$ ,  $\theta_{JA}$  and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_{J(\max)} - T_A) / \theta_{JA}$ .

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

|                      |                                                                                              | VALUE           | UNIT |
|----------------------|----------------------------------------------------------------------------------------------|-----------------|------|
| V <sub>I</sub>       | Voltage range on VDD1, VDD2, OUTA, OUTB <sup>(3)</sup>                                       | –0.3 to 20      | V    |
|                      | Voltage range on RXC, TXC, RESETZ, CFG/OE, ENB <sup>(3)</sup> (VDD is the active 3.3V input) | –0.3 to VDD+0.3 | V    |
|                      | Voltage range on CPO                                                                         | –0.3 to 13      | V    |
|                      | Voltage range on RXH, TXH                                                                    | –0.3 to 4.0     | V    |
| T <sub>A</sub>       | Operating ambient temperature range                                                          | –40 to 85       | °C   |
| T <sub>J (MAX)</sub> | Maximum operating junction temperature                                                       | 125             | °C   |
| T <sub>stg</sub>     | Storage temperature range                                                                    | –65 to 150      | °C   |
|                      | Charge Device Model (JESD 22 C101)                                                           | 350             | V    |
|                      | Human Body Model (JESD 22 A114)                                                              | 2               | kV   |
|                      | Contact discharge on VDD1, VDD2 (IEC 61000-4-2) <sup>(4)</sup>                               | 4.4             | kV   |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T<sub>A(max)</sub>] is dependent on the maximum operating junction temperature [T<sub>J(max)</sub>], the maximum power dissipation of the device in the application [P<sub>D(max)</sub>], and the junction-to-ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the following equation: T<sub>A(max)</sub> = T<sub>J(max)</sub> – (θ<sub>JA</sub> × P<sub>D(max)</sub>)
- (3) All voltage values are with respect to network ground terminal.
- (4) IEC tests are run with 0.1 μF on VDD1 and VDD2. IEC rating is non-destructive.

## RECOMMENDED OPERATING CONDITIONS

|                     |                                    | MIN                   | MAX  | UNIT |
|---------------------|------------------------------------|-----------------------|------|------|
| V <sub>DD1</sub>    | Supply voltage range               | 2.8                   | 19.8 | V    |
| V <sub>DD2</sub>    |                                    | 2.8                   | 19.8 |      |
| I <sub>LIM1/2</sub> | FET1 and FET2 switch current range | 0                     | 10   | mA   |
| I <sub>LIM3/4</sub> | FET3 and FET4 switch current range | 0                     | 500  | mA   |
| V <sub>IH</sub>     | Input logic high                   | RXH, TXC, CFG/OE, ENB | 2    | V    |
| V <sub>IL</sub>     | Input logic low                    | RXH, TXC, CFG/OE, ENB | 0.8  | V    |
| V <sub>OH</sub>     | Output logic high                  | RXC, TXH, RESETZ      | 2.25 | V    |
| V <sub>OL</sub>     | Output logic low                   | RXC, TXH, RESETZ      | 0.4  | V    |
| C <sub>OUT</sub>    | Output capacitance on OUTA         | 1                     | 4    | μF   |
|                     | Output capacitance on OUTB         | 4                     | 22   |      |
| C <sub>CPO</sub>    | Output capacitance on CPO          | 2                     | 10   | nF   |
| T <sub>A</sub>      | Operating temperature range        | –40                   | 85   | °C   |

## ELECTRICAL CHARACTERISTICS

Unless otherwise noted the specification applies over the  $V_{DD}$  range and operating junction temp  $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ . Typical values are for  $V_{DD} = 3.3\text{V}$  and  $T_J = 25^{\circ}\text{C}$

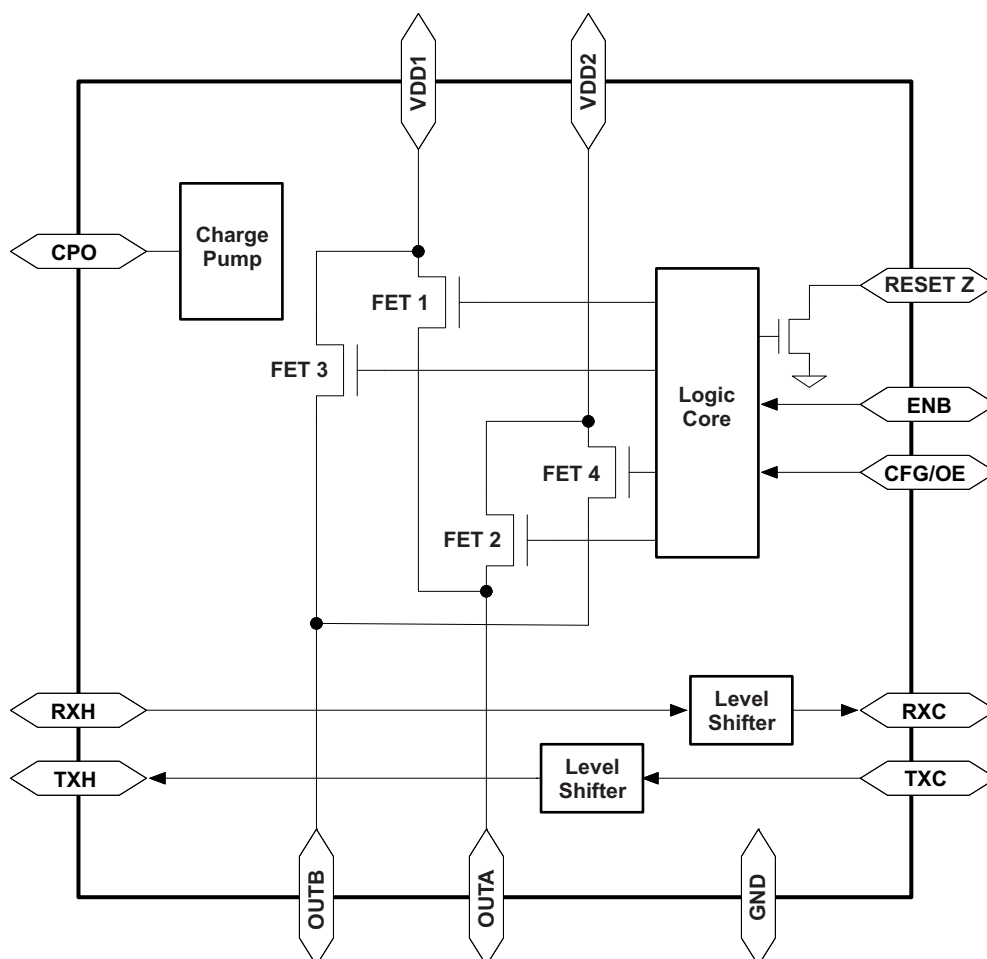
| PARAMETER                                    |                                          | TEST CONDITIONS                                                                                                                                                                                               | MIN | TYP  | MAX  | UNIT          |
|----------------------------------------------|------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|------|---------------|
| <b>POWER SUPPLIES AND CURRENTS</b>           |                                          |                                                                                                                                                                                                               |     |      |      |               |
| $V_{DD1/2}$                                  | Input voltage range                      |                                                                                                                                                                                                               | 2.8 |      | 19.8 | V             |
| $I_{DD-1}$                                   | VDD1 Quiescent current                   | $V_{DD1} = 2.5$ to $15\text{ V}$                                                                                                                                                                              |     | 250  | 500  | $\mu\text{A}$ |
| $I_{DD-2}$                                   | VDD2 Quiescent current                   | $V_{DD2} = 3.3\text{ V}$ , $V_{DD1} = 3.3\text{ V}$                                                                                                                                                           |     | 20   |      | $\mu\text{A}$ |
|                                              |                                          | $V_{DD2} = 3.3\text{ V}$ , $V_{DD1} = 15\text{ V}$                                                                                                                                                            |     | 20   |      |               |
| $I_{DDOFF-2}$                                | VDD2 Off current                         | $V_{DD2} = 3.3\text{ V}$ , $V_{DD1} = 0\text{ V}$                                                                                                                                                             |     |      | 1    | $\mu\text{A}$ |
| $I_{IN-ENB}$                                 | ENB Input current                        | $V_{IN} = 1.8\text{ V}$ to $3.6\text{ V}$                                                                                                                                                                     |     |      | 1    | $\mu\text{A}$ |
| $I_{IN-UART}$                                | RXH Input current                        | $V_{IN} = 1.8\text{V}$ to $3.6\text{ V}$                                                                                                                                                                      |     |      | 1    | $\mu\text{A}$ |
| $I_{IN-CFGOE}$                               | CFG/OE Input current <sup>(1)</sup>      | $V_{CFG/OE} = 0\text{ V}$                                                                                                                                                                                     | -1  | -1.8 | -5   | $\mu\text{A}$ |
| $V_{PUCFGOE}$                                | CFG/OE pull-up voltage <sup>(1)</sup>    |                                                                                                                                                                                                               | 2.3 |      | 6.7  | V             |
| $I_{IN-RESETZ}$                              | RESETZ Input current                     | $V_{RESETZ} = 100\text{ mV}$                                                                                                                                                                                  | 0.8 | 2    | 3    | mA            |
| <b>SWITCH AND RESISTANCE CHARACTERISTICS</b> |                                          |                                                                                                                                                                                                               |     |      |      |               |
| $R_{F1}$                                     | FET1 On resistance                       | $V_{DD} = 3.3\text{ V}$ , $I_{OUT} = 10\text{ mA}$                                                                                                                                                            |     |      | 5    | $\Omega$      |
| $R_{F2}$                                     | FET2 On resistance                       |                                                                                                                                                                                                               |     |      | 5    |               |
| $R_{F3}$                                     | FET3 On resistance                       | $V_{DD} = 3.3\text{ V}$ , $I_{OUT} = 350\text{ mA}$                                                                                                                                                           |     | 170  | 250  | m $\Omega$    |
| $R_{F4}$                                     | FET4 On resistance                       |                                                                                                                                                                                                               |     | 170  | 250  |               |
| $R_{PDRESETZ}$                               | RESETZ Pull-down resistance              | RESETZ asserted                                                                                                                                                                                               | 33  | 50   | 100  | $\Omega$      |
| $R_{PUCFGOE}$                                | CFG/OE Pull-up resistance <sup>(1)</sup> |                                                                                                                                                                                                               | 1.2 | 2    | 2.6  | M $\Omega$    |
| $R_{PDUART}$                                 | TXC Pull-down resistance                 | See the UART RX and TX Section                                                                                                                                                                                | 80  | 130  | 180  | k $\Omega$    |
| <b>VOLTAGE THRESHOLDS AND AMPLITUDES</b>     |                                          |                                                                                                                                                                                                               |     |      |      |               |
| $V_{HVLO}$                                   | High voltage lockout                     | 3.3V Supply rising                                                                                                                                                                                            | 3.5 | 3.55 | 3.6  | V             |
|                                              | Hysteresis                               |                                                                                                                                                                                                               | 20  | 40   | 60   | mV            |
| $V_{UVLO}$                                   | Under voltage lockout                    | 3.3V Supply rising                                                                                                                                                                                            | 2.7 | 2.75 | 2.8  | V             |
|                                              |                                          | 3.3V Supply falling                                                                                                                                                                                           | 2.4 | 2.45 | 2.5  |               |
| $V_{CPO}$                                    | Charge pump voltage                      | $C_{CPO} = 2\text{ nF}$ , $I_{CPO} = 0\text{ }\mu\text{A}$                                                                                                                                                    | 7   | 8    | 9    | V             |
| $V_{OS}$                                     | Voltage overshoot on OUTA/B              | $C_{OUTB} = 4\text{ }\mu\text{F}$ , $I_{OUTB} = 0\text{ mA}$ ,<br>$C_{OUTA} = 1\text{ }\mu\text{F}$ , $I_{OUTA} = 0\text{ mA}$<br>$V_{DD1} \text{ SR}_{3.3 \rightarrow 4\text{V}} = 10\text{ mV}/\mu\text{s}$ |     |      | 200  | mV            |

(1) CFG/OE is pulled up to  $V_{PUCFGOE}$  through the resistance  $R_{PUCFGOE}$ .

## ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted the specification applies over the  $V_{DD}$  range and operating junction temp  $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ . Typical values are for  $V_{DD} = 3.3\text{V}$  and  $T_J = 25^{\circ}\text{C}$

| PARAMETER                        |                           | TEST CONDITIONS                                       | MIN  | TYP | MAX | UNIT |
|----------------------------------|---------------------------|-------------------------------------------------------|------|-----|-----|------|
| THERMAL SHUTDOWN                 |                           |                                                       |      |     |     |      |
| T <sub>SD</sub>                  | Shutdown temperature      |                                                       | 110  |     | 130 | °C   |
| T <sub>SDHYST</sub>              | Shutdown hysteresis       |                                                       |      | 15  |     | °C   |
| TRANSITION TIMING                |                           |                                                       |      |     |     |      |
| t <sub>d</sub>                   | UVLO to FETn open time    | C <sub>OUTB</sub> = 4 μF,<br>C <sub>OUTA</sub> = 1 μF |      |     | 200 | μs   |
| t <sub>e</sub>                   | UVLO to FETn closed time  |                                                       |      |     | 2   | ms   |
| t <sub>dh</sub>                  | HVLO to FETn open time    |                                                       |      |     | 20  | μs   |
| t <sub>eh</sub>                  | HVLO to FETn closed time  | See The Supply Switch-Over During HVLO Section        |      |     |     |      |
| TRANSITION TIMING (NORMAL MODE)  |                           |                                                       |      |     |     |      |
| t <sub>eb</sub>                  | ENB to FET3/4 closed time | C <sub>OUTB</sub> = 4 μF,<br>C <sub>OUTA</sub> = 1 μF |      |     | 2   | ms   |
| t <sub>db</sub>                  | ENB to FET3/4 open time   |                                                       |      |     | 200 | μs   |
| TRANSITION TIMING (CONTROL MODE) |                           |                                                       |      |     |     |      |
| t <sub>U2R</sub>                 | UVLO to RESETZ time       |                                                       | 5    | 6   | 7   | ms   |
| t <sub>E2R</sub>                 | ENB to RESETZ time        |                                                       |      | 2   | 10  | μs   |
| t <sub>E2O</sub>                 | ENB to FET3/4 open time   | C <sub>OUTB</sub> = 4 μF,<br>C <sub>OUTA</sub> = 1 μF |      | 100 | 200 | μs   |
| t <sub>RX2O</sub>                | RX to FET3/4 closed time  | C <sub>OUTB</sub> = 4 μF,<br>C <sub>OUTA</sub> = 1 μF |      | 0.8 | 2   | ms   |
| t <sub>RX2R</sub>                | RX to RESETZ Time         |                                                       | 5    | 6   | 7   | ms   |
| t <sub>OE2TX</sub>               | OE to TXH Valid Time      |                                                       |      |     | 20  | μs   |
| t <sub>OE2TXZ</sub>              | OE to TXH Hi-Z Time       |                                                       |      |     | 20  | μs   |
| TXC/TXH I/O (CONTROL MODE)       |                           |                                                       |      |     |     |      |
| V <sub>IH</sub>                  | TXC Input logic high      |                                                       | 2    |     |     | V    |
| V <sub>IL</sub>                  | TXC Input logic low       |                                                       |      |     | 0.8 | V    |
| V <sub>OH</sub>                  | TXH Output logic high     |                                                       | 2.25 |     |     | V    |
| V <sub>OL</sub>                  | TXH Output logic low      |                                                       |      |     | 0.4 | V    |
| T <sub>R</sub> / T <sub>F</sub>  | TXH Rise and fall time    | 10-90% CL = 20 pF                                     | 5    |     | 70  | ns   |
| Z <sub>O</sub>                   | TXH Output impedance      |                                                       |      | 35  |     | Ω    |
| f <sub>MAX</sub>                 | TX Input signal frequency |                                                       |      |     | 1   | Mb/s |
| DC                               | TX Duty cycle             |                                                       | 40%  |     | 60% |      |
| RXC/RXH I/O (CONTROL MODE)       |                           |                                                       |      |     |     |      |
| V <sub>IH</sub>                  | RXH Input logic high      |                                                       | 2    |     |     | V    |
| V <sub>IL</sub>                  | RXH Input logic low       |                                                       |      |     | 0.8 | V    |
| V <sub>OH</sub>                  | RXC Output logic high     |                                                       | 2.25 |     |     | V    |
| V <sub>OL</sub>                  | RXC Output logic low      |                                                       |      |     | 0.4 | V    |
| T <sub>R</sub> / T <sub>F</sub>  | RXC Rise and fall time    | 10-90% CL = 20 pF                                     | 20   |     | 120 | ns   |
| f <sub>MAX</sub>                 | RX Input signal frequency |                                                       |      |     | 1   | Mb/s |
| DC                               | RX Duty cycle             |                                                       | 40%  |     | 60% |      |

**FUNCTIONAL BLOCK DIAGRAM****Figure 2. Functional Block Diagram**

## DEVICE INFORMATION

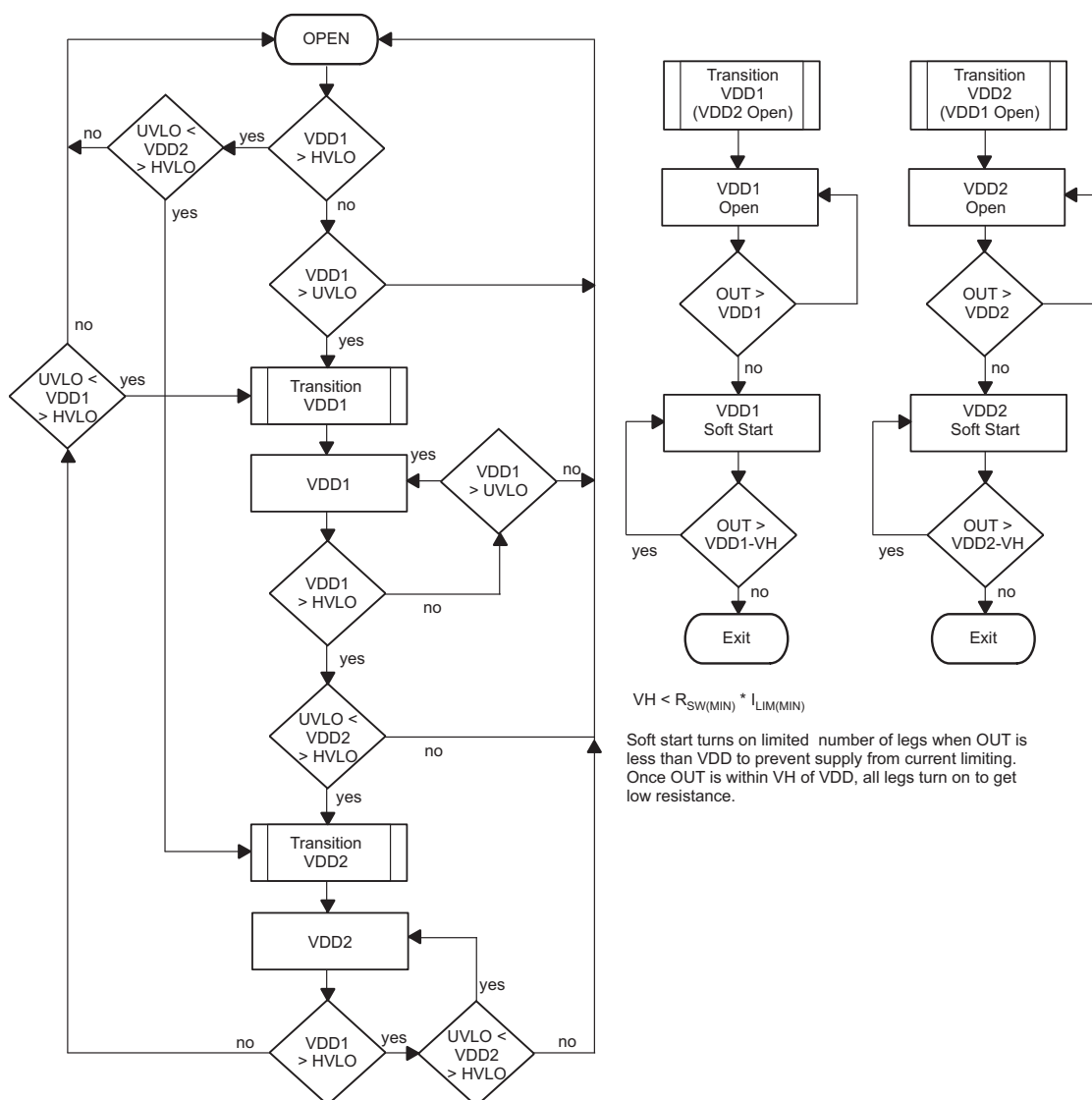
### PIN FUNCTIONS

| PIN NAME | TYPE   | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|----------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDD1     | Supply | <b>Device Supply 1.</b> 0V to 19.8-V Input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| VDD2     | Supply | <b>Device Supply 2.</b> 0V to 19.8-V Input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| OUTA     | Output | <b>Output A.</b> 10-mA capable output. Refer to the <a href="#">Supply Selection</a> section for more information.                                                                                                                                                                                                                                                                                                                                                                                                                |
| OUTB     | Output | <b>Output B.</b> 500-mA capable output. Refer to the <a href="#">Normal Mode</a> and <a href="#">Control Mode</a> sections for more information.                                                                                                                                                                                                                                                                                                                                                                                  |
| CPO      | Output | <b>Charge Pump Output.</b> This pin is the output of the internal charge pump. It drives the gates of the internal FET switches. Connect a capacitor of at least 2nF to this pin.                                                                                                                                                                                                                                                                                                                                                 |
| CFG/OE   | Input  | <b>Mode Configuration/Output Enable.</b> When CFG is floating, the device is in Normal Mode. When CFG is ground, the device is in Control Mode (see the <a href="#">APPLICATION INFORMATION</a> section for more information). The mode is latched at power-up. When the device enters Control Mode, this pin becomes an output enable for the UART TXH output. See the <a href="#">UART RX and TX</a> section for more information. A pull-down resistance between this pin and GND is recommended when Control Mode is desired. |
| RXH      | Input  | <b>UART RX Input.</b> Monitored Input for data activity to enable outputs. In Control Mode, this pin is monitored for a high to low transition to enable the outputs. This input is level shifted and driven on RXC. See the <a href="#">UART RX and TX</a> section for more information.                                                                                                                                                                                                                                         |
| RXC      | Output | <b>UART RX Output.</b> This output is a level shifted version of RXH. RXC is referenced to OUTA. See the <a href="#">UART RX and TX</a> section for more information.                                                                                                                                                                                                                                                                                                                                                             |
| TXC      | Input  | <b>UART TX Input.</b> This input is buffered and level shifted on TXH. See the <a href="#">UART RX and TX</a> section for more information.                                                                                                                                                                                                                                                                                                                                                                                       |
| TXH      | Output | <b>UART TX Output.</b> This output is a buffered and level shifted version of TXC. TXH is referenced to OUTA. See the <a href="#">UART RX and TX</a> section for more information.                                                                                                                                                                                                                                                                                                                                                |
| RESETZ   | Output | <b>Microcontroller Reset.</b> This pin is a delayed reset signal indicating OUTB is connected to a valid VDD. RESETZ in an open-drain pull-down. RESETZ is low when OUTB is high impedance.                                                                                                                                                                                                                                                                                                                                       |
| ENB      | Input  | <b>OUTB Enable.</b> In Normal Mode, this pin is the active high OUTB enable. In Control Mode, this pin opens OUTB when asserted high and resets the device until a new transition on RX occurs.                                                                                                                                                                                                                                                                                                                                   |
| GND      | Supply | <b>Device ground.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

## APPLICATION INFORMATION

## Supply Selection

The TPS22985 selects between two separate power supplies, VDD1 or VDD2, and connects these to two outputs (OUTA and OUTB) through non-current limited switches. When a valid VDD ( $V_{UVLO} < VDD < V_{HVL0}$ ) is present on VDD1, VDD1 will be connected to the outputs. When  $VDD1 > V_{HVL0}$ , the TPS22985 will connect the outputs to VDD2 when a valid VDD is present on this input. OUTB is also opened and closed by other digital inputs, ENB and RXH, depending on the mode of the TPS22985. Refer to the [Normal Mode](#) and [Control Mode](#) sections for more information on the control of OUTB. VDD1 and VDD2 can power up in any order; however, VDD1 always takes priority over VDD2 and only allows VDD2 to connect when the  $VDD1 > V_{HVL0}$  condition is present. When the outputs are connected to VDD2, and VDD1 drops below  $V_{HVL0}$ , the TPS22985 will disconnect the outputs from VDD2. [Figure 3](#) shows a flow diagram illustrating the selection of VDD1 or VDD2 as the appropriate supply to connect to OUTA and OUTB. Note, this diagram does not show the enabling and disabling of OUTB by ENB and RXH.



**Figure 3. Flow Diagram of Supply Selection and Switch-Over**

## Normal Mode

When the CFG/OE pin is floating at power-up, the device enters Normal Mode. In Normal Mode, the TPS22985 provides power via OUTA and OUTB.

OUTA is connected whenever a valid VDD is present on VDD1. OUTA may also be connected if  $VDD1 > V_{HVLO}$  and a valid VDD is connected to VDD2. OUTB is connected whenever a valid VDD is present on VDD1. OUTB may also be connected if  $VDD1 > V_{HVLO}$ , a valid VDD is connected to VDD2, and the control signal ENB is high. When OUTB is connected it will supply  $\geq 500$  mA to a load.

When a valid VDD is not present, the TPS22985 enters into a shutdown mode and blocks current flow through the switches.

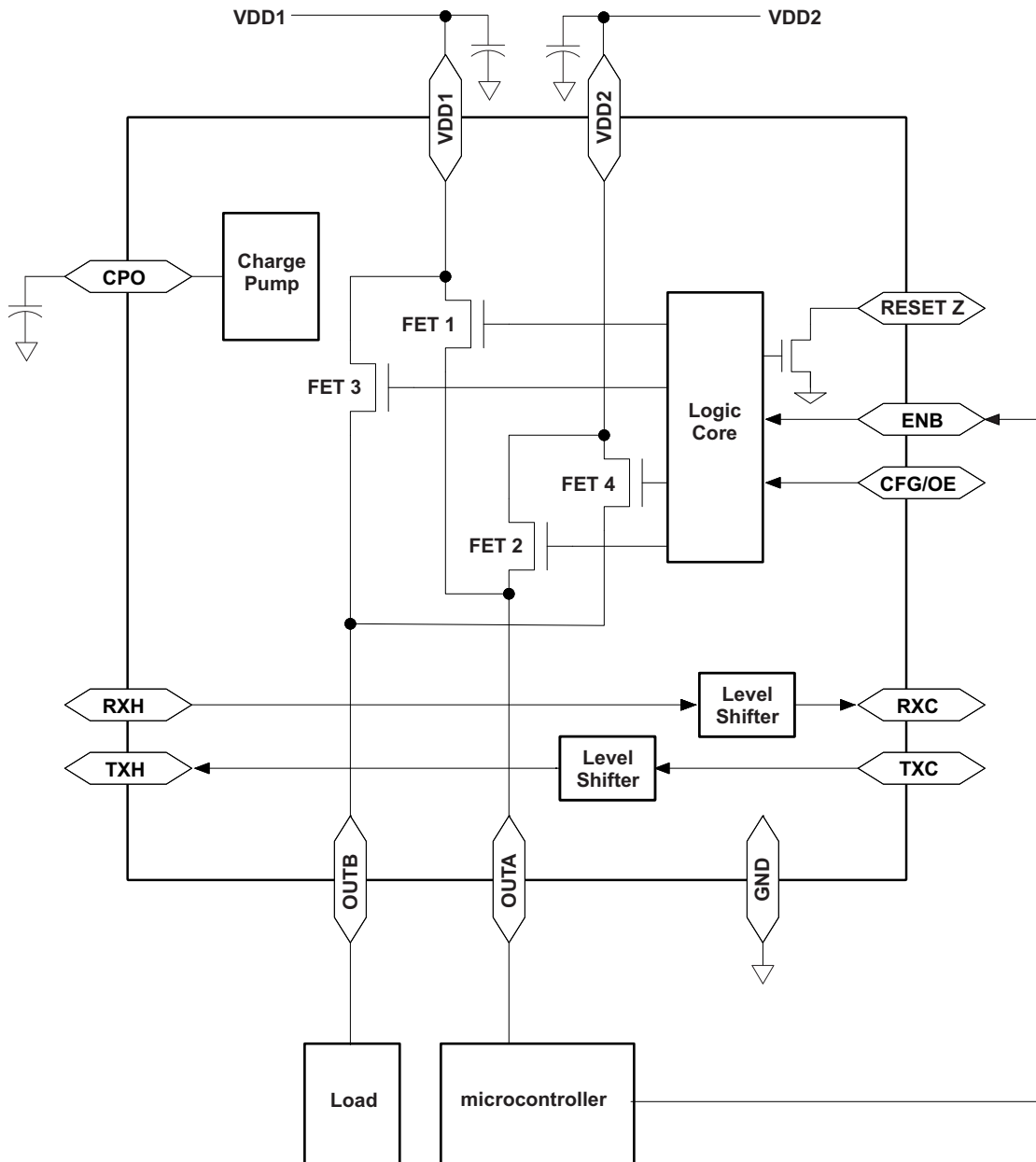


Figure 4. Normal Mode Typical Application

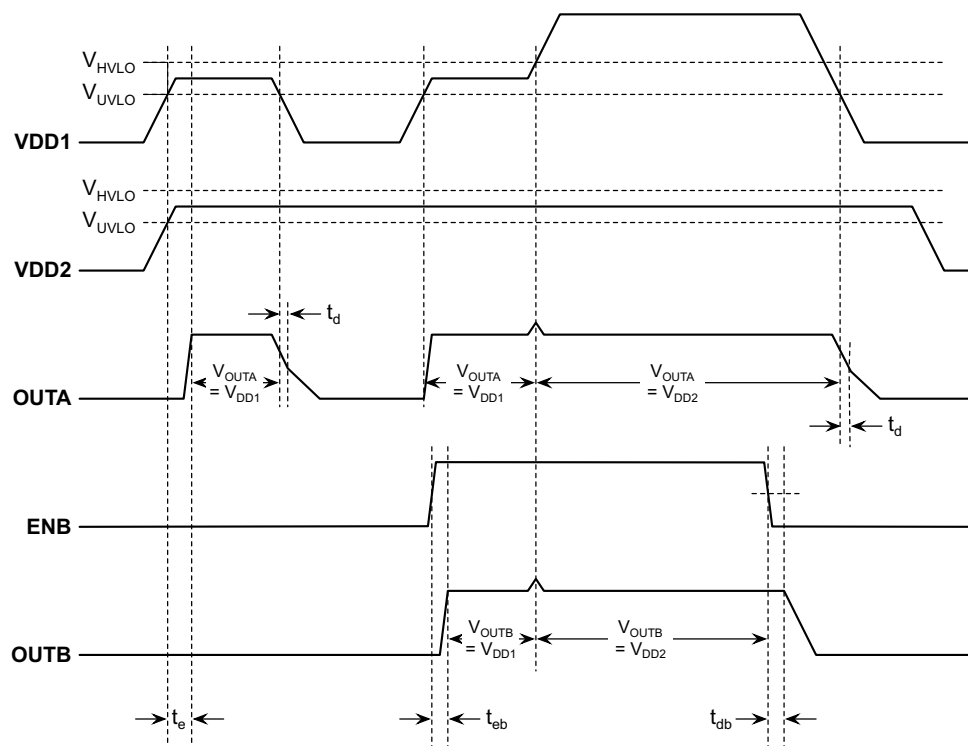


Figure 5. Timing During Normal Mode

## Control Mode

When CFG/OE pin is grounded at power-up, the device latches into Control Mode. In Control Mode, the TPS22985 provides power to a microcontroller/CDR device.

When a valid VDD is connected, OUTA and OUTB are connected to the VDD. OUTB remains connected to VDD until ENB transitions high. OUTA remains connected to VDD as long as a valid VDD exists. RESETZ indicates that a valid VDD is available at OUTB. When RESETZ is low, a valid VDD is not available, if RESETZ is high, a valid VDD is available.

When ENB transitions high, RESETZ is asserted low and OUTB is opened until a falling edge on RXH is detected, as illustrated in Figure 7 and Figure 8. When ENB transitions high, RESETZ will assert low after time  $t_{E2R}$  and OUTB will open after time  $t_{E2O}$ . During the time  $t_{E2O}$ , RXH is not monitored. After the time  $t_{E2O}$ , the TPS22985 starts monitoring RXH for a falling edge. When a falling edge occurs and a valid VDD is available, RESETZ is transitioned from low to high and OUTB is connected to VDD until ENB transitions high again or until no valid VDD is available. When a valid VDD is not available, RESETZ is asserted low and the TPS22985 blocks current flow through the switches.

After the device is latched into Control Mode, the CFG/OE pin becomes the output enable for the TX buffer/level-shifter. Refer to the [UART RX and TX](#) section for more information.

OUTA can be used as a pull-up for the Thunderbolt™ CFG2 connector pin as an indicator that power is available to the cable active circuitry. Place a resistor greater than 1kΩ between OUTA and CFG2 in this case.

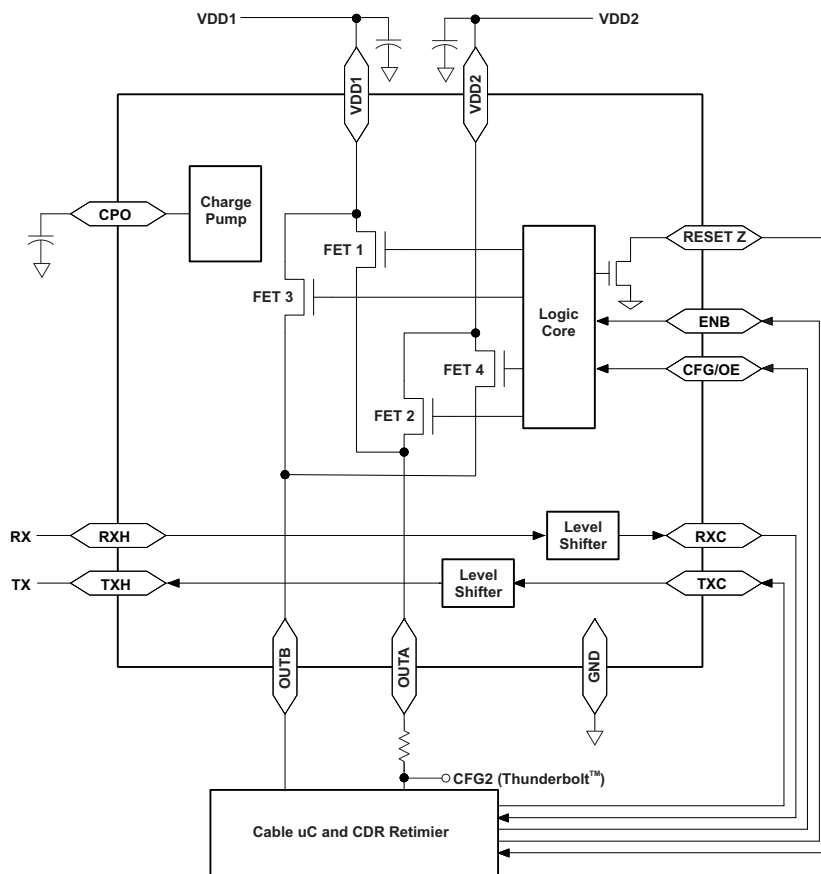


Figure 6. Control Mode Typical Application

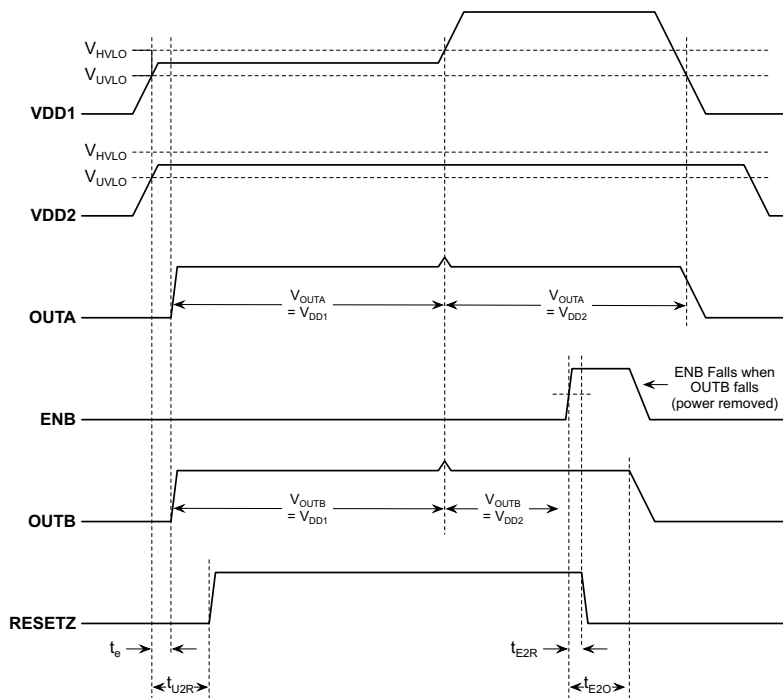


Figure 7. Timing During Control Mode

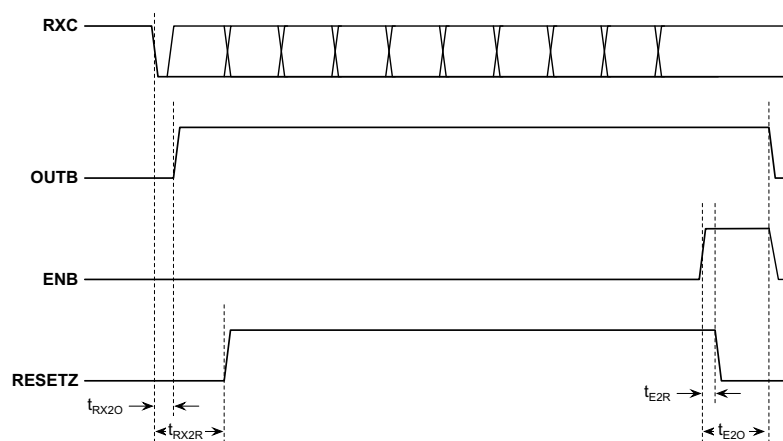
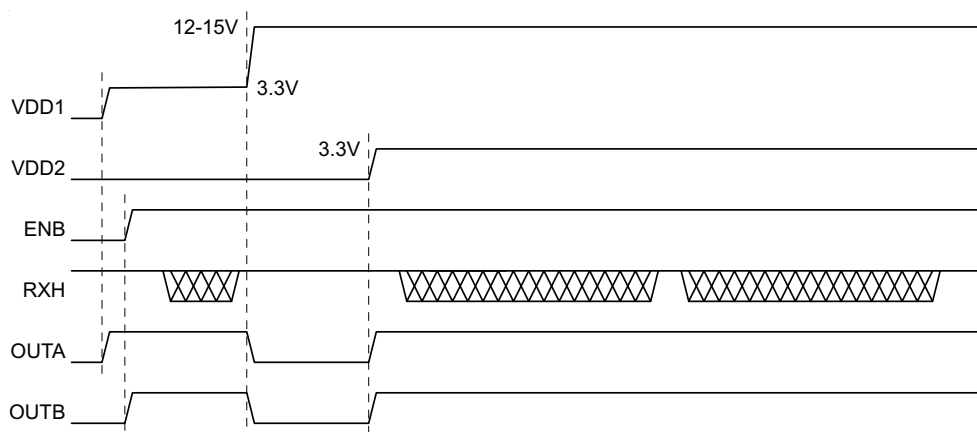
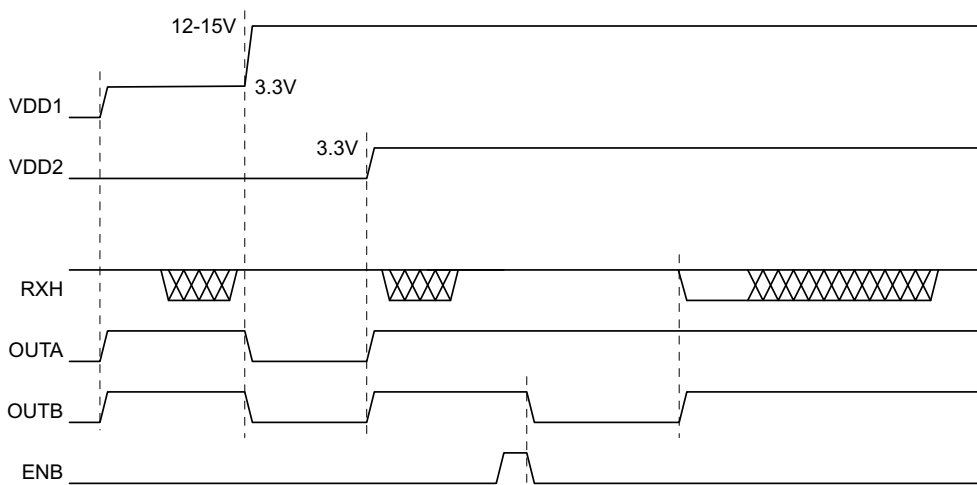


Figure 8. Timing During Control Mode Continued

## Typical Startup



**Figure 9. Typical Startup in Normal Mode**



**Figure 10. Typical Startup Timing for Control Mode**

**Figure 10. Typical Startup Timing for Control Mode**

## Soft Start

To prevent inrush current to the load, the TPS22985 soft starts OUTA and OUTB. When OUTA and OUTB are first enabled, the resistance of the FET switches (FET1, FET2, FET3, and FET4) starts high and reduces every 250 $\mu$ s in four steps. [Figure 11](#) shows the nominal resistance ramp profile for OUTB. The resistance shown in this figure is the equivalent resistance through FET3 and FET4 in [Figure 2](#).

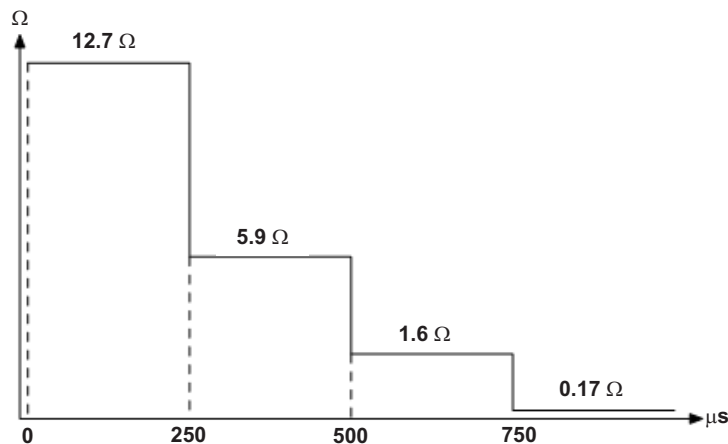


Figure 11. OUTB Soft Start Resistance vs Time Profile

## Supply Switch-Over During HVLO

When OUTA and OUTB are connected to VDD1 and VDD1 crosses  $V_{HVLO}$ , the TPS22985 will open the FET1/3 switches. Due to the delay  $t_{dh}$ , the output will overshoot  $V_{HVLO}$  by  $V_{OS}$ . When a valid VDD is present on VDD2, OUTA and OUTB will connect to VDD2 after time  $t_{eh}$ . Figure 12 illustrates this switch-over event.

The overshoot  $V_{OS}$  will occur when the VDD (VDD1 or VDD2) that is connected to the output transitions above  $V_{HVLO}$ .  $V_{OS}$  is set by the delay  $t_{dh}$  and the slew rate of the connected VDD. However, the connection of the outputs to VDD2 will only occur when VDD1 transitions above  $V_{HVLO}$  and VDD2 is a valid VDD.

The following equation determines the overshoot  $V_{OS}$ .

$$V_{OS} = SR_{VDD} \times t_{DH} \quad (1)$$

$SR_{VDD}$  is the slew rate of the supply that is transitioning above  $V_{HVLO}$ . As an example, when  $SR_{VDD}$  is 10mV/ $\mu$ s and  $t_{dh}$  is 20 $\mu$ s,  $V_{OS}$  is 200mV.

When switching to VDD2 due to an HVLO event on VDD1, the outputs OUTA and OUTB are discharged by their respective loads until they reach the VDD2 voltage. This prevents in-rush current when charging the output caps. The discharge time  $t_{eh}$  is variable and is determined by the following equation.

$$t_{eh} = t_{dh} + (V_{HVLO} + V_{OS} - V_{DD2}) \times C_{LOAD} / I_{LOAD} \quad (2)$$

In this equation,  $V_{OS}$  is determined by Equation 1,  $C_{LOAD}$  is the load capacitance at the respective output, and  $I_{LOAD}$  is load current flowing out of the same output. As an example, when VDD2 is 3.3V,  $t_{dh}$  is 20 $\mu$ s,  $V_{OS}$  is 200mV,  $C_{LOAD}$  is 4 $\mu$ F, and  $I_{LOAD}$  is 350mA, the resulting  $t_{eh}$  is 25.7 $\mu$ s.

Note, when VDD1 transitions above  $V_{HVLO}$  and a valid VDD is not present on VDD2, the outputs will open and will discharge through each respective load.

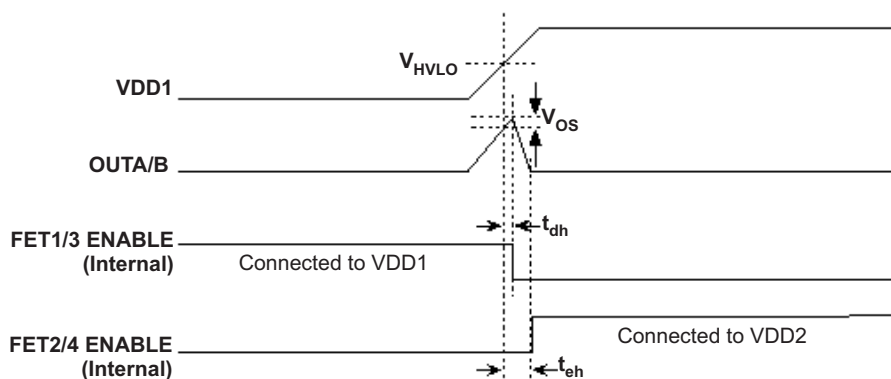


Figure 12. VDD switch-over at VDD1 rising above  $V_{HVLO}$

## UART RX and TX

The TPS22985 provides failsafe buffers for digital UART RX and TX lines. The failsafe mechanism prevents the RX and TX lines from being loaded when power is removed from the device. The RX line is divided into a host side RXH input and a cable side RXC output. The TX line is divided into host side TXH output and a cable side TXC input.

The RXH and TXC inputs are used in Control Mode only and must be pulled low when the device is in Normal Mode. In Normal Mode, leave the RXH and TXC pins disconnected from the UART signal lines and pull low through a  $> 1k\Omega$  resistance.

In Control Mode, when the TPS22985 is unpowered or when RESETZ is asserted low, the TXH output is high impedance. This prevents loading the system TX line and allowing other devices on the UART bus to communicate. The RXC output is pulled low through the output driver during this same condition.

Figure 13 illustrates the RXC and TXH control when in Control Mode. When RESETZ is high, CFG/OE controls TXH. When CFG/OE is low, TXH is high impedance. When CFG/OE is high, TXH is a buffered and level-shifted TXC. The CFG/OE, ENB, and TXC inputs are ignored when RESETZ is asserted low. Figure 14 shows the delay from CFG/OE to TXH.

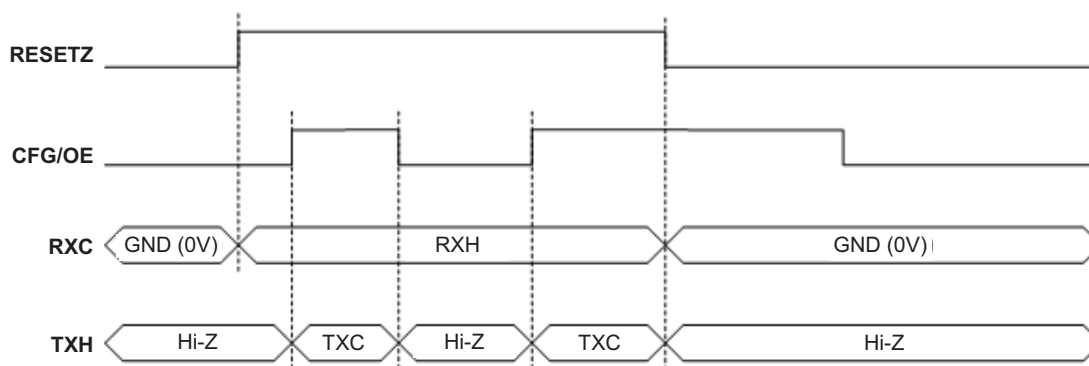


Figure 13. UART RX and TX Buffer Control During Control Mode

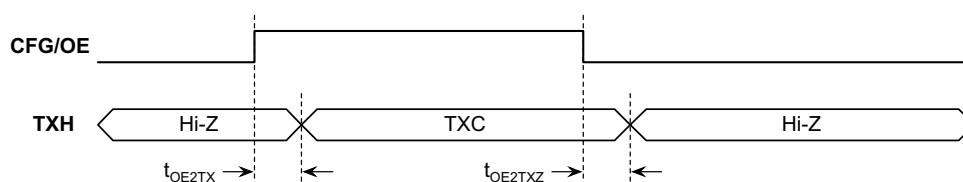
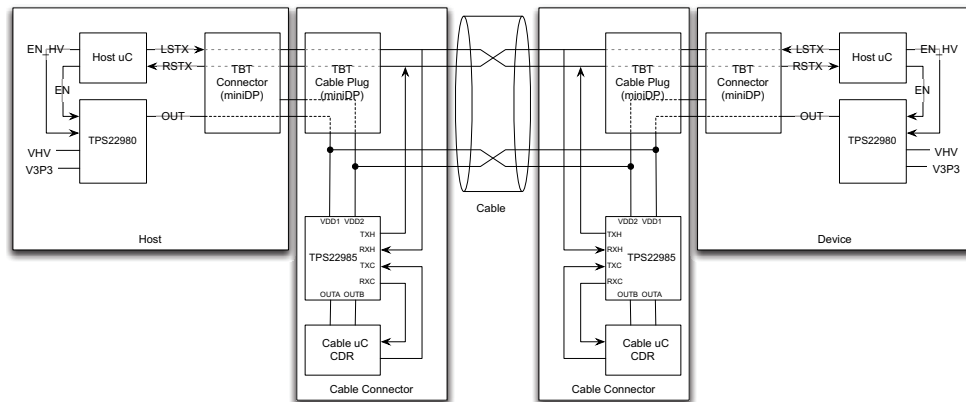


Figure 14. CFG/OE to TXH Timing During Control Mode

## THUNDERBOLT™ SYSTEM WITH TPS22980/TPS22985



**Figure 15. Thunderbolt System with TPS22980/TPS22985**

PACKAGING INFORMATION

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS22985YFPR          | NRND          | Production           | DSBGA (YFP)   16 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | 9U                  |
| TPS22985YFPR.A        | NRND          | Production           | DSBGA (YFP)   16 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | 9U                  |
| TPS22985YFPR.B        | NRND          | Production           | DSBGA (YFP)   16 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | 9U                  |

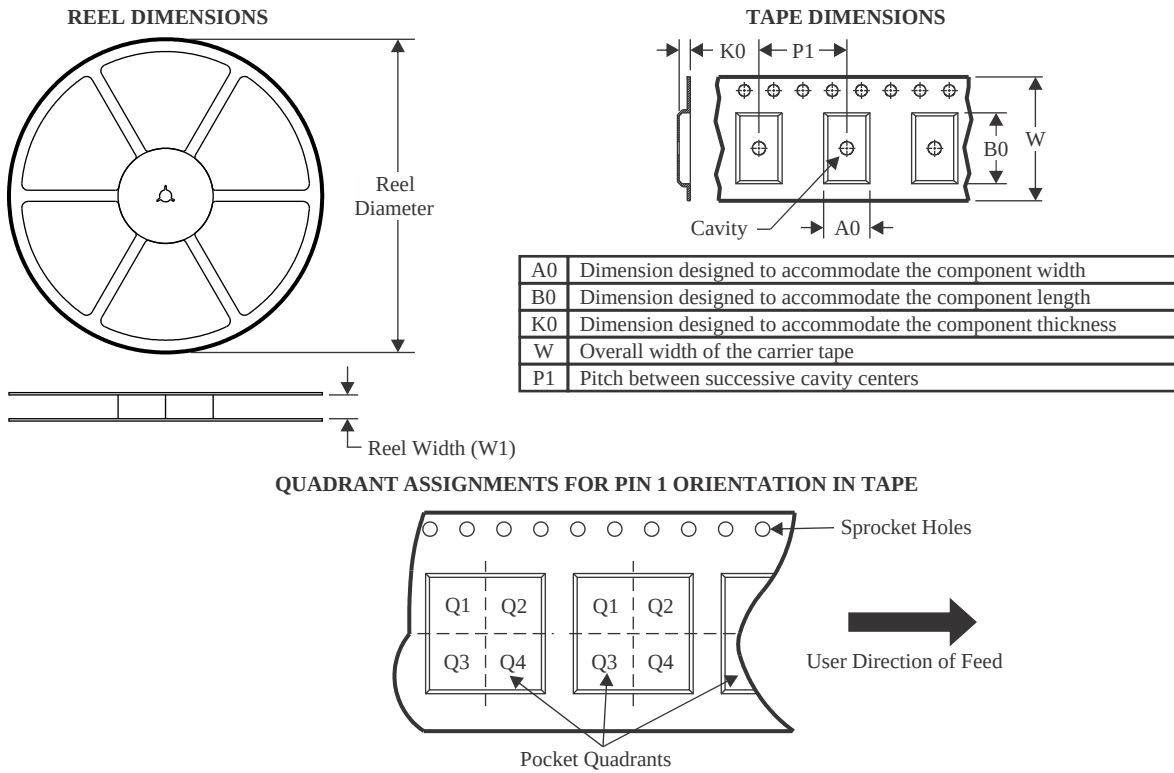
- <sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).
- <sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- <sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- <sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- <sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- <sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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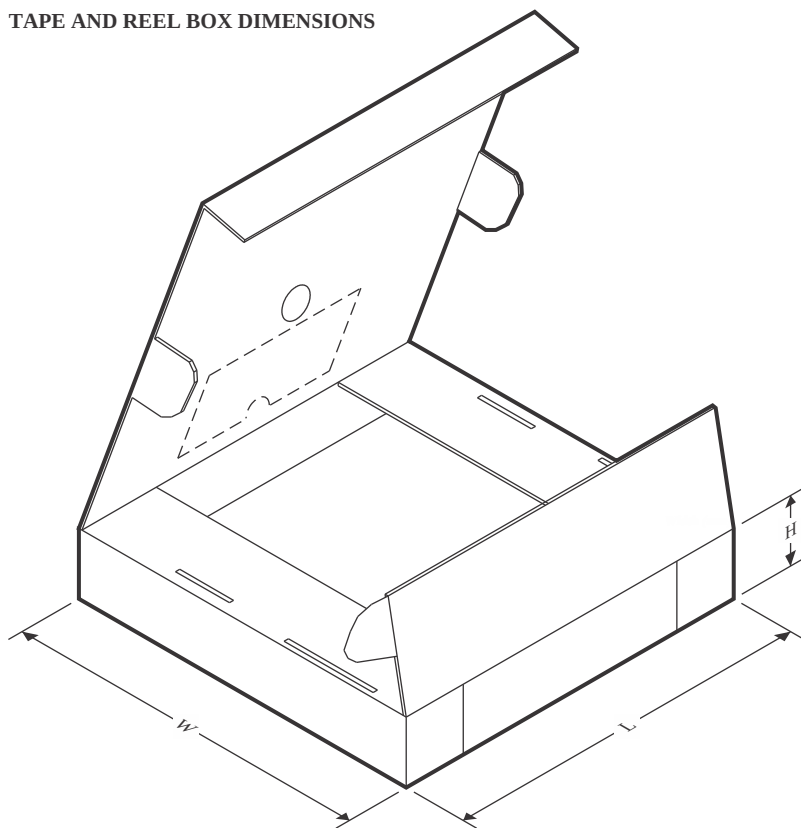
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS22985YFPR | DSBGA        | YFP             | 16   | 3000 | 180.0              | 8.4                | 1.71    | 1.71    | 0.81    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS22985YFPR | DSBGA        | YFP             | 16   | 3000 | 182.0       | 182.0      | 20.0        |

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