SNx5C3232E 3-V To 5.5-V Two-Channel RS-232 1-MBIT/S Line Drivers and Receivers With ±15-kV IEC ESD Protection

1 Features

- Operate with 3-V to 5.5-V V_{CC} supply
- Operate up to 1 Mbit/s
- Low supply current . . . 300 µA typical
- External capacitors . . . 4 × 0.1 µF
- Accept 5-V logic input with 3.3-V supply
- Latch-up performance exceeds 100 mA Per JESD 78, class II
- ESD protection for RS-232 pins
  - ±15-kV Human-body model (HBM)
  - ±15-kV IEC 61000-4-2 Air-gap discharge
  - ±8-kV IEC 61000-4-2 Contact discharge

2 Applications

- Industrial PCs
- Wired networking
- Data center and enterprise computing
- Battery-powered systems
- PDAs
- Notebooks
- Palmtop PCs
- Hand-held equipment

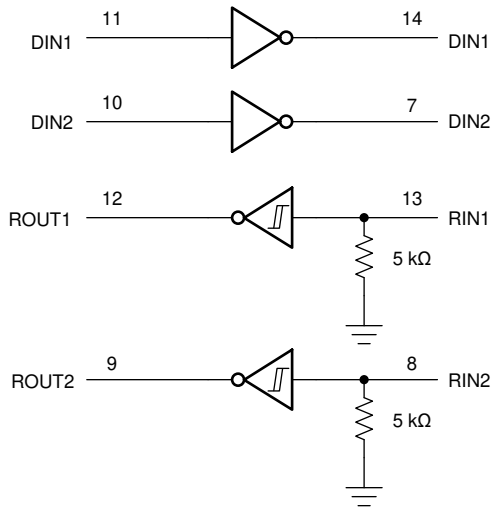
3 Description

The SN65C3232E and SN75C3232E consist of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). These devices provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 1 Mbit/s and a driver output slew rate of 14 V/µs to 150 V/µs.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN65C3232E SN75C3232E	D (SOIC)	9.90 mm x 3.91 mm
	DB (SSOP)	6.20 mm x 5.30 mm
	DW (SOIC)	10.3 mm x 7.50 mm
	PW (TSSOP)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2007) to Revision B (June 2021)	Page
• Added *Device Information* table, *Pin Configuration and Functions* section, *Thermal Information* tables, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Updated the list of *Applications*	1
• Added a note specifying a minimum capacitor of 1 µF between V_{CC} and GND to satisfy IEC ESD specifications in the *ESD Protection, Driver* table	4
• Added a note specifying the need for a 1-µF capacitor between V_{CC} and GND to satisfy IEC ESD specifications in the *ESD Protection, Receiver* table	4

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5 Pin Configuration and Functions

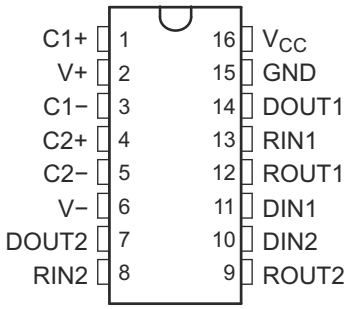

Figure 5-1. D, DB, DW, or PW Package (Top View)

Table 5-1. Pin Functions

PIN		I/O[(1)]	DESCRIPTION
NAME	D, DB, DW or PW		
C1+	1	-	Positive lead of C1 capacitor
V+	2	O	Positive charge pump output for storage capacitor only
C1-	3	-	Negative lead of C1 capacitor
C2+	4	-	Positive lead of C2 capacitor
C2-	5	-	Negative lead of C2 capacitor
V-	6	O	Negative charge pump output for storage capacitor only
DOUT2	7	O	RS232 line data output (to remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT2	9	O	Logic data output (to UART)
DIN2	10	I	Logic data input (from UART)
DIN1	11	I	Logic data input (from UART)
ROUT1	12	O	Logic data output (to UART)
RIN1	13	I	RS232 line data input (from remote RS232 system)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
GRD	15	-	Ground
V_{CC}	16	-	Supply Voltage, Connect to external 3-V to 5.5-V power supply
Thermal Pad	-	-	Exposed thermal pad. Can be connected to GND or left floating.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) see [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range[2]		–0.3	6	V
V+	Positive output supply voltage range[2]		–0.3	7	V
V–	Negative output supply voltage range[2]		0.3	–7	V
V+ – V–	Supply voltage difference[2]			13	V
V_I	Input voltage range	Drivers	–0.3	6	V
		Receivers	–25	25	
V_O	Output voltage range	Drivers	–13.2	13.2	V
		Receivers	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute MaximumRatings do not imply functional operation of the device at these or any other conditions beyond those listed underRecommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability,functionality, performance, and shorten the device lifetime..
(2) All voltages are with respect to network GND.

6.2 ESD Protection

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1].	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Protection, Driver

PIN		TEST CONDITIONS	TYP	UNIT
NAME	NO.			
DOUT	7, 14	HBM, per ANSI/ESDA/JEDEC JS-001	±15	kV
		IEC 61000-4-2 Air-Gap Discharge [1]	±15	
		IEC 61000-4-2 Contact Discharge [1]	±8	

(1) For D, DB, PW packages of SN65C3232E and PW package of SN75C3232E: A minimum of 1-µF capacitor is needed between VCC and GND to meet the specified IEC ESD level

6.4 ESD Protection, Receiver

PIN		TEST CONDITIONS	TYP	UNIT
NAME	NO.			
RIN	8, 13	HBM, per ANSI/ESDA/JEDEC JS-001	±15	kV
		IEC 61000-4-2 Air-Gap Discharge [1]	±15	
		IEC 61000-4-2 Contact Discharge [1]	±8	

(1) For D, DB, PW packages of SN65C3232E and PW package of SN75C3232E: A minimum of 1-µF capacitor is needed between VCC and GND to meet the specified IEC ESD level

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6.5 Recommended Operating Conditions

see note (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver high-level input voltage	DIN	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver low-level input voltage		DIN			0.8	V
V_I	Driver input voltage		DIN	0		5.5	V
	Receiver input voltage			–25		25	
T_A	Operating free-air temperature		SN65C3232E	–40		85	°C
			SN75C3232E	0		70	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V (see Figure 9-1).

6.6 Thermal Information, SN65C3232E

THERMAL METRIC(1)		SN65C3232E				UNIT
		PW (TSSOP)	D (SOIC)	DW (SOIC)	DB (SSOP)	
		16 Pins	16 Pins	16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.0	85.9	57.0	103.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.0	43.1	33.5	49.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.4	44.5	37.1	54.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	10.1	7.5	12.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	44.1	37.1	54.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.7 Thermal Information, SN75C3232E

THERMAL METRIC(1)		SN75C3232E				UNIT
		PW (TSSOP)	D (SOIC)	DW (SOIC)	DB (SSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.0	82.0	57.0	46.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.0	36.7	33.5	36.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.4	33.6	37.1	43.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	4.2	7.5	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	33.3	37.1	42.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

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6.8 Electrical Characteristics, Power

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS[2]		MIN	TYP[1]	MAX	UNIT
I_{CC}	Supply current	No load,	V_{CC} = 3.3 V or 5 V		0.3	1	mA

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V (see Figure 9-1).

6.9 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS[3]		MIN	TYP[1]	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND	5	5.5		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}	–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}			±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	µA
I_{OS} [2]	Short-circuit output current	V_{CC} = 3.6 V,	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V		±35	±90	
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V	300	10M		Ω

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
(3) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V (see Figure 9-1) .

6.10 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS[2]	MIN	TYP[1]	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.2		V
		V_{CC} = 5 V	0.8	1.5		
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			0.3		V
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V (see Figure 9-1).

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6.11 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS[3]			MIN	TYP[1]	MAX	UNIT
	Maximum data rate (see Figure 7-1)	R_L = 3 kΩ, One DOUT switching	C_L = 250 pF,	V_{CC} = 3 V to 4.5 V	1000			kbit/s
			C_L = 1000 pF,	V_{CC} = 3.5 V to 5.5 V	1000			
$t_{sk(p)}$	Pulse skew[2]	C_L = 150 pF to 2500 pF, R_L = 3 kΩ to 7 kΩ, See Figure 7-2				300		ns
SR(tr)	Slew rate, transition region (see Figure 7-1)	R_L = 3 kΩ to 7 kΩ, C_L = 150 pF to 1000 pF, V_{CC} = 3.3 V			14		150	V/µs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V (see Figure 9-1).

6.12 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS[3]	TYP[1]	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF	300	ns
t_{PHL}	Propagation delay time, high- to low-level output		300	ns
$t_{sk(p)}$	Pulse skew[2]		300	ns

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V (see Figure 9-1).

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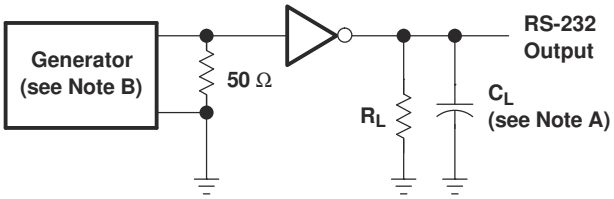
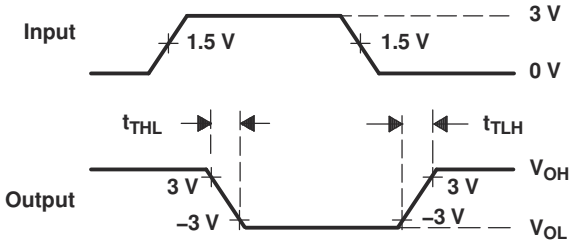
7 Parameter Measurement Information



TEST CIRCUIT

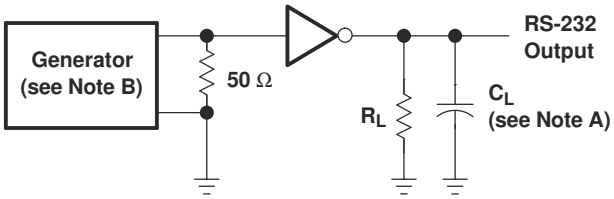


VOLTAGE WAVEFORMS

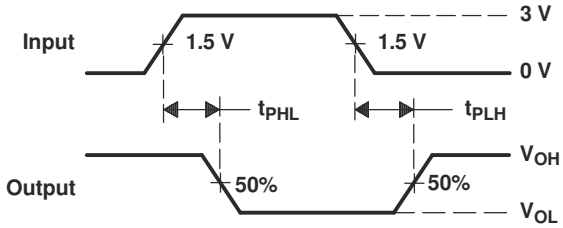
$$SR(tr) = \frac{6\ V}{t_{THL}\ \text{or}\ t_{TLH}}$$

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 7-1. Driver Slew Rate



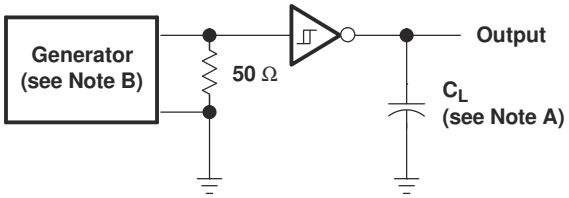
TEST CIRCUIT



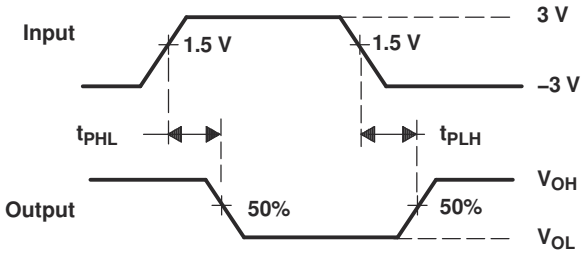
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 7-2. Driver Pulse Skew



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 7-3. Receiver Propagation Delay Times

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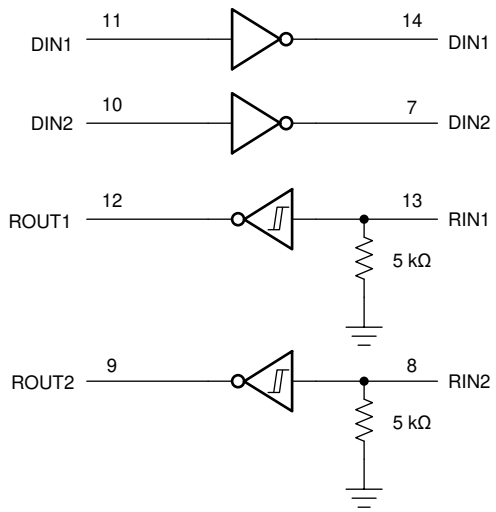
8 Detailed Description

8.1 Overview

The SNx5C3232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV IEC ESD protection between serial-port connection terminals and GND. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from one 3-V to 5.5-V supply. The device operates at data signaling rates up to 1 Mbps and a maximum of 150-V/µs driver output slew rate. Outputs are protected against shorts to ground.

8.1.1 Functional Block Diagram



8.1.2 Feature Description

8.1.2.1 Power

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors.

8.1.2.2 RS232 Driver

Two drivers interface the standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

8.1.2.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input results in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

8.1.3 Device Functional Modes

Table 8-1. Each Driver

INPUT DIN[(1)]	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

Table 8-2. Each Receiver

INPUT RIN[(1)]	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,
Open = input disconnected or connected driver off

8.1.3.1 V_{CC} Powered by 3 V to 5.5 V

The device is in normal operation.

8.1.3.2 V_{CC} Unpowered, V_{CC} = 0 V

When the SNx5C3232E device is unpowered, it can be safely connected to an active remote RS232 device.

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9 Application and Implenentation

Note

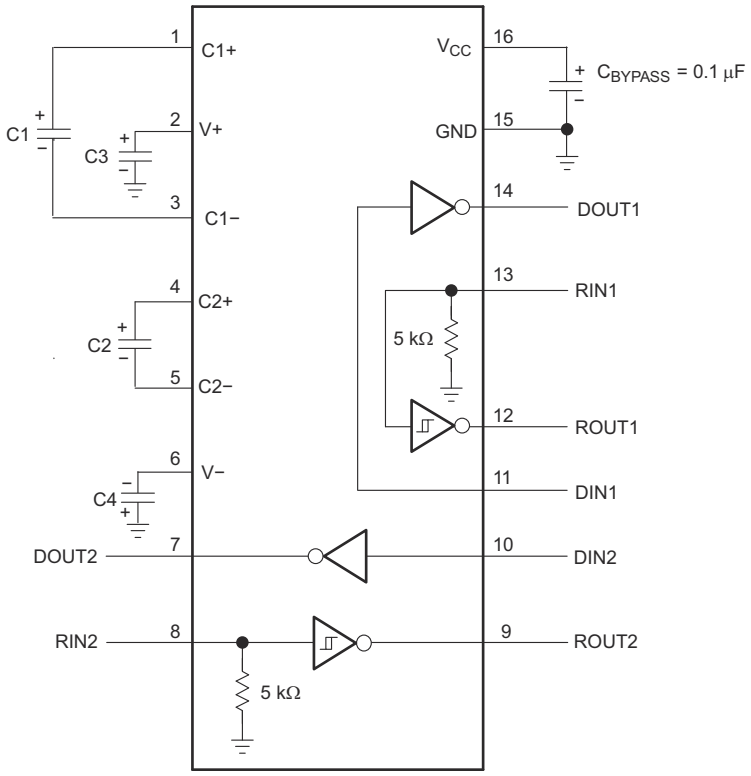
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SNx5C3232E device is designed to convert single-ended signals into RS232-compatible signals, and vice-versa. This device can be used in any application where an RS232 line driver or receiver is required.

ROUT and DIN connect to UART or general-purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable.

Typical Application



A. C3 can be connected to V_{CC} or GND.

Figure 9-1. Typical Operating Circuit and Capacitor Values

Table 9-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

9.2.1 Design Requirements

- Recommended V_{CC} is 3.3 V or 5 V
  - 3 V to 5.5 V is also possible
- Maximum recommended bit rate is 1 Mbps

9.2.2 Detailed Design Procedure

All DIN inputs must be connected to valid low or high logic levels. Select capacitor values based on V_{CC} level for best performance.

9.2.3 Application Performance Plots

VCC must be between 3 V and 5.5 V. Charge pump capacitors must be chosen using V_{CC} vs Capacitor Values

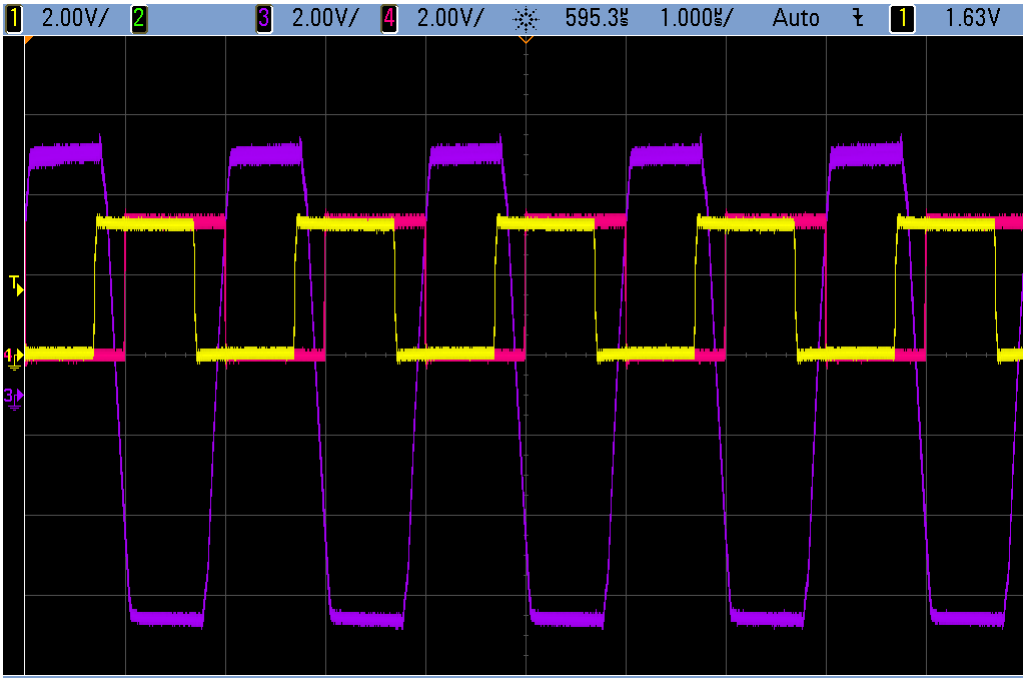


Figure 9-2. 1 Mbps timing waveform from driver input to receiver output loopback. DOUT to RIN trace is in purple, DIN trace is in yellow and ROUT trace is in pink

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10 Power Supply Recommendations

The supply voltage, V_{CC}, should be between 3 V and 5.5 V. Select the charge-pump capacitors using V_{CC} vs Capacitor Values.

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short, specifically on the C1 and C2 nodes that have the fastest rise and fall times.

11.2 Layout Example

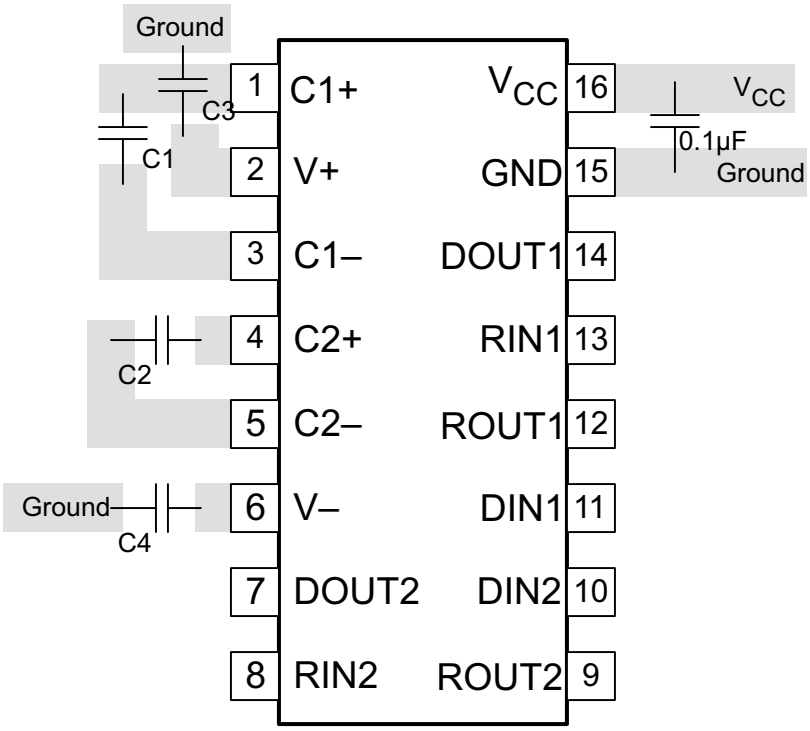

Figure 11-1. Layout Diagram

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65C3232EDBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU232E
SN65C3232EDBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU232E
SN65C3232EDBRG4	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU232E
SN65C3232EDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3232E
SN65C3232EDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3232E
SN65C3232EDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3232E
SN65C3232EDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3232E
SN65C3232EDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3232E
SN65C3232EDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3232E
SN65C3232EDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3232E
SN65C3232EPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU232E
SN65C3232EPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU232E
SN65C3232EPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU232E
SN65C3232EPWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU232E
SN75C3232EDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3232E
SN75C3232EDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3232E
SN75C3232EDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3232E
SN75C3232EDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3232E
SN75C3232EPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	MY232E
SN75C3232EPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MY232E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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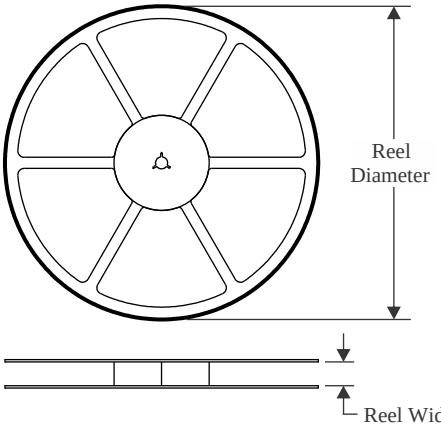
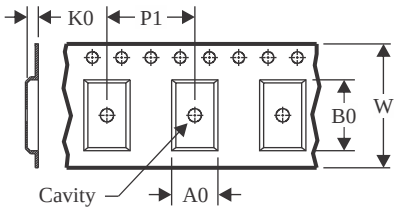
TAPE AND REEL INFORMATION

REEL DIMENSIONS

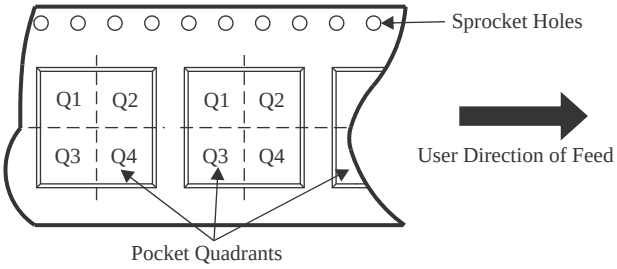


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

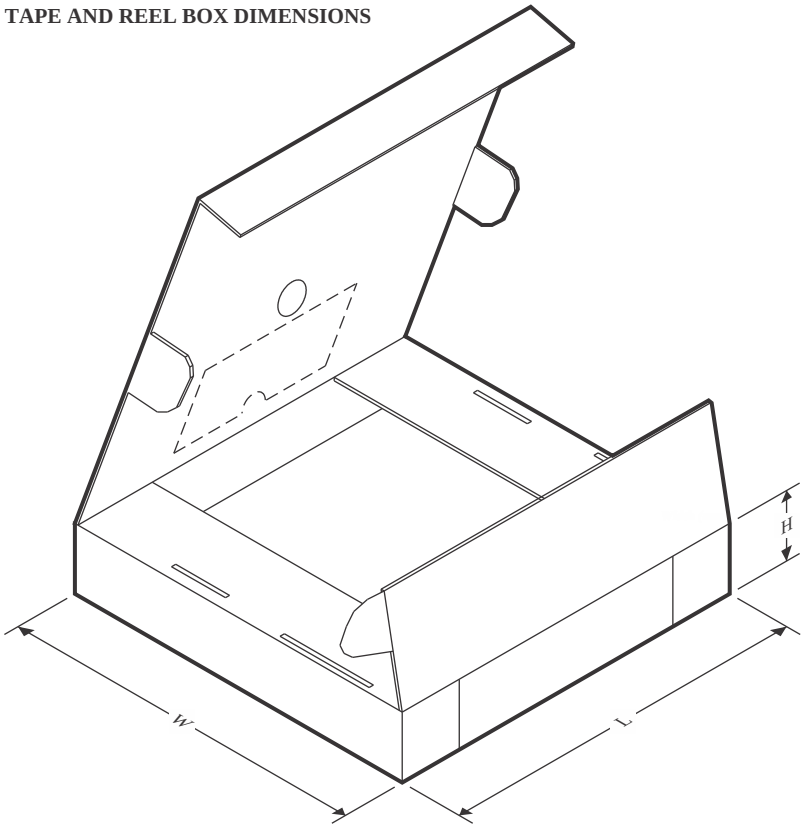
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3232EDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN65C3232EDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65C3232EDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN65C3232EPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C3232EPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75C3232EDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN75C3232EPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

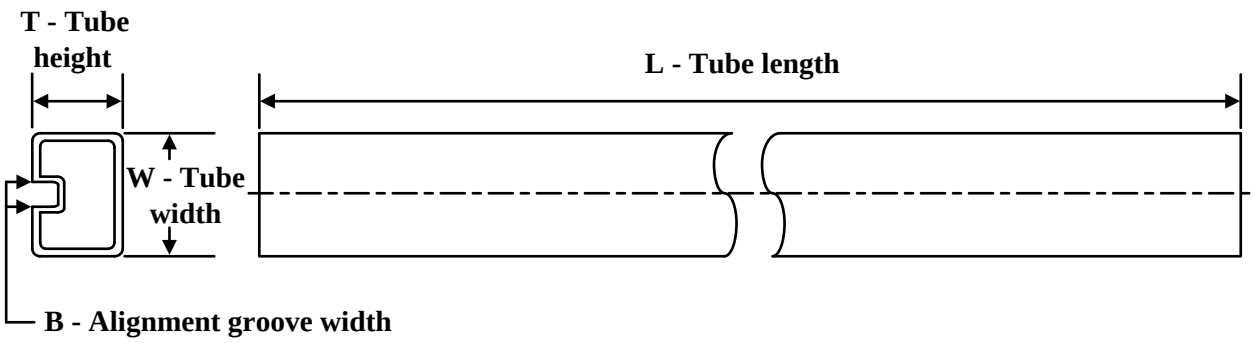
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3232EDBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN65C3232EDR	SOIC	D	16	2500	356.0	356.0	35.0
SN65C3232EDWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN65C3232EPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN65C3232EPWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN75C3232EDWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN75C3232EPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

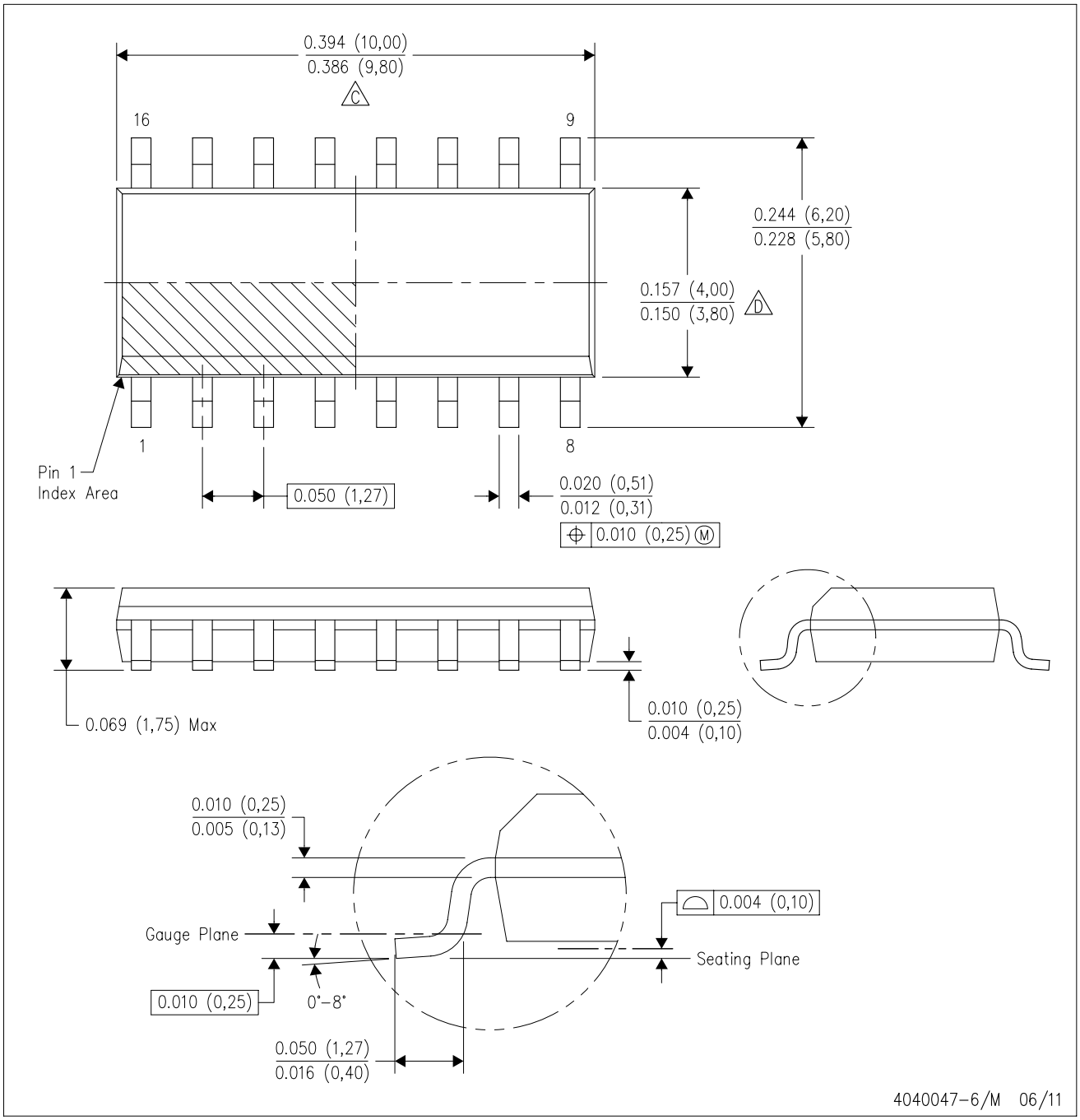
TUBE



*All dimensions are nominal

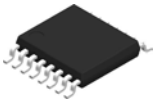
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65C3232EDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
SN65C3232EDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
SN75C3232EDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
SN75C3232EDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

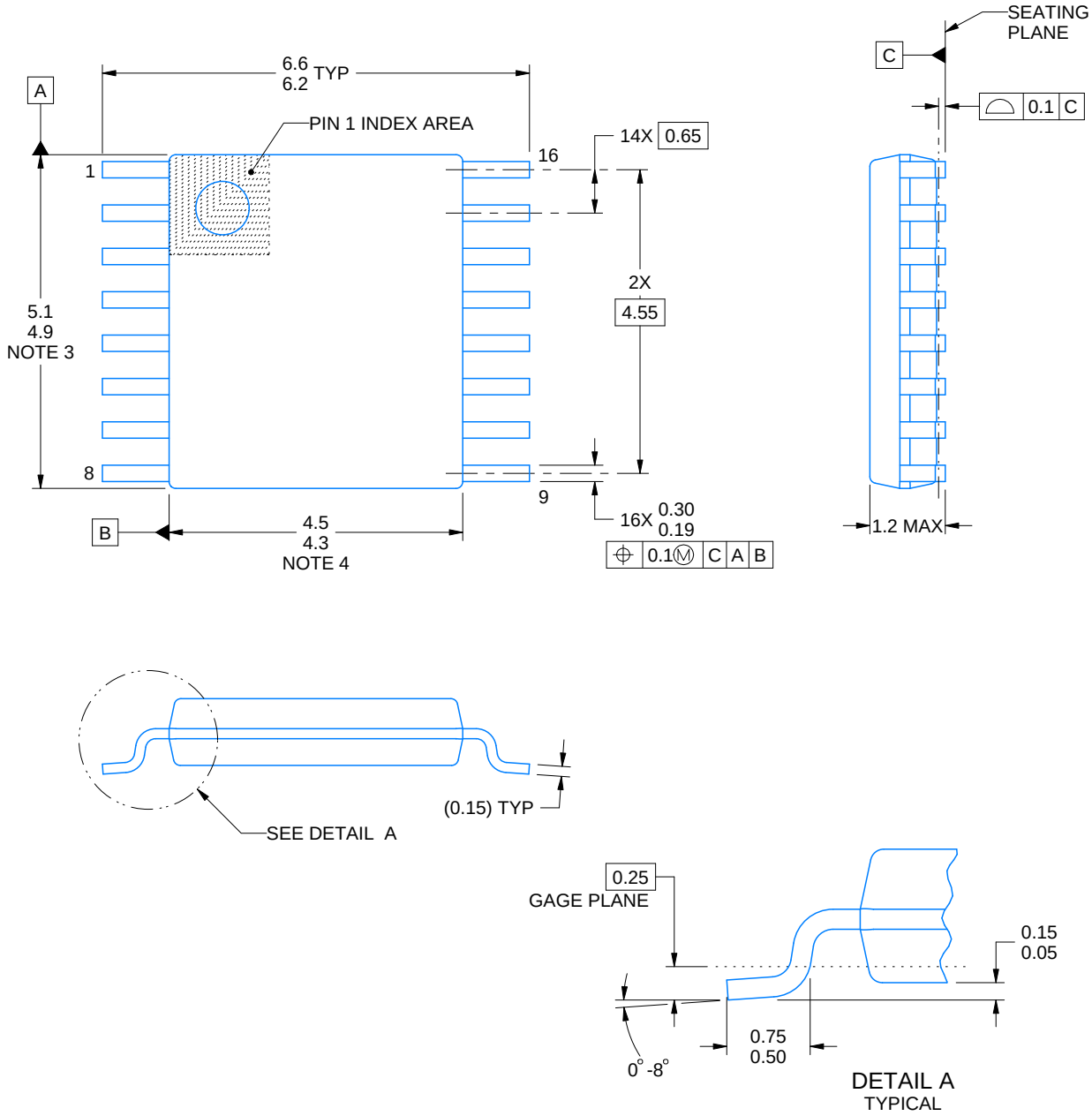
PW0016A



PACKAGE OUTLINE

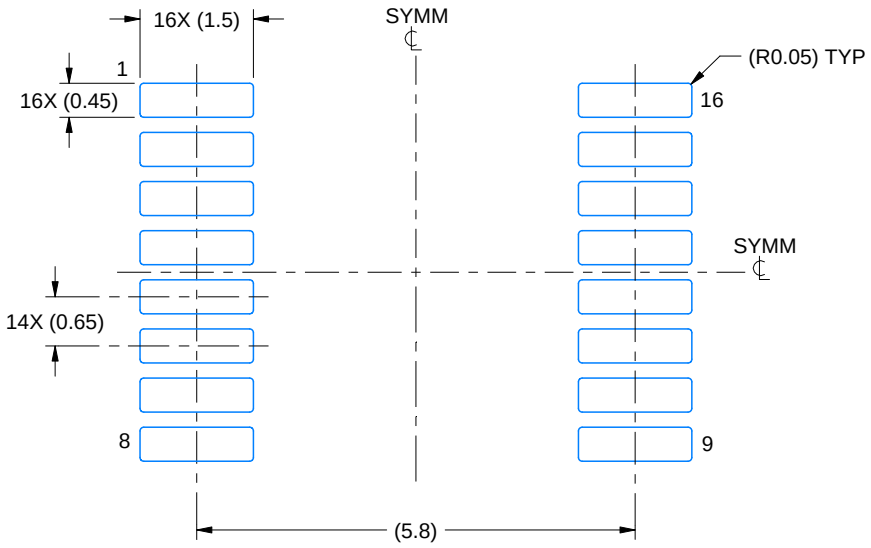
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

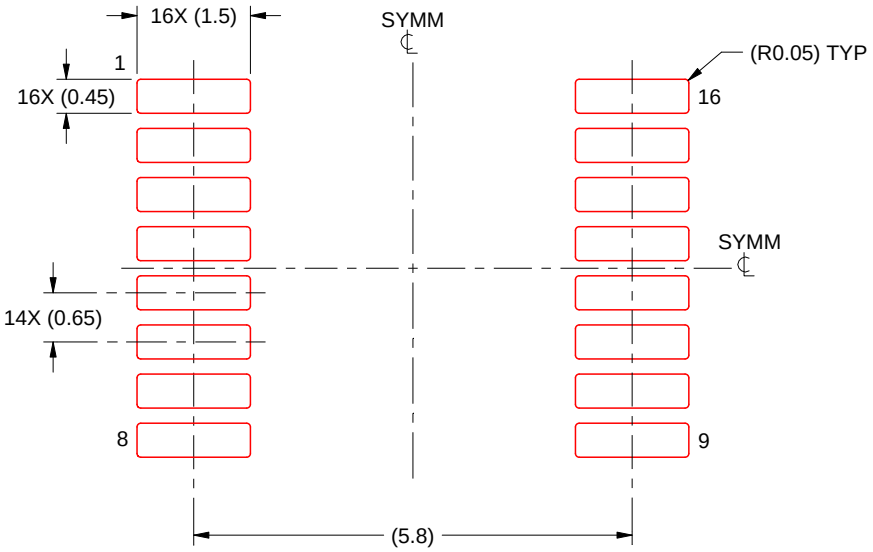
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

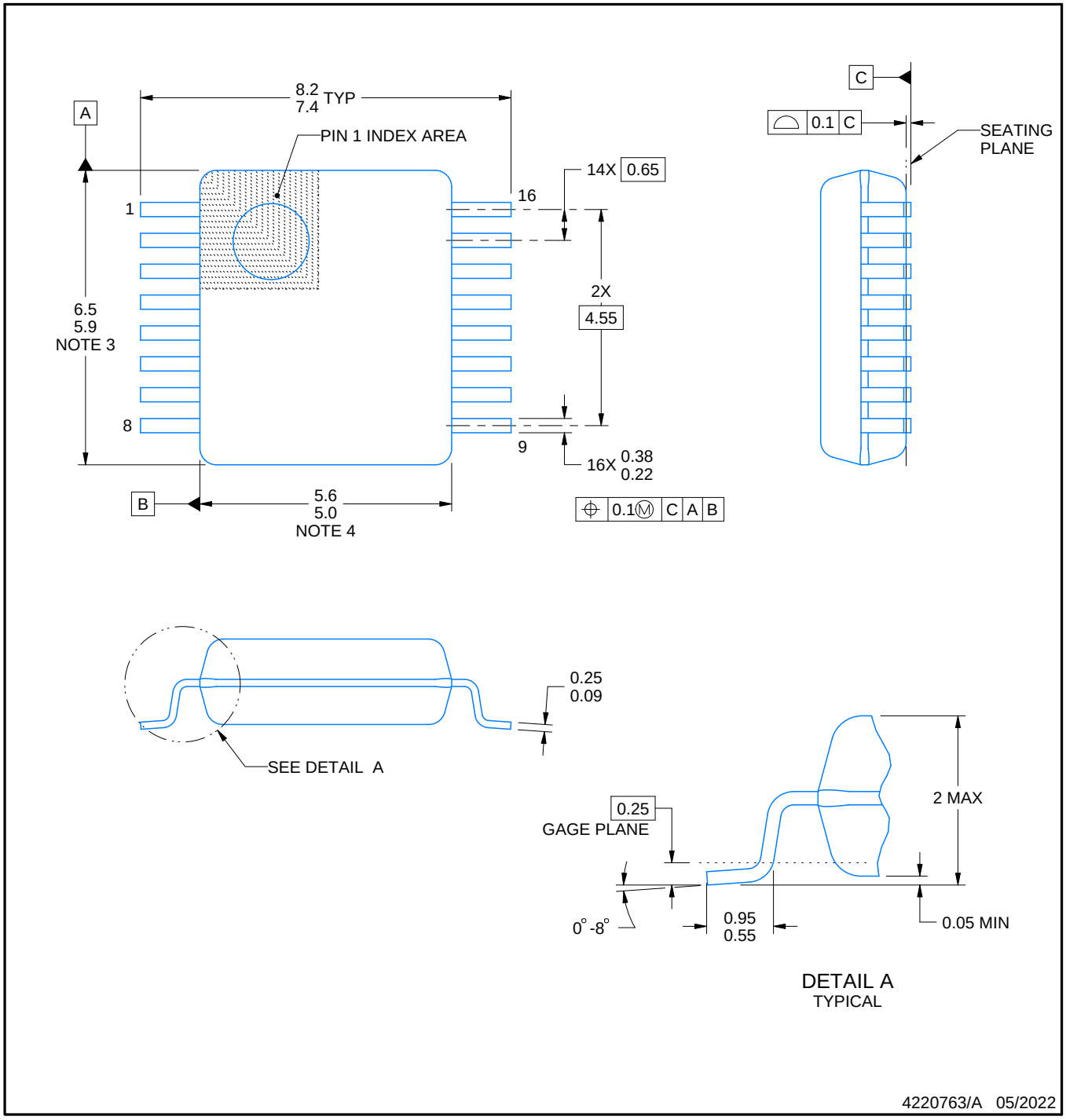


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

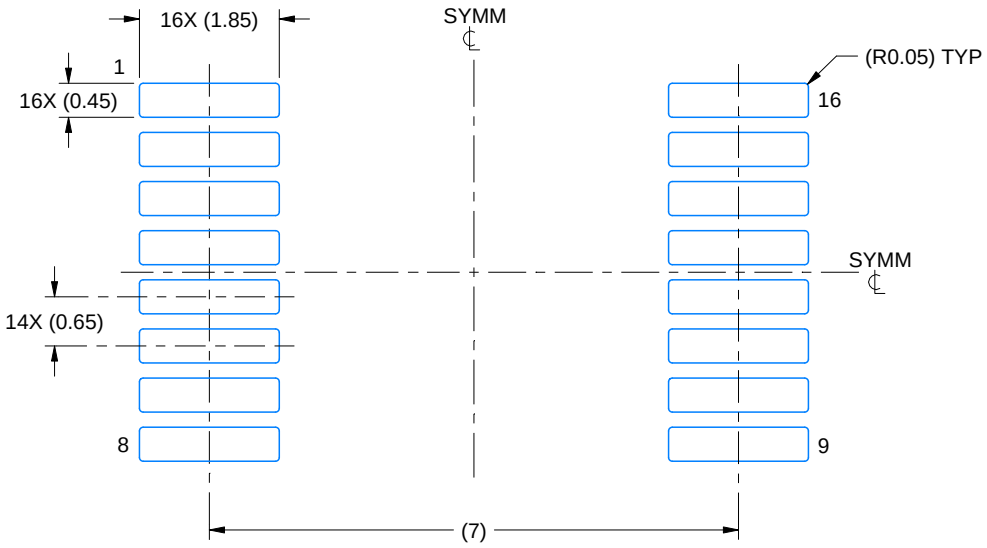
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

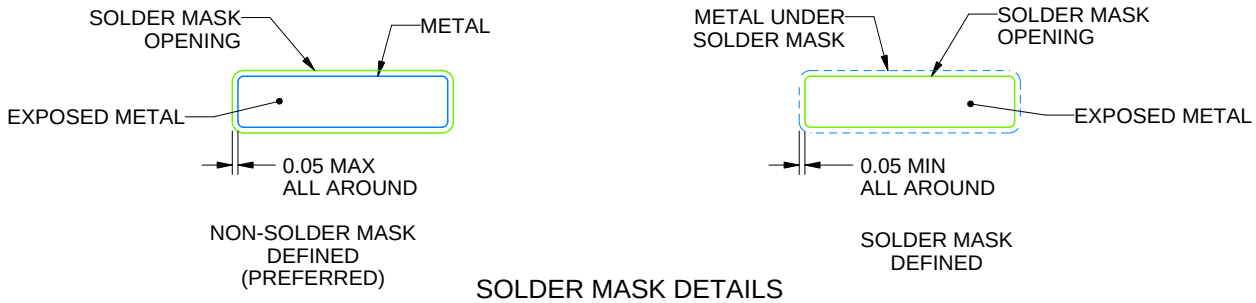


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

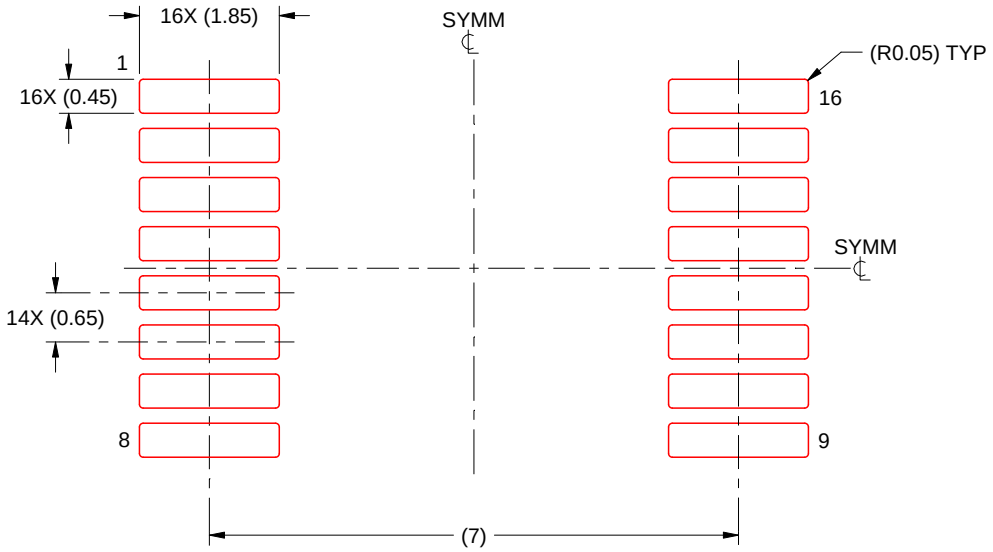


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

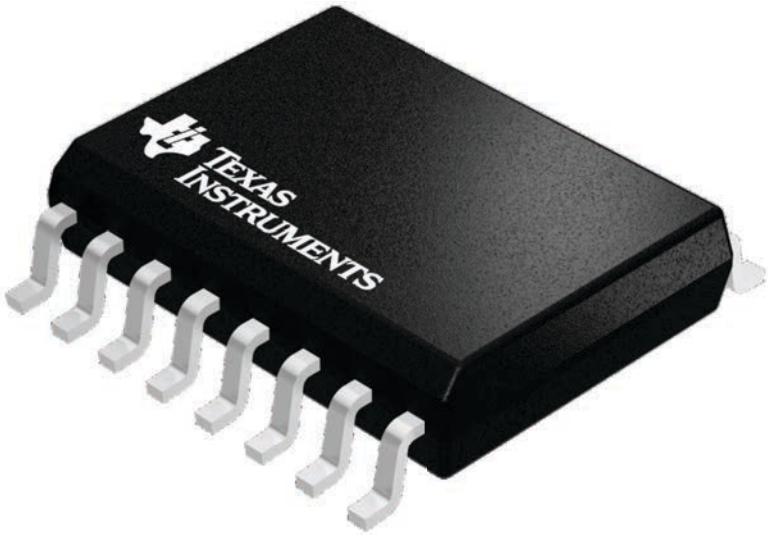
DW 16

SOIC - 2.65 mm max height

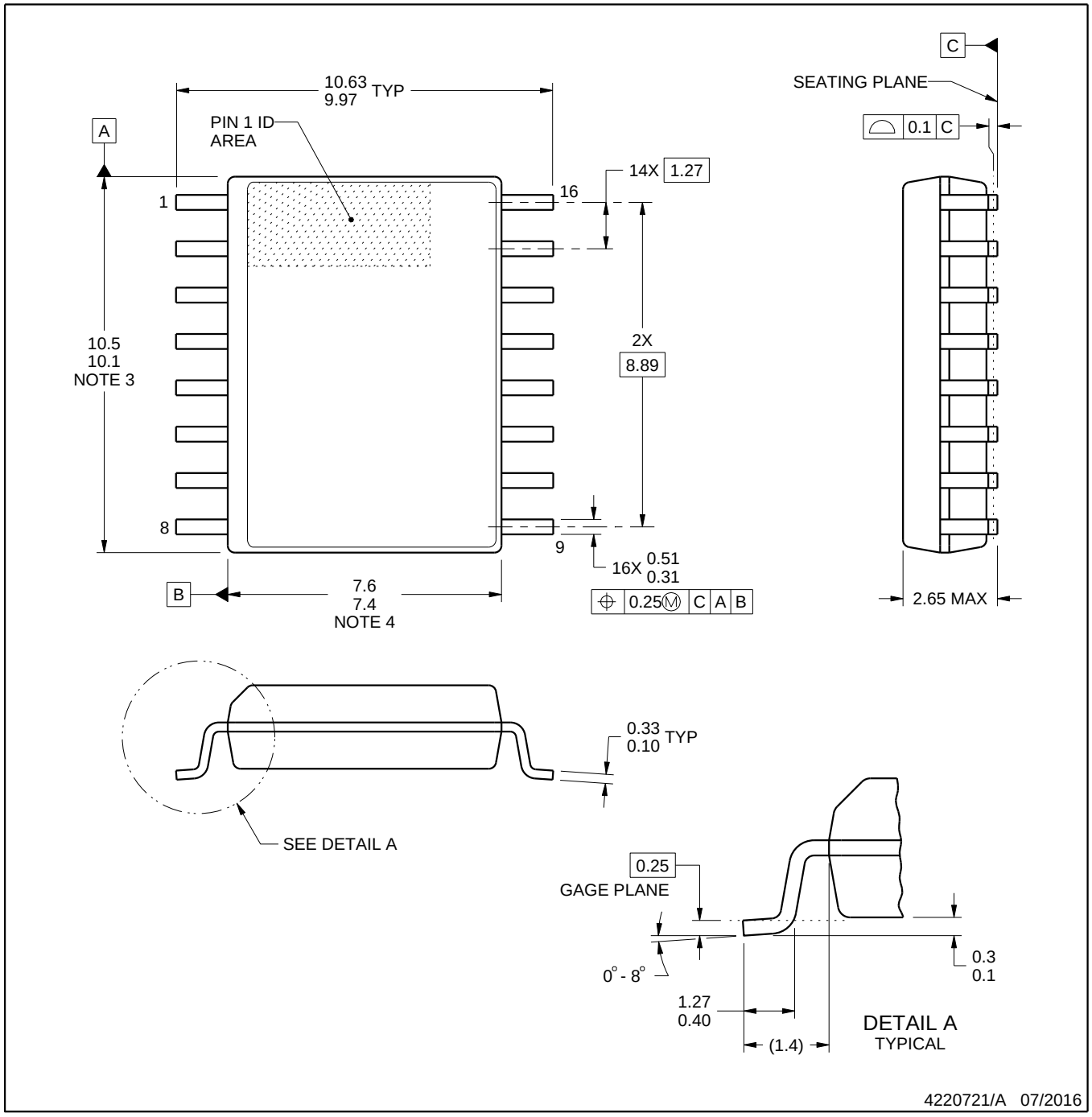
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

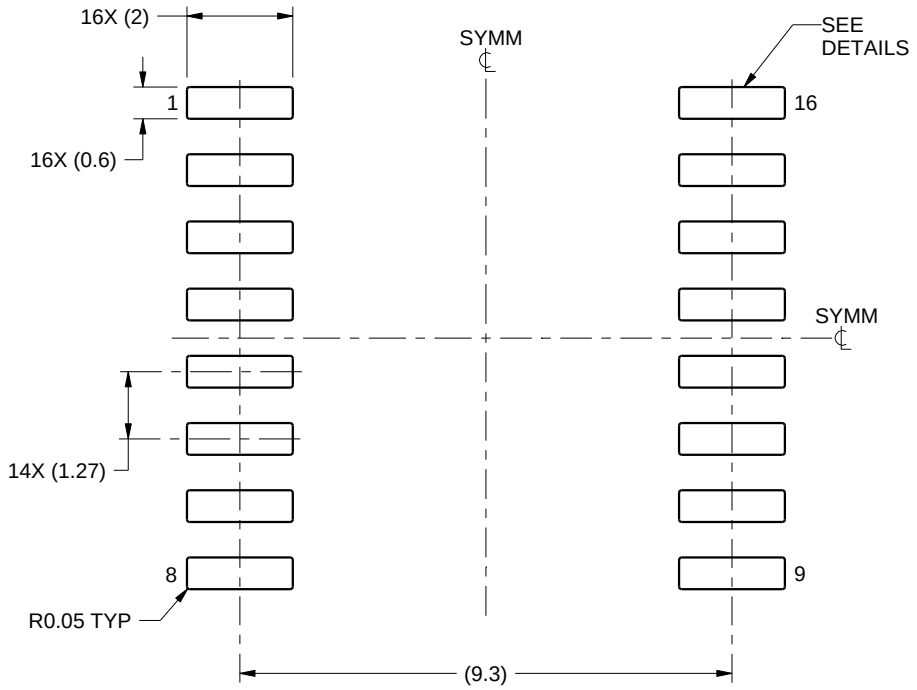


4224780/A

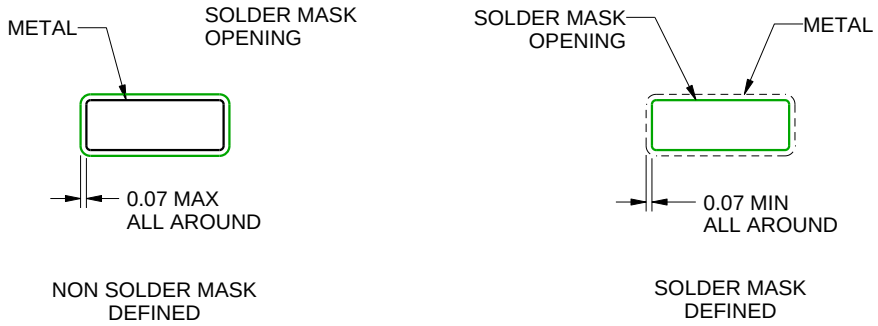


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

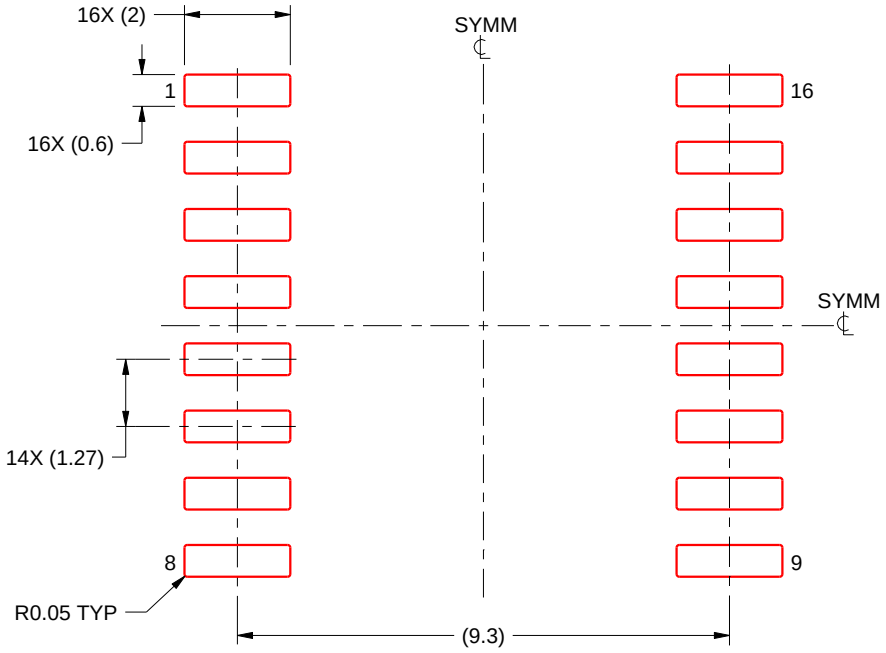


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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