DS90UB964-Q1 12-Bit, 100MHz FPD-Link III Quad Deserializer Hub

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 2: –40°C to +105°C ambient operating temperature range
  - Device HBM ESD classification level ±4kV
  - Device CDM ESD classification level C6
- Aggregates data from up to 4 sensors over FPD-Link III interface
- Supports 1-megapixel sensors with HD 720p/800p/960p resolution at 30Hz or 60Hz frame rate
- Multi-camera synchronization
- MIPI D-PHY version 1.2 / CSI-2 version 1.3 compliant
  - 2 × MIPI CSI-2 output ports
  - Supports 1, 2, 3, 4 data lanes per CSI-2 port
  - CSI-2 data rate scalable for 400Mbps / 800Mbps / 1.5Gbps / 1.6Gbps per data lane
  - Programmable data types
  - Four virtual channels
  - ECC and CRC generation
- Supports single-ended coaxial including Power-over-Coax (PoC) or Shielded Twisted-Pair (STP) cable
- Adaptive receive equalization
- I2C with fast-mode plus up to 1Mbps
- Flexible GPIOs for sensor synchronization and diagnostics
- Compatible with DS90UB933-Q1/DS90UB913A-Q1 serializers
- CRC protection on the internal data path
- ISO 10605 and IEC 61000-4-2 ESD compliant

2 Applications

- Automotive ADAS
  - Surround View Systems (SVS)
  - Camera Monitoring Systems (CMS)
  - Satellite RADAR, Time-of-Flight (ToF), LIDAR Sensors Modules, and Sensor Fusion
- Security and surveillance

3 Description

The DS90UB964-Q1 is a versatile sensor hub capable of connecting serialized sensor data received from four independent video data streams through an FPD-Link III interface. When coupled with DS90UB913A-Q1/933-Q1 serializers, the DS90UB964-Q1 receives data from 1-Megapixel image sensors supporting 720p/800p/960p resolution at 30Hz or 60Hz frame rates. Data is received and aggregated into a MIPI CSI-2 compliant output for interconnect to a downstream processor. A second MIPI CSI-2 output port is available to provide additional bandwidth, or offers a second replicated output for data-logging and parallel processing.

The DS90UB964-Q1 includes four FPD-Link III deserializers, each enabling a connection through cost-effective 50Ω single-ended coaxial or 100Ω differential STP cables. The receive equalizers automatically adapt to compensate for cable loss characteristics, including degradation over time.

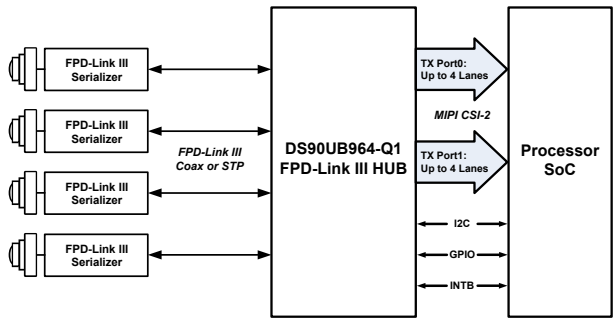
Each of the FPD-Link III interfaces also includes a separate low latency bidirectional control channel that continuously conveys I2C, GPIOs, and other control information. General-purpose I/O signals such as those required for camera synchronization and diagnostics features also make use of this bidirectional control channel.

The DS90UB964-Q1 is AEC-Q100 qualified for automotive applications and is offered in a cost-effective and space-saving 64 pin VQFN package.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
DS90UB964-Q1	VQFN (64)	9.00mm × 9.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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Pin Configuration and Functions

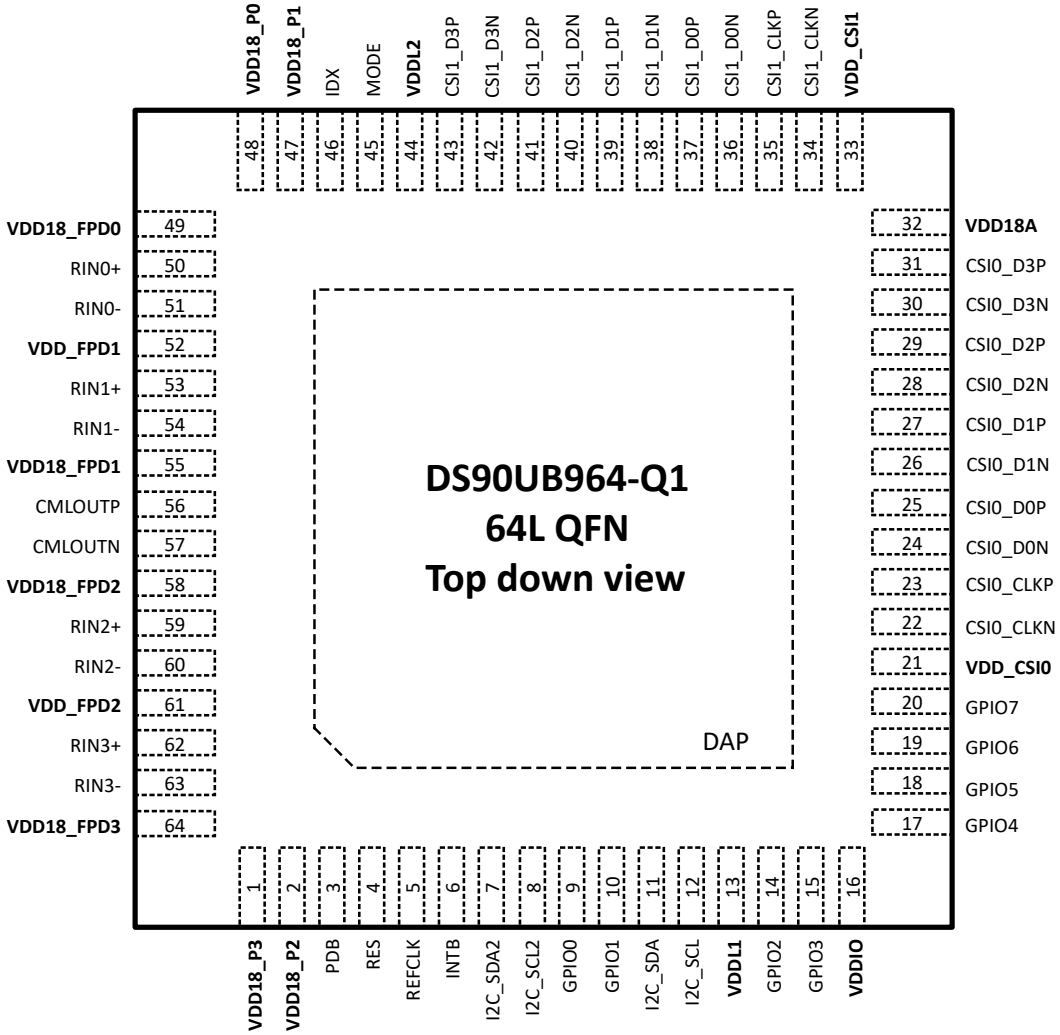

Figure 4-1. RGC Package
64 Pin VQFN
(Top View)

Table 4-1. Pin Functions

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
MIPI CSI-2 TX INTERFACE			
CSI0_CLKN	22	O	CSI-2 TX Port 0 differential clock output pins. Leave unused pins as No Connect.
CSI0_CLKP	23		
CSI0_D0N	24		CSI-2 TX Port 0 differential data output pins. Use CSI_PORT_SEL, CSI_CTL, and CSI_CTL2 registers for the CSI-2 TX control. Leave unused pins as No Connect.
CSI0_D0P	25		
CSI0_D1N	26		
CSI0_D1P	27		
CSI0_D2N	28		
CSI0_D2P	29		
CSI0_D3N	30		
CSI0_D3P	31		
CSI1_CLKN	34	O	CSI-2 TX Port 1 differential clock output pins. Leave unused pins as No Connect.
CSI1_CLKP	35		
CSI1_D0N	36		CSI-2 TX Port 1 differential data output pins. Use CSI_PORT_SEL, CSI_CTL, and CSI_CTL2 registers for the CSI-2 TX control. Leave unused pins as No Connect.
CSI1_D0P	37		
CSI1_D1N	38		
CSI1_D1P	39		
CSI1_D2N	40		
CSI1_D2P	41		
CSI1_D3N	42		
CSI1_D3P	43		
FPD-LINK III RX INTERFACE			
RIN0+	50	I/O	FPD-Link III RX Port 0 pins. The port receives FPD-Link III high-speed forward channel video and control data and transmits back channel control data. The port can interface with a compatible FPD-Link III serializer TX through an STP or coaxial cable (see Figure 6-3 and Figure 6-4). The port must be AC-coupled per Table 6-3. If port is unused, set RX_PORT_CTL register bit 0 to 0 to disable RX Port 0 and leave the pins as No Connect.
RIN0-	51		
RIN1+	53		FPD-Link III RX Port 1 pins. The port receives FPD-Link III high-speed forward channel video and control data and transmits back channel control data. The port can interface with a compatible FPD-Link III serializer TX through an STP or coaxial cable (see Figure 6-3 and Figure 6-4). The port must be AC-coupled per Table 6-3. If port is unused, set RX_PORT_CTL register bit 1 to 0 to disable RX Port 1 and leave the pins as No Connect.
RIN1-	54		
RIN2+	59		FPD-Link III RX Port 2 pins. The port receives FPD-Link III high-speed forward channel video and control data and transmits back channel control data. The port can interface with a compatible FPD-Link III serializer TX through an STP or coaxial cable (see Figure 6-3 and Figure 6-4). The port must be AC-coupled per Table 6-3. If port is unused, set RX_PORT_CTL register bit 2 to 0 to disable RX Port 2 and leave the pins as No Connect.
RIN2-	60		
RIN3+	62		FPD-Link III RX Port 3 pins. The port receives FPD-Link III high-speed forward channel video and control data and transmits back channel control data. The port can interface with a compatible FPD-Link III serializer TX through an STP or coaxial cable (see Figure 6-3 and Figure 6-4). The port must be AC-coupled per Table 6-3. If port is unused, set RX_PORT_CTL register bit 3 to 0 to disable RX Port 3 and leave the pins as No Connect.
RIN3-	63		

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Table 4-1. Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
GENERAL-PURPOSE I/O			
GPIO0	9	I/O, PD	General-Purpose Input/Output pins. The pins can be used to control and respond to various commands. The pins can be configured to be input signals for the corresponding GPIOs on the serializer, or the pins can be configured to be outputs to follow local register settings. At power up, the GPIO pins are disabled and by default include a pulldown resistor (25kΩ typical). See *Section 5.4.9*. for programmability. If unused, leave the pin as No Connect.
GPIO1	10		
GPIO2	14		
GPIO3	15		
GPIO4	17		
GPIO5	18		
GPIO6	19		
GPIO7	20		
SERIAL CONTROL BUS (I2C)			
I2C_SCL	12	I/O, OD	Primary I2C Clock Input / Output interface pin. See *Section 5.5.1*. Refer to *"I2C Bus Pullup Resistor Calculation"* (SLVA689) to determine the pull-up resistor value to VDDIO.
I2C_SDA	11	I/O, OD	Primary I2C Data Input / Output interface pin. See *Section 5.5.1*. Refer to *"I2C Bus Pullup Resistor Calculation"* (SLVA689) to determine the pull-up resistor value to VDDIO.
I2C_SCL2	8	I/O, OD	Secondary I2C Clock Input / Output interface pin. See *Section 5.5.2*. Refer to *"I2C Bus Pullup Resistor Calculation"* (SLVA689) to determine the pull-up resistor value to VDDIO.
I2C_SDA2	7	I/O, OD	Secondary I2C Data Input / Output interface pin. See *Section 5.5.2*. Refer to *"I2C Bus Pullup Resistor Calculation"* (SLVA689) to determine the pull-up resistor value to VDDIO.
CONFIGURATION AND CONTROL			
IDX	46	S	I2C Serial Control Bus Device ID Address Select configuration pin. Connect to an external pullup to VDD18 and a pulldown to GND to create a voltage divider. See Table 5-13.
MODE	45	S	Mode Select configuration pin. Connect to external pullup to VDD18 and a pulldown to GND to create a voltage divider. See Table 5-2.
PDB	3	I, PD	Inverted Power-Down input pin. Typically connected to a processor GPIO with a pulldown. When PDB input is brought HIGH, the device is enabled and internal registers and state machines are reset to default values. Asserting PDB signal low powers down the device and consumes minimum power. The default function of this pin is PDB = LOW; POWER DOWN with an internal 50kΩ internal pulldown enabled. PDB must remain low until after power supplies are applied and reach minimum required levels. See *Section 6.4.1*. **INPUT IS 3.3V TOLERANT** PDB = 1.8V or 3.3V, device is enabled (normal operation) PDB = 0V, device is powered down.
POWER AND GROUND			
VDDIO	16	P	1.8V (±5%) OR 3.3V (±10%) LVCMOS I/O Power Recommend 1µF, 0.1F, and 0.1µF or 0.01µF capacitors to GND (see Section 6.2)
VDD_CSI0 VDD_CSI1	21 33	P	1.1V (±5%) Power Supplies Recommend 0.1µF or 0.01µF capacitors to GND at each VDD pin. Additional 1µF decoupling is recommended for the pin group (see Section 6.2)
VDDL1 VDDL2	13 44	P	1.1V (±5%) Power Supplies Recommend 0.1µF or 0.01µF capacitors to GND at each VDD pin. Additional 0.1µF and 1µF decoupling is recommended for the pin group (see Section 6.2)
VDD_FPD1 VDD_FPD2	52 61	P	1.1V (±5%) Power Supplies Recommend 0.1µF or 0.01µF capacitors to GND at each VDD pin. Additional 0.1µF and 1µF decoupling is recommended for the pin group (see Section 6.2)

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Table 4-1. Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
VDD18_P2 VDD18_P3 VDD18_P1 VDD18_P0	2 1 47 48	P	1.8V (±5%) Power Supplies Recommend 0.1µF or 0.01µF capacitors to GND at each VDD pin. Additional 0.1µF and 1µF decoupling is recommended for the pin group (see Section 6.2)
VDD18A	32	P	1.8V (±5%) Power Supplies Recommend 0.1µF or 0.01µF capacitors to GND at each VDD pin. Additional 0.1µF, and 1µF decoupling is recommended for the pin group (see Section 6.2)
VDD18_FPD0 VDD18_FPD1 VDD18_FPD2 VDD18_FPD3	49 55 58 64	P	1.8V (±5%) Power Supplies Recommend 0.1µF or 0.01µF capacitors to GND at each VDD pin. Additional 0.1µF, 1µF, and 10uF decoupling is recommended for the pin group (see Section 6.2)
GND	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the VQFN package. Connect to the ground plane (GND).
OTHERS			
INTB	6	O, OD	Interrupt Output pin. INTB is an active-low open drain and controlled by the status registers. See *Section 5.5.9*. Recommend a 4.7kΩ Pullup to 1.8V or 3.3V. If unused, leave the pin as No Connect.
REFCLK	5	I	Reference clock oscillator input. Typically connected to a 23MHz to 25MHz LVCMOS-level oscillator (100 ppm). For 400Mbps, 800Mbps or 1.6Gbps CSI-2 data rates, use 25MHz frequency. For <1.5Gbps operation use 23MHz (1.47Gbps) For the oscillator requirements, see *Section 5.4.3*. For other common CSI-2 data rates, see *Section 5.4.18*.
RES	4	-	This pin must be tied to GND for normal operation.
CMLOUTP	56	O	Channel Monitor Loop-through Driver differential output. Route to a test point or a pad with 100Ω termination resistor between pins for channel monitoring (recommended). See *Section 5.4.7*.
CMLOUTN	57		

The definitions below define the functionality of the I/O cells for each pin. TYPE:

- I = Input
- O = Output
- I/O = Input/Output
- S = Strap Input
- PD = Internal Pulldown
- OD = Open Drain
- P = Power Supply
- G = Ground

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4 Specifications

4.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage	VDD11	–0.3	1.8	V
	VDD18	–0.3	2.5	V
	VDDIO	–0.3	4	V
LVCMOS IO voltage		–0.3	VDDIO + 0.3	V
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office or Distributors for availability and specifications.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 ESD Ratings – JEDEC

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	RIN[3:0]+, RIN[3:0]-	±8000	V
			Other pins	±4000	
		Charged device model (CDM), per AEC Q100-011		±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4.3 ESD Ratings – IEC and ISO

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ESD Rating (IEC 61000-4-2) R_D= 330 Ω, C_S = 150 pF	Contact Discharge (RIN[3:0]+, RIN[3:0]-)	±8000	V
			Air Discharge (RIN[3:0]+, RIN[3:0]-)	±18000	
		ESD Rating (ISO 10605) R_D= 330 Ω, C_S = 150 pF and 330 pF R_D= 2 kΩ, C_S = 150 pF and 330 pF	Contact Discharge (RIN[3:0]+, RIN[3:0]-)	±8000	V
			Air Discharge (RIN[3:0]+, RIN[3:0]-)	±18000	

4.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply voltage	VDD11		1.045	1.1	1.155	V
	VDD18		1.71	1.8	1.89	V
LVCMOS supply voltage	VDDIO	1.8V Option	1.71	1.8	1.89	V
		3.3V Option	3.0	3.3	3.6	V
Operating free-air temperature, T_A			–40	25	105	°C
MIPI data rate (per CSI-2 lane)			400	800	1600	Mbps
MIPI CSI-2 HS clock frequency			200	400	800	MHz
Local I^2C frequency, f_{I2C}					1	MHz

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4.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply Noise[1]	VDD11				25	mV_{P-P}
	VDD18				50	mV_{P-P}
	VDDIO	1.8V Option			50	mV_{P-P}
		3.3V Option			100	mV_{P-P}

(1) Supply noise testing was performed with minimum capacitors (as shown in the Typical Application Diagram). A sinusoidal signal is AC coupled from DC to 10 MHz to the VDD11, VDD18, and VDDIO (1.8V / 3.3V) supply pins with amplitude of 25 mVp-p, 50 mVp-p, and 50 mVp-p / 100 mVp-p respectively measured at the device VDD pins.

4.5 Thermal Information

THERMAL METRIC[1]		DS90UB964-Q1 RGC (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

4.6 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
1.8 V LVCMOS I/O (VDDIO = 1.8 V ± 5%)								
V_{IH}	High Level Input Voltage			GPIO[7:0], PDB, REFCLK	0.65 × VDDIO		VDDIO	V
V_{IL}	Low Level Input Voltage				GND		0.35 × VDDIO	V
I_{IH}	Input High Current	VIN = 0 V or VDDIO	Internal Pulldown Enabled	GPIO[7:0][1], PDB	–20		150	µA
I_{IH}	Input High Current	VIN = 0 V or VDDIO	Internal Pulldown Disabled	GPIO[7:0][1]	–20		20	µA
I_{IL}	Input Low Current	VIN = 0 V or VDDIO		GPIO[7:0][1], PDB	–20		20	µA
V_{OH}	High Level Output Voltage	I_{OH} = –2 mA		GPIO[7:0]	VDDIO – 0.45		VDDIO	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		GPIO[7:0], INTB	GND		0.45	V
I_{OS}	Output Short Circuit Current	VOUT = 0 V		GPIO[7:0]		–35		mA
I_{OZ}	TRI-STATE Output Current	VOUT = 0 V or VDDIO, PDB = LOW		GPIO[7:0]	–20		20	µA
3.3 V LVCMOS I/O (VDDIO = 3.3 V ± 10%)								
V_{IH}	High Level Input Voltage			GPIO[7:0]	2		VDDIO	V
V_{IH}				REFCLK, PDB	1.17		VDDIO	
V_{IL}	Low Level Input Voltage			GPIO[7:0]	GND		0.8	V
V_{IL}				REFCLK, PDB	GND		0.63	
I_{IH}	Input High Current	VIN = 0 V or VDDIO	Internal Pulldown Enabled	GPIO[7:0][1], PDB	–20		200	µA
I_{IH}	Input High current	VIN = 0 V or VDDIO	Internal Pulldown Disabled	GPIO[7:0][1]	–20		20	µA

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4.6 DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
I_{IL}	Input Low current	VIN = 0 V or VDDIO		GPIO[7:0][(1)], PDB	–20		20	µA
V_{OH}	High Level Output Voltage	I_{OH} = –4 mA		GPIO[7:0]	2.4		VDDIO	V
V_{OL}	Low Level Output Voltage	I_{OL} = 4 mA		GPIO[7:0], INTB	GND		0.4	V
I_{OS}	Output Short Circuit Current	VOUT = 0 V		GPIO[7:0]		–50		mA
I_{OZ}	TRI-STATE Output Current	VOUT = 0 V or VDDIO, PDB = LOW		GPIO[7:0]	–20		20	µA
I^2C SERIAL CONTROL BUS (VDDIO = 1.8 V ± 5% OR 3.3 V ± 10%)								
V_{IH}	Input High Level			I2C_SDA, I2C_SCL I2C_SDA2, I2C_SCL2	0.7 × VDDIO		VDDIO	V
V_{IL}	Input Low Level				GND		0.3 × VDDIO	V
V_{HY}	Input Hysteresis					>50		mV
V_{OL}	Output Low Level	I_{OL} = 4 mA	Standard-mode Fast-mode		0		0.4	V
		I_{OL} = 15 mA	Fast-mode Plus		0		0.4	V
I_{IN}	Input Current	VIN = 0 V or VDDIO			–10		10	µA
FPD-LINK III RECEIVER INPUT								
V_{IN}	Single-ended Input Voltage	(Figure 5-2)		RIN0±, RIN1±, RIN2±, RIN3±	60			mV
V_{ID}	Differential Input Voltage	(Figure 5-2)		RIN0±, RIN1±, RIN2±, RIN3±	115			mV
V_{CM}	Common Mode Voltage					1.0		V
I_{IZ}	Power-down input current	PDB = LOW			–10		–10	µA
R_T	Internal Termination Resistance	Single-ended RIN+ or RIN-			40	50	60	Ω
		Differential across RIN+ and RIN-			80	100	120	Ω
FPD-LINK III BI-DIRECTIONAL CONTROL CHANNEL								
V_{OUT-BC}	Back Channel Single-Ended Output Voltage	R_L = 50 Ω Coaxial configuration Forward channel disabled		RIN0+, RIN1+ RIN2+, RIN3+	+190	+220	+260	mV
				RIN0-, RIN1- RIN2-, RIN3-	–190	–220	–260	
V_{OD-BC}	Back Channel Differential Output Voltage (RIN+) - (RIN-)	R_L = 100 Ω STP configuration Forward channel disabled		RIN0±, RIN1±, RIN2±, RIN3±	380	440	520	mV
HSTX DRIVER								
V_{CMTX}	HS transmit static common-mode voltage			CSI0_D[3:0]P/N, CSI0_CLKP/N, CSI1_D[3:0]P/N, CSI1_CLKP/N	150	200	250	mV
$\lvert\Delta V_{CMTX(1,0)}\rvert$	V_{CMTX} mismatch when output is 1 or 0						5	mV_{P-P}
$\lvert V_{OD}\rvert$	HS transmit differential voltage				140	200	270	mV
$\lvert\Delta V_{OD}\rvert$	V_{OD} mismatch when output is 1 or 0						14	mV
V_{OHHS}	HS output high voltage						360	mV
Z_{OS}	Single-ended output impedance				40	50	62.5	Ω
ΔZ_{OS}	Mismatch in single-ended output impedance						10	%
LPTX DRIVER								
V_{OH}	High Level Output Voltage	I_{OH} = –4 mA		CSI0_D[3:0]P/N, CSI0_CLKP/N, CSI1_D[3:0]P/N, CSI1_CLKP/N	1.1	1.2	1.3	V
V_{OL}	Low Level Output Voltage	I_{OL} = 4 mA			–50		50	mV
Z_{OLP}	Output impedance				110			Ω

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4.6 DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
POWER CONSUMPTION							
P_T	Total Power Consumption in Operation Mode	CSI-2 data rate = 1.6Gbps 4 × FPD-Link III RX inputs CSI-2 TX = 2 × (4 data lanes + 1 CLK lane) <Non-Replicate> Default registers				1100	mW
SUPPLY CURRENT							
I_{DDT1}	DPHY TX Supply Current (includes load current)	CSI-2 data rate = 800 Mbps 4 × FPD-Link III RX inputs CSI-2 TX = 1 data lanes + 1 CLK lane <Non-Replicate> Default registers	VDD11		90	275	mA
			VDD18		177	240	
			VDDIO		10	50	
		CSI-2 data rate = 1.6Gbps 4 × FPD-Link III RX inputs CSI-2 TX = 1 data lanes + 1 CLK lane <Non-Replicate> Default registers	VDD11		100	280	mA
			VDD18		177	240	
			VDDIO		10	50	
I_{DDT2}	DPHY TX Supply Current (includes load current)	CSI-2 data rate = 800 Mbps 4 × FPD-Link III RX inputs CSI-2 TX = 2 × (4 data lanes + 1 CLK lane) <Replicate Mode> Default registers	VDD11		105	285	mA
			VDD18		180	240	
			VDDIO		10	50	
		CSI-2 data rate = 1.6Gbps 4 × FPD-Link III RX inputs CSI-2 TX = 2 × (4 data lanes + 1 CLK lane) <Replicate Mode> Default registers	VDD11		120	380	mA
			VDD18		180	240	
			VDDIO		10	50	
I_{DDZ}	Standby Current	PDB = LOW	VDD11			100	mA
			VDD18			1	
			VDDIO			3	

(1) GPIO[7:0] Register 0xBE = 0xFF

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4.7 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
LVCMOS I/O							
t_{CLH}	LVCMOS Low-to-High Transition Time	VDDIO: 1.71 V to 1.89 V OR VDDIO: 3.0 V to 3.6 V C_L = 8 pF (lumped load) Default Registers (Figure 5-1)	GPIO[7:0]		2.5		ns
t_{CHL}	LVCMOS High-to-Low Transition Time		GPIO[7:0]		2.5		ns
FPD-LINK III RECEIVER INPUT							
t_{DDLT}	Deserializer Data Lock Time	With Adaptive Equalization (Figure 5-3)	RIN0±, RIN1±, RIN2±, RIN3±		15	22	ms
t_{IJIT}	Input Jitter	Jitter Frequency > FPD3_PCLK(1) / 15				0.4	UI

(1) FPD3_PCLK is equivalent to PCLK frequency based on the operating MODE:
10-bit mode: PCLK_Freq. /2
12-bit HF mode: PCLK_Freq. x 2/3
12-bit LF mode: PCLK_Freq.

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4.8 Recommended Timing for the Serial Control Bus

Over I^2C supply and temperature ranges unless otherwise specified.

PARAMETER		STANDARD-MODE		FAST-MODE		FAST-MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I^2C SERIAL CONTROL BUS (Figure 5-4)								
f_{SCL}	SCL Clock Frequency	>0	100	>0	400	>0	1000	kHz
t_{LOW}	SCL Low Period	4.7		1.3		0.5		µs
t_{HIGH}	SCL High Period	4.0		0.6		0.26		µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	4.0		0.6		0.26		µs
$t_{SU;STA}$	Set Up time for a start or a repeated start condition	4.7		0.6		0.26		µs
$t_{HD;DAT}$	Data Hold Time	0		0		0		µs
$t_{SU;DAT}$	Data Set Up Time	250		100		50		ns
$t_{SU;STO}$	Set Up Time for STOP Condition	4.0		0.6		0.26		µs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		µs
t_r	SCL & SDA Rise Time		1000		300		120	ns
t_f	SCL & SDA Fall Time		300		300		120	ns
C_b	Capacitive Load for Each Bus Line		400		400		550	pF
t_{SP}	Input Filter		-		50		50	ns

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4.9 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
HSTX DRIVER							
$HSTX_{DBR}$	Data rate		CSI0_D[3:0]P/N CSI1_D[3:0]P/N	400	800	1600	Mbps
fCLK	DDR Clock frequency		CSI0_CLKP/N CSI1_CLKP/N	200	400	800	MHz
$\Delta V_{CMTX(HF)}$	Common mode voltage variations HF	Above 450MHz	CSI0_D0P/N CSI0_D1P/N CSI0_D2P/N CSI0_D3P/N CSI0_CLKP/N CSI1_D0P/N CSI1_D1P/N CSI1_D2P/N CSI1_D3P/N CSI1_CLKP/N			15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common mode voltage variations LF	Between 50 and 450MHz				25	mV_{RMS}
t_{RHS} t_{FHS}	20% to 80% Rise and Fall HS	HS data rates ≤ 1Gbps (UI ≥ 1ns)				0.3	UI
		HS data rates > 1Gbps (UI ≤ 1ns) but less than 1.5Gbps (UI ≥ 0.667ns)				0.35	UI
		Applicable when supporting maximum HS data rates ≤ 1.5Gbps.		100			ps
		Applicable for all HS data rates when supporting > 1.5Gbps.				0.4	UI
		Applicable for all HS data rates when supporting > 1.5Gbps.		50			ps
SDD_{TX}	TX differential return loss	f_{LPMAX}	HS data rates <1.5Gbps			-18	dB
		f_H				-9	dB
		f_{MAX}				-3	dB
		f_{LPMAX}	HS data rates >1.5Gbps			-18	dB
		f_H				-4.5	dB
		f_{MAX}				-2.5	dB

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4.9 AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
LPTX DRIVER							
t_{RLP}	Rise Time LP(1)	15% to 85% rise time	CSI0_D0P/N CSI0_D1P/N CSI0_D2P/N CSI0_D3P/N CSI1_D0P/N CSI1_D1P/N CSI1_D2P/N CSI1_D3P/N CSI0_CLKP/N CSI1_CLKP/N			25	ns
t_{FLP}	Fall Time LP (1)	15% to 85% fall time				25	ns
t_{REOT}	Rise Time Post-EoT(1)	30%-85% rise time				35	ns
$t_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock(1)	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state		40			ns
		All other pulses		20			ns
$t_{LP-PER-TX}$	Period of the LP exclusive-OR clock			90			ns
DV/DtSR	Slew rate (1)	C_{LOAD} = 0 pF				500	mV/ns
		C_{LOAD} = 5 pF				300	mV/ns
		C_{LOAD} = 20 pF				250	mV/ns
		C_{LOAD} = 70 pF				150	mV/ns
		C_{LOAD} = 0 to 70 pF (Falling Edge Only)		30			mV/ns
		C_{LOAD} = 0 to 70 pF (Rising Edge Only)		30			mV/ns
		C_{LOAD} = 0 to 70 pF (Rising Edge Only) (2) (3)		30 - 0.075× (VO,IN ST - 700)			mV/ns
		C_{LOAD} = 0 to 70 pF (Rising Edge Only) (4) (5)		25 - 0.0625 × (VO,IN ST - 500)			mV/ns
C_{LOAD}	Load capacitance(1)			0		70	pF
CSI-2 TIMING SPECIFICATIONS — DATA-CLOCK TIMING (Figure 4-6, Figure 4-7)							
UI_{INST}	UI instantaneous	In 1, 2, 3, or 4 Lane Configuration HS Data rate = 400 Mbps	CSI0_D0P/N CSI0_D1P/N CSI0_D2P/N CSI0_D3P/N CSI1_D0P/N CSI1_D1P/N CSI1_D2P/N CSI1_D3P/N CSI0_CLKP/N CSI1_CLKP/N		2.5		ns
		In 1, 2, 3, or 4 Lane Configuration HS Data rate = 800 Mbps			1.25		ns
		In 1, 2, 3, or 4 Lane Configuration HS Data rate = 1.6Gbps			0.625		ns
ΔUI	UI variation	UI ≥ 1ns (Figure 4-5)		-10%		10%	UI
		UI < 1ns (Figure 4-5)		-5%		5%	UI
$t_{SKEW(TX)}$	Data to Clock Skew (measured at transmitter) Skew between clock and data from ideal center	HS Data rate ≤ 1Gbps (Figure 4-5)		-0.15		0.15	UI_{INST}
		1Gbps ≤ HS Data rate ≤ 1.5Gbps (Figure 4-5)		-0.2		0.2	UI_{INST}
$t_{SKEW(TX)}$ static	Static Data to Clock Skew	HS Data rate > 1.5Gbps		-0.2		0.2	UI_{INST}
$t_{SKEW(TX)}$ dynamic	Dynamic Data to Clock Skew	HS Data rate > 1.5Gbps		-0.15		0.15	UI_{INST}

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4.9 AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
CSI-2 TIMING SPECIFICATIONS - GLOBAL OPERATION (Figure 4-6, Figure 4-7)							
$t_{CLK-POST}$	HS exit		CSI0_D0P/N CSI0_D1P/N CSI0_D2P/N CSI0_D3P/N CSI1_D0P/N CSI1_D1P/N CSI1_D2P/N CSI1_D3P/N CSI0_CLKP/N CSI1_CLKP/N	60 + 52×UI_{INST}			ns
$t_{CLK-PRE}$	Time HS clock shall be driver prior to any associated Data Lane beginning the transition from LP to HS mode			8			UI_{INST}
$t_{CLK-PREPARE}$	Clock Lane HS Entry			38		95	ns
$t_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions			95		300	ns
$t_{CLK-TERM-EN}$	Time-out at Clock Lane Display Module to enable HS Termination			Time for Dn to reach VTERM-EN		38	ns
$t_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst			60			ns
$t_{CLK-PREPARE}$ + $t_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock			300			ns
$t_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination			Time for Dn to reach V-TERM-EN		35 + 4×UI_{INST}	ns
t_{EOT}	Transmitted time interval from the start of $t_{HS-TRAIL}$ to the start of the LP-11 state following a HS burst					105 + 12×UI_{INST}	ns
$t_{HS-EXIT}$	Time that the transmitter drives LP=11 following a HS burst			100			ns
$t_{HS-PREPARE}$	Data Lane HS Entry			40 + 4×UI_{INST}		85 + 6×UI_{INST}	ns
$t_{HS-PREPARE}$ + $t_{HS-ZERO}$	$t_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence			145 + 10×UI_{INST}			ns
$t_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $t_{HS-SETTLE}$			85 + 6×UI_{INST}		145 + 10×UI_{INST}	ns

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4.9 AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$t_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.			40		55 + 4×UI_{INST}	ns
$t_{HS-TRAIL}$	Data Lane HS Exit			60 + 4×UI_{INST}			ns
t_{LPX}	Transmitted length of LP state			50			ns
t_{WAKEUP}	Recovery Time from Ultra Low Power State (ULPS)			1			ms

(1) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2ns delay.
(2) When the output voltage is between 700 mV and 930 mV
(3) Applicable when the supported data rate ≤ 1.5Gbps
(4) When the output voltage is between 550 mV and 790 mV
(5) Applicable when the supported data rate > 1.5Gbps.

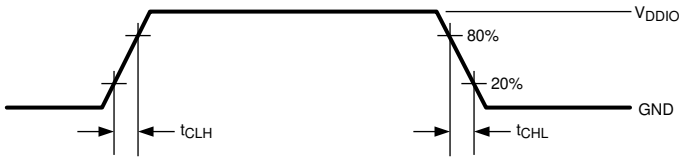

Figure 4-1. LVCMOS Transition Times

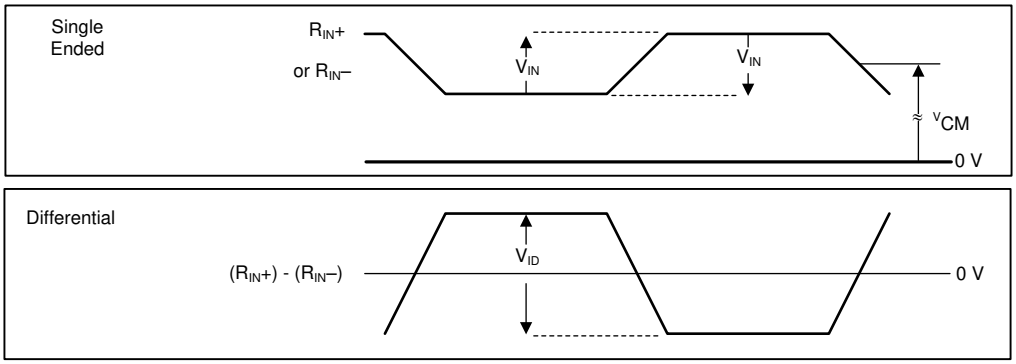

Figure 4-2. FPD-Link III Receiver V_{ID}, V_{IN}, V_{CM}

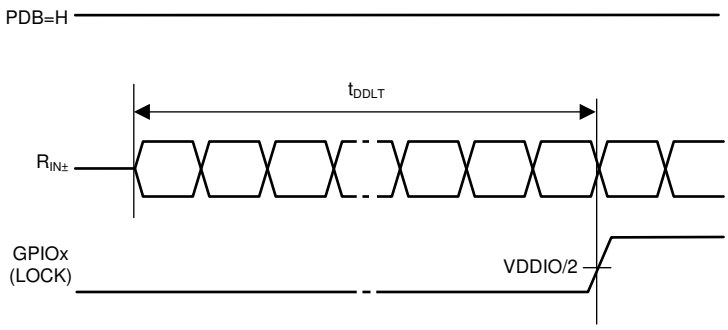

Figure 4-3. Deserializer Data Lock Time

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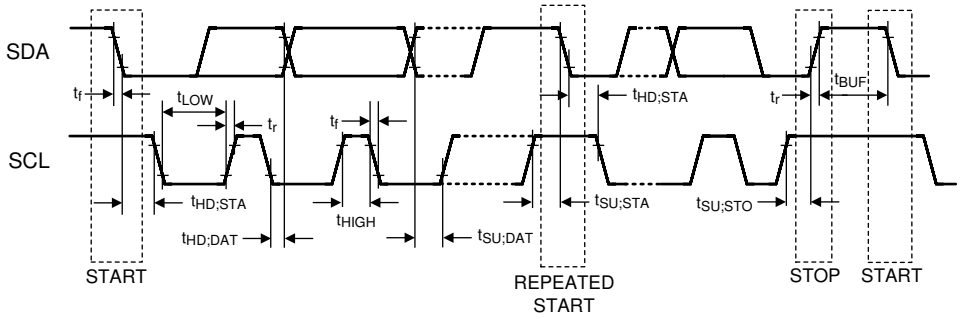

Figure 4-4. I2C Serial Control Bus Timing

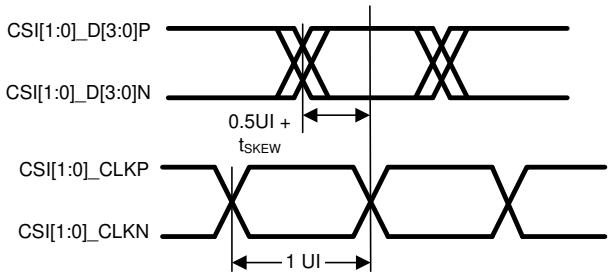

Figure 4-5. Clock and Data Timing in HS Transmission

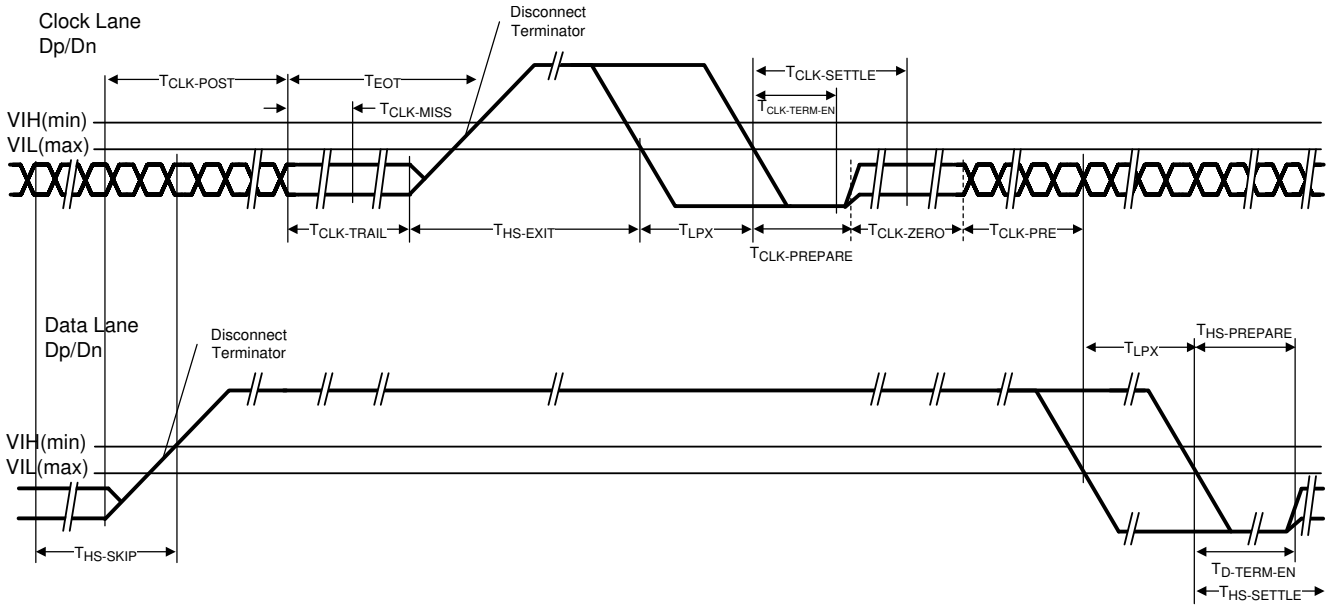

Figure 4-6. Switching the Clock Lane Between Clock Transmission and Low-Power Mode

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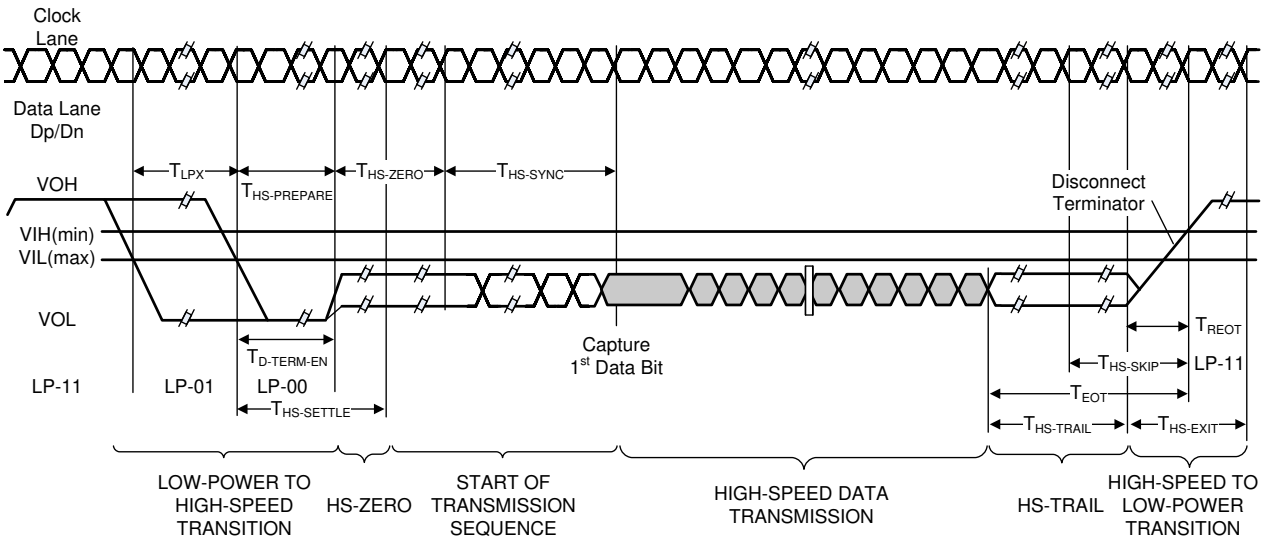

Figure 4-7. High-Speed Data Transmission Burst

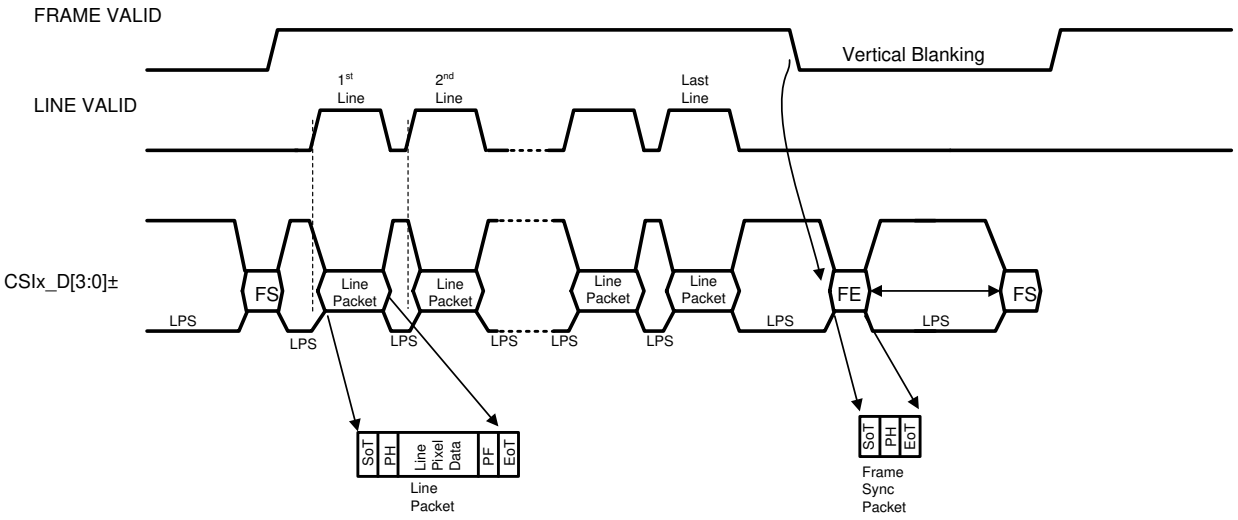

Figure 4-8. Long Line Packets and Short Frame Sync Packets

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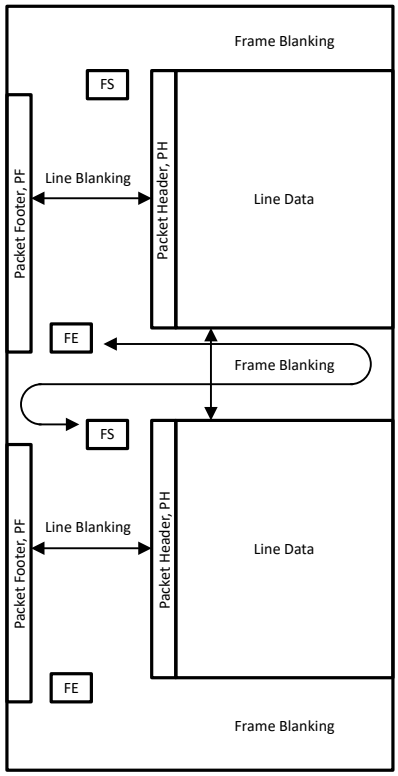
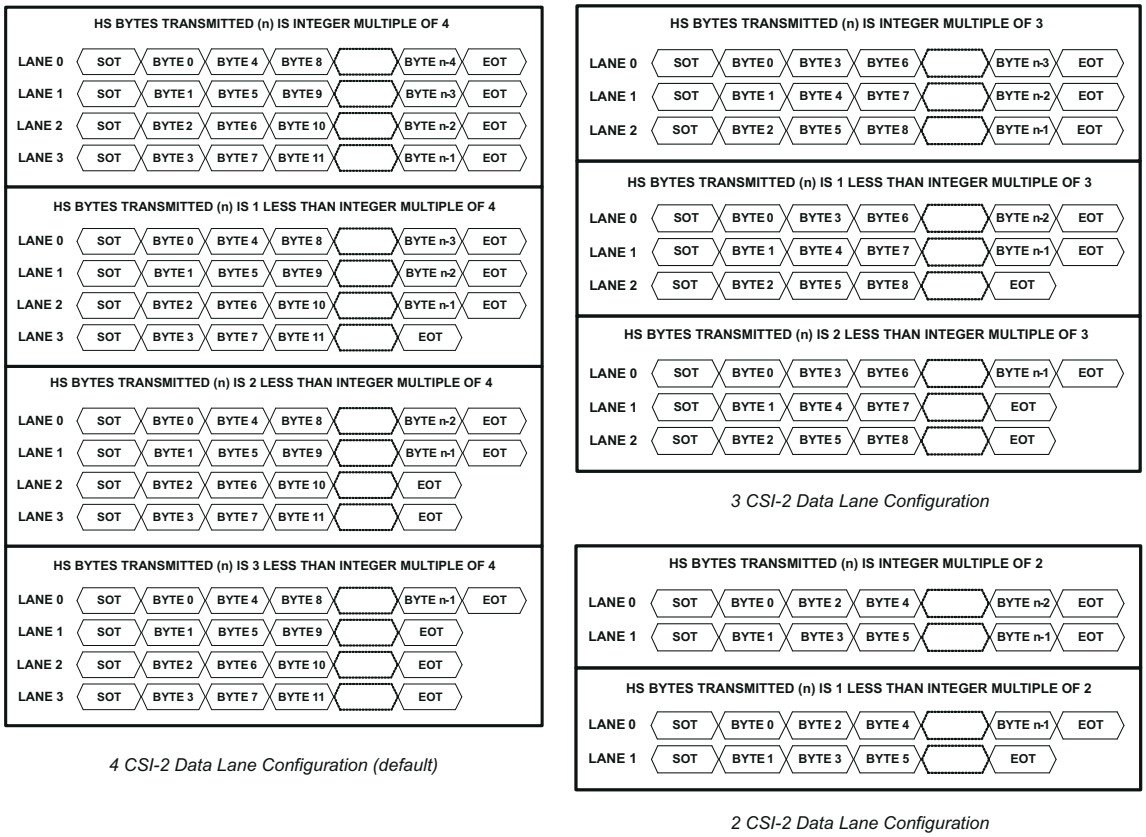


Figure 4-9. CSI-2 General Frame Format (Single Rx / VC)



4 CSI-2 Data Lane Configuration (default)

3 CSI-2 Data Lane Configuration

2 CSI-2 Data Lane Configuration

Figure 4-10. 4 MIPI Data Lane Configuration

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4.10 Typical Characteristics

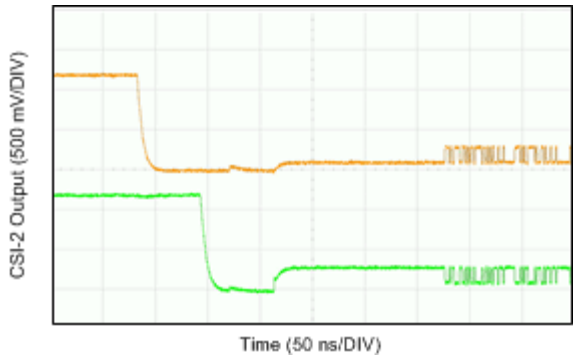

Figure 4-11. CSI-2 Start of Transmission (SoT)

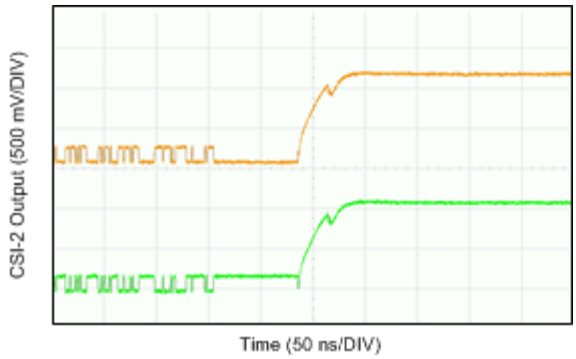

Figure 4-12. CSI-2 End of Transmission (EoT)

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5 Detailed Description

5.1 Overview

The DS90UB964-Q1 is a sensor hub that accepts four sensor inputs from a FPD-Link III interface. When coupled with serializers DS90UB933-Q1 or DS90UB913A-Q1, the device combines data streams from multiple sensor sources onto one or two MIPI CSI-2 ports with up to four data lanes on each port.

Table 5-1. Serializer Compatibility

SERIALIZER	DS90UB933-Q1	DS90UB913A-Q1
Compatibility	Yes	Yes

5.1.1 Functional Description

The DS90UB964-Q1 is a sensor hub that aggregates up to four inputs acquired from a FPD-Link III stream and transmitted over a MIPI sensor serial interface (CSI-2). When coupled with the DS90UB913A-Q1 or DS90UB933-Q1 FPD-Link III serializers, the DS90UB964-Q1 receives data streams from multiple imagers that can be multiplexed on the same CSI-2 links. The DS90UB964-Q1 supplies two MIPI CSI-2 ports, configured with four lanes per port with up to 1.6Gbps per lane. The second MIPI CSI-2 output port is available to provide either more bandwidth or supply a second replicated output. The DS90UB964-Q1 can support multiple data formats (programmable as RAW, YUV, RGB) and different sensor resolutions. The CSI-2 TX module accommodates both image data and non-image data (including synchronization or embedded data packets).

The DS90UB964-Q1 CSI-2 interface combines each of the sensor data streams into packets designated for each virtual channel. The output generated is composed of virtual channels to separate different streams to be interleaved. Each virtual channel is identified by a unique channel identification number in the packet header.

The DS90UB964-Q1 device recovers a high-speed, FPD-Link III forward channel signal and generates a bidirectional control channel control signal in the reverse channel direction. The DS90UB964-Q1 converts the FPD-Link III stream into a MIPI CSI-2 output interface designed to support automotive sensors, including 1MP/60fps image sensors.

The DS90UB964-Q1 device has four receive input ports to accept up to four sensor streams simultaneously. The control channel function of the serializer/deserializer pair supplies bidirectional communication between the image sensors and ECU. The integrated bidirectional control channel transfers data bidirectionally over the same differential pair used for video data interface. This interface has advantages over other chipsets because the interface eliminates the need for additional wires for programming and control. The bidirectional control channel bus is controlled through an I2C port. The bidirectional control channel supplies continuous low latency communication and is not dependent on video blanking intervals.

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5.2 Functional Block Diagram

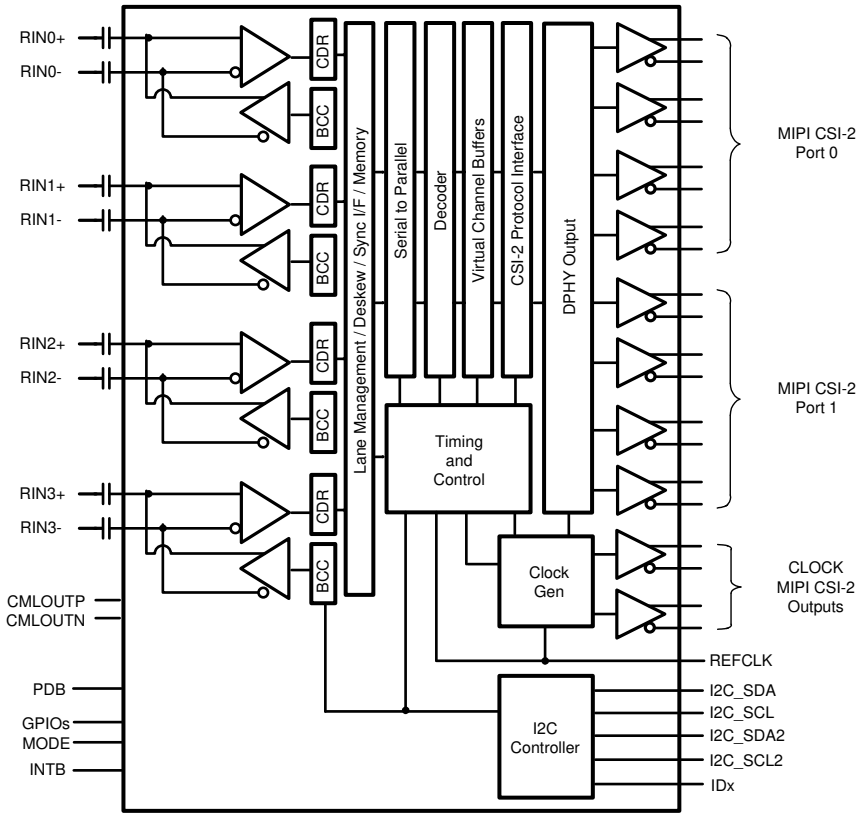

Figure 5-1. Functional Block Diagram

5.3 Feature Description

The DS90UB964-Q1 provides a 4:2 hub for sensor applications. The device includes four FPD-Link III inputs for sensor data streams from up to four serializers. Data received from the four input ports is aggregated onto one or two 4-lane CSI-2 interfaces.

5.4 Device Functional Modes

The DS90UB964-Q1 supports the following operating modes:

- RAW10 (DS90UB913A/933 compatible)
- RAW12 LF (DS90UB913A/933 compatible)
- RAW12 HF (DS90UB913A/933 compatible)

The modes mainly control the FPD-Link III receiver operation of the device. In each of the cases, the forward channel input consists of 28-bit frames, and the output format for the device is CSI-2 through one or two CSI-2 transmit ports.

Each RX input port can be individually configured for RAW modes of operation. The input mode of operation is controlled by the FPD3_MODE 0x6D[1:0] register bits in the PORT_CONFIG register. The input mode can also be controlled by the MODE strap pin.

The DS90UB964-Q1 includes forwarding control to allow multiple video streams from any of the received ports to be mapped to either of the CSI-2 ports.

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5.4.1 RAW Data Type Support and Rates

The DS90UB964-Q1 receives RAW8, RAW10, or RAW12 data from a DS90UB933-Q1 or DS90UB913A-Q1 serializer. The data is translated into a RAW8, RAW10, or RAW12 CSI-2 video stream for forwarding on one of the CSI-2 transmit ports. For each input port, the CSI-2 packet header VC-ID and Data Type are programmable.

Each Rx Port can support up to:

- 12 bits of DATA + 2 SYNC bits for an input PCLK range of 37.5MHz to 100MHz (75MHz for DS90UB913A-Q1) in the 12-bit, high-frequency mode. Line rate = PCLK × (2/3) × 28. For example, PCLK = 100MHz, line rate = (100MHz) × (2/3) × 28 = 1.87Gbps. Note: No HS/VS restrictions (raw). The back channel rate must be set to 2.5Mbps in this mode.
- 12 bits of DATA + 2 bits SYNC for an input PCLK range of 25MHz to 50MHz in the 12-bit, low-frequency mode. Line rate = PCLK × 28. For example, PCLK = 50MHz, line rate = 50MHz × 28 = 1.40Gbps. Note: No HS/VS restrictions (raw). The back channel rate must be set to 2.5Mbps in this mode.
- 10 bits of DATA + 2 SYNC bits for an input PCLK range of 50MHz to 100MHz in the 10-bit mode. Line rate = (PCLK / 2) × 28. For example, PCLK = 100MHz, line rate = (100 MHz / 2) × 28 = 1.40Gbps. Note: HS/HV is restricted to no more than one transition per 10 PCLK cycles. The back channel rate must be set to 2.5Mbps in this mode.

The DS90UB964-Q1 deserializer also supports DVP formats such as YUV-422 which have the same pixel packing as RAW8, RAW10 or RAW12. For example; there are 3 YUV CSI-2 data types that have the same pixel packing as RAW10: YUV420 10 bit, YUV420 10 bit Chroma shifted or YUV422 10 bit. These formats can be used as well as 8 bit and 12 bit YUV formats which adhere to the same structure as RAW8 and RAW12 respectively.

5.4.2 MODE Pin

Configuration of the device can be done through the MODE input strap pin or through the configuration register bits. A pullup resistor and a pulldown resistor of suggested values can be used to set the voltage ratio of the MODE input (V_{MODE}) and V_{DD18} to select one of the six possible modes. Possible configurations are:

- 12-bit LF / 12-bit HF / 10-bit RAW modes (DS90UB933-Q1 and DS90UB913A-Q1 compatible)

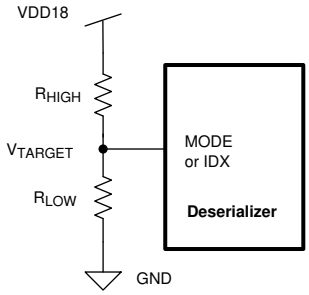

Figure 5-2. Strap Pin Connection Diagram

Table 5-2. Strap Configuration Mode Select

NO.	V_{MODE} VOLTAGE RANGE			V_{MODE} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		RX MODE
	V_{MIN}	V_{TYP}	V_{MAX}	VDD18 = 1.80 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	
0	0	0	0.131 × $V_{(VDD18)}$	0	OPEN	10.0	RESERVED
1	0.179 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.374	88.7	23.2	RAW12 LF
2	0.296 × $V_{(VDD18)}$	0.330 × $V_{(VDD18)}$	0.362 × $V_{(VDD18)}$	0.582	75.0	35.7	RAW12 HF
3	0.412 × $V_{(VDD18)}$	0.443 × $V_{(VDD18)}$	0.474 × $V_{(VDD18)}$	0.792	71.5	56.2	RAW10
4	0.525 × $V_{(VDD18)}$	0.559 × $V_{(VDD18)}$	0.592 × $V_{(VDD18)}$	0.995	78.7	97.6	RESERVED
5	0.642 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.704 × $V_{(VDD18)}$	1.202	39.2	78.7	RAW12 LF
6	0.761 × $V_{(VDD18)}$	0.792 × $V_{(VDD18)}$	0.823 × $V_{(VDD18)}$	1.420	25.5	95.3	RAW12 HF
7	0.876 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	RAW10

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The strapped values can be viewed and/or modified in the following locations:

- RX Mode – Port Configuration FPD3_MODE Register 0x6D[1:0] bits

5.4.3 REFCLK

A valid 23MHz to 25MHz reference clock is required on the REFCLK pin 5 for precise frequency operation. The REFCLK frequency defines all internal clock timers, including the back channel rate, I2C timers, CSI-2 data-rate, FrameSync signal parameters, and other timing critical internal circuitry. REFCLK input must be continuous. If the REFCLK input does not detect a transition for more than 20µs, this can cause a disruption in the CSI-2 output. REFCLK can be applied to the DS90UB964-Q1 only when the supply rails are above minimum levels (see Figure 6-11).

The REFCLK LVCMOS input oscillator specifications are listed in Table 5-3.

Table 5-3. REFCLK Oscillator Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE CLOCK					
Frequency tolerance				±100	ppm
Duty cycle		40%	50%	60%	
Rise/Fall Time	10% - 90%			8	ns
Jitter	500kHz - 50MHz		50	80	ps p-p
Frequency		23		25	MHz

5.4.4 Receiver Port Control

The DS90UB964-Q1 can support up to four simultaneous inputs to Rx ports 0 - 4. The Receiver port control register RX_PORT_CTL 0x0C allows for disabling any Rx inputs when not in use. These bits can only be written by a local I2C controller at the deserializer side of the FPD-Link.

Each FPD-Link III Receive port has a unique set of registers that provides control and status corresponding to Rx ports 0 - 4. Control of the FPD-Link III port registers is assigned by the FPD3_PORT_SEL register, which sets the page controls for reading or writing individual ports unique registers. For each of the FPD-Link III Receive Ports, the FPD3_PORT_SEL 0x4C register defaults to selecting that port's registers as detailed in the register description.

As an alternative to paging to access FPD-Link III Receive unique port registers, separate I2C addresses can be enabled to allow direct access to the port-specific registers. The Port I2C address registers 0xF8 - 0xFB allow programming a separate 7-bit I2C address to allow access to unique, port-specific registers without paging. I2C commands to these assigned I2C addresses are also allowed access to all shared registers.

5.4.5 Input Jitter Tolerance

Input jitter tolerance is the ability of the clock and data recovery (CDR) and phase-locked loop (PLL) of the receiver to track and recover the incoming serial data stream. Jitter tolerance at a specific frequency is the maximum jitter permissible before data errors occur. Figure 5-3 shows the allowable total jitter of the receiver inputs and must be less than the values in Table 5-4.

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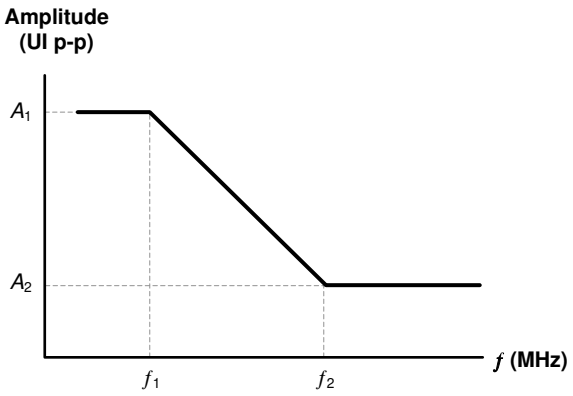

Figure 5-3. Input Jitter Tolerance Plot

Table 5-4. Input Jitter Tolerance Limit

INTERFACE	JITTER AMPLITUDE (UI p-p)		FREQUENCY (MHz) (1)	
FPD3	A1	A2	*f*1	*f*2
	1	0.4	FPD3_PCLK / 80	FPD3_PCLK / 15

(1) FPD3_PCLK frequency is a function of the PCLK, CLK_IN, or REFCLK frequency and dependent on the serializer operating MODE:
10-bit mode: FPD3_PCLK = PCLK / 2
RAW 12-bit HF mode: FPD3_PCLK = 2 x PCLK / 3
RAW 12-bit LF mode: FPD3_PCLK = PCLK

5.4.6 Adaptive Equalizer

The receiver inputs provide an adaptive equalization filter to compensate for signal degradation from the interconnect components. To determine the maximum cable reach, factors that affect signal integrity such as jitter, skew, ISI, crosstalk, and so forth, must be considered. The equalization status and configuration are selected through AEQ registers 0xD2–0xD5.

Each RX receiver incorporates an adaptive equalizer (AEQ), which continuously monitors cable characteristics for long-term cable aging and temperature changes. The AEQ attempts to optimize the equalization setting of the RX receiver.

If the deserializer loses LOCK, the adaptive equalizer resets and performs the LOCK algorithm again to reacquire the serial data stream being sent by the serializer.

5.4.6.1 Channel Requirements

For best AEQ performance and error free operation, the end-to-end transmission channel (including cables, connectors, and PCBs) needs to meet insertion loss, return loss (impedance control), and crosstalk requirements given in Table 5-5 and Table 5-6. Poor impedance control or insertion loss of the transmission channel and poor channel to channel isolation (low IL / FEXT) can result in significant reductions in the maximum transmission distance.

Table 5-5. Transmission Channel Requirements for Coaxial Cable Applications

PARAMETER			MIN	TYP	MAX	UNIT
Z_{trace}	Single-ended PCB trace characteristic impedance		45	50	55	Ω
Z_{cable}	Coaxial cable characteristic impedance		45	50	55	Ω
Z_{con}	Connector (mounted) characteristic impedance		40	50	62.5	Ω
RL	Return Loss, S11	½ f_{BC} < f < 0.1GHz			–16	dB
		0.1GHz < f < 1GHz (f in GHz)			–9 + 7 × log(f)	dB
		1GHz < f < f_{FC}			–9	dB

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Table 5-5. Transmission Channel Requirements for Coaxial Cable Applications (continued)

PARAMETER			MIN	TYP	MAX	UNIT
IL	Insertion Loss, S12	f = 1MHz	–1.4			dB
		f = 5MHz	–2.3			dB
		f = 10MHz	–2.5			dB
		f = 50MHz	–3.5			dB
		f = 100MHz	–4.5			dB
		f = 0.5GHz	–9.5			dB
		f = 1GHz	–14.0			dB
FEXT	Maximum Far End Crosstalk	f < 1.0GHz		–30		dB
NEXT	Maximum Near End Crosstalk	f < 100MHz		–30		dB

Table 5-6. Transmission Channel Requirements for STP / STQ Cable Applications

PARAMETER			MIN	TYP	MAX	UNIT
Z_{trace}	Differential PCB trace characteristic impedance		90	100	110	Ω
Z_{cable}	STP / STQ cable characteristic impedance		85	100	115	Ω
Z_{con}	Differential connector (mounted) characteristic impedance		80	100	125	Ω
RL	Return Loss, SDD11	½ f_{BC} < f < 0.01GHz			–20	dB
		0.01GHz < f < 0.5GHz (f in GHz)			–20 + 20(f)	dB
		0.5GHz < f < f_{FC}			–10	dB
IL	Insertion Loss, SDD12	f = 1MHz	–1.35			dB
		f = 5MHz	–1.8			dB
		f = 10MHz	–2.1			dB
		f = 50MHz	–3.8			dB
		f = 100MHz	–4.9			dB
		f = 0.5GHz	–11.3			dB
		f = 1GHz	–17.3			dB
IL/ FEXT	Insertion Loss to Far End Crosstalk Ratio	f < 1.0GHz	-20			dB
NEXT	Maximum Near End Crosstalk	f < 200MHz			-30	dB

5.4.6.2 Adaptive Equalizer Algorithm

The AEQ process steps through the allowed equalizer control values to find a value that allows the Clock Data Recovery (CDR) circuit to keep a valid lock condition. The circuit waits for a programmed re-lock time period for each EQ setting, then the circuit checks the results for a valid lock. If a valid lock is detected, the circuit stops at the current EQ setting and maintains a constant value as long as the lock state persists. If the deserializer loses the lock, the adaptive equalizer resumes the LOCK algorithm and the EQ setting is incremented to the next valid state. When the lock is lost, the circuit searches the EQ settings to find another valid setting to reacquire the serial data stream sent by the serializer that remains locked. TI recommends setting LINK_ERROR_COUNT_EN and LINK_SFIL_WAIT to 1 in Register 0xB9 to increase link robustness.

5.4.6.3 AEQ Settings

5.4.6.3.1 AEQ Start-Up and Initialization

The AEQ circuit can be restarted at any time by setting the AEQ_RESTART bit in the AEQ_CTL2 register 0xD2. When the deserializer is powered on, the AEQ is continually searching through the EQ settings and can be at any setting when the serializer supplies a signal. If the Rx Port CDR locks to the signal, the EQ setting can be acceptable for low bit errors, but the setting can be unoptimized or overequalized. When connected to a compatible serializer (DS90UB933-Q1 or DS90UB913A-Q1), the DS90UB964-Q1 restarts the AEQ adaption by

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default after the device achieves the first positive lock indication to supply a more consistent start-up from known conditions.

With this feature disabled, the AEQ can lock at a relatively random EQ setting based on when the FPD-Link III input signal is initially present. Alternatively, AEQ_RESTART or DIGITAL_RESET0 can be applied once the compatible serializer input signal frequency is stable to restart adaption from the minimum EQ gain value. These techniques allow for a more consistent initial EQ setting following adaption.

5.4.6.3.2 AEQ Range

The AEQ circuit can be programmed with minimum and maximum settings used during the EQ adaption. Using the full AEQ range provides the most flexibility if the channel conditions are known. However, an improved deserializer lock time can be achieved by narrowing the search window for allowable EQ gain settings. For example, in a system use case with a longer cable and multiple interconnects creating higher channel attenuation, the AEQ does not adapt to the minimum EQ gain settings. Likewise, in a system use case with a short cable and low channel attenuation, the AEQ does not generally adapt to the highest EQ gain settings. The AEQ range is determined by the AEQ_MIN_MAX register 0xD5 where AEQ_MAX sets the maximum value of EQ gain. The ADAPTIVE_EQ_FLOOR_VALUE determines the starting value for EQ gain adaption. To enable the minimum AEQ limit, the SET_AEQ_FLOOR bit in the AEQ_CTL2 register 0xD2[2] must also be set. An AEQ range (AEQ_MAX - AEQ_FLOOR) to allow a variation around the nominal setting of –2/+4 or ±3 around the nominal AEQ value specific to Rx port channel characteristics gives a good trade-off in lock time and adaptability. The setting for the AEQ after adaption can be read back from the AEQ_STATUS register 0xD3.

5.4.6.3.3 AEQ Timing

The dwell time for AEQ to wait for lock or error-free status is also programmable. When checking each EQ setting, the AEQ waits for a time interval which is controlled by the ADAPTIVE_EQ_RELOCK_TIME field in the AEQ_CTL2 register before incrementing to the next allowable EQ gain setting. The default wait time is set to 2.62ms based on REFCLK = 25MHz. When the maximum setting is reached and there is no lock acquired during the programmed relock time, the AEQ restarts adaption at minimum setting or AEQ_FLOOR value.

5.4.6.3.4 AEQ Threshold

The DS90UB964-Q1 receiver adapts by default based on the FPD-Link error checking during the Adaptive Equalization process. The specific errors linked to equalizer adaption, FPD-Link III clock recovery error, packet encoding error, and parity error can be individually selected in AEQ_CTL register 0x42. Errors are accumulated over 1/2 of the period of the timer set by the ADAPTIVE_EQ_RELOCK_TIME. If the number of errors is greater than the programmed threshold (AEQ_ERR_THOLD), the AEQ attempts to increase the EQ setting.

5.4.7 Channel Monitor Loop-Through Output Driver

The DS90UB964-Q1 includes an internal **C**hannel **M**onitor **L**oop-through output on the CMLOUTP/N pins. The CMLOUTP/N pins supply a buffered loop-through output driver to observe the jitter after equalization for each of the four RX receiver channels. The CMLOUT monitors the post EQ stage, thus providing the recovered input of the deserializer signal. The measured serial data width on the CMLOUT loop-through is the total jitter including the internal driver, AEQ, back channel echo, and so forth. Each channel also has a CMLOUT monitor and can be used for debug purposes. This CMLOUT is useful in identifying gross signal conditioning issues.

Table 5-7 shows the minimum CMLOUT differential eye opening as a measure of acceptable forward channel signal integrity. A CMLOUT eye opening of at least 0.45 UI suggests that the forward channel signal integrity is likely acceptable. However, further testing such as BIST is recommended to verify error-free operation. An eye opening of less than 0.45 UI indicates possible issues with the forward channel signal integrity.

Table 5-7. CML Monitor Output Driver

PARAMETER		TEST CONDITIONS	PIN	MIN	TYP	MAX	UNIT
E_W	Differential Output Eye Opening	R_L = 100Ω (Figure 5-4)	CMLOUTP, CMLOUTN	0.45			UI(1)

(1) Unit Interval (UI) is equivalent to one ideal serialized data bit width. The UI scales with serializer input PCLK frequency.
10-bit mode: 1 UI = 1 / (28 x PCLK / 2)
RAW 12-bit HF mode: 1 UI = 1 / (28 x 2/3 x PCLK)

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RAW 12-bit LF mode: 1 UI = 1 / (28 x PCLK)

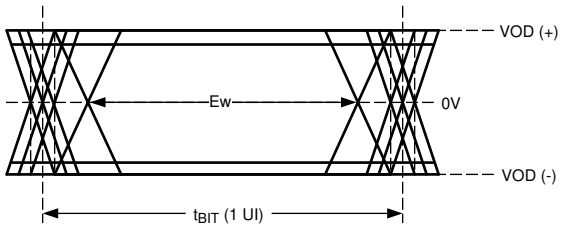

Figure 5-4. CMLOUT Output Driver

Table 5-8 includes details on selecting the corresponding RX receiver of CMLOUTP/N configuration.

Table 5-8. Channel Monitor Loop-Through Output Configuration

	FPD3 RX Port 0	FPD3 RX Port 1	FPD3 RX Port 2	FPD3 RX Port 3
ENABLE MAIN LOOPTHRU DRIVER	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80
SELECT CHANNEL MUX	0xB1 = 0x01 0xB2 = 0x01	0xB1 = 0x01 0xB2 = 0x02	0xB1 = 0x01 0xB2 = 0x04	0xB1 = 0x01 0xB2 = 0x08
SELECT RX PORT	0xB0 = 0x04 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02	0xB0 = 0x08 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02	0xB0 = 0x0C 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02	0xB0 = 0x10 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02

5.4.7.1 Code Example for CMLOUT FPD3 RX Port 0:

```
WriteI2C(0xB0,0x14)   # FPD3 RX Shared, page 0
WriteI2C(0xB1,0x00)   # Offset 0 (reg_0_sh)
WriteI2C(0xB2,0x80)   # Enable loop throu driver
WriteI2C(0xB1,0x01)   # Select Drive Mux
WriteI2C(0xB2,0x01)   #
WriteI2C(0xB0,0x04)   # FPD3 RX Port 0, page 0
WriteI2C(0xB1,0x0F)   #
WriteI2C(0xB2,0x01)   # Loop through select
WriteI2C(0xB1,0x10)   #
WriteI2C(0xB2,0x02)   # Enable CML data output
```

5.4.8 RX Port Status

The DS90UB964-Q1 is able to monitor and detect several other RX port specific conditions and interrupt states. This information is latched into the RX port status registers RX_PORT_STS1 0x4D and RX_PORT_STS2 0x4E. There are bits to flag any change in LOCK status (LOCK_STS_CHG) or detect any errors in the control channel over the forward link (BCC_CRC_ERROR, BCC_SEQ_ERROR) which are cleared upon read. The Rx Port status registers also allow monitoring of the presence stable input signal along with monitoring parity and CRC errors, line length, and lines per video frame.

5.4.8.1 RX Parity Status

The FPD-Link III receiver checks the decoded data parity to detect any errors in the received FPD-Link III frame. Parity errors are counted up and accessible through the RX_PAR_ERR_HI and RX_PAR_ERR_LO registers 0x55 and 0x56 to provide combined 16-bit error counter. In addition, a parity error flag can be set once a programmed number of parity errors have been detected. This condition is indicated by the PARITY_ERROR flag in the RX_PORT_STS1 register. Reading the counter value clears the counter value and PARITY_ERROR flag. An interrupt can also be generated based on assertion of the parity error flag. By default, the parity error

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counter is cleared and flag is cleared on loss of Receiver lock. To get an exact read of the parity error counter, parity checking must be disabled in the GENERAL_CFG register 0x02 before reading the counter.

5.4.8.2 FPD-Link Decoder Status

The FPD-Link III receiver also checks the decoded data for encoding or sequence errors in the received FPD-Link III frame. If either of these error conditions are detected the FPD3_ENC_ERROR bit latches in the RX_PORT_STS2 register 0x4E[5]. An interrupt can also be generated based on assertion of the encoded error flag. To detect FPD-Link III Encoder errors, the LINK_ERROR_COUNT must be enabled with a LINK_ERR_THRESH value greater than 1. Otherwise, the loss of Receiver Lock prevents detection of the Encoder error. The FPD3_ENC_ERROR flag is cleared on read.

5.4.8.3 RX Port Input Signal Detection

The DS90UB964-Q1 can detect and measure the approximate input frequency and frequency stability of each RX input port and indicate status in bits [2:1] of RX_PORT_STS2. Frequency measurement stable FREQ_STABLE indicates the FPD-Link III input clock frequency is stable. When no FPD-Link III input clock is detected at the RX input port, the NO_FPD3_CLK bit indicates that condition has occurred. The setting of these error flags is dependent on the stability control settings in the FREQ_DET_CTL register 0x77. The NO_FPD3_CLK bit is set if the input frequency is below the setting programmed in the FREQ_LO_THR setting in the FREQ_DET_CTL register. A change in frequency FREQ_STABLE = 0, is defined as any change in MHz greater than the value programmed in the FREQ_HYST value. The frequency is continually monitored and provided for readback through the I2C interface less than every 1 ms. A 16-bit value is used to provide the frequency in registers 0x4F and 0x50. An interrupt can also be generated for any of the ports to indicate if a change in frequency is detected on any port.

5.4.9 GPIO Support

The DS90UB964-Q1 supports 8 pins which are programmable for use in multiple options through the GPIOx_PIN_CTL registers.

5.4.9.1 GPIO Input Control and Status

Upon initialization GPIO0 through GPIO7 are enabled as inputs by default. Each GPIO pin has an input disable and a pulldown disable control bit with exception of the open-drain GPIO3 pin. By default, the GPIO pin input paths are enabled and the internal pulldown circuit for the GPIO is enabled. The GPIO_INPUT_CTL and GPIO_PD_CTL registers allow control of the input enable and the pulldown, respectively. For example, to disable GPIO1 and GPIO2 as inputs, set register 0x0F[2:1] = 11. For most applications, there is no need to modify the default register settings for the pull down resistors. The status HIGH or LOW of each GPIO pin 0 through 7 can be read through the GPIO_PIN_STS register 0x0E. This register read operation provides the status of the GPIO pin independent of whether the GPIO pin is configured as an input or output.

5.4.9.2 GPIO Output Pin Control

Individual GPIO output pin control is programmable through the GPIOx_PIN_CTL registers 0x10 to 0x17. To enable any of the GPIO as output, set bit 0 = 1 in the respective register 0x10 to 0x17 after clearing the corresponding input enable bit in register 0x0F.

5.4.9.3 Back Channel GPIO

Each DS90UB964-Q1 GPIO pin defaults to input mode at start-up. The deserializer can link GPIO pin input data on up to four available slots to send on the back channel per each remote serializer connection. Any of the 8 GPIO pin data can be mapped to send over the available back channel slots for each FPD-Link III Rx port. The same GPIO on the deserializer pin can be mapped to multiple back channel GPIO signals. For 2.5Mbps back channel operation, the frame period is 12µs (30 bits × 400ns/bit).

In addition to sending GPIO from pins, an internally generated FrameSync or external FrameSync input signal can be mapped to any of the back channel GPIOs for synchronization of multiple sensors with extremely low skew (see *Section 5.4.22*).

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For each port, the following GPIO control is available through the BC_GPIO_CTL0 register 0x6E and BC_GPIO_CTL1 register 0x6F.

5.4.9.4 GPIO Pin Status

GPIO pin status can be read through the GPIO_PIN_STS register 0x0E. This register provides the status of the GPIO pin independent of whether the GPIO pin is configured as an input or output.

5.4.9.5 Other GPIO Pin Controls

Each GPIO pin can has a input disable and a pulldown disable. By default, the GPIO pin input paths are enabled and the internal pulldown circuit in the GPIO is enabled. The GPIO_INPUT_CTL register 0x0F and GPIO_PD_CTL register 0xBE allow control of the input enable and the pulldown, respectively. For most applications, there is no need to modify the default register settings.

5.4.10 RAW Mode LV / FV Controls

The RAW modes provide FrameValid (FV) and LineValid (LV) controls for the video framing. The FV is equivalent to a Vertical Sync (VSYNC) while the LineValid is equivalent to a Horizontal Sync (HSYNC) input to the DS90UB913A-Q1 / DS90UB933-Q1 device.

The DS90UB964-Q1 allows setting the polarity of these signals by register programming. The FV and LV polarity are controlled on a per-port basis and can be independently set in the PORT_CONFIG2 register 0x7C.

To prevent false detection of FrameValid, FV must be asserted for a minimum number of clocks prior to first video line to be considered valid. The minimum FrameValid time is programmable in the FV_MIN_TIME register 0xBC. Because the measurement is in FPD-Link III clocks, the minimum FrameValid setup to LineValid timing at the Serializer varies based on operating mode.

A minimum FV to LV timing is required when processing video frames at the serializer input. If the FV to LV minimum setup is not met (by default), the first video line is discarded. Optionally, a register control (PORT_CONFIG:DISCARD_1ST_ON_ERR) forwards the first video line missing some number of pixels at the start of the line.

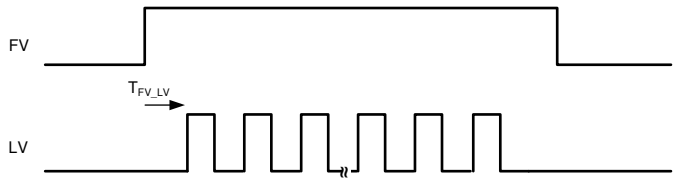

Figure 5-5. Minimum FV to LV

Table 5-9. Minimum FV to LV Setup Requirement (in Serializer PCLKs)

MODE	FV_MIN_TIME Conversion Factor	Absolute Min (FV_MIN_TIME = 0)	Default (FV_MIN_TIME = 128)
RAW12 LF	1	2	130
RAW12 HF	1.5	3	195
RAW10	2	5	261

For other settings of FV_MIN_TIME, use Equation 1 to determine the required FV to LV setup in Serializer PCLKs.

$$\text{Absolute Min} + (\text{FV_MIN_TIME} \times \text{Conversion factor}) \quad (1)$$

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5.4.11 Video Stream Forwarding

Video stream forwarding is handled by the Rx Port forwarding control in register 0x20. Forwarding from input ports are disabled by default and must be enabled using per-port controls. Different options for forwarding CSI-2 packets can also be selected as described starting in *Section 5.4.23*.

5.4.12 CSI-2 Protocol Layer

The DS90UB964-Q1 implements High-Speed mode to forward CSI-2 Low Level Protocol data. This includes features as described in the Low Level Protocol section of the MIPI CSI-2 Specification. This mode supports short and long packet formats.

The feature set of the protocol layer implemented by the CSI-2 TX is:

- Transport of arbitrary data (payload-independent)
- 8-bit word size
- Support for up to four interleaved virtual channels on the same link
- Special packets for frame start, frame end, line start, and line end information
- Descriptor for the type, pixel depth, and format of the Application Specific Payload data
- 16-bit Checksum Code for error detection

Figure 5-6 shows the CSI-2 protocol layer with short and long packets.

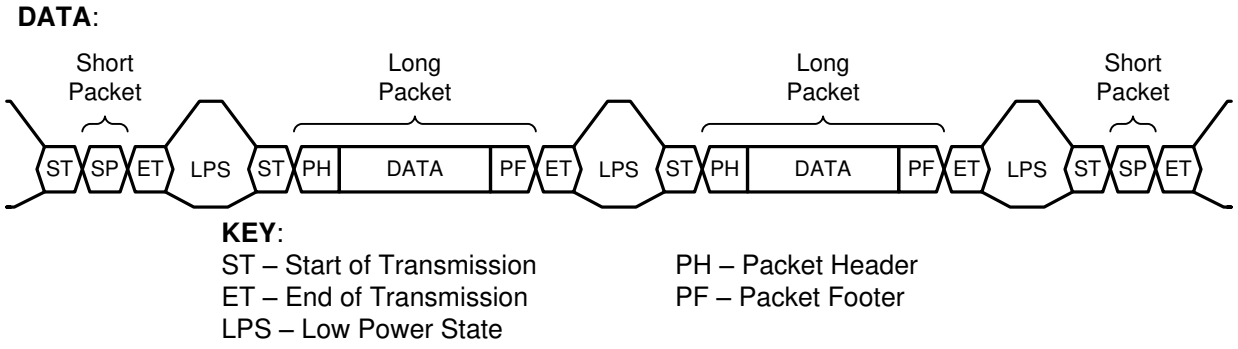

Figure 5-6. CSI-2 Protocol Layer With Short and Long Packets

5.4.13 CSI-2 Short Packet

The short packet provides frame or line synchronization. Figure 5-7 shows the structure of a short packet. A short packet is identified by data types 0x00 to 0x0F.

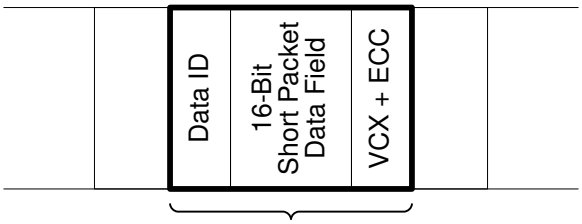

Figure 5-7. CSI-2 Short Packet Structure

5.4.14 CSI-2 Long Packet

A long packet consists of three elements: a 32-bit packet header (PH), an application-specific data payload with a variable number of 8-bit data words, and a 16-bit packet footer (PF). The packet header is further composed of three elements: an 8-bit data identifier, a 16-bit word count field, and an 8-bit ECC. The packet footer has one element, a 16-bit checksum. Figure 5-8 shows the structure of a long packet.

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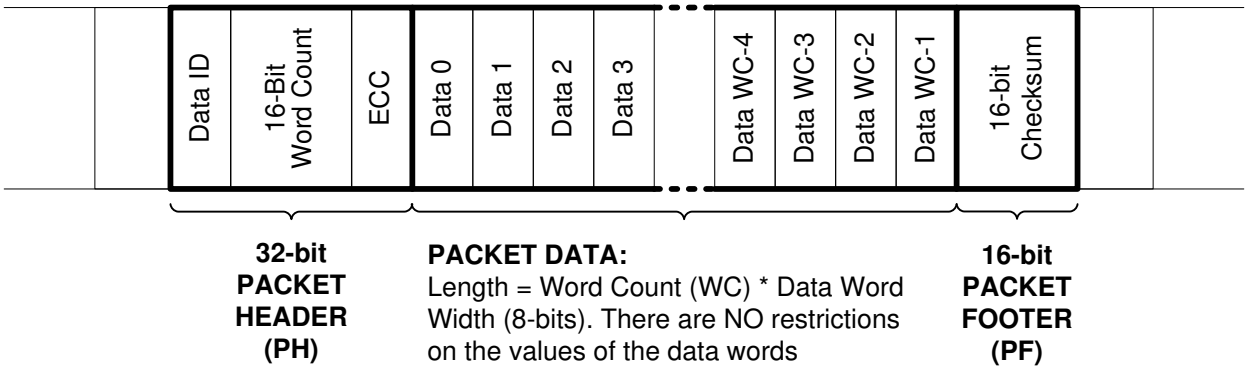

Figure 5-8. CSI-2 Long Packet Structure

Table 5-10. CSI-2 Long Packet Structure Description

PACKET PART	FIELD NAME	SIZE (BIT)	DESCRIPTION
Header	VC / Data ID	8	Contains the virtual channel identifier and the data-type information.
	Word Count	16	Number of data words in the packet data. A word is 8 bits.
	ECC	8	ECC for data ID and WC field. Allows 1-bit error recovery and 2-bit error detection.
Data	Data	WC * 8	Application-specific payload (WC words of 8 bits).
Footer	Checksum	16	16-bit cyclic redundancy check (CRC) for packet data.

5.4.15 CSI-2 Data Identifier

The DS90UB964-Q1 MIPI CSI-2 protocol interface transmits the data identifier byte containing the values for the virtual channel ID (VC) and data type (DT) for the application specific payload data, as shown in Figure 5-9. The virtual channel ID is contained in the 2 MSBs of the data identifier byte and identify the data as directed to one of four virtual channels. The value of the data type is contained in the 6 LSBs of the data identifier byte. The received RAW mode data is converted to CSI-2 Tx packets with assigned data type and virtual channel ID.

DVP format serializer inputs must have discrete synchronization signals. The DS90UB964-Q1 utilizes the HSYNC and VSYNC inputs to construct the MIPI CSI-2 Tx data packets. The DS90UB964-Q1 deserializer supports RAW8, RAW10 or RAW12 as well as formats which have the same pixel packing as RAW8, RAW10 or RAW12 such as YUV-422.

For each RX Port, register defines with which channel and data type the context is associated:

- Register 0x70 describes RAW10 Mode and 0x71 describes RAW12 Mode.
- For RAW8 support, configure the link for RAW10 mode and set 0x7C[7:6] to select the upper or lower 8-bits.
- RAW1x_VC[7:6] field defines the associated virtual ID transported by the CSI-2 protocol from the camera sensor.
- RAW1x_ID[5:0] field defines the associated data type. The data type is a combination of the data type transported by the CSI-2 protocol.

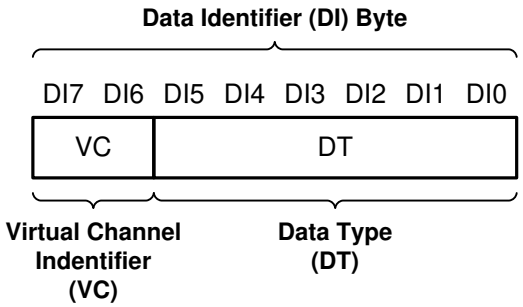

Figure 5-9. CSI-2 Data Identifier Structure

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5.4.16 Virtual Channel and Context

The CSI-2 protocol layer transports virtual channels. The purpose of virtual channels is to separate different data flows interleaved in the same data stream. Each virtual channel is identified by a unique channel identification number in the packet header. Therefore, a CSI-2 TX context can be associated with a virtual channel and a data type. Virtual channels are defined by a 2-bit field. This channel identification number is encoded in the 2-bit code.

The CSI-2 TX transmits the channel identifier number and multiplexes the interleaved data streams. The CSI-2 TX supports up to four concurrent virtual channels.

5.4.17 CSI-2 Mode Virtual Channel Mapping

The CSI-2 Mode provides per-port Virtual Channel ID mapping. For each FPD-Link III input port, separate mapping can be done for each input to any of the four VC-ID values. The mapping is controlled by the VC_ID_MAP register. This function sends the output as a time-multiplexed CSI-2 stream, where the video sources are differentiated by the virtual channel.

5.4.17.1 Example 1

The DS90UB964-Q1 is receiving data from sensors attached to each port. Each port is sending a video stream. The DS90UB964-Q1 can be configured to map the VC-IDs so that each video stream has a unique ID. The direct implementation maps VC-ID of 0 for RX Port 0, VC-ID of 1 for RX Port 1, VC-ID of 2 for RX Port 2, and VC-ID of 3 for RX Port 3.

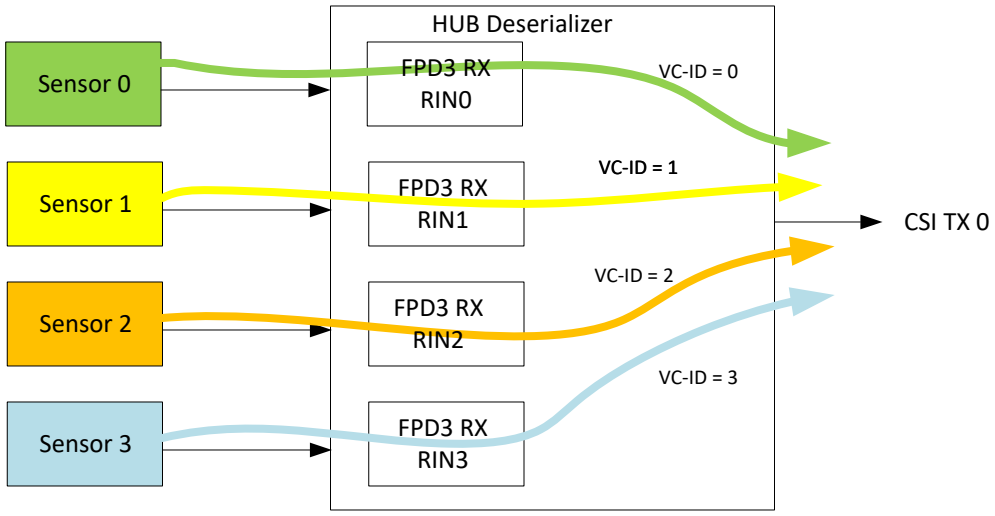

Figure 5-10. VC-ID Mapping Example 1

5.4.17.2 Example 2

The DS90UB964-Q1 is receiving data from sensors attached to each port. Each port is sending a video stream. The DS90UB964-Q1 can be configured to map the VC-IDs and distribute to different CSI-2 Transmitters. This implementation maps VC-ID of 0 for RX Port 0, VC-ID of 1 for RX Port 1, VC-ID of 0 for RX Port 2, and VC-ID of 1 for RX Port 3. RX Ports 0 and 1 are assigned to CSI-2 Transmitter 0 which RX Ports 2 and 3 are assigned to CSI-2 Transmitter 1.

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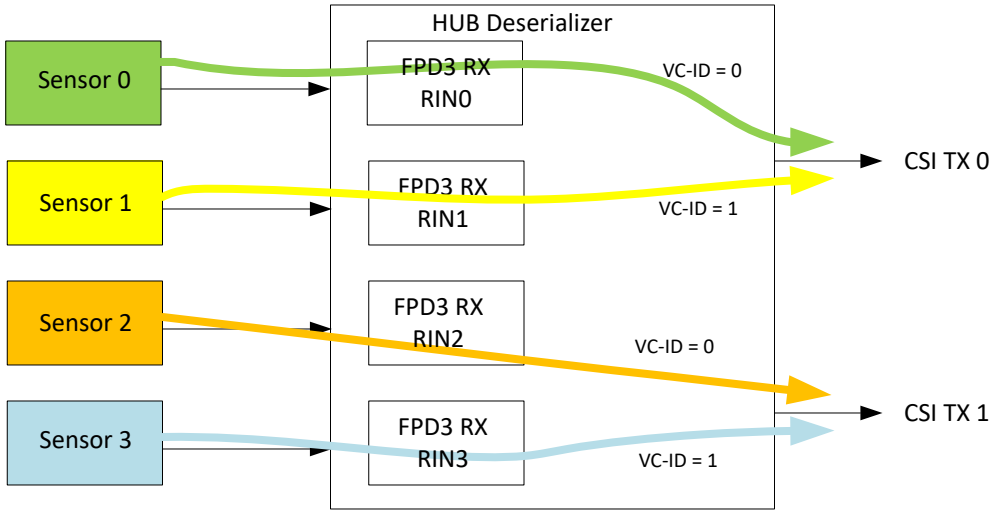

Figure 5-11. VC-ID Mapping Example 2

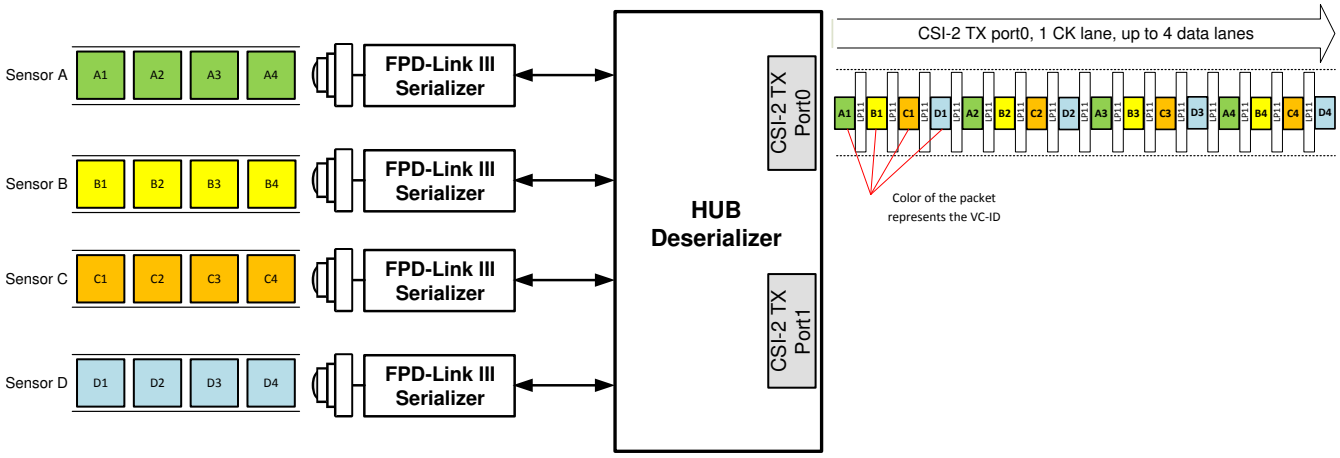

Figure 5-12. Four Sensor Data onto CSI-2 With Virtual Channels (VC-ID)

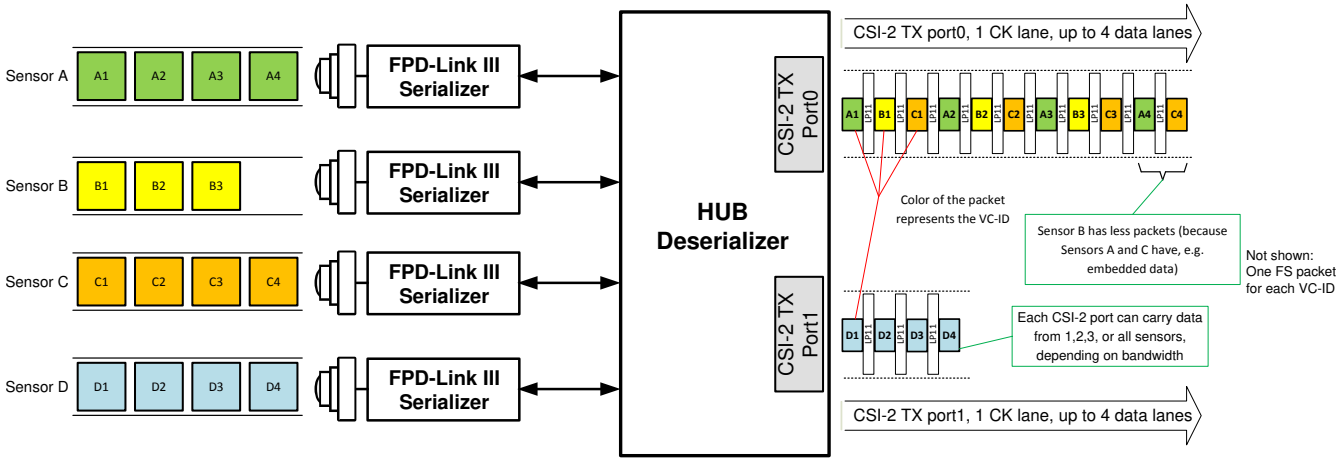

Figure 5-13. Four Sensor Data onto CSI-2 With Virtual Channels (VC-ID) With Different Frame Size

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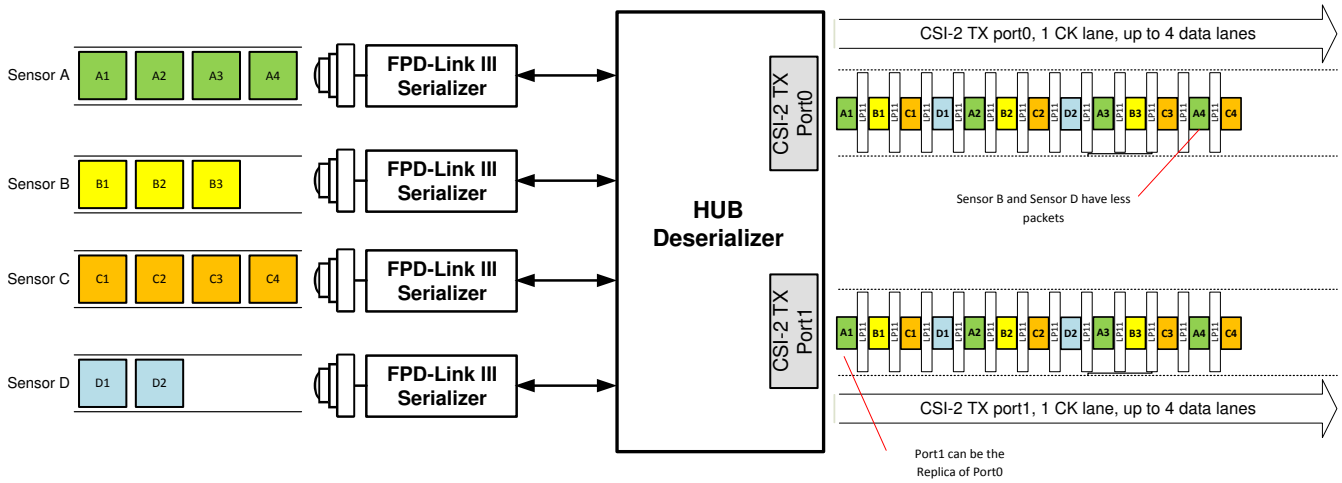

Figure 5-14. Four Sensor Data onto 1xCSI-2 Replicated With Virtual Channels (VC-ID) With Different Frame Size

5.4.18 CSI-2 Transmitter Frequency

The CSI-2 Transmitters can operate at 400Mbps, 800Mbps, or 1.6Gbps per data lane. This operation is controlled through the CSI_PLL_CTL 0x1F register.

Table 5-11. CSI-2 Transmitter Frequency vs CSI_PLL_CTL

CSI_PLL_CTL[1:0]	CSI-2 TX Data Rate	REFCLK Frequency
00	1.6Gbps	25MHz
	1.472Gbps	23MHz
01	Reserved	Reserved
10	800Mbps	25MHz
11	400Mbps	25MHz

When configuring to 800Mbps or 1.6Gbps, the CSI-2 timing parameters are automatically set based on the CSI_PLL_CTL 0x1F register. In the case of 400Mbps, the respective CSI-2 timing parameters registers must be programmed, and the appropriate override bit must be set. To enable CSI-2 400Mbps mode, set the following registers:

```
# Set CSI-2 Timing parameters
WriteI2C(0xB0,0x2)    # set auto-increment, page 0
WriteI2C(0xB1,0x40)   # CSI-2 Port 0
WriteI2C(0xB2,0x83)   # TCK Prep
WriteI2C(0xB2,0x8D)   # TCK Zero
WriteI2C(0xB2,0x87)   # TCK Trail
WriteI2C(0xB2,0x87)   # TCK Post
WriteI2C(0xB2,0x83)   # THS Prep
WriteI2C(0xB2,0x86)   # THS Zero
WriteI2C(0xB2,0x84)   # THS Trail
WriteI2C(0xB2,0x86)   # THS Exit
WriteI2C(0xB2,0x84)   # TLPX
```

```
# Set CSI-2 Timing parameters
WriteI2C(0xB0,0x2)    # set auto-increment, page 0
WriteI2C(0xB1,0x60)   # CSI-2 Port 1
WriteI2C(0xB2,0x83)   # TCK Prep
WriteI2C(0xB2,0x8D)   # TCK Zero
WriteI2C(0xB2,0x87)   # TCK Trail
WriteI2C(0xB2,0x87)   # TCK Post
WriteI2C(0xB2,0x83)   # THS Prep
WriteI2C(0xB2,0x86)   # THS Zero
WriteI2C(0xB2,0x84)   # THS Trail
WriteI2C(0xB2,0x86)   # THS Exit
WriteI2C(0xB2,0x84)   # TLPX
```

5.4.19 CSI-2 Transmitter Status

The status of the CSI-2 Transmitter can be monitored by readback of the CSI_STS register 0x35, or brought to one of the configurable GPIO pins as an output. The TX_PORT_PASS 0x35[0] indicates valid CSI-2 data being presented on CSI-2 port. If no data is being forwarded or if error conditions have been detected on the video data, the CSI-2 Pass signal is cleared. The TX_PORT_SYNC 0x35[0] indicates the CSI-2 Tx port is able to properly synchronize input data streams from multiple sources. TX_PORT_SYNC always returns 0 if Synchronized Forwarding is disabled. Interrupts can also be generated based on changes in the CSI-2 port status.

5.4.20 Video Buffers

The DS90UB964-Q1 implements four video line buffer/FIFO, one for each RX channel. The video buffers provide storage of data payload and forward requirements for sending multiple video streams on the CSI-2 transmit ports. The total line buffer memory size is a 16-kB block for each RX port.

The CSI-2 transmitter waits for an entire packet to be available before pulling data from the video buffers.

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5.4.21 CSI-2 Line Count and Line Length

The DS90UB964-Q1 counts the number of lines (long packets) to determine line count on LINE_COUNT_1/0 registers 0x73–74. For line length, DS90UB964-Q1 generates the word count field in the CSI-2 header on LINE_LEN_1/0 registers 0x75 – 0x76.

5.4.22 FrameSync Operation

A frame synchronization signal (FrameSync) can be sent through the back channel using any of the back channel GPIOs. The signal can be generated in two different methods. The first option offers sending the external FrameSync using one of the available GPIO pins on the DS90UB964-Q1 and mapping that GPIO to a back channel GPIO on one or more of the FPD-Link III ports.

The second option is to have the DS90UB964-Q1 internally generate a FrameSync signal to send through GPIO to one or more of the attached Serializers.

FrameSync signaling on the four back channels is synchronous. Thus, the FrameSync signal arrives at each of the four serializers with limited skew.

5.4.22.1 External FrameSync Control

In External FrameSync mode, an external signal is input to the DS90UB964-Q1 through one of the GPIO pins on the device. The external FrameSync signal can be propagated to one or more of the attached FPD3 Serializers through a GPIO signal in the back channel.

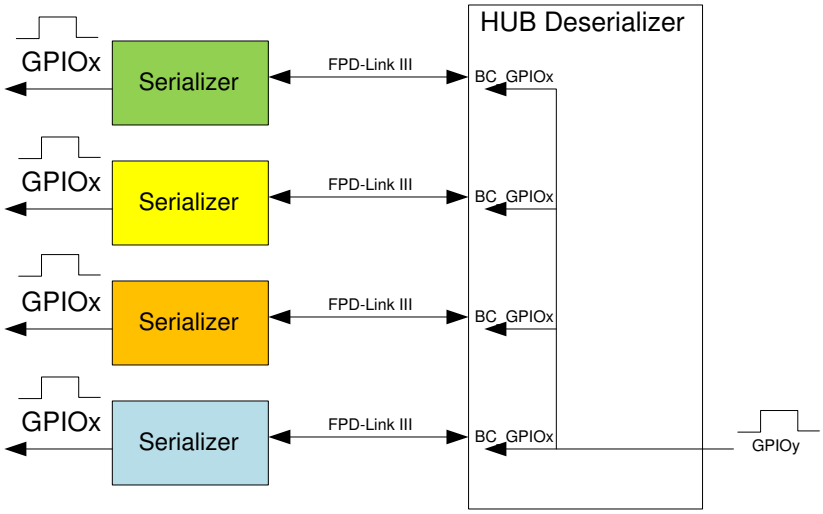

Figure 5-15. External FrameSync

Enabling the external FrameSync mode is done by setting the FS_MODE control in the FS_CTL register to a value between 0x8 (GPIO0 pin) to 0xF (GPIO7 pin). Set FS_GEN_ENABLE to 0 for this mode.

To send the FrameSync signal on the BC_GPIOx signal of an FPD-Link port, the BC_GPIO_CTL0 or BC_GPIO_CTL1 register can be programmed for that port to select the FrameSync signal.

5.4.22.2 Internally Generated FrameSync

In Internal FrameSync mode, an internally generated FrameSync signal is sent to one or more of the attached FPD3 Serializers through a GPIO signal in the back channel.

FrameSync operation is controlled by the FS_CTL, FS_HIGH_TIME_x, and FS_LOW_TIME_x 0x18 – 0x1C registers. The resolution of the FrameSync generator clock (FS_CLK_PD) is derived from the back channel frame period (BC_FREQ_SELECT register). For each 2.5Mbps back channel operation, the frame period is 12µs (30 bits × 400ns/bit).

Once enabled, the FrameSync signal is sent continuously based on the programmed conditions.

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Note

The value programmed to the FS_HIGH_TIME register must be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field results in a 1 cycle high pulse on the FrameSync signal.

Enabling the internal FrameSync mode is done by setting the FS_GEN_ENABLE control in the FS_CTL register to a value of 1. The FS_MODE field controls the clock source used for the FrameSync generation. The FS_GEN_MODE field configures whether the duty cycle of the FrameSync is 50/50 or whether the high and low periods are controlled separately. The FrameSync high and low periods are controlled by the FS_HIGH_TIME and FS_LOW_TIME registers.

The accuracy of the internally generated FrameSync is directly dependent on the accuracy of the REFCLK.

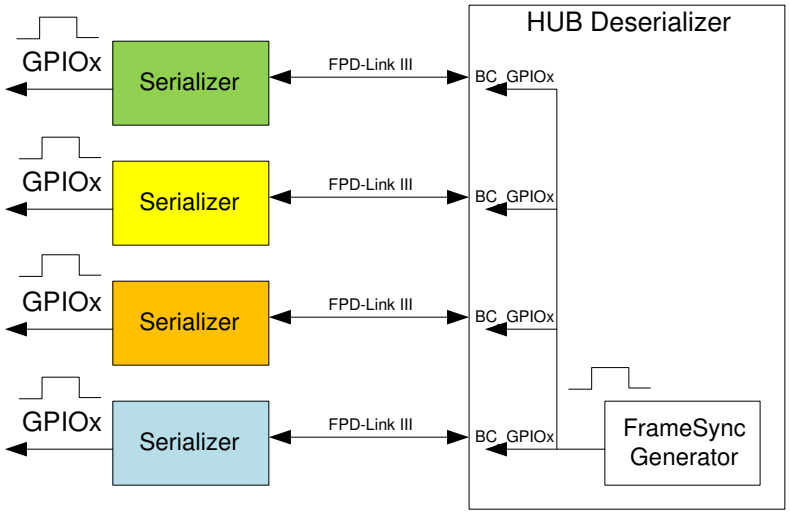
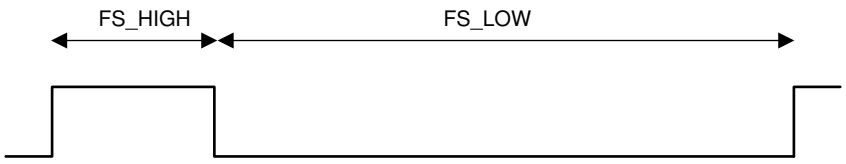


Figure 5-16. Internal FrameSync



FS_LOW = FS_LOW_TIME * FS_CLK_PD
FS_HIGH = FS_HIGH_TIME * FS_CLK_PD
where FS_CLK_PD is the resolution of the FrameSync generator clock

Figure 5-17. Internal FrameSync Signal

The following example shows generation of a FrameSync signal at 60 pulses per second. Mode settings:

- Programmable High/Low periods: FS_GEN_MODE 0x18[1]=0
- Use port 0 back channel frame period: FS_MODE 0x18[7:4]=0x0
- Back channel rate of 2.5Mbps: BC_FREQ_SELECT for port 0 0x58[2:0]=0x0
- Initial FS state of 0: FS_INIT_STATE 0x18[2]=0

Based on mode settings, the FrameSync is generated based upon FS_CLK_PD of 12µs.

The total period of the FrameSync is (1 sec / 60 Hz) / 12µs or approximately 1,389 counts.

For a 10% duty cycle, set the high time to 139 (0x008A) cycles, and the low time to 1,250 (0x04E1) cycles:

- FS_HIGH_TIME_1: 0x19=0x00
- FS_HIGH_TIME_0: 0x1A=0x8A
- FS_LOW_TIME_1: 0x1B=0x04

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- FS_LOW_TIME_0: 0x1C=0xE1

5.4.22.2.1 Code Example for Internally Generated FrameSync

```
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x10,0x91) # FrameSync signal; Device Status; Enabled
WriteI2C(0x58,0x58) # BC FREQ SELECT: 2.5 Mbps
WriteI2C(0x19,0x00) # FS_HIGH_TIME_1
WriteI2C(0x1A,0x8A) # FS_HIGH_TIME_0
WriteI2C(0x1B,0x04) # FS_LOW_TIME_1
WriteI2C(0x1C,0xE1) # FS_LOW_TIME_0
WriteI2C(0x18,0x01) # Enable FrameSync
```

5.4.23 CSI-2 Forwarding

Video stream forwarding is handled by the forwarding control in the DS90UB964-Q1 on FWD_CTL1 register 0x20. The forwarding control pulls data from the video buffers for each FPD-Link III RX port and forwards the data to one of the CSI-2 output interfaces. Forwarding control also handles generation of transitions between LP and HS modes as well as sending of Synchronization frames. The forwarding control monitors each of the video buffers for packet and data availability.

Forwarding from input ports can be disabled using per-port controls. Each of the forwarding engines can be configured to pull data from any of the four video buffers, although a buffer can only be assigned to one CSI-2 Transmitter at a time. The two forwarding engines operate independently. Video buffers are assigned to the CSI-2 Transmitters using the mapping bits in the FWD_CTL1 register 0x20[7:4].

5.4.23.1 Best-Effort Round Robin CSI-2 Forwarding

By default, the round-robin (RR) forwarding of packets use standard CSI-2 method of video stream determination. No special ordering of CSI-2 packets are specified, effectively relying on the Virtual Channel Identifier (VC) and Data Type (DT) fields to distinguish video streams. Each image sensor is assigned a VC-ID to identify the source. Different data types within a virtual channel is also supported in this mode.

The forwarding engine forwards packets as packets become available to the forwarding engine. In the case where multiple packets are available to transmit, the forwarding engine typically operates in an RR fashion based on the input port from which the packets are received.

Best-effort CSI-2 RR forwarding has the following characteristics and capabilities:

- Uses Virtual Channel ID to differentiate each video stream
- Separate Frame Synchronization packets for each VC
- No synchronization requirements

This mode of operation allows input RX ports to have different video characteristics, and there is no requirement that the video be synchronized between ports. The attached video processor is required to properly decode the various video streams based on the VC and DT fields.

Best-effort forwarding is enabled by setting the CSIx_RR_FWD bits in the FWD_CTL2 register 0x21.

5.4.23.2 Synchronized CSI-2 Forwarding

In cases with multiple input sources, synchronized forwarding offers synchronization of all incoming data stored within the buffer. If packets arrive within a certain window, the forwarding control can be programmed to attempt to synchronize the video buffer data. In this mode, the forwarding control attempts to send each channel synchronization packets in order (VC0, VC1, VC2, VC3) as well as sending packet data in the same order. In the following sections, Sensor 0 (S0), Sensor 1 (S1), Sensor 2 (S2), and Sensor 3 (S3) refers to the sensors

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connected at FPD3 RX port 0, RX port 1, RX port 2, and RX port 3, respectively. The following describe only the 4-port operation, but other possible port combinations can be applied.

The forwarding engine for each CSI-2 Transmitter can be configured independently and synchronize up to all four video sources.

Requirements:

- Video arriving at input ports must be synchronized within approximately 1 video line period
- All enabled ports must have valid, synchronized video
- Each port must have identical video parameters, including number and size of video lines, presence of synchronization packets, and so forth.

The forwarding engine attempts to send the video synchronized. If synchronization fails, the CSI-2 transmitter stops forwarding packets and attempt to restart sending synchronized video at the next FrameStart indication. Packets are discarded as long as the forwarding engine is unable to send the synchronized video.

Status is provided to indicate when the forwarding engine is synchronized. In addition, a flag is used to indicate that synchronization has been lost (status is cleared on a read).

Three options are available for Synchronized forwarding:

- Basic Synchronized forwarding
- Line-Interleave forwarding
- Line-Concatenated forwarding

Synchronized forwarding modes are selected by setting the CSIx_SYNC_FWD controls in the FWD_CTL2 register. To enable synchronized forwarding the following order of operations is recommended:

1. Disable Best-effort forwarding by clearing the CSIx_RR_FWD bits in the FWD_CTL2 register
2. Enable forwarding per Receive port by clearing the FWD_PORTx_DIS bits in the FWD_CTL1 register
3. Enable Synchronized forwarding in the FWD_CTL2 register

5.4.23.3 Basic Synchronized CSI-2 Forwarding

During Basic Synchronized Forwarding each forwarded frame is an independent CSI-2 video frame including FrameStart (FS), video lines, and FrameEnd (FE) packets. Each forwarded stream can have a unique VC-ID. If the forwarded streams do not have a unique VC-ID, the receiving process can use the frame order to differentiate the video stream packets.

The forwarding engine attempts to send the video synchronized. If synchronization fails, the CSI-2 transmitter stops forwarding packets and attempts to restart sending synchronized video at the next FS indication. Packets are discarded as long as the forwarding engine is unable to send the synchronized video.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS0 – FS1 – FS2 – FS3 – S0L1 – S1L1 – S2L1 – S3L1 – S0L2 – S1L2 – S2L2 – S3L2 – S0L3 …

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... S0LN – S1LN – S2LN – S3LN – FE0 – FE1 – FE2 – FE3

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Notes:

FSx	FrameStart for Sensor X
FEx	FrameEnd for Sensor X
SxLy	Line Y for Sensor X video frame
SxLN	Last line for Sensor X video frame

Each packet includes the virtual channel ID assigned to receive port for each sensor.

5.4.23.3.1 Code Example for Basic Synchronized CSI-2 Forwarding

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x70,0x1F) # RAW10_datatype_yuv422b10_VC0
# "*** RX1 VC=1 ***"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x70,0x5F) # RAW10_datatype_yuv422b10_VC1
# "*** RX2 VC=2 ***"
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0x70,0x9F) # RAW10_datatype_yuv422b10_VC2
# "*** RX3 VC=3 ***"
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0x70,0xDF) # RAW10_datatype_yuv422b10_VC3
#  "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI0 select
#  "CSI_EN"
WriteI2C(0x33,0x01) # CSI_EN & CSI0 4L
#  "***Basic_FWD"
WriteI2C(0x21,0x14) # Synchronized Basic_FWD
#  "***FWD_PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0
```

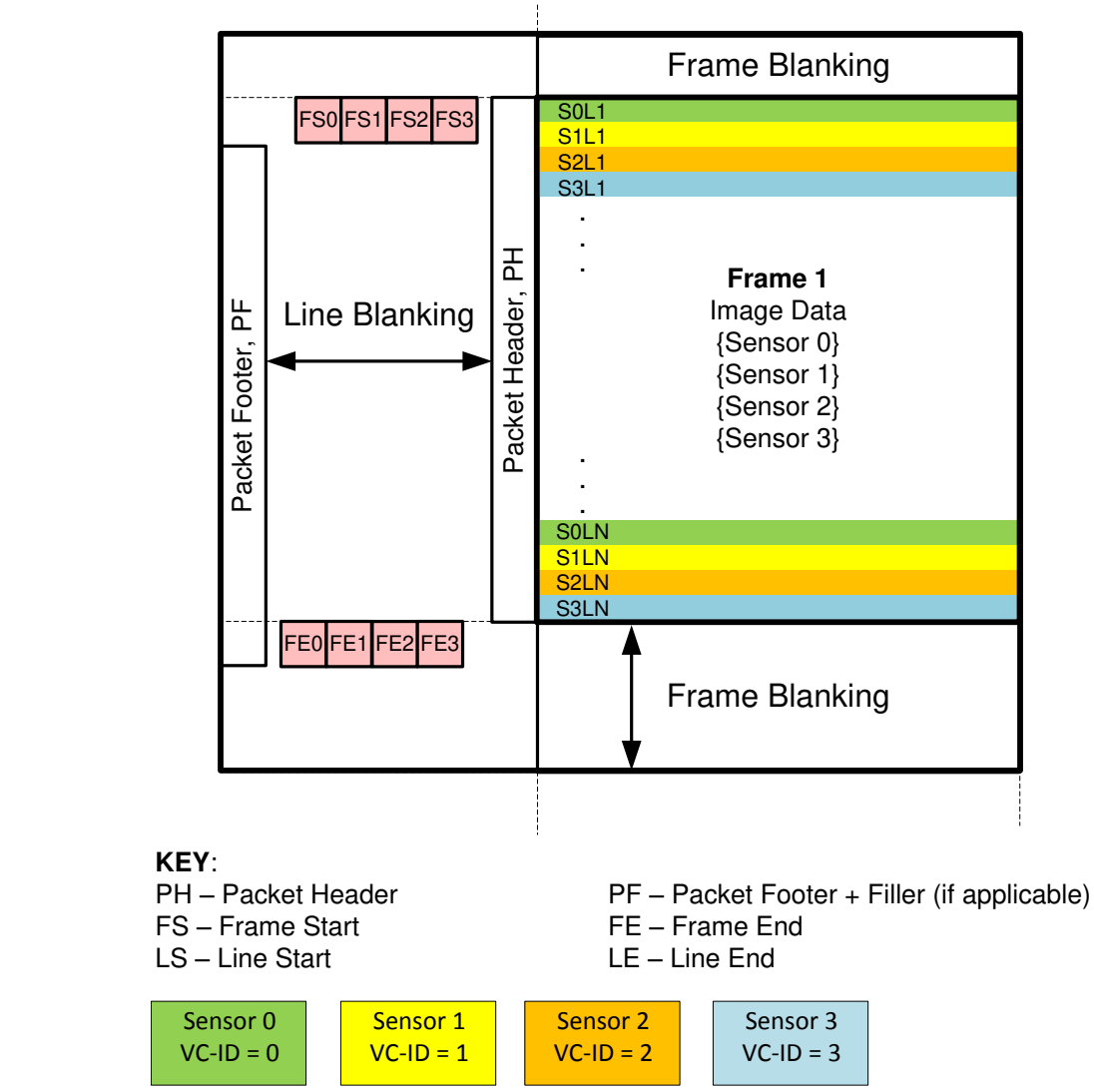

Figure 5-18. Basic Synchronized Format

5.4.23.4 Line-Interleaved CSI-2 Forwarding

In synchronized forwarding, the forwarding engine can be programmed to send only one of each synchronization packet. For example, if forwarding from all four input ports, only one FS, FE packet is sent for each video frame. The synchronization packets for the other 3 ports are dropped. The video line packets for each video stream are sent as individual packets. This effectively merges the frames from N video sources into a single frame that has N times the number of video lines.

In this mode, all video streams must also have the same VC, although this is not checked by the forwarding engine. This is useful when connected to a controller that does not support multiple VCs. The receiving processor must process the image based on order of video line reception.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS0 – S0L1 – S1L1 – S2L1 – S3L1 – S0L2 – S1L2 – S2L2 – S3L2 – S0L3 …

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... S0LN – S1LN – S2LN – S3LN – FE0

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Notes:

FSx	FrameStart for Sensor X
FEx	FrameEnd for Sensor X
SxLy	Line Y for Sensor X video frame
SxLN	Last line for Sensor X video frame

All packets must have the same VC-ID.

5.4.23.4.1 Code Example for Line-Interleaved CSI-2 Forwarding

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4c,0x01) # RX0
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX1 VC=0 ***"
WriteI2C(0x4c,0x12) # RX1
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX2 VC=0 ***"
WriteI2C(0x4c,0x24) # RX2
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX3 VC=0 ***"
WriteI2C(0x4c,0x38) # RX3
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
#  "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI0 select
#  "CSI_EN"
WriteI2C(0x33,0x01) # CSI_EN & CSI0 4L
# "*** CSI0_SYNC_FWD synchronous forwarding with line interleaving ***"
WriteI2C(0x21,0x28) # synchronous forwarding with line interleaving
#  "*** FWD_PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0
```

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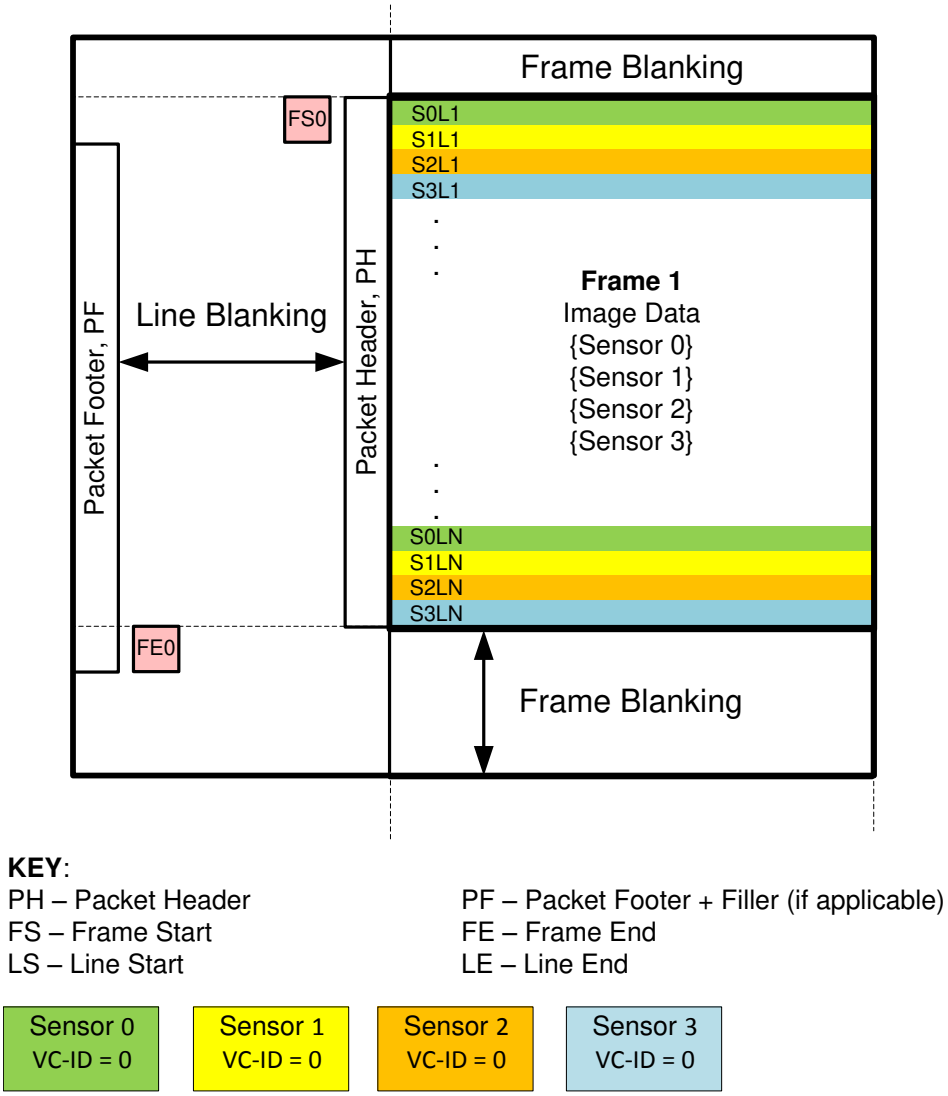

Figure 5-19. Line-Interleave Format

5.4.23.5 Line-Concatenated CSI-2 Forwarding

In synchronized forwarding, the forwarding engine can be programmed to merge video frames from multiple sources into a single video frame by concatenating video lines. Each of the sensors for each RX carry different data streams that get concatenated into one CSI-2 stream. For example, if forwarding from all four input ports, only one FS and one FE packet is sent for each video frame. The synchronization packets for the other 3 ports are dropped. In addition, the video lines from each sensor are combined into a single line. The controller must separate the single video line into the separate components based on position within the concatenated video line.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS0 – S0L1,S1L1,S2L1,S3L1 – S0L2,S1L2,S2L2,S3L2 – S0L3,S1L3,S2L3,S3L3 …

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... S0LN,S1LN,S2LN,S3LN – FE0

Notes:

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FSx	FrameStart for Sensor X
FEx	FrameEnd for Sensor X
SxLy	Line Y for Sensor X video frame
SxLN	Last line for Sensor X video frame

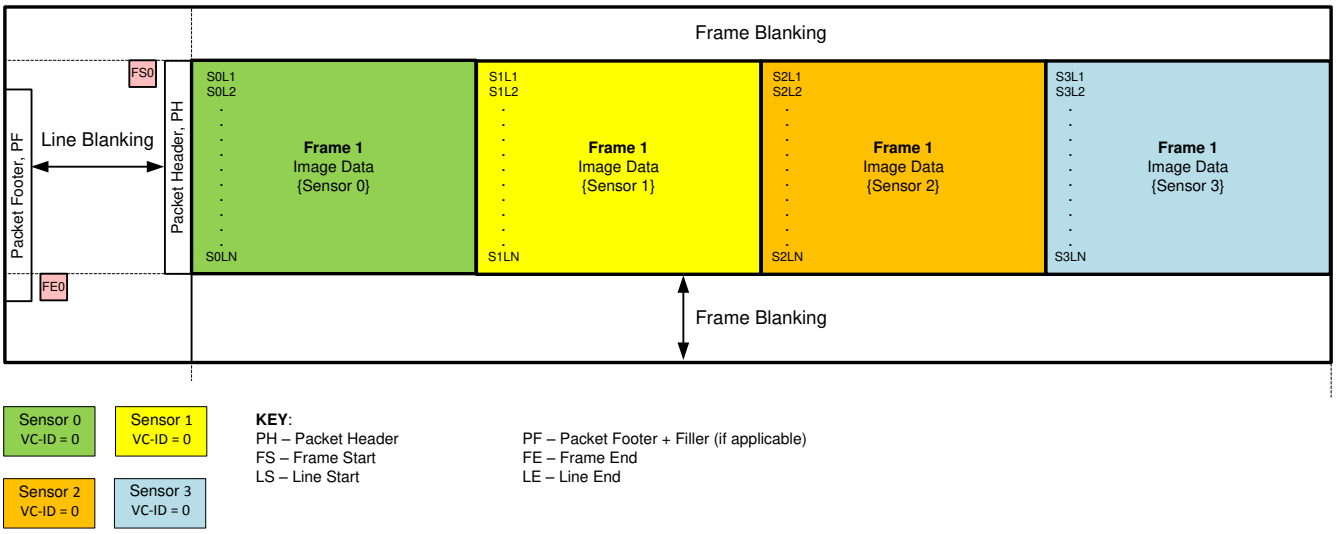
S0L1,S1L1,S2L1,S3L1 indicates concatenation of the first video line from each sensor into a single video line. This packet has a modified header and footer that matches the concatenated line data.

Packets must have the same VC-ID, based on the VC-ID for the lowest number sensor port being forwarded.

Lines are concatenated on a byte basis without padding between video line data.

5.4.23.5.1 Code Example for Line-Concatenated CSI-2 Forwarding

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4c,0x01) # RX0
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX1 VC=0 ***"
WriteI2C(0x4c,0x12) # RX1
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX2 VC=0 ***"
WriteI2C(0x4c,0x24) # RX2
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX3 VC=0 ***"
WriteI2C(0x4c,0x38) # RX3
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
#  "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI0 select
#  "CSI_EN"
WriteI2C(0x33,0x01) # CSI_EN & CSI0 4L
# "*** CSI0_SYNC_FWD synchronous forwarding with line concatenation ***"
WriteI2C(0x21,0x3c) # synchronous forwarding with line concatenation
#  "***FWD_PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0
```



**Blanking intervals do not provide accurate synchronization timing*

Figure 5-20. Line-Concatenated Format

5.4.23.6 CSI-2 Replicate Mode

In CSI-2 Replicate mode, both ports can be programmed to output the same data. The output from CSI-2 port 0 is also presented on CSI-2 port 1.

To configure this mode of operation, set the CSI_REPLICATE bit in the FWD_CTL2 register. This bit must only be set before forwarding is enabled. If this bit is set after forwarding is enabled, unexpected errors can occur.

5.4.23.7 CSI-2 Transmitter Output Control

Two register controls allow control of CSI-2 Transmitter outputs to disable the CSI-2 Transmitter outputs. If the OUTPUT_SLEEP_STATE_SELECT (OSS_SEL) control is set to 0 in the GENERAL_CFG 0x02 register, the CSI-2 Transmitter outputs are forced to the HS-0 state. If the OUTPUT_ENABLE (OEN) register bit is set to 0 in the GENERAL_CFG register, the CSI-2 pins are set to the high-impedance state.

For normal operation (OSS_SEL and OEN both set to 1), the detection of activity on FPD3 inputs determines the state of the CSI-2 outputs. The FPD3 inputs are considered active if the Receiver indicates valid lock to the incoming signal. For a CSI-2 TX port, lock is considered valid if any Received port mapped to the TX port is indicating Lock.

Table 5-12. CSI-2 Output Control Options

PDB pin	OSS_SEL	OEN	FPD3 INPUT	CSI-2 PIN STATE
0	X	X	X	Hi-Z
1	0	X	X	HS-0
1	1	0	X	Hi-Z
1	1	1	Inactive	Hi-Z
1	1	1	Active	Valid

5.4.23.8 Enabling and Disabling CSI-2 Transmitters

Once enabled, the best practice is to leave the CSI-2 Transmitter enabled and only change the forwarding controls if changes are required to the system. When enabling and disabling the CSI-2 Transmitter, forwarding must be disabled for proper start and stop of the CSI-2 Transmitter.

When enabling and disabling the CSI-2 Transmitter, use the following sequence:

To Disable:
1. Disable Forwarding for assigned ports in the FWD_CTL1 register
2. Disable CSI-2 Periodic Calibration (if enabled) in the CSI_ CTL2 register
3. Disable Continuous Clock operation (if enabled) in the CSI_ CTL register
4. Clear CSI-2 Transmit enable in CSI_ CTL register

To Enable:
1. Set CSI-2 Transmit enable (and Continuous clock if desired) in CSI_ CTL register
2. Enable CSI-2 Periodic Calibration (if desired) in the CSI_CTL2 register
3. Enable Forwarding for assigned ports in the FWD_CTL1 register

5.5 Programming

5.5.1 Serial Control Bus

The DS90UB964-Q1 implements two I2C-compatible serial control buses. Both I2C ports support local device configuration and incorporate a bidirectional control channel (BCC) that allows communication with a remote serializers as well as remote I2C target devices.

The device address is set through a resistor divider connected to the IDx pin (R1 and R2 – see Figure 5-21).

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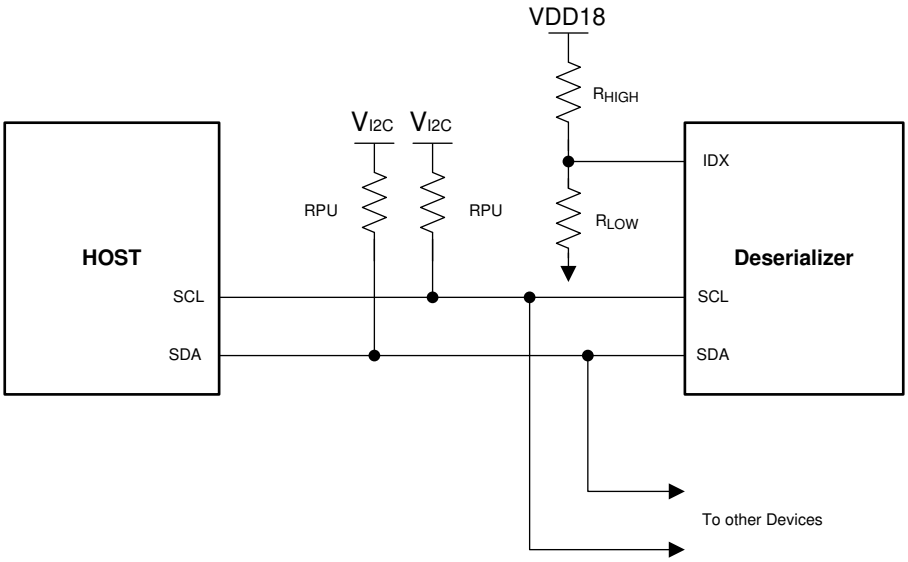

Figure 5-21. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pullup resistor to V_{I2C}, **where V_{I2C} is a voltage rail that matches the voltage applied to VDDIO**. The pull-up resistor value can be adjusted to account for capacitive loading and data rate requirements. Refer to "I2C Bus Pullup Resistor Calculation" (SLVA689) to determine the pull-up resistor value to V_{I2C}. The signals are either pulled High, or driven Low.

The IDX pin configures the control interface to one of eight possible device addresses. A pullup resistor and a pulldown resistor can be used to set the appropriate voltage ratio between the IDX input pin (V_{IDX}) and $V_{(VDD18)}$, each ratio corresponding to a specific device address. See Table 5-13, Serial Control Bus Addresses for IDX.

Table 5-13. Serial Control Bus Addresses for IDX

NO.	V_{IDX} VOLTAGE RANGE			V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		PRIMARY ASSIGNED I2C ADDRESS	
	V_{MIN}	V_{TYP}	V_{MAX}	VDD18 = 1.80 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	7-BIT	8-BIT
0	0	0	0.131 × $V_{(VDD18)}$	0	OPEN	10.0	0x30	0x60
1	0.179 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.374	88.7	23.2	0x32	0x64
2	0.296 × $V_{(VDD18)}$	0.330 × $V_{(VDD18)}$	0.362 × $V_{(VDD18)}$	0.582	75.0	35.7	0x34	0x68
3	0.412 × $V_{(VDD18)}$	0.443 × $V_{(VDD18)}$	0.474 × $V_{(VDD18)}$	0.792	71.5	56.2	0x36	0x6C
4	0.525 × $V_{(VDD18)}$	0.559 × $V_{(VDD18)}$	0.592 × $V_{(VDD18)}$	0.995	78.7	97.6	0x38	0x70
5	0.642 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.704 × $V_{(VDD18)}$	1.202	39.2	78.7	0x3A	0x74
6	0.761 × $V_{(VDD18)}$	0.792 × $V_{(VDD18)}$	0.823 × $V_{(VDD18)}$	1.420	25.5	95.3	0x3C	0x78
7	0.876 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	0x3D	0x7A

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SDA transitions Low while SCL is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See Figure 5-22.

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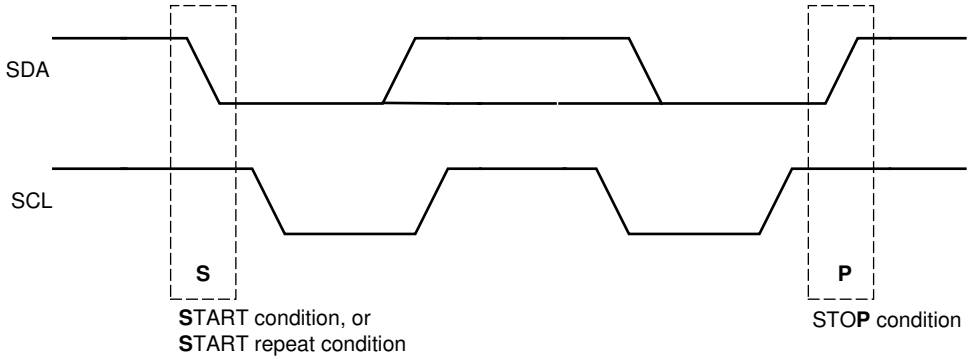

Figure 5-22. START and STOP Conditions

To communicate with a remote device, the host controller sends the target address and listens for a response from the target. This response is referred to as an acknowledge bit (ACK). If a target on the bus is addressed correctly, the target acknowledges (ACKs) the controller by driving the SDA bus low. If the address does not match one of the target addresses of the device, the target not-acknowledges (NACKs) the controller by letting SDA be pulled High. ACKs can also occur on the bus when data transmissions are in process. When the controller is writing data, the target ACKs after every data byte is successfully received. When the controller is reading data, the controller ACKs after every data byte is received to let the target know the controller wants to receive another data byte. When the controller wants to stop reading, the controller NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 5-23 and a WRITE is shown in Figure 5-24.

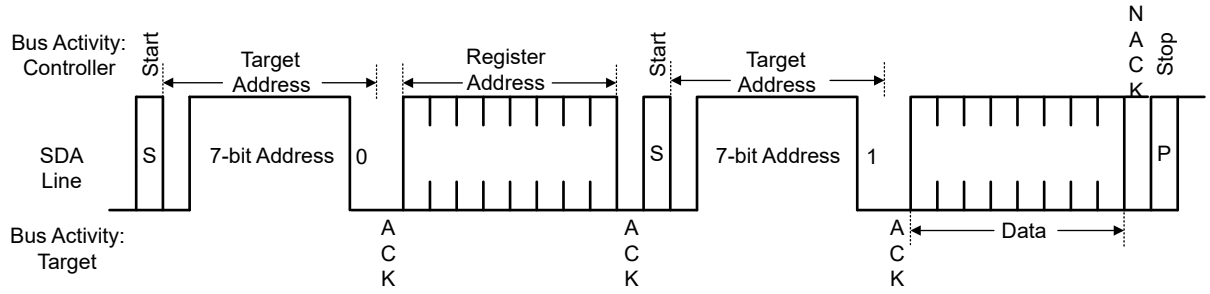

Figure 5-23. Serial Control Bus — READ

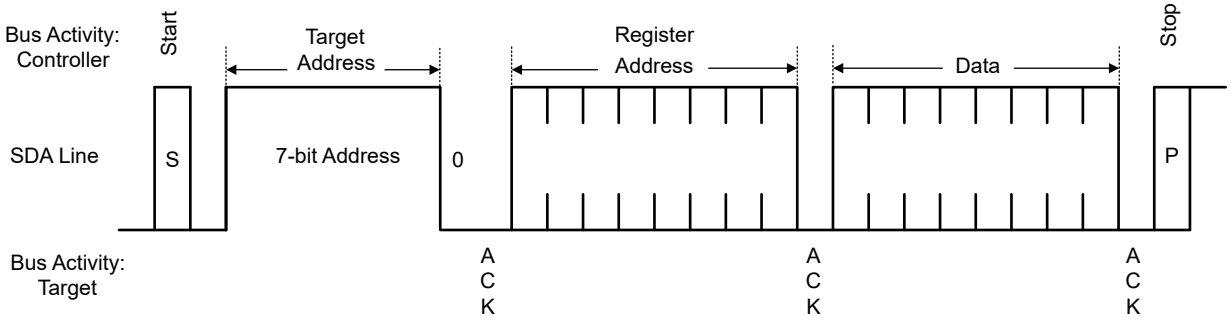

Figure 5-24. Serial Control Bus — WRITE

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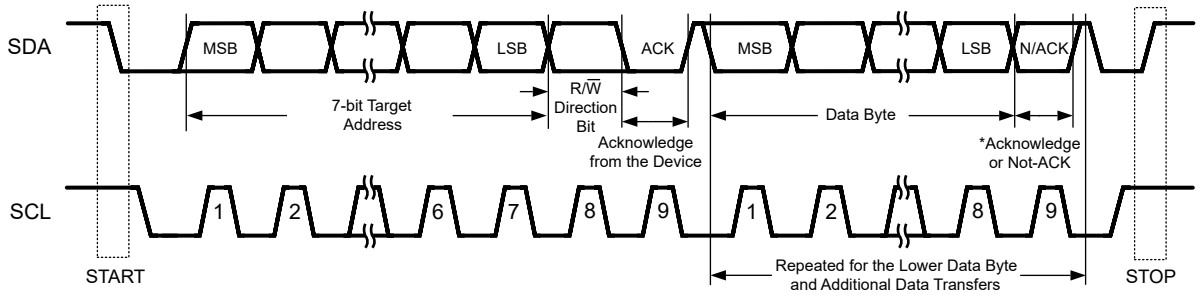

Figure 5-25. Basic Operation

The I2C Controller located at the Deserializer must support I2C clock stretching. For more information on I2C interface requirements and throughput considerations, refer to *I2C Communication Over FPD-Link III With Bidirectional Control Channel* (SNLA131) and *I2C over DS90UB913/4 FPD-Link III With Bidirectional Control Channel* (SNLA222).

5.5.2 Second I2C Port

The DS90UB964-Q1 includes a second I2C port that allows bidirectional control channel access to both local registers and remote devices. Remote device access is configured on BCCx_MAP register 0x0C[7:4].

The second I2C port uses the same I2C address as the primary I2C port. In addition, RX Port I2C IDs are also available for the second I2C port.

In general, TI recommends that the second I2C port be used in cases where the CSI-2 TX ports are connected to separate processors. The second I2C port allows independent control of the DS90UB964-Q1 as well as remote devices by the second processor. However, Register 0x01 (RESET_CTL) can only be written by the primary I2C port.

5.5.3 I2C Target Operation

The DS90UB964-Q1 implements an I2C target capable of operation supporting the Standard, Fast, and Fast-plus modes of operation allowing I2C operation at up to 1MHz clock frequencies. Local I2C transactions to access DS90UB964-Q1 registers can be conducted 2ms after power supplies are stable and PDB is brought high. For accesses to local registers, the I2C Target operates without stretching the clock. The primary I2C target address is set through the IDx pin. The primary I2C target address is stored in the I2C Device ID register at address 0x0. In addition to the primary I2C target address, the DS90UB964-Q1 can be programmed to respond to up to four other I2C addresses (reg 0xF8-0xFB). The four RX Port ID addresses provide direct access to the Receive Port registers without the need to set the paging controls normally required to access the port registers.

5.5.4 Remote Target Operation

The bidirectional control channel provides a mechanism to read or write I2C registers in remote devices over the FPD-Link III interface. The I2C Controller located at the Deserializer must support I2C clock stretching. Accesses to serializer or remote target devices over the bidirectional control channel results in clock stretching to allow for response time across the link. The DS90UB964-Q1 acts as an I2C target on the local bus, forwards read and write requests to the remote device, and returns the response from the remote device to the local I2C bus. To allow for the propagation and regeneration of the I2C transaction at the remote device, the DS90UB964-Q1 stretches the I2C clock while waiting for the remote response. The I2C address of the currently selected RX Port serializer is populated in register 0x5B of the DS90UB964-Q1. The BCC_CONFIG register 0x58 also must have bit 6, I2C_PASS_THROUGH set to one. If enabled, local I2C transactions with valid address decode is then forwarded through the bidirectional control channel to the remote I2C bus. When I2C_PASS_THROUGH is set, the deserializer only propagates messages that the deserializer recognizes, such as the registered serializer alias address (SER_ALIAS_ID), or any registered remote target alias attached to the serializer I2C bus (TARGET_ALIAS) assigned to the specific Rx Port. Setting I2C_PASS_THROUGH_ALL and AUTO_ACK_ALL are less common use cases and primarily used for debugging I2C messaging as these settings respectively pass all addresses regardless of valid I2C address (I2C_PASS_THROUGH_ALL) and acknowledge all I2C commands without waiting for a response from serializer (AUTO_ACK_ALL).

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5.5.5 Remote Target Addressing

Various system use cases require multiple sensor devices with the same fixed I2C target address to be remotely accessible from the same I2C bus at the deserializer. The DS90UB964-Q1 provides TargetID virtual addressing to differentiate target addresses when connecting two or more remote devices. Eight pairs of TargetAlias and TargetID registers are allocated for each FPD-Link III Receive port in registers 0x5D through 0x6C. The TargetAlias register allows programming a virtual address which the host controller uses to access the remote device. The TargetID register provides the actual target address for the device on the remote I2C bus. The write enable bit in register 0x4C must be set before configuring the TargetAlias and TargetID for each selected RX Port. Eight pairs of registers are available for each port (total of 32 pairs), so multiple devices can be directly accessible remotely without the need for reprogramming. Multiple TargetAlias can be assigned to the same TargetID as well.

5.5.6 Broadcast Write to Remote Devices

The DS90UB964-Q1 provides a mechanism to broadcast I2C writes to remote devices (either remote targets or serializers). For each Receive port, the TargetID/Alias register pairs can be programmed with the same TargetAlias value so each device responds to the same local I2C command. The TargetID value must match the intended remote device address. The SER_ALIAS_ID at each receive port can also be set with the same Alias value to send a broadcast write to each connected remote serializer. Before setting the register values for the TargetID/Alias or SER_ID/SER_ALIAS_ID, RX_WRITE_PORT_x in register 0x4C must be set to select one or more receive ports to be configured for the ID/Alias values. When performing broadcast writes, the ACK and other return data from the I2C transaction comes from only one of the Target devices included in the broadcast write. The receive port selected in RX_READ_PORT in register 0x4C determines the source of the return I2C transaction on the local bus.

5.5.6.1 Code Example for Broadcast Write

```
#  "FPD3_PORT_SEL Broadcast RX0/1/2/3"
WriteI2C(0x4c,0x0f) # RX_PORT0 read; RX0/1/2/3 write
#  "Enable I2C Pass Through"
WriteI2C(0x58,0x58) # enable I2C pass through
WriteI2C(0x5c,0x18) # "SER_ALIAS_ID"
WriteI2C(0x5d,0x60) # "TargetID[0]"
WriteI2C(0x65,0x60) # "TargetAlias[0]"
```

5.5.7 I2C Proxy Controller

The DS90UB964-Q1 implements an I2C controller that acts as a proxy controller to regenerate I2C accesses originating from a remote serializer. By default, the I2C Controller Enable bit (I2C_CONTROLLER_EN) is set to 0 in register 0x02[5] to block Controller access to local deserializer I2C from remote serializers. Set I2C_CONTROLLER_EN = 1 if there is a remote controller device located on the I2C bus of any of the connected serializers that sends remote I2C commands to the deserializer. The proxy controller is an I2C-compatible controller capable of operating with Standard-mode, Fast-mode, or Fast-mode Plus I2C timing. The proxy controller is also capable of arbitration with other controllers, allowing multiple controllers and targets to exist on the I2C bus. A separate I2C proxy controller is implemented for each Receive port. This allows independent operation for all sources to the I2C interface. Arbitration between multiple sources is handled automatically using I2C multi-controller arbitration.

5.5.8 I2C Proxy Controller Timing

The proxy controller timing parameters are based on the REFCLK timing. Timing accuracy for the I2C proxy controller based on the REFCLK clock source attached to the DS90UB964-Q1 deserializer. The I2C Controller regenerates the I2C read or write access using timing controls in the registers 0xA and 0xB to regenerate the clock and data signals to meet the desired I2C timing in Standard, Fast, or Fast-mode Plus modes of operation.

I2C Controller SCL High Time is set in register 0xA[7:0]. This field configures the high pulse width of the SCL output when the Serializer is the controller on the local deserializer I2C bus. The default value is set to provide a minimum 5µs SCL high time with the reference clock at 25MHz + 100ppm including four additional oscillator

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clock periods or synchronization and response time. Units are 40ns for the nominal oscillator clock frequency, giving Min_delay = 40ns × (SCL_HIGH_TIME + 5).

I2C Controller SCL Low Time is set in register 0xB[7:0]. This field configures the low pulse width of the SCL output when the Serializer is the Controller on the local deserializer I2C bus. This value is also used as the SDA setup time by the I2C Target for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. The default value is set to provide a minimum 5µs SCL low time with the reference clock at 25MHz + 100ppm including four additional oscillator clock periods or synchronization and response time. Units are 40ns for the nominal oscillator clock frequency, giving Min_delay = 40ns × (SCL_LOW_TIME + 5). See Table 5-14 example settings for Standard mode, Fast mode and Fast-mode Plus timing.

Table 5-14. Typical I2C Timing Register Settings

I2C MODE	SCL HIGH TIME		SCL LOW TIME	
	0xA[7:0]	NOMINAL DELAY AT REFCLK = 25MHz	0xB[7:0]	NOMINAL DELAY AT REFCLK = 25MHz
Standard	0x7A	5.04µs	0x7A	5.04µs
Fast	0x13	0.920µs	0x25	1.64µs
Fast - Plus	0x06	0.400µs	0x0C	0.640µs

5.5.8.1 Code Example for Configuring Fast-Mode Plus I2C Operation

```
#  "RX0 I2C Controller Fast Plus Configuration"
WriteI2C(0x02,0x3E) # Enable Proxy
WriteI2C(0x4c,0x01) # Select RX_PORT0
# Set SCL High and Low Time delays
WriteI2C(0x0a,0x06) # SCL High
WriteI2C(0x0b,0x0C) # SCL Low
```

5.5.9 Interrupt Support

Interrupts can be brought out on the INTB pin as controlled by the INTERRUPT_CTL 0x23 and INTERRUPT_STS 0x24 registers. The main interrupt control registers provide control and status for interrupts from the individual sources. Sources include each of the four FPD3 Receive ports as well as CSI-2 Transmit ports. Clearing interrupt conditions requires reading the associated status register for the source. The setting of the individual interrupt status bits is not dependent on the related interrupt enable controls. The interrupt enable controls whether an interrupt is generated based on the condition, but does not prevent the interrupt status assertion.

For an interrupt to be generated based on one of the interrupt status assertions, both the individual interrupt enable and the INT_EN control must be set in the INTERRUPT_CTL 0x23 register. For example, to generate an interrupt if IS_RX0 is set, both the IE_RX0 and INT_EN bits must be set. If IE_RX0 is set but INT_EN is not, the INT status is indicated in the INTERRUPT_STS register, and the INTB pin does not indicate the interrupt condition.

See the INTERRUPT_CTL and INTERRUPT_STS register for details.

5.5.9.1 Code Example to Enable Interrupts

```
#  "RX01/2/3/4 INTERRUPT_CTL enable"
WriteI2C(0x23,0xBF) # RX all & INTB PIN EN
# Individual RX01/2/3/4 INTERRUPT_CTL enable
# "RX0 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x23,0x81) # RX0 & INTB PIN EN
# "RX1 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x23,0x82) # RX1 & INTB PIN EN
# "RX2 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0x23,0x84) # RX2 & INTB PIN EN
# "RX3 INTERRUPT_CTL enable"
```

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```
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0x23,0x88) # RX3 & INTB PIN EN
```

5.5.9.2 FPD-Link III Receive Port Interrupts

For each FPD-Link III Receive port, multiple options are available for generating interrupts. Interrupt generation is controlled through the PORT_ICR_HI 0xD8 and PORT_ICcR_LO 0xD9 registers. In addition, the PORT_ISR_HI 0xDA and PORT_ISR_LO 0xDB registers provide read-only status for the interrupts. Clearing of interrupt conditions is handled by reading the RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS registers. The status bits in the PORT_ISR_HI/LO registers are copies of the associated bits in the main status registers.

To enable interrupts from one of the Receive port interrupt sources:

1. Enable the interrupt source by setting the appropriate interrupt enable bit in the PORT_ICR_HI or PORT_ICR_LO register
2. Set the RX Port X Interrupt control bit (IE_RXx) in the INTERRUPT_CTL register
3. Set the INT_EN bit in the INTERRUPT_CTL register to allow the interrupt to assert the INTB pin low

To clear interrupts from one of the Receive port interrupt sources:

1. (optional) Read the INTERRUPT_STS register to determine which RX Port caused the interrupt
2. (optional) Read the PORT_ISR_HI and PORT_ISR_LO registers to determine source of interrupt
3. Read the appropriate RX_PORT_STS1, RX_PORT_STS2, or CSI_RX_STS register to clear the interrupt.

The first two steps are optional. The interrupt can be determined and cleared by just reading the status registers.

5.5.9.3 Code Example to Readback Interrupts

```
INTERRUPT_STS = ReadI2C(0x24) # 0x24 INTERRUPT_STS
if ((INTERRUPT_STS & 0x80) >> 7):
    print "# GLOBAL INTERRUPT DETECTED "
if ((INTERRUPT_STS & 0x40) >> 6):
    print "# RESERVED "
if ((INTERRUPT_STS & 0x20) >> 5):
    print "# IS_CSI_TX1 DETECTED "
if ((INTERRUPT_STS & 0x10) >> 4):
    print "# IS_CSI_TX0 DETECTED "
if ((INTERRUPT_STS & 0x08) >> 3):
    print "# IS_RX3 DETECTED "
if ((INTERRUPT_STS & 0x04) >> 2):
    print "# IS_RX2 DETECTED "
if ((INTERRUPT_STS & 0x02) >> 1):
    print "# IS_RX1 DETECTED "
if ((INTERRUPT_STS & 0x01) ):
    print "# IS_RX0 DETECTED "
# "################################################"
#  "RX0 status"
# "################################################"
WriteReg(0x4C,0x01) # RX0
PORT_ISR_LO = ReadI2C(0xDB)
print "0xDB PORT_ISR_LO : ", hex(PORT_ISR_LO) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED " # Forward Channel parity errors exceed set threshold
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "    # RX Port PASS status has changed since last read
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "     # RX Port LOCK status has changed since last read
################################################
PORT_ISR_HI = ReadI2C(0xDA)
print "0xDA PORT_ISR_HI : ", hex(PORT_ISR_HI) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
```


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```
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "
################################################
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR
if (  (RX_PORT_STS1 & 0xc0) >> 6) == 3:
    print "# RX_PORT_NUM = RX3"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 2:
    print "# RX_PORT_NUM = RX2"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED " # Cleared when RX_PAR_ERR_HI/LO registers are cleared
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "            # Shows current PASS status at RX Port
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "             # Shows current LOCK status at RX Port
################################################
RX_PORT_STS2 = ReadI2C(0x4E)
if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "       # Clears when CSI_RX_STS register is cleared
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "
################################################
# "################################################"
#  "RX1 status"
# "################################################"
WriteReg(0x4C,0x12) # RX1
PORT_ISR_LO = ReadI2C(0xDB) # PORT_ISR_LO readout; cleared by RX_PORT_STS2
if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED " # Forward Channel parity errors exceed set threshold
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "    # RX Port PASS status has changed since last read
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "     # RX Port LOCK status has changed since last read
################################################
PORT_ISR_HI = ReadI2C(0xDA) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "
################################################
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR
if (  (RX_PORT_STS1 & 0xc0) >> 6) == 3:
    print "# RX_PORT_NUM = RX3"
```

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```
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 2:
    print "# RX_PORT_NUM = RX2"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED " # Cleared when RX_PAR_ERR_HI/LO registers are cleared
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "           # Shows current PASS status at RX Port
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "            # Shows current LOCK status at RX Port
################################################
RX_PORT_STS2 = ReadI2C(0x4E)
if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "      # Clears when CSI_RX_STS register is cleared
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "
################################################
# "################################################"
#  "RX2 status"
# "################################################"
WriteReg(0x4C,0x24) # RX2
PORT_ISR_LO = ReadI2C(0xDB) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED " # Forward Channel parity errors exceed set threshold
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "    # RX Port PASS status has changed since last read
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "     # RX Port LOCK status has changed since last read
################################################
PORT_ISR_HI = ReadI2C(0xDA) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "
################################################
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR
if (  (RX_PORT_STS1 & 0xc0) >> 6) == 3:
    print "# RX_PORT_NUM = RX3"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 2:
    print "# RX_PORT_NUM = RX2"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"
```


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```
if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "  # Cleared when RX_PAR_ERR_HI/LO registers are cleared
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "            # Shows current PASS status at RX Port
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "             # Shows current LOCK status at RX Port
################################################
RX_PORT_STS2 = ReadI2C(0x4E)
if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "       # Clears when CSI_RX_STS register is cleared
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "

################################################
# "################################################"
#  "RX3 status"
# "################################################"
WriteReg(0x4C,0x38) # RX3
PORT_ISR_LO = ReadI2C(0xDB) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "  # Forward Channel parity errors exceed set threshold
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "     # RX Port PASS status has changed since last read
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "      # RX Port LOCK status has changed since last read
################################################
PORT_ISR_HI = ReadI2C(0xDA) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "
################################################
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR
if (  (RX_PORT_STS1 & 0xc0) >> 6) == 3:
    print "# RX_PORT_NUM = RX3"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 2:
    print "# RX_PORT_NUM = RX2"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
```

```
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "  # Cleared when RX_PAR_ERR_HI/LO registers are cleared
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "            # Shows current PASS status at RX Port
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "             # Shows current LOCK status at RX Port
##############################################
RX_PORT_STS2 = ReadI2C(0x4E)
if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "       # Clears when CSI_RX_STS register is cleared
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "
##############################################
```

5.5.9.4 CSI-2 Transmit Port Interrupts

The following interrupts are available for each CSI-2 Transmit Port:

- Pass indication
- Synchronized status
- Deassertion of Pass indication for an input port assigned to the CSI-2 TX Port
- Loss of Synchronization between input video streams
- RX Port Interrupt – interrupts from RX Ports mapped to this CSI-2 Transmit port

See the CSI_TX_ICR address 0x36 and CSI_TX_ISR address 0x37 registers for details.

The setting of the individual interrupt status bits is not dependent on the related interrupt enable controls. The interrupt enable controls whether an interrupt is generated based on the condition, but the enable does not prevent the interrupt status assertion.

5.5.10 Timestamp – Video Skew Detection

The DS90UB964-Q1 implements logic to detect skew between video signaling from attached sensors. For each input port, the DS90UB964-Q1 provides the ability to capture a time-stamp for both a start-of-frame and start-of-line event. Comparison of timestamps can provide information on the relative skew between the ports. Start-of-frame timestamps are generated at the active edge of the Vertical Sync signal in Raw mode. Start-of-line timestamps are generated at the start of reception of the Nth line of video data after the Start of Frame for either mode of operation. The function does not use the Line Start (LS) packet or Horizontal Sync controls to determine the start of lines.

The skew detection can run in either a FrameSync mode or free-run mode.

Skew detection can be individually enabled for each RX port.

For start-of-line timestamps, a line number must be programmed. The same line number is used for all 4 channels. Prior to reading timestamps, the TS_FREEZE bit for each port that is read must be set. This prevents overwrite of the timestamps by the detection circuit until all timestamps have been read. The freeze condition is released automatically once all frozen timestamps have been read. The freeze bits can also be cleared if the bits do not read all the timestamp values.

The TS_STATUS register includes the following:

- Flags to indicate multiple start-of-frame per FrameSync period
- Flag to indicate Timestamps Ready

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- Flags to indicate Timestamps valid (per port) – if ports are not synchronized, all ports do not indicate valid timestamps

The Timestamp Ready flag is cleared when the TS_FREEZE bit is cleared.

5.5.11 Pattern Generation

The deserializer supports internal pattern generation feature to provide a simple way to generate video test patterns for the CSI-2 transmitter outputs. CSI-2 port 0 and port 1 each have their own pattern generator. Two types of patterns are supported: Reference Color Bar pattern and Fixed Color patterns and accessed by the Pattern Generator page 0 in the indirect register set.

Prior to enabling the Packet Generator, the following is done:

1. Set the TX_WRITE_PORT bit in CSI_PORT_SEL (reg 0x32).
2. Disable video forwarding by configuring bits [7:4] of the FWD_CTL1 register.
3. Configure CSI-2 Transmitter operating speed using the CSI_PLL_CTL register.
4. Enable the CSI-2 Transmitter using the CSI_CTL register.

5.5.11.1 Reference Color Bar Pattern

The Reference Color Bar Patterns are based on the pattern defined in Appendix D of the mipi_CTS_for_D-PHY_v1-1_r03 specification. The pattern is an eight color bar pattern designed to provide high, low, and medium frequency outputs on the CSI-2 transmit data lanes.

The CSI-2 Reference pattern provides eight color bars by default with the following byte data for the color bars: X bytes of 0xAA (high-frequency pattern, inverted) X bytes of 0x33 (mid-frequency pattern) X bytes of 0xF0 (low-frequency pattern, inverted) X bytes of 0x7F (lone 0 pattern) X bytes of 0x55 (high-frequency pattern) X bytes of 0xCC (mid-frequency pattern, inverted) X bytes of 0x0F (low-frequency pattern) Y bytes of 0x80 (lone 1 pattern) In most cases, Y is the same as X. For certain data types, the last color bar can be larger than the others to properly fill the video line dimensions.

The Pattern Generator is programmable with the following options:

- Number of color bars (1, 2, 4, or 8)
- Number of bytes per line
- Number of bytes per color bar
- CSI-2 DataType field and VC-ID
- Number of active video lines per frame
- Number of total lines per frame (active plus blanking)
- Line period (program in units of 10ns depending on CSI-2 rate)
- Vertical front porch – number of blank lines prior to FrameEnd packet
- Vertical back porch – number of blank lines following FrameStart packet

The pattern generator relies on proper programming by software to make sure the color bar widths are set to multiples of the block (or word) size required for the specified DataType. For example, for RGB888, the block size is 3 bytes which also matches the pixel size. In this case, the number of bytes per color bar must be a multiple of 3. The Pattern Generator is implemented in the CSI-2 Transmit clock domain, providing the pattern directly to the CSI-2 Transmitter. The circuit generates the CSI-2 formatted data.

5.5.11.2 Fixed Color Patterns

When programmed for Fixed Color Pattern mode, Pattern Generator can generate a video image with a programmable fixed data pattern. The basic programming fields for image dimensions are the same as used with the Color Bar Patterns. When sending Fixed Color Patterns, the color bar controls allow alternating between the fixed pattern data and the bit-wise inverse of the fixed pattern data.

The Fixed Color patterns assume a fixed block size for the byte pattern to be sent. The block size is programmable through the register and is designed to support most 8-bit, 10-bit, and 12-bit pixel formats. The block size can be set based on the pixel size converted to blocks that are an integer multiple of bytes. For example, a 2x12-bit pixel image requires a 3-byte block size, while a 3x12-bit pixel image requires nine bytes (two pixels) to send an integer number of bytes. Sending a RAW10 pattern typically requires a 5-byte block size

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for four pixels, so 1x10-bit and 2x10-bit can both be sent with a 5-byte block size. For 3x10-bit, a 15-byte block size is required.

The Fixed Color patterns support block sizes up to 16 bytes in length, allowing additional options for patterns in some conditions. For example, an alternating black and white YUV 422 8-bit image can be sent with a block size of 2-bytes and setting the first byte to 0xFF and the next byte to 0x00.

To support up to 16-byte block sizes, a set of sixteen registers are implemented to allow programming the value for each data byte. The line period is calculated in units of 10ns, unless the CSI-2 mode is set to 400Mbps operation in which case the unit time dependency is 20ns.

5.5.11.3 Pattern Generator Programming

The information in this section provides details on how to program the Pattern Generator to provide a specific color bar pattern, based on data type, frame size, and line size.

Most basic configuration information is determined directly from the expected video frame parameters. The requirements include the data type, frame rate (frames per second), number of active lines per frame, number of total lines per frame (active plus blanking), and number of pixels per line.

- PGEN_ACT_LPF – Number of active lines per frame
- PGEN_TOT_LPF – Number of total lines per frame
- PGEN_LSIZE – Video line length size in bytes. Compute based on pixels per line multiplied by pixel size in bytes
- CSI-2 DataType field and VC-ID
- Optional: PGEN_VBP – Vertical back porch. This is the number of lines of vertical blanking following Frame Valid
- Optional: PGEN_VFP – Vertical front porch. This is the number of lines of vertical blanking preceding Frame Valid
- PGEN_LINE_PD – Line period in 10-ns units. Compute based on Frame Rate and total lines per frame
- PGEN_BAR_SIZE – Color bar size in bytes. Compute based on datatype and line length in bytes (see details below)

5.5.11.3.1 Determining Color Bar Size

The color bar pattern can be programmed in units of a block or word size dependent on the datatype of the video being sent. The sizes are defined in the MIPI CSI-2 specification. For example, RAW10 requires a 5-byte block size which is equal to 4 pixels. RAW12 requires a 3-byte block size which is equal to 2 pixels.

When programming the Pattern Generator, software can compute the required bar size in bytes based on the line size and the number of bars. For the standard eight color bar pattern, that requires the following algorithm:

- Select the desired data type, and a valid length for that data type (in pixels).
- Convert pixels/line to blocks/line (by dividing by the number of pixels/block, as defined in the data type specification).
- Divide the blocks/line result by the number of color bars (8), giving blocks/bar
- Round result down to the nearest integer
- Convert blocks/bar to bytes/bar and program that value into the PGEN_BAR_SIZE register

As an alternative, the blocks/line can be computed by converting pixels/line to bytes/line and divide by bytes/block.

5.5.11.4 Code Example for Pattern Generator

Follow the example here to configure a 1280x720 pattern with 30 fps rate, RAW10 data type, and reference color bar. The user can also use the Analog LaunchPad GUI to configure the PatGen register settings based on their desired parameters.

```
#Patgen Fixed Colorbar 1280x720p30
WriteI2C(0x33,0x01) # CSI0 enable
WriteI2C(0xB0,0x00) # Indirect Pattern Gen Registers
```


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```
WriteI2C(0xB1,0x01) # PGEN_CTL
WriteI2C(0xB2,0x01)
WriteI2C(0xB1,0x02) # PGEN_CFG
WriteI2C(0xB2,0x35)
WriteI2C(0xB1,0x03) # PGEN_CSI_DI
WriteI2C(0xB2,0x2B)
WriteI2C(0xB1,0x04) # PGEN_LINE_SIZE1
WriteI2C(0xB2,0x06)
WriteI2C(0xB1,0x05) # PGEN_LINE_SIZE0
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0x06) # PGEN_BAR_SIZE1
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x07) # PGEN_BAR_SIZE0
WriteI2C(0xB2,0xC8)
WriteI2C(0xB1,0x08) # PGEN_ACT_LPF1
WriteI2C(0xB2,0x02)
WriteI2C(0xB1,0x09) # PGEN_ACT_LPF0
WriteI2C(0xB2,0xD0)
WriteI2C(0xB1,0x0A) # PGEN_TOT_LPF1
WriteI2C(0xB2,0x02)
WriteI2C(0xB1,0x0B) # PGEN_TOT_LPF0
WriteI2C(0xB2,0xEE)
WriteI2C(0xB1,0x0C) # PGEN_LINE_PD1
WriteI2C(0xB2,0x11)
WriteI2C(0xB1,0x0D) # PGEN_LINE_PD0
WriteI2C(0xB2,0x5C)
WriteI2C(0xB1,0x0E) # PGEN_VBP
WriteI2C(0xB2,0x14)
WriteI2C(0xB1,0x0F) # PGEN_VFP
WriteI2C(0xB2,0x08)
```

5.5.12 FPD-Link BIST Mode

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high-speed serial link and the back channel without external data connections. The BIST mode is enabled by programming the BIST configuration register. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

When BIST is activated, the DS90UB964-Q1 sends register writes to the Serializer through the Back Channel. The control channel register writes configure the Serializer for BIST mode operation. The serializer outputs a continuous stream of a pseudo-random sequence and drives the link at speed. The deserializer detects the test pattern and monitors the pattern for errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The CMLOUT output function is also available during BIST mode. While the lock indications are required to identify the beginning of proper data reception, for any link failures or data corruption, the best indication is the contents of the error counter in the BIST_ERR_COUNT register 0x57 for each RX port. The test can select whether the Serializer uses an external or internal clock as reference for the BIST pattern frequency.

5.5.12.1 BIST Operation

The FPD-Link III BIST is configured and enabled by programming the BIST Control register. Set 0xB3 = 0x01 to enable BIST and set 0xB3 = 00 to disable BIST. BIST pass or fail status can be brought to GPIO pins by selecting the Pass indication for each receive port using the GPIOx_PIN_CTL registers. The Pass/Fail status is de-asserted low for each data error detected on the selected port input data. In addition, the Receiver Lock status for selected ports can be brought out to the GPIO pins as well. After completion of BIST, the BIST Error Counter can be read to determine if errors occurred during the test. If the DS90UB964-Q1 failed to lock to the input signal or lost lock to the input signal, the BIST Error Counter indicates 0xFF. The maximum normal count value is 0xFE. The SER_BIST_ACT register bit 0xD0[5] can be monitored during testing to make sure BIST is activated in the serializer.

During BIST, DS90UB964-Q1 output activity are gated by BIST_Control[7:6] (BIST_OUT_MODE[1:0]) as follows:

00 : Outputs disabled during BIST

10 : Outputs enabled during BIST

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When enabling the outputs by setting BIST_OUT_MODE = 10, the CSI-2 is inactive by default (LP11 state). To exercise the CSI-2 interface during BIST mode, the Pattern Generator can be enabled to send a video data pattern on the CSI-2 outputs.

The BIST clock frequency is controlled by the BIST_CLOCK_SOURCE field in the BIST Control register. This 2-bit value is written to the Serializer register 0x14[2:1]. A value of 00 selects an external clock. A non-zero value enables an internal clock of the frequency defined in the Serializer register 0x14. The BIST_CLOCK_SOURCE field is sampled at the start of BIST. Changing this value after BIST is enabled does not change operation.

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5.6 Register Maps

The DS90UB964-Q1 implements the following register blocks, accessible through I2C as well as the bidirectional control channel:

- Main Registers
- FPD3 RX Port Registers (separate register block for each of the four RX ports)
- CSI-2 Port Registers (separate register block for each of the CSI-2 ports)

Table 5-15. Main Register Map Descriptions

ADDRESS RANGE	DESCRIPTION	ADDRESS MAP			
0x00-0x32	Digital Registers	Shared			
0x33-0x3A	Digital CSI-2 Registers (paged, broadcast write allowed)	CSI-2 TX Port 0 *R: 0x32[4]=0* *W: 0x32[0]=1*		CSI-2 TX Port 1 *R: 0x32[4]=1* *W: 0x32[1]=1*	
0x3B-0x3F	Reserved Registers	Reserved			
0x40-0x45	AEQ Registers	Shared			
0x46-0x7D	Digital RX Port Registers (paged, broadcast write allowed)	FPD3 RX Port 0 *R: 0x4C[5:4]=00* *W: 0x4C[0]=1*	FPD3 RX Port 1 *R: 0x4C[5:4]=01* *W: 0x4C[1]=1*	FPD3 RX Port 2 *R: 0x4C[5:4]=10* *W: 0x4C[2]=1*	FPD3 RX Port 3 *R: 0x4C[5:4]=11* *W: 0x4C[3]=1*
0x7E-0xAF	Reserved Registers	Reserved			
0xB0-0xB2	Indirect Access Registers	Shared			
0xB3-0xBE	Digital Registers	Shared			
0xBF-0xCF	Reserved Registers	Reserved			
0xD0-0xDB	Digital RX Port Debug Registers	FPD3 RX Port 0 *R: 0x4C[5:4]=00* *W: 0x4C[0]=1*	FPD3 RX Port 1 *R: 0x4C[5:4]=01* *W: 0x4C[1]=1*	FPD3 RX Port 2 *R: 0x4C[5:4]=10* *W: 0x4C[2]=1*	FPD3 RX Port 3 *R: 0x4C[5:4]=11* *W: 0x4C[3]=1*
0xDC-0xEF	Reserved Registers	Reserved			
0xF0-0xF5	FPD3 RX ID Registers	Shared			
0xF6-0xF7	Reserved Registers	Reserved			
0xF8-0xFB	Port I2C Addressing	Shared			
0xFC-0xFF	Reserved Registers	Reserved			

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5.6.1 Main_Page Registers

Table 5-16 lists the memory-mapped registers for the Main_Page registers. All register offset addresses not listed in Table 5-16 should be considered as reserved locations and the register contents should not be modified.

Table 5-16. MAIN_PAGE Registers

Address	Acronym	Register Name	Section
0x0	I2C_DEVICE_ID	I2C_DEVICE_ID	Go
0x1	RESET_CTL	RESET_CTL	Go
0x2	GENERAL_CFG	GENERAL_CFG	Go
0x3	REV_MASK_ID	REV_MASK_ID	Go
0x4	DEVICE_STS	DEVICE_STS	Go
0x5	PAR_ERR_THOLD1	PAR_ERR_THOLD1	Go
0x6	PAR_ERR_THOLD0	PAR_ERR_THOLD0	Go
0x7	BCC_WATCHDOG_CONTROL	BCC_WATCHDOG_CONTROL	Go
0x8	I2C_CONTROL_1	I2C_CONTROL_1	Go
0x9	I2C_CONTROL_2	I2C_CONTROL_2	Go
0xA	SCL_HIGH_TIME	SCL_HIGH_TIME	Go
0xB	SCL_LOW_TIME	SCL_LOW_TIME	Go
0xC	RX_PORT_CTL	RX_PORT_CTL	Go
0xD	IO_CTL	IO_CTL	Go
0xE	GPIO_PIN_STS	GPIO_PIN_STS	Go
0xF	GPIO_INPUT_CTL	GPIO_INPUT_CTL	Go
0x10	GPIO0_PIN_CTL	GPIO0_PIN_CTL	Go
0x11	GPIO1_PIN_CTL	GPIO1_PIN_CTL	Go
0x12	GPIO2_PIN_CTL	GPIO2_PIN_CTL	Go
0x13	GPIO3_PIN_CTL	GPIO3_PIN_CTL	Go
0x14	GPIO4_PIN_CTL	GPIO4_PIN_CTL	Go
0x15	GPIO5_PIN_CTL	GPIO5_PIN_CTL	Go
0x16	GPIO6_PIN_CTL	GPIO6_PIN_CTL	Go
0x17	GPIO7_PIN_CTL	GPIO7_PIN_CTL	Go
0x18	FS_CTL	FS_CTL	Go
0x19	FS_HIGH_TIME_1	FS_HIGH_TIME_1	Go
0x1A	FS_HIGH_TIME_0	FS_HIGH_TIME_0	Go
0x1B	FS_LOW_TIME_1	FS_LOW_TIME_1	Go
0x1C	FS_LOW_TIME_0	FS_LOW_TIME_0	Go
0x1D	MAX_FRM_HI	MAX_FRM_HI	Go
0x1E	MAX_FRM_LO	MAX_FRM_LO	Go
0x1F	CSI_PLL_CTL	CSI_PLL_CTL	Go
0x20	FWD_CTL1	FWD_CTL1	Go
0x21	FWD_CTL2	FWD_CTL2	Go
0x22	FWD_STS	FWD_STS	Go
0x23	INTERRUPT_CTL	INTERRUPT_CTL	Go
0x24	INTERRUPT_STS	INTERRUPT_STS	Go
0x25	TS_CONFIG	TS_CONFIG	Go
0x26	TS_CONTROL	TS_CONTROL	Go
0x27	TS_LINE_HI	TS_LINE_HI	Go
0x28	TS_LINE_LO	TS_LINE_LO	Go
0x29	TS_STATUS	TS_STATUS	Go

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Table 5-16. MAIN_PAGE Registers (continued)

Address	Acronym	Register Name	Section
0x2A	TIMESTAMP_P0_HI	TIMESTAMP_P0_HI	Go
0x2B	TIMESTAMP_P0_LO	TIMESTAMP_P0_LO	Go
0x2C	TIMESTAMP_P1_HI	TIMESTAMP_P1_HI	Go
0x2D	TIMESTAMP_P1_LO	TIMESTAMP_P1_LO	Go
0x2E	TIMESTAMP_P2_HI	TIMESTAMP_P2_HI	Go
0x2F	TIMESTAMP_P2_LO	TIMESTAMP_P2_LO	Go
0x30	TIMESTAMP_P3_HI	TIMESTAMP_P3_HI	Go
0x31	TIMESTAMP_P3_LO	TIMESTAMP_P3_LO	Go
0x32	CSI_PORT_SEL	CSI_PORT_SEL	Go
0x33	CSI_CTL	CSI_CTL	Go
0x34	CSI_CTL2	CSI_CTL2	Go
0x35	CSI_STS	CSI_STS	Go
0x36	CSI_TX_ICR	CSI_TX_ICR	Go
0x37	CSI_TX_ISR	CSI_TX_ISR	Go
0x41	SFILTER_CFG	SFILTER_CFG	Go
0x42	AEQ_CTL	AEQ_CTL	Go
0x43	AEQ_ERR_THOLD	AEQ_ERR_THOLD	Go
0x4C	FPD3_PORT_SEL	FPD3_PORT_SEL	Go
0x4D	RX_PORT_STS1	RX_PORT_STS1	Go
0x4E	RX_PORT_STS2	RX_PORT_STS2	Go
0x4F	RX_FREQ_HIGH	RX_FREQ_HIGH	Go
0x50	RX_FREQ_LOW	RX_FREQ_LOW	Go
0x55	RX_PAR_ERR_HI	RX_PAR_ERR_HI	Go
0x56	RX_PAR_ERR_LO	RX_PAR_ERR_LO	Go
0x57	BIST_ERR_COUNT	BIST_ERR_COUNT	Go
0x58	BCC_CONFIG	BCC_CONFIG	Go
0x59	DATAPATH_CTL1	DATAPATH_CTL1	Go
0x5A	DATAPATH_CTL2	DATAPATH_CTL2	Go
0x5B	SER_ID	SER_ID	Go
0x5C	SER_ALIAS_ID	SER_ALIAS_ID	Go
0x5D	TARGET_ID_0	TARGET_ID_0	Go
0x5E	TARGET_ID_1	TARGET_ID_1	Go
0x5F	TARGET_ID_2	TARGET_ID_2	Go
0x60	TARGET_ID_3	TARGET_ID_3	Go
0x61	TARGET_ID_4	TARGET_ID_4	Go
0x62	TARGET_ID_5	TARGET_ID_5	Go
0x63	TARGET_ID_6	TARGET_ID_6	Go
0x64	TARGET_ID_7	TARGET_ID_7	Go
0x65	TARGET_ALIAS_0	TARGET_ALIAS_0	Go
0x66	TARGET_ALIAS_1	TARGET_ALIAS_1	Go
0x67	TARGET_ALIAS_2	TARGET_ALIAS_2	Go
0x68	TARGET_ALIAS_3	TARGET_ALIAS_3	Go
0x69	TARGET_ALIAS_4	TARGET_ALIAS_4	Go
0x6A	TARGET_ALIAS_5	TARGET_ALIAS_5	Go
0x6B	TARGET_ALIAS_6	TARGET_ALIAS_6	Go

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Table 5-16. MAIN_PAGE Registers (continued)

Address	Acronym	Register Name	Section
0x6C	TARGET_ALIAS_7	TARGET_ALIAS_7	Go
0x6D	PORT_CONFIG	PORT_CONFIG	Go
0x6E	BC_GPIO_CTL0	BC_GPIO_CTL0	Go
0x6F	BC_GPIO_CTL1	BC_GPIO_CTL1	Go
0x70	RAW10_ID	RAW10_ID	Go
0x71	RAW12_ID	RAW12_ID	Go
0x73	LINE_COUNT_1	LINE_COUNT_1	Go
0x74	LINE_COUNT_0	LINE_COUNT_0	Go
0x75	LINE_LEN_1	LINE_LEN_1	Go
0x76	LINE_LEN_0	LINE_LEN_0	Go
0x77	FREQ_DET_CTL	FREQ_DET_CTL	Go
0x78	MAILBOX_1	MAILBOX_1	Go
0x79	MAILBOX_2	MAILBOX_2	Go
0x7C	PORT_CONFIG2	PORT_CONFIG2	Go
0x7D	PORT_PASS_CTL	PORT_PASS_CTL	Go
0xB0	IND_ACC_CTL	IND_ACC_CTL	Go
0xB1	IND_ACC_ADDR	IND_ACC_ADDR	Go
0xB2	IND_ACC_DATA	IND_ACC_DATA	Go
0xB3	BIST_CTL	BIST_CTL	Go
0xB6	PAR_ERR_CTRL	PAR_ERR_CTRL	Go
0xB8	MODE_IDX_STS	MODE_IDX_STS	Go
0xB9	LINK_ERROR_COUNT	LINK_ERROR_COUNT	Go
0xBC	FV_MIN_TIME	FV_MIN_TIME	Go
0xBE	GPIO_PD_CTL	GPIO_PD_CTL	Go
0xD0	PORT_DEBUG	PORT_DEBUG	Go
0xD2	AEQ_CTL2	AEQ_CTL2	Go
0xD3	AEQ_STATUS	AEQ_STATUS	Go
0xD4	AEQ_BYPASS	AEQ_BYPASS	Go
0xD5	AEQ_MIN_MAX	AEQ_MIN_MAX	Go
0xD8	PORT_ICR_HI	PORT_ICR_HI	Go
0xD9	PORT_ICR_LO	PORT_ICR_LO	Go
0xDA	PORT_ISR_HI	PORT_ISR_HI	Go
0xDB	PORT_ISR_LO	PORT_ISR_LO	Go
0xF0	FPD3_RX_ID0	FPD3_RX_ID0	Go
0xF1	FPD3_RX_ID1	FPD3_RX_ID1	Go
0xF2	FPD3_RX_ID2	FPD3_RX_ID2	Go
0xF3	FPD3_RX_ID3	FPD3_RX_ID3	Go
0xF4	FPD3_RX_ID4	FPD3_RX_ID4	Go
0xF5	FPD3_RX_ID5	FPD3_RX_ID5	Go
0xF8	I2C_RX0_ID	I2C_RX0_ID	Go
0xF9	I2C_RX1_ID	I2C_RX1_ID	Go
0xFA	I2C_RX2_ID	I2C_RX2_ID	Go
0xFB	I2C_RX3_ID	I2C_RX3_ID	Go

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Complex bit access types are encoded to fit into small table cells. Table 5-17 shows the codes that are used for access types in this section.

Table 5-17. Main_Page Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

5.6.1.1 I2C_DEVICE_ID Register (Address = 0x0) [Default = 0x00]

I2C_DEVICE_ID is shown in Table 5-18.

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Table 5-18. I2C_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	DEVICE_ID	R/W	0x0	7-bit I2C ID of Deserializer. This field always indicates the current value of the I2C ID. When bit 0 of this register is 0, this field is read-only and show the strapped ID. When bit 1 of this register is 1, this field is read/write and can be used to assign any valid I2C ID.
0	DES_ID	R/W	0x0	0: Device ID is from strap 1: Register I2C Device ID overrides strapped value

5.6.1.2 RESET_CTL Register (Address = 0x1) [Default = 0x00]

RESET_CTL is shown in Table 5-19.

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Reset control register This register can only be written from the primary local I2C interface.

Table 5-19. RESET_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4:3	RESERVED	R	0x0	Reserved
2	RESTART_AUTOLOAD	RH/W1S	0x0	Restart ROM Auto-load Setting this bit to 1 causes a re-load of the ROM. This bit is self-clearing. Software can check for Auto-load complete by checking the CFG_INIT_DONE bit in the DEVICE_STS register.

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Table 5-19. RESET_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	DIGITAL_RESET1	RH/W1S	0x0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation
0	DIGITAL_RESET0	RH/W1S	0x0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation

5.6.1.3 GENERAL_CFG Register (Address = 0x2) [Default = 0x1E]

GENERAL_CFG is shown in Table 5-20.

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Table 5-20. GENERAL_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	OUTPUT_EN_MODE	R/W	0x1	Output Enable Mode If set to 0, the CSI TX output port is forced to the high-impedance state if no assigned RX ports have an active Receiver lock. If set to 1, the CSI TX output port continues in normal operation if no assigned RX ports have an active Receiver lock. CSI TX operation remains under register control via the CSI_CTL register for each port. If no assigned RX ports have an active Receiver lock, this results in the CSI Transmitter entering the LP-11 state.
3	OUTPUT_ENABLE	R/W	0x1	Output Enable Control (in conjunction with Output Sleep State Select) If OUTPUT_SLEEP_STATE_SEL is set to 1 and this bit is set to 0, the CSI TX outputs are forced into a high impedance state.
2	OUTPUT_SLEEP_STATE_SEL	R/W	0x1	OSS Select to control output state when LOCK is low (used in conjunction with Output Enable) When this bit is set to 0, the CSI TX outputs are forced into a HS-0 state.
1	RX_PARITY_CHECK_EN	R/W	0x1	FPD3 Receiver Parity Checker Enable When enabled, the parity check function is enabled for the FPD3 receiver. This allows detection of errors on the FPD3 receiver data bits. 0: Disable 1: Enable
0	FORCE_REFCLK_DET	R/W	0x0	Force indication of external reference clock 0: Normal operation, reference clock detect circuit indicates the presence of an external reference clock 1: Force reference clock to be indicated present

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5.6.1.4 REV_MASK_ID Register (Address = 0x3) [Default = 0x00]

REV_MASK_ID is shown in Table 5-21.

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Table 5-21. REV_MASK_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	REVISION_ID	R	0x0	Revision ID 0010: DS90UB964 A0 0011: DS90UB964 A1
3:0	MASK_ID	R	0x0	Mask ID

5.6.1.5 DEVICE_STS Register (Address = 0x4) [Default = 0xC2]

DEVICE_STS is shown in Table 5-22.

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Table 5-22. DEVICE_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	CFG_CKSUM_STS	R	0x1	Config Checksum Passed This bit is set following initialization if the Configuration data in the eFuse ROM had a valid checksum
6	CFG_INIT_DONE	R	0x1	Power-up initialization complete This bit is set after Initialization is complete. Configuration from eFuse ROM has completed.
5:2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

5.6.1.6 PAR_ERR_THOLD1 Register (Address = 0x5) [Default = 0x01]

PAR_ERR_THOLD1 is shown in Table 5-23.

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Table 5-23. PAR_ERR_THOLD1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PAR_ERR_THOLD_HI	R/W	0x1	FPD3 Parity Error Threshold High byte This register provides the 8 most significant bits of the Parity Error Threshold value. For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to this value, the PARITY_ERROR flag is set in the RX_PORT_STS1 register.

5.6.1.7 PAR_ERR_THOLD0 Register (Address = 0x6) [Default = 0x00]

PAR_ERR_THOLD0 is shown in Table 5-24.

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Table 5-24. PAR_ERR_THOLD0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PAR_ERR_THOLD_LO	R/W	0x0	FPD3 Parity Error Threshold Low byte This register provides the 8 least significant bits of the Parity Error Threshold value. For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to this value, the PARITY_ERROR flag is set in the RX_PORT_STS1 register.

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5.6.1.8 BCC_WATCHDOG_CONTROL Register (Address = 0x7) [Default = 0xFE]

BCC_WATCHDOG_CONTROL is shown in Table 5-25.

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Table 5-25. BCC_WATCHDOG_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	BCC_WATCHDOG_TIMER	R/W	0x7F	The watchdog timer allows termination of a control channel transaction if the transaction fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field must not be set to 0.
0	BCC_WATCHDOG_TIMER_DISABLE	R/W	0x0	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation

5.6.1.9 I2C_CONTROL_1 Register (Address = 0x8) [Default = 0x1C]

I2C_CONTROL_1 is shown in Table 5-26.

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Table 5-26. I2C_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LOCAL_WRITE_DISABLE	R/W	0x0	Disable Remote Writes to Local Registers Setting this bit to a 1 prevents remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I2C controller attached to the Serializer. Setting this bit does not affect remote access to I2C targets at the Deserializer.
6:4	I2C_SDA_HOLD	R/W	0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds.
3:0	I2C_FILTER_DEPTH	R/W	0xC	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that are rejected. Units are 5 nanoseconds.

5.6.1.10 I2C_CONTROL_2 Register (Address = 0x9) [Default = 0x10]

I2C_CONTROL_2 is shown in Table 5-27.

Return to the Summary Table.

Table 5-27. I2C_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	SDA_OUTPUT_SETUP	R/W	0x1	Remote Ack SDA Output Setup When a Control Channel (remote) access is active, this field configures setup time from the SDA output relative to the rising edge of SCL during ACK cycles. Setting this value increases setup time in units of 640ns. The nominal output setup time value for SDA to SCL when this field is 0 is 80ns.
3:2	SDA_OUTPUT_DELAY	R/W	0x0	SDA Output Delay This field configures additional delay on the SDA output relative to the falling edge of SCL. Setting this value increases output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00: 240ns 01: 280ns 10: 320ns 11: 360ns

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Table 5-27. I2C_CONTROL_2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	I2C_BUS_TIMER_SPEED UP	R/W	0x0	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
0	I2C_BUS_TIMER_DISAB LE	R/W	0x0	Disable I2C Bus Watchdog Timer The I2C Watchdog Timer can be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 second, the I2C bus id assumed to be free. If SDA is low and no signaling occurs, the device attempts to clear the bus by driving 9 clocks on SCL

5.6.1.11 SCL_HIGH_TIME Register (Address = 0xA) [Default = 0x79]

SCL_HIGH_TIME is shown in Table 5-28.

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Table 5-28. SCL_HIGH_TIME Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SCL_HIGH_TIME	R/W	0x79	I2C Controller SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Controller on the local I2C bus. Units are 40ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the reference clock at 25MHz + 100ppm. The delay includes 5 additional oscillator clock periods. Min_delay= 39.996ns * (SCL_HIGH_TIME + 5)

5.6.1.12 SCL_LOW_TIME Register (Address = 0xB) [Default = 0x79]

SCL_LOW_TIME is shown in Table 5-29.

Return to the Summary Table.

Table 5-29. SCL_LOW_TIME Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SCL_LOW_TIME	R/W	0x79	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Controller on the local I2C bus. This value is also used as the SDA setup time by the I2C Target for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the reference clock at 25MHz + 100ppm. The delay includes 5 additional clock periods. Min_delay= 39.996ns * (SCL_LOW_TIME+ 5)

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5.6.1.13 RX_PORT_CTL Register (Address = 0xC) [Default = 0x0F]

RX_PORT_CTL is shown in Table 5-30.

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Table 5-30. RX_PORT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	BCC3_MAP	R/W	0x0	Map Control Channel 3 to I2C Target Port 0: I2C Target Port 0 1: I2C Target Port 1
6	BCC2_MAP	R/W	0x0	Map Control Channel 2 to I2C Target Port 0: I2C Target Port 0 1: I2C Target Port 1
5	BCC1_MAP	R/W	0x0	Map Control Channel 1 to I2C Target Port 0: I2C Target Port 0 1: I2C Target Port 1
4	BCC0_MAP	R/W	0x0	Map Control Channel 0 to I2C Target Port 0: I2C Target Port 0 1: I2C Target Port 1
3	PORT3_EN	R/W	0x1	Port 3 Receiver Enable 0: Disable Port 3 Receiver 1: Enable Port 3 Receiver
2	PORT2_EN	R/W	0x1	Port 2 Receiver Enable 0: Disable Port 2 Receiver 1: Enable Port 2 Receiver
1	PORT1_EN	R/W	0x1	Port 1 Receiver Enable 0: Disable Port 1 Receiver 1: Enable Port 1 Receiver
0	PORT0_EN	R/W	0x1	Port 0 Receiver Enable 0: Disable Port 0 Receiver 1: Enable Port 0 Receiver

5.6.1.14 IO_CTL Register (Address = 0xD) [Default = 0x09]

IO_CTL is shown in Table 5-31.

Return to the Summary Table.

Table 5-31. IO_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	SEL3P3V	R/W	0x0	3.3V I/O Select on pins PDB,INTB,I2C 0: 1.8V I/O Supply 1: 3.3V I/O Supply If IO_SUPPLY_MODE_OV is 0, a read of this register returns the detected I/O voltage level.
6	IO_SUPPLY_MODE_OV	R/W	0x0	Override I/O Supply Mode bit If set to 0, the detected voltage level is used for both SEL3P3V and IO_SUPPLY_MODE controls. If set to 1, the values written to the SEL3P3V and IO_SUPPLY_MODE fields are used.
5:4	IO_SUPPLY_MODE	R/W	0x0	I/O Supply Mode 00: 1.8V 01: Reserved 10: Reserved 11: 3.3V If IO_SUPPLY_MODE_OV is 0, a read of this register returns the detected I/O voltage level.
3:0	RESERVED	R	0x0	Reserved

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5.6.1.15 GPIO_PIN_STS Register (Address = 0xE) [Default = 0x00]

GPIO_PIN_STS is shown in Table 5-32.

Return to the Summary Table.

Table 5-32. GPIO_PIN_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	GPIO_STS	R	0x0	GPIO Pin Status This register reads the current values on each of the 8 GPIO pins. Bit 7 reads GPIO7 and bit 0 reads GPIO0.

5.6.1.16 GPIO_INPUT_CTL Register (Address = 0xF) [Default = 0xFF]

GPIO_INPUT_CTL is shown in Table 5-33.

Return to the Summary Table.

Table 5-33. GPIO_INPUT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO7_INPUT_EN	R/W	0x1	GPIO7 Input Enable 0: Disabled 1: Enabled
6	GPIO6_INPUT_EN	R/W	0x1	GPIO6 Input Enable 0: Disabled 1: Enabled
5	GPIO5_INPUT_EN	R/W	0x1	GPIO5 Input Enable 0: Disabled 1: Enabled
4	GPIO4_INPUT_EN	R/W	0x1	GPIO4 Input Enable 0: Disabled 1: Enabled
3	GPIO3_INPUT_EN	R/W	0x1	GPIO3 Input Enable 0: Disabled 1: Enabled
2	GPIO2_INPUT_EN	R/W	0x1	GPIO2 Input Enable 0: Disabled 1: Enabled
1	GPIO1_INPUT_EN	R/W	0x1	GPIO1 Input Enable 0: Disabled 1: Enabled
0	GPIO0_INPUT_EN	R/W	0x1	GPIO0 Input Enable 0: Disabled 1: Enabled

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5.6.1.17 GPIO0_PIN_CTL Register (Address = 0x10) [Default = 0x00]

GPIO0_PIN_CTL is shown in Table 5-34.

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Table 5-34. GPIO0_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO0_OUT_SEL	R/W	0x0	GPIO0 Output Select Determines the output data for the selected source. If GPIO0_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO0_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101 - 111: Reserved If GPIO0_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt 111: Reserved
4:2	GPIO0_OUT_SRC	R/W	0x0	GPIO0 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO0_OUT_VAL	R/W	0x0	GPIO0 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO0_OUT_EN	R/W	0x0	GPIO0 Output Enable 0: Disabled 1: Enabled

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5.6.1.18 GPIO1_PIN_CTL Register (Address = 0x11) [Default = 0x00]

GPIO1_PIN_CTL is shown in Table 5-35.

Return to the Summary Table.

Table 5-35. GPIO1_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO1_OUT_SEL	R/W	0x0	GPIO1 Output Select Determines the output data for the selected source. If GPIO1_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO1_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101 - 111: Reserved If GPIO1_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt 111: Reserved
4:2	GPIO1_OUT_SRC	R/W	0x0	GPIO1 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO1_OUT_VAL	R/W	0x0	GPIO1 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO1_OUT_EN	R/W	0x0	GPIO1 Output Enable 0: Disabled 1: Enabled

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5.6.1.19 GPIO2_PIN_CTL Register (Address = 0x12) [Default = 0x00]

GPIO2_PIN_CTL is shown in Table 5-36.

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Table 5-36. GPIO2_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO2_OUT_SEL	R/W	0x0	GPIO2 Output Select Determines the output data for the selected source. If GPIO2_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO2_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101 - 111: Reserved If GPIO2_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt 111: Reserved
4:2	GPIO2_OUT_SRC	R/W	0x0	GPIO2 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO2_OUT_VAL	R/W	0x0	GPIO2 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO2_OUT_EN	R/W	0x0	GPIO2 Output Enable 0: Disabled 1: Enabled

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5.6.1.20 GPIO3_PIN_CTL Register (Address = 0x13) [Default = 0x00]

GPIO3_PIN_CTL is shown in Table 5-37.

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Table 5-37. GPIO3_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO3_OUT_SEL	R/W	0x0	GPIO3 Output Select Determines the output data for the selected source. If GPIO3_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO3_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: Frame Valid signal 101: Line Valid signal 110 - 111: Reserved If GPIO3_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt 111: Reserved
4:2	GPIO3_OUT_SRC	R/W	0x0	GPIO3 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO3_OUT_VAL	R/W	0x0	GPIO3 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO3_OUT_EN	R/W	0x0	GPIO3 Output Enable 0: Disabled 1: Enabled

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5.6.1.21 GPIO4_PIN_CTL Register (Address = 0x14) [Default = 0x00]

GPIO4_PIN_CTL is shown in Table 5-38.

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Table 5-38. GPIO4_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO4_OUT_SEL	R/W	0x0	GPIO4 Output Select Determines the output data for the selected source. If GPIO4_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO4_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101 - 111: Reserved If GPIO4_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt 111: Reserved
4:2	GPIO4_OUT_SRC	R/W	0x0	GPIO4 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO4_OUT_VAL	R/W	0x0	GPIO4 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO4_OUT_EN	R/W	0x0	GPIO4 Output Enable 0: Disabled 1: Enabled

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5.6.1.22 GPIO5_PIN_CTL Register (Address = 0x15) [Default = 0x00]

GPIO5_PIN_CTL is shown in Table 5-39.

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Table 5-39. GPIO5_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO5_OUT_SEL	R/W	0x0	GPIO5 Output Select Determines the output data for the selected source. If GPIO5_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO5_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101 - 111: Reserved If GPIO5_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt 111: Reserved
4:2	GPIO5_OUT_SRC	R/W	0x0	GPIO5 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO5_OUT_VAL	R/W	0x0	GPIO5 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO5_OUT_EN	R/W	0x0	GPIO5 Output Enable 0: Disabled 1: Enabled

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5.6.1.23 GPIO6_PIN_CTL Register (Address = 0x16) [Default = 0x00]

GPIO6_PIN_CTL is shown in Table 5-40.

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Table 5-40. GPIO6_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO6_OUT_SEL	R/W	0x0	GPIO6 Output Select Determines the output data for the selected source. If GPIO6_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO6_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101 - 111: Reserved If GPIO6_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt 111: Reserved
4:2	GPIO6_OUT_SRC	R/W	0x0	GPIO6 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO6_OUT_VAL	R/W	0x0	GPIO6 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO6_OUT_EN	R/W	0x0	GPIO6 Output Enable 0: Disabled 1: Enabled

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5.6.1.24 GPIO7_PIN_CTL Register (Address = 0x17) [Default = 0x00]

GPIO7_PIN_CTL is shown in Table 5-41.

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Table 5-41. GPIO7_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO7_OUT_SEL	R/W	0x0	GPIO7 Output Select Determines the output data for the selected source. If GPIO7_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO7_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101 - 111: Reserved If GPIO7_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt 111: Reserved
4:2	GPIO7_OUT_SRC	R/W	0x0	GPIO7 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO7_OUT_VAL	R/W	0x0	GPIO7 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO7_OUT_EN	R/W	0x0	GPIO7 Output Enable 0: Disabled 1: Enabled

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5.6.1.25 FS_CTL Register (Address = 0x18) [Default = 0x00]

FS_CTL is shown in Table 5-42.

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Table 5-42. FS_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	FS_MODE	R/W	0x0	FrameSync Mode 0000: Internal Generated FrameSync, use Back-channel frame clock from port 0 0001: Internal Generated FrameSync, use Back-channel frame clock from port 1 0010: Internal Generated FrameSync, use Back-channel frame clock from port 2 0011: Internal Generated FrameSync, use Back-channel frame clock from port 3 01xx: Internal Generated FrameSync, use 25MHz clock 1000: External FrameSync from GPIO0 1001: External FrameSync from GPIO1 1010: External FrameSync from GPIO2 1011: External FrameSync from GPIO3 1100: External FrameSync from GPIO4 1101: External FrameSync from GPIO5 1110: External FrameSync from GPIO6 1111: External FrameSync from GPIO7
3	FS_SINGLE	RH/W1S	0x0	Generate Single FrameSync pulse When this bit is set, a single FrameSync pulse is generated. The system must wait for the full duration of the desired pulse before generating another pulse. When using this feature, the FS_GEN_ENABLE bit must remain set to 0. This bit is self-clearing and always returns 0.
2	FS_INIT_STATE	R/W	0x0	FrameSync Initial State This register controls the initial state of the FrameSync signal. 0: FrameSync initial state is 0 1: FrameSync initial state is 1
1	FS_GEN_MODE	R/W	0x0	FrameSync Generation Mode This control selects between Hi/Lo and 50/50 modes. In Hi/Lo mode, the FrameSync generator uses the FS_HIGH_TIME and FS_LOW_TIME register values to separately control the High and Low periods for the generated FrameSync signal. FrameSync times are based on the settings of the FS_MODE field. In 50/50 mode, the FrameSync generator uses the values in the FS_HIGH_TIME_0, FS_LOW_TIME_1 and FS_LOW_TIME_0 registers as a 24-bit value for both the High and Low periods of the generated FrameSync signal. 0: Hi/Lo 1: 50/50
0	FS_GEN_ENABLE	R/W	0x0	FrameSync Generation Enable 0: Disabled 1: Enabled

5.6.1.26 FS_HIGH_TIME_1 Register (Address = 0x19) [Default = 0x00]

FS_HIGH_TIME_1 is shown in Table 5-43.

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Table 5-43. FS_HIGH_TIME_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAMESYNC_HIGH_TIME_1	R/W	0x0	FrameSync High Time bits 15:8 The value programmed to the FS_HIGH_TIME register must be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field results in a 1 cycle high pulse on the FrameSync signal.

5.6.1.27 FS_HIGH_TIME_0 Register (Address = 0x1A) [Default = 0x00]

FS_HIGH_TIME_0 is shown in Table 5-44.

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Table 5-44. FS_HIGH_TIME_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAMESYNC_HIGH_TIME_0	R/W	0x0	FrameSync High Time bits 7:0 The value programmed to the FS_HIGH_TIME register must be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field results in a 1 cycle high pulse on the FrameSync signal.

5.6.1.28 FS_LOW_TIME_1 Register (Address = 0x1B) [Default = 0x00]

FS_LOW_TIME_1 is shown in Table 5-45.

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Table 5-45. FS_LOW_TIME_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAMESYNC_LOW_TIME_1	R/W	0x0	FrameSync Low Time bits 15:8 The value programmed to the FS_HIGH_TIME register must be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field results in a 1 cycle high pulse on the FrameSync signal.

5.6.1.29 FS_LOW_TIME_0 Register (Address = 0x1C) [Default = 0x00]

FS_LOW_TIME_0 is shown in Table 5-46.

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Table 5-46. FS_LOW_TIME_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAMESYNC_LOW_TIME_0	R/W	0x0	FrameSync Low Time bits 7:0 The value programmed to the FS_HIGH_TIME register must be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field results in a 1 cycle high pulse on the FrameSync signal.

5.6.1.30 MAX_FRM_HI Register (Address = 0x1D) [Default = 0x00]

MAX_FRM_HI is shown in Table 5-47.

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Table 5-47. MAX_FRM_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MAX_FRAME_HI	R/W	0x0	CSI-2 Maximum Frame Count bits 15:8 In RAW mode operation, the FPD3 Receiver creates CSI2 video frames. For the Frame Start and Frame End packets of each video frame, a 16-bit frame number field is generated. If the Maximum Frame Count value is set to 0, the frame number is disabled and is always 0. If Maximum Frame Count value is non-zero, the frame number increments for each from 1 up to the Maximum Frame Count value before resetting to 1.

5.6.1.31 MAX_FRM_LO Register (Address = 0x1E) [Default = 0x04]

MAX_FRM_LO is shown in Table 5-48.

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Table 5-48. MAX_FRM_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MAX_FRAME_LO	R/W	0x4	CSI-2 Maximum Frame Count bits 7:0 In RAW mode operation, the FPD3 Receiver creates CSI2 video frames. For the Frame Start and Frame End packets of each video frame, a 16-bit frame number field is generated. If the Maximum Frame Count value is set to 0, the frame number is disabled and is always 0. If Maximum Frame Count value is non-zero, the frame number increments for each from 1 up to the Maximum Frame Count value before resetting to 1.

5.6.1.32 CSI_PLL_CTL Register (Address = 0x1F) [Default = 0x02]

CSI_PLL_CTL is shown in Table 5-49.

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Table 5-49. CSI_PLL_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1:0	CSI_TX_SPEED	R/W	0x2	CSI Transmitter Speed select: Controls the CSI Transmitter frequency. 00: 1.6Gbps serial rate 01: Reserved 10: 800Mbps serial rate 11: 400Mbps serial rate

5.6.1.33 FWD_CTL1 Register (Address = 0x20) [Default = 0xF0]

FWD_CTL1 is shown in Table 5-50.

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Table 5-50. FWD_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	FWD_PORT3_DIS	R/W	0x1	Disable forwarding of RX Port 3 0: Forwarding enabled 1: Forwarding disabled
6	FWD_PORT2_DIS	R/W	0x1	Disable forwarding of RX Port 2 0: Forwarding enabled 1: Forwarding disabled

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Table 5-50. FWD_CTL1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	FWD_PORT1_DIS	R/W	0x1	Disable forwarding of RX Port 1 0: Forwarding enabled 1: Forwarding disabled
4	FWD_PORT0_DIS	R/W	0x1	Disable forwarding of RX Port 0 0: Forwarding enabled 1: Forwarding disabled
3	RX3_MAP	R/W	0x0	Map RX Port 3 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping.
2	RX2_MAP	R/W	0x0	Map RX Port 2 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping.
1	RX1_MAP	R/W	0x0	Map RX Port 1 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping.
0	RX0_MAP	R/W	0x0	Map RX Port 0 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping.

5.6.1.34 FWD_CTL2 Register (Address = 0x21) [Default = 0x03]

FWD_CTL2 is shown in Table 5-51.

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Table 5-51. FWD_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	CSI_REPLICATE	R/W	0x0	CSI Replicate Mode When set to a 1, the CSI output from port 0 is also generated on CSI port 1. The same output data is presented on both ports.
6	FWD_SYNC_AS_AVAIL	R/W	0x0	Synchronized Forwarding As Available During Synchronized Forwarding, each forwarding engine waits for video data to be available from each enabled port, prior to sending the video line. Setting this bit to a 1 allows sending the next video line as the data becomes available. For example, if RX Ports 0 and 1 are being forwarded, port 0 video line is forwarded when the data becomes available, rather than waiting until both ports 0 and ports 1 have video data available. This operation can reduce the likelihood of buffer overflow errors in some conditions. This bit has no affect in video line concatenation mode and only affects video lines (long packets) rather than synchronization packets. This bit applies to both CSI output ports
5:4	CSI1_SYNC_FWD	R/W	0x0	Enable synchronized forwarding for CSI output port 1 00: Synchronized forwarding disabled 01: Basic Synchronized forwarding enabled 10: Synchronous forwarding with line interleaving 11: Synchronous forwarding with line concatenation Only one of CSI1_RR_FWD and CSI1_SYNC_FWD must be enabled at a time.

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Table 5-51. FWD_CTL2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:2	CSI0_SYNC_FWD	R/W	0x0	Enable synchronized forwarding for CSI output port 0 00: Synchronized forwarding disabled 01: Basic Synchronized forwarding enabled 10: Synchronous forwarding with line interleaving 11: Synchronous forwarding with line concatenation Only one of CSI0_RR_FWD and CSI0_SYNC_FWD must be enabled at a time.
1	CSI1_RR_FWD	R/W	0x1	Enable best-effort forwarding for CSI output port 1. When this mode is enabled, no attempt is made to synchronize the video traffic. When multiple sources have data available to forward, the data tends to be forwarded in a round-robin fashion. 0: Round robin forwarding disabled 1: Round robin forwarding enabled Only one of CSI1_RR_FWD and CSI1_SYNC_FWD must be enabled at a time.
0	CSI0_RR_FWD	R/W	0x1	Enable best-effort forwarding for CSI output port 0. When this mode is enabled, no attempt is made to synchronize the video traffic. When multiple sources have data available to forward, the data tends to be forwarded in a round-robin fashion. 0: Round robin forwarding disabled 1: Round robin forwarding enabled Only one of CSI0_RR_FWD and CSI0_SYNC_FWD must be enabled at a time.

5.6.1.35 FWD_STS Register (Address = 0x22) [Default = 0x00]

FWD_STS is shown in Table 5-52.

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Table 5-52. FWD_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	FWD_SYNC_FAIL1	RC	0x0	Forwarding synchronization failed for CSI output port 1 During Synchronized forwarding, this flag indicates a failure of synchronized video has been detected. For this bit to be set, the forwarding process must have previously been successful at sending at least one synchronized video frame. 0: No failure 1: Synchronization failure This bit is cleared on read.
2	FWD_SYNC_FAIL0	RC	0x0	Forwarding synchronization failed for CSI output port 0 During Synchronized forwarding, this flag indicates a failure of synchronized video has been detected. For this bit to be set, the forwarding process must have previously been successful at sending at least one synchronized video frame. 0: No failure 1: Synchronization failure This bit is cleared on read.
1	FWD_SYNC1	R	0x0	Forwarding synchronized for CSI output port 1 During Synchronized forwarding, this bit indicates that the forwarding engine is currently able to provide synchronized video from enabled Receive ports. This bit is always 0 if Synchronized forwarding is disabled. 0: Video is not synchronized 1: Video is synchronized

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Table 5-52. FWD_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	FWD_SYNC0	R	0x0	Forwarding synchronized for CSI output port 0 During Synchronized forwarding, this bit indicates that the forwarding engine is currently able to provide synchronized video from enabled Receive ports. This bit is always 0 if Synchronized forwarding is disabled. 0: Video is not synchronized 1: Video is synchronized

5.6.1.36 INTERRUPT_CTL Register (Address = 0x23) [Default = 0x00]

INTERRUPT_CTL is shown in Table 5-53.

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Table 5-53. INTERRUPT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	INT_EN	R/W	0x0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.
6	RESERVED	R	0x0	Reserved
5	IE_CSI_TX1	R/W	0x0	CSI Transmit Port 1 Interrupt: Enable interrupt from CSI Transmitter Port 1.
4	IE_CSI_TX0	R/W	0x0	CSI Transmit Port 0 Interrupt: Enable interrupt from CSI Transmitter Port 0.
3	IE_RX3	R/W	0x0	RX Port 3 Interrupt: Enable interrupt from Receiver Port 3.
2	IE_RX2	R/W	0x0	RX Port 2 Interrupt: Enable interrupt from Receiver Port 2.
1	IE_RX1	R/W	0x0	RX Port 1 Interrupt: Enable interrupt from Receiver Port 1.
0	IE_RX0	R/W	0x0	RX Port 0 Interrupt: Enable interrupt from Receiver Port 0.

5.6.1.37 INTERRUPT_STS Register (Address = 0x24) [Default = 0x00]

INTERRUPT_STS is shown in Table 5-54.

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Table 5-54. INTERRUPT_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	INT	R	0x0	Global Interrupt: Set if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INT_EN bit in the INTERRUPT_CTL register but does depend on the IE_xxx bits. For example, if IE_RX0 and IS_RX0 are both asserted, the INT bit is set to 1.
6	RESERVED	R	0x0	Reserved
5	IS_CSI_TX1	R	0x0	CSI Transmit Port 1 Interrupt: An interrupt has occurred for CSI Transmitter Port 1. This interrupt is cleared upon reading the CSI_TX_ISR register for CSI Transmit Port 1.
4	IS_CSI_TX0	R	0x0	CSI Transmit Port 0 Interrupt: An interrupt has occurred for CSI Transmitter Port 0. This interrupt is cleared upon reading the CSI_TX_ISR register for CSI Transmit Port 0.

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Table 5-54. INTERRUPT_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	IS_RX3	R	0x0	RX Port 3 Interrupt: An interrupt has occurred for Receive Port 3. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
2	IS_RX2	R	0x0	RX Port 2 Interrupt: An interrupt has occurred for Receive Port 2. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
1	IS_RX1	R	0x0	RX Port 1 Interrupt: An interrupt has occurred for Receive Port 1. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
0	IS_RX0	R	0x0	RX Port 0 Interrupt: An interrupt has occurred for Receive Port 0. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.

5.6.1.38 TS_CONFIG Register (Address = 0x25) [Default = 0x00]

TS_CONFIG is shown in Table 5-55.

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Table 5-55. TS_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	FS_POLARITY	R/W	0x0	Framesync Polarity Indicates active edge of FrameSync signal 0: Rising edge 1: Falling edge
5:4	TS_RES_CTL	R/W	0x0	Timestamp Resolution Control 00: 40ns 01: 80ns 10: 160ns 11: 1.0us
3	TS_AS_AVAIL	R/W	0x0	Timestamp Ready Control 0: Normal operation 1: Indicate timestamps ready as soon as all port timestamps are available
2	RESERVED	R	0x0	Reserved
1	TS_FREERUN	R/W	0x0	FreeRun Mode 0: FrameSync mode 1: FreeRun mode
0	TS_MODE	R/W	0x0	Timestamp Mode 0: Line start 1: Frame start

5.6.1.39 TS_CONTROL Register (Address = 0x26) [Default = 0x00]

TS_CONTROL is shown in Table 5-56.

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Table 5-56. TS_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	TS_FREEZE	R/W	0x0	Freeze Timestamps 0: Normal operation 1: Freeze timestamps Setting this bit freezes timestamps and clears the TS_READY flag. The TS_FREEZE bit must be cleared after reading timestamps to resume operation.
3	TS_ENABLE3	R/W	0x0	Timestamp Enable RX Port 3 0: Disabled 1: Enabled
2	TS_ENABLE2	R/W	0x0	Timestamp Enable RX Port 2 0: Disabled 1: Enabled
1	TS_ENABLE1	R/W	0x0	Timestamp Enable RX Port 1 0: Disabled 1: Enabled
0	TS_ENABLE0	R/W	0x0	Timestamp Enable RX Port 0 0: Disabled 1: Enabled

5.6.1.40 TS_LINE_HI Register (Address = 0x27) [Default = 0x00]

TS_LINE_HI is shown in Table 5-57.

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Table 5-57. TS_LINE_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TS_LINE_HI	R/W	0x0	Timestamp Line, upper 8 bits This field is the line number at which to capture the timestamp when Line Start mode is enabled. For proper operation, the line number must be set to a value greater than 1. During Frame Start mode, if TS_FREERUN is set, the TS_LINE value is used to determine when to begin checking for Frame Start

5.6.1.41 TS_LINE_LO Register (Address = 0x28) [Default = 0x00]

TS_LINE_LO is shown in Table 5-58.

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Table 5-58. TS_LINE_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TS_LINE_LO	R/W	0x0	Timestamp Line, lower 8 bits This field is the line number at which to capture the timestamp when Line Start mode is enabled. For proper operation, the line number must be set to a value greater than 1. During Frame Start mode, if TS_FREERUN is set, the TS_LINE value is used to determine when to begin checking for Frame Start

5.6.1.42 TS_STATUS Register (Address = 0x29) [Default = 0x00]

TS_STATUS is shown in Table 5-59.

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Table 5-59. TS_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	TS_READY	R	0x0	Timestamp Ready This flag indicates when timestamps are ready to be read. This flag is cleared when the TS_FREEZE bit is set.
3	TS_VALID3	R	0x0	Timestamp Valid, RX Port 3
2	TS_VALID2	R	0x0	Timestamp Valid, RX Port 2
1	TS_VALID1	R	0x0	Timestamp Valid, RX Port 1
0	TS_VALID0	R	0x0	Timestamp Valid, RX Port 0

5.6.1.43 TIMESTAMP_P0_HI Register (Address = 0x2A) [Default = 0x00]

TIMESTAMP_P0_HI is shown in Table 5-60.

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Table 5-60. TIMESTAMP_P0_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P0_HI	R	0x0	Timestamp, upper 8 bits, RX Port 0

5.6.1.44 TIMESTAMP_P0_LO Register (Address = 0x2B) [Default = 0x00]

TIMESTAMP_P0_LO is shown in Table 5-61.

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Table 5-61. TIMESTAMP_P0_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P0_LO	R	0x0	Timestamp, lower 8 bits, RX Port 0

5.6.1.45 TIMESTAMP_P1_HI Register (Address = 0x2C) [Default = 0x00]

TIMESTAMP_P1_HI is shown in Table 5-62.

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Table 5-62. TIMESTAMP_P1_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P1_HI	R	0x0	Timestamp, upper 8 bits, RX Port 1

5.6.1.46 TIMESTAMP_P1_LO Register (Address = 0x2D) [Default = 0x00]

TIMESTAMP_P1_LO is shown in Table 5-63.

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Table 5-63. TIMESTAMP_P1_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P1_LO	R	0x0	Timestamp, lower 8 bits, RX Port 1

5.6.1.47 TIMESTAMP_P2_HI Register (Address = 0x2E) [Default = 0x00]

TIMESTAMP_P2_HI is shown in Table 5-64.

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Table 5-64. TIMESTAMP_P2_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P2_HI	R	0x0	Timestamp, upper 8 bits, RX Port 2

5.6.1.48 TIMESTAMP_P2_LO Register (Address = 0x2F) [Default = 0x00]

TIMESTAMP_P2_LO is shown in Table 5-65.

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Table 5-65. TIMESTAMP_P2_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P2_LO	R	0x0	Timestamp, lower 8 bits, RX Port 2

5.6.1.49 TIMESTAMP_P3_HI Register (Address = 0x30) [Default = 0x00]

TIMESTAMP_P3_HI is shown in Table 5-66.

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Table 5-66. TIMESTAMP_P3_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P3_HI	R	0x0	Timestamp, upper 8 bits, RX Port 3

5.6.1.50 TIMESTAMP_P3_LO Register (Address = 0x31) [Default = 0x00]

TIMESTAMP_P3_LO is shown in Table 5-67.

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Table 5-67. TIMESTAMP_P3_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P3_LO	R	0x0	Timestamp, lower 8 bits, RX Port 3

5.6.1.51 CSI_PORT_SEL Register (Address = 0x32) [Default = 0x00]

CSI_PORT_SEL is shown in Table 5-68.

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Table 5-68. CSI_PORT_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	TX_READ_PORT	R/W	0x0	Select TX port for register read This field selects one of the two TX port register blocks for readback. This applies to the subsequent registers prefixed CSI. 0: Port 0 registers 1: Port 1 registers
3:2	RESERVED	R	0x0	Reserved

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Table 5-68. CSI_PORT_SEL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	TX_WRITE_PORT_1	R/W	0x0	Write Enable for TX port 1 registers This bit enables writes to TX port 1 registers. Any combination of TX port registers can be written simultaneously. This applies to the subsequent registers prefixed CSI. 0: Writes disabled 1: Writes enabled
0	TX_WRITE_PORT_0	R/W	0x0	Write Enable for TX port 0 registers This bit enables writes to TX port 0 registers. Any combination of TX port registers can be written simultaneously. This applies to the subsequent registers prefixed CSI. 0: Writes disabled 1: Writes enabled

5.6.1.52 CSI_CTL Register (Address = 0x33) [Default = 0x00]

CSI_CTL is shown in Table 5-69.

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Table 5-69. CSI_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	CSI_CAL_EN	R/W	0x0	Enable initial CSI Skew-Calibration sequence When the initial skew-calibration sequence is enabled, the CSI Transmitter sends the sequence at initialization, prior to sending any HS data. This bit is recommended to be set when operating at 1.6Gbps CSI speed (as configured in the CSI_PLL register). 0: Disabled 1: Enabled
5:4	CSI_LANE_COUNT	R/W	0x0	CSI lane count 00: 4 lanes 01: 3 lanes 10: 2 lanes 11: 1 lane
3:2	CSI_ULP	R/W	0x0	Force LP00 state on data/clock lanes 00: Normal operation 01: LP00 state forced only on data lanes 10: Reserved 11: LP00 state forced on data and clock lanes
1	CSI_CONTS_CLOCK	R/W	0x0	Enable CSI continuous clock mode When enabled, the CSI Transmitter enters continuous clock mode upon transmission of the first packet. 0: Disabled 1: Enabled
0	CSI_ENABLE	R/W	0x0	Enable CSI output 0: Disabled 1: Enabled Forwarding is recommended to be disabled (via the FWD_CTL1 register) prior to enabling or disabling the CSI output.

5.6.1.53 CSI_CTL2 Register (Address = 0x34) [Default = 0x00]

CSI_CTL2 is shown in Table 5-70.

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Table 5-70. CSI_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	CSI_PASS_MODE	R/W	0x0	CSI PASS indication mode Determines whether the CSI Pass indication is for a single port or all enabled ports. 0: Assert PASS if at least one enabled Receive port is providing valid video data 1: Assert PASS only if ALL enabled Receive ports are providing valid video data
2	CSI_CAL_INV	R/W	0x0	CSI Calibration Inverted Data pattern During the CSI skew-calibration pattern, the CSI Transmitter sends a sequence of 01010101 data (first bit 0). Setting this bit to a 1 inverts the sequence to 10101010 data.
1	CSI_CAL_SINGLE	RH/W1S	0x0	Enable single periodic CSI Skew-Calibration sequence Setting this bit sends a single skew-calibration sequence from the CSI Transmitter. The skew-calibration sequence has 2^{10} bits in the 1010 bit sequence required for periodic calibration. The calibration sequence is sent at the next idle period on the CSI interface. This bit is self-clearing and resets to 0 after the calibration sequence is sent.
0	CSI_CAL_PERIODIC	R/W	0x0	Enable periodic CSI Skew-Calibration sequence When the periodic skew-calibration sequence is enabled, the CSI Transmitter sends the periodic skew-calibration sequence following the sending of Frame End packets. 0: Disabled 1: Enabled

5.6.1.54 CSI_STS Register (Address = 0x35) [Default = 0x00]

CSI_STS is shown in Table 5-71.

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Table 5-71. CSI_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	TX_PORT_NUM	R	0x0	TX Port Number This read-only field indicates the number of the currently selected TX read port.
3:2	RESERVED	R	0x0	Reserved
1	TX_PORT_SYNC	R	0x0	TX Port Synchronized Thist bit indicates the CSI Transmit Port is able to properly synchronize input data streams from multiple sources. This bit is 0 if synchronization is disabled via the FWD_CTL2 register. 0: Input streams are not synchronized 1: Input streams are synchronized
0	PASS	R	0x0	TX Port Pass Indicates valid data is available on at least one port, or on all ports if configured for all port status via the CSI_PASS_MODE bit in the CSI_CTL2 register. The function differs based on mode of operation. In asynchronous operation, the TX_PORT_PASS indicates the CSI port is actively delivering valid video data. The status is cleared based on detection of an error condition that interrupts transmission. During Synchronized forwarding, the TX_PORT_PASS indicates valid data is available for delivery on the CSI TX output. Data can not be delivered if ports are not synchronized. The TX_PORT_SYNC status is a better indicator that valid data is being delivered to the CSI transmit port.

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5.6.1.55 CSI_TX_ICR Register (Address = 0x36) [Default = 0x00]

CSI_TX_ICR is shown in Table 5-72.

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CSI Transmit Interrupt Control Register

Table 5-72. CSI_TX_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	IE_RX_PORT_INT	R/W	0x0	RX Port Interrupt Enable Enable interrupt based on receiver port interrupt for the RX Ports being forwarded to the CSI Transmit Port.
3	IE_CSI_SYNC_ERROR	R/W	0x0	CSI Sync Error interrupt Enable Enable interrupt on CSI Synchronization enable.
2	IE_CSI_SYNC	R/W	0x0	CSI Synchronized interrupt Enable Enable interrupts on CSI Transmit Port assertion of CSI Synchronized Status.
1	IE_CSI_PASS_ERROR	R/W	0x0	CSI RX Pass Error interrupt Enable Enable interrupt on CSI Pass Error
0	IE_CSI_PASS	R/W	0x0	CSI Pass interrupt Enable Enable interrupt on CSI Transmit Port assertion of CSI Pass.

5.6.1.56 CSI_TX_ISR Register (Address = 0x37) [Default = 0x00]

CSI_TX_ISR is shown in Table 5-73.

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CSI Transmit Interrupt Status Register

Table 5-73. CSI_TX_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	IS_RX_PORT_INT	R	0x0	RX Port Interrupt A Receiver port interrupt has been generated for one of the RX Ports being forwarded to the CSI Transmit Port. A read of the associated port receive status registers clears this interrupt. See the PORT_ISR_HI and PORT_ISR_LO registers for details.
3	IS_CSI_SYNC_ERROR	RC	0x0	CSI Sync Error interrupt A synchronization error has been detected for multiple video stream inputs to the CSI Transmitter.
2	IS_CSI_SYNC	RC	0x0	CSI Synchronized interrupt CSI Transmit Port assertion of CSI Synchronized Status. Current status for CSI Sync can be read from the TX_PORT_SYNC flag in the CSI_STS register.
1	IS_CSI_PASS_ERROR	RC	0x0	CSI RX Pass Error interrupt A deassertion of CSI Pass has been detected on one of the RX Ports being forwarded to the CSI Transmit Port
0	IS_CSI_PASS	RC	0x0	CSI Pass interrupt CSI Transmit Port assertion of CSI Pass detected. Current status for the CSI Pass indication can be read from the TX_PORT_PASS flag in the CSI_STS register

5.6.1.57 SFILTER_CFG Register (Address = 0x41) [Default = 0xA3]

SFILTER_CFG is shown in Table 5-74.

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SFILTER Configuration

Table 5-74. SFILTER_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	SFILTER_MAX	R/W	0xA	SFILTER Maximum setting This field controls the maximum SFILTER setting. Allowed values are 0-12 with 6 being the mid point. These values are used during AEQ adaption, but not with dynamic SFILTER control.
3:0	SFILTER_MIN	R/W	0x3	SFILTER Maximum setting This field controls the maximum SFILTER setting. Allowed values are 0-12, where 6 is the mid point. These values are used during AEQ adaption, but not with dynamic SFILTER control.

5.6.1.58 AEQ_CTL Register (Address = 0x42) [Default = 0x01]

AEQ_CTL is shown in Table 5-75.

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AEQ Control

Table 5-75. AEQ_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	AEQ_ERR_CTL	R/W	0x0	AEQ Error Control Setting any of these bits enables FPD3 error checking during the Adaptive Equalization process. Errors are accumulated over 1/2 of the period of the timer set by the ADAPTIVE_EQ_RELOCK_TIME filed in the AEQ_TEST register. If the number of errors is greater than the programmed threshold (AEQ_ERR_THOLD), the AEQ attempts to increase the EQ setting. The errors can also be checked as part of EQ setting validation if AEQ_2STEP_EN is set. The following errors are checked based on this three bit field: [2] FPD3 clk1/clk0 errors [1] Encoding sequence errors [0] Parity errors
3	RESERVED	R	0x0	Reserved
2	AEQ_2STEP_EN	R/W	0x0	AEQ 2-step enable This bit enables a two-step operation as part of the Adaptive EQ algorithm. If disabled, the state machine waits for a programmed period of time, then check status to determine if setting is valid. If enabled, the state machine waits for 1/2 the programmed period, then check for errors over an additional 1/2 the programmed period. If errors occur during the 2nd step, the state machine immediately moves to the next setting. 0: Wait for full programmed delay, then check instantaneous lock value 1: Wait for 1/2 programmed time, then check for errors over 1/2 programmed time. The programmed time is controlled by the ADAPTIVE_EQ_RELOCK_TIME field in the AEQ_TEST register
1	AEQ_OUTER_LOOP	R/W	0x0	AEQ outer loop control This bit controls whether the Equalizer or SFILTER adaption is the outer loop when the AEQ adaption includes SFILTER adaption. 0: AEQ is inner loop, SFILTER is outer loop 1: AEQ is outer loop, SFILTER is inner loop
0	AEQ_SFILTER_EN	R/W	0x1	Enable SFILTER Adaption with AEQ Setting this bit allows SFILTER adaption as part of the Adaptive Equalizer algorithm.

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5.6.1.59 AEQ_ERR_THOLD Register (Address = 0x43) [Default = 0x01]

AEQ_ERR_THOLD is shown in Table 5-76.

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AEQ Error Threshold

Table 5-76. AEQ_ERR_THOLD Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	AEQ_ERR_THRESHOLD	R/W	0x1	AEQ Error Threshold This register controls the error threshold to determine when to re-adapt the EQ settings. This register must not be programmed to a value of 0.

5.6.1.60 FPD3_PORT_SEL Register (Address = 0x4C) [Default = 0x00]

FPD3_PORT_SEL is shown in Table 5-77.

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Table 5-77. FPD3_PORT_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PHYS_PORT_NUM	R	0x0	Physical port number This field porvides the physical port connection when reading from a remote device via the Bidirectional Control Channel. When accessed via local I2C interfaces, the value returned is always 0. When accessed via Bidirectional Control Channel, the value returned is the port number of the Receive port connection.
5:4	RX_READ_PORT	R/W	0x0	Select RX port for register read This field selects one of the four RX port register blocks for readback. This applies to all paged FPD3 Receiver port registers. 00: Port 0 registers 01: Port 1 registers 10: Port 2 registers 11: Port 3 registers When accessed via local I2C interfaces, the default setting is 0. When accessed via Bidirectional Control Channel, the default value is the port number of the Receive port connection.
3	RX_WRITE_PORT_3	R/W	0x0	Write Enable for RX port 3 registers This bit enables writes to RX port 3 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 3.
2	RX_WRITE_PORT_2	R/W	0x0	Write Enable for RX port 2 registers This bit enables writes to RX port 2 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 2.
1	RX_WRITE_PORT_1	R/W	0x0	Write Enable for RX port 1 registers This bit enables writes to RX port 1 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 1.

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Table 5-77. FPD3_PORT_SEL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	RX_WRITE_PORT_0	R/W	0x0	Write Enable for RX port 0 registers This bit enables writes to RX port 0 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 0.

5.6.1.61 RX_PORT_STS1 Register (Address = 0x4D) [Default = 0x00]

RX_PORT_STS1 is shown in Table 5-78.

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Table 5-78. RX_PORT_STS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RX_PORT_NUM	R	0x0	RX Port Number This read-only field indicates the number of the currently selected RX read port.
5	BCC_CRC_ERROR	RC	0x0	Bidirectional Control Channel CRC Error Detected This bit indicates a CRC error has been detected in the forward control channel. If this bit is set, an error can have occurred in the control channel operation. This bit is cleared on read.
4	LOCK_STS_CHG	RC	0x0	Lock Status Changed This bit is set if a change in receiver lock status has been detected since the last read of this register. Current lock status is available in the LOCK_STS bit of this register This bit is cleared on read.
3	BCC_SEQ_ERROR	RC	0x0	Bidirectional Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in the forward control channel. If this bit is set, an error can have occurred in the control channel operation. This bit is cleared on read.
2	PARITY_ERROR	R	0x0	FPD3 parity errors detected This flag is set when the number of parity errors detected is greater than the threshold programmed in the PAR_ERR_THOLD registers. 1: Number of FPD3 parity errors detected is greater than the threshold 0: Number of FPD3 parity errors is below the threshold This bit is cleared when the RX_PAR_ERR_HI/LO registers are cleared. This bit is cleared on read.
1	PORT_PASS	R	0x0	Receiver PASS indication This bit indicates the current status of the Receiver PASS indication. The requirements for setting the Receiver PASS indication are controlled by the PORT_PASS_CTL register. 1: Receive input has met PASS criteria 0: Receive input does not meet PASS criteria
0	LOCK_STS	R	0x0	FPD-Link III receiver is locked to incoming data 1: Receiver is locked to incoming data 0: Receiver is not locked

5.6.1.62 RX_PORT_STS2 Register (Address = 0x4E) [Default = 0x00]

RX_PORT_STS2 is shown in Table 5-79.

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Table 5-79. RX_PORT_STS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_LEN_UNSTABLE	RC	0x0	Line Length Unstable If set, this bit indicates the line length was detected as unstable during a previous video frame. The line length is considered to be stable if all the lines in the video frame have the same length. This flag remains set until read.
6	LINE_LEN_CHG	RC	0x0	Line Length Changed 1: Change of line length detected 0: Change of line length not detected This bit is cleared on read.
5	FPD3_ENCODE_ERROR	RC	0x0	FPD3 Encoder error detected If set, this flag indicates an error in the FPD-Link III encoding has been detected by the FPD-Link III receiver. This bit is cleared on read. Note, to detect FPD3 Encoder errors, the LINK_ERROR_COUNT must be enabled with a LINK_ERR_THRESH value greater than 1. Otherwise, the loss of Receiver Lock prevents detection of the Encoder error.
4	BUFFER_ERROR	RC	0x0	Packet buffer error detected. If this bit is set, an overflow condition has occurred on the packet buffer FIFO. 1: Packet Buffer error detected 0: No Packet Buffer errors detected This bit is cleared on read.
3	RESERVED	R	0x0	Reserved
2	FREQ_STABLE	R	0x0	FPD3 Frequency measurement stable Indicates the FPD3 input clock frequency is stable. Setting of this flag is dependent on the stability control settings in the FREQ_DET_CTL register.
1	NO_FPD3_CLK	R	0x0	No FPD-Link III input clock detected When set, this bit indicates that no FPD3 Clock has been detected. This bit is set if the input frequency is below the setting programmed in the FREQ_LO_THR setting in the FREQ_DET_CTL register.
0	LINE_CNT_CHG	RC	0x0	Line Count Changed 1: Change of line count detected 0: Change of line count not detected This bit is cleared on read.

5.6.1.63 RX_FREQ_HIGH Register (Address = 0x4F) [Default = 0x00]

RX_FREQ_HIGH is shown in Table 5-80.

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Table 5-80. RX_FREQ_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FREQ_CNT_HIGH	R	0x0	Frequency Counter High Byte (MHz) The Frequency counter reports the measured frequency for the FPD3 Receiver. This portion of the field is the integer value in MHz.

5.6.1.64 RX_FREQ_LOW Register (Address = 0x50) [Default = 0x00]

RX_FREQ_LOW is shown in Table 5-81.

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Table 5-81. RX_FREQ_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FREQ_CNT_LOW	R	0x0	Frequency Counter Low Byte (1/256MHz) The Frequency counter reports the measured frequency for the FPD3 Receiver. This portion of the field is the fractional value in 1/256MHz.

5.6.1.65 RX_PAR_ERR_HI Register (Address = 0x55) [Default = 0x00]

RX_PAR_ERR_HI is shown in Table 5-82.

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Table 5-82. RX_PAR_ERR_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PAR_ERROR_BYTE_1	R	0x0	Number of FPD3 parity errors – 8 most significant bits The parity error counter registers return the number of data parity errors that have been detected on the FPD3 Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX PARITY CHECKER ENABLE bit in register 0x2 prior to reading the parity error count registers. This register is cleared upon reading the RX_PAR_ERR_LO register. This register is cleared on setting the RX PARITY CHECKER ENABLE bit in register 0x2

5.6.1.66 RX_PAR_ERR_LO Register (Address = 0x56) [Default = 0x00]

RX_PAR_ERR_LO is shown in Table 5-83.

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Table 5-83. RX_PAR_ERR_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PAR_ERROR_BYTE_0	RC	0x0	Number of FPD3 parity errors – 8 least significant bits The parity error counter registers return the number of data parity errors that have been detected on the FPD3 Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX PARITY CHECKER ENABLE bit in register 0x2 prior to reading the parity error count registers. This register is cleared on read. This register is cleared on setting the RX PARITY CHECKER ENABLE bit in register 0x2

5.6.1.67 BIST_ERR_COUNT Register (Address = 0x57) [Default = 0x00]

BIST_ERR_COUNT is shown in Table 5-84.

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Table 5-84. BIST_ERR_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BIST_ERROR_COUNT	R	0x0	Bist Error Count Returns BIST error count

5.6.1.68 BCC_CONFIG Register (Address = 0x58) [Default = 0x1X]

BCC_CONFIG is shown in Table 5-85.

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Table 5-85. BCC_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7	I2C_PASS_THROUGH_ALL	R/W	0x0	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
6	I2C_PASS_THROUGH	R/W	0x0	I2C Pass-Through to Serializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled
5	AUTO_ACK_ALL	R/W	0x0	Automatically Acknowledge all I2C writes independent of the forward channel lock state or status of the remote Acknowledge 1: Enable 0: Disable
4	BC_ALWAYS_ON	R/W	0x1	Back channel enable 1: Back channel is always enabled independent of I2C_PASS_THROUGH and I2C_PASS_THROUGH_ALL 0: Back channel enable requires setting of either I2C_PASS_THROUGH and I2C_PASS_THROUGH_ALL This bit can only be written via a local I2C Controller.
3	BC_CRC_GENERATOR_ENABLE	R/W	0x1	Back Channel CRC Generator Enable 0: Disable 1: Enable
2:0	BC_FREQ_SELECT	R/W	0x0	Back Channel Frequency Select 000: 2.5Mbps (default for DS90UB913 compatibility) 001: 1.5625Mbps 010 - 111: Reserved Note that changing this setting can result in some errors on the back channel for a short period of time. If set over the control channel, the Deserializer must first be programmed to Auto-Ack operation to avoid a control channel timeout due to lack of response from the Serializer.

5.6.1.69 DATAPATH_CTL1 Register (Address = 0x59) [Default = 0x00]

DATAPATH_CTL1 is shown in Table 5-86.

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Table 5-86. DATAPATH_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	OVERRIDE_FC_CONFIG	R/W	0x0	1: Disable loading of the DATAPATH_CTL registers from the forward channel, keeping locally written values intact 0: Allow forward channel loading of DATAPATH_CTL registers
6:2	RESERVED	R	0x0	Reserved
1:0	FC_GPIO_EN	R/W	0x0	Forward Channel GPIO Enable Configures the number of enabled forward channel GPIOs 00: GPIOs disabled 01: One GPIO 10: Two GPIOs 11: Four GPIOs This field is normally loaded from the remote serializer. This field can be overwritten if the OVERRIDE_FC_CONFIG bit in this register is 1.

5.6.1.70 DATAPATH_CTL2 Register (Address = 0x5A) [Default = 0x00]

DATAPATH_CTL2 is shown in Table 5-87.

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Table 5-87. DATAPATH_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RESERVED	R	0x0	Reserved This field is normally loaded from the remote serializer. This field can be overwritten if the OVERRIDE_FC_CONFIG bit in the DATAPATH_CTL0 register is 1.

5.6.1.71 SER_ID Register (Address = 0x5B) [Default = 0x00]

SER_ID is shown in Table 5-88.

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Table 5-88. SER_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SER_ID	R/W	0x0	Remote Serializer ID This field is normally loaded automatically from the remote Serializer.
0	FREEZE_DEVICE_ID	R/W	0x0	Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID is frozen at the value written.

5.6.1.72 SER_ALIAS_ID Register (Address = 0x5C) [Default = 0x00]

SER_ALIAS_ID is shown in Table 5-89.

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Table 5-89. SER_ALIAS_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SER_ALIAS_ID	R/W	0x0	7-bit Remote Serializer Alias ID Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction is remapped to the address specified in the Target ID register. A value of 0 in this field disables access to the remote I2C Target.
0	SER_AUTO_ACK	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Serializer independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

5.6.1.73 TARGET_ID_0 Register (Address = 0x5D) [Default = 0x00]

TARGET_ID_0 is shown in Table 5-90.

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Table 5-90. TARGET_ID_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID0	R/W	0x0	7-bit Remote Target Device ID 0 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID0, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

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5.6.1.74 TARGET_ID_1 Register (Address = 0x5E) [Default = 0x00]

TARGET_ID_1 is shown in Table 5-91.

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Table 5-91. TARGET_ID_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID1	R/W	0x0	7-bit Remote Target Device ID 1 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID1, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

5.6.1.75 TARGET_ID_2 Register (Address = 0x5F) [Default = 0x00]

TARGET_ID_2 is shown in Table 5-92.

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Table 5-92. TARGET_ID_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID2	R/W	0x0	7-bit Remote Target Device ID 2 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID2, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

5.6.1.76 TARGET_ID_3 Register (Address = 0x60) [Default = 0x00]

TARGET_ID_3 is shown in Table 5-93.

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Table 5-93. TARGET_ID_3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID3	R/W	0x0	7-bit Remote Target Device ID 3 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID3, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

5.6.1.77 TARGET_ID_4 Register (Address = 0x61) [Default = 0x00]

TARGET_ID_4 is shown in Table 5-94.

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Table 5-94. TARGET_ID_4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID4	R/W	0x0	7-bit Remote Target Device ID 4 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID4, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

5.6.1.78 TARGET_ID_5 Register (Address = 0x62) [Default = 0x00]

TARGET_ID_5 is shown in Table 5-95.

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Table 5-95. TARGET_ID_5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID5	R/W	0x0	7-bit Remote Target Device ID 5 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID5, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

5.6.1.79 TARGET_ID_6 Register (Address = 0x63) [Default = 0x00]

TARGET_ID_6 is shown in Table 5-96.

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Table 5-96. TARGET_ID_6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID6	R/W	0x0	7-bit Remote Target Device ID 6 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID6, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

5.6.1.80 TARGET_ID_7 Register (Address = 0x64) [Default = 0x00]

TARGET_ID_7 is shown in Table 5-97.

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Table 5-97. TARGET_ID_7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID7	R/W	0x0	7-bit Remote Target Device ID 7 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID7, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

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5.6.1.81 TARGET_ALIAS_0 Register (Address = 0x65) [Default = 0x00]

TARGET_ALIAS_0 is shown in Table 5-98.

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Table 5-98. TARGET_ALIAS_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID0	R/W	0x0	7-bit Remote Target Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID0 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_0	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 0 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

5.6.1.82 TARGET_ALIAS_1 Register (Address = 0x66) [Default = 0x00]

TARGET_ALIAS_1 is shown in Table 5-99.

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Table 5-99. TARGET_ALIAS_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID1	R/W	0x0	7-bit Remote Target Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID1 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_1	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 1 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

5.6.1.83 TARGET_ALIAS_2 Register (Address = 0x67) [Default = 0x00]

TARGET_ALIAS_2 is shown in Table 5-100.

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Table 5-100. TARGET_ALIAS_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID2	R/W	0x0	7-bit Remote Target Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID2 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_2	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 2 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

5.6.1.84 TARGET_ALIAS_3 Register (Address = 0x68) [Default = 0x00]

TARGET_ALIAS_3 is shown in Table 5-101.

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Table 5-101. TARGET_ALIAS_3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID3	R/W	0x0	7-bit Remote Target Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID3 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_3	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 3 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

5.6.1.85 TARGET_ALIAS_4 Register (Address = 0x69) [Default = 0x00]

TARGET_ALIAS_4 is shown in Table 5-102.

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Table 5-102. TARGET_ALIAS_4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID4	R/W	0x0	7-bit Remote Target Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID4 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_4	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 4 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

5.6.1.86 TARGET_ALIAS_5 Register (Address = 0x6A) [Default = 0x00]

TARGET_ALIAS_5 is shown in Table 5-103.

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Table 5-103. TARGET_ALIAS_5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID5	R/W	0x0	7-bit Remote Target Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID5 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_5	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 5 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

5.6.1.87 TARGET_ALIAS_6 Register (Address = 0x6B) [Default = 0x00]

TARGET_ALIAS_6 is shown in Table 5-104.

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Table 5-104. TARGET_ALIAS_6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID6	R/W	0x0	7-bit Remote Target Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID6 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_6	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 6 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

5.6.1.88 TARGET_ALIAS_7 Register (Address = 0x6C) [Default = 0x00]

TARGET_ALIAS_7 is shown in Table 5-105.

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Table 5-105. TARGET_ALIAS_7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID7	R/W	0x0	7-bit Remote Target Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID7 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_7	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 7 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

5.6.1.89 PORT_CONFIG Register (Address = 0x6D) [Default = 0x7X]

PORT_CONFIG is shown in Table 5-106.

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Table 5-106. PORT_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	DISCARD_1ST_LINE_ON_ERR	R/W	0x1	In RAW Mode, Discard first video line if FV to LV setup time is not met. 0: Forward truncated 1st video line 1: Discard truncated 1st video line
2	RESERVED	R	X	Reserved
1:0	FPD3_MODE	R/W	0x0	FPD3 Input Mode 00: Reserved 01: RAW12 Mode LF (DS90UB913A-Q1 / DS90UB933-Q1 compatible) 10: RAW12 Mode HF (DS90UB913A-Q1 / DS90UB933-Q1 compatible) 11: RAW10 Mode (DS90UB913A-Q1 / DS90UB933-Q1 compatible)

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5.6.1.90 BC_GPIO_CTL0 Register (Address = 0x6E) [Default = 0x88]

BC_GPIO_CTL0 is shown in Table 5-107.

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Table 5-107. BC_GPIO_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	BC_GPIO1_SEL	R/W	0x8	Back channel GPIO1 Select: Determines the data sent on GPIO1 for the port back channel. 0xxx: Pin GPIOx where x is BC_GPIO1_SEL[2:0] 1000: Constant value of 0 1001: Constant value of 1 1010: FrameSync signal 1011 - 1111: Reserved
3:0	BC_GPIO0_SEL	R/W	0x8	Back channel GPIO0 Select: Determines the data sent on GPIO0 for the port back channel. 0xxx: Pin GPIOx where x is BC_GPIO0_SEL[2:0] 1000: Constant value of 0 1001: Constant value of 1 1010: FrameSync signal 1011 - 1111: Reserved

5.6.1.91 BC_GPIO_CTL1 Register (Address = 0x6F) [Default = 0x88]

BC_GPIO_CTL1 is shown in Table 5-108.

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Table 5-108. BC_GPIO_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	BC_GPIO3_SEL	R/W	0x8	Back channel GPIO3 Select: Determines the data sent on GPIO3 for the port back channel. 0xxx: Pin GPIOx where x is BC_GPIO3_SEL[2:0] 1000: Constant value of 0 1001: Constant value of 1 1010: FrameSync signal 1011 - 1111: Reserved
3:0	BC_GPIO2_SEL	R/W	0x8	Back channel GPIO2 Select: Determines the data sent on GPIO2 for the port back channel. 0xxx: Pin GPIOx where x is BC_GPIO2_SEL[2:0] 1000: Constant value of 0 1001: Constant value of 1 1010: FrameSync signal 1011 - 1111: Reserved

5.6.1.92 RAW10_ID Register (Address = 0x70) [Default = 0x2B]

RAW10_ID is shown in Table 5-109.

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Table 5-109. RAW10_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RAW10_VC	R/W	0x0	RAW10 Mode Virtual Channel This field configures the CSI Virtual Channel assigned to the port when receiving RAW10 data. The field value defaults to the FPD-Link III receive port number (0, 1, 2, or 3)

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Table 5-109. RAW10_ID Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5:0	RAW10_DT	R/W	0x2B	RAW10 Data Type This field configures the CSI data type used in RAW10 mode. The default of 0x2B matches the CSI specification.

5.6.1.93 RAW12_ID Register (Address = 0x71) [Default = 0x2C]

RAW12_ID is shown in Table 5-110.

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Table 5-110. RAW12_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RAW12_VC	R/W	0x0	RAW12 Mode Virtual Channel This field configures the CSI Virtual Channel assigned to the port when receiving RAW12 data. The field value defaults to the FPD-Link III receive port number (0, 1, 2, or 3)
5:0	RAW12_DT	R/W	0x2C	RAW12 Data Type This field configures the CSI data type used in RAW12 mode. The default of 0x2C matches the CSI specification.

5.6.1.94 LINE_COUNT_1 Register (Address = 0x73) [Default = 0x00]

LINE_COUNT_1 is shown in Table 5-111.

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Table 5-111. LINE_COUNT_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_COUNT_HI	R	0x0	High byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value is frozen until read.

5.6.1.95 LINE_COUNT_0 Register (Address = 0x74) [Default = 0x00]

LINE_COUNT_0 is shown in Table 5-112.

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Table 5-112. LINE_COUNT_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_COUNT_LO	R	0x0	Low byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value is frozen until read. In addition, when reading the LINE_COUNT registers, the LINE_COUNT_LO is latched upon reading LINE_COUNT_HI to ensure consistency between the two portions of the Line Count.

5.6.1.96 LINE_LEN_1 Register (Address = 0x75) [Default = 0x00]

LINE_LEN_1 is shown in Table 5-113.

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Table 5-113. LINE_LEN_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_LEN_HI	R	0x0	High byte of Line Length The Line Length reports the line length recorded during the most recent video frame. If line length is not stable during the frame, this register reports the length of the last line in the video frame. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value is frozen until read.

5.6.1.97 LINE_LEN_0 Register (Address = 0x76) [Default = 0x00]

LINE_LEN_0 is shown in Table 5-114.

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Table 5-114. LINE_LEN_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_LEN_LO	R	0x0	Low byte of Line Length The Line Length reports the lenth of the most recent video line. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value is frozen until read. In addition, when reading the LINE_LEN registers, the LINE_LEN_LO is latched upon reading LINE_LEN_HI to ensure consistency between the two portions of the Line Length.

5.6.1.98 FREQ_DET_CTL Register (Address = 0x77) [Default = 0xC5]

FREQ_DET_CTL is shown in Table 5-115.

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Table 5-115. FREQ_DET_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	FREQ_HYST	R/W	0x3	Frequency Detect Hysteresis: The Frequency detect hysteresis controls reporting of the FPD3 Clock frequency stability via the FREQ_STABLE status in the RX_PORT_STS2 register. The frequency is considered stable when the frequency remains within a range of +/- the FREQ_HYST value from the previous measurement. The FREQ_HYST setting is in MHz.
5:4	FREQ_STABLE_THR	R/W	0x0	Frequency Stability Threshold: The Frequency detect circuit can be used to detect a stable clock frequency. The Stability Threshold determines the amount of time required for the clock frequency to stay within the FREQ_HYST range to be considered stable: 00: 40us 01: 80us 10: 320us 11: 1.28ms
3:0	FREQ_LO_THR	R/W	0x5	Frequency Low Threshold

5.6.1.99 MAILBOX_1 Register (Address = 0x78) [Default = 0x00]

MAILBOX_1 is shown in Table 5-116.

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Table 5-116. MAILBOX_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MAILBOX_0	R/W	0x0	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C controllers on opposite ends of the link.

5.6.1.100 MAILBOX_2 Register (Address = 0x79) [Default = 0x01]

MAILBOX_2 is shown in Table 5-117.

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Table 5-117. MAILBOX_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MAILBOX_1	R/W	0x1	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C controllers on opposite ends of the link.

5.6.1.101 PORT_CONFIG2 Register (Address = 0x7C) [Default = 0x20]

PORT_CONFIG2 is shown in Table 5-118.

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Table 5-118. PORT_CONFIG2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RAW10_8BIT_CTL	R/W	0x0	Raw10 8-bit mode When Raw10 Mode is enabled for the port, the input data is processed as 8-bit data and packed accordingly for transmission over CSI. 00: Normal Raw10 Mode 01: Reserved 10: 8-bit processing using upper 8 bits 11: 8-bit processing using lower 8 bits
5	DISCARD_ON_PAR_ERR	R/W	0x1	Discard frames on Parity Error 0: Forward packets with parity errors 1: Truncate Frames if a parity error is detected
4	DISCARD_ON_LINE_SIZE	R/W	0x0	Discard frames on Line Size 0: Allow changes in Line Size within packets 1: Truncate Frames if a change in line size is detected
3	DISCARD_ON_FRAME_SIZE	R/W	0x0	Discard frames on change in Frame Size When enabled, a change in the number of lines in a frame results in truncation of the packet. The device resumes forwarding video frames based on the PASS_THRESHOLD setting in the PORT_PASS_CTL register. 0: Allow changes in Frame Size 1: Truncate Frames if a change in frame size is detected
2	RESERVED	R	0x0	Reserved
1	LV_POLARITY	R/W	0x0	LineValid Polarity This register indicates the expected polarity for the LineValid indication received in Raw mode. 1: LineValid is low for the duration of the video line 0: LIneValid is high for the duration of the video line

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Table 5-118. PORT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	FV_POLARITY	R/W	0x0	FrameValid Polarity This register indicates the expected polarity for the FrameValid indication received in Raw mode. 1: FrameValid is low for the duration of the video frame 0: FrameValid is high for the duration of the video frame

5.6.1.102 PORT_PASS_CTL Register (Address = 0x7D) [Default = 0x00]

PORT_PASS_CTL is shown in Table 5-119.

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Port Pass Control Register

Table 5-119. PORT_PASS_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	PASS_DISCARD_EN	R/W	0x0	Pass Discard Enable Discard packets if PASS is not indicated. 0: Ignore PASS for forwarding packets 1: Discard packets when PASS is not true
6	RESERVED	R	0x0	Reserved
5	PASS_LINE_CNT	R/W	0x0	Pass Line Count Control This register controls whether the device includes line count in qualification of the Pass indication: 0: Don't check line count 1: Check line count When checking line count, Pass is deasserted upon detection of a change in the number of video lines per frame. Pass is not reasserted until the PASS_THRESHOLD setting is met.
4	PASS_LINE_SIZE	R/W	0x0	Pass Line Size Control This register controls whether the device includes line size in qualification of the Pass indication: 0: Don't check line size 1: Check line size When checking line size, Pass is deasserted upon detection of a change in video line size. Pass is not reasserted until the PASS_THRESHOLD setting is met.
3	PASS_PARITY_ERR	R/W	0x0	Parity Error Mode If this bit is set to 0, the port Pass indication is deasserted for every parity error detected on the FPD3 Receive interface. If this bit is set to a 1, the port Pass indication is cleared on a parity error and remain clear until the PASS_THRESHOLD is met.
2	PASS_WDOG_DIS	R/W	0x0	RX Port Pass Watchdog disable When enabled, if the FPD Receiver does not detect a valid frame end condition within two video frame periods, the Pass indication is deasserted. The watchdog timer does not have any effect if the PASS_THRESHOLD is set to 0. 0: Enable watchdog timer for RX Pass 1: Disable watchdog timer for RX Pass
1:0	PASS_THRESHOLD	R/W	0x0	Pass Threshold Register This register controls the number of valid frames before asserting the port Pass indication. If set to 0, PASS is asserted after Receiver Lock detect. If non-zero, PASS is asserted following reception of the programmed number of valid frames.

5.6.1.103 IND_ACC_CTL Register (Address = 0xB0) [Default = 0x00]

IND_ACC_CTL is shown in Table 5-120.

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Table 5-120. IND_ACC_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:2	IA_SEL	R/W	0x0	Indirect Access Register Select: Selects target for register access 0000: Pattern Generator and CSI-2 Registers xxxx: RESERVED
1	IA_AUTO_INC	R/W	0x0	Indirect Access Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address automatically increments by 1
0	IA_READ	R/W	0x0	Indirect Access Read: Setting this allows generation of a read strobe to the selected register block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes are also asserted following a read of the IND_ACC_DATA register. This function is only required for blocks that need to pre-fetch register data.

5.6.1.104 IND_ACC_ADDR Register (Address = 0xB1) [Default = 0x00]

IND_ACC_ADDR is shown in Table 5-121.

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Table 5-121. IND_ACC_ADDR Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IA_ADDR	R/W	0x0	Indirect Access Register Offset: This register contains the 8-bit register offset for the indirect access.

5.6.1.105 IND_ACC_DATA Register (Address = 0xB2) [Default = 0x00]

IND_ACC_DATA is shown in Table 5-122.

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Table 5-122. IND_ACC_DATA Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IA_DATA	R/W	0x0	Indirect Access Data: Writing this register causes an indirect write of the IND_ACC_DATA value to the selected analog block register. Reading this register returns the value of the selected block register

5.6.1.106 BIST_CTL Register (Address = 0xB3) [Default = 0x08]

BIST_CTL is shown in Table 5-123.

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Table 5-123. BIST_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	BIST_OUT_MODE	R/W	0x0	BIST Output Mode 00: No toggling 01: Alternating 1/0 toggling 1x: Toggle based on BIST data
5:4	RESERVED	R	0x0	Reserved

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Table 5-123. BIST_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	BIST_PIN_CONFIG	R/W	0x1	Bist Configured through Pin. 1: Bist configured through pin. 0: Bist configured through bits 2:0 in this register
2:1	BIST_CLOCK_SOURCE	R/W	0x0	BIST Clock Source This register field selects the BIST Clock Source at the Serializer. These register bits are automatically written to the CLOCK SOURCE bits (register offset 0x14) in the Serializer after BIST is enabled. See the appropriate Serializer register descriptions for details. Note: When connected to a DS90UB913A, a setting of 0x3 can result in a clock frequency that is too slow for proper recovery.
0	BIST_EN	R/W	0x0	BIST Control 1: Enabled 0: Disabled

5.6.1.107 PAR_ERR_CTRL Register (Address = 0xB6) [Default = 0x18]

PAR_ERR_CTRL is shown in Table 5-124.

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CSI TX Clock Polarity

Table 5-124. PAR_ERR_CTRL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	PAR_ERR_CNTR_MODE	R/W	0x0	Parity Error Counter Mode 0: Clear Parity Error counter if receiver is not locked 1: Maintain Parity Error count value through loss of lock
4	DIS_LINK_PAR	R/W	0x1	Disable checking of Parity Errors when checking for FPD-Link Lock 0: Parity errors prevent assertion of forward channel lock detect (RX Lock). 1: Parity errors do NOT prevent assertion of forward channel lock detect (RX Lock). This is the default mode of the device.
3	DIS_LINKLOSS_PAR	R/W	0x1	Disable checking of Parity Errors when checking for loss of link 0: Parity errors prevent assertion of forward channel loss of link (RX Lock). 1: Parity errors do NOT prevent assertion of forward channel loss of link (RX Lock). This is the default mode of the device.
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

5.6.1.108 MODE_IDX_STS Register (Address = 0xB8) [Default = 0xXX]

MODE_IDX_STS is shown in Table 5-125.

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Table 5-125. MODE_IDX_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	IDX_DONE	R	0x1	IDX Done: If set, indicates the IDX decode has completed and latched into the IDX status bits.
6:4	IDX	R	0x0	IDX Decode 3-bit decode from IDX pin

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Table 5-125. MODE_IDX_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	MODE_DONE	R	0x1	MODE Done: If set, indicates the MODE decode has completed and latched into the MODE status bits.
2:0	MODE	R	0x0	MODE Decode 3-bit decode from MODE pin

5.6.1.109 LINK_ERROR_COUNT Register (Address = 0xB9) [Default = 0x03]

LINK_ERROR_COUNT is shown in Table 5-126.

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Table 5-126. LINK_ERROR_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	LINK_SFIL_WAIT	R/W	0x0	During SFILTER adaption, setting this bit causes the Lock detect circuit to ignore errors during the SFILTER wait period after the SFILTER control is updated. 1: Errors during SFILTER Wait period are ignored 0: Errors during SFILTER Wait period are not ignored and can cause loss of Lock
4	LINK_ERR_COUNT_EN	R/W	0x0	Enable serial link data integrity error count 1: Enable error count 0: DISABLE
3:0	LINK_ERR_THRESH	R/W	0x3	Link error count threshold. The Link Error Counter monitors the forward channel link and determines when link is dropped. If the error counter is enabled, the deserializer loses lock once the error counter reaches the LINK_ERR_THRESH value. If the link error counter is disabled, the deserializer loses lock after one error. The control bits in PAR_ERR_CTRL register can be used to disable error conditions individually.

5.6.1.110 FV_MIN_TIME Register (Address = 0xBC) [Default = 0x80]

FV_MIN_TIME is shown in Table 5-127.

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Table 5-127. FV_MIN_TIME Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAME_VALID_MIN	R/W	0x80	Frame Valid Minimum Time This register controls the minimum time the FrameValid (FV) must be active before the Raw mode FPD3 receiver generates a FrameStart packet. Duration is in FPD3 clock periods.

5.6.1.111 GPIO_PD_CTL Register (Address = 0xBE) [Default = 0x00]

GPIO_PD_CTL is shown in Table 5-128.

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GPIO Pulldown control register

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Table 5-128. GPIO_PD_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO7_PD_DIS	R/W	0x0	GPI7 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor is also disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
6	GPIO6_PD_DIS	R/W	0x0	GPIO6 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor is also disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
5	GPIO5_PD_DIS	R/W	0x0	GPIO5 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor is also disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
4	GPIO4_PD_DIS	R/W	0x0	GPIO4 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor is also disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
3	GPIO3_PD_DIS	R/W	0x0	GPIO3 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor is also disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
2	GPIO2_PD_DIS	R/W	0x0	GPIO2 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor is also disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
1	GPIO1_PD_DIS	R/W	0x0	GPIO1 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor is also disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
0	GPIO0_PD_DIS	R/W	0x0	GPIO0 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor is also disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor

5.6.1.112 PORT_DEBUG Register (Address = 0xD0) [Default = 0x00]

PORT_DEBUG is shown in Table 5-129.

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Table 5-129. PORT_DEBUG Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	SER_BIST_ACT	R	0x0	Serializer BIST active This register indicates the Serializer is in BIST mode. If the Deserializer is not in BIST mode, this could indicate an error condition.
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

5.6.1.113 AEQ_CTL2 Register (Address = 0xD2) [Default = 0x84]

AEQ_CTL2 is shown in Table 5-130.

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Table 5-130. AEQ_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ADAPTIVE_EQ_RELOCK_TIME	R/W	0x4	Time to wait for lock before incrementing the EQ to next setting 000: 164us 001: 328us 010: 655us 011: 1.31ms 100: 2.62ms 101: 5.24ms 110: 10.5ms 111: 21.0ms
4	AEQ_1ST_LOCK_MODE	R/W	0x0	AEQ First Lock Mode This register bit controls the Adaptive Equalizer algorithm operation at initial Receiver Lock. 0: Initial AEQ lock can occur at any value 1: Initial Receiver lock restarts AEQ at 0, providing a more deterministic initial AEQ value
3	AEQ_RESTART	RH/W1S	0x0	Set high to restart AEQ adaptation from initial value. This bit is self clearing. Adaption is restarted.
2	SET_AEQ_FLOOR	R/W	0x1	AEQ adaptation starts from a pre-set floor value rather than from zero - good in long cable situations
1:0	RESERVED	R	0x0	Reserved

5.6.1.114 AEQ_STATUS Register (Address = 0xD3) [Default = 0x00]

AEQ_STATUS is shown in Table 5-131.

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Adaptive Equalizer Status Register

Table 5-131. AEQ_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	

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Table 5-131. AEQ_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5:0	EQ_STATUS	R	0x0	Adaptive EQ Status

5.6.1.115 AEQ_BYPASS Register (Address = 0xD4) [Default = 0x60]

AEQ_BYPASS is shown in Table 5-132.

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Adaptive Equalizer Bypass Register

Table 5-132. AEQ_BYPASS Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	EQ_STAGE_1_SELECT_VALUE	R/W	0x3	EQ select value[5:3] - Used if adaptive EQ is bypassed.
4	AEQ_LOCK_MODE	R/W	0x0	Adaptive Equalizer lock mode When set to a 1, Receiver Lock status requires the Adaptive Equalizer to complete adaption. When set to a 0, Receiver Lock is based only on the Lock circuit itself. AEQ can not have stabilized.
3:1	EQ_STAGE_2_SELECT_VALUE	R/W	0x0	EQ select value [2:0] - Used if adaptive EQ is bypassed.
0	ADAPTIVE_EQ_BYPASS	R/W	0x0	1: Disable adaptive EQ 0: Enable adaptive EQ

5.6.1.116 AEQ_MIN_MAX Register (Address = 0xD5) [Default = 0xF8]

AEQ_MIN_MAX is shown in Table 5-133.

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Adaptive Equalizer Min/Max register

Table 5-133. AEQ_MIN_MAX Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	AEQ_MAX	R/W	0xF	Adaptive Equalizer Maximum value This register sets the maximum value for the Adaptive EQ algorithm.
3:0	ADAPTIVE_EQ_FLOOR_VALUE	R/W	0x8	When AEQ floor is enabled by the SET_AEQ_FLOOR register bit (0xD2[2]), the starting setting is given by this register.

5.6.1.117 PORT_ICR_HI Register (Address = 0xD8) [Default = 0x00]

PORT_ICR_HI is shown in Table 5-134.

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Interrupt Control High Register This register contains the upper 8 bit controls for enabling various receive port-specific interrupts.

Table 5-134. PORT_ICR_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	IE_FPD3_ENC_ERR	R/W	0x0	Interrupt on FPD-Link III Receiver Encoding Error When enabled, an interrupt is generated on detection of an encoding error on the FPD-Link III interface for the receive port as reported in the FPD3_ENC_ERROR bit in the RX_PORT_STS2 register

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Table 5-134. PORT_ICR_HI Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	IE_BCC_SEQ_ERR	R/W	0x0	Interrupt on BCC SEQ Sequence Error When enabled, an interrupt is generated if a Sequence Error is detected for the Bidirectional Control Channel forward channel receiver as reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register.
0	IE_BCC_CRC_ERR	R/W	0x0	Interrupt on BCC CRC error detect When enabled, an interrupt is generated if a CRC error is detected on a Bidirectional Control Channel frame received over the FPD-Link III forward channel as reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register.

5.6.1.118 PORT_ICR_LO Register (Address = 0xD9) [Default = 0x00]

PORT_ICR_LO is shown in Table 5-135.

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Interrupt Control Low Register This register contains the lower 8 bit controls for enabling various receive port-specific interrupts. Interrupt status for the respective conditions are reported in the PORT_ISR_LO register.

Table 5-135. PORT_ICR_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_LINE_LEN_CHG	R/W	0x0	Interrupt on Video Line length When enabled, an interrupt is generated if the length of the video line changes. Status is reported in the LINE_LEN_CHG bit in the RX_PORT_STS2 register.
5	IE_LINE_CNT_CHG	R/W	0x0	Interrupt on Video Line count When enabled, an interrupt is generated if the number of video lines per frame changes. Status is reported in the LINE_CNT_CHG bit in the RX_PORT_STS2 register.
4	IE_BUFFER_ERR	R/W	0x0	Interrupt on Receiver Buffer Error When enabled, an interrupt is generated if the Receive Buffer overflow is detected as reported in the BUFFER_ERROR bit in the RX_PORT_STS2 register.
3	RESERVED	R	0x0	Reserved
2	IE_FPD3_PAR_ERR	R/W	0x0	Interrupt on FPD-Link III Receiver Parity Error When enabled, an interrupt is generated on detection of parity errors on the FPD-Link III interface for the receive port. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register.
1	IE_PORT_PASS	R/W	0x0	Interrupt on change in Port PASS status When enabled, an interrupt is generated on a change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register.
0	IE_LOCK_STS	R/W	0x0	Interrupt on change in Lock Status When enabled, an interrupt is generated on a change in lock status. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register.

5.6.1.119 PORT_ISR_HI Register (Address = 0xDA) [Default = 0x00]

PORT_ISR_HI is shown in Table 5-136.

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Interrupt Status High Register This register contains the upper 8 bit status of various receive port-specific interrupts.

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Table 5-136. PORT_ISR_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	IS_FPD3_ENC_ERR	R	0x0	FPD-Link III Receiver Encode Error Interrupt Status An encoding error on the FPD-Link III interface for the receive port has been detected. Status is reported in the FPD3_ENC_ERROR bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
1	IS_BCC_SEQ_ERR	R	0x0	BCC CRC Sequence Error Interrupt Status A Sequence Error has been detected for the Bidirectional Control Channel forward channel receiver. Status is reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
0	IS_BCC_CRC_ERR	R	0x0	BCC CRC error detect Interrupt Status A CRC error has been detected on a Bidirectional Control Channel frame received over the FPD-Link III forward channel. Status is reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.

5.6.1.120 PORT_ISR_LO Register (Address = 0xDB) [Default = 0x00]

PORT_ISR_LO is shown in Table 5-137.

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Interrupt Status Low Register This register contains the lower 8 bit status of various receive port-specific interrupts.

Table 5-137. PORT_ISR_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_LINE_LEN_CHG	R	0x0	Video Line Length Interrupt Status A change in video line length has been detected. Status is reported in the LINE_LEN_CHG bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
5	IS_LINE_CNT_CHG	R	0x0	Video Line Count Interrupt Status A change in number of video lines per frame has been detected. Status is reported in the LINE_CNT_CHG bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
4	IS_BUFFER_ERR	R	0x0	Receiver Buffer Error Interrupt Status A Receive Buffer overflow has been detected as reported in the BUFFER_ERROR bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
3	RESERVED	R	0x0	Reserved
2	IS_FPD3_PAR_ERR	R	0x0	FPD-Link III Receiver Parity Error Interrupt Status A parity error on the FPD-Link III interface for the receive port has been detected. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.

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Table 5-137. PORT_ISR_LO Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	IS_PORT_PASS	R	0x0	Port Valid Interrupt Status A change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
0	IS_LOCK_STS	R	0x0	Lock Interrupt Status A change in lock status has been detected. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.

5.6.1.121 FPD3_RX_ID0 Register (Address = 0xF0) [Default = 0x5F]

FPD3_RX_ID0 is shown in Table 5-138.

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Table 5-138. FPD3_RX_ID0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD3_RX_ID0	R	0x5F	FPD3_RX_ID0: First byte ID code: '_ '

5.6.1.122 FPD3_RX_ID1 Register (Address = 0xF1) [Default = 0x55]

FPD3_RX_ID1 is shown in Table 5-139.

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Table 5-139. FPD3_RX_ID1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD3_RX_ID1	R	0x55	FPD3_RX_ID1: 2nd byte of ID code: 'U '

5.6.1.123 FPD3_RX_ID2 Register (Address = 0xF2) [Default = 0x42]

FPD3_RX_ID2 is shown in Table 5-140.

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Table 5-140. FPD3_RX_ID2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD3_RX_ID2	R	0x42	FPD3_RX_ID2: 3rd byte of ID code: 'B '

5.6.1.124 FPD3_RX_ID3 Register (Address = 0xF3) [Default = 0x39]

FPD3_RX_ID3 is shown in Table 5-141.

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Table 5-141. FPD3_RX_ID3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD3_RX_ID3	R	0x39	FPD3_RX_ID3: 4th byte of ID code: '9 '

5.6.1.125 FPD3_RX_ID4 Register (Address = 0xF4) [Default = 0x36]

FPD3_RX_ID4 is shown in Table 5-142.

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Table 5-142. FPD3_RX_ID4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD3_RX_ID4	R	0x36	FPD3_RX_ID4: 5th byte of ID code: '6'

5.6.1.126 FPD3_RX_ID5 Register (Address = 0xF5) [Default = 0x34]

FPD3_RX_ID5 is shown in Table 5-143.

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Table 5-143. FPD3_RX_ID5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD3_RX_ID5	R	0x34	FPD3_RX_ID5: 6th byte of ID code: '4'

5.6.1.127 I2C_RX0_ID Register (Address = 0xF8) [Default = 0x00]

I2C_RX0_ID is shown in Table 5-144.

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Table 5-144. I2C_RX0_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RX_PORT0_ID	R/W	0x0	7-bit Receive Port 0 I2C ID Configures the decoder for detecting transactions designated for Receiver port 0 registers. This provides a simpler method of accessing device registers specifically for port 0 without having to use the paging function to select the register page. A value of 0 in this field disables the Port0 decoder.
0	RESERVED	R	0x0	Reserved

5.6.1.128 I2C_RX1_ID Register (Address = 0xF9) [Default = 0x00]

I2C_RX1_ID is shown in Table 5-145.

Return to the Summary Table.

Table 5-145. I2C_RX1_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RX_PORT1_ID	R/W	0x0	7-bit Receive Port 1 I2C ID Configures the decoder for detecting transactions designated for Receiver port 1 registers. This provides a simpler method of accessing device registers specifically for port 1 without having to use the paging function to select the register page. A value of 0 in this field disables the Port1 decoder.
0	RESERVED	R	0x0	Reserved

5.6.1.129 I2C_RX2_ID Register (Address = 0xFA) [Default = 0x00]

I2C_RX2_ID is shown in Table 5-146.

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Table 5-146. I2C_RX2_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RX_PORT2_ID	R/W	0x0	7-bit Receive Port 2 I2C ID Configures the decoder for detecting transactions designated for Receiver port 2 registers. This provides a simpler method of accessing device registers specifically for port 2 without having to use the paging function to select the register page. A value of 0 in this field disables the Port2 decoder.
0	RESERVED	R	0x0	Reserved

5.6.1.130 I2C_RX3_ID Register (Address = 0xFB) [Default = 0x00]

I2C_RX3_ID is shown in Table 5-147.

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Table 5-147. I2C_RX3_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RX_PORT3_ID	R/W	0x0	7-bit Receive Port 3 I2C ID Configures the decoder for detecting transactions designated for Receiver port 3 registers. This provides a simpler method of accessing device registers specifically for port 3 without having to use the paging function to select the register page. A value of 0 in this field disables the Port3 decoder.
0	RESERVED	R	0x0	Reserved

5.6.2 Indirect Access Registers

Several functional blocks include register sets contained in the Indirect Access map (Indirect Register Map Description); i.e. Pattern Generator, CSI-2 timing, and Analog controls. Register access is provided via an indirect access mechanism through the Indirect Access registers (IND_ACC_CTL, IND_ACC_ADDR, and IND_ACC_DATA). These registers are located at offsets 0xB0-0xB2 in the main register space.

The indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:

1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Write the data value to the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 writes additional data bytes to subsequent register offset locations

For reads, the process is as follows:

1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Read from the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 reads additional data bytes from subsequent register offset locations.

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5.6.2.1 PATGEN_And_CSI-2 Registers

Table 5-148 lists the memory-mapped registers for the PATGEN_And_CSI-2 registers. All register offset addresses not listed in Table 5-148 should be considered as reserved locations and the register contents should not be modified.

Table 5-148. PATGEN_AND_CSI-2 Registers

Address	Acronym	Register Name	Section
0x1	PGEN_CTL	PGEN_CTL	Go
0x2	PGEN_CFG	PGEN_CFG	Go
0x3	PGEN_CSI_DI	PGEN_CSI_DI	Go
0x4	PGEN_LINE_SIZE1	PGEN_LINE_SIZE1	Go
0x5	PGEN_LINE_SIZE0	PGEN_LINE_SIZE0	Go
0x6	PGEN_BAR_SIZE1	PGEN_BAR_SIZE1	Go
0x7	PGEN_BAR_SIZE0	PGEN_BAR_SIZE0	Go
0x8	PGEN_ACT_LPF1	PGEN_ACT_LPF1	Go
0x9	PGEN_ACT_LPF0	PGEN_ACT_LPF0	Go
0xA	PGEN_TOT_LPF1	PGEN_TOT_LPF1	Go
0xB	PGEN_TOT_LPF0	PGEN_TOT_LPF0	Go
0xC	PGEN_LINE_PD1	PGEN_LINE_PD1	Go
0xD	PGEN_LINE_PD0	PGEN_LINE_PD0	Go
0xE	PGEN_VBP	PGEN_VBP	Go
0xF	PGEN_VFP	PGEN_VFP	Go
0x10	PGEN_COLOR0	PGEN_COLOR0	Go
0x11	PGEN_COLOR1	PGEN_COLOR1	Go
0x12	PGEN_COLOR2	PGEN_COLOR2	Go
0x13	PGEN_COLOR3	PGEN_COLOR3	Go
0x14	PGEN_COLOR4	PGEN_COLOR4	Go
0x15	PGEN_COLOR5	PGEN_COLOR5	Go
0x16	PGEN_COLOR6	PGEN_COLOR6	Go
0x17	PGEN_COLOR7	PGEN_COLOR7	Go
0x18	PGEN_COLOR8	PGEN_COLOR8	Go
0x19	PGEN_COLOR9	PGEN_COLOR9	Go
0x1A	PGEN_COLOR10	PGEN_COLOR10	Go
0x1B	PGEN_COLOR11	PGEN_COLOR11	Go
0x1C	PGEN_COLOR12	PGEN_COLOR12	Go
0x1D	PGEN_COLOR13	PGEN_COLOR13	Go
0x1E	PGEN_COLOR14	PGEN_COLOR14	Go
0x40	CSI0_TCK_PREP	CSI0_TCK_PREP	Go
0x41	CSI0_TCK_ZERO	CSI0_TCK_ZERO	Go
0x42	CSI0_TCK_TRAIL	CSI0_TCK_TRAIL	Go
0x43	CSI0_TCK_POST	CSI0_TCK_POST	Go
0x44	CSI0_THS_PREP	CSI0_THS_PREP	Go
0x45	CSI0_THS_ZERO	CSI0_THS_ZERO	Go
0x46	CSI0_THS_TRAIL	CSI0_THS_TRAIL	Go
0x47	CSI0_THS_EXIT	CSI0_THS_EXIT	Go
0x48	CSI0_TPLX	CSI0_TPLX	Go
0x60	CSI1_TCK_PREP	CSI1_TCK_PREP	Go
0x61	CSI1_TCK_ZERO	CSI1_TCK_ZERO	Go

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Table 5-148. PATGEN_AND_CSI-2 Registers (continued)

Address	Acronym	Register Name	Section
0x62	CSI1_TCK_TRAIL	CSI1_TCK_TRAIL	Go
0x63	CSI1_TCK_POST	CSI1_TCK_POST	Go
0x64	CSI1_THS_PREP	CSI1_THS_PREP	Go
0x65	CSI1_THS_ZERO	CSI1_THS_ZERO	Go
0x66	CSI1_THS_TRAIL	CSI1_THS_TRAIL	Go
0x67	CSI1_THS_EXIT	CSI1_THS_EXIT	Go
0x68	CSI1_TPLX	CSI1_TPLX	Go

Complex bit access types are encoded to fit into small table cells. Table 5-149 shows the codes that are used for access types in this section.

Table 5-149. PATGEN_And_CSI-2 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

5.6.2.1.1 PGEN_CTL Register (Address = 0x1) [Default = 0x00]

PGEN_CTL is shown in Table 5-150.

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Pattern Generator Control Register

Table 5-150. PGEN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RESERVED	R	0x0	Reserved
0	PGEN_ENABLE	R/W	0x0	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

5.6.2.1.2 PGEN_CFG Register (Address = 0x2) [Default = 0x33]

PGEN_CFG is shown in Table 5-151.

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Pattern Generator Configuration Register

Table 5-151. PGEN_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7	PGEN_FIXED_EN	R/W	0x0	Fixed Pattern Enable Setting this bit enables Fixed Color Patterns. 0: Send Color Bar Pattern 1: Send Fixed Color Pattern
6	RESERVED	R	0x0	Reserved

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Table 5-151. PGEN_CFG Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5:4	NUM_CBARS	R/W	0x3	Number of Color Bars 00: 1 Color Bar 01: 2 Color Bars 10: 4 Color Bars 11: 8 Color Bars
3:0	BLOCK_SIZE	R/W	0x3	Block Size. For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 15.

5.6.2.1.3 PGEN_CSI_DI Register (Address = 0x3) [Default = 0x24]

PGEN_CSI_DI is shown in Table 5-152.

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Pattern Generator CSI DI Register

Table 5-152. PGEN_CSI_DI Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PGEN_CSI_VC	R/W	0x0	CSI Virtual Channel Identifier This field controls the value sent in the CSI packet for the Virtual Channel Identifier
5:0	PGEN_CSI_DT	R/W	0x24	CSI Data Type This field controls the value sent in the CSI packet for the Data Type. The default value (0x24) indicates RGB888.

5.6.2.1.4 PGEN_LINE_SIZE1 Register (Address = 0x4) [Default = 0x07]

PGEN_LINE_SIZE1 is shown in Table 5-153.

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Pattern Generator Line Size Register 1

Table 5-153. PGEN_LINE_SIZE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_SIZE[15:8]	R/W	0x7	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

5.6.2.1.5 PGEN_LINE_SIZE0 Register (Address = 0x5) [Default = 0x80]

PGEN_LINE_SIZE0 is shown in Table 5-154.

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Pattern Generator Line Size Register 0

Table 5-154. PGEN_LINE_SIZE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_SIZE[7:0]	R/W	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

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5.6.2.1.6 PGEN_BAR_SIZE1 Register (Address = 0x6) [Default = 0x00]

PGEN_BAR_SIZE1 is shown in Table 5-155.

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Pattern Generator Bar Size Register 1

Table 5-155. PGEN_BAR_SIZE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_BAR_SIZE[15:8]	R/W	0x0	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

5.6.2.1.7 PGEN_BAR_SIZE0 Register (Address = 0x7) [Default = 0xF0]

PGEN_BAR_SIZE0 is shown in Table 5-156.

Return to the Summary Table.

Pattern Generator Bar Size Register 0

Table 5-156. PGEN_BAR_SIZE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_BAR_SIZE[7:0]	R/W	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

5.6.2.1.8 PGEN_ACT_LPF1 Register (Address = 0x8) [Default = 0x01]

PGEN_ACT_LPF1 is shown in Table 5-157.

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Pattern Generator Active LPF Register 1

Table 5-157. PGEN_ACT_LPF1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_ACT_LPF[15:8]	R/W	0x1	Active Lines Per Frame Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

5.6.2.1.9 PGEN_ACT_LPF0 Register (Address = 0x9) [Default = 0xE0]

PGEN_ACT_LPF0 is shown in Table 5-158.

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Pattern Generator Active LPF Register 0

Table 5-158. PGEN_ACT_LPF0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_ACT_LPF[7:0]	R/W	0xE0	Active Lines Per Frame Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

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5.6.2.1.10 PGEN_TOT_LPF1 Register (Address = 0xA) [Default = 0x02]

PGEN_TOT_LPF1 is shown in Table 5-159.

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Pattern Generator Total LPF Register 1

Table 5-159. PGEN_TOT_LPF1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_TOT_LPF[15:8]	R/W	0x2	Total Lines Per Frame Most significant byte of the number of total lines per frame including vertical blanking

5.6.2.1.11 PGEN_TOT_LPF0 Register (Address = 0xB) [Default = 0x0D]

PGEN_TOT_LPF0 is shown in Table 5-160.

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Pattern Generator Total LPF Register 0

Table 5-160. PGEN_TOT_LPF0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_TOT_LPF[7:0]	R/W	0xD	Total Lines Per Frame Least significant byte of the number of total lines per frame including vertical blanking

5.6.2.1.12 PGEN_LINE_PD1 Register (Address = 0xC) [Default = 0x0C]

PGEN_LINE_PD1 is shown in Table 5-161.

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Pattern Generator Line Period Register 1

Table 5-161. PGEN_LINE_PD1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_PD[15:8]	R/W	0xC	Line Period Most significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds.

5.6.2.1.13 PGEN_LINE_PD0 Register (Address = 0xD) [Default = 0x67]

PGEN_LINE_PD0 is shown in Table 5-162.

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Pattern Generator Line Period Register 0

Table 5-162. PGEN_LINE_PD0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_PD[7:0]	R/W	0x67	Line Period Least significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds.

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5.6.2.1.14 PGEN_VBP Register (Address = 0xE) [Default = 0x21]

PGEN_VBP is shown in Table 5-163.

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Pattern Generator VBP Register

Table 5-163. PGEN_VBP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_VBP	R/W	0x21	Vertical Back Porch This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.

5.6.2.1.15 PGEN_VFP Register (Address = 0xF) [Default = 0x0A]

PGEN_VFP is shown in Table 5-164.

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Pattern Generator VFP Register

Table 5-164. PGEN_VFP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_VFP	R/W	0xA	Vertical Front Porch This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.

5.6.2.1.16 PGEN_COLOR0 Register (Address = 0x10) [Default = 0xAA]

PGEN_COLOR0 is shown in Table 5-165.

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Pattern Generator Color 0 Register

Table 5-165. PGEN_COLOR0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR0	R/W	0xAA	Pattern Generator Color 0 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0. For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.

5.6.2.1.17 PGEN_COLOR1 Register (Address = 0x11) [Default = 0x33]

PGEN_COLOR1 is shown in Table 5-166.

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Pattern Generator Color 1 Register

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Table 5-166. PGEN_COLOR1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR1	R/W	0x33	Pattern Generator Color 1 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1. For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.

5.6.2.1.18 PGEN_COLOR2 Register (Address = 0x12) [Default = 0xF0]

PGEN_COLOR2 is shown in Table 5-167.

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Pattern Generator Color 2 Register

Table 5-167. PGEN_COLOR2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR2	R/W	0xF0	Pattern Generator Color 2 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2. For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.

5.6.2.1.19 PGEN_COLOR3 Register (Address = 0x13) [Default = 0x7F]

PGEN_COLOR3 is shown in Table 5-168.

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Pattern Generator Color 3 Register

Table 5-168. PGEN_COLOR3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR3	R/W	0x7F	Pattern Generator Color 3 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3. For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.

5.6.2.1.20 PGEN_COLOR4 Register (Address = 0x14) [Default = 0x55]

PGEN_COLOR4 is shown in Table 5-169.

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Pattern Generator Color 4 Register

Table 5-169. PGEN_COLOR4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR4	R/W	0x55	Pattern Generator Color 4 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4. For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.

5.6.2.1.21 PGEN_COLOR5 Register (Address = 0x15) [Default = 0xCC]

PGEN_COLOR5 is shown in Table 5-170.

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Pattern Generator Color 5 Register

Table 5-170. PGEN_COLOR5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR5	R/W	0xCC	Pattern Generator Color 5 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5. For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

5.6.2.1.22 PGEN_COLOR6 Register (Address = 0x16) [Default = 0x0F]

PGEN_COLOR6 is shown in Table 5-171.

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Pattern Generator Color 6 Register

Table 5-171. PGEN_COLOR6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR6	R/W	0xF	Pattern Generator Color 6 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6. For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.

5.6.2.1.23 PGEN_COLOR7 Register (Address = 0x17) [Default = 0x80]

PGEN_COLOR7 is shown in Table 5-172.

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Pattern Generator Color 7 Register

Table 5-172. PGEN_COLOR7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR7	R/W	0x80	Pattern Generator Color 7 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7. For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.

5.6.2.1.24 PGEN_COLOR8 Register (Address = 0x18) [Default = 0x00]

PGEN_COLOR8 is shown in Table 5-173.

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Pattern Generator Color 8 Register

Table 5-173. PGEN_COLOR8 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR8	R/W	0x0	Pattern Generator Color 8 For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.

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5.6.2.1.25 PGEN_COLOR9 Register (Address = 0x19) [Default = 0x00]

PGEN_COLOR9 is shown in Table 5-174.

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Pattern Generator Color 9 Register

Table 5-174. PGEN_COLOR9 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR9	R/W	0x0	Pattern Generator Color 9 For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.

5.6.2.1.26 PGEN_COLOR10 Register (Address = 0x1A) [Default = 0x00]

PGEN_COLOR10 is shown in Table 5-175.

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Pattern Generator Color 10 Register

Table 5-175. PGEN_COLOR10 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR10	R/W	0x0	Pattern Generator Color 10 For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.

5.6.2.1.27 PGEN_COLOR11 Register (Address = 0x1B) [Default = 0x00]

PGEN_COLOR11 is shown in Table 5-176.

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Pattern Generator Color 11 Register

Table 5-176. PGEN_COLOR11 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR11	R/W	0x0	Pattern Generator Color 11 For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.

5.6.2.1.28 PGEN_COLOR12 Register (Address = 0x1C) [Default = 0x00]

PGEN_COLOR12 is shown in Table 5-177.

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Pattern Generator Color 12 Register

Table 5-177. PGEN_COLOR12 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR12	R/W	0x0	Pattern Generator Color 12 For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.

5.6.2.1.29 PGEN_COLOR13 Register (Address = 0x1D) [Default = 0x00]

PGEN_COLOR13 is shown in Table 5-178.

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Pattern Generator Color 13 Register

Table 5-178. PGEN_COLOR13 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR13	R/W	0x0	Pattern Generator Color 13 For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.

5.6.2.1.30 PGEN_COLOR14 Register (Address = 0x1E) [Default = 0x00]

PGEN_COLOR14 is shown in Table 5-179.

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Pattern Generator Color 14 Register

Table 5-179. PGEN_COLOR14 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR14	R/W	0x0	Pattern Generator Color 14 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

5.6.2.1.31 CSI0_TCK_PREP Register (Address = 0x40) [Default = 0x00]

CSI0_TCK_PREP is shown in Table 5-180.

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Table 5-180. CSI0_TCK_PREP Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_PREP_OV	R/W	0x0	Override CSI Tck-prep parameter 0: Tck-prep is automatically determined 1: Override Tck-prep with value in bits 6:0 of this register
6:0	MR_TCK_PREP	R/W	0x0	Tck-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.32 CSI0_TCK_ZERO Register (Address = 0x41) [Default = 0x00]

CSI0_TCK_ZERO is shown in Table 5-181.

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Table 5-181. CSI0_TCK_ZERO Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_ZERO_OV	R/W	0x0	Override CSI Tck-zero parameter 0: Tck-zero is automatically determined 1: Override Tck-zero with value in bits 6:0 of this register
6:0	MR_TCK_ZERO	R/W	0x0	Tck-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

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5.6.2.1.33 CSI0_TCK_TRAIL Register (Address = 0x42) [Default = 0x00]

CSI0_TCK_TRAIL is shown in Table 5-182.

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Table 5-182. CSI0_TCK_TRAIL Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_TRAIL_OV	R/W	0x0	Override CSI Tck-trail parameter 0: Tck-trail is automatically determined 1: Override Tck-trail with value in bits 6:0 of this register
6:0	MR_TCK_TRAIL	R/W	0x0	Tck-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.34 CSI0_TCK_POST Register (Address = 0x43) [Default = 0x00]

CSI0_TCK_POST is shown in Table 5-183.

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Table 5-183. CSI0_TCK_POST Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_POST_OV	R/W	0x0	Override CSI Tck-post parameter 0: Tck-post is automatically determined 1: Override Tck-post with value in bits 6:0 of this register
6:0	MR_TCK_POST	R/W	0x0	Tck-post value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.35 CSI0_THS_PREP Register (Address = 0x44) [Default = 0x00]

CSI0_THS_PREP is shown in Table 5-184.

Return to the Summary Table.

Table 5-184. CSI0_THS_PREP Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_PREP_OV	R/W	0x0	Override CSI Ths-prep parameter 0: Ths-prep is automatically determined 1: Override Ths-prep with value in bits 6:0 of this register
6:0	MR_THS_PREP	R/W	0x0	Ths-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.36 CSI0_THS_ZERO Register (Address = 0x45) [Default = 0x00]

CSI0_THS_ZERO is shown in Table 5-185.

Return to the Summary Table.

Table 5-185. CSI0_THS_ZERO Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_ZERO_OV	R/W	0x0	Override CSI Ths-zero parameter 0: Ths-zero is automatically determined 1: Override Ths-zero with value in bits 6:0 of this register

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Table 5-185. CSI0_THS_ZERO Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:0	MR_THS_ZERO	R/W	0x0	Ths-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.37 CSI0_THS_TRAIL Register (Address = 0x46) [Default = 0x00]

CSI0_THS_TRAIL is shown in Table 5-186.

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Table 5-186. CSI0_THS_TRAIL Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_TRAIL_OV	R/W	0x0	Override CSI Ths-trail parameter 0: Ths-trail is automatically determined 1: Override Ths-trail with value in bits 6:0 of this register
6:0	MR_THS_TRAIL	R/W	0x0	Ths-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.38 CSI0_THS_EXIT Register (Address = 0x47) [Default = 0x00]

CSI0_THS_EXIT is shown in Table 5-187.

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Table 5-187. CSI0_THS_EXIT Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_EXIT_OV	R/W	0x0	Override CSI Ths-exit parameter 0: Ths-exit is automatically determined 1: Override Ths-exit with value in bits 6:0 of this register
6:0	MR_THS_EXIT	R/W	0x0	Ths-exit value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.39 CSI0_TPLX Register (Address = 0x48) [Default = 0x00]

CSI0_TPLX is shown in Table 5-188.

Return to the Summary Table.

Table 5-188. CSI0_TPLX Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TPLX_OV	R/W	0x0	Override CSI Tplx parameter 0: Tplx is automatically determined 1: Override Tplx with value in bits 6:0 of this register
6:0	MR_TPLX	R/W	0x0	Tplx value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

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5.6.2.1.40 CSI1_TCK_PREP Register (Address = 0x60) [Default = 0x00]

CSI1_TCK_PREP is shown in Table 5-189.

Return to the Summary Table.

Table 5-189. CSI1_TCK_PREP Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_PREP_OV	R/W	0x0	Override CSI Tck-prep parameter 0: Tck-prep is automatically determined 1: Override Tck-prep with value in bits 6:0 of this register
6:0	MR_TCK_PREP	R/W	0x0	Tck-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.41 CSI1_TCK_ZERO Register (Address = 0x61) [Default = 0x00]

CSI1_TCK_ZERO is shown in Table 5-190.

Return to the Summary Table.

Table 5-190. CSI1_TCK_ZERO Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_ZERO_OV	R/W	0x0	Override CSI Tck-zero parameter 0: Tck-zero is automatically determined 1: Override Tck-zero with value in bits 6:0 of this register
6:0	MR_TCK_ZERO	R/W	0x0	Tck-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.42 CSI1_TCK_TRAIL Register (Address = 0x62) [Default = 0x00]

CSI1_TCK_TRAIL is shown in Table 5-191.

Return to the Summary Table.

Table 5-191. CSI1_TCK_TRAIL Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_TRAIL_OV	R/W	0x0	Override CSI Tck-trail parameter 0: Tck-trail is automatically determined 1: Override Tck-trail with value in bits 6:0 of this register
6:0	MR_TCK_TRAIL	R/W	0x0	Tck-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.43 CSI1_TCK_POST Register (Address = 0x63) [Default = 0x00]

CSI1_TCK_POST is shown in Table 5-192.

Return to the Summary Table.

Table 5-192. CSI1_TCK_POST Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_POST_OV	R/W	0x0	Override CSI Tck-post parameter 0: Tck-post is automatically determined 1: Override Tck-post with value in bits 6:0 of this register

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Table 5-192. CSI1_TCK_POST Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:0	MR_TCK_POST	R/W	0x0	Tck-post value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.44 CSI1_THS_PREP Register (Address = 0x64) [Default = 0x00]

CSI1_THS_PREP is shown in Table 5-193.

Return to the Summary Table.

Table 5-193. CSI1_THS_PREP Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_PREP_OV	R/W	0x0	Override CSI Ths-prep parameter 0: Ths-prep is automatically determined 1: Override Ths-prep with value in bits 6:0 of this register
6:0	MR_THS_PREP	R/W	0x0	Ths-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.45 CSI1_THS_ZERO Register (Address = 0x65) [Default = 0x00]

CSI1_THS_ZERO is shown in Table 5-194.

Return to the Summary Table.

Table 5-194. CSI1_THS_ZERO Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_ZERO_OV	R/W	0x0	Override CSI Ths-zero parameter 0: Ths-zero is automatically determined 1: Override Ths-zero with value in bits 6:0 of this register
6:0	MR_THS_ZERO	R/W	0x0	Ths-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.46 CSI1_THS_TRAIL Register (Address = 0x66) [Default = 0x00]

CSI1_THS_TRAIL is shown in Table 5-195.

Return to the Summary Table.

Table 5-195. CSI1_THS_TRAIL Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_TRAIL_OV	R/W	0x0	Override CSI Ths-trail parameter 0: Ths-trail is automatically determined 1: Override Ths-trail with value in bits 6:0 of this register
6:0	MR_THS_TRAIL	R/W	0x0	Ths-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

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5.6.2.1.47 CSI1_THS_EXIT Register (Address = 0x67) [Default = 0x00]

CSI1_THS_EXIT is shown in Table 5-196.

Return to the Summary Table.

Table 5-196. CSI1_THS_EXIT Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_EXIT_OV	R/W	0x0	Override CSI Ths-exit parameter 0: Ths-exit is automatically determined 1: Override Ths-exit with value in bits 6:0 of this register
6:0	MR_THS_EXIT	R/W	0x0	Ths-exit value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

5.6.2.1.48 CSI1_TPLX Register (Address = 0x68) [Default = 0x00]

CSI1_TPLX is shown in Table 5-197.

Return to the Summary Table.

Table 5-197. CSI1_TPLX Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TPLX_OV	R/W	0x0	Override CSI Tplx parameter 0: Tplx is automatically determined 1: Override Tplx with value in bits 6:0 of this register
6:0	MR_TPLX	R/W	0x0	Tplx value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

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6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The DS90UB964-Q1 is a highly integrated sensor hub deserializer which includes four FPD-Link III inputs targeted at ADAS applications, such as front/rear/surround-view camera sensors, driver monitoring systems, and sensor fusion.

6.1.1 Power-Over-Coax

The DS90UB964-Q1 is designed to support the Power-over-Coax (PoC) method of powering remote sensor systems. With this method, the power is delivered over the same medium (a coaxial cable) used for high-speed digital video data and bidirectional control and diagnostics data transmission. The method uses passive networks or filters that isolate the transmission line from the loading of the DC-DC regulator circuits and their connecting power traces on both sides of the link as shown in Figure 6-1.

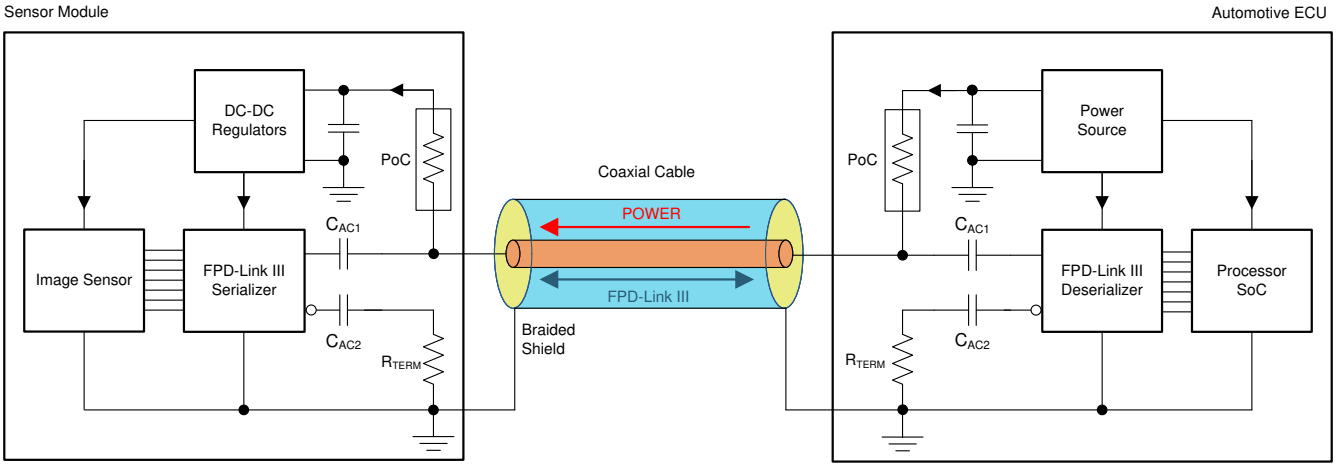

Figure 6-1. Power-over-Coax (PoC) System Diagram

The PoC networks' impedance of ≥ 1kΩ over a specific frequency band is recommended to isolate the transmission line from the loading of the regulator circuits provided good layout practices are followed and the PCB return loss requirements given in Table 6-2 are met. Higher PoC network impedance contributes to favorable insertion loss and return loss characteristics in the high-speed channel. The lower limit of the frequency band is defined as ½ of the frequency of the back channel, f_{BC}. The upper limit of the frequency band is the frequency of the forward high-speed channel, f_{FC}. However, the main criteria that need to be met in the total high-speed channel, which consists of a serializer PCB, a deserializer PCB, and a cable, are the insertion loss and return loss limits defined in the Total Channel Requirements (see Section 5.4.6.1), while the system is under maximum current load and extreme temperature conditions.

Figure 6-2 shows a PoC network recommended for a "2G" FPD-Link III consisting of a DS90UB913A-Q1 or DS90UB933-Q1 serializer and DS90UB964-Q1 with the bidirectional channel operating at the data rate of 2.5Mbps (½ f_{BC} = 1.25MHz) and the forward channel operating at the data rate as high as 1.87Gbps (f_{FC} ≈ 1GHz).

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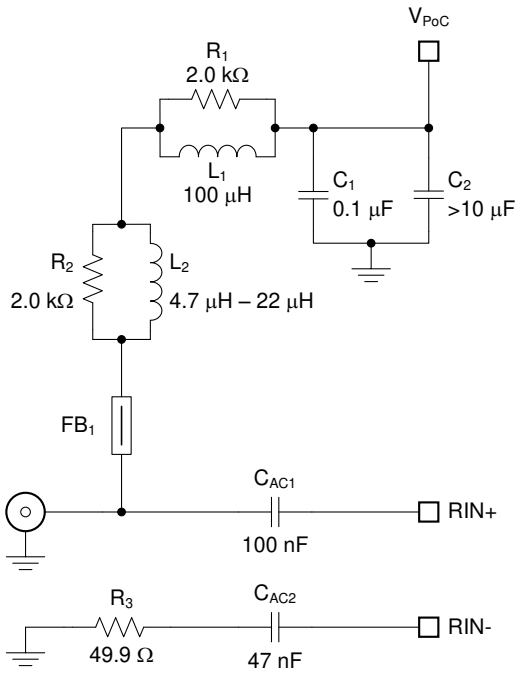

Figure 6-2. Example Recommended PoC Network for a "2G" FPD-Link III

Table 6-1 lists essential components for this particular PoC network.

Table 6-1. Suggested Components for a "2G" FPD-Link III PoC Network

Count	Ref Des	Description	Part Number	MFR
1	L1	Inductor, 100µH, 0.310Ω max, 710mA MIN (Isat, Itemp) 7.2MHz SRF typ, 6.6mm × 6.6mm, AEC-Q200	MSS7341-104ML	Coilcraft
		Inductor, 100µH, 0.606Ω max, 750mAMIN (Isat, Itemp) 7.2MHz SRF typ, 6.0mm × 6.0mm, AEC-Q200	NRS6045T101MMGKV	Taiyo Yuden
1	L2	Inductor, 4.7µH, 0.350Ω max, 700mA MIN (Isat, Itemp) 160MHz SRF typ, 3.8mm × 3.8mm, AEC-Q200	1008PS-472KL	Coilcraft
		Inductor, 4.7µH, 0.130Ω max, 830mA MIN (Isat, Itemp), 70MHz SRF typ, 3.2mm × 2.5mm, General Purpose	CBC3225T4R7MRV	Taiyo Yuden
		Inductor, 10µH, 0.288Ω max, 530mA MIN (Isat, Itemp) 30MHz SRF min, 3mm × 3mm, AEC-Q200	LQH3NPZ100MJR	Murata
1	FB1	Ferrite Bead, 1500kΩ at 1GHz, 0.5Ω max at DC 500mA at 85°C, SM0603, General Purpose	BLM18HE152SN1	Murata
		Ferrite Bead, 1500kΩ at 1GHz, 0.5Ω max at DC 500mA at 85°C, SM0603, AEC-Q200	BLM18HE152SZ1	Murata

Application report *Sending Power over Coax in DS90UB913A Designs* (SNLA224) discusses and defines the PoC networks in more detail.

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In addition to the PoC network components selection, the placement and layout play a critical role as well.

- Place the smallest component, typically a ferrite bead or a chip inductor, as close to the connector as possible. Route the high-speed trace through one of the ferrite bead pads to avoid stubs.
- Use the smallest component pads as allowed by manufacturer's design rules. Add anti-pads in the inner planes below the component pads to minimize impedance drop.
- Consult with connector manufacturer for optimized connector footprint.
- Use coupled 100Ω differential signal traces from the device pins to the AC-coupling caps. Use 50Ω single-ended traces from the AC-coupling capacitors to the connector.
- Terminate the inverting signal traces close to the connectors with standard 49.9Ω resistors.

The suggested characteristics for single-ended PCB traces (microstrips or striplines) for serializer or deserializer boards are detailed in Table 6-2. The effects of the PoC networks need to be accounted for when testing the traces for compliance to the suggested limits.

Table 6-2. Suggested Characteristics for Single-Ended PCB Traces With Attached PoC Networks

PARAMETER			MIN	TYP	MAX	UNIT
L_{trace}	Single-ended PCB trace length from the device pin to the connector pin				5	cm
Z_{trace}	Single-ended PCB trace characteristic impedance		45	50	55	Ω
Z_{con}	Connector (mounted) characteristic impedance		40	50	62.5	Ω
RL	Return Loss, S11	½ f_{BC} < f < 0.1GHz			–20	dB
		0.1GHz < f < 1GHz (f in GHz)			–12 + 8 × log(f)	dB
		1GHz < f < f_{FC}			–12	dB
IL	Insertion Loss, S12	f < 0.5GHz	–0.35			dB
		f = 1GHz	–0.6			dB

The V_{POC} noise must be kept to 10mVp-p or lower on the source / deserializer side of the system. The V_{POC} fluctuations on the serializer side, caused by the sensor's transient current draw and the DC resistance of cables and PoC components, must be kept at minimum as well. Increasing the V_{POC} voltage and adding extra decoupling capacitance (> 10µF) help reduce the amplitude and slew rate of the V_{POC} fluctuations.

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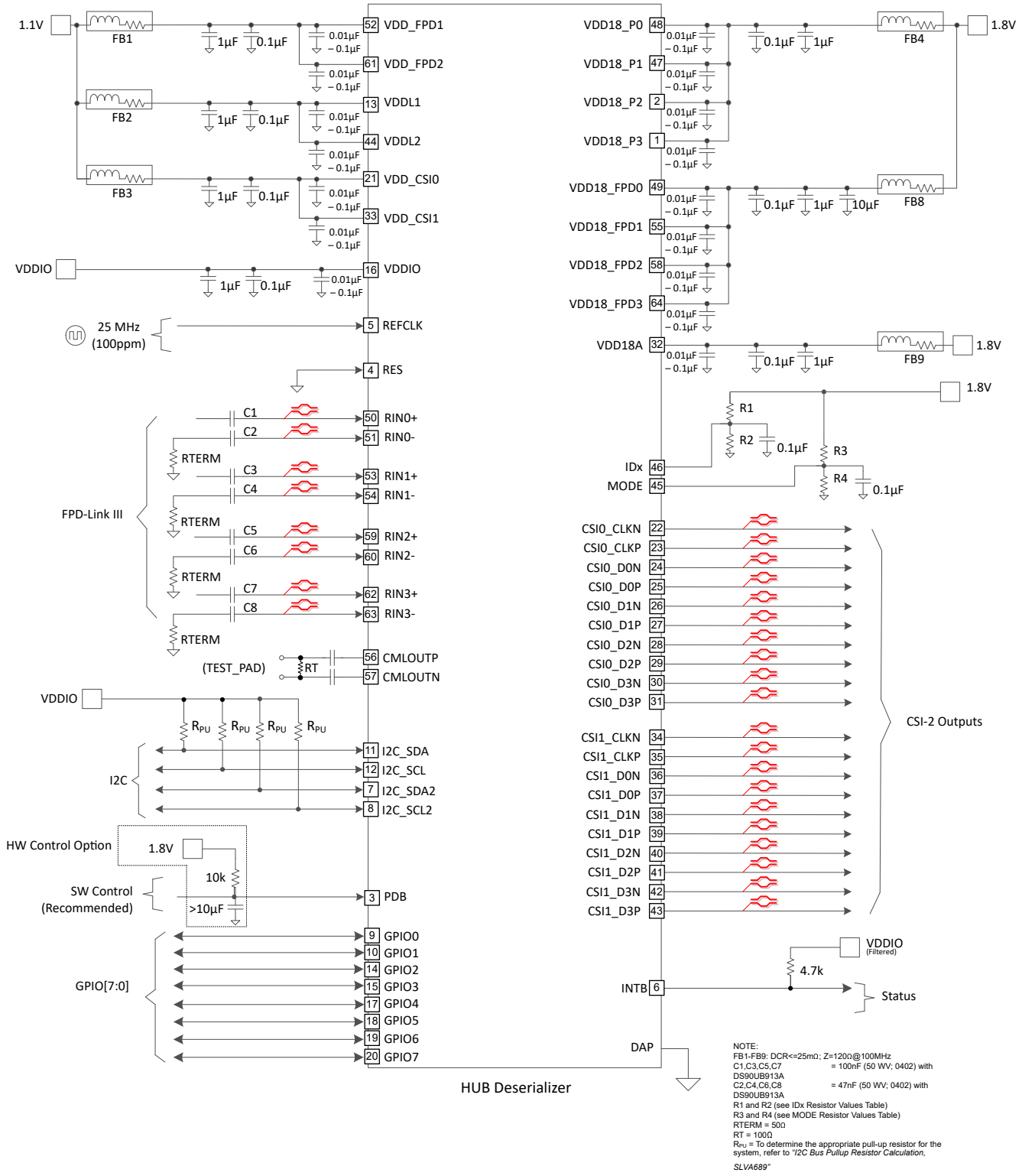
6.2 Typical Application



6.2.1 Design Requirements

For the typical design application, use the parameters listed in Table 6-3.

Table 6-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8V or 3.3V
VDD11	1.1V
VDD18	1.8V
AC-Coupling Capacitor for STP with 933A / 913A: RIN[3:0]±	100nF (50V/X7R/0402)
AC-Coupling Capacitor for Coaxial with 933A / 913A: RIN[3:0]+	100nF (50V/X7R/0402)
AC-Coupling Capacitor for Coaxial with 933A / 913A: RIN[3:0]-	47nF (50V/X7R/0402)

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as shown in Figure 6-3. For applications using single-ended 50Ω coaxial cable, terminate the unused data pins (RIN0–, RIN1–, RIN2–, RIN3–) with an AC-coupling capacitor and a 50Ω resistor.

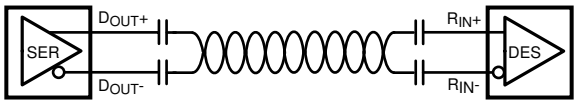


Figure 6-3. AC-Coupled Connection (STP)

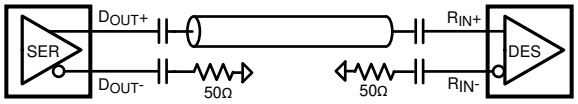


Figure 6-4. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link III transmissions, use the smallest available package for the AC-coupling capacitor to help minimize degradation of signal quality due to package parasitics.

6.2.2 Detailed Design Procedure

Figure 6-9 and Figure 6-10 show typical applications of the DS90UB964-Q1 for a multi-camera surround view system. The FPD-Link III must have an external 100nF / 47nF, AC-coupling capacitors for coaxial interconnects. The same AC-coupling capacitor values must be matched on the paired serializer boards. The deserializer has an internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, 0.1µF or 0.01µF capacitors must be used for each of the core supply pins for local device bypassing. Ferrite beads are placed on the VDD18 and VDD11 supplies for effective noise suppression.

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6.2.3 Application Curves

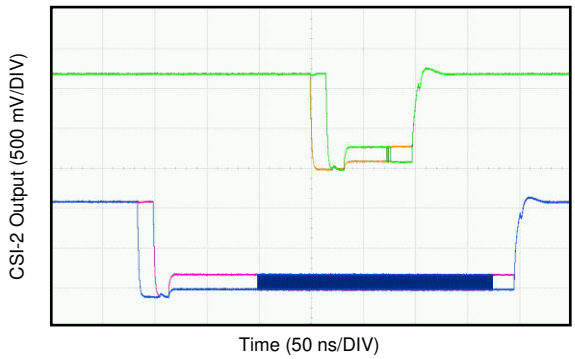

Figure 6-5. CSI-2 DATA and CLK Output

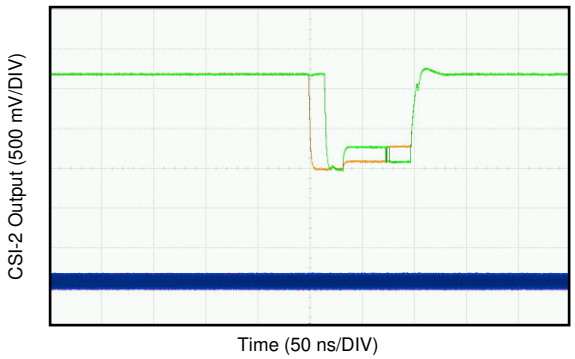

Figure 6-6. CSI-2 DATA and Continuous CLK Output

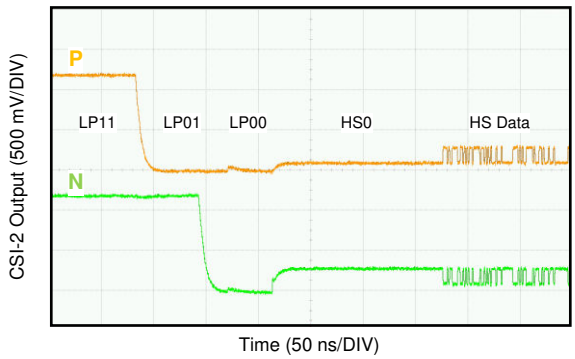

Figure 6-7. CSI-2 Start of Transmission (SoT)

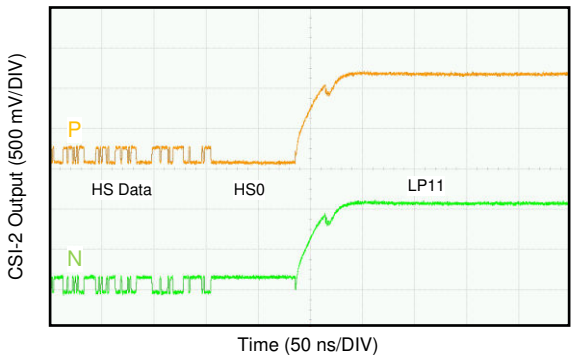

Figure 6-8. CSI-2 End of Transmission (EoT)

6.3 System Examples

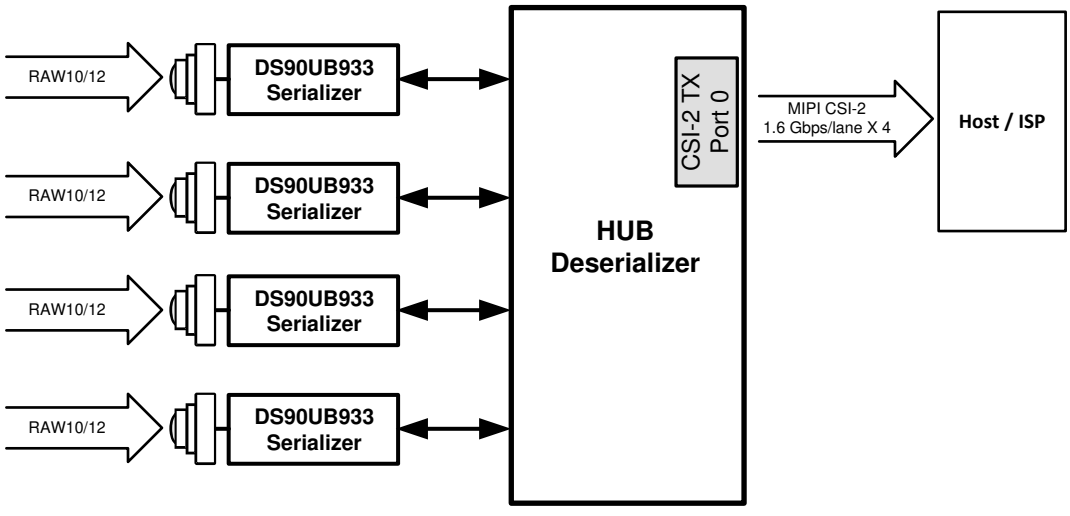

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Figure 6-9. Four DS90UB933-Q1 Sensor Data Onto CSI-2 Over 1 Port

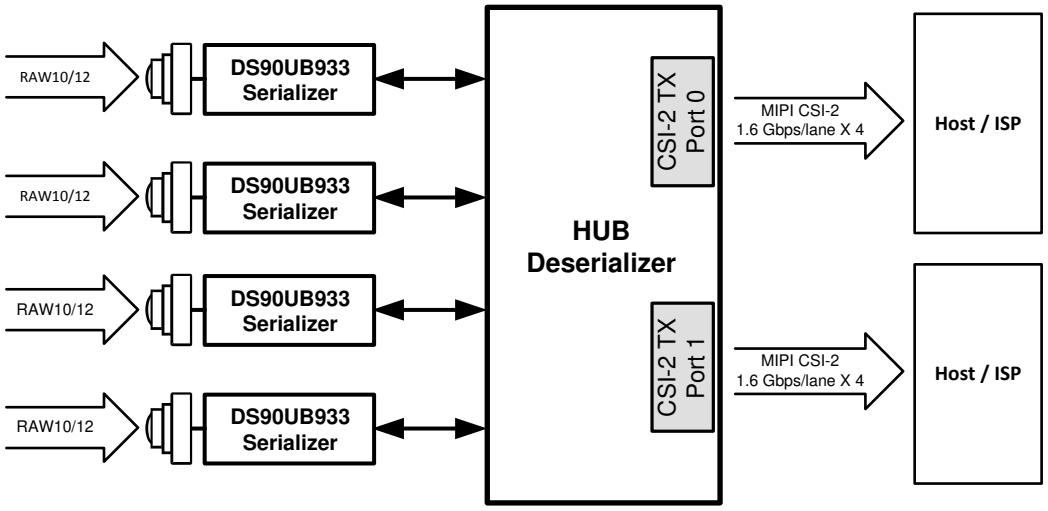

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Figure 6-10. Four DS90UB933-Q1 Sensor Data Onto CSI-2 Over 2 Ports

6.4 Power Supply Recommendations

This device has separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. The *Pin Configuration and Functions* section provides guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

6.4.1 VDD Power Supply

Each VDD power supply pin must have a 10nF (or 100nF) capacitor to ground connected as close as possible to DS90UB964-Q1 device. TI recommends having additional decoupling capacitors (0.1uF, 1µF, and 10µF) and the pins connected to a solid power plane.

6.4.2 Power-Up Sequencing

The power-up sequence for the DS90UB964-Q1 is as follows:

Table 6-4. Timing Diagram for the Power-Up Sequence

PARAMETER		MIN	TYP	MAX	UNIT	NOTES
t_{r0}	VDD18 / VDDIO rise time	0.2			ms	@10/90%
t_{r1}	VDD11 rise time	0.05			ms	@10/90%
t_0	VDD18 / VDDIO to VDD11 delay	0			ms	
t_1	VDDx to REFCLK delay	0			ms	Keep REFCLK low until all supplies are up and stable.
t_2	VDDx to PDB delay	0			ms	Release PDB after all supplies are up and stable.
t_3	PDB to I2C ready (IDX and MODE valid) delay	2			ms	
t_4	PDB pulse width	2			ms	Hard reset
t_5	PDB to GPIO delay	0			ms	Keep GPIOs low or high until PDB is high.

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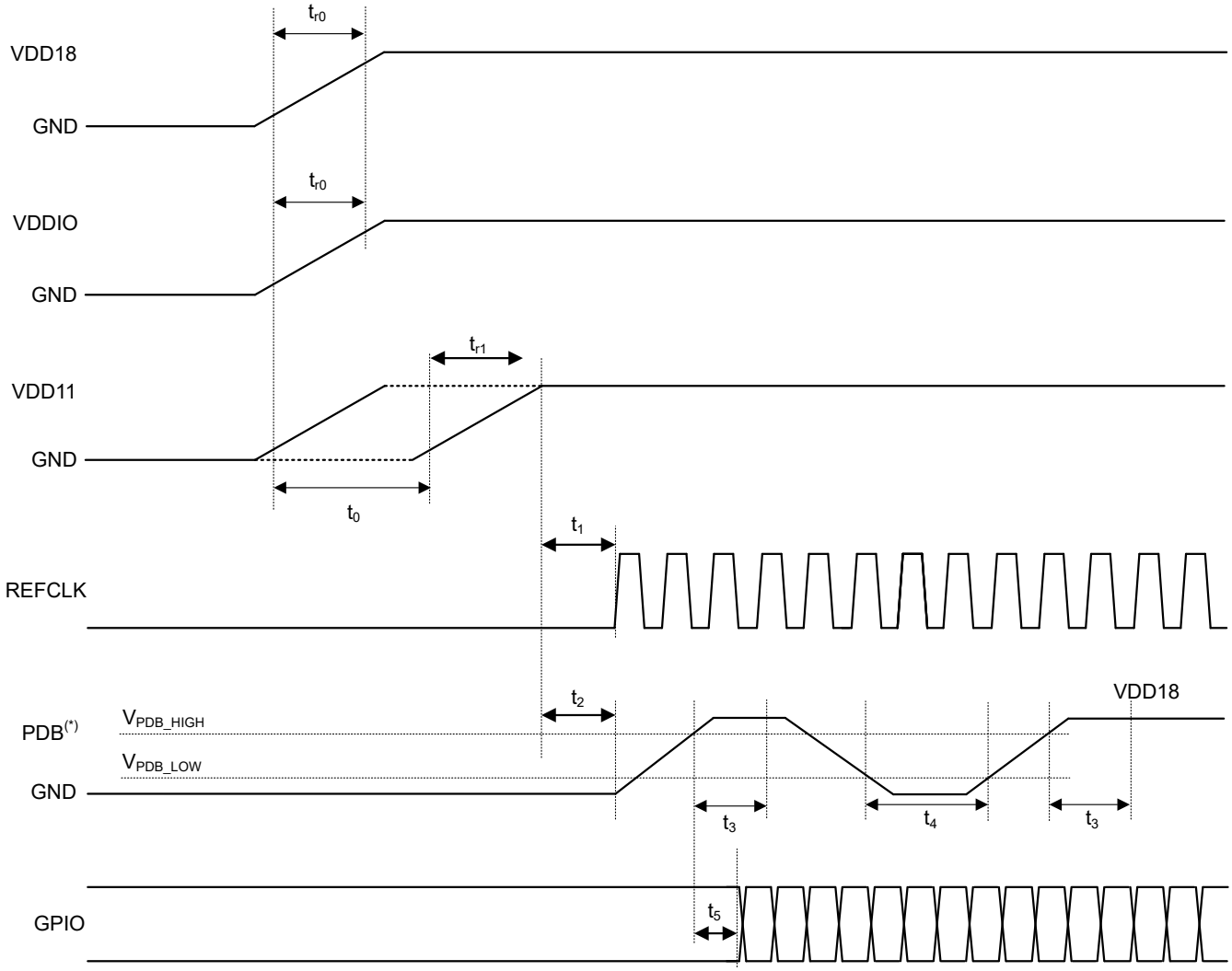

(*) It is recommended to assert PDB (active High) with a microcontroller rather than an RC filter network to achieve proper sequencing of PDB pin after settling of power supplies.

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Figure 6-11. Power-Up Sequencing

6.4.2.1 PDB Pin

The PDB pin is active HIGH and must remain LOW while the VDD pin power supplies are in transition. An external RC network on the PDB pin can be connected so PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to VDD18, a 10kΩ pullup and a > 10µF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until both power supplies have reached steady state.

Table 6-5. PDB Reset Signal Pulse Width

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PDB						
tLRST	PDB Reset Low Pulse		2			ms

6.5 Layout

6.5.1 Layout Guidelines

Circuit board layout and stack-up for the FPD-Link III devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise pick-up, feedback, and interference. Power system performance can be greatly improved by using thin dielectrics (2 to 4 mils) for power/ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors can include both RF ceramic and tantalum electrolytic types. RF capacitors can use values in the range of 0.01µF to 0.1µF. Ceramic capacitors can be in the 2.2µF to 10µF range. The voltage rating of the ceramic capacitors must be at least 5× the power supply voltage being used

TI recommends surface-mount capacitors due to the smaller parasitics. When using multiple capacitors per supply pin, place the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50µF to 100µF range, which smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. The small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, common practice is to use two vias from power and ground pins to the planes to reduce the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter can be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Differential impedance of 100Ω are typically recommended for STP interconnect and single-ended impedance of 50Ω for coaxial interconnect. The closely coupled lines cause coupled noise to appear as common-mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

6.5.1.1 Ground

TI recommends that a consistent ground plane reference for the high-speed signals is used in the PCB design to provide the best image plane for signal traces running parallel to the plane. Connect the thermal pad of the DS90UB964-Q1 to this plane with vias.

6.5.1.2 Routing FPD-Link III Signal Traces and PoC Filter

Routing the FPD-Link III signal traces between the R_{IN} pins and the connector as well as connecting the PoC filter to these traces are the most critical pieces of a successful DS90UB964-Q1 PCB layout. Figure 6-12 shows an example PCB layout of the DS90UB964-Q1 configured for interface to remote sensor modules over coaxial cables. The layout example also uses a footprint of an edge-mount Quad Mini-FAKRA connector provided by Rosenberger.

The following list provides essential recommendations for routing the FPD-Link III signal traces between the DS90UB964-Q1 receiver input pins (R_{IN}) and the FAKRA connector, and connecting the PoC filter.

- The routing of the FPD-Link III traces can be all on the top layer (as shown in the example) or partially embedded in middle layers if EMI is a concern.
- The AC-coupling capacitors are advised to be on the top layer and very close to the DS90UB964-Q1 receiver input pins to minimize the length of coupled differential trace pair between the pins and the capacitors.

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- Route the RIN+ trace between the AC-coupling capacitor and the FAKRA connector as a 50Ω single-ended micro-strip with tight impedance control (±10%). Calculate the proper width of the trace for a 50Ω impedance based on the PCB stack-up. Verify that the trace can carry the PoC current for the maximum load presented by the remote sensor module.
- The PoC filter must be connected to the RIN+ trace through the first ferrite bead (FB_1). The FB_1 is advised to touch the high-speed trace to minimize the stub length seen by the transmission line. Create an anti-pad or a moat under the FB_1 pad that touches the trace. The anti-pad is a plane cutout of the ground plane directly underneath the top layer without cutting out the ground reference under the trace. The purpose of the anti-pad is to maintain the impedance as close to 50Ω as possible.
- Route the RIN– trace with minimum coupling to the RIN+ trace (S > 3W).
- Consult with connector manufacturer for optimized connector footprint. If the connector is mounted on the same side as the IC, minimize the impact of the thru-hole connector stubs by routing the high-speed signal traces on the opposite side of the connector mounting side.

When configured for STP and routing differential signals to the DS90UB964-Q1 receiver inputs, the traces must maintain a 100Ω differential impedance routed to the connector. When choosing to implement a common mode choke for common mode noise reduction, take care to minimize the effect of any mismatch.

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6.5.1.3 CSI-2 Guidelines

1. Route CSI0_D*P/N and CSI1_D*P/N pairs with controlled 100Ω differential impedance (±20%) or 50Ω single-ended impedance (±15%).
2. Keep away from other high-speed signals.
3. Minimize intra-pair and inter-pair length mismatch within a single CSI-2 TX Port (recommended <= 5 mils).
4. Length matching is recommended to be near the location of mismatch.
5. Each pair is recommended to be separated at least by 3 times the signal trace width.
6. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bend is recommended to be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
7. Route all differential pairs on the same layer.
8. Keep the number of VIAS to a minimum — TI recommends keeping the VIA count to 2 or fewer.
9. Keep traces on layers adjacent to ground plane.
10. Do NOT route differential pairs over any plane split.
11. Adding Test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Test points must not be placed in a manner that causes a stub on the differential pair.

6.5.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the VQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder can flow unevenly through the DAP.

Example PCB layout is used to demonstrate both proper routing and proper solder techniques when designing in the Deserializer.

Figure 6-12 shows a PCB layout example are derived from the layout design of the DS90UB96X-Q1 Evaluation Board. The graphic and layout description are used to determine proper routing when designing the board. The high-speed FPD-Link III traces routed differentially up to the connector. A 100Ω differential characteristic impedance and 50Ω single-ended characteristic impedance traces are maintained as much as possible for both STP and coaxial applications. For the layout of a coaxial interconnects, coupled traces are recommended to be used with the RINx- termination near the connector.

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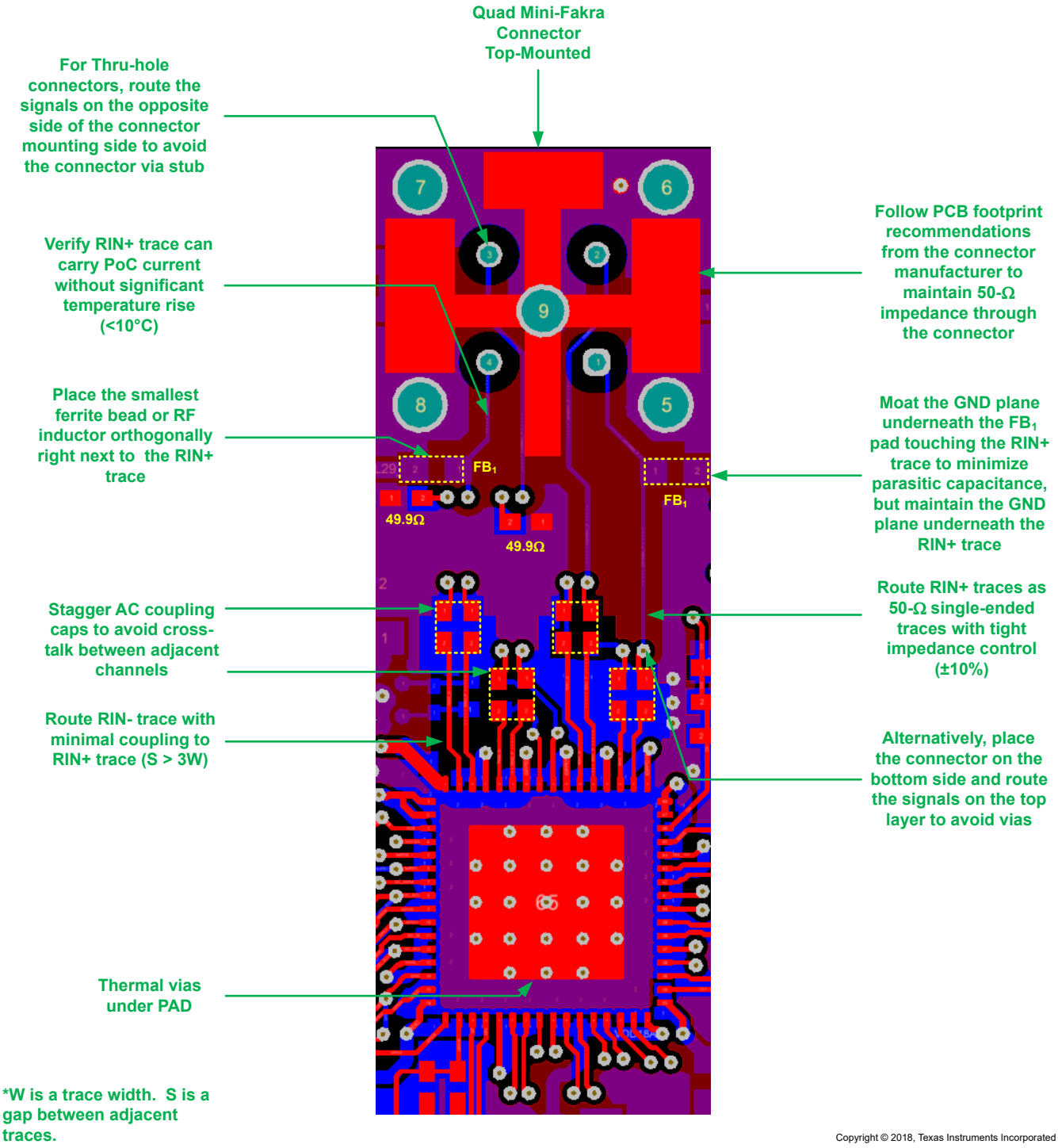

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Figure 6-12. DS90UB964 Example PCB Layout With Quad Mini-Fakra Connector

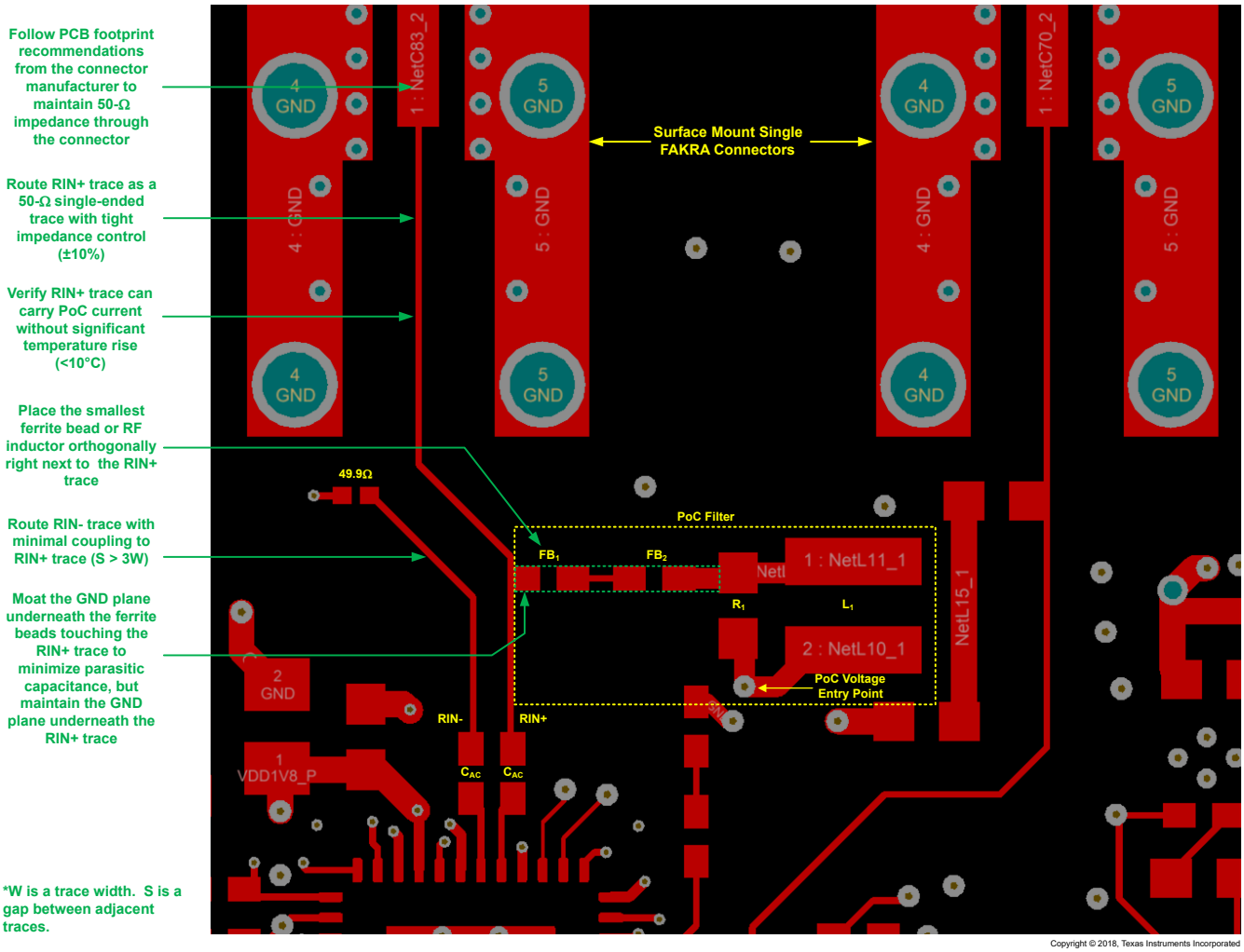

Figure 6-13. Example Routing of FPD-Link III Traces to a Single Mini-Fakra Connector and PoC Components

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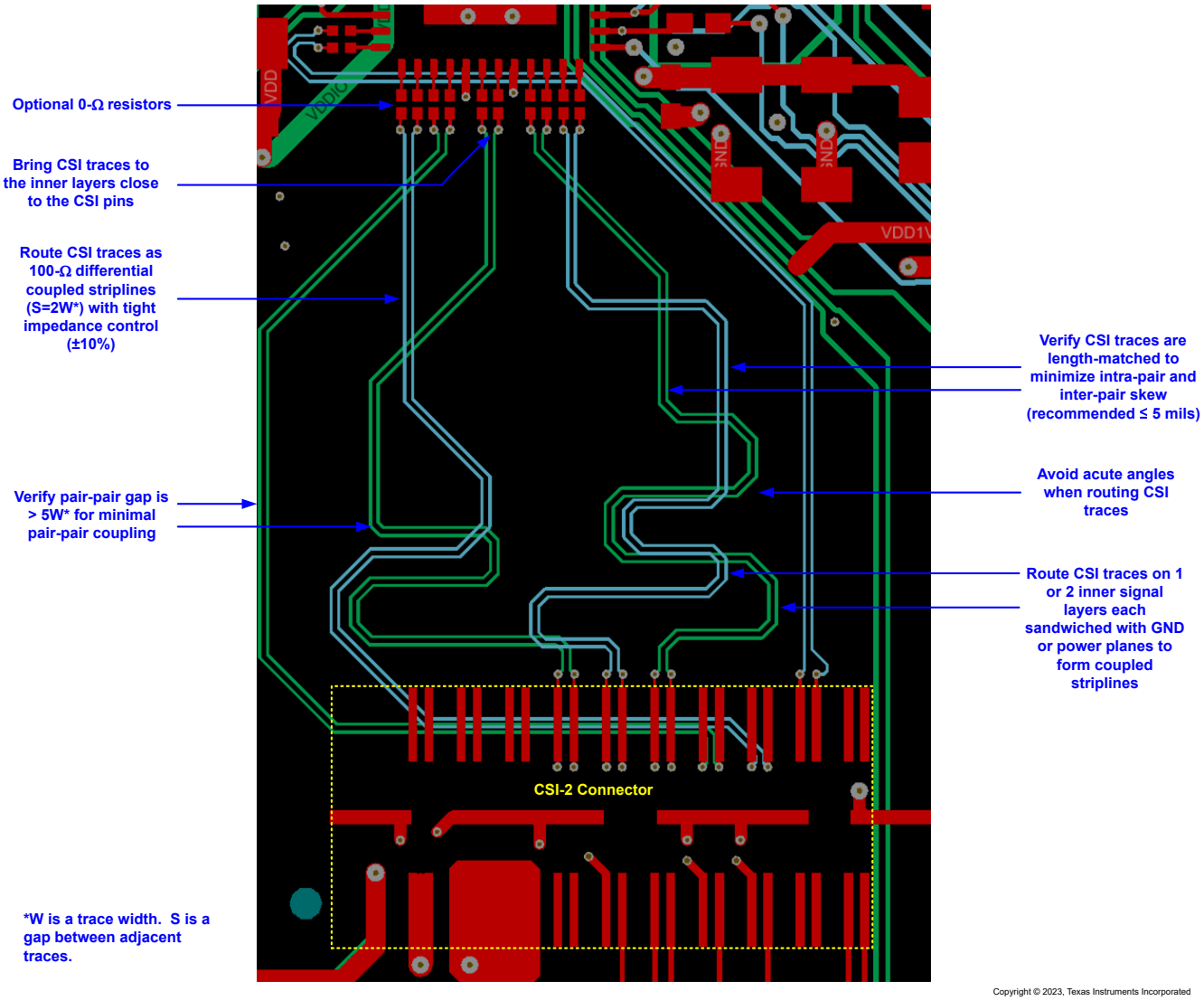

Figure 6-14. Example Routing of CSI-2 Traces

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation see the following:

- *Sending Power over Coax in DS90UB913A Designs* (SNLA224)
- *I2C Over DS90UB913/4 FPD-Link III With Bidirectional Control Channel* (SNLA222)
- *I2C Communication Over FPD-Link III With Bidirectional Control Channel* (SNLA131)
- *I2C Bus Pullup Resistor Calculation* (SLVA689)
- FPD-Link University Training Material
- *An EMC/EMI System-Design and Testing Methodology for FPD-Link III SerDes* (SLYT719)
- *Ten Tips for Successfully Designing With Automotive EMC/EMI Requirements* (SLYT636)

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2016) to Revision A (December 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Fixed spelling errors and minor format issues throughout the document	1
• Updated format of data sheet	1
• Updated Typical Application Schematic to clearly show two CSI-2 output ports	1
• Updated I2C pull-up resistor recommendations	3
• Updated Legend for Pin Functions Table	3
• Moved INTB pin description to OTHERS category	3
• Renamed Pin 4 to RES	3
• Updated VDD pin descriptions	3
• Updated REFCLK pin description	3
• Updated input current specification to include internal pulldowns for GPIO and PDB pins	8
• Updated V_{IH} and V_{IL} specifications for PDB and REFCLK pins	8

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- Added V_{IN} specification ... 8
- Updated V_{ID} specification ... 8
- Changed input jitter symbol from IJT to T_{IJIT} and renamed Input Jitter Tolerance parameter to Input Jitter to be consistent with specifying max input jitter ... 11
- Removed the t_{CLK_MISS} specification from the CSI-2 Timing Specifications table ... 13
- Updated V_{ID} diagram ... 13
- Added information about the bidirectional control channel ... 21
- Corrected serializer part numbers throughout data sheet ... 21
- Renamed section to RAW Data Type Support & Rates for clarity ... 23
- Added information about YUV support ... 23
- Added information about FPD-Link line rates ... 23
- Removed mentions of Coaxial or STP mode since device automatically accepts either configuration regardless of MODE strap ... 23
- Updated resistor values while keeping the same voltage ratio ... 23
- Rewrote target voltage range in terms of $V_{(VDD18)}$ ... 23
- Clarified default back channel rate ... 23
- Clarified that the REFCLK value can range between 23MHz to 25MHz throughout the document ... 24
- Added section on receiver port control ... 24
- Added a channel requirements section to the data sheet ... 25
- Updated AEQ section and register 0xB9 register setting recommendation for clarity ... 26
- Added additional AEQ sections for clarity ... 26
- Added sections related to the RX port status for clarity ... 28
- Added additional GPIO sections on input and output control ... 29
- Added additional information on back channel GPIO ... 29
- Added section on video stream forwarding ... 31
- Added information about YUV and RAW8 support ... 32
- Added information about conversion from DVP format to CSI-2 data packets ... 32
- Updated VC-ID mapping example graphics ... 33
- Added section on CSI-2 Transmitter Status for clarity ... 36
- Added note about how to program the FS_HIGH_TIME register ... 37
- Clarified that CSI-2 forwarding must be disabled before CSI-2 replicate mode is enabled ... 45
- Added section on enabling and disabling CSI-2 transmitters ... 46
- Added additional I2C sections to clarify functionality ... 46
- Changed I2C terminology to "Controller" and "Target" ... 46
- Added a sentence to clarify that V_{I2C} must match the voltage applied to VDDIO ... 46
- Reworded the Serial Control Bus section to reference V_{I2C} instead of VDDIO ... 46
- Updated resistor values while keeping the same voltage ratio ... 46
- Rewrote target voltage range in terms of V_{VDD18} ... 46
- Clarified that Register 0x01 (RESET_CTL) can only be written by the primary I2C port ... 49
- Added additional information about how to configure a broadcast write to remote devices ... 50
- Removed unnecessary register writes in the Code Example for Broadcast Write ... 50
- Clarified instructions for how to configure Pattern Generation on the CSI-2 Port ... 57
- Updated Pattern Generator example script to update data type to RAW10 ... 58
- Renamed section to FPD-Link BIST Mode ... 59
- Added additional information about BIST ... 59
- Renamed section to BIST Operation ... 59
- Added additional information about BIST operation ... 59
- Removed all RESERVED registers from the data sheet ... 61
- Updated the description of register bit 0x34[1] ... 61
- Made register 0x41 public ... 61
- Updated the description of register bits 0x42[6:4] ... 61
- Updated the description of register bit 0x4E[1] to clarify functionality ... 61
- RESERVED register 0x6D[2] as the bit is no longer applicable ... 61
- Corrected default value of register bit 0x7C[5] ... 61
- RESERVED value of register bit 0x7D[6] ... 61

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- Removed RESERVED indirect register pages in the description of register bits 0xB0[5:2]..... 61
- Updated the description of register bits 0xB3[2:1]..... 61
- Made register bits 0xB6[5:3] public..... 61
- Updated the description of register bits 0xB9[3:0]..... 61
- Corrected default value of register bit 0xD2[2]..... 61
- Updated name of register 0xD2..... 61
- Updated the name of Indirect Register Page 0 to PATGEN_AND_CSI-2..... 61
- Added additional information about PoC..... 136
- Added 2G PoC network example..... 136
- Updated typical connection diagram to include a reference to App Note SLVA689..... 139
- Removed optional 10 kΩ pulldown resistor on Pin 4 in the Typical Connection Diagram..... 139
- Highlighted HW and SW control options on PDB pin..... 139
- Added pin numbers to Typical Application Diagram..... 139
- Added additional CSI-2 diagrams for Start of Transmission and End of Transmission..... 141
- Updated power-up sequencing diagram and table..... 142
- Added additional layout section for clarity..... 144
- Updated MIPI CSI-2 D-PHY layout recommendations..... 146
- Updated layout example..... 146
- Added additional related documentation..... 150

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90UB964TRGCRQ1	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB964Q
DS90UB964TRGCRQ1.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB964Q
DS90UB964TRGCRQ1.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB964Q
DS90UB964TRGCTQ1	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB964Q
DS90UB964TRGCTQ1.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB964Q
DS90UB964TRGCTQ1.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB964Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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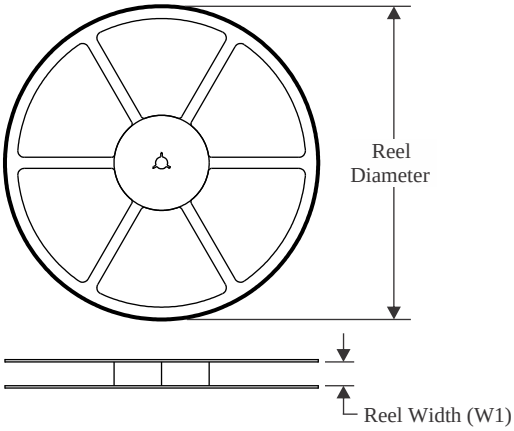
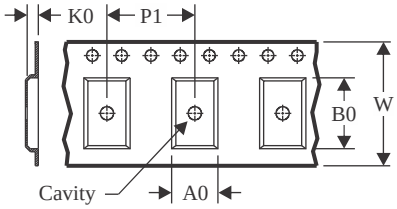
TAPE AND REEL INFORMATION

REEL DIMENSIONS

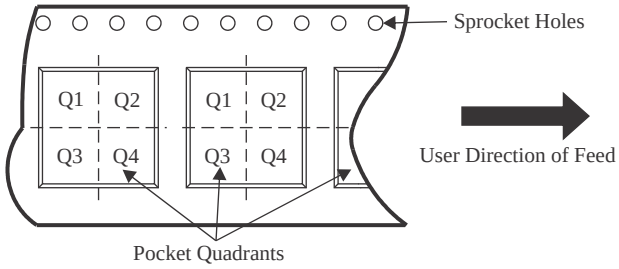


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

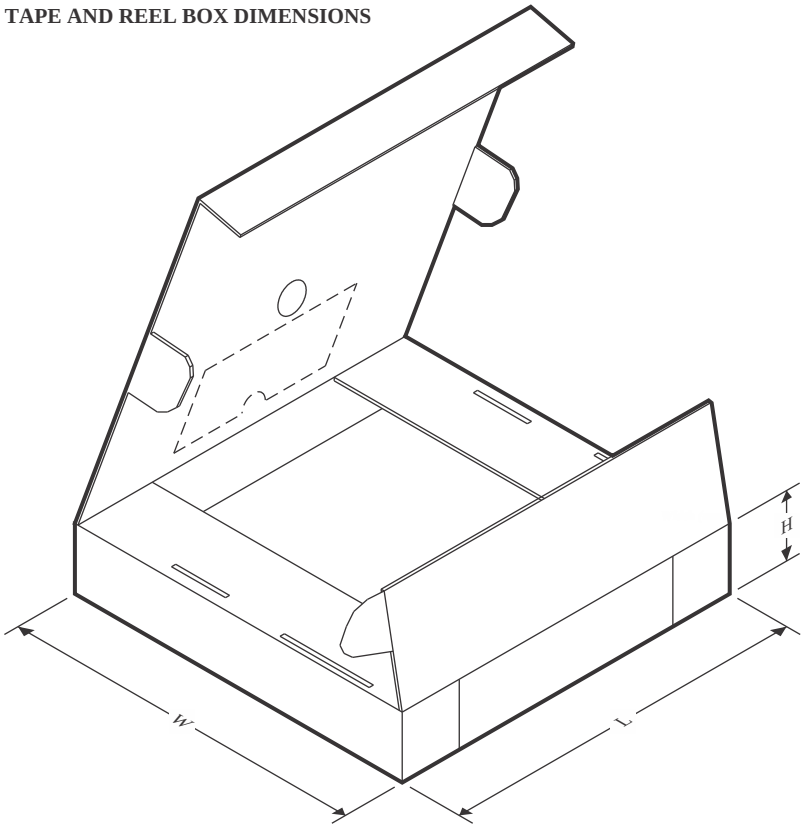
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB964TRGCRQ1	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
DS90UB964TRGCTQ1	VQFN	RGC	64	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB964TRGCRQ1	VQFN	RGC	64	2000	356.0	356.0	36.0
DS90UB964TRGCTQ1	VQFN	RGC	64	250	208.0	191.0	35.0

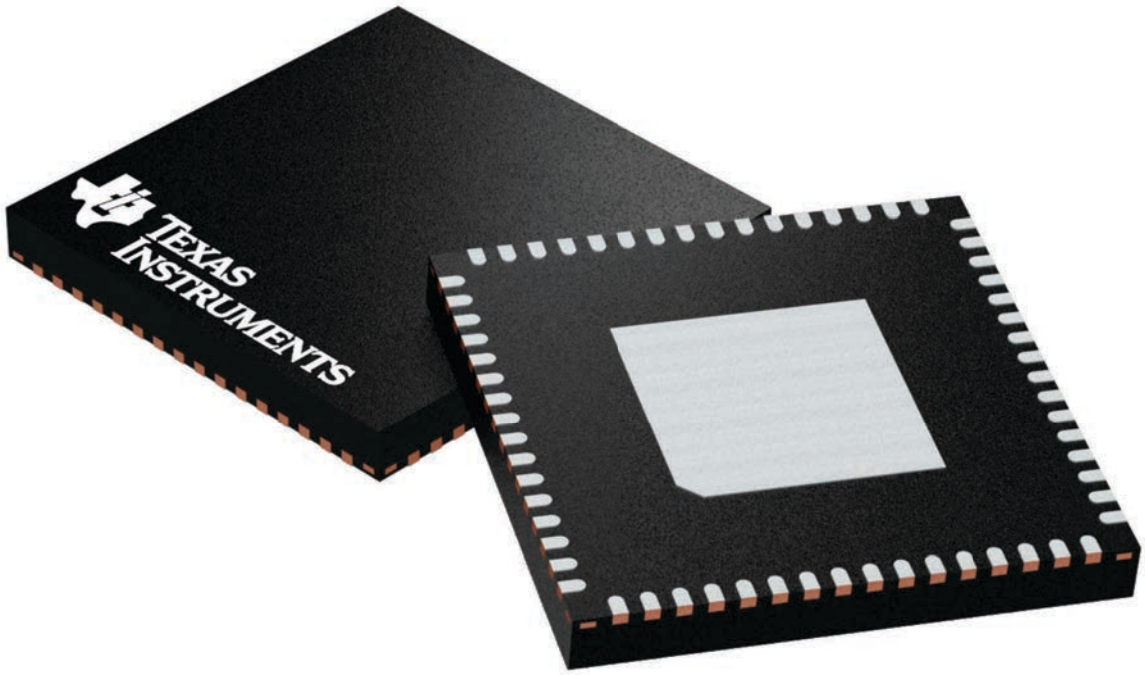
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

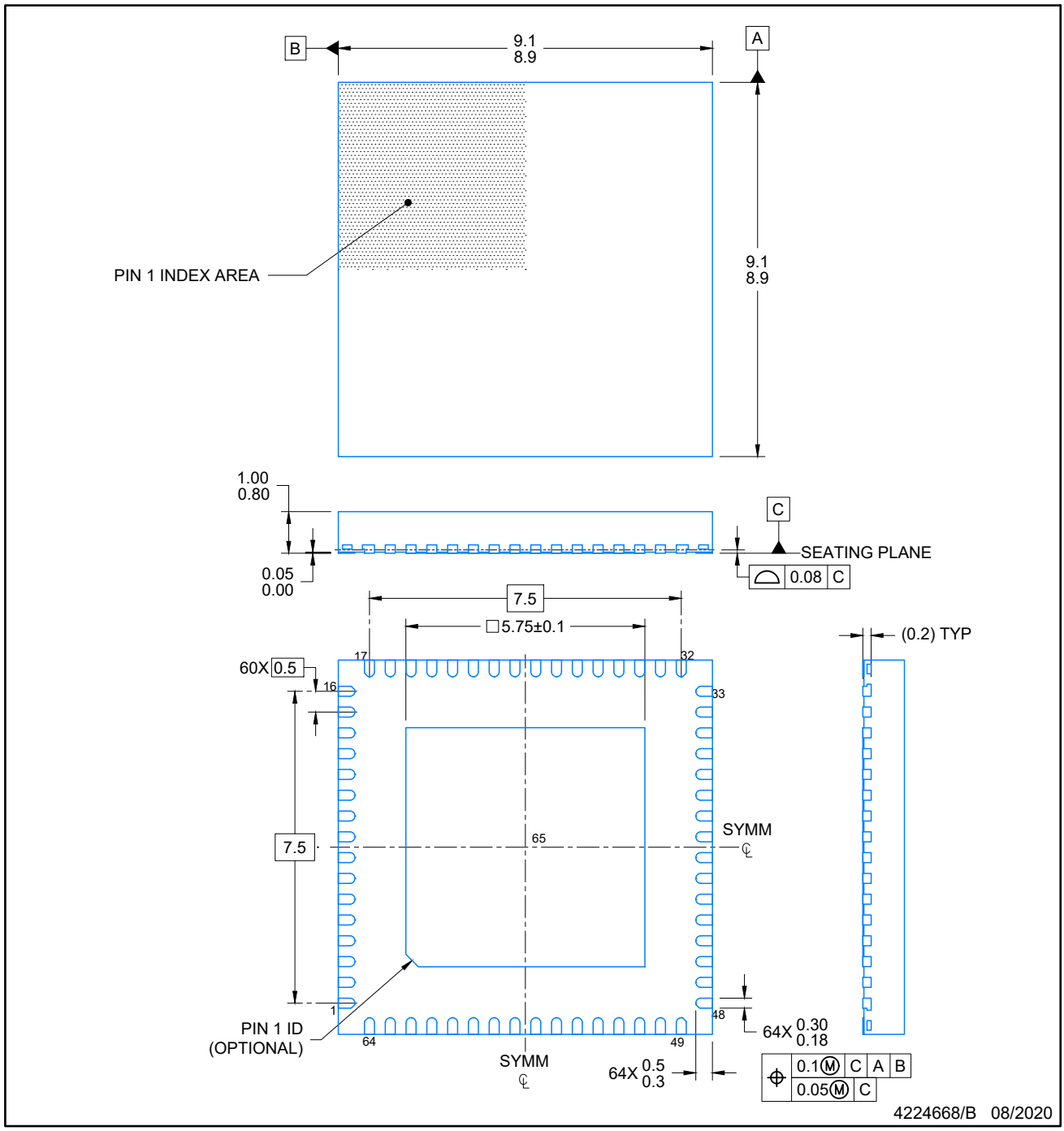
4224597/A

PACKAGE OUTLINE

RGC0064K

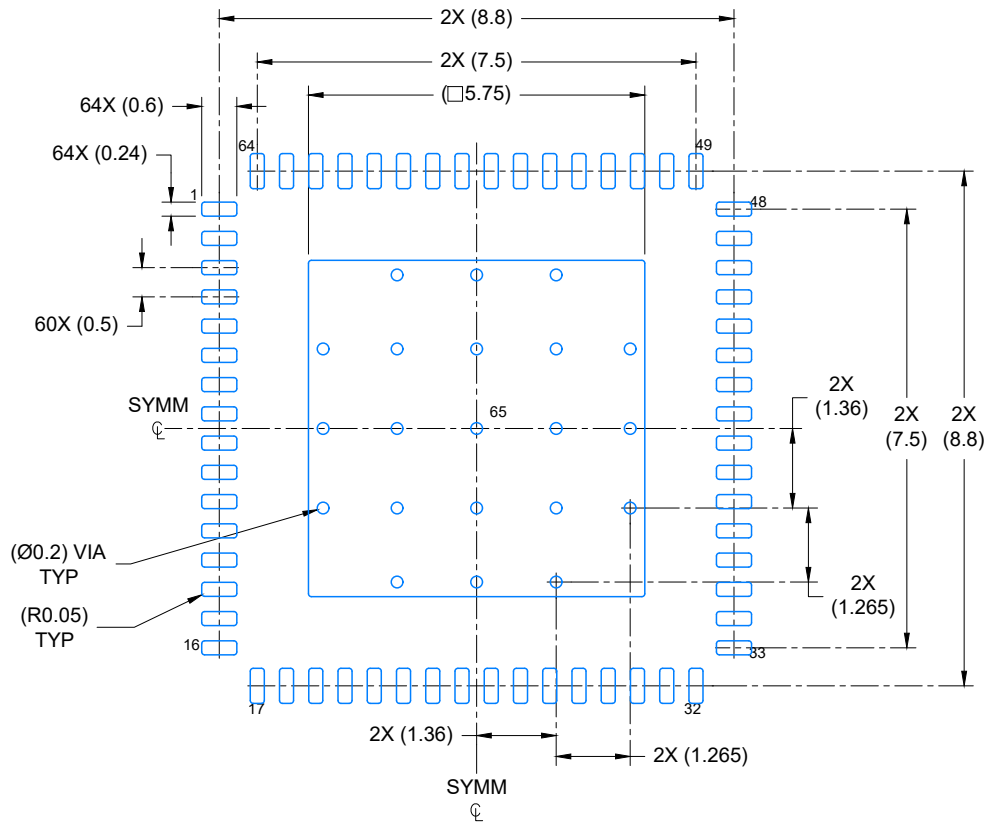
VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

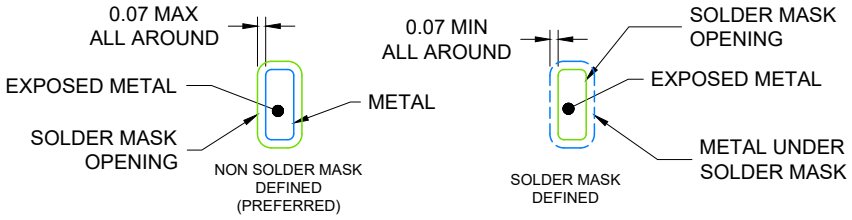


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

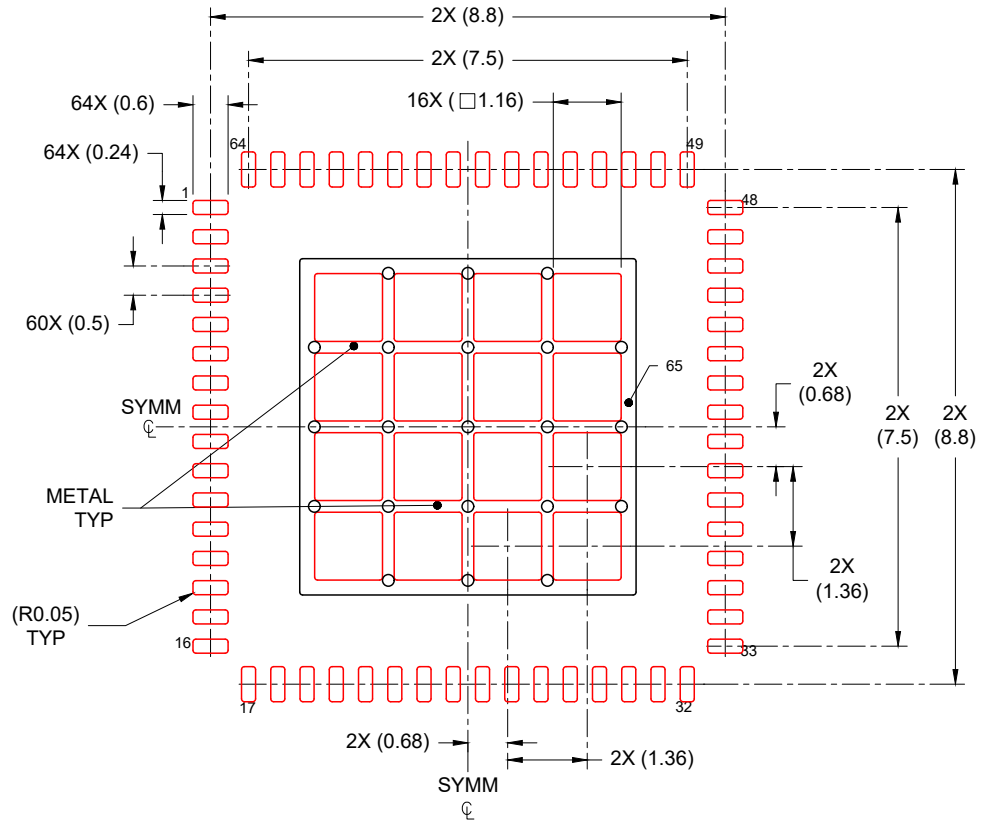


SOLDER MASK DETAILS

4224668/B 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED COVERAGE BY AREA
SCALE: 8X

4224668/B 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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