

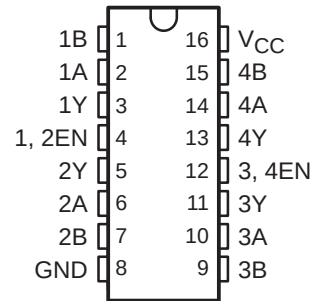
SN75ALS199

QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS046C – JANUARY 1989 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27
- Designed to Operate Up To 20 Mbaud
- -7 V to 7 V Common-Mode Input Voltage Range With 300-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . . 12 k Ω Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement
35 mA Max
- Improved Speed and Power Consumption Compared to MC3486

D OR N PACKAGE
(TOP VIEW)



description

The SN75ALS199 is a monolithic, quadruple line receiver with 3-state outputs designed using advanced, low-power, Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication, providing significantly less power consumption and permitting much higher data throughput than other designs. The device meets the specification of ITU Recommendations V.10, V.11, X.26, and X.27.

The SN75ALS199 features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open. The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high-input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 300 mV over a common-mode input voltage range of ± 7 V. It also features an active-high enable function for each of two receiver pairs. The SN75ALS199 is designed for optimum performance when used with the SN75ALS194 quadruple, differential line driver.

The SN75ALS199 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A-B	EN	OUTPUT Y
$V_{ID} \geq 0.3$ V	H	H
-0.3 V $< V_{ID} < 0.3$ V	H	?
$V_{ID} \leq -0.3$ V	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant,
? = indeterminate, Z = high impedance (off)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

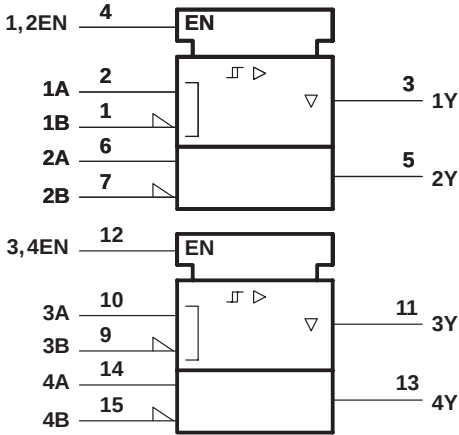
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated

SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER

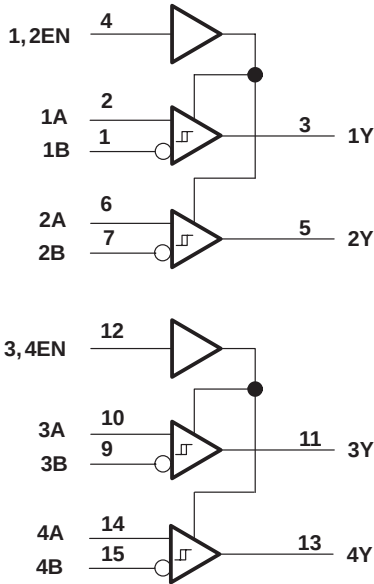
SLLS046C – JANUARY 1989 – REVISED MAY 1995

logic symbol†

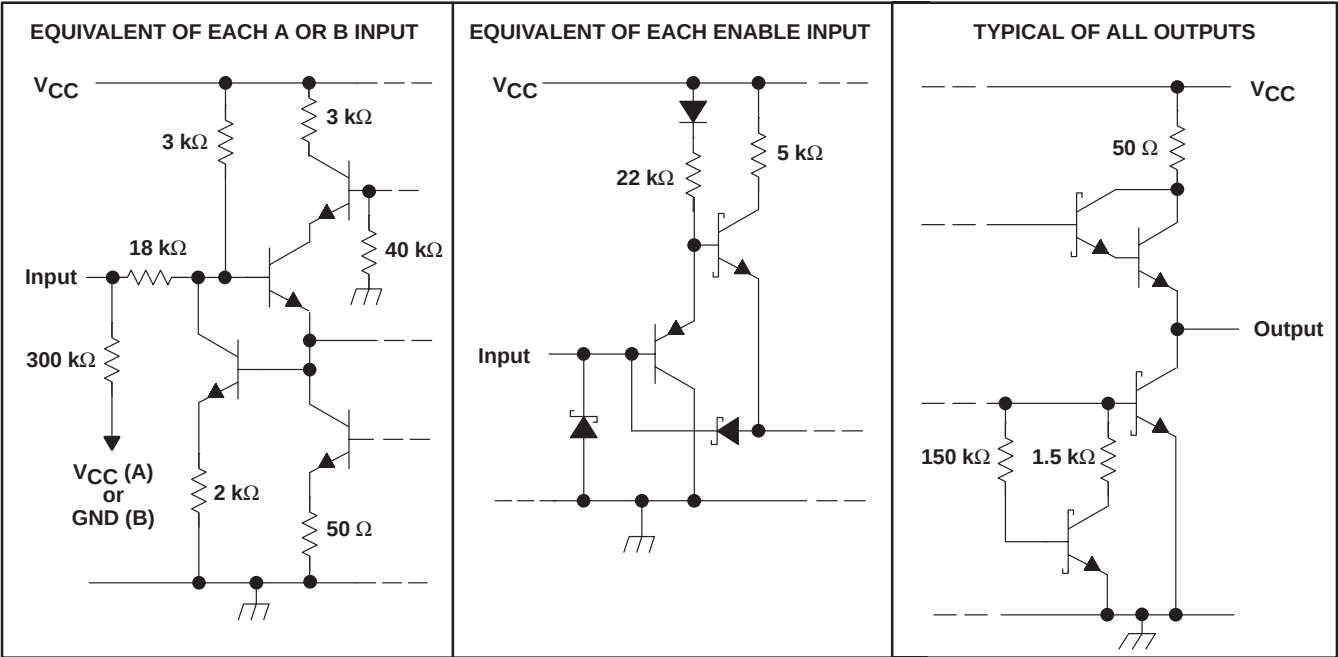


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I (A or B inputs)	± 15 V
Differential input voltage, V_{ID} (see Note 2)	± 15 V
Enable input voltage, V_I	7 V
Low-level output current, I_{OL}	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			± 7	V
Differential input voltage, V_{ID}			± 12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

SN75ALS199

QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS046C – JANUARY 1989 – REVISED MAY 1995

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage			300			mV
V _{IT−}	Negative-going input threshold voltage			−300 [‡]			mV
V _{hys}	Hysteresis voltage (V _{IT+} − V _{IT−})			120			mV
V _{IK}	Enable-input clamp voltage	I _I = −18 mA		−1.5			V
V _{OH}	High-level output voltage	V _{ID} = 300 mV,	I _{OH} = −400 μA	2.7	3.6		V
V _{OL}	Low-level output voltage	V _{ID} = −300 mV	I _{OL} = 8 mA	0.45		V	
			I _{OL} = 16 mA	0.5			
I _{OZ}	High-impedance-state output current	V _{IL} = 0.8 V, V _{ID} = −3 V,	V _O = 2.7 V	20		μA	
		V _{IL} = 0.8 V, V _{IO} = 3 V,	V _O = 0.5 V	−20			
I _I	Line input current	Other input at 0 V, See Note 3	V _I = 15 V	0.7	1.2	mA	
			V _I = −15 V	−1	−1.7		
I _{IH}	High-level enable-input current		V _{IH} = 2.7 V	20		μA	
			V _{IH} = 5.25 V	100			
I _{IL}	Low-level enable-input current	V _{IL} = 0.4 V		−100		μA	
	Input resistance			12	18	kΩ	
I _{OS}	Short-circuit output current [§]	V _{ID} = 3 V,	V _O = 0	−15	−78	−130	mA
I _{CC}	Supply current	Outputs disabled		22		35	mA

[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[‡] The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 3: Refer to ITU Recommendations V.10 and V.11 for exact conditions.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$V_{ID} = 0$ V to 3 V, $C_L = 15$ pF, See Figure 2	15	22		ns
t_{PHL} Propagation delay time, high- to low-level output		15	22		
t_{PZH} Output enable time to high level	$C_L = 15$ pF, See Figure 3	13	25		ns
t_{PZL} Output enable time to low level		11	25		
t_{PHZ} Output disable time from high level	$C_L = 15$ pF, See Figure 3	13	25		ns
t_{PLZ} Output disable time from low level		15	22		



PARAMETER MEASUREMENT INFORMATION

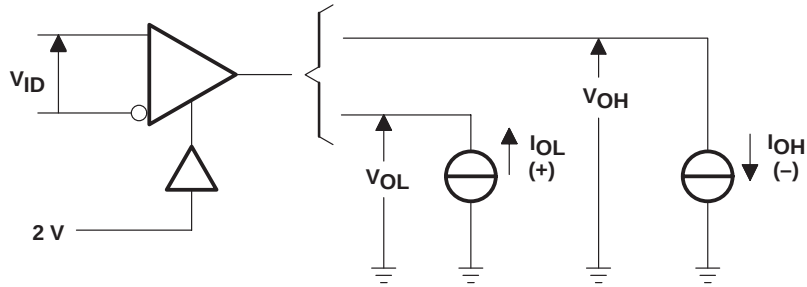
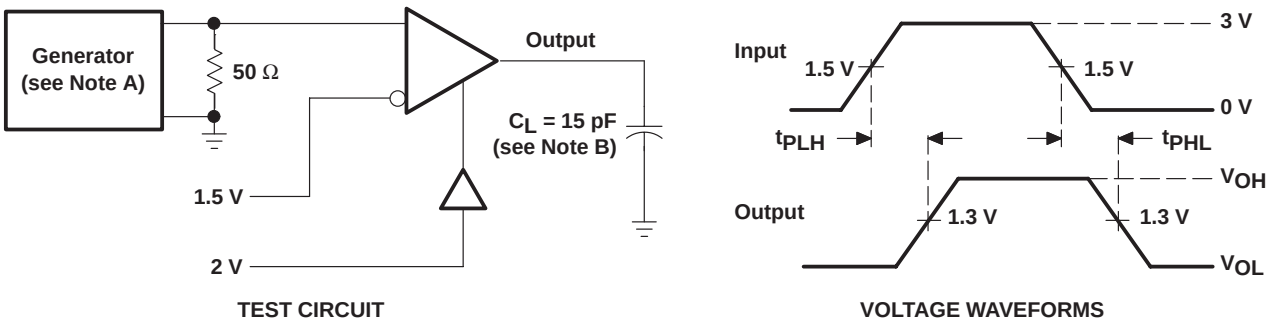


Figure 1. V_{OH} and V_{OL} Test Circuit



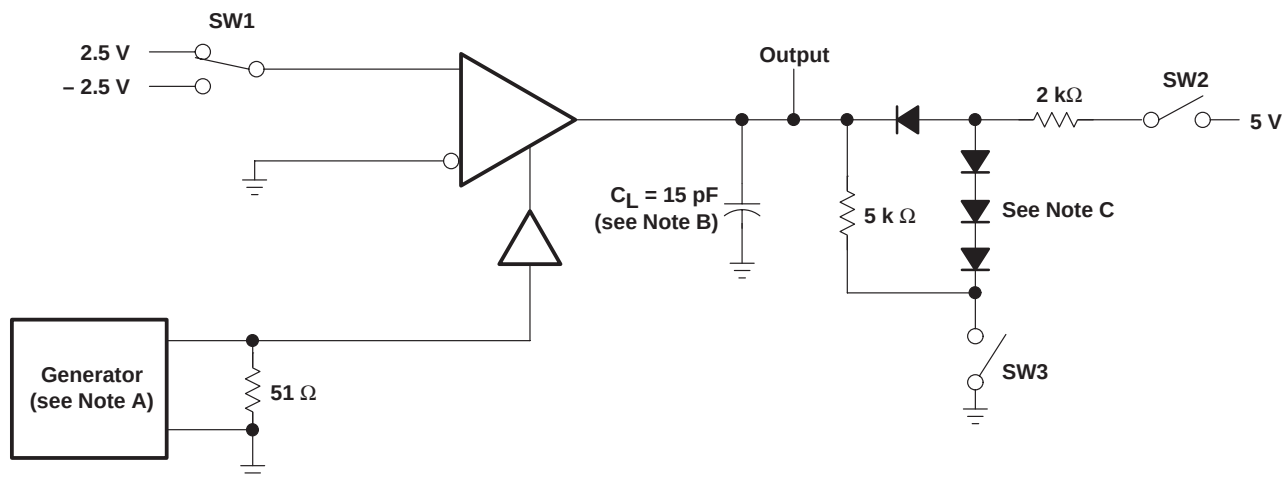
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_O = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

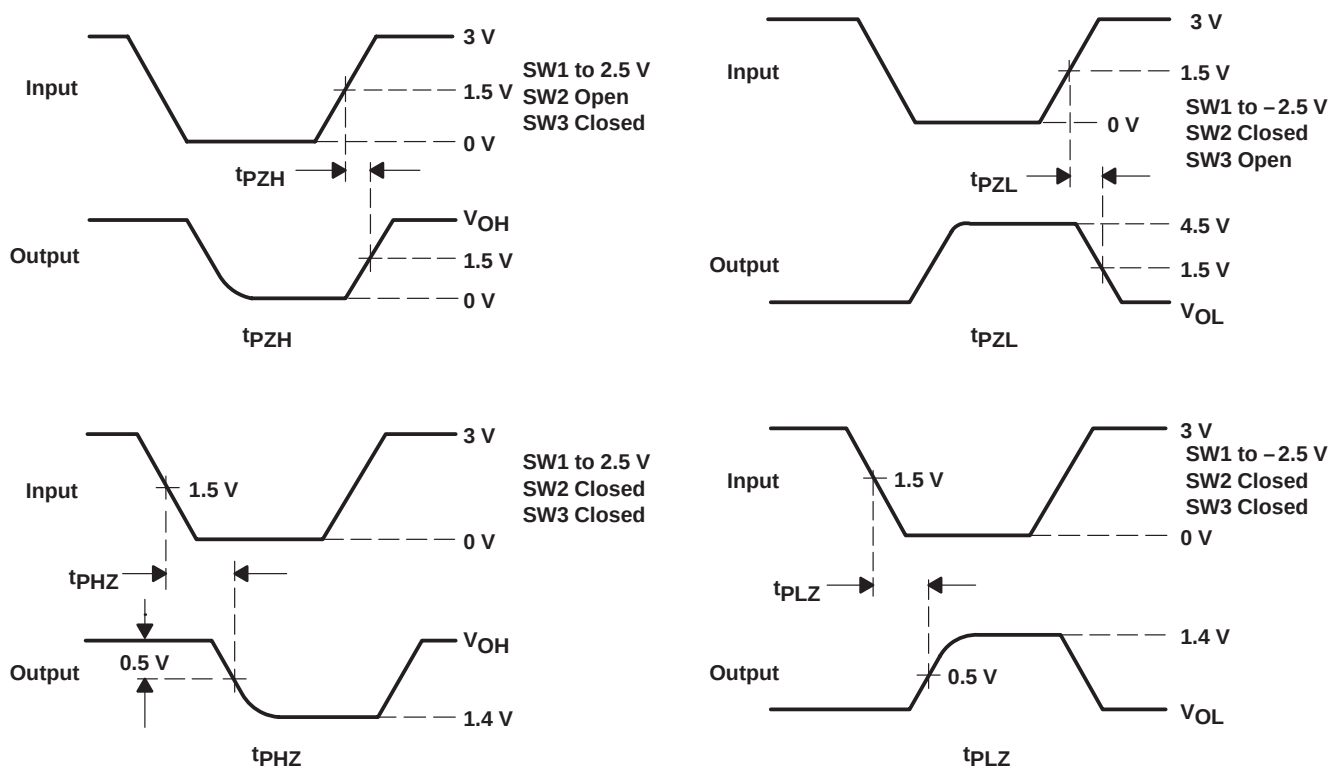
SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS046C – JANUARY 1989 – REVISED MAY 1995

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_O = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

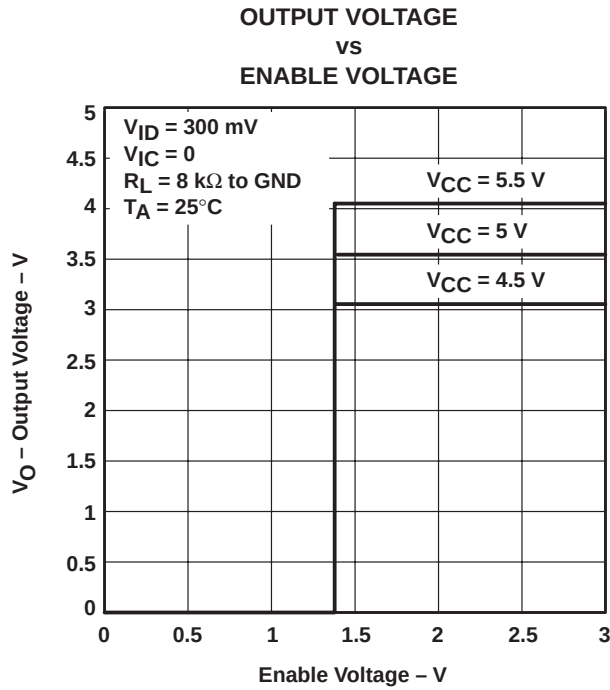


Figure 4

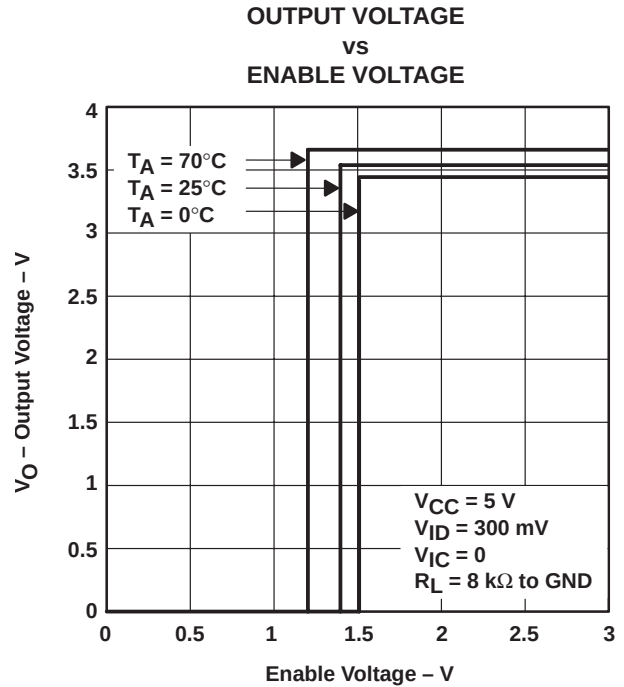


Figure 5

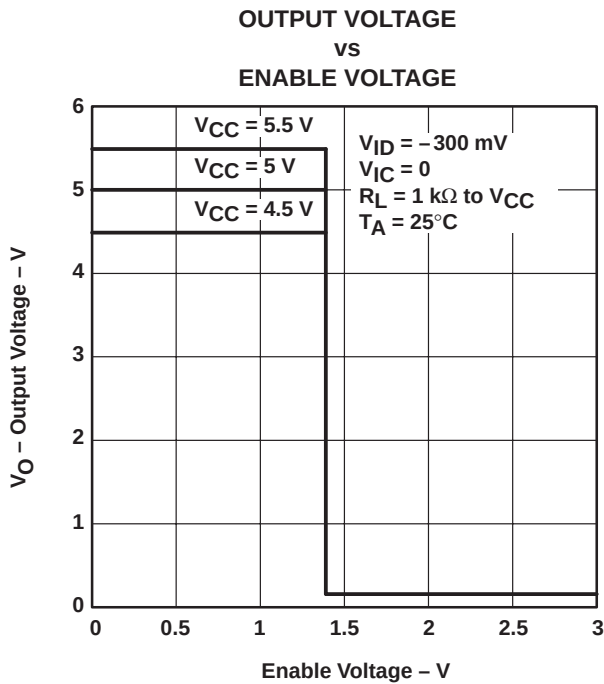


Figure 6

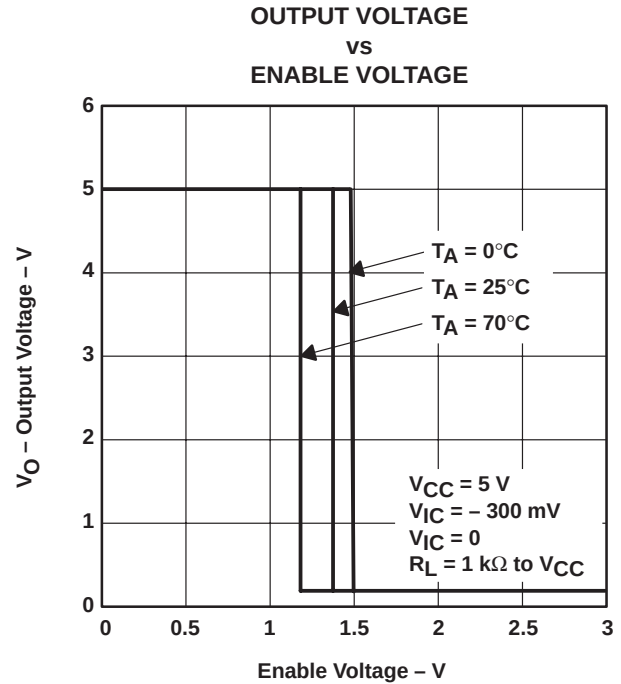


Figure 7

SN75ALS199
QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS046C – JANUARY 1989 – REVISED MAY 1995

TYPICAL CHARACTERISTICS

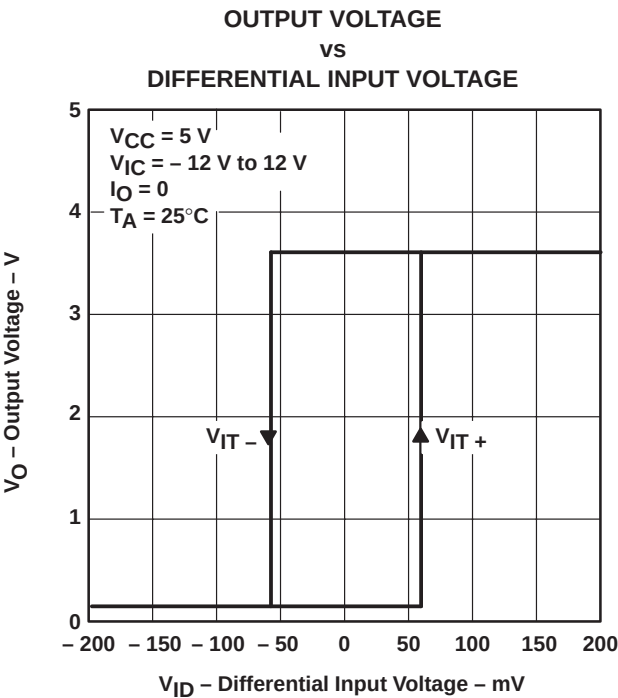


Figure 8

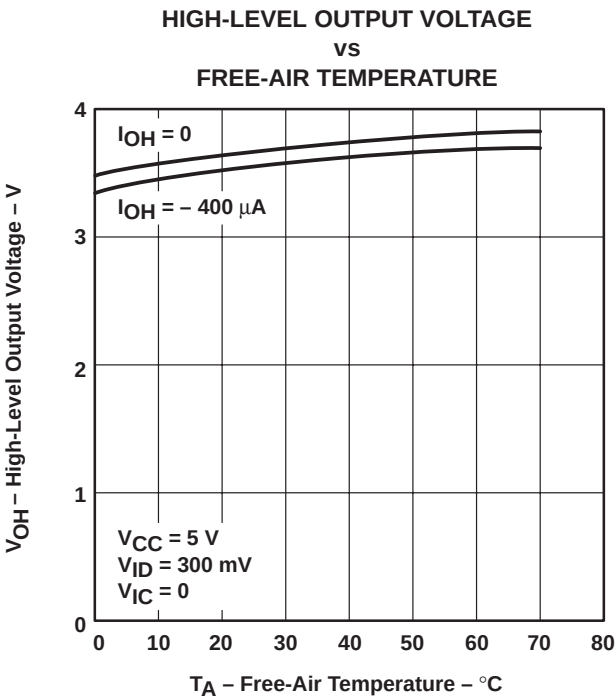


Figure 9

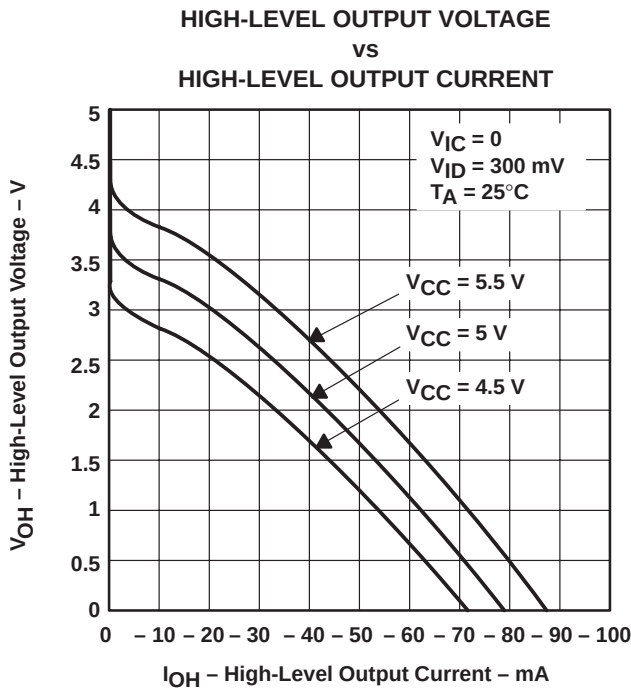


Figure 10

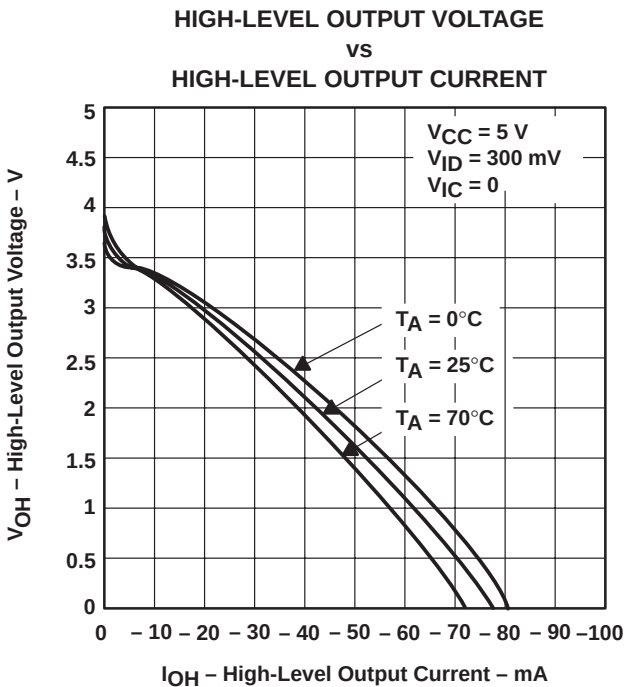


Figure 11

TYPICAL CHARACTERISTICS

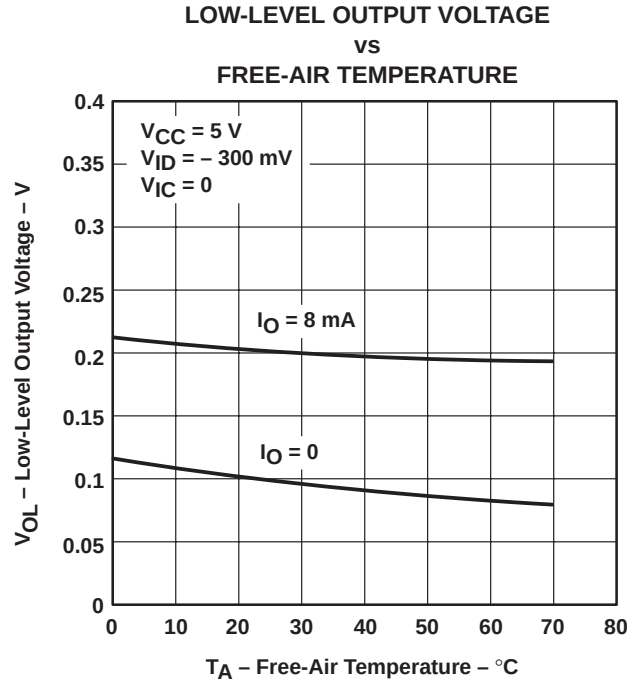


Figure 12

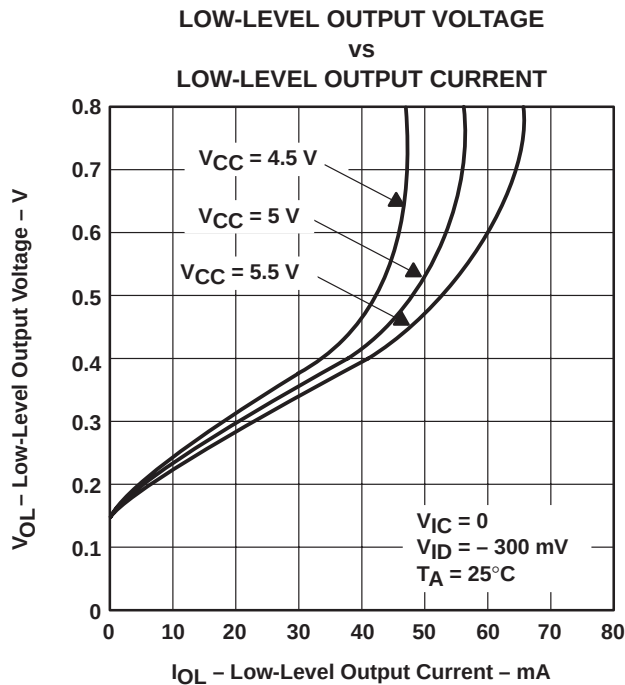


Figure 13

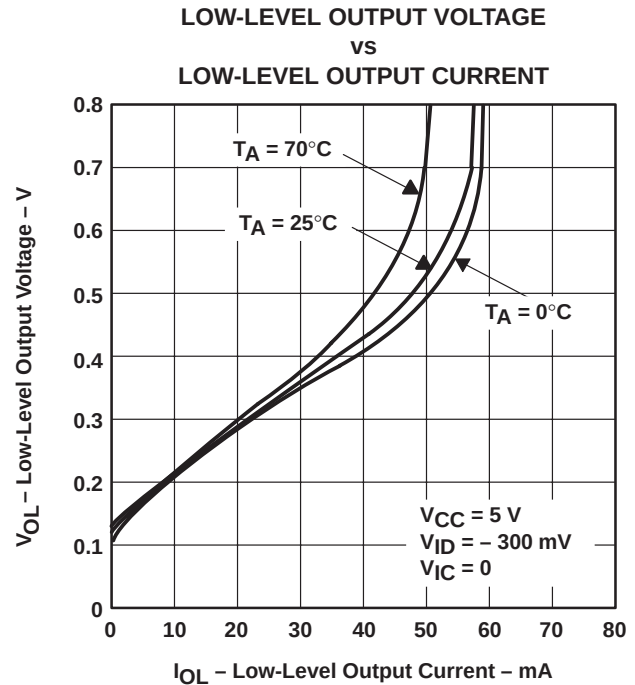


Figure 14

SN75ALS199

QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS046C – JANUARY 1989 – REVISED MAY 1995

TYPICAL CHARACTERISTICS

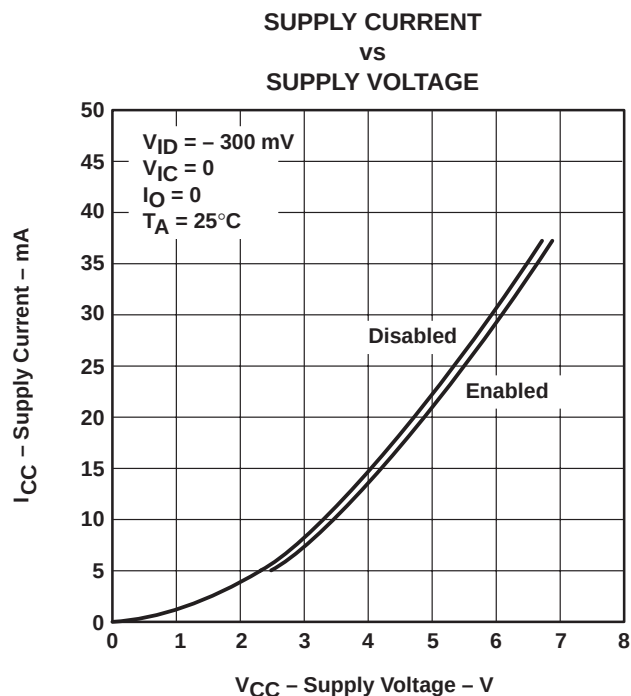


Figure 15

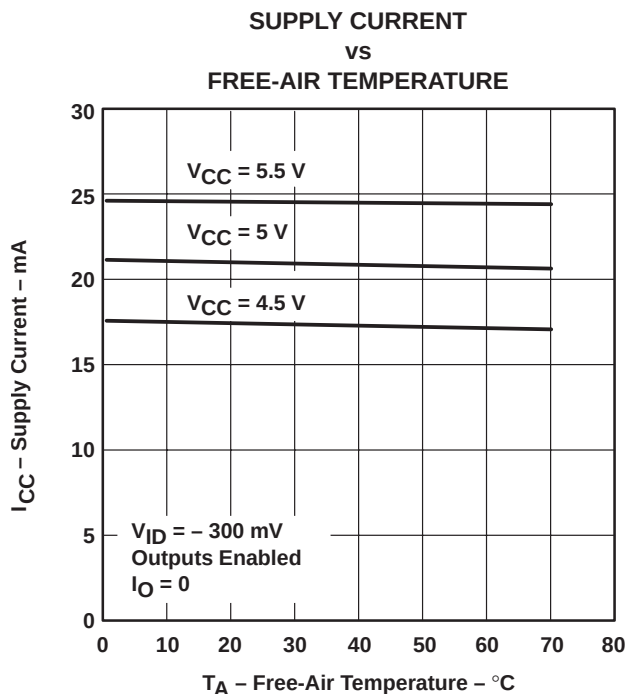


Figure 16

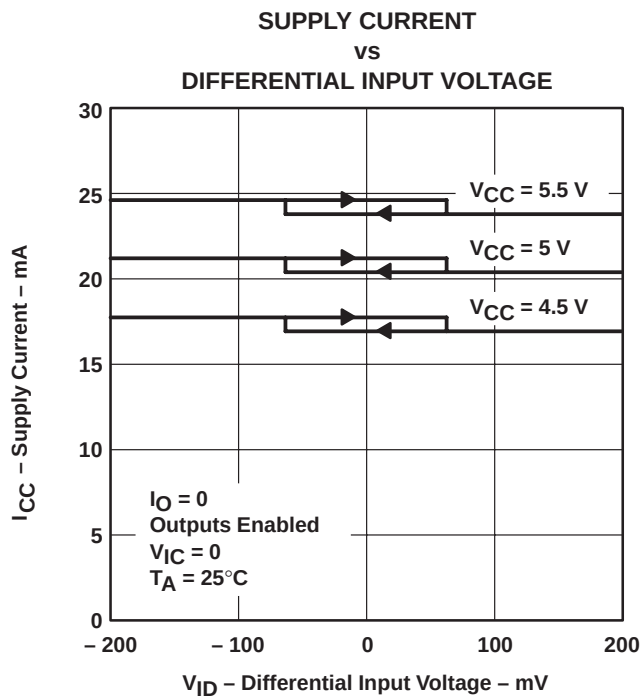


Figure 17

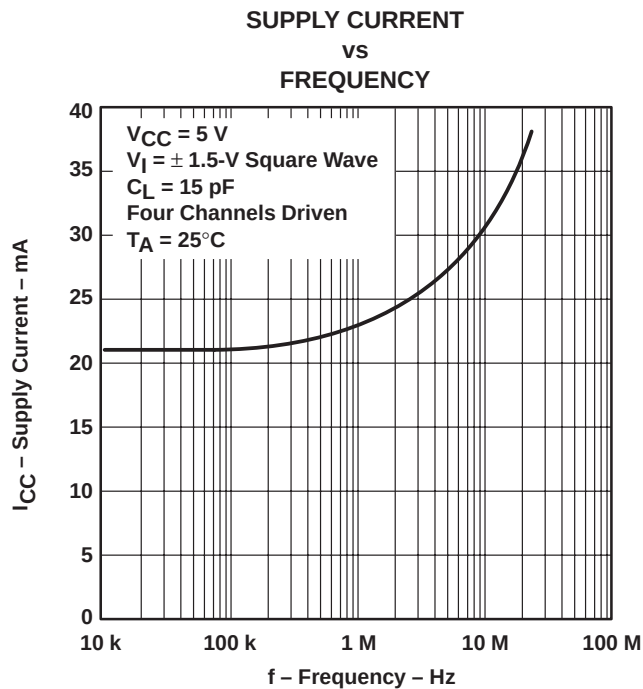


Figure 18

TYPICAL CHARACTERISTICS

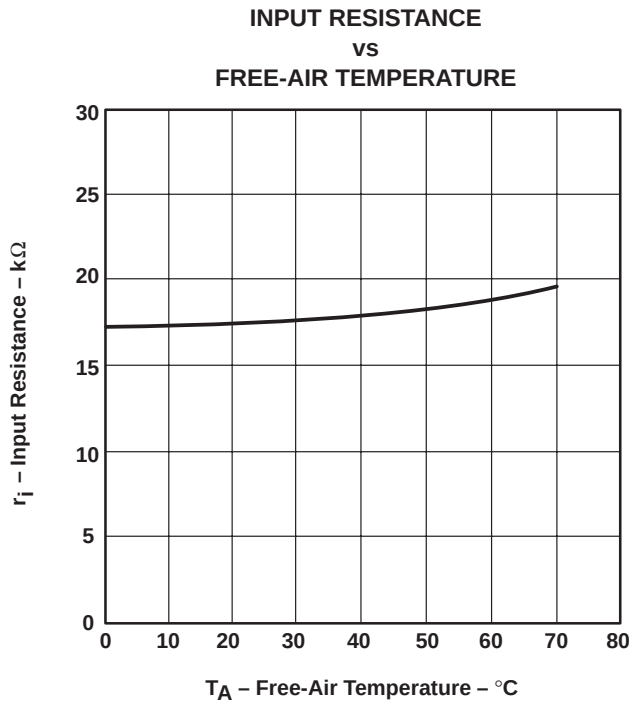


Figure 19

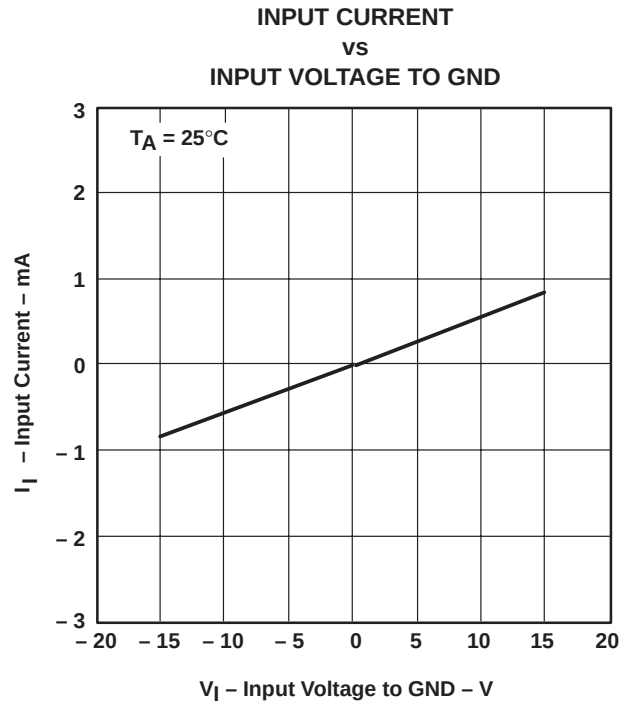


Figure 20

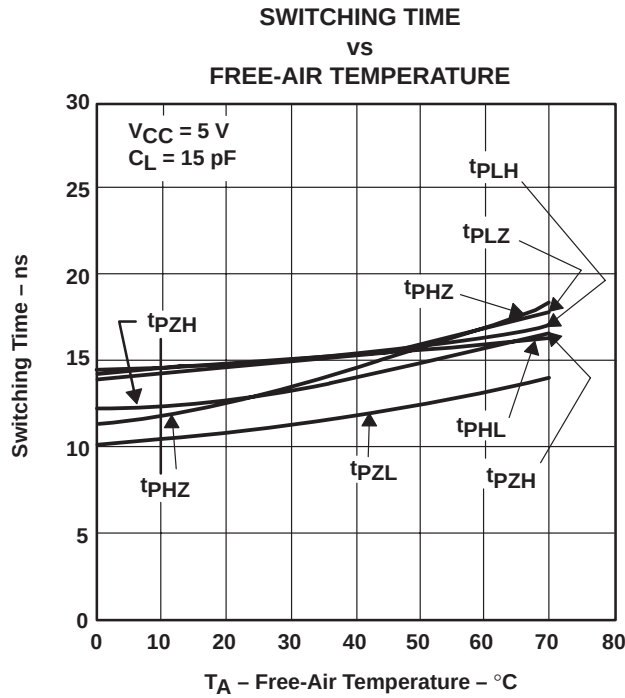


Figure 21

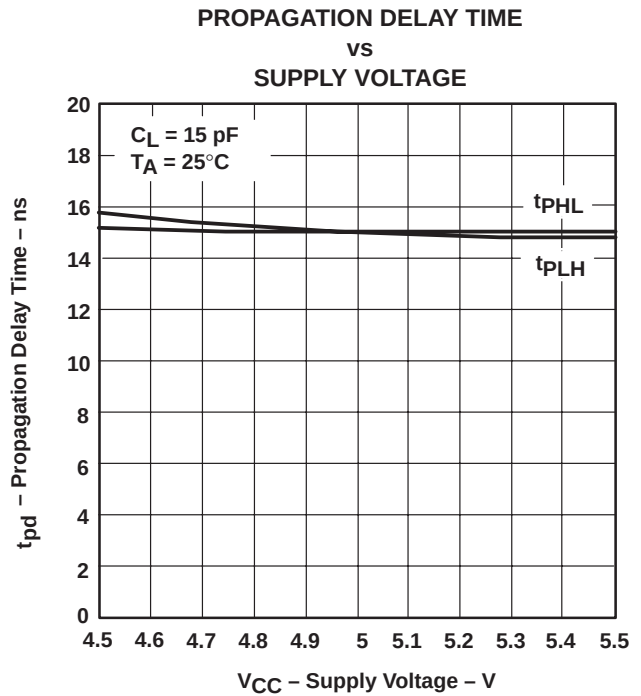


Figure 22

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75ALS199D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS199
SN75ALS199D.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS199
SN75ALS199DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS199
SN75ALS199DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS199
SN75ALS199N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS199N
SN75ALS199N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS199N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

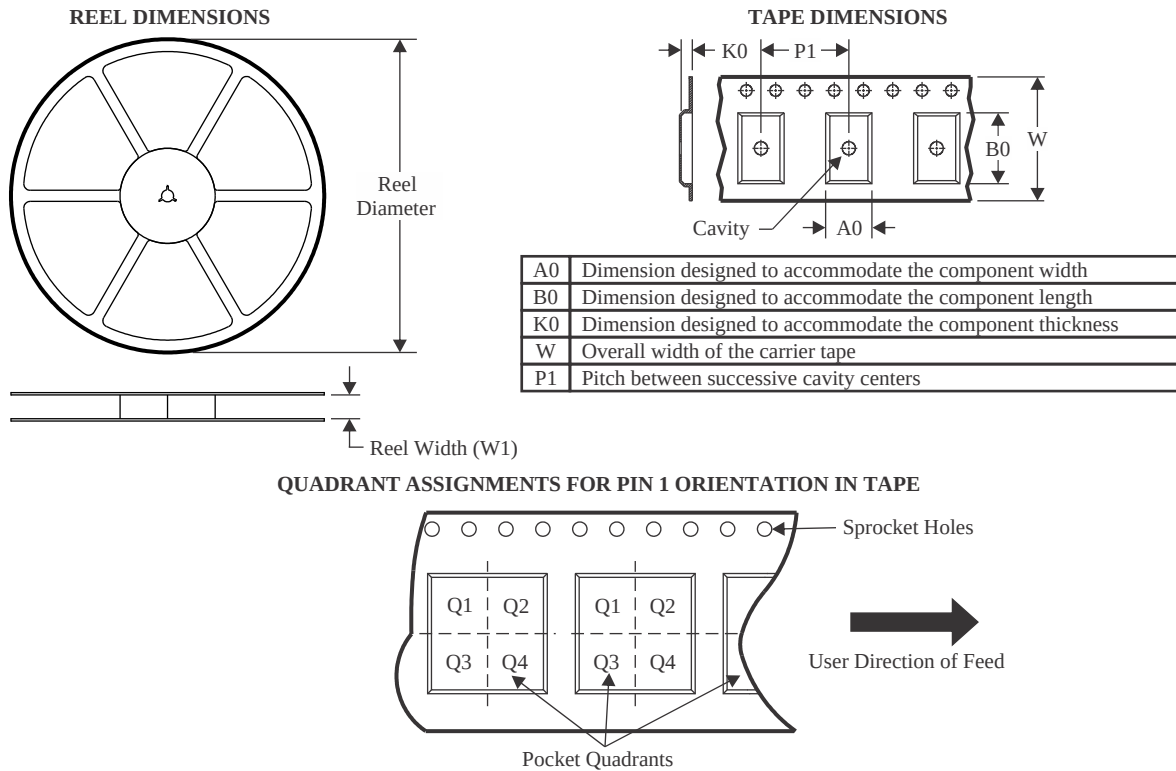
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

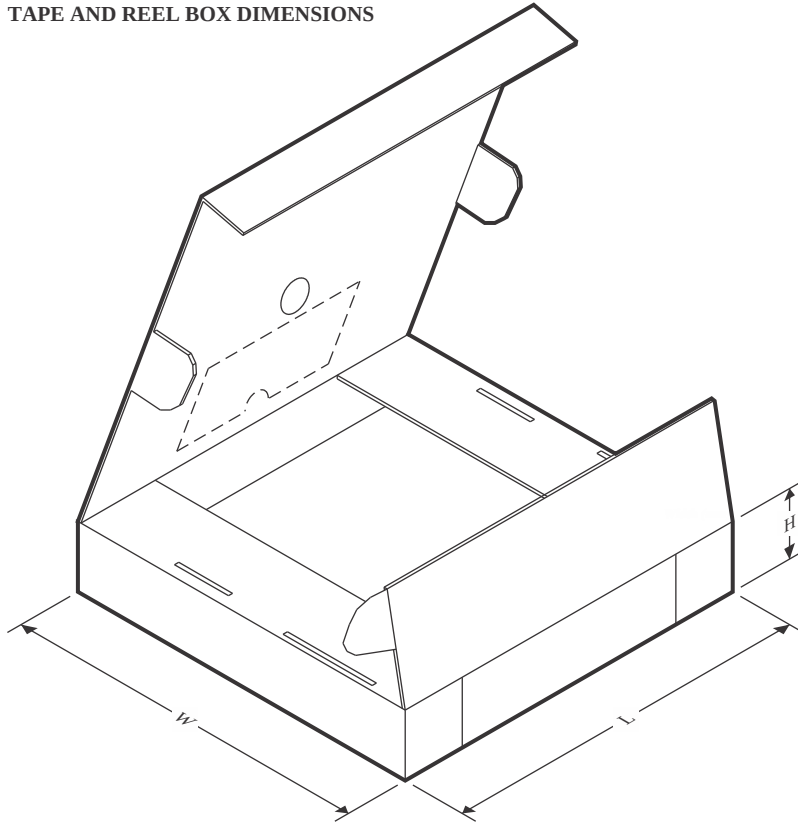
TAPE AND REEL INFORMATION



*All dimensions are nominal

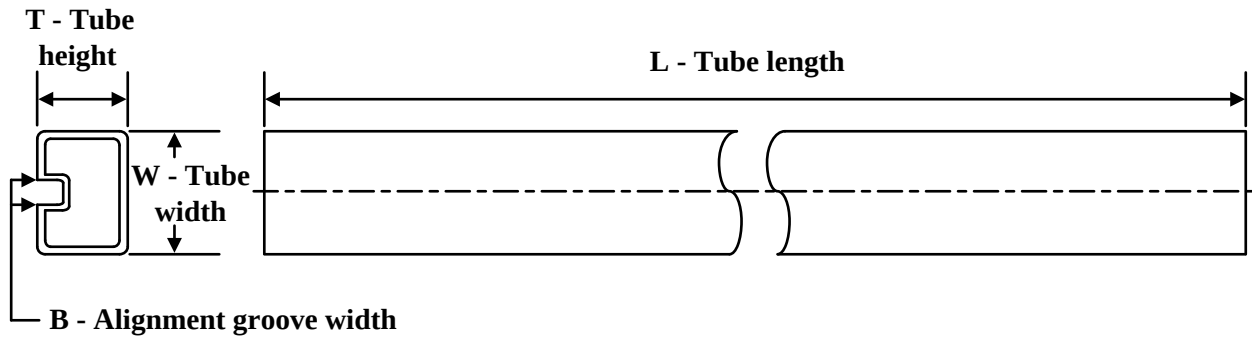
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS199DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS199DR	SOIC	D	16	2500	353.0	353.0	32.0

TUBE


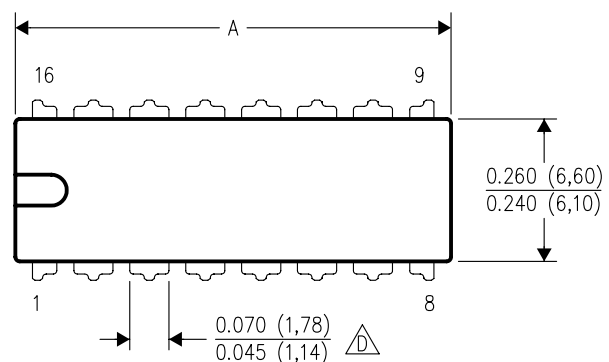
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS199D	D	SOIC	16	40	507	8	3940	4.32
SN75ALS199D.A	D	SOIC	16	40	507	8	3940	4.32
SN75ALS199N	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS199N.A	N	PDIP	16	25	506	13.97	11230	4.32

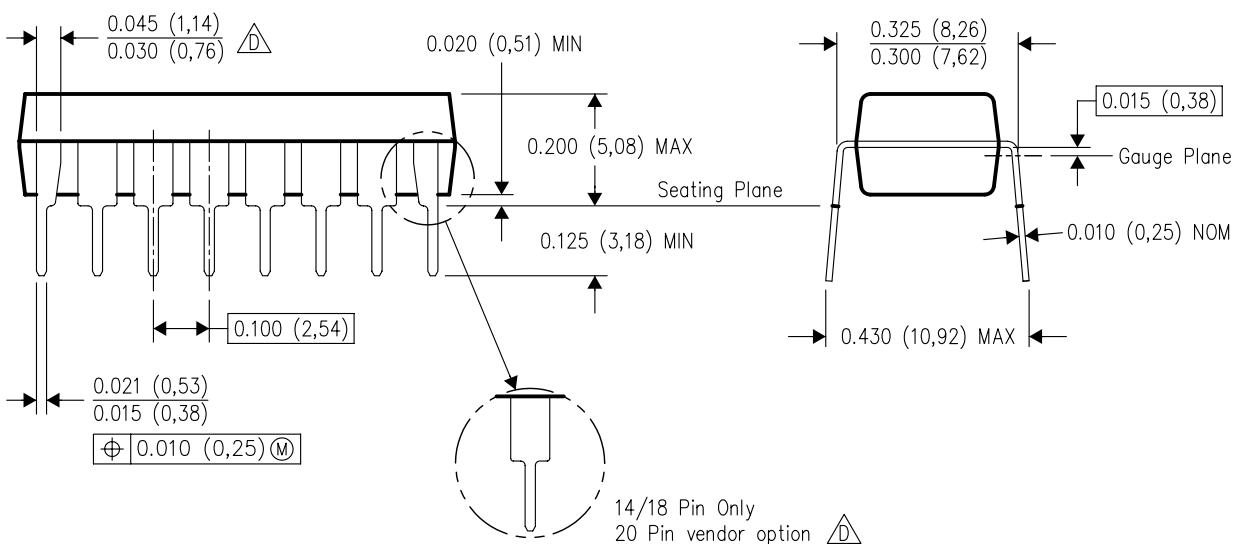
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



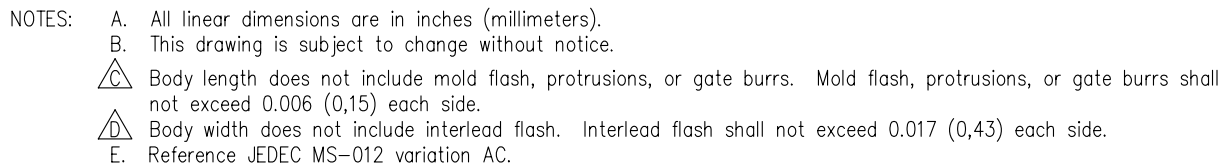
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated