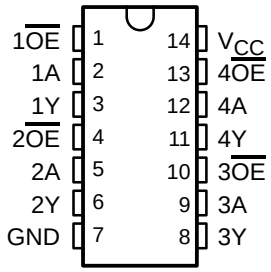
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V $V_{CC}$**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 1000 V Per MIL-STD-833, Method 3015; Exceeds 150 V Using Machine Model (C = 200 pF, R = 0)**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

**D OR PW PACKAGE**
**(TOP VIEW)**




## description/ordering information

The SN74AHC125 is a quadruple bus buffer gate featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, the respective gate passes the data from the A input to its Y output.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –55°C to 125°C | SOIC – D | Tape and reel | SN74AHC125MDREP | AHC125MEP |
| | TSSOP – PW | Tape and reel | SN74AHC125MPWREP | AH125EP |

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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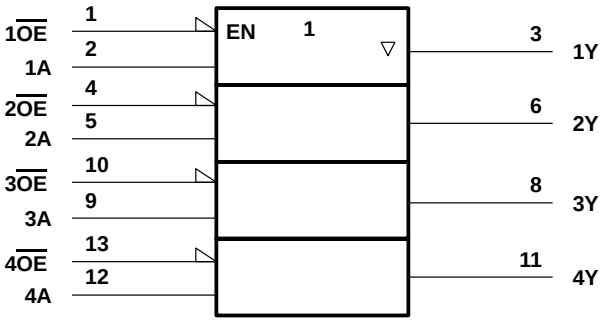
**FUNCTION TABLE**
**(each buffer)**

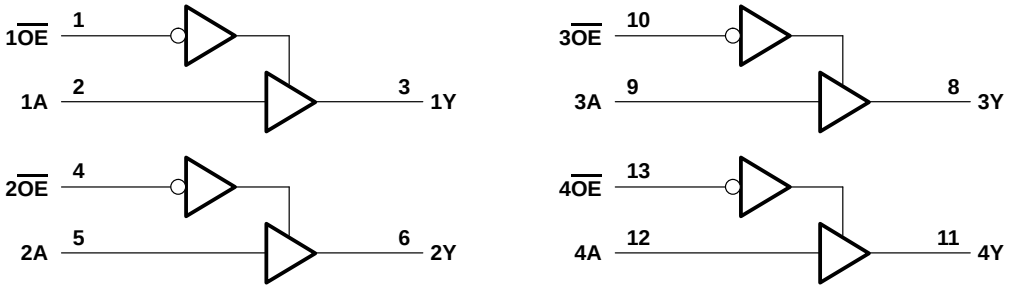
| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$ (see Note 1) | –0.5 V to 7 V |
| Output voltage range, $V_O$ (see Note 1) | –0.5 V to $V_{CC}$ + 0.5 V |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | –20 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) | ±20 mA |
| Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) | ±25 mA |
| Continuous current through $V_{CC}$ or GND | ±50 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package | 86°C/W |
| PW package | 113°C/W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5.6 | 8 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.4 | 8 | 1 | 9.5 | ns |
| $t_{PZL}$ | | | | | 5.4 | 8 | 1 | 9.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7 | 9.7 | 1 | 11.5 | ns |
| $t_{PLZ}$ | | | | | 7 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 8.1 | 11.5 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.5 | 1 | 13 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.9 | 11.5 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 7.9 | 11.5 | 1 | 13 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 9.5 | 13.2 | 1 | 15 | ns |
| $t_{PLZ}$ | | | | | 9.5 | 13.2 | 1 | 15 | |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 3.6 | 5.1 | 1 | 6 | ns |
| $t_{PZL}$ | | | | | 3.6 | 5.1 | 1 | 6 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$ | | | | | 4.6 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 5.1 | 7.1 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 5.1 | 7.1 | 1 | 8 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

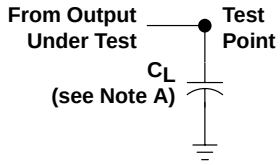
| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.4 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

NOTE 4: Characteristics are for surface-mount packages only.

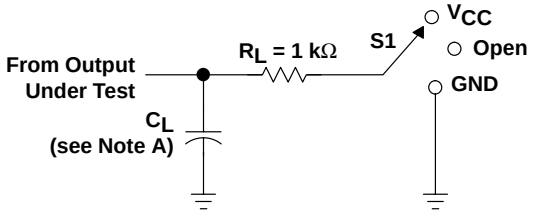
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 14 | pF |

## PARAMETER MEASUREMENT INFORMATION

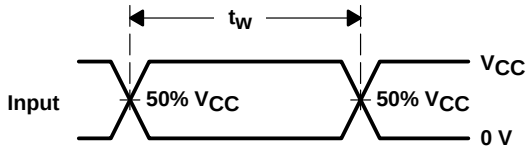



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

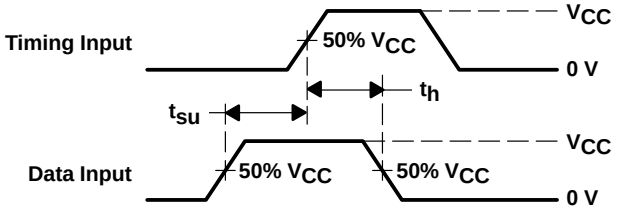



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

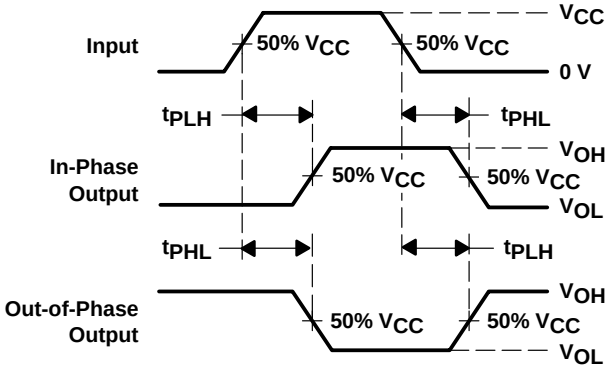
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



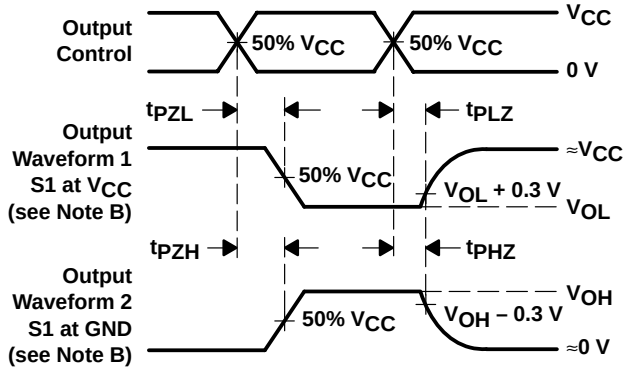

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AHC125MDREP | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AHC125MEP |
| SN74AHC125MDREP.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AHC125MEP |
| SN74AHC125MPWREP | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AH125EP |
| SN74AHC125MPWREP.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AH125EP |
| V62/03648-01XE | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AH125EP |
| V62/03648-01YE | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AHC125MEP |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN74AHC125-EP :**

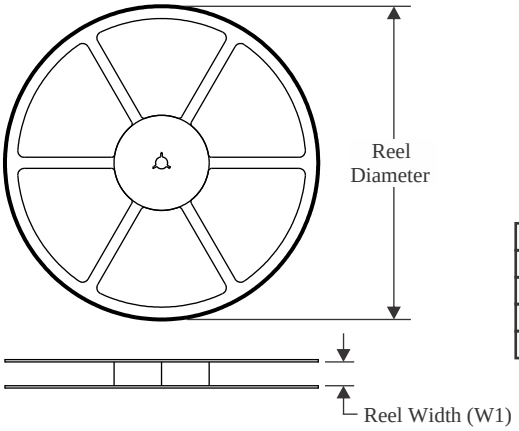
- Catalog : SN74AHC125
- Automotive : SN74AHC125-Q1
- Military : SN54AHC125

NOTE: Qualified Version Definitions:

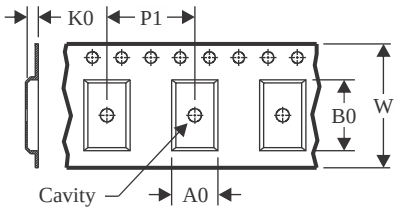
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

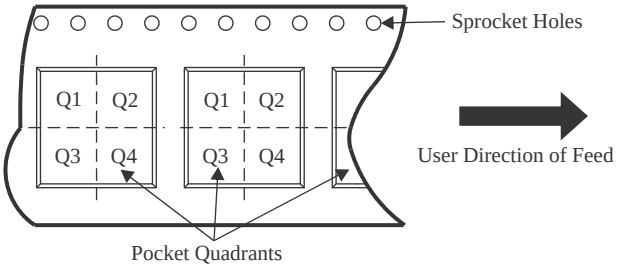



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

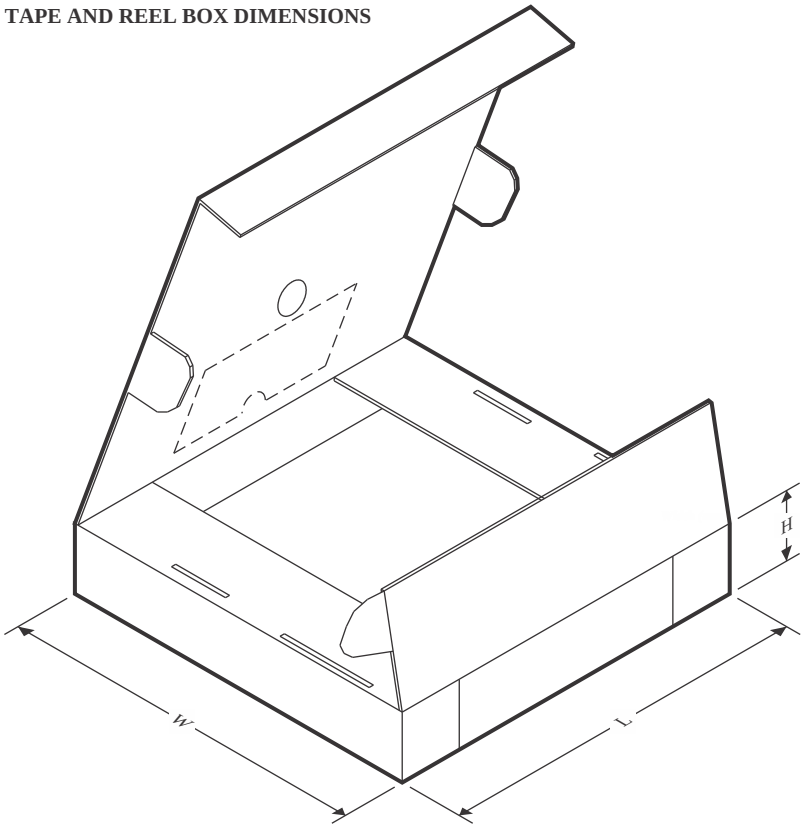
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHC125MDREP | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AHC125MPWREP | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AHC125MDREP | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74AHC125MPWREP | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |

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