

CD40175B Types

CMOS Quad 'D'-Type Flip-Flop

High-Voltage Types (20-Volt Rating)

Features:

- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
1 V at $V_{DD} = 5$ V
2 V at $V_{DD} = 10$ V
2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Output compatible with two HTL loads, two low power TTL loads, or one low power Schottky TTL load
- Functional equivalent to TTL 74175
- Standardized symmetrical output characteristics

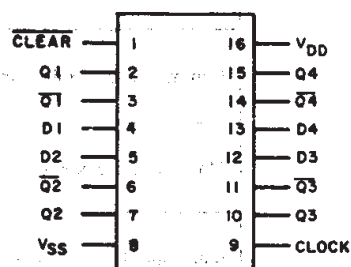
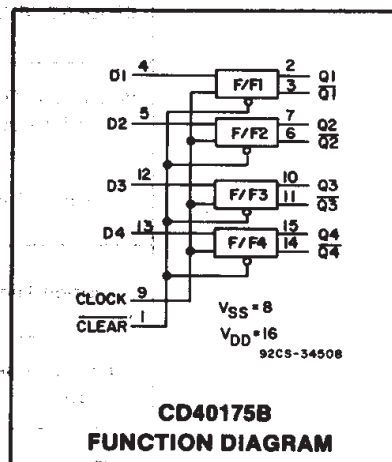
Applications:

- Shift registers
- Buffer/storage registers
- Pattern generators

■ CD40175B consists of four identical D-type flip-flops. Each flip-flop has an independent DATA D input and complementary Q and $\bar{Q}$ outputs. The CLOCK and CLEAR inputs are common to all flip-flops. Data are transferred to the Q outputs on the positive-going transition of the clock pulse. All four flip-flops are simultaneously reset by a low level on the CLEAR input.

These devices can function as shift register elements or as T-type flip-flops for toggle and counter applications.

The CD40175B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).



V_{DD} = PIN 16

V_{SS} = PIN 8

92CS-34507

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal)

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to +20V

DC INPUT CURRENT, ANY ONE INPUT -0.5V to $V_{DD} + 0.5$ V

POWER DISSIPATION PER PACKAGE (P_D): ± 10 mA

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package-Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10s max $+265^\circ\text{C}$

CD40175B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	—	3	18	V
Data Setup Time t_{SU}	5	120	—	ns
	10	50	—	
	15	40	—	
Data Hold Time t_H	5	80	—	ns
	10	40	—	
	15	30	—	
Clock Input Frequency f_{CL}	5	—	2	MHz
	10	dc	5	
	15	—	6.5	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}	5	—	15	μs
	10	—	15	
	15	—	15	
Clock Input Pulse Width t_{WL}, t_{WH}	5	250	—	ns
	10	100	—	
	15	75	—	
Clear Pulse Width t_{WL}	5	200	—	ns
	10	80	—	
	15	60	—	
Clear Removal Time t_{REM}	5	250	—	ns
	10	100	—	
	15	80	—	

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs

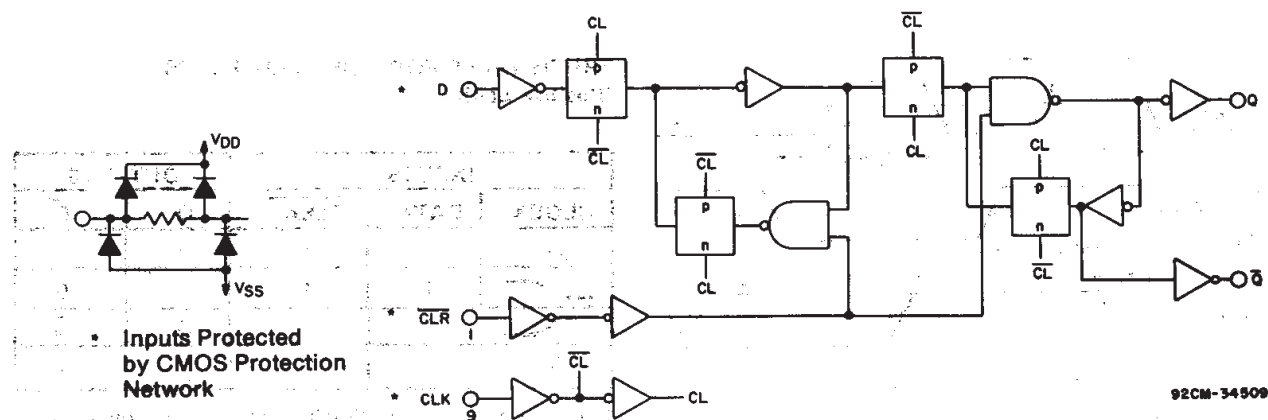


Fig. 1 - Logic diagram (1 of 4 flip-flops).

CD40175B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
		Vo (V)	VIN (V)	VDD (V)	-55	-40	+85	+125	+25			
									Min.	Typ.	Max.	
Quiescent Device Current Max.	IDD	—	0, 5	5	1	1	30	30	—	0.02	1	μA
		—	0, 10	10	2	2	60	60	—	0.02	2	
		—	0, 15	15	4	4	120	120	—	0.02	4	
		—	0, 20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current Min.	IOL	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
		0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
		1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current Min.	IOH	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
		2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
		9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
		13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level Max.	VOL	—	0, 5	5	0.05				—	0	0.05	V
		—	0, 10	10	0.05				—	0	0.05	
		—	0, 15	15	0.05				—	0	0.05	
Output Voltage: High-Level Min.	VOH	—	0, 5	5	4.95				4.95	5	—	V
		—	0, 10	10	9.95				9.95	10	—	
		—	0, 15	15	14.95				14.95	15	—	
Input Low Voltage Max.	VIL	0.5,4.5	—	5	1.5				—	—	1.5	V
		1, 9	—	10	3				—	—	3	
		1.5,13.5	—	15	4				—	—	4	
Input High Voltage Min.	VIH	0.5,4.5	—	5	3.5				3.5	—	—	V
		1, 9	—	10	7				7	—	—	
		1.5,13.5	—	15	11				11	—	—	
Input Current Max.	IIN	—	0, 18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

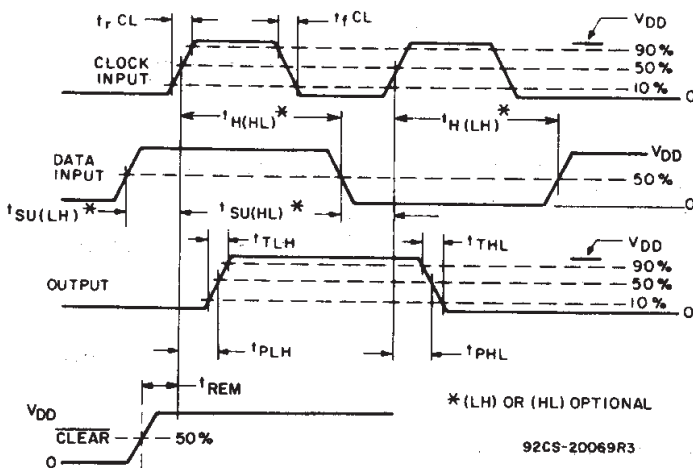


Fig. 2 - Definition of setup, hold, propagation delay, and removal times.

TRUTH TABLE FOR 1 OF 4 FLIP-FLOPS (Positive Logic)

INPUTS			OUTPUTS	
CLOCK	DATA	CLEAR	Q	$\overline{Q}$
	0	1	0	1
	1	1	1	0
	X	1	Q	$\overline{Q}$
X	X	0	0	1

1=High Level

X=Don't Care

0=Low Level

CD40175B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Transition Time t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Propagation Delay Time Clock to Q Output t_{PHL}, t_{PLH}	5	—	220	400	
	10	—	90	160	
	15	—	70	120	
Propagation Delay Time $\overline{\text{CLEAR}}$ to Q Output t_{PHL}	5	—	325	500	
	10	—	130	200	
	15	—	100	150	
Minimum Pulse Width Clock t_{WH}	5	—	110	250	
	10	—	45	100	
	15	—	35	75	
$\overline{\text{Clear}}$ t_{WL}	5	—	100	200	
	10	—	40	80	
	15	—	30	60	
Maximum Clock Frequency f_{CL}	5	2	4.5	—	MHz
	10	5	11	—	
	15	6.5	14	—	
Maximum Clock Rise or Fall Time t_{rCL}, t_{fCL}	5	15	—	—	μs
	10	15	—	—	
	15	15	—	—	
Minimum Data Setup Time t_{SU}	5	—	60	120	ns
	10	—	25	50	
	15	—	20	40	
Minimum Data Hold Time t_H	5	—	40	80	
	10	—	20	40	
	15	—	15	30	
Minimum $\overline{\text{Clear}}$ Removal Time $\ddagger$ t_{REM}	5	—	125	250	
	10	—	50	100	
	15	—	40	80	
Input Capacitance C_{IN}	—	—	5	7.5	pF

$\ddagger$ $\overline{\text{CLEAR}}$ signal must be high prior to positive-going transition of CLOCK pulse.

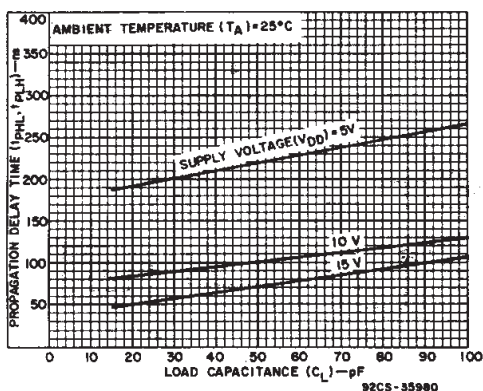


Fig. 3 - Typical propagation delay time (CLOCK to OUTPUT) as a function of load capacitance.

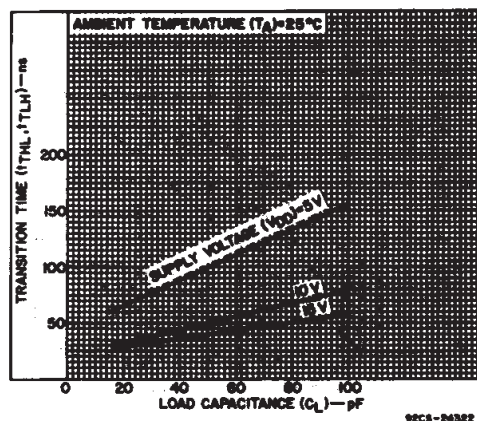


Fig. 4 - Typical transition time as a function of load capacitance.

CD40175B Types

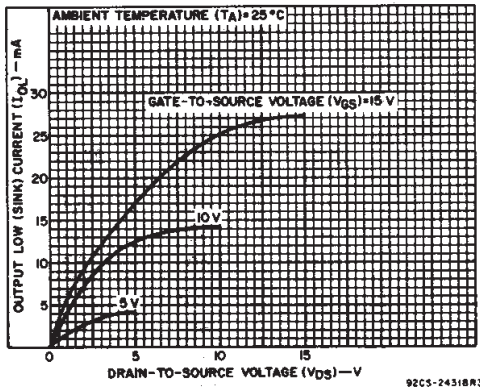


Fig. 5 - Typical output low (sink) current characteristics.

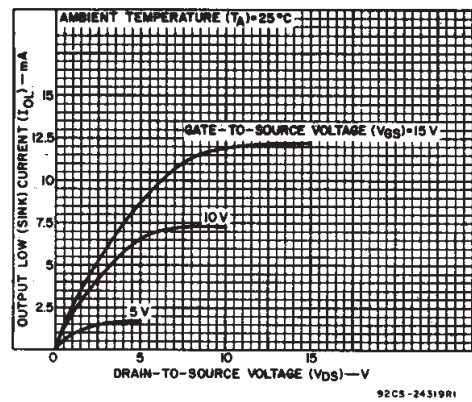


Fig. 6 - Minimum output low (sink) current characteristics.

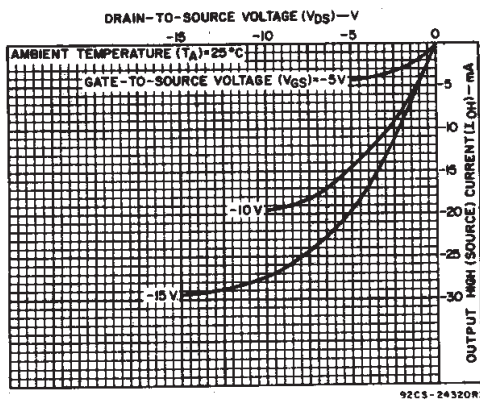


Fig. 7 - Typical output high (source) current characteristics.

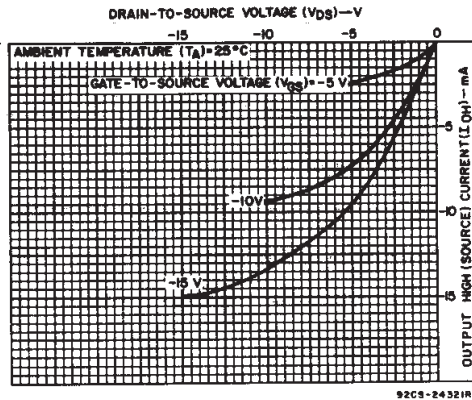


Fig. 8 - Minimum output high (source) current characteristics.

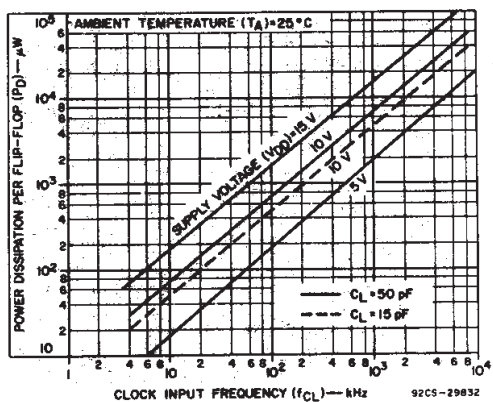


Fig. 9 - Typical dynamic power dissipation as a function of CLOCK frequency.

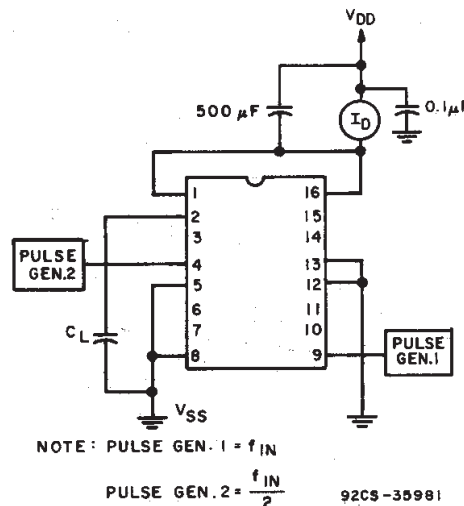


Fig. 10 - Dynamic power dissipation test circuit.

CD40175B Types

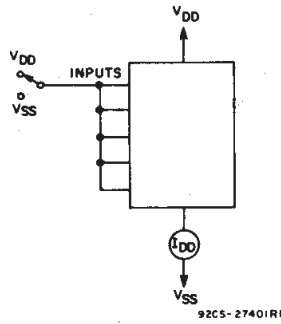


Fig. 11 - Quiescent device current test circuit.

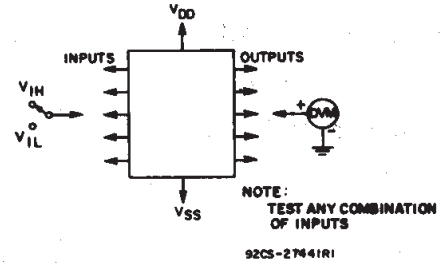


Fig. 12 - Noise immunity test circuit.

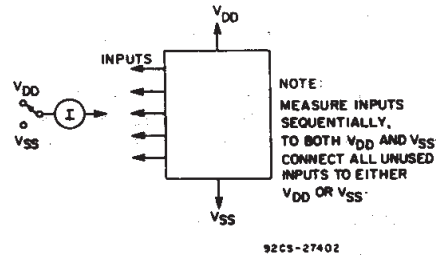
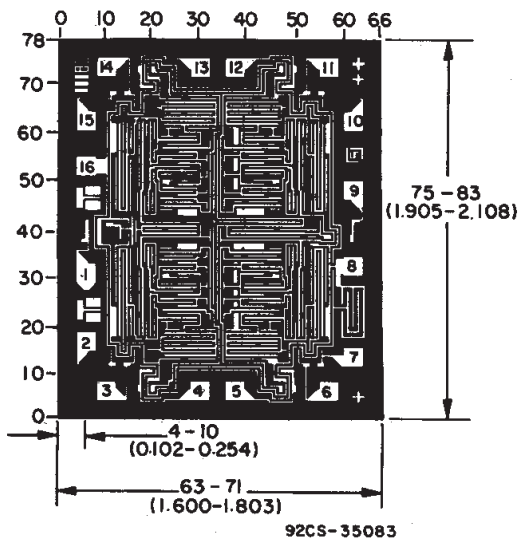


Fig. 13 - Input leakage current test circuit.



Dimensions and pad layout for CD40175BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD40175BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD40175BE
CD40175BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD40175BE
CD40175BEE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD40175BE
CD40175BF3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40175BF3A
CD40175BF3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40175BF3A
CD40175BM	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	CD40175BM
CD40175BM96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40175BM
CD40175BM96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40175BM
CD40175BMT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	CD40175BM
CD40175BNSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40175B
CD40175BNSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40175B
CD40175BPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0175B
CD40175BPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0175B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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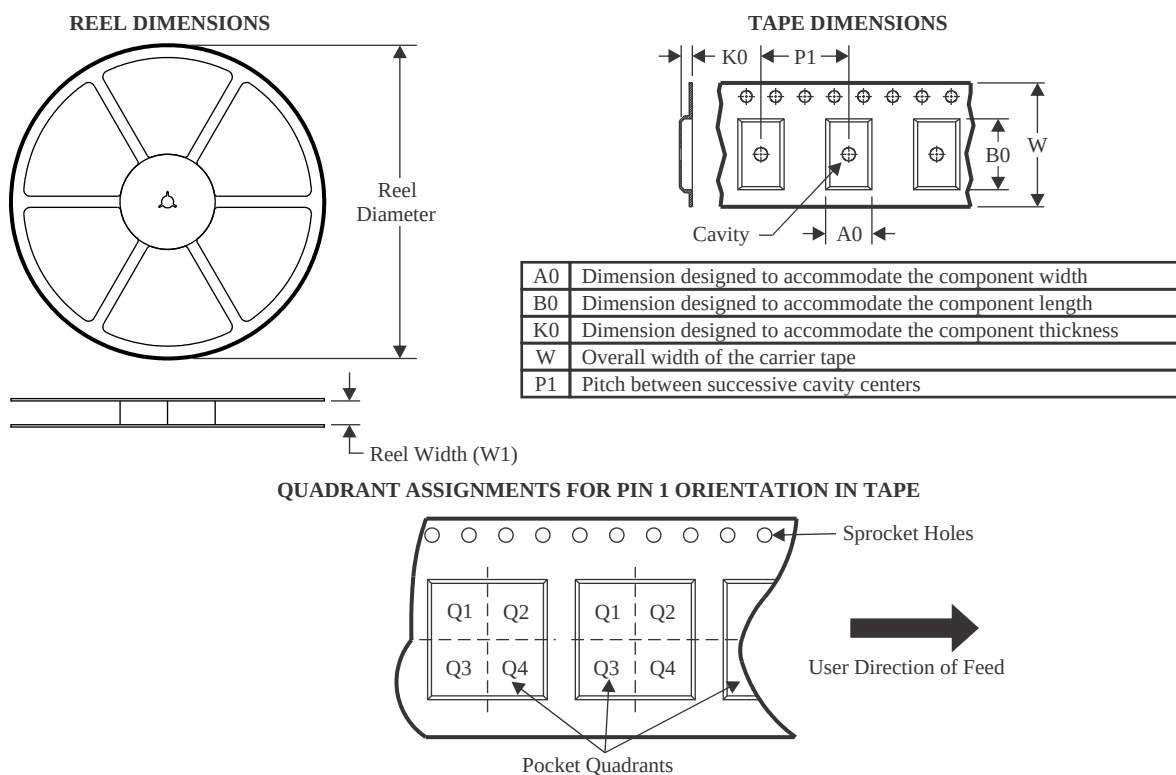
OTHER QUALIFIED VERSIONS OF CD40175B, CD40175B-MIL :

- Catalog : [CD40175B](#)
- Military : [CD40175B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

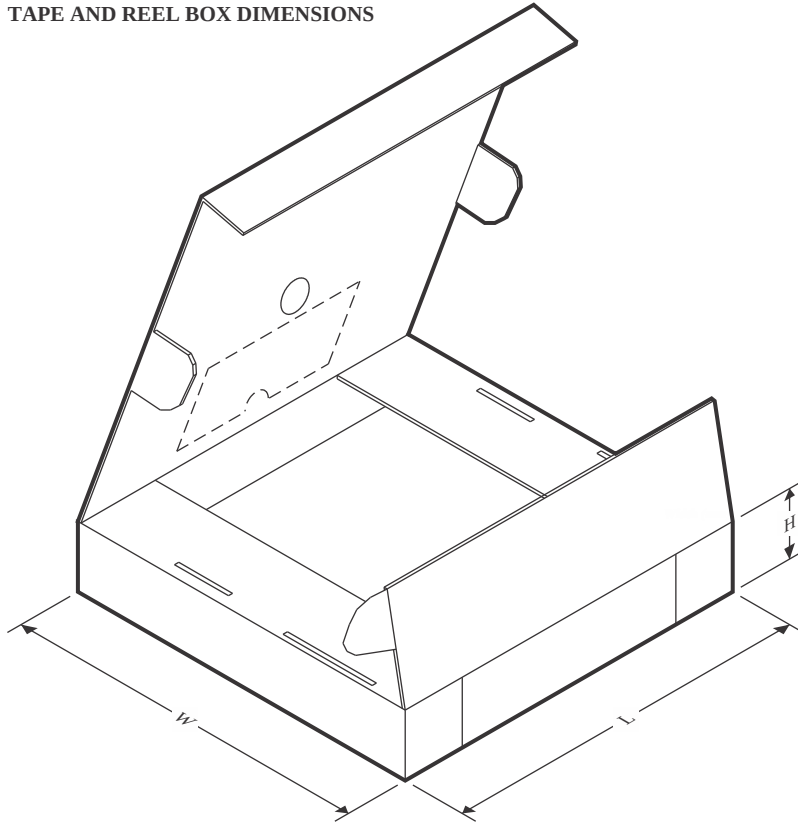
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40175BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD40175BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD40175BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

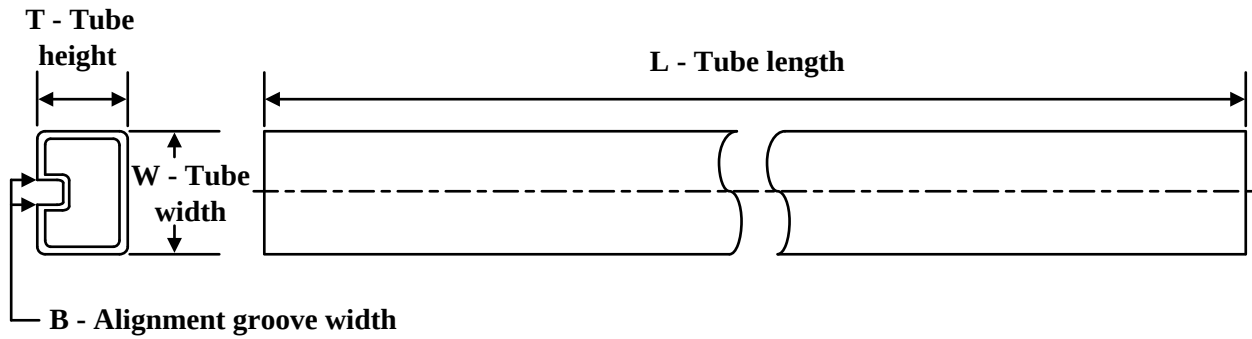
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40175BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD40175BNSR	SOP	NS	16	2000	356.0	356.0	35.0
CD40175BPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE

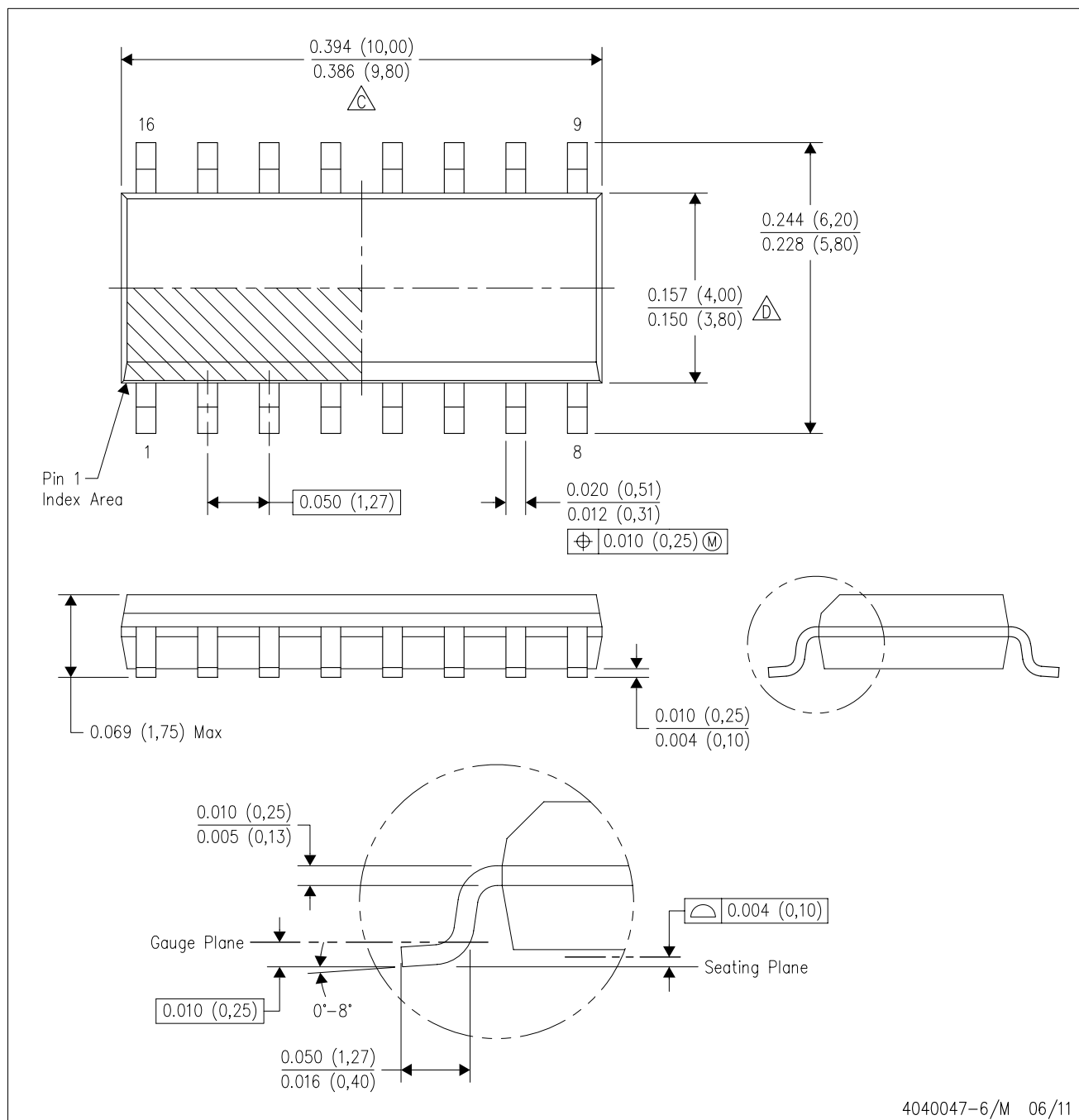


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD40175BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40175BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40175BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD40175BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD40175BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD40175BEE4	N	PDIP	16	25	506	13.97	11230	4.32

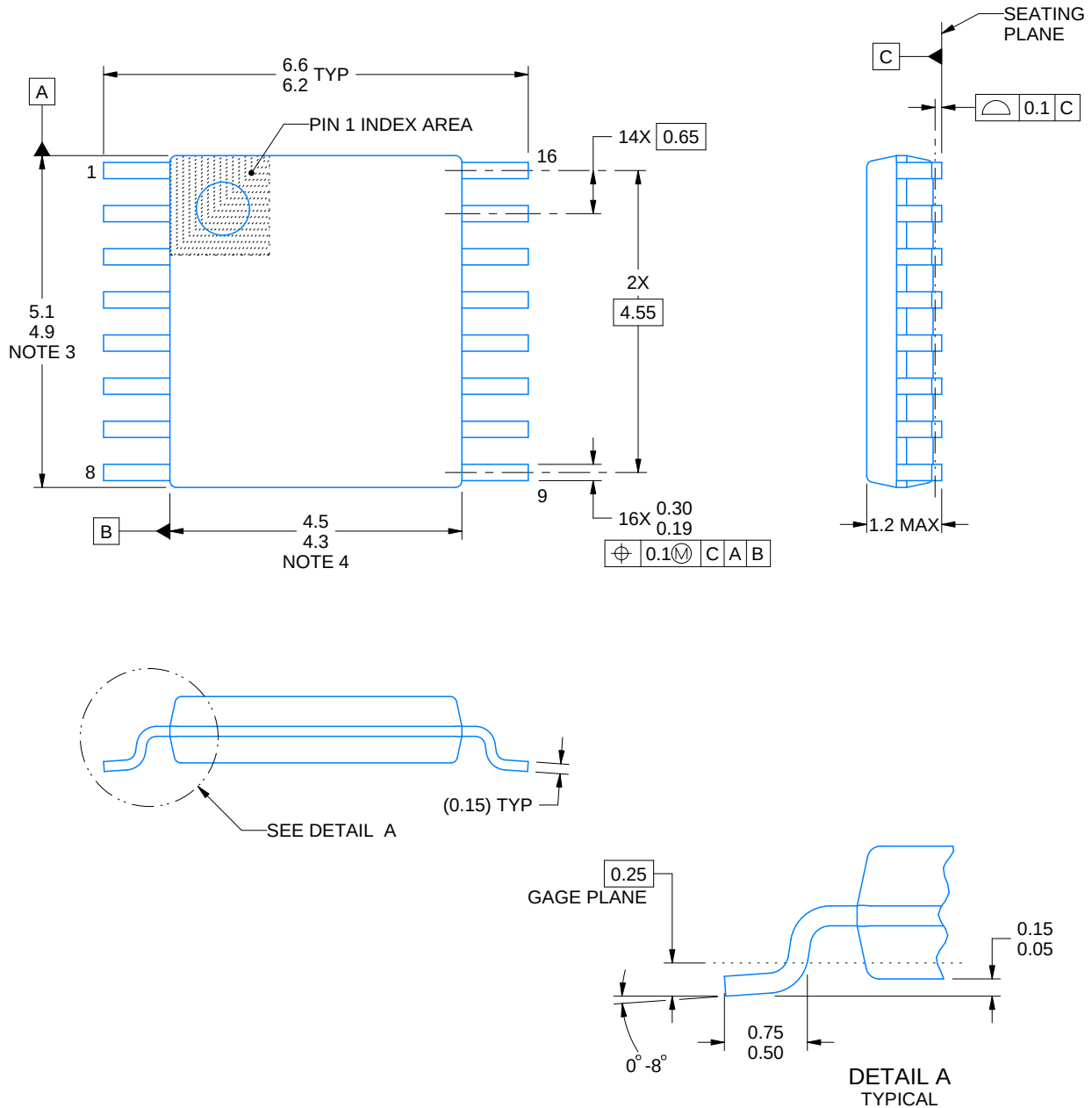
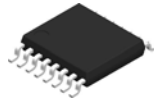
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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NOTES:

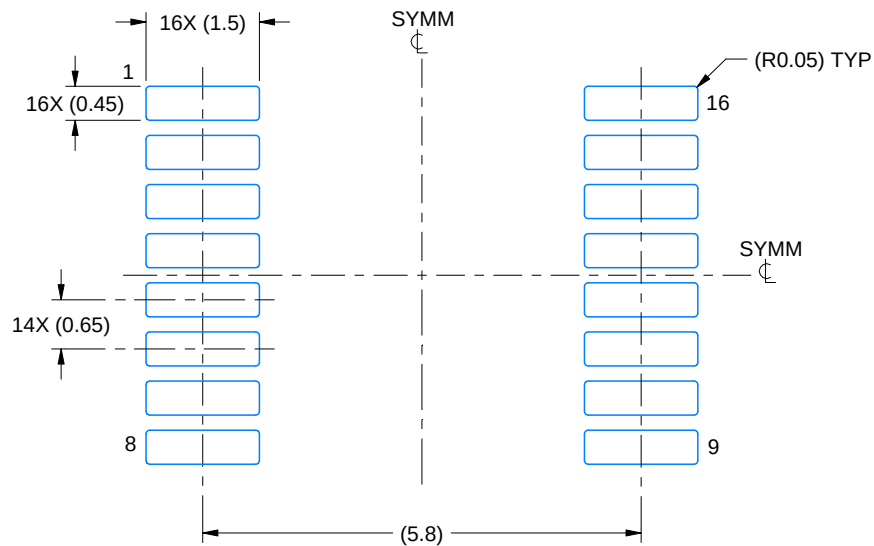
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

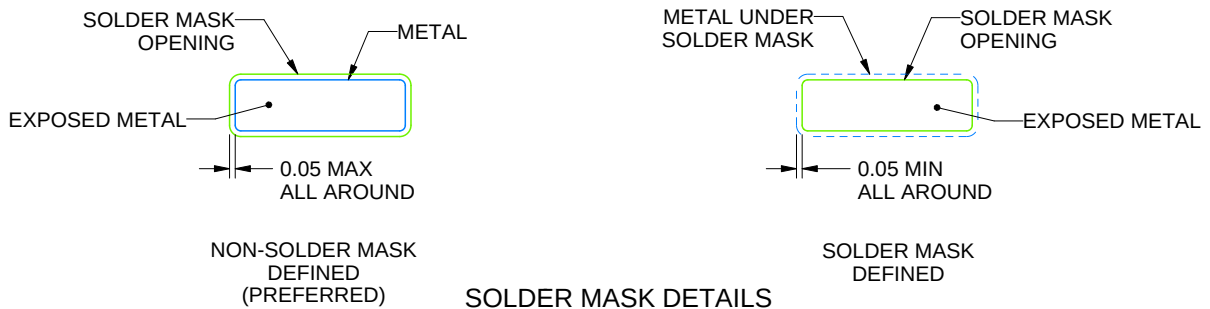
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

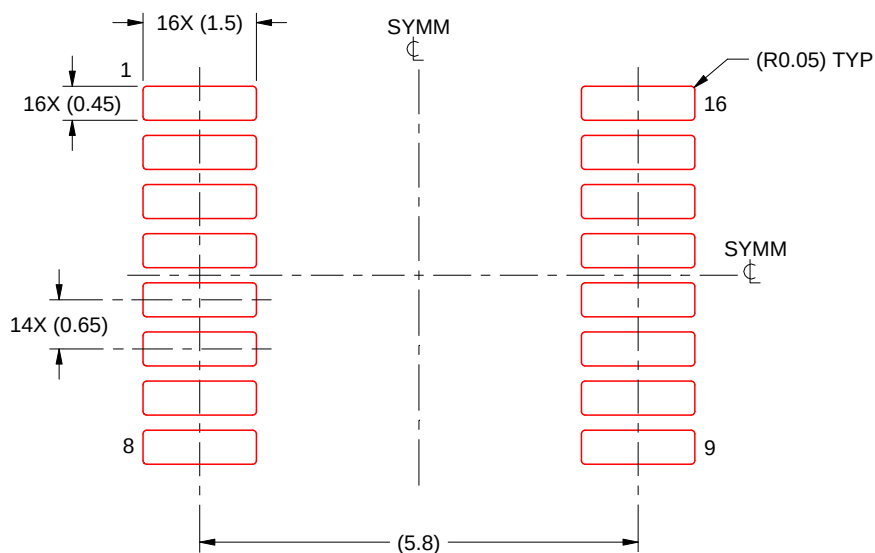
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

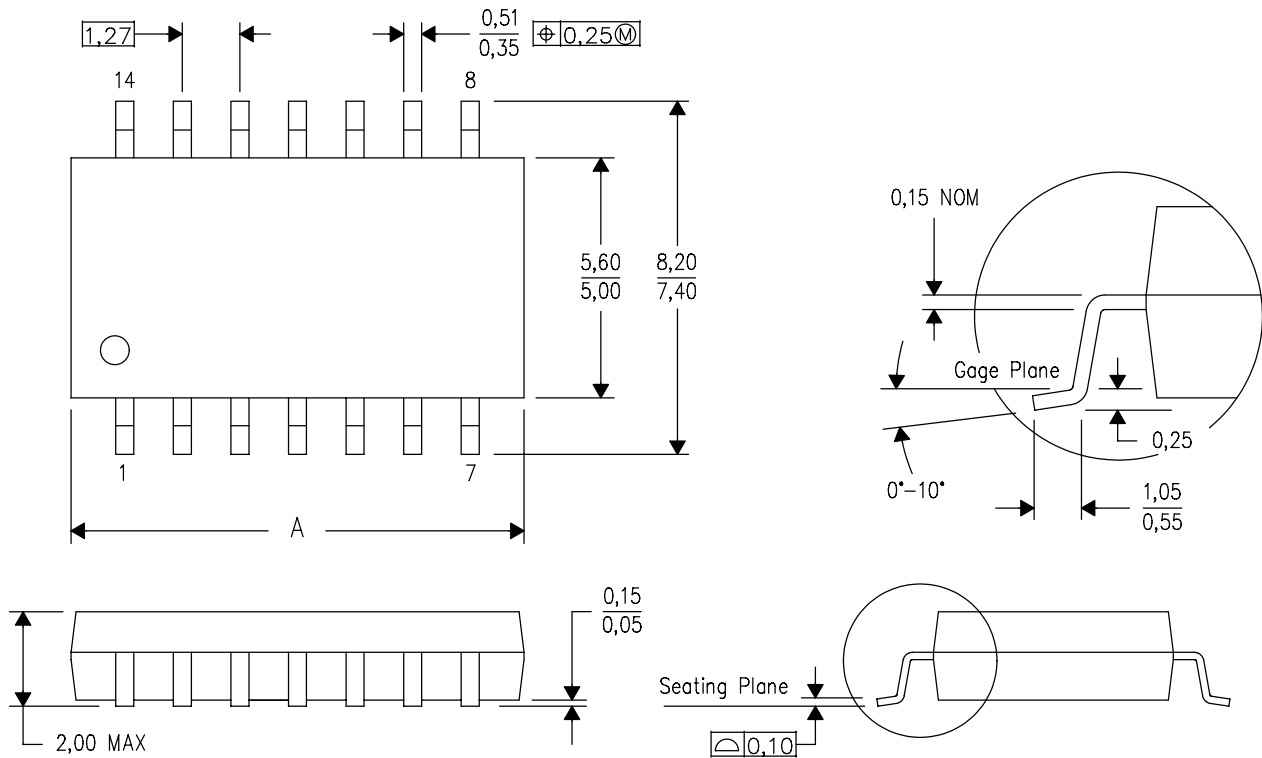
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

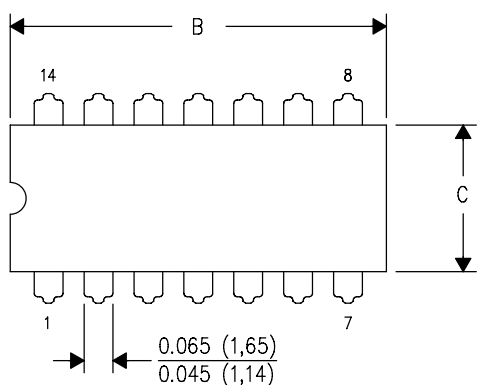
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

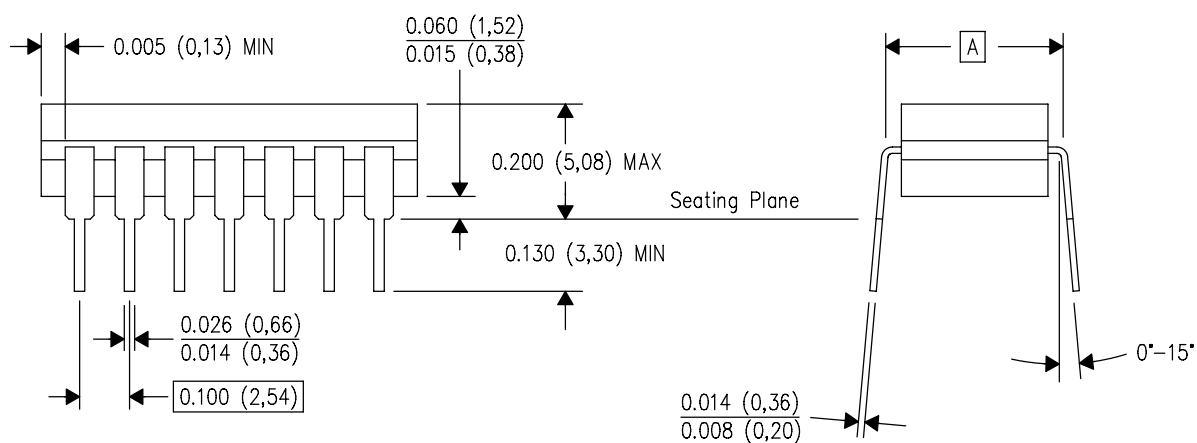
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



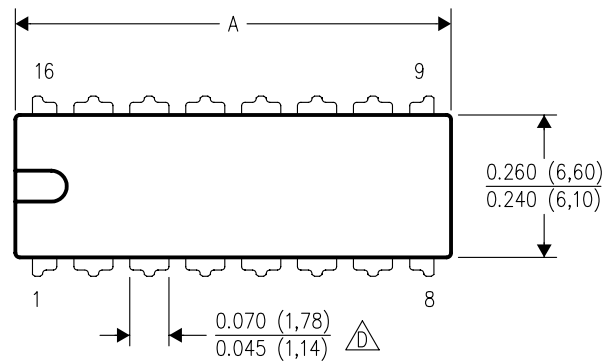
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

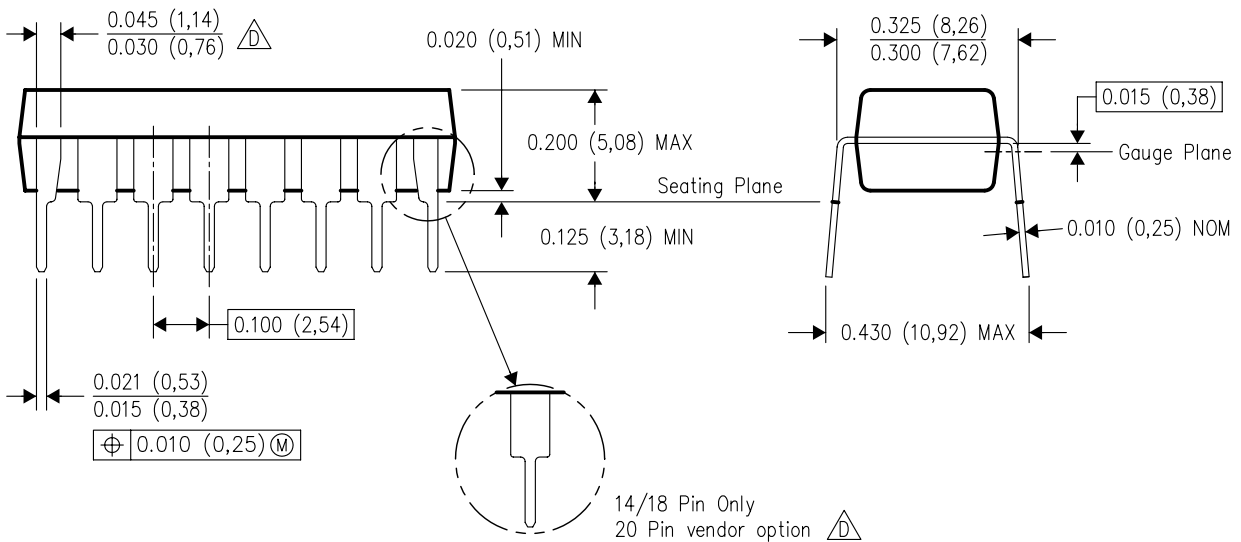
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



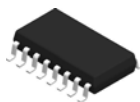
PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

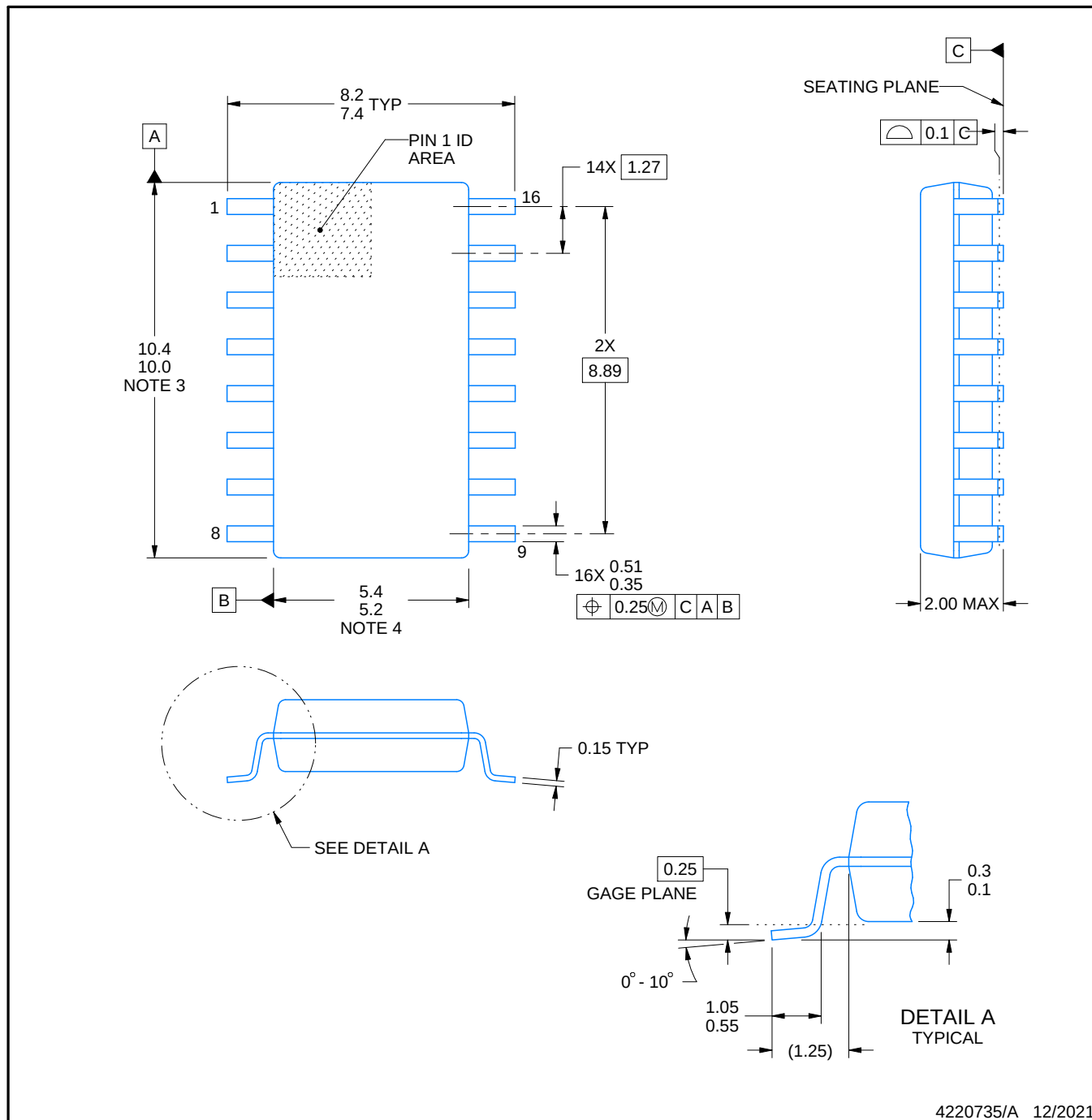


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

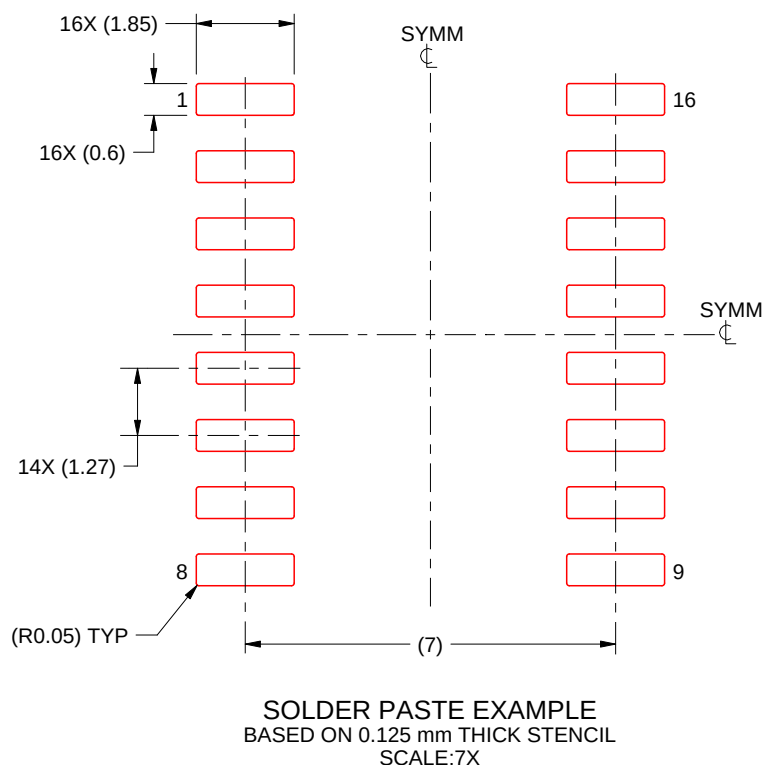
SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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