TLC5940 16-Channel LED Driver With DOT Correction and Grayscale PWM Control

1 Features

- 16 Channels
- 12 bit (4096 Steps) Grayscale PWM Control
- Dot Correction
  - 6 bit (64 Steps)
  - Storable in Integrated EEPROM
- Drive Capability (Constant-Current Sink)
  - 0 mA to 60 mA (V_{CC} < 3.6 V)
  - 0 mA to 120 mA (V_{CC} > 3.6 V)
- LED Power Supply Voltage up to 17 V
- V_{CC} = 3 V to 5.5 V
- Serial Data Interface
- Controlled In-Rush Current
- 30 MHz Data Transfer Rate
- CMOS Level I/O
- Error Information
  - LOD: LED Open Detection
  - TEF: Thermal Error Flag

2 Applications

- Monocolor, Multicolor, Full-Color LED Displays
- LED Signboards
- Display Backlighting
- General, High-Current LED Drive

3 Description

The TLC5940 is a 16-channel, constant-current sink LED driver. Each channel has an individually adjustable 4096-step grayscale PWM brightness control and a 64-step, constant-current sink (dot correction). The dot correction adjusts the brightness variations between LED channels and other LED drivers. The dot correction data is stored in an integrated EEPROM. Both grayscale control and dot correction are accessible through a serial interface. A single external resistor sets the maximum current value of all 16 channels.

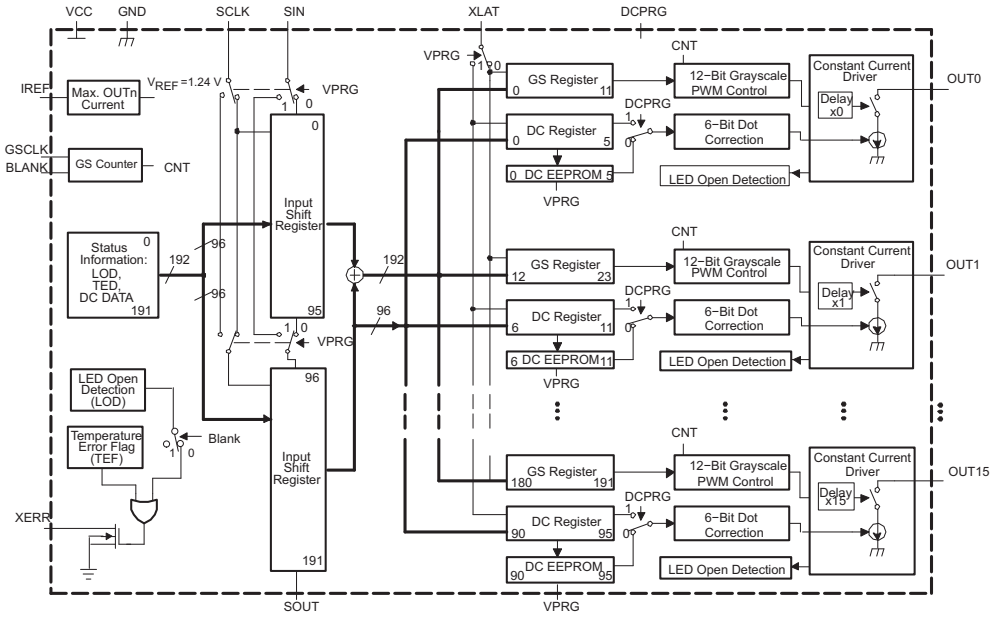
The TLC5940 features two error information circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an overtemperature condition.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC5940	PDIP (28)	35.69 mm × 6.73 mm
	HTSSOP (28)	9.70 mm × 4.40 mm
	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2007) to Revision D	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

Changes from Revision B (September 2007) to Revision C	Page
• Changed t_{su5} setup time from: 30 ms to: 30 ns	6

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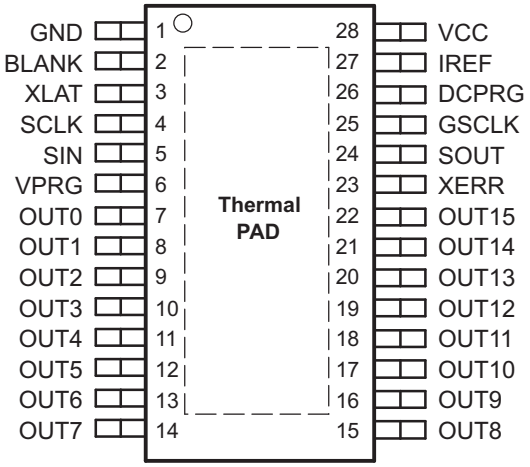
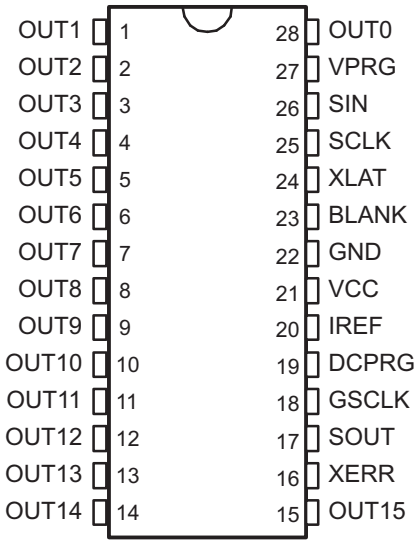
5 Pin Configuration and Functions

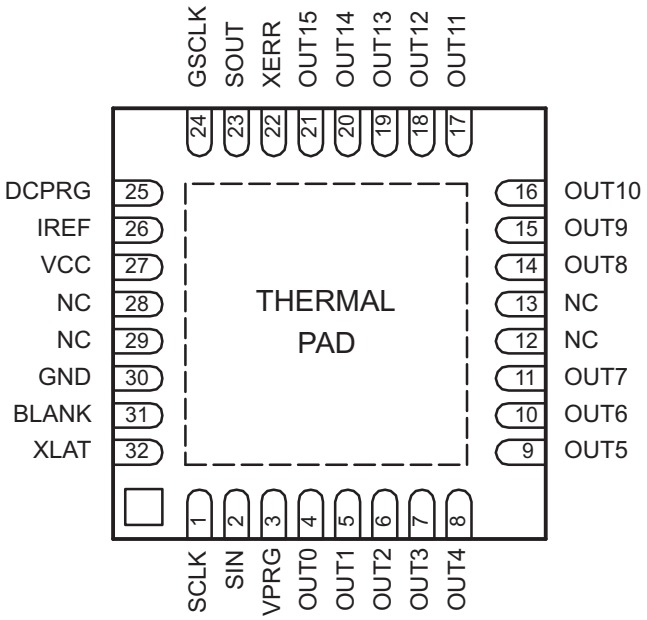
PWP Package
28-Pin HTSSOP
Top View



NT Package
28-Pin PDIP
Top View



RHB Package
32-Pin VQFN
Top View



NC – No internal connection

Pin Functions

PIN				TYPE	DESCRIPTION
NAME	DIP NO.	PWP NO.	RHB NO.		
BLANK	23	2	31	I	Blank all outputs. When BLANK = H, all OUTn outputs are forced OFF. GS counter is also reset. When BLANK = L, OUTn are controlled by grayscale PWM control.
DCPRG	19	26	25	I	Switch DC data input. When DCPRG = L, DC is connected to EEPROM. When DCPRG = H, DC is connected to the DC register. DCPRG also controls EEPROM writing, when VPRG = $V_{(PRG)}$. EEPROM data = 3 Fh (default)
GND	22	1	30	G	Ground
GSCLK	18	25	24	I	Reference clock for grayscale PWM control
IREF	20	27	26	I	Reference current terminal
NC	—	—	12	—	No connection
	—	—	13		
	—	—	28		
	—	—	29		
OUT0	28	7	4	O	Constant current output
OUT1	1	8	5	O	Constant current output
OUT2	2	9	6	O	Constant current output
OUT3	3	10	7	O	Constant current output
OUT4	4	11	8	O	Constant current output
OUT5	5	12	9	O	Constant current output
OUT6	6	13	10	O	Constant current output
OUT7	7	14	11	O	Constant current output
OUT8	8	15	14	O	Constant current output
OUT9	9	16	15	O	Constant current output
OUT10	10	17	16	O	Constant current output
OUT11	11	18	17	O	Constant current output
OUT12	12	19	18	O	Constant current output
OUT13	13	20	19	O	Constant current output
OUT14	14	21	20	O	Constant current output
OUT15	15	22	21	O	Constant current output
SCLK	25	4	1	I	Serial data shift clock
SIN	26	5	2	I	Serial data input
SOUT	17	24	23	O	Serial data output
VCC	21	28	27	I	Power supply voltage
VPRG	27	6	3	I	Multifunction input pin. When VPRG = GND, the device is in GS mode. When VPRG = V_{CC}, the device is in DC mode. When VPRG = $V_{(VPRG)}$, DC register data can programmed into DC EEPROM with DCPRG=HIGH. EEPROM data = 3 Fh (default)
XERR	16	23	22	O	Error output. XERR is an open-drain terminal. XERR goes L when LOD or TEF is detected.
XLAT	24	3	32	I	Level triggered latch signal. When XLAT = high, the TLC5940 writes data from the input shift register to either GS register (VPRG = low) or DC register (VPRG = high). When XLAT = low, the data in GS or DC register is held constant.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage[2]	VCC	–0.3	6	V
	$V_{(BLANK)}$, $V_{(DCPRG)}$, $V_{(SCLK)}$, $V_{(XLAT)}$, $V_{(SIN)}$, $V_{(GSCLK)}$, $V_{(IREF)}$	–0.3	V_{CC} +0.3	V
Output voltage	$V_{(SOUT)}$, $V_{(XERR)}$	–0.3	V_{CC} +0.3	V
	$V_{(OUT0)}$ to $V_{(OUT15)}$	–0.3	18	V
Output current (dc)			130	mA
EEPROM program range	$V_{(VPRG)}$	–0.3	24	V
EEPROM write cycles			50	—
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operting Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
DC CHARACTERISTICS						
V_{CC}	Supply Voltage		3		5.5	V
V_O	Voltage applied to output (OUT0–OUT15)				17	V
V_{IH}	High-level input voltage		0.8 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.2 V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 5 V at SOUT			–1	mA
I_{OL}	Low-level output current	V_{CC} = 5 V at SOUT, XERR			1	mA
I_{OLC}	Constant output current	OUT0 to OUT15, V_{CC} < 3.6 V			60	mA
		OUT0 to OUT15, V_{CC} > 3.6 V			120	mA
$V_{(VPRG)}$	EEPROM program voltage		20	22	23	V
T_A	Operating free-air temperature range		-40		85	°C
AC CHARACTERISTICS V_{CC} = 3 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)						
$f_{(SCLK)}$	Data shift clock frequency	SCLK			30	MHz
$f_{(GSCLK)}$	Grayscale clock frequency	GSCLK			30	MHz
t_{wh0}/t_{wl0}	SCLK pulse duration	SCLK = H/L (see Figure 11)	16			ns
t_{wh1}/t_{wl1}	GSCLK pulse duration	GSCLK = H/L (see Figure 11)	16			ns
t_{wh2}	XLAT pulse duration	XLAT = H (see Figure 11)	20			ns
t_{wh3}	BLANK pulse duration	BLANK = H (see Figure 11)	20			ns

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Recommended Operating Conditions (continued)

			MIN	NOM	MAX	UNIT
t_{su0}	Setup time	SIN to SCLK ↑[1] (see Figure 11)	5			ns
t_{su1}		SCLK ↓ to XLAT ↑ (see Figure 11)	10			ns
t_{su2}		VPRG ↑ ↓ to SCLK ↑ (see Figure 11)	10			ns
t_{su3}		VPRG ↑ ↓XLAT ↑ (see Figure 11)	10			ns
t_{su4}		BLANK ↓ to GSCLK ↑ (see Figure 11)	10			ns
t_{su5}		XLAT ↑ to GSCLK ↑ (see Figure 11)	30			ns
t_{su6}		VPRG ↑ to DCPRG ↑ (see Figure 16)	1			ms
t_{h0}	Hold Time	SCLK ↑ to SIN (see Figure 11)	3			ns
t_{h1}		XLAT ↓ to SCLK ↑ (see Figure 11)	10			ns
t_{h2}		SCLK ↑ to VPRG ↑ ↓ (see Figure 11)	10			ns
t_{h3}		XLAT ↓ to VPRG ↑ ↓ (see Figure 11)	10			ns
t_{h4}		GSCLK ↑ to BLANK ↑ (see Figure 11)	10			ns
t_{h5}		DCPRG ↓ to VPRG ↓ (see Figure 11)	1			ms
t_{prog}		Programming time for EEPROM (see Figure 16)	20			ms

(1) ↑ and ↓ indicates a rising edge, and a falling edge respectively.

6.4 Thermal Information

THERMAL METRIC[1]		TLC5940		UNIT
		PWP (HTSSOP)	RHB (VQFN)	
		28 PINS	32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.7	34.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.9	36.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	8.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.8	8.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

V_{CC} = 3 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1 mA, SOUT	V_{CC} –0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, SOUT			0.5	V
I_I	Input current	V_I = V_{CC} or GND; BLANK, DCPRG, GSCLK, SCLK, SIN, XLAT	–1		1	µA
		V_I = GND; VPRG	–1		1	
		V_I = V_{CC}; VPRG			50	
		V_I = 22 V; VPRG; DCPRG = V_{CC}		4	10	mA
I_{CC}	Supply current	No data transfer, all output OFF, V_O = 1 V, $R_{(IREF)}$ = 10 kΩ		0.9	6	mA
		No data transfer, all output OFF, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ		5.2	12	
		Data transfer 30MHz, all output ON, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ		16	25	
		Data transfer 30MHz, all output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω		30	60	
$I_{O(LC)}$	Constant sink current (see Figure 10)	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω	54	61	69	mA
I_{lkg}	Leakage output current	All output OFF, V_O = 15 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15			0.1	µA
$\Delta I_{O(LC0)}$	Constant sink current error (see Figure 10)	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15, –20°C to 85°C		±1%	±4%	
		All output ON, V_O = 1V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15(1)		±1%	±8%	
		All output ON, V_O = 1V, $R_{(IREF)}$ = 320 Ω, OUT0 to OUT15, –20°C to 85°C		±1%	±6%	
		All output ON, V_O = 1V, $R_{(IREF)}$ = 320 Ω, V_{CC} = 4.5 V to 5.5 V, OUT0 to OUT15(1)		±1%	±8%	
$\Delta I_{O(LC1)}$	Constant sink current error (see Figure 10)	Device to device, Averaged current from OUT0 to OUT15, $R_{(IREF)}$ = 1920 Ω (20 mA)(2)		–2% +0.4%	±4%	
$\Delta I_{O(LC2)}$	Constant sink current error (see Figure 10)	Device to device, Averaged current from OUT0 to OUT15, $R_{(IREF)}$ = 480 Ω (80 mA)(2)		–2.7% +2%	±4%	
$\Delta I_{O(LC3)}$	Line regulation (see Figure 10)	All output ON, V_O = 1V, $R_{(IREF)}$ = 640 Ω OUT0 to OUT15, V_{CC} = 3 V to 5.5 V(3)		±1	±4	%/V
		All output ON, V_O = 1V, $R_{(IREF)}$ = 320 Ω , OUT0 to OUT15, V_{CC} = 3 V to 5.5 V(3)		±1	±6	%/V
$\Delta I_{O(LC4)}$	Load regulation (see Figure 10)	All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15(4)		±2	±6	%/V
		All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 320 Ω, OUT0 to OUT15(4)		±2	±8	%/V
$T_{(TEF)}$	Thermal error flag threshold	Junction temperature(5)	150		170	°C
$V_{(LED)}$	LED open detection threshold			0.3	0.4	V
$V_{(IREF)}$	Reference voltage output	$R_{(IREF)}$ = 640 Ω	1.20	1.24	1.28	V

(1) The deviation of each output from the average of OUT0-15 constant current. It is calculated by Equation 1 in *Test Parameter Equations*.
(2) The deviation of average of OUT1-15 constant current from the ideal constant-current value. It is calculated by Equation 2 in *Test Parameter Equations*. The ideal current is calculated by Equation 3 in *Test Parameter Equations*.
(3) The line regulation is calculated by Equation 4 in *Test Parameter Equations*.
(4) The load regulation is calculated by Equation 5 in *Test Parameter Equations*.
(5) Not tested. Specified by design

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6.6 Switching Characteristics

V_{CC} = 3V to 5.5V, T_A = -40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{r0}	Rise time	SOUT			16	ns
t_{r1}		OUTn, V_{CC} = 5 V, T_A = 60°C, DCn = 3 Fh		10	30	
t_{f0}	Fall time	SOUT			16	ns
t_{f1}		OUTn, V_{CC} = 5 V, T_A = 60°C, DCn = 3 Fh		10	30	
t_{pd0}	Propagation delay time	SCLK to SOUT (see Figure 11)			30	ns
t_{pd1}		BLANK to OUT0			60	ns
t_{pd2}		OUTn to XERR (see Figure 11)			1000	ns
t_{pd3}		GSCLK to OUT0 (see Figure 11)			60	ns
t_{pd4}		XLAT to I_{OUT} (dot correction) (see Figure 11)			60	ns
t_{pd5}		DCPRG to OUT0 (see Figure 11)			30	ns
t_d	Output delay time	OUTn to OUT(n+1) (see Figure 11)		20	30	ns
$t_{on\text{-}err}$	Output on-time error	t_{outon}– T_{gsclk} (see Figure 11), GSn = 01h, GSCLK = 11 MHz	10	–50	–90	ns

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6.7 Typical Characteristics

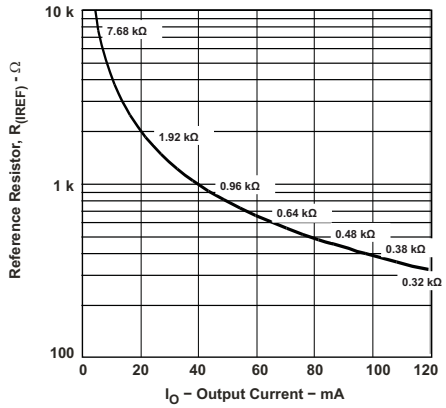

Figure 1. Reference Resistor vs Output Current

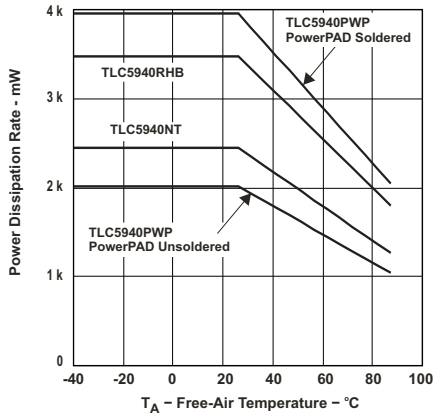

Figure 2. Power Dissipation Rate vs Free-Air Temperature

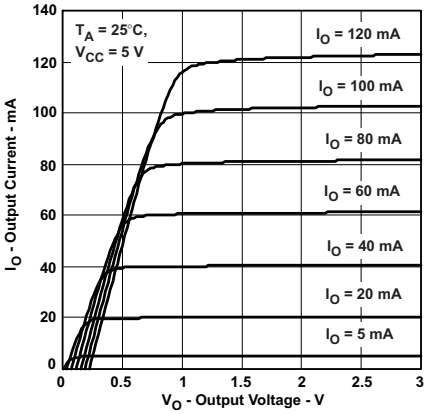

Figure 3. Output Current vs Output Voltage

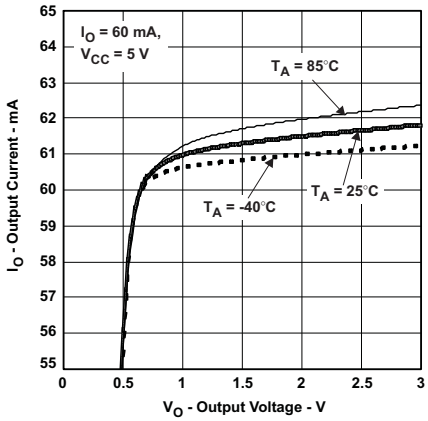

Figure 4. Output Current vs Output Voltage

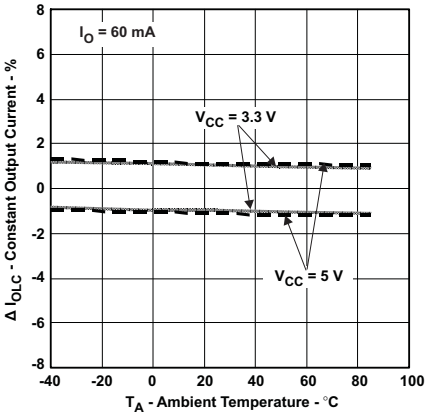

Figure 5. Constant Output Current, ΔI_{OLC} vs Ambient Temperature

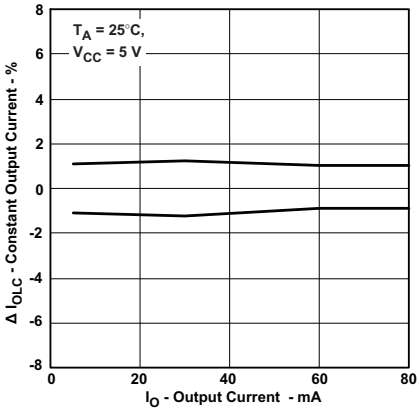

Figure 6. Constant Output Current, ΔI_{OLC} vs Output Current

Typical Characteristics (continued)

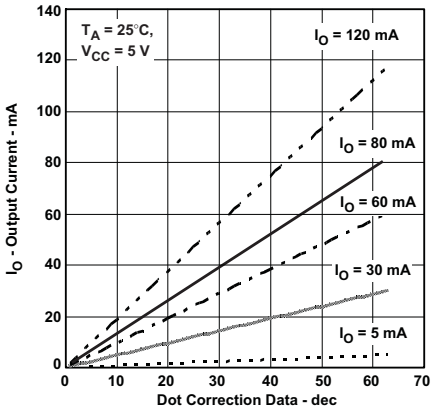

Figure 7. Output Current vs DOT Correction Linearity (ABS Value)

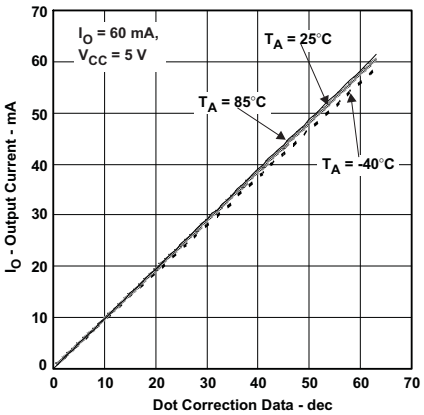

Figure 8. Output Current vs DOT Correction Linearity (ABS Value)

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7 Parameter Measurement Information

Resistor values are equivalent resistances, and they are not tested.

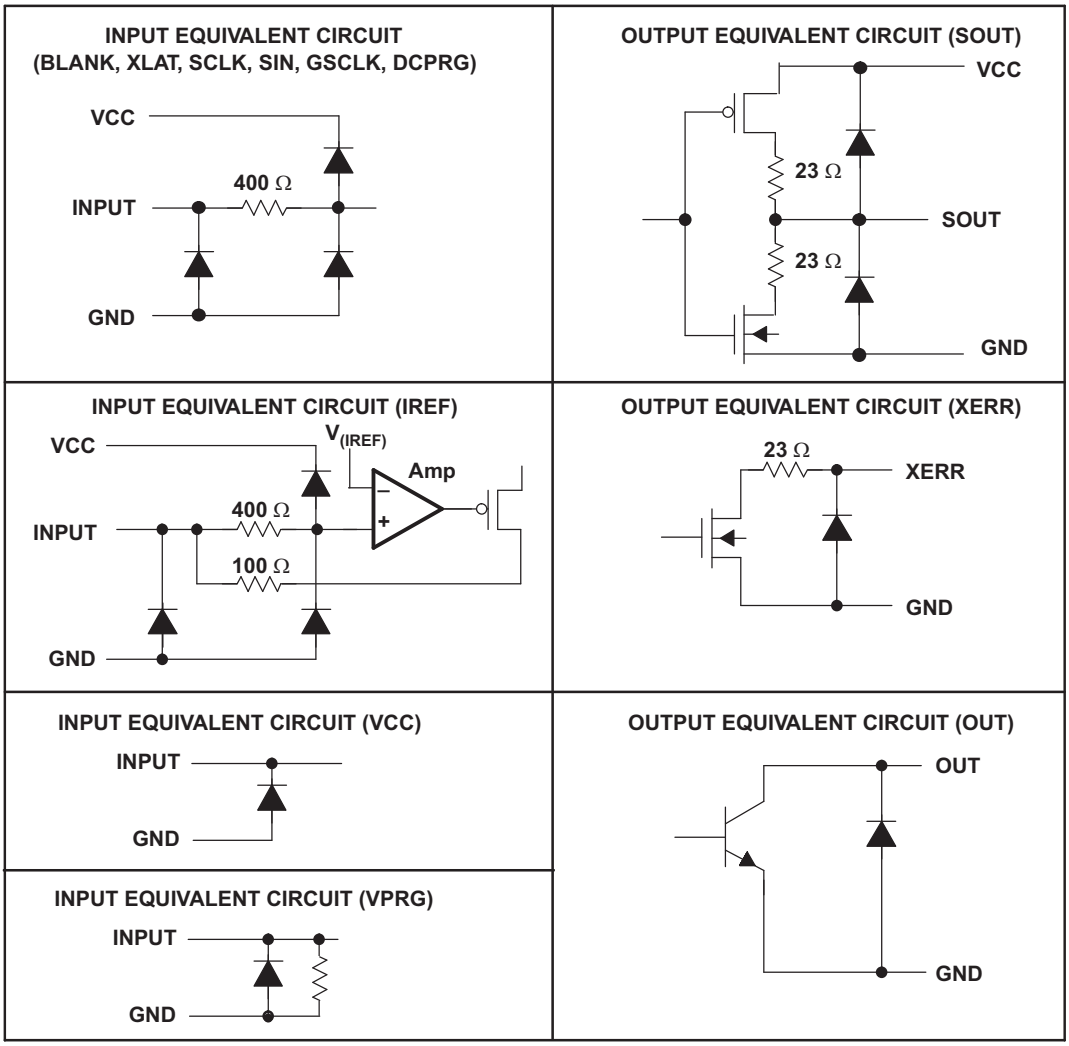

Figure 9. Input and Output Equivalent Circuits

Parameter Measurement Information (continued)

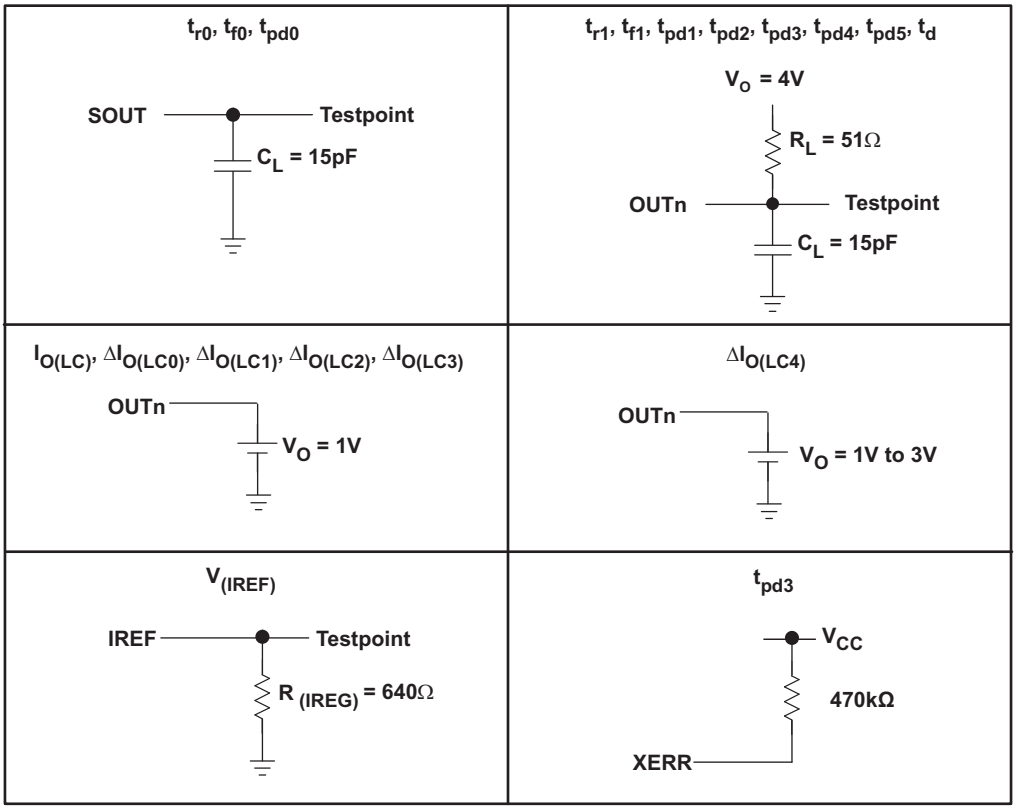

Figure 10. Parameter Measurement Circuits

7.1 Test Parameter Equations

$$\Delta(\%) = \frac{I_{OUTn} - I_{OUTavg_0-15}}{I_{OUTavg_0-15}} \times 100 \tag{1}$$

$$\Delta(\%) = \frac{I_{OUTavg} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}} \times 100 \tag{2}$$

$$I_{OUT(IDEAL)} = 31.5 \times \left(\frac{1.24V}{R_{IREF}}\right) \tag{3}$$

$$\Delta(\%/V) = \frac{(I_{OUTn} \text{ at } V_{CC} = 5.5V) - (I_{OUTn} \text{ at } V_{CC} = 3.0V)}{(I_{OUTn} \text{ at } V_{CC} = 3.0V)} \times \frac{100}{2.5} \tag{4}$$

$$\Delta(\%/V) = \frac{(I_{OUTn} \text{ at } V_{OUTn} = 3.0V) - (I_{OUTn} \text{ at } V_{OUTn} = 1.0V)}{(I_{OUTn} \text{ at } V_{OUTn} = 1.0V)} \times \frac{100}{2.0} \tag{5}$$

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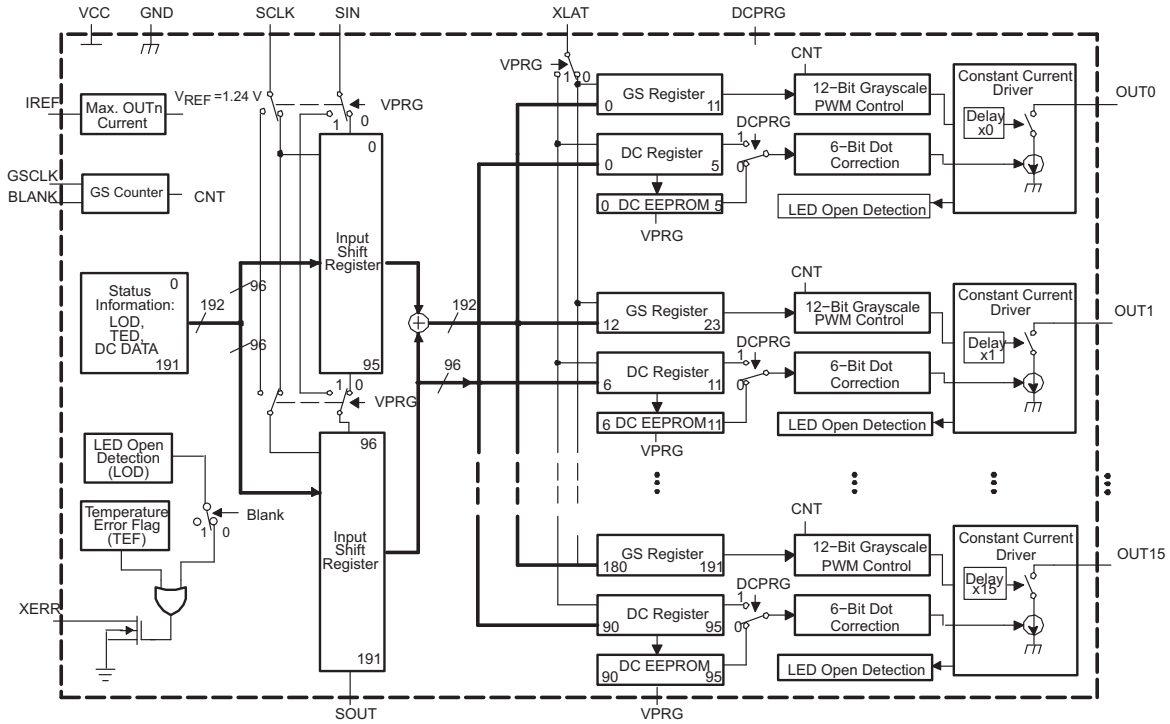
8 Detailed Description

8.1 Overview

The TLC5940 is a 16-channel constant current sink driver. Each channel has an individually-adjustable, 4096-step, pulse width modulation (PWM), grayscale (GS) brightness control, and a 64-step dot correction brightness control. GS data and DC data are input via a serial interface port. The dot correction data is stored in an integrated EEPROM. The TLC5940 has a 120-mA current capability. The maximum current value of all channels is determined by an external resistor. The TLC5940 has a LED open detection (LOD) function that indicates a broken or disconnected LED at an output terminal and a thermal error flag (TEF) indicates an overtemperature condition.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Serial Interface

The TLC5940 has a flexible serial interface, which can be connected to microcontrollers or digital signal processors in various ways. Only 3 pins are needed to input data into the device. The rising edge of SCLK signal shifts the data from the SIN pin to the internal register. After all data is clocked in, a high-level pulse of XLAT signal latches the serial data to the internal registers. The internal registers are level-triggered latches of XLAT signal. All data are clocked in with the MSB first. The length of serial data is 96 bit or 192 bit, depending on the programming mode. Grayscale data and dot correction data can be entered during a grayscale cycle. Although new grayscale data can be clocked in during a grayscale cycle, the XLAT signal should only latch the grayscale data at the end of the grayscale cycle. Latching in new grayscale data immediately overwrites the existing grayscale data. Figure 11 shows the timing chart. More than two TLC5940s can be connected in series by connecting an SOUT pin from one device to the SIN pin of the next device. An example of cascading two TLC5940s is shown in Figure 12 and the timing chart is shown in Figure 13. The SOUT pin can also be connected to the controller to receive status information from TLC5940 as shown in Figure 22.

Feature Description (continued)

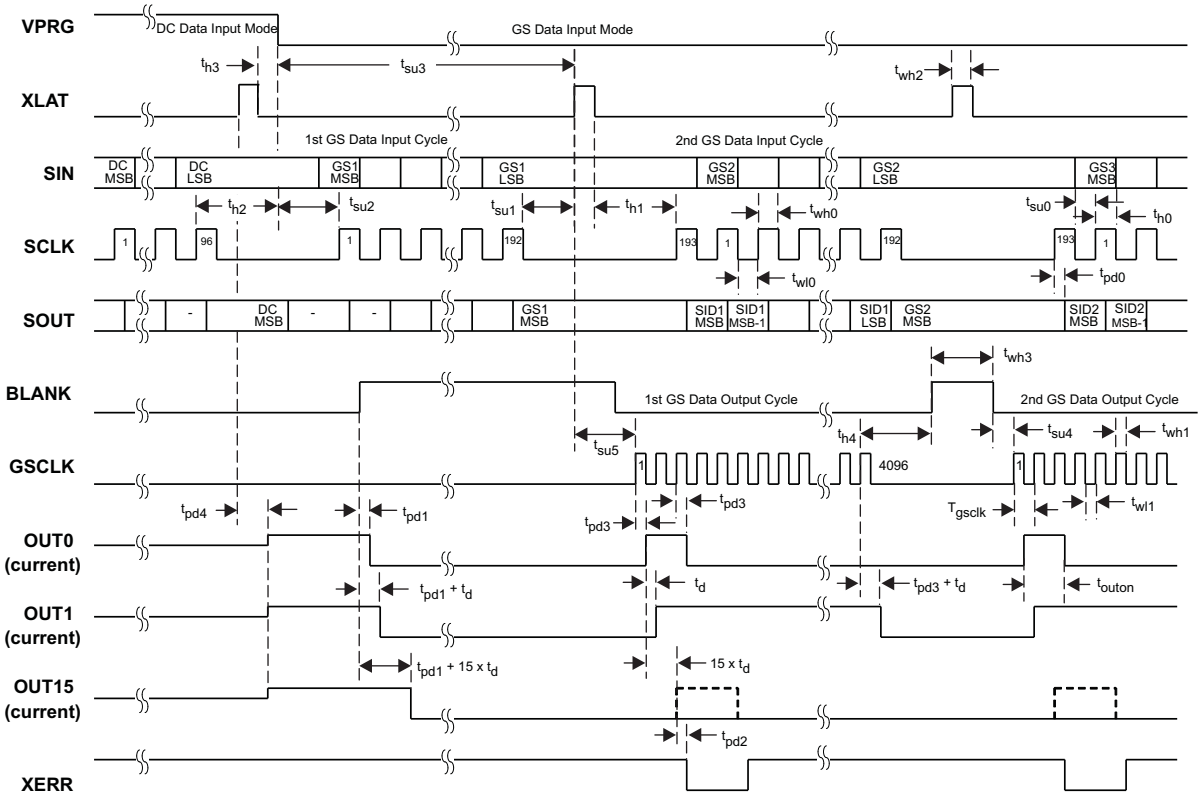


Figure 11. Serial Data Input Timing Chart

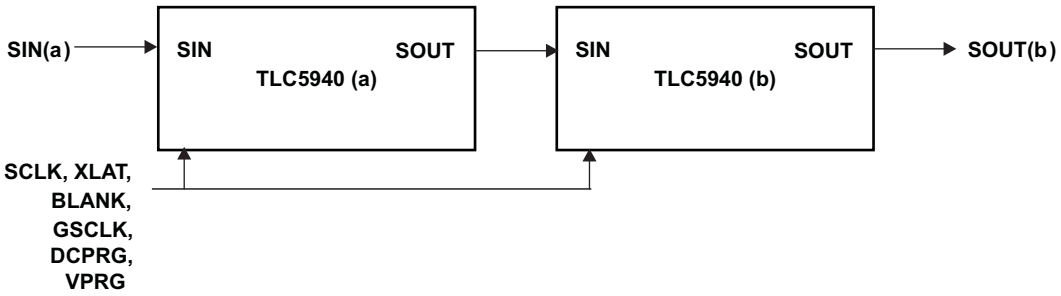


Figure 12. Cascading Two TLC5940 Devices

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Feature Description (continued)

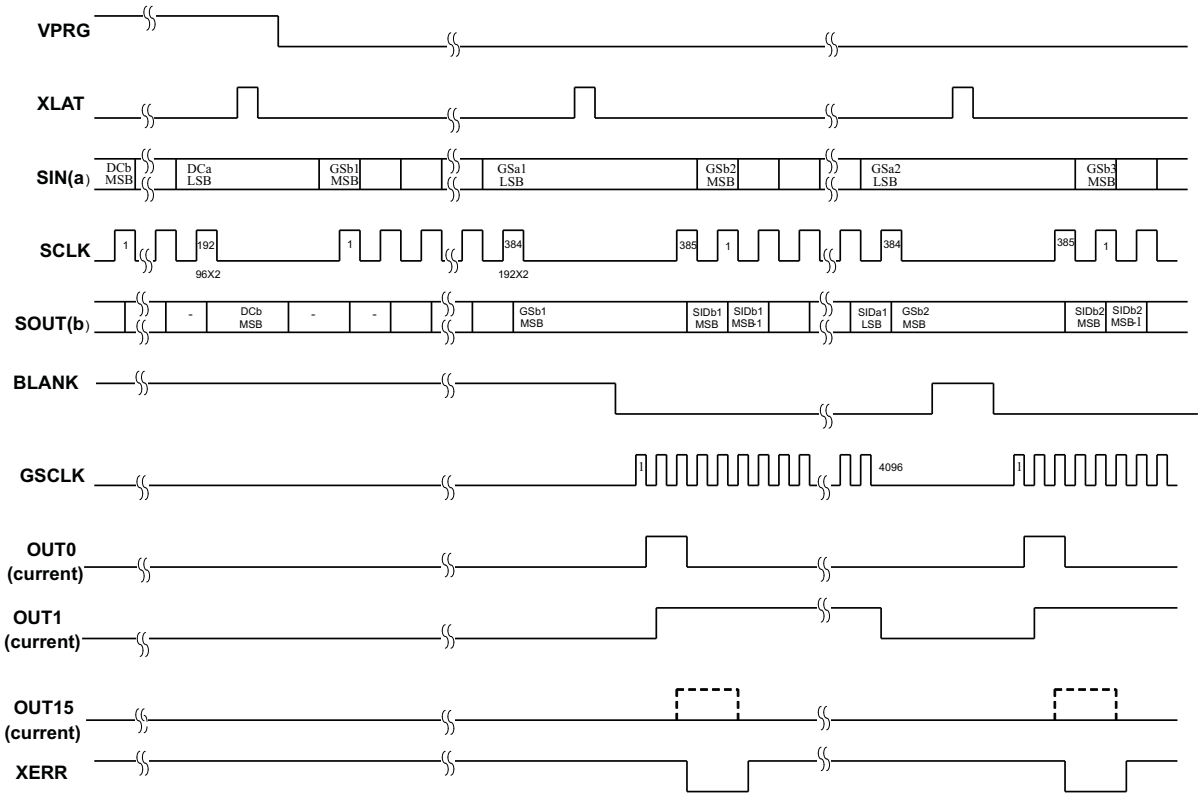

Figure 13. Timing Chart for Two Cascaded TLC5940 Devices

8.3.2 Error Information Output

The open-drain output XERR is used to report both of the TLC5940 error flags, TEF and LOD. During normal operating conditions, the internal transistor connected to the XERR pin is turned off. The voltage on XERR is pulled up to V_{CC} through an external pullup resistor. If TEF or LOD is detected, the internal transistor is turned on, and XERR is pulled to GND. Since XERR is an open-drain output, multiple ICs can be OR'ed together and pulled up to V_{CC} with a single pullup resistor. This reduces the number of signals needed to report a system error (see Figure 22).

To differentiate LOD and TEF signal from XERR pin, LOD can be masked out with BLANK = HIGH.

Table 1. XERR Truth Table

ERROR CONDITION		ERROR INFORMATION		SIGNALS	
TEMPERATURE	OUTn VOLTAGE	TEF	LOD	BLANK	XERR
$T_J < T_{(TEF)}$	Don't Care	L	X	H	H
$T_J > T_{(TEF)}$	Don't Care	H	X		L
$T_J < T_{(TEF)}$	OUTn > $V_{(LED)}$	L	L	L	H
	OUTn < $V_{(LED)}$	L	H		L
$T_J > T_{(TEF)}$	OUTn > $V_{(LED)}$	H	L		L
	OUTn < $V_{(LED)}$	H	H		L

8.3.3 TEF: Thermal Error Flag

The TLC5940 provides a temperature error flag (TEF) circuit to indicate an overtemperature condition of the IC. If the junction temperature exceeds the threshold temperature (160°C typical), TEF becomes H and XERR pin goes to low level. When the junction temperature becomes lower than the threshold temperature, TEF becomes L and XERR pin becomes high impedance. TEF status can also be read out from the TLC5940 status register.

8.3.4 LOD: LED Open Detection

The TLC5940 has an LED-open detector that detects broken or disconnected LEDs. The LED open detector pulls the XERR pin to GND when an open LED is detected. XERR and the corresponding error bit in the Status Information Data is only active under the following open-LED conditions.

1. OUTn is on and the time tpd2 (1 μs typical) has passed.
2. The voltage of OUTn is < 0.3 V (typical)

The LOD status of each output can be also read out from the SOUT pin. See STATUS INFORMATION OUTPUT section for details. The LOD error bits are latched into the Status Information Data when XLAT returns to a low after a high. Therefore, the XLAT pin must be pulsed high then low while XERR is active in order to latch the LOD error into the Status Information Data for subsequent reading via the serial shift register.

8.3.5 Delay Between Outputs

The TLC5940 has graduated delay circuits between outputs. These circuits can be found in the constant current driver block of the device (see the functional block diagram). The fixed-delay time is 20 ns (typical), OUT0 has no delay, OUT1 has a 20-ns delay, and OUT2 has a 40-ns delay, etc. The maximum delay is 300 ns from OUT0 to OUT15. The delay works during switch on and switch off of each output channel. These delays prevent large inrush currents which reduces the bypass capacitors when the outputs turn on.

8.3.6 Output Enable

All OUTn channels of the TLC5940 can be switched off with one signal. When BLANK is set high, all OUTn channels are disabled, regardless of logic operations of the device. The grayscale counter is also reset. When BLANK is set low, all OUTn channels work under normal conditions. If BLANK goes low and then back high again in less than 300 ns, all outputs programmed to turn on still turn on for either the programmed number of grayscale clocks, or the length of time that the BLANK signal was low, which ever is lower. For example, if all outputs are programmed to turn on for 1 ms, but the BLANK signal is only low for 200 ns, all outputs still turn on for 200 ns, even though some outputs are turning on after the BLANK signal has already gone high.

Table 2. BLANK Signal Truth Table

BLANK	OUT0 - OUT15
LOW	Normal condition
HIGH	Disabled

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8.3.7 Setting Maximum Channel Current

The maximum output current per channel is programmed by a single resistor, $R_{(IREF)}$, which is placed between IREF pin and GND pin. The voltage on IREF is set by an internal band gap $V_{(IREF)}$ with a typical value of 1.24 V. The maximum channel current is equivalent to the current flowing through $R_{(IREF)}$ multiplied by a factor of 31.5. The maximum output current per channel can be calculated by Equation 6.

$$I_{max} = \frac{V_{(IREF)}}{R_{(IREF)}} \times 31.5$$

where

- $V_{(IREF)}$ = 1.24 V
- $R_{(IREF)}$ = User-selected external resistor. (6)

I_{max} must be set between 5 mA and 120 mA. The output current may be unstable if I_{max} is set lower than 5 mA. Output currents lower than 5 mA can be achieved by setting Imax to 5 mA or higher and then using dot correction.

Figure 1 shows the maximum output current I_O versus $R_{(IREF)}$. $R_{(IREF)}$ is the value of the resistor between IREF terminal to GND, and I_O is the constant output current of OUT0 to OUT15. A variable power supply may be connected to the IREF pin through a resistor to change the maximum output current per channel. The maximum output current per channel is 31.5 times the current flowing out of the IREF pin.

8.4 Device Functional Modes

8.4.1 Operating Modes

The TLC5940 has operating modes depending on the signals DCPRG and VPRG. Table 3 shows the available operating modes. The TPS5940 GS operating mode (see Figure 11) and shift register values are not defined after power up. One solution to solve this is to set dot correction data after TLS5940 power-up and switch back to GS PWM mode. The other solution is to overflow the input shift register with 193 bits of dummy data and latch it while TLS540 is in GS PWM mode. The values in the input shift register, DC register and GS register are unknown just after power on. The DC and GS register values should be properly stored through the serial interface before starting the operation.

Table 3. TLC5940 Operating Modes Truth Table

SIGNAL		INPUT SHIFT REGISTER	MODE	DC VALUE
DCPRG	VPRG			
L	GND	192 bit	Grayscale PWM Mode	EEPROM
H				DC Register
L	V_{CC}	96 bit	Dot Correction Data Input Mode	EEPROM
H				DC Register
L	$V_{(VPRG)}$	X	EEPROM Programming Mode	EEPROM
H				Write dc register value to EEPROM. (Default data: 3Fh)

8.4.2 Setting DOT Correction

The TLC5940 has the capability to fine adjust the output current of each channel OUT0 to OUT15 independently. This is also called dot correction. This feature is used to adjust the brightness deviations of LEDs connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0% to 100% of the maximum output current I_{max}. Dot correction for all channels must be entered at the same time. Equation 7 determines the output current for each output n.

$$I_{OUTn} = I_{max} \times \frac{DCn}{63}$$

where

- I_{max} = the maximum programmable output current for each output.
- DCn = the programmed dot correction value for output n (DCn = 0 to 63).
- n = 0 to 15 (7)

Figure 14 shows the dot correction data packet format which consists of 6 bits x 16 channel, total 96 bits. The format is Big-Endian format. This means that the MSB is transmitted first, followed by the MSB-1, etc. The DC 15.5 in Figure 14 stands for the 5th most significant bit for output 15.

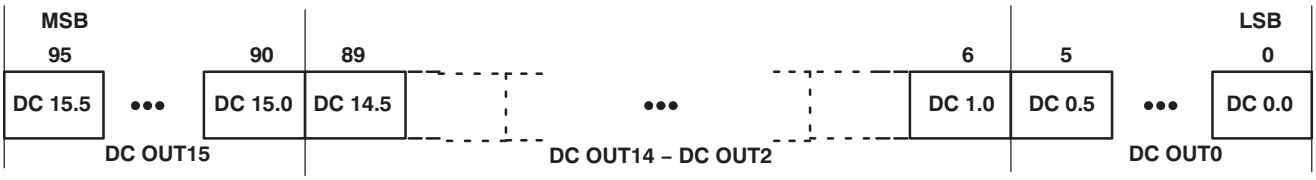

Figure 14. Dot Correction Data Packet Format

When VPRG is set to VCC, the TLC5940 enters the dot correction data input mode. The length of input shift register becomes 96 bits. After all serial data are shifted in, the TLC5940 writes the data in the input shift register to DC register when XLAT is high, and holds the data in the DC register when XLAT is low. The DC register is a level triggered latch of XLAT signal. Since XLAT is a level-triggered signal, SCLK and SIN must not be changed while XLAT is high. After XLAT goes low, data in the DC register is latched and does not change. BLANK signal does not need to be high to latch in new data. XLAT has setup time (tsu1) and hold time (th1) to SCLK as shown in Figure 15.

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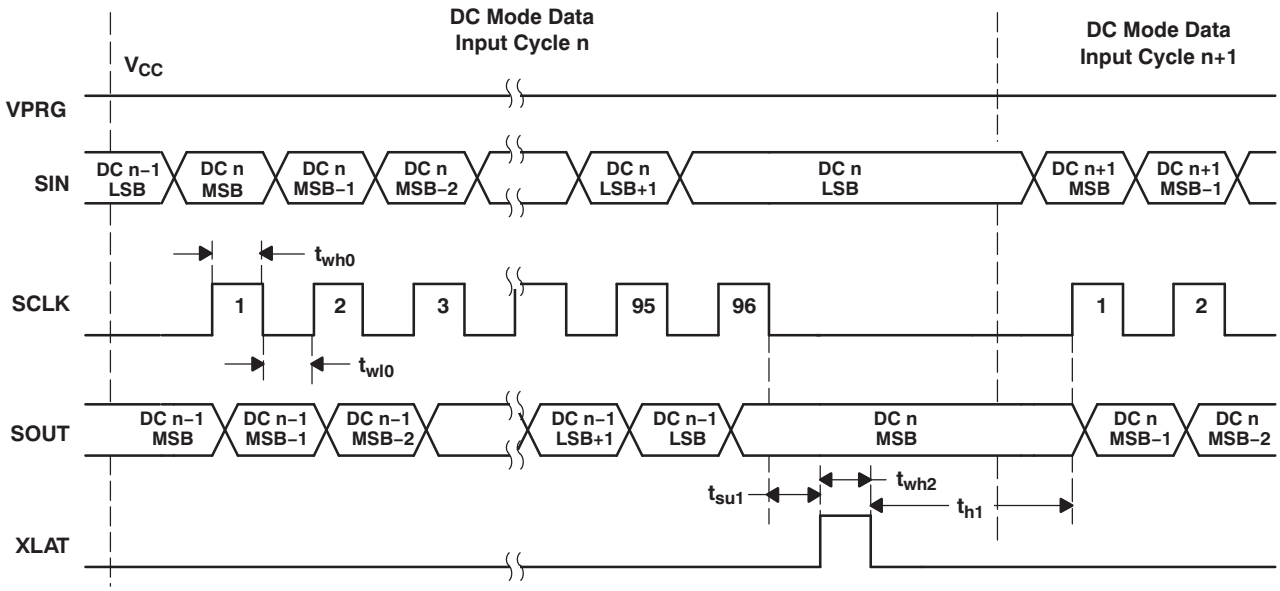

Figure 15. Dot Correction Data Input Timing Chart

The TLC5940 also has an EEPROM to store dot correction data. To store data from the dot correction register to EEPROM, DCPRG is set to high after applying V_{PRG} to the VPRG pin. Figure 16 shows the EEPROM programming timings. The EEPROM has a default value of all 1 s.

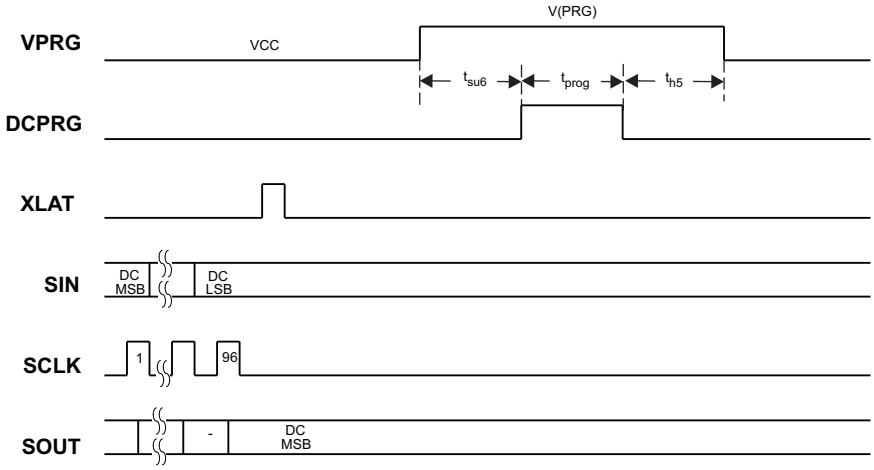

Figure 16. EEPROM Programming Timing Chart

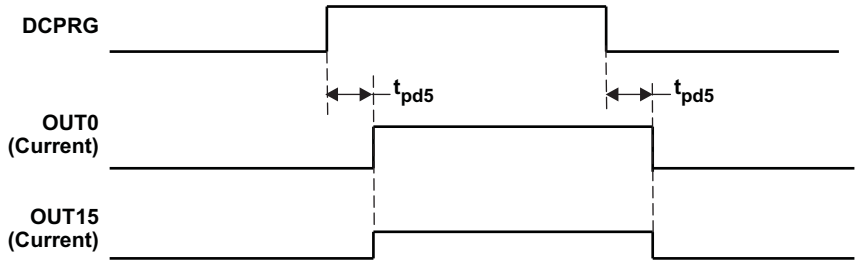

Figure 17. DCPRG and OUTn Timing Diagram

8.4.3 Setting Grayscale

The TLC5940 can adjust the brightness of each channel OUTn using a PWM control scheme. The use of 12 bits per channel results in 4096 different brightness steps, respective 0% to 100% brightness. Equation 8 determines the brightness level for each output n.

$$\text{Brightness in \%} = \frac{GSn}{4095} \times 100$$

where

- GSn = the programmed grayscale value for output n (GSn = 0 to 4095)
- n = 0 to 15
- Grayscale data for all OUTn (8)

Figure 18 shows the grayscale data packet format which consists of 12 bits x 16 channels, totaling 192 bits. The format is Big-Endian format. This means that the MSB is transmitted first, followed by the MSB-1, etc.

Figure 18. Grayscale Data Packet Format

When VPRG is set to GND, the TLC5940 enters the grayscale data input mode. The device switches the input shift register to 192-bit width. After all data is clocked in, a rising edge of the XLAT signal latches the data into the grayscale register (see Figure 11). New grayscale data immediately becomes valid at the rising edge of the XLAT signal; therefore, new grayscale data should be latched at the end of a grayscale cycle when BLANK is high.The first GS data input cycle after dot correction requires an additional SCLK pulse after the XLAT signal to complete the grayscale update cycle. All GS data in the input shift register is replaced with status information data (SID) after updated the grayscale register.

8.4.4 Status Information Output

The TLC5940 does have a status information register, which can be accessed in grayscale mode (VPRG=GND). After the XLAT signal latches the data into the GS register the input shift register data will be replaced with status information data (SID) of the device (see Figure 18). LOD, TEF, and dot correction EEPROM data (DCPRG=LOW) or dot correction register data (DCPRG=HIGH) can be read out at SOUT pin. The status information data packet is 192 bits wide. Bits 0-15 contain the LOD status of each channel. Bit 16 contains the TEF status. If DCPRG is low, bits 24-119 contain the data of the dot-correction EEPROM. If DCPRG is high, bits 24-119 contain the data of the dot-correction register.The remaining bits are reserved. The complete status information data packet is shown in Figure 19.

SOUT outputs the MSB of the SID at the same time the SID are stored in the SID register, as shown Figure 20. The next SCLK pulse, which will be the clock for receiving the SMB of the next grayscale data, transmits MSB-1 of SID. If output voltage is < 0.3 V (typical) when the output sink current turns on, LOD status flage becomes active. The LOD status flag is an internal signal that pulls XERR pin down to low when the LOD status flag becomes active. The delay time, tpd2 (1 µs maximum), is from the time of turning on the output sink current to the time LOD status flage becomes valid. The timing for each channel's LOD status to become valid is shifted by the 30-ns (maximum) channel-to-channel turn-on time. After the first GSCLK goes high, OUT0 LOD status is valid; tpd3 + tpd2 = 60 ns + 1 µs. OUT1 LOD status is valid; tpd3 + td + tpd2 = 60 ns + 30 ns + 1 µs = 1.09 µs. OUT2 LOD status is valid; tpd3 + 2*td + tpd2 = 1.12 µs, and so on. It takes 1.51 µs maximum (tpd3 + 15*td + tpd2) from the first GSCLK rising edge until all LOD become valid; *tsuLOD* must be > 1.51 µs (see Figure 20) to ensure that all LOD data are valid.

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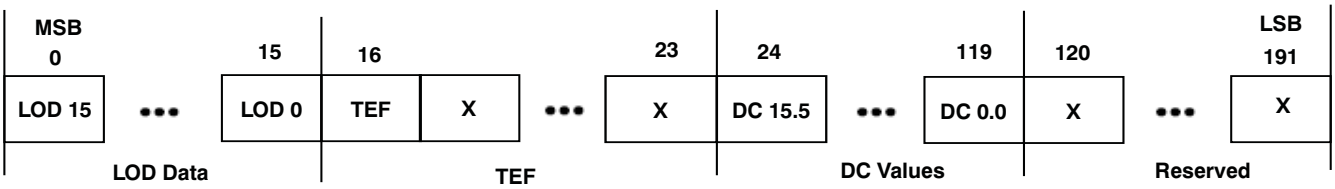

Figure 19. Status Information Data Packet Format

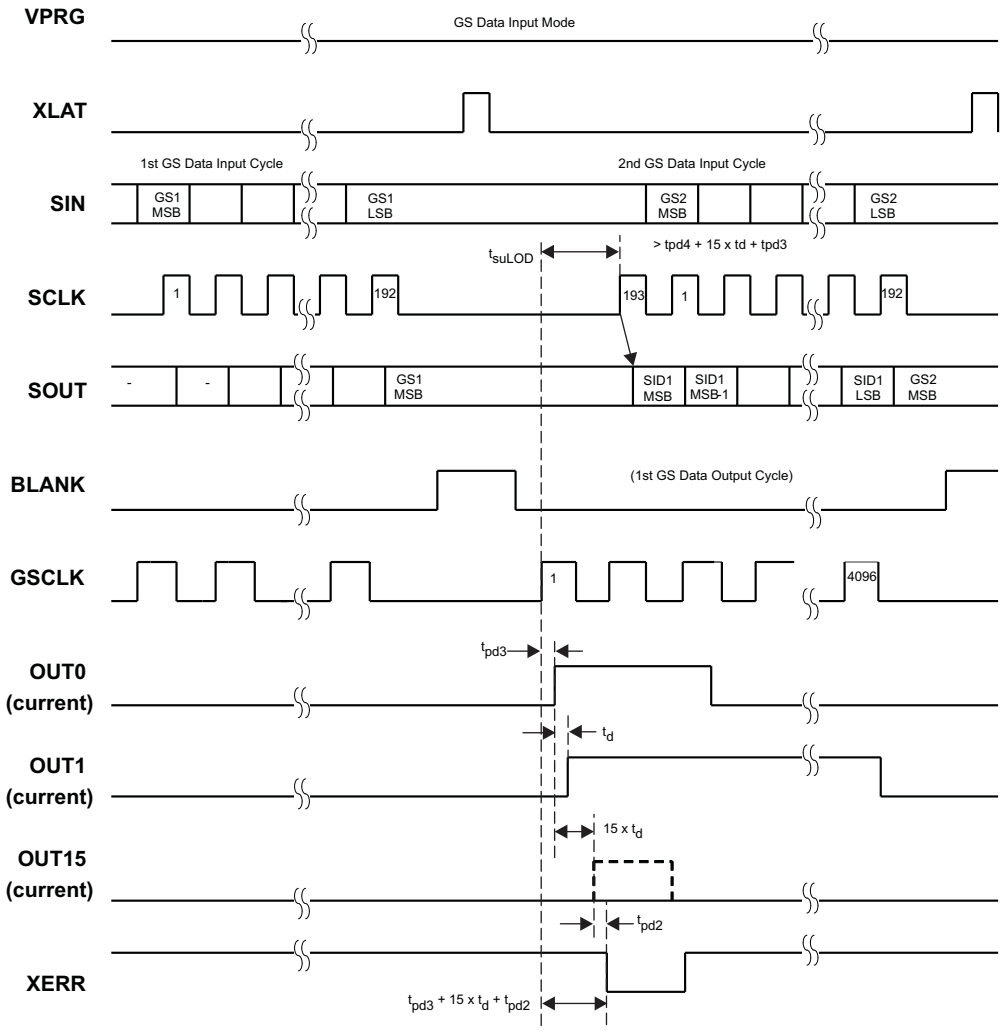

Figure 20. Readout Status Information Data (SID) Timing Chart

8.4.5 Grayscale PWM Operation

The grayscale PWM cycle starts with the falling edge of BLANK. The first GSCLK pulse after BLANK goes low increases the grayscale counter by one and switches on all OUTn with grayscale value not zero. Each following rising edge of GSCLK increases the grayscale counter by one. The TLC5940 compares the grayscale value of each output OUTn with the grayscale counter value. All OUTn with grayscale values equal to the counter values are switched off. A BLANK=H signal after 4096 GSCLK pulses resets the grayscale counter to zero and completes the grayscale PWM cycle (see Figure 21). When the counter reaches a count of FFFh, the counter stops counting and all outputs turn off. Pulling BLANK high before the counter reaches FFFh immediately resets the counter to zero.

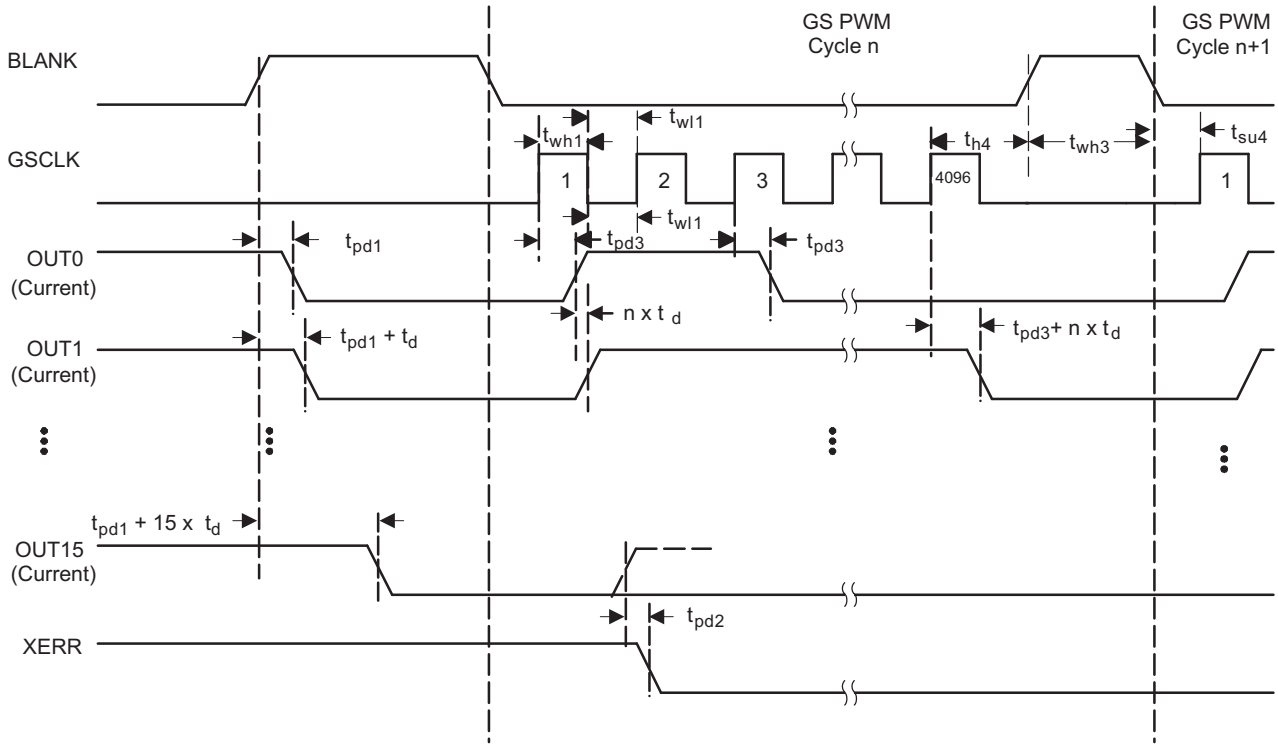

Figure 21. Grayscale PWM Cycle Timing Chart

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The device is a 16-channel, constant sink current, LED driver. This device can be connected in series to drive many LED lamps with only a few controller ports. Output current control data, dot correction data and PWM control data can be written from the SIN input terminal.

9.2 Typical Application

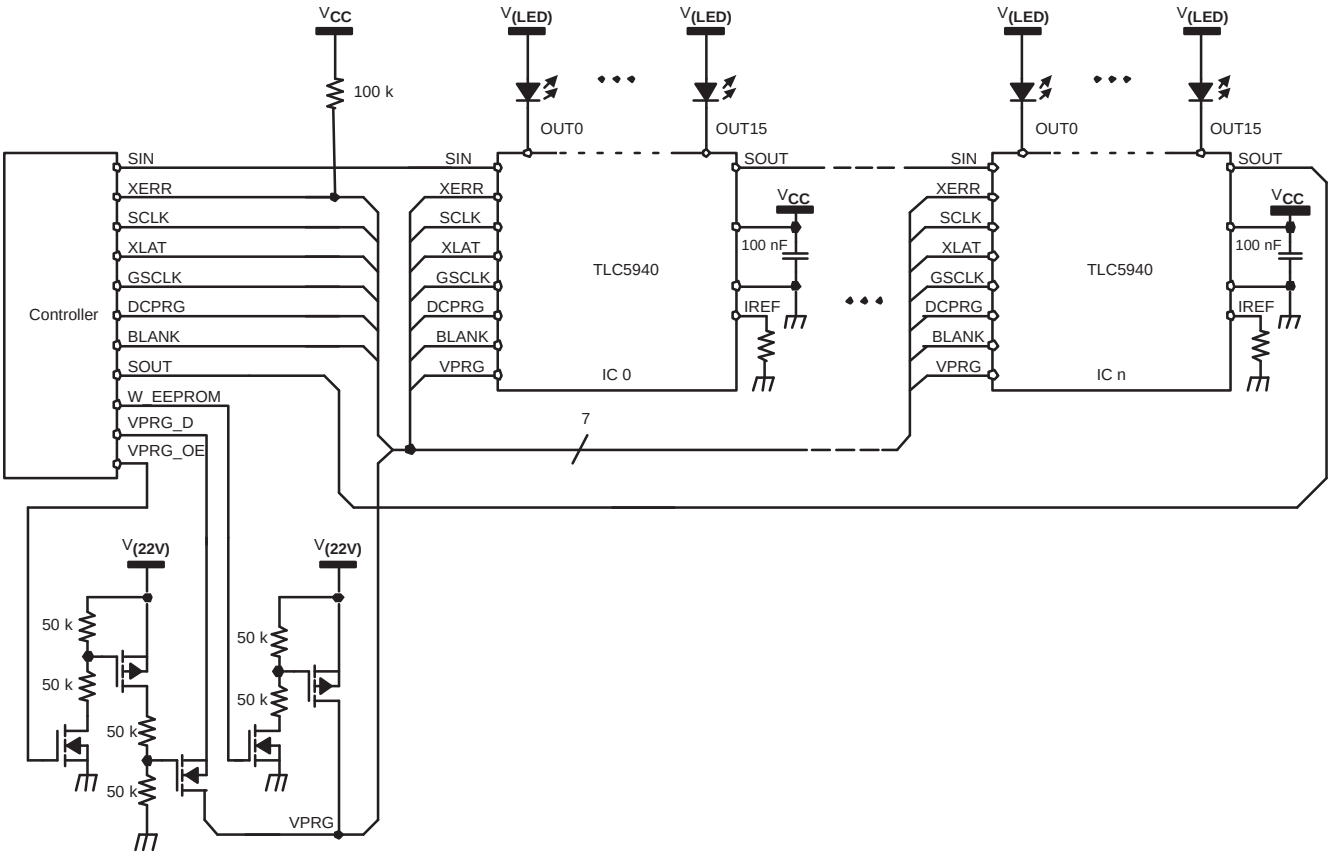

Figure 22. Cascading Devices

9.2.1 Design Requirements

For this design example, use the input parameters shown in Table 4.

Table 4. Design Parameters

PARAMETERS	VALUES
VCC input voltage range	3.0 V to 5.5 V
LED lamp (V_{LED}) input voltage range	>Maximum LED forward voltage (V_F) + IC knee voltage
SIN, SCLK, XLAT, GSCLK, and BLANK voltage range	Low level = GND, High level = VCC

9.2.2 Detailed Design Procedure

9.2.2.1 Serial Data Transfer Rate

Figure 22 shows a cascading connection of *n* TLC5940 devices connected to a controller, building a basic module of an LED display system. The maximum number of cascading TLC5940 devices depends on the application system and is in the range of 40 devices. Equation 9 calculates the minimum frequency needed:

$$f_{(GSCLK)} = 4096 \times f_{(update)}$$

$$f_{(SCLK)} = 193 \times f_{(update)} \times n \tag{9}$$

where

- $f_{(GSCLK)}$: minimum frequency needed for GSCLK
- $f_{(SCLK)}$: minimum frequency needed for SCLK and SIN
- $f_{(update)}$: update rate of whole cascading system
- n: number cascaded of TLC5940 device

9.2.2.2 Grayscale (GS) Data

There are a total of 16 sets of 12-bit GS data for the PWM control of each output. Select the GS data of each LED lamp and write the GS data to the register following the signal timing.

9.2.3 Application Curve

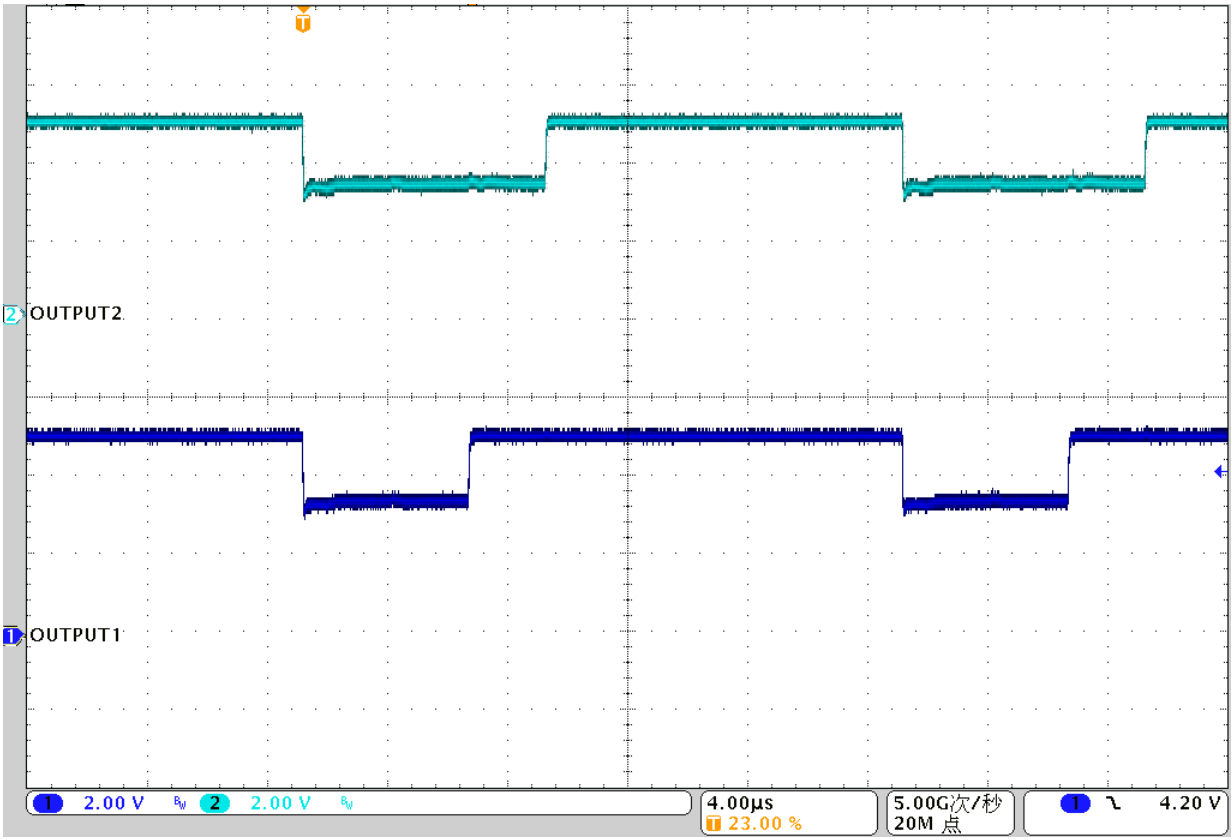

Figure 23. Output Waveform with Different Grayscale PWM Data

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10 Power Supply Recommendations

The V_{CC} power supply voltage should be decoupled by placing a 0.1uF ceramic capacitor close to VCC pin and GND plane. Depending on panel size, several electrolytic capacitors must be placed on board equally distributed to get a well regulated LED supply voltage (VLED). VLED voltage ripple should be less than 5% of its nominal value. Furthermore, the VLED should be set to the voltage calculated by equation:

VLED > VF + 0.4V (10mA constant current example) where Vf = maximum forward voltage of all LEDs.

11 Layout

11.1 Layout Guidelines

1. Place the decoupling capacitor near the VCC pin and GND plane.
2. Place the current programming resistor Riref close to IREF pin and IREFGND pin.
3. Route the GND pattern as widely as possible for large GND currents.
4. Routing wire between the LED cathode side and the device OUTn pin should be as short and straight as possible to reduce wire inductance.
5. When several ICs are chained, symmetric placements are recommended.

11.2 Layout Example

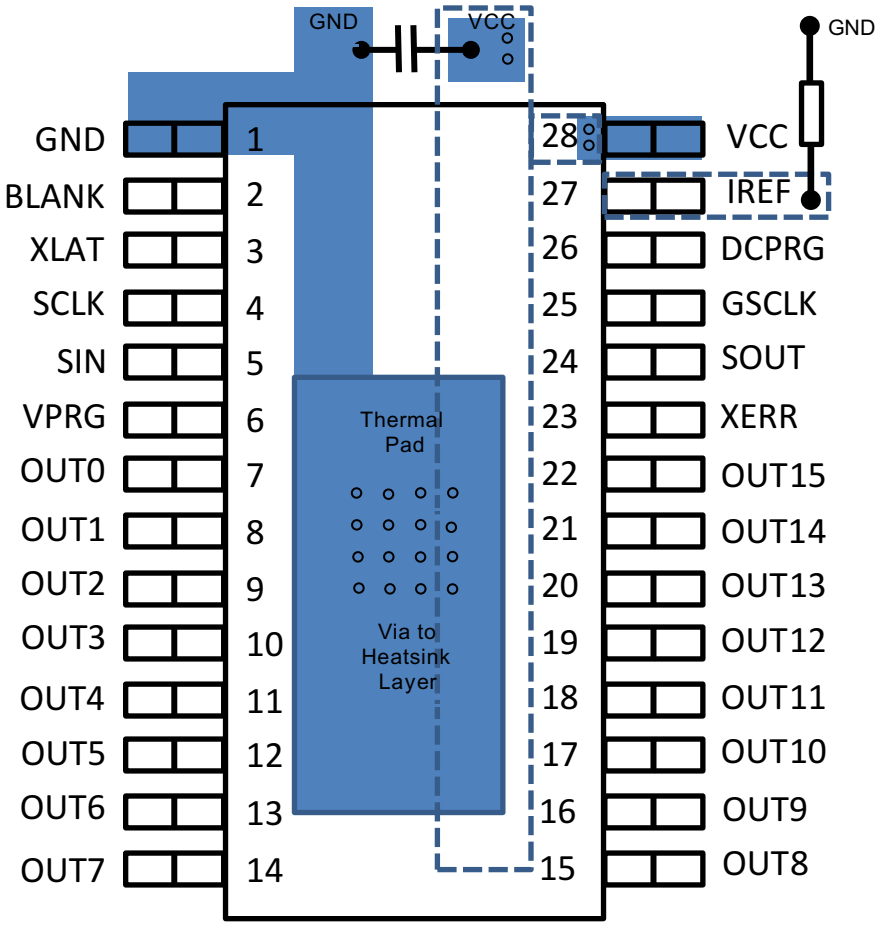

Figure 24. Layout Recommendation

11.3 Power Dissipation Calculation

The device power dissipation must be below the power dissipation rating of the device package to ensure correct operation. Equation 10 calculates the power dissipation of device.

$$P_D = \left(V_{CC} \times I_{CC}\right) + \left(V_{OUT} \times I_{MAX} \times \frac{DC_n}{63} \times d_{PWM} \times N\right)$$

where

- V_{CC}: device supply voltage
- I_{CC}: device supply current
- V_{OUT}: TLC5940 OUTn voltage when driving LED current
- I_{MAX}: LED current adjusted by $R_{(IREF)}$ Resistor
- DC_n: maximum dot correction value for OUTn
- N: number of OUTn driving LED at the same time
- d_{PWM}: duty cycle defined by BLANK pin or GS PWM value (10)

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12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC5940PWP	Obsolete	Production	HTSSOP (PWP) | 28	-	-	Call TI	Call TI	-40 to 85	TLC5940
TLC5940PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5940
TLC5940PWPR.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5940
TLC5940PWPR.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5940
TLC5940PWPRG4	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5940
TLC5940RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5940
TLC5940RHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5940
TLC5940RHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5940
TLC5940RHBRG4	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5940

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC5940 :

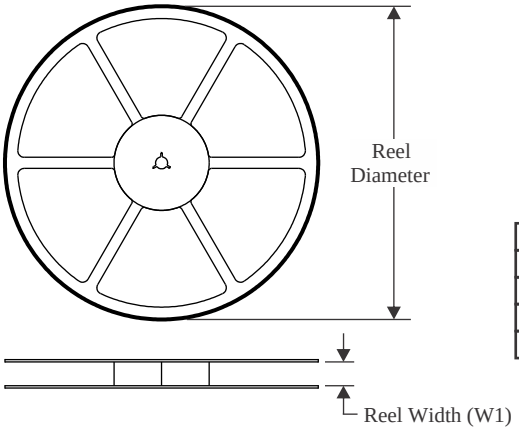
- Enhanced Product : TLC5940-EP

NOTE: Qualified Version Definitions:

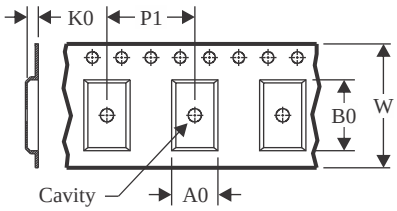
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

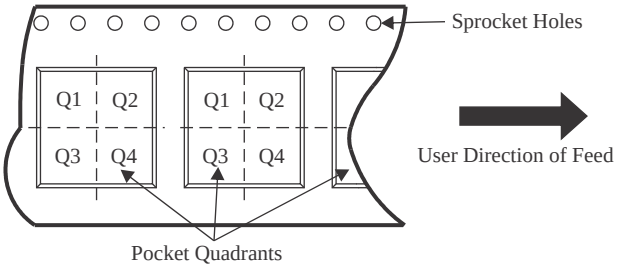


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

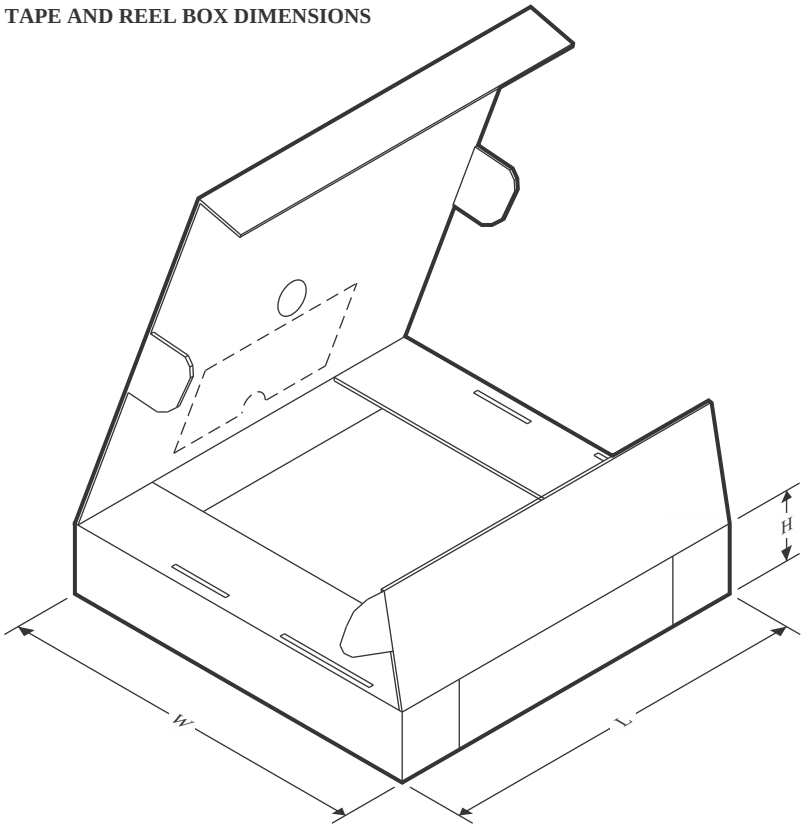
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5940PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
TLC5940RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5940PWPR	HTSSOP	PWP	28	2000	356.0	356.0	35.0
TLC5940RHBR	VQFN	RHB	32	3000	356.0	356.0	35.0

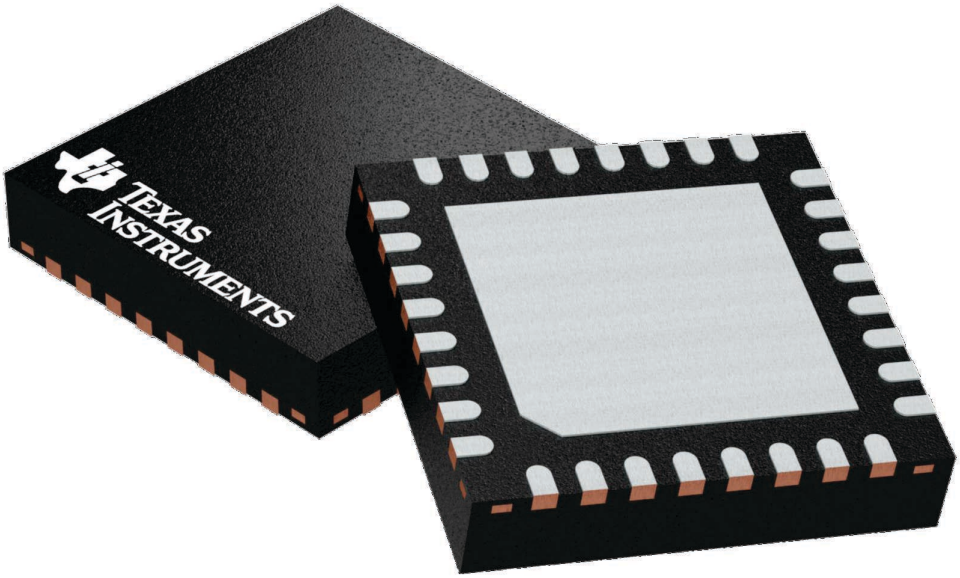
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

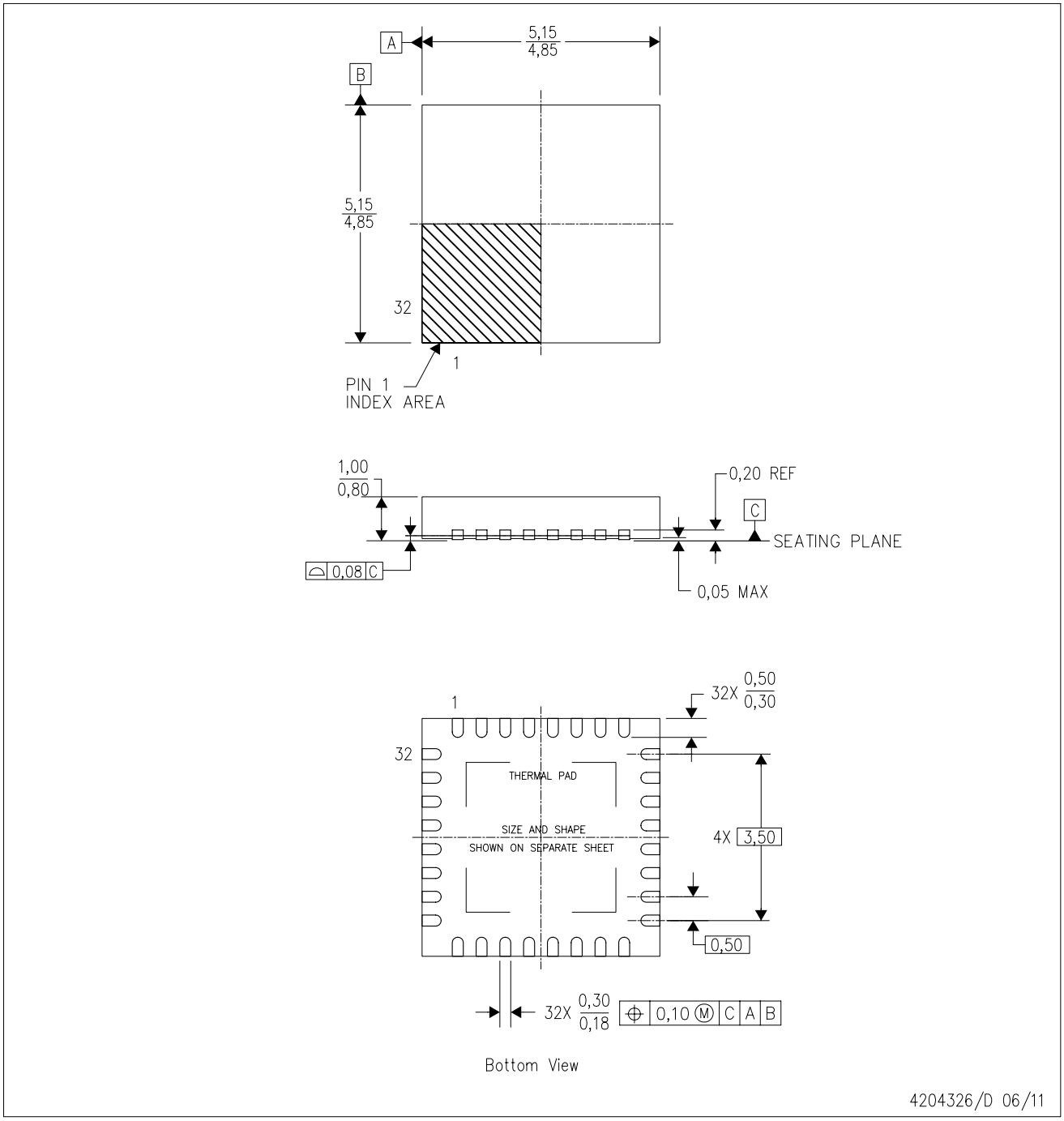
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

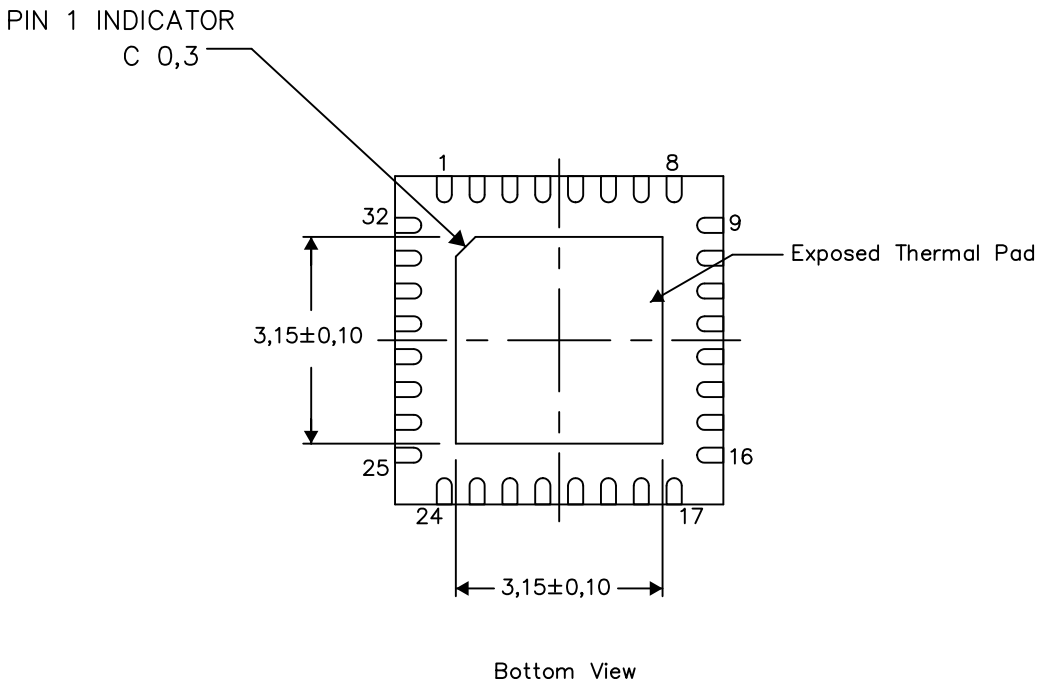
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

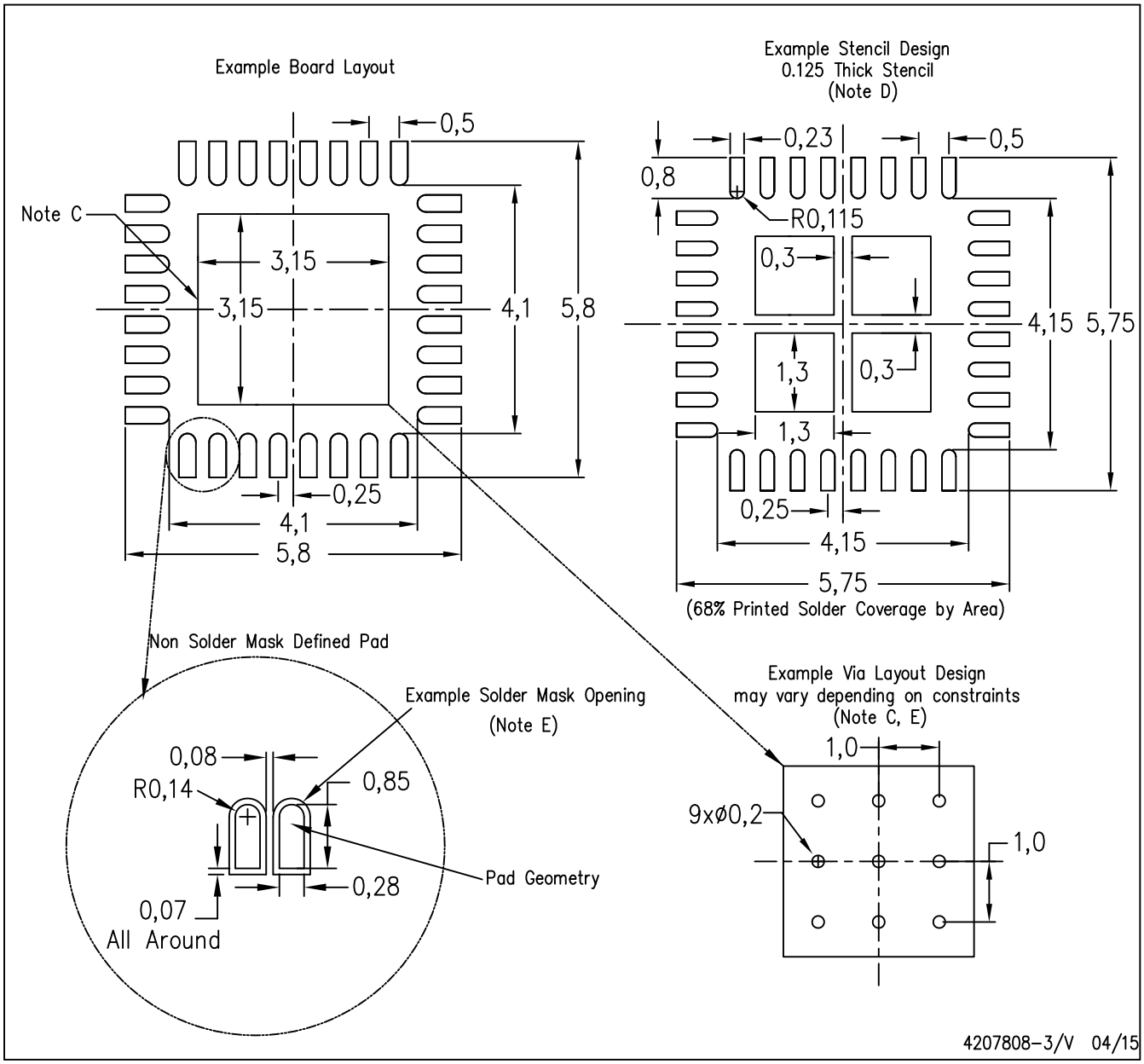


Exposed Thermal Pad Dimensions

4206356–3/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

GENERIC PACKAGE VIEW

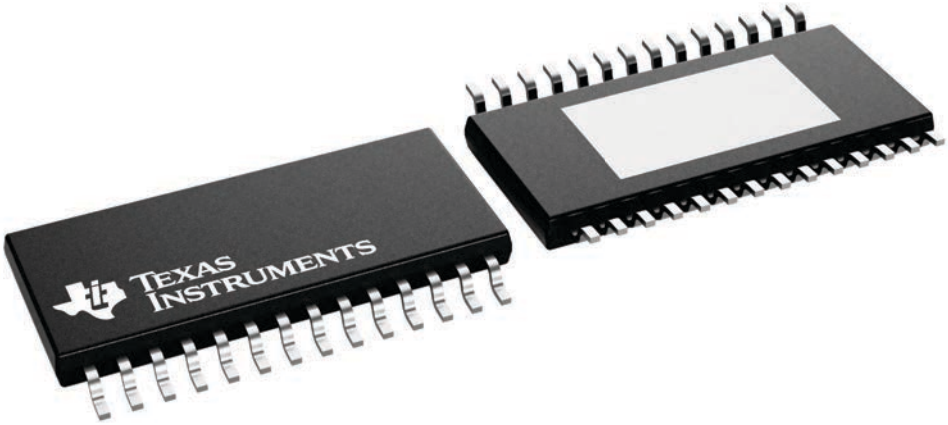
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

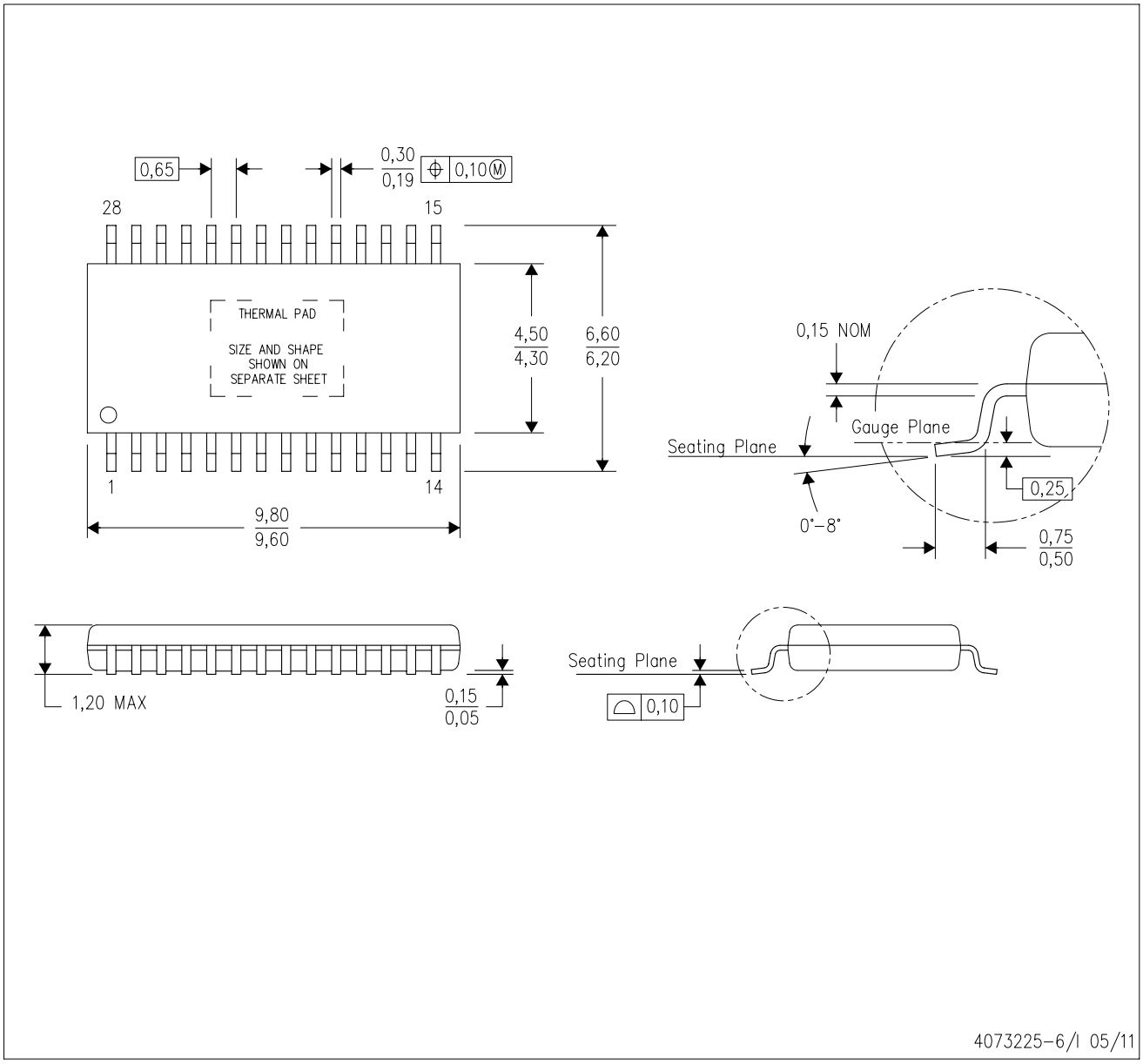
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R-PDSO-G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

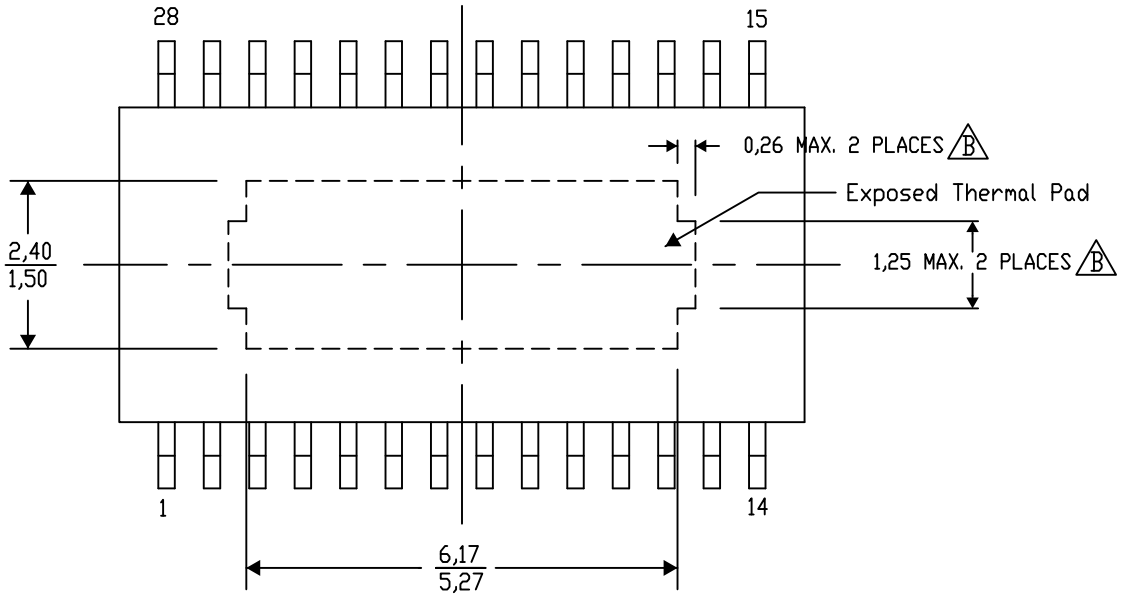
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

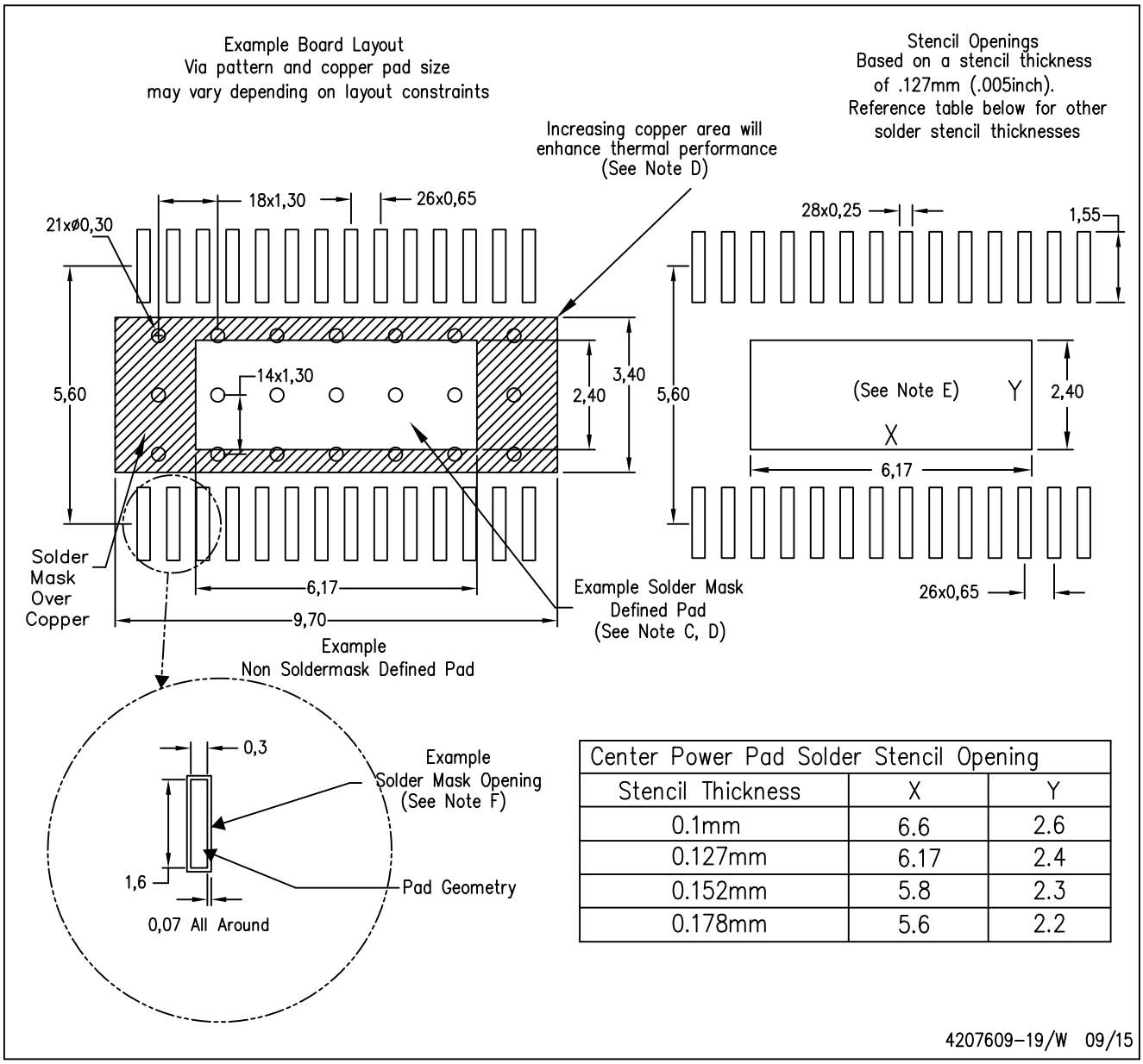
4206332-33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609-19/W 09/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
- E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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