ADC12L080 12-Bit, 80 MSPS, 450 MHz Bandwidth A/D Converter with Internal Reference

Check for Samples: ADC12L080

FEATURES

- **Single Supply Operation**
- **Low Power Consumption**
- **Power Down Mode**
- **Internal or External Reference**
- **Selectable Offset Binary or 2's Complement Data Format**
- **Pin-Compatible with ADC12010, ADC12020, ADC12040, ADC12L063, ADC12L066**

APPLICATIONS

- **Ultrasound and Imaging**
- **Instrumentation**
- **Cellular Base Stations/Communication Receivers**
- **Sonar/Radar**
- **xDSL**
- **Wireless Local Loops**
- **Data Acquisition Systems**
- **DSP Front Ends**

KEY SPECIFICATIONS

- **Full Power Bandwidth: 450 MHz**
- **DNL: ±0.4 LSB (typ)**
- **SNR (f_{IN} = 10 MHz): 66 dB (typ)**
- **SFDR (f_{IN} = 10 MHz): 80 dB (typ)**
- **Power Consumption, 80 MHz**
  - **Operating: 425 mW (typ)**
  - **Power Down: 50 mW (typ)**

DESCRIPTION

The ADC12L080 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 80 Megasamples per second (MSPS). This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to minimize die size and power consumption while providing excellent dynamic performance. The ADC12L080 can be operated with either the internal or an external reference. Operating on a single 3.3V power supply, this device consumes just 425 mW at 80 MSPS, including the reference current. The Power Down feature reduces power consumption to just 50 mW.

The differential inputs provide a full scale input swing equal to $\pm V_{REF}$. The buffered, high impedance, single-ended external reference input is converted on-chip to a differential reference for use by the processing circuitry. Output data format may be selected as either offset binary or two's complement.

This device is available in the 32-lead LQFP package and operates over the industrial temperature range of −40°C to +85°C.

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Connection Diagram

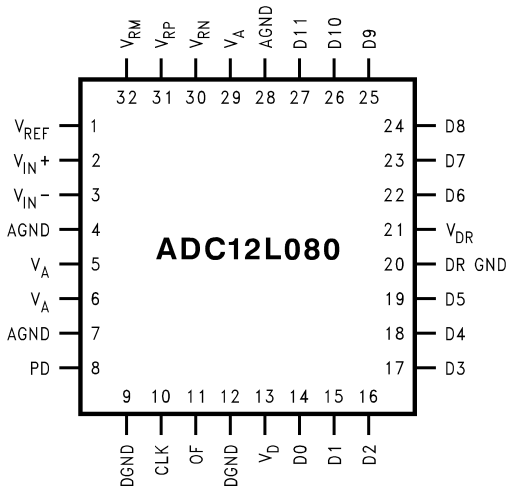
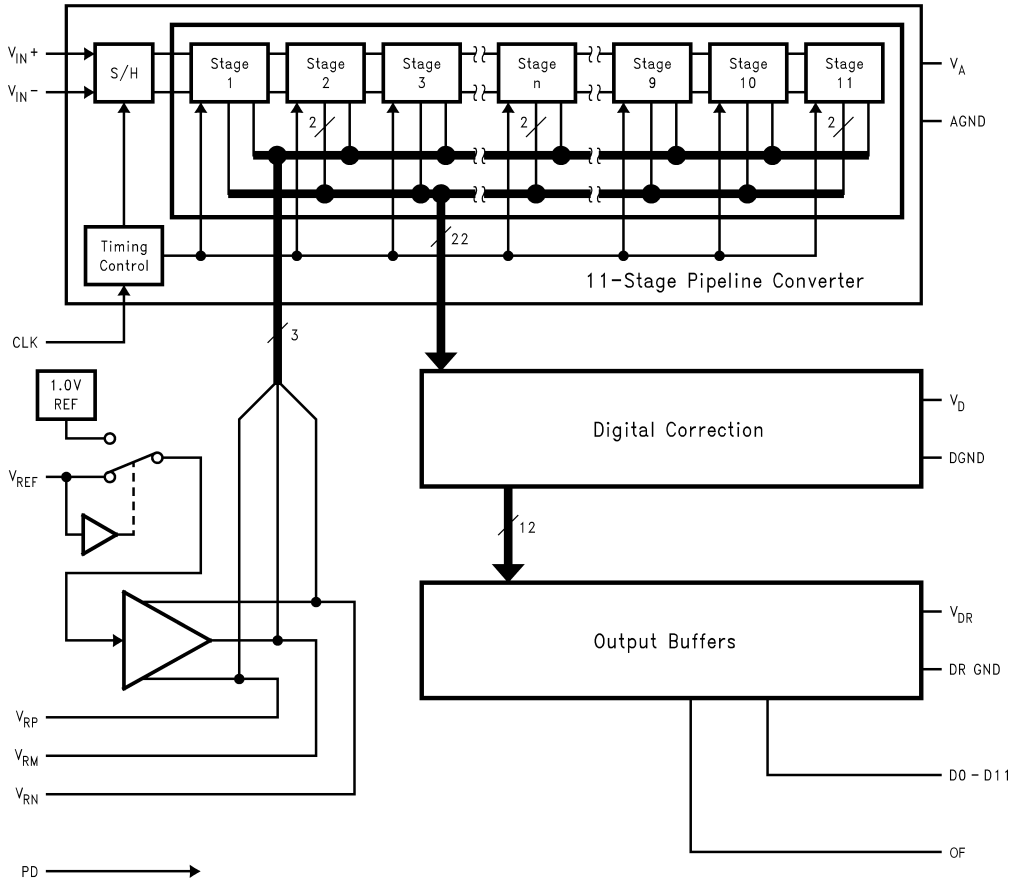


Figure 1. 32-Lead LQFP Package
See Package Number NEY0032A

Block Diagram



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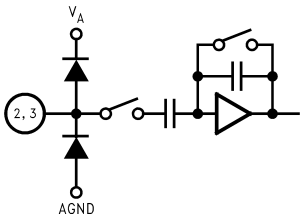
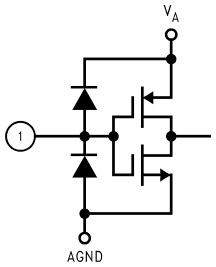
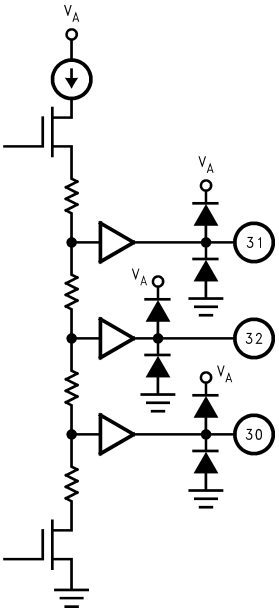
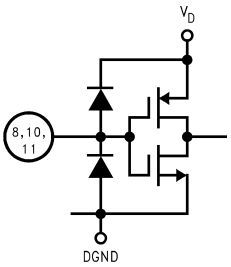
Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
2	V_{IN}^+		Differential analog signal Input pins. With a 1.0V reference voltage the full-scale differential input signal level is 2.0 V_{P-P} with each input pin centered on a common mode voltage, V_{CM}. The V_{IN}- pin may be connected to V_{CM} for single-ended operation, but a differential input signal is required for best performance.
3	V_{IN}^-		
1	V_{REF}		Reference input. This pin should be connected to V_A to use the internal 1.0V reference. If it is desired to use an external reference voltage, this pin should be bypassed to AGND with a 0.1 µF low ESL capacitor. Specified operation is with a V_{REF} of 1.0V, but the device will function well with a V_{REF} range indicated in the Electrical Tables.
31	V_{RP}		These pins are high impedance reference bypass pins only. Connect a 0.1 µF capacitor from each of these pins to AGND. Connect a 1.0 µF capacitor from V_{RP} to V_{RN}. DO NOT LOAD these pins.
32	V_{RM}		
30	V_{RN}		
DIGITAL I/O			
10	CLK		Digital clock input. The range of frequencies for this input is 10 MHz to 80 MHz with guaranteed performance at 80 MHz. The input is sampled on the rising edge of this input.
11	OF		Output format selection. When this pin is LOW, the output format is offset binary. When this pin is HIGH the output format is two's complement. This pin may be changed asynchronously, but such a change will result in errors for one or two conversions.
8	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.

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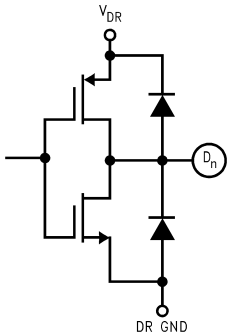
Pin Descriptions and Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent Circuit	Description
14–19, 22–27	D0–D11		Digital data output pins that make up the 12-bit conversion results. D0 is the LSB, while D11 is the MSB of the output word.
ANALOG POWER			
5, 6, 29	V_A		Positive analog supply pins. These pins should be connected to a quiet +3.3V source and bypassed to AGND with 0.1 µF low ESL capacitors located within 1 cm of these power pins, and with a 10 µF capacitor.
4, 7, 28	AGND		The ground return for the analog supply.
DIGITAL POWER			
13	V_D		Positive digital supply pin. This pin should be connected to the same quiet +3.3V source as is V_A and bypassed to DGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor, both located within 1 cm of the power pin.
9, 12	DGND		The ground return for the digital supply.
21	V_{DR}		Positive digital supply pin for the ADC12L080's output drivers. This pin should be connected to a voltage source in the range indicated in the Operating Ratings table and be bypassed to DR GND with a 0.1 µF capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF capacitor. The voltage at this pin should never exceed the voltage on V_D by more than 300 mV. All bypass capacitors should be located within 1 cm of the supply pin.
20	DR GND		The ground return for the digital supply for the ADC12L080's output drivers. This pin should be connected to the system digital ground, but not be connected in close proximity to the ADC12L080's DGND or AGND pins. See LAYOUT AND GROUNDING for more details.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2][3]

V_A, V_D, V_{DR}		4.2V
$\|V_A–V_D\|$		≤ 100 mV
$V_{DR}–V_D$		≤ 300 mV
Voltage on Any Pin		−0.3V to V_A or (V_D + 0.3V)
Input Current at Any Pin[4]		±25 mA
Package Input Current[4]		±50 mA
Package Dissipation at T_A = 25°C		See[5]
ESD Susceptibility	Human Body Model[6]	2500V
	Machine Model[6]	250V
Soldering Temperature, Infrared, 10 sec.[7]		235°C
Storage Temperature		−65°C to +150°C

(1) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A, V_D or V_{DR}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula P_DMAX = ($T_J$max - T_A)/θ_{JA}. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.
(7) The 235°C reflow temperature refers to infrared reflow. For Vapor Phase Reflow (VPR), the following Conditions apply: Maintain the temperature at the top of the package body above 183°C for a minimum 60 seconds. The temperature measured on the package body must not exceed 220°C. Only one excursion above 183°C is allowed per reflow cycle.

Operating Ratings[1][2]

Operating Temperature	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A, V_D)	+3.0V to +3.60V
Output Driver Supply (V_{DR})	+2.4V to V_D
V_{REF}	0.8V to 1.5V
CLK, PD, OF	−0.05V to V_D + 0.05V
V_{IN} Input	−0V to (V_A − 0.5V)
V_{CM}	0.5V to (V_A-1.5V)
|AGND–DGND|	0V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

Package Thermal Resistances

Package	θ_{J-A}
32-Lead LQFP	79°C / W

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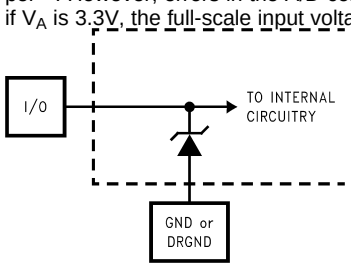
Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D$ = +3.3V, V_{DR} = +2.5V, PD = 0V, V_{REF} = +1.0V external, V_{CM} = 1.65V, R_S < 100Ω, f_{CLK} = 80 MHz, $t_r = t_f$ = 2 ns, f_{IN} = 70 MHz, C_L = 15 pF/pin. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits T_J = 25°C (1)(2)(3)(4)

Symbol	Parameter	Conditions		Typical (4)	Limits (4)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits
INL	Integral Non Linearity	Best Fit Method		±1.2	**4.0**	LSB (max)
					-3.3	LSB (min)
DNL	Differential Non Linearity	No missing codes		±0.4	**1.5**	LSB (max)
					-1.0	LSB (min)
GE	Gain Error	Positive Error		−0.15	**+5.7** **-2**	%FS (max) %FS (min)
		Negative Error		+0.4	**+5** **-3.7**	%FS (max) %FS (min)
	Offset Error (V_{IN}+ = V_{IN}−)			+0.2	**+1.7** **-0.6**	%FS (max)
	Under Range Output Code			0	**0**	
	Over Range Output Code			4095	**4095**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CM}	Common Mode Input Voltage			1.65	0.5	V (min)
					2.0	V (max)
C_{IN}	V_{IN} Input Capacitance (each pin to GND)	V_{IN} = 1.0 Vdc + 1 V_{P-P}	(CLK LOW)	8		pF
			(CLK HIGH)	7		pF
V_{REF}	Reference Voltage (5)(6)			1.0	0.8	V (min)
					1.5	V (max)

(1) The inputs are protected as shown below. Input voltages above V_A or below GND will not damage this device, provided current is limited per(6). However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 3.3V, the full-scale input voltage must be ≤3.4V to ensure accurate conversions.



(2) To guarantee accuracy, it is required that $|V_A–V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V (2 V_{P-P} differential input), the 12-bit LSB is 488 µV.
(4) Typical figures are at $T_A = T_J$ = 25°C, and represent most likely parametric norms. Test limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).
(5) Optimum dynamic performance will be obtained by keeping the reference input in the 0.8V to 1.5V range. The LM4051CIM3-ADJ or the LM4051CIM3-1.2 band gap voltage reference is recommended for this application.
(6) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or $V_{IN} > V_A$, V_D or V_{DR}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

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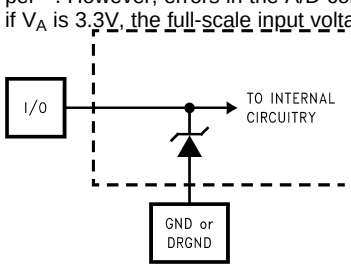
DC and Logic Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, V_{REF} = +1.0V external, V_{CM} = 1.65V, R_S < 100Ω, f_{CLK} = 80 MHz, t_r = t_f = 2 ns, f_{IN} = 70 MHz, C_L = 15 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C (1)(2)(3)(4)

Symbol	Parameter	Conditions	Typical (4)	Limits (4)	Units (Limits)
DYNAMIC CONVERTER CHARACTERISTICS					
BW	Full Power Bandwidth	-0.5 dBFS Input, Output at −3 dB	450		MHz
SNR	Signal-to-Noise Ratio	f_{IN} = 10 MHz, Differential V_{IN} = −0.5 dBFS	66	**64**	dB (min)
		f_{IN} = 40 MHz, Differential V_{IN} = −0.5 dBFS	65		dB
		f_{IN} = 70 MHz, Differential V_{IN} = −0.5 dBFS	65	**63**	dB (min)
		f_{IN} = 150 MHz, Differential V_{IN} = −0.5 dBFS	63		dB
SINAD	Signal-to-Noise & Distortion	f_{IN} = 10 MHz, Differential V_{IN} = −0.5 dBFS	66	**63**	dB (min)
		f_{IN} = 40 MHz, Differential V_{IN} = −0.5 dBFS	64.5		dB
		f_{IN} = 70 MHz, Differential V_{IN} = −0.5 dBFS	64	**62.7**	dB (min)
		f_{IN} = 150 MHz, Differential V_{IN} = −0.5 dBFS	62		dB
ENOB	Effective Number of Bits	f_{IN} = 10 MHz, Differential V_{IN} = −0.5 dBFS	10.7	**10.2**	Bits (min)
		f_{IN} = 40 MHz, Differential V_{IN} = 0.5 dBFS	10.4		Bits
		f_{IN} = 70 MHz, Differential V_{IN} = −0.5 dBFS	10.3	**10.1**	Bits (min)
		f_{IN} = 150 MHz, Differential V_{IN} = −0.5 dBFS	10.0		Bits
THD	Total Harmonic Distortion	f_{IN} = 10 MHz, Differential V_{IN} = −0.5 dBFS	−77	**-66**	dB (max)
		f_{IN} = 40 MHz, Differential V_{IN} = −0.5 dBFS	-74		dB
		f_{IN} = 70 MHz, Differential V_{IN} = −0.5 dBFS	-71	**-65**	dB (max)
		f_{IN} = 150 MHz, Differential V_{IN} = −0.5 dBFS	-70		dB
2nd Harm	Second Harmonic Distortion	f_{IN} = 10 MHz, Differential V_{IN} = −0.5 dBFS	−80	**-68**	dB (max)
		f_{IN} = 40 MHz, Differential V_{IN} = −0.5 dBFS	-80		dB
		f_{IN} = 70 MHz, Differential V_{IN} = −0.5 dBFS	-80	**-65.5**	dB (max)
		f_{IN} = 150 MHz, Differential V_{IN} = −0.5 dBFS	-79		dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 10 MHz, Differential V_{IN} = −0.5 dBFS	−84	**-69**	dB (max)
		f_{IN} = 40 MHz, Differential V_{IN} = −0.5 dBFS	-81		dB
		f_{IN} = 70 MHz, Differential V_{IN} = −0.5 dBFS	-79	**-66**	dB (max)
		f_{IN} = 150 MHz, Differential V_{IN} = −0.5 dBFS	-78		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 10 MHz, Differential V_{IN} = −0.5 dBFS	80	**68**	dB (min)
		f_{IN} = 40 MHz, Differential V_{IN} = −0.5 dBFS	77		dB
		f_{IN} = 70 MHz, Differential V_{IN} = −0.5 dBFS	74	**-65.5**	dB (min)
		f_{IN} = 150 MHz, Differential V_{IN} = −0.5 dBFS	73		dB
IMD	Intermodulation Distortion	$f_{IN}1$ = 19.6MHz, $f_{IN}2$ = 20.5 MHz, each = -6.0 dBFS	66		dBFS

(1) The inputs are protected as shown below. Input voltages above V_A or below GND will not damage this device, provided current is limited per(6). However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 3.3V, the full-scale input voltage must be ≤3.4V to ensure accurate conversions.



(2) To guarantee accuracy, it is required that $|V_A–V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V (2 V_{P-P} differential input), the 12-bit LSB is 488 µV.
(4) Typical figures are at T_A = T_J = 25°C, and represent most likely parametric norms. Test limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).

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DC and Logic Electrical Characteristics (continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D$ = +3.3V, V_{DR} = +2.5V, PD = 0V, V_{REF} = +1.0V external, V_{CM} = 1.65V, R_S < 100Ω, f_{CLK} = 80 MHz, $t_r = t_f$ = 2 ns, f_{IN} = 70 MHz, C_L = 15 pF/pin. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits T_J = 25°C(1)(2)(3)(4)

Symbol	Parameter	Conditions	Typical (4)	Limits (4)	Units (Limits)
CLK, PD, OF DIGITAL INPUT CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_D = 3.3V		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	V_D = 3.3V		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	V_{IN}+, V_{IN}− = 3.3V	10		µA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN}+, V_{IN}− = 0V	−10		µA
C_{IN}	Digital Input Capacitance		5		pF
D0–D11 DIGITAL OUTPUT CHARACTERISTICS					
$V_{OUT(1)}$	Logical "1" Output Voltage	I_{OUT} = −0.5 mA		**V_{DR} − 0.18**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{OUT} = 1.6 mA		**0.4**	V (max)
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V	−20		mA
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = 2.5V	20		mA
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD Pin = DGND PD Pin = V_{DR}	120 10	**168**	mA (max) mA
I_D	Digital Supply Current	PD Pin = DGND PD Pin = V_{DR}	6 5	**11.5**	mA (max) mA
I_{DR}	Digital Output Supply Current	PD Pin = DGND, f_{in} = 0(5)(6) PD Pin = V_{DR}	<1 0		mA mA
	Total Power Consumption	PD Pin = DGND, C_L = 0 pF(7) PD Pin = V_{DR}	425 50	**590**	mW (max) mW
PSRR1	Power Supply Rejection Ratio	Rejection of Full-Scale Gain Error change with V_A = 3.0V vs. 3.6V	41		dB

(5) I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). $I_{DR}=V_{DR}(C_0 \times f_0 + C_1 \times f_1 + ...C_{11} \times f_{11})$ where V_{DR} is the output driver power supply voltage, C_n is total capacitance on the output pin, and f_n is the average frequency at which that pin is toggling.

(6) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or $V_{IN} > V_A$, V_D or V_{DR}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

(7) Power consumption excludes output driver power. See Note 5.

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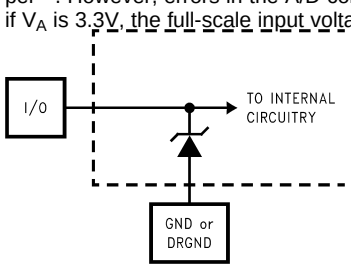
AC Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D$ = +3.3V, V_{DR} = +2.5V, PD = 0V, V_{REF} = +1.0V external, V_{CM} = 1.65V, R_S < 100Ω, f_{CLK} = 80 MHz, $t_r = t_f$ = 2 ns, f_{IN} = 70 MHz, C_L = 15 pF/pin. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits T_J = 25°C (1)(2)(3)(4)(5)(6)

Symbol	Parameter	Conditions	Typical (4)	Limits (4)	Units (Limits)
	Maximum Clock Frequency			**80**	MHz (min)
	Minimum Clock Frequency		10		MHz
	Clock Duty Cycle		60 40		% (max) % (min)
t_{CH}	Clock High Time		5.5		ns (min)
t_{CL}	Clock Low Time		5.5		ns (min)
t_{CONV}	Conversion Latency			**6**	Clock Cycles
t_{OD}	Data Output Delay after Rising CLK Edge	V_{DR} = 2.5V	5.2	**8.3**	ns (max)
		V_{DR} = 3.3V	4.8	**7.5**	ns (max)
t_{AD}	Aperture Delay		2		ns
t_{AJ}	Aperture Jitter		0.7		ps rms
t_{PD}	Power Down Mode Exit Cycle	0.1 µF on pins 30, 31, 32, and 1.0 µF from pin 30 to 31	1		µs

(1) The inputs are protected as shown below. Input voltages above V_A or below GND will not damage this device, provided current is limited per(6). However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 3.3V, the full-scale input voltage must be ≤3.4V to ensure accurate conversions.



(2) To guarantee accuracy, it is required that $|V_A–V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V (2 V_{P-P} differential input), the 12-bit LSB is 488 µV.
(4) Typical figures are at $T_A = T_J$ = 25°C, and represent most likely parametric norms. Test limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).
(5) Timing specifications are tested at TTL logic levels, V_{IL} = 0.4V for a falling edge and V_{IH} = 2.4V for a rising edge.
(6) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or $V_{IN} > V_A$, V_D or V_{DR}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Specification Definitions

APERTURE DELAY is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

COMMON MODE VOLTAGE (V_{CM}) is the d.c. potential present at both signal inputs to the ADC.

CONVERSION LATENCY See PIPELINE DELAY.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

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FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

$$\text{Gain Error} = \text{Positive Full Scale Error} - \text{Offset Error} \tag{1}$$

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a best fit straight line. The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC12L080 is guaranteed not to have any missing codes.

NEGATIVE FULL SCALE ERROR is the difference between the input voltage ($V_{IN}+ - V_{IN}-$) just causing a transition from negative full scale to the first code and its ideal value of 0/5 LSB.

OFFSET ERROR is the input voltage that will cause a transition from a code of 01 1111 1111 to a code of 10 0000 0000/

OUTPUT DELAY is the time delay after the rising edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. PSRR1 is the ratio of the change in Full-Scale Gain Error that results from a change in the d.c. power supply voltage, expressed in dB. PSRR2 is a measure of how well an a.c. signal riding upon the power supply is rejected at the output.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$\text{THD} = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}} \tag{2}$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power in the first 9 harmonic frequencies.

Second Harmonic Distortion (2nd Harm) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

Third Harmonic Distortion (3rd Harm) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

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Timing Diagram

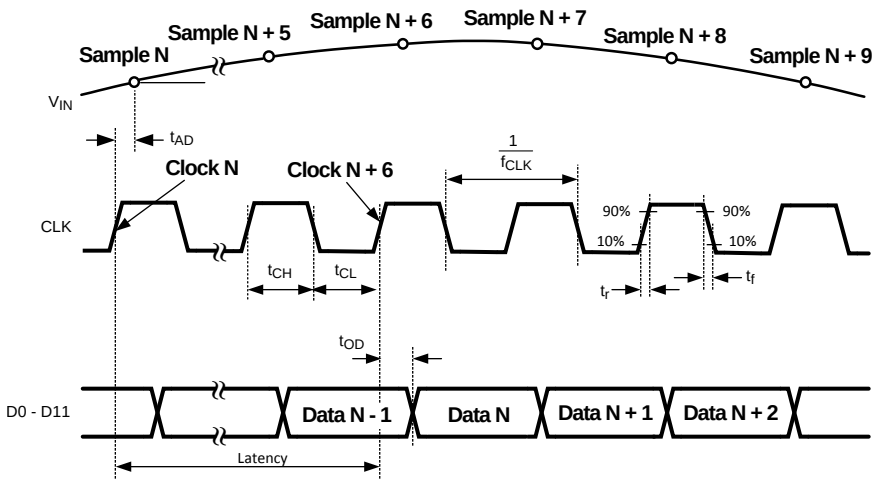

Figure 2. Output Timing

Transfer Characteristic

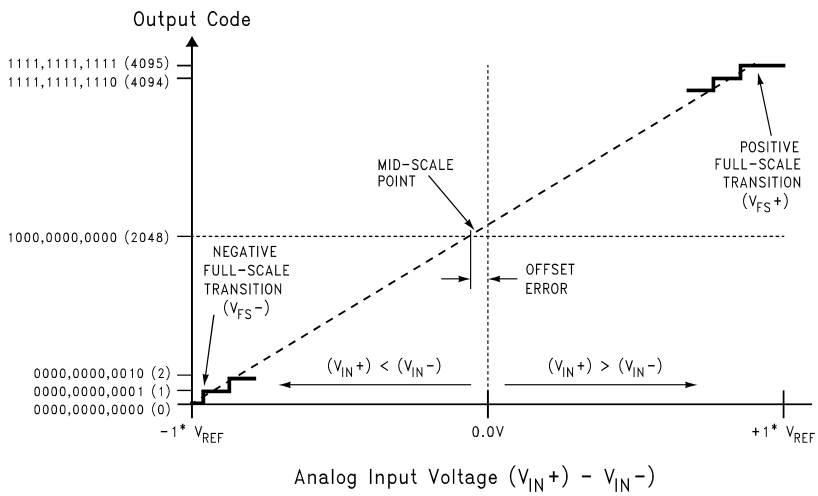

Figure 3. Transfer Characteristic

Typical Performance Characteristics DNL, INL

$V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $V_{REF} = 1.0V$ external, $V_{CM} = 1.65V$, $f_{CLK} = 80$ MHz, $f_{IN} = 0$, unless otherwise stated.

DNL

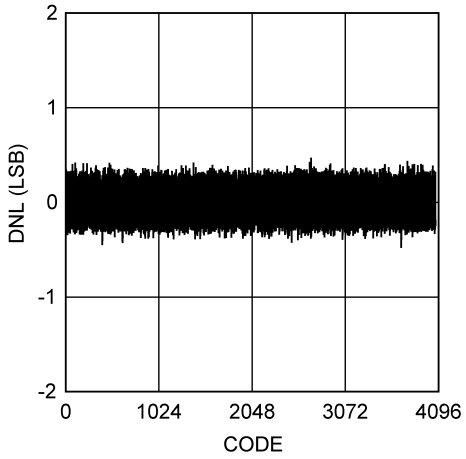

Figure 4.

INL

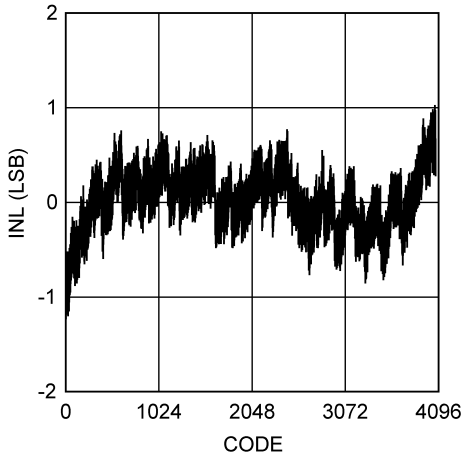

Figure 5.

DNL vs. f_{CLK}

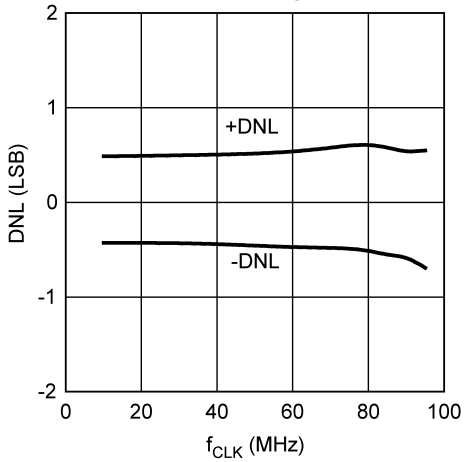

Figure 6.

INL vs. f_{CLK}

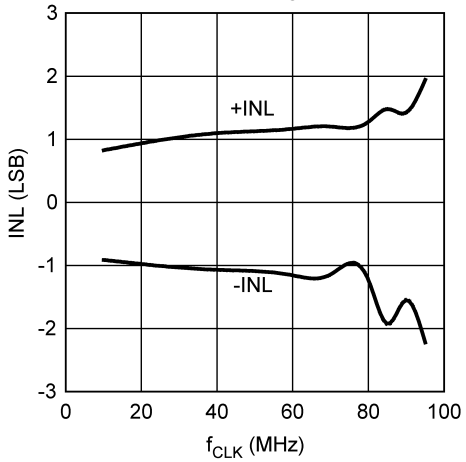

Figure 7.

DNL vs. Clock Duty Cycle

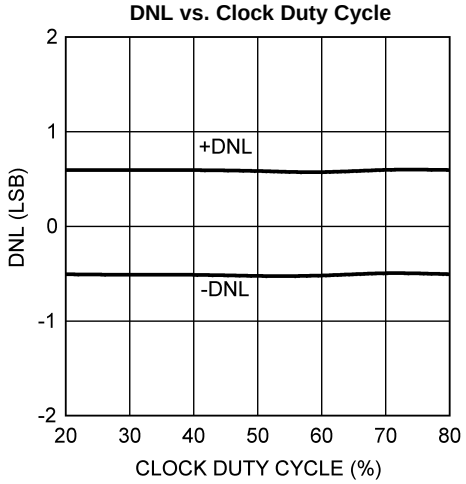

Figure 8.

INL vs. Clock Duty Cycle

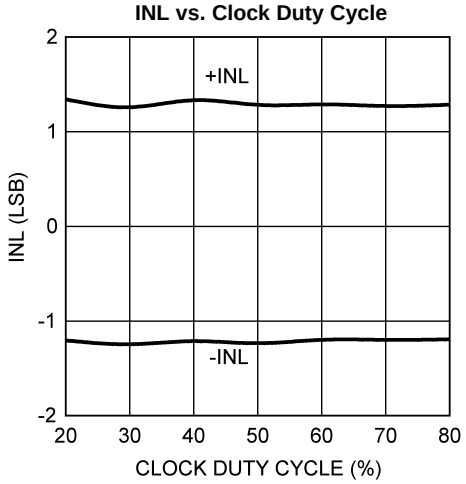

Figure 9.

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Typical Performance Characteristics DNL, INL (continued)

$V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $V_{REF} = 1.0V$ external, $V_{CM} = 1.65V$, $f_{CLK} = 80$ MHz, $f_{IN} = 0$, unless otherwise stated.

DNL vs. Temperature

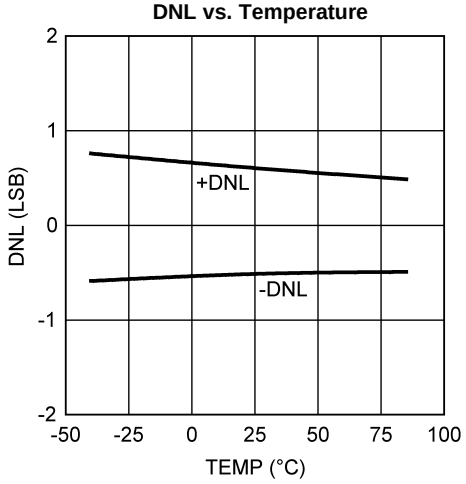

Figure 10.

INL vs. Temperature

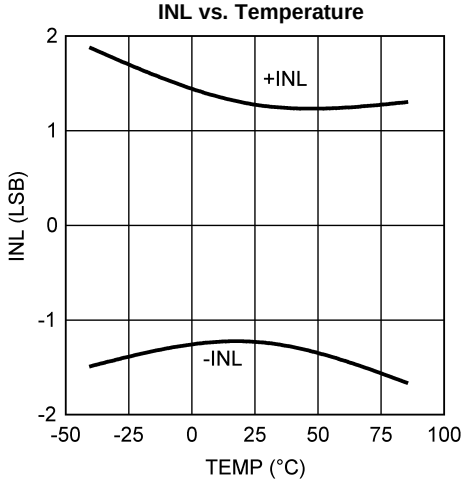

Figure 11.

DNL vs. V_{DR}

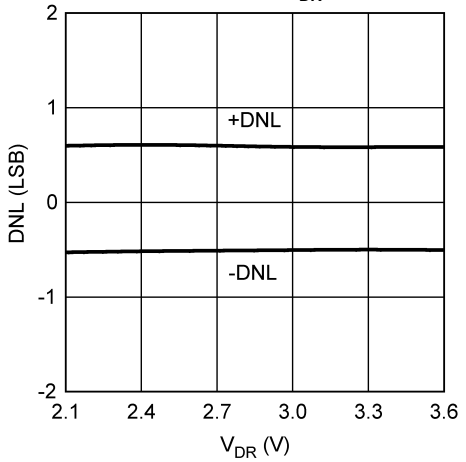

Figure 12.

INL vs. V_{DR}

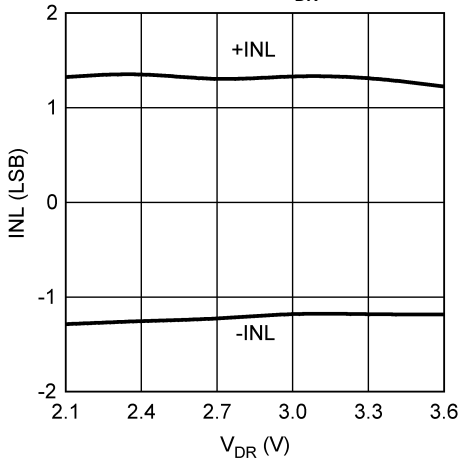

Figure 13.

Typical Performance Characteristics

$V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $V_{REF} = 1.0V$ external, $V_{CM} = 1.65V$, $f_{CLK} = 80$ MHz, $f_{IN} = 70$ MHz, unless otherwise stated.

SNR,SINAD,SFDR vs. V_A

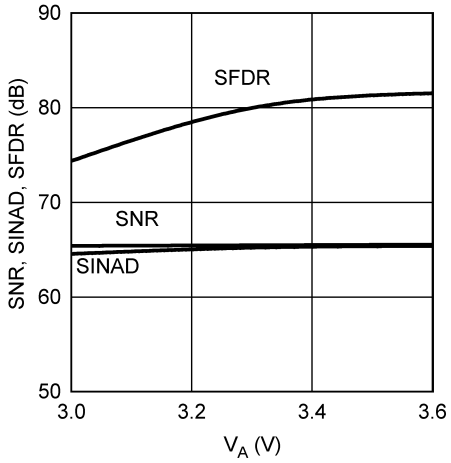

Figure 14.

Distortion vs. V_A

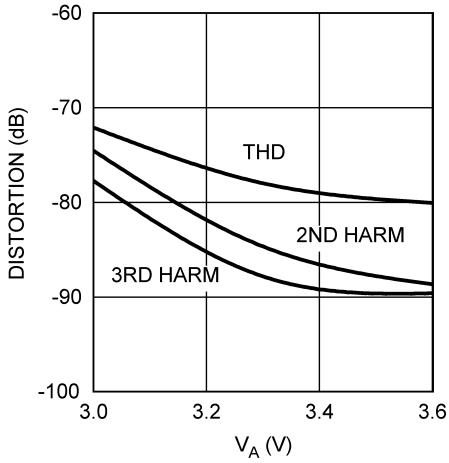

Figure 15.

SNR,SINAD,SFDR vs. V_{DR}

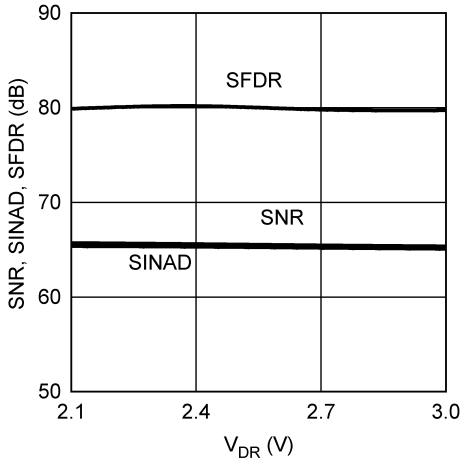

Figure 16.

Distortion vs. V_{DR}

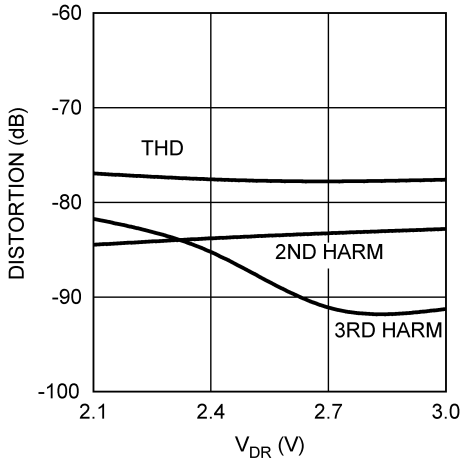

Figure 17.

SNR,SINAD,SFDR vs. V_{CM}

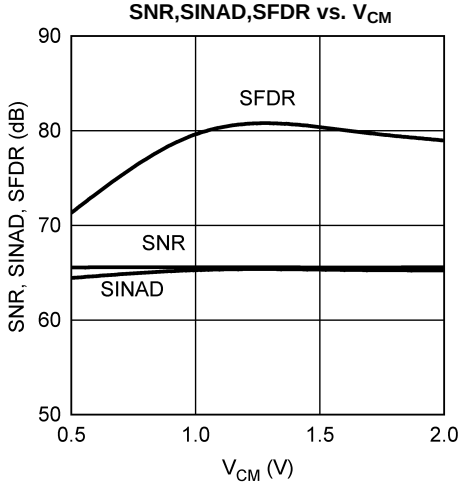

Figure 18.

Distortion vs. V_{CM}

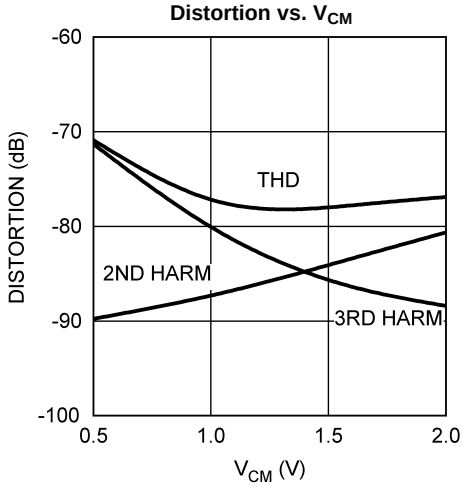

Figure 19.

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Typical Performance Characteristics (continued)

$V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $V_{REF} = 1.0V$ external, $V_{CM} = 1.65V$, $f_{CLK} = 80$ MHz, $f_{IN} = 70$ MHz, unless otherwise stated.

SNR,SINAD,SFDR vs. f_{CLK}

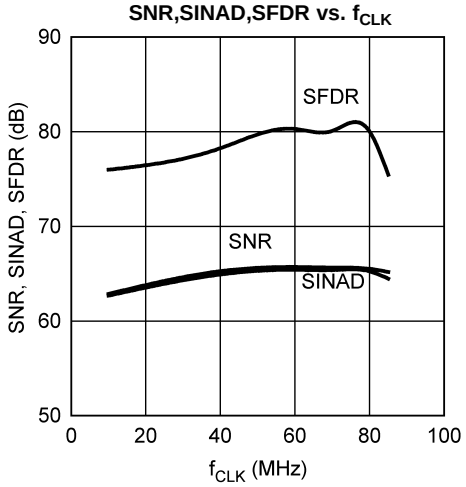

Figure 20.

Distortion vs. f_{CLK}

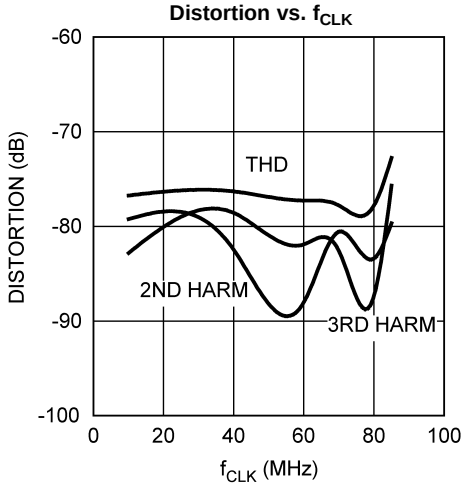

Figure 21.

SNR,SINAD,SFDR vs. Clock Duty Cycle

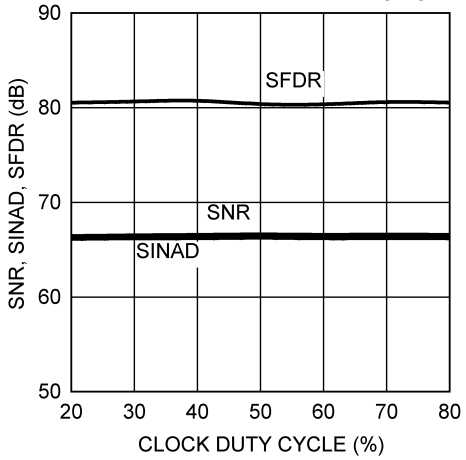

Figure 22.

Distortion vs. Clock Duty Cycle

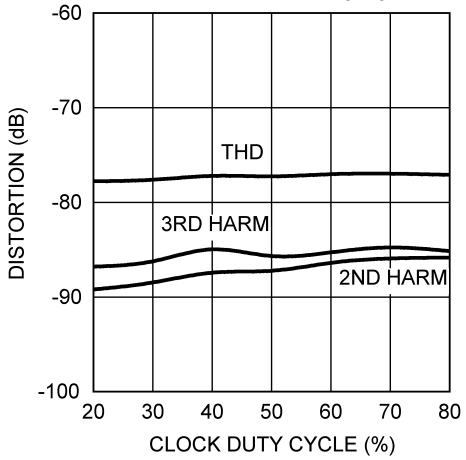

Figure 23.

SNR,SINAD,SFDR vs. V_{REF}

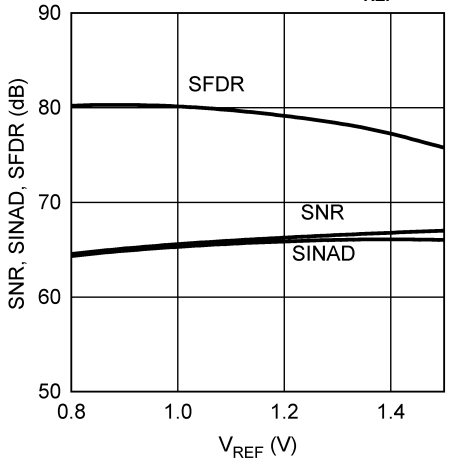

Figure 24.

Distortion vs. V_{REF}

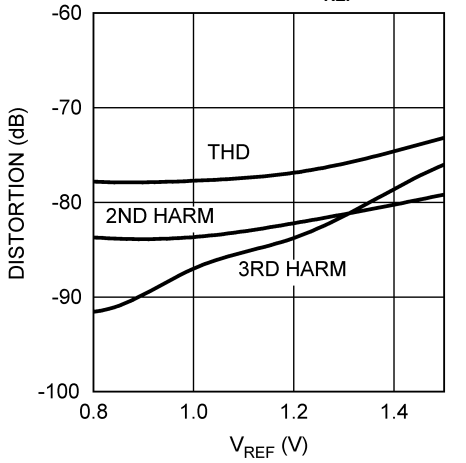

Figure 25.

Typical Performance Characteristics (continued)

$V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $V_{REF} = 1.0V$ external, $V_{CM} = 1.65V$, $f_{CLK} = 80$ MHz, $f_{IN} = 70$ MHz, unless otherwise stated.

SNR,SINAD,SFDR vs. f_{IN}

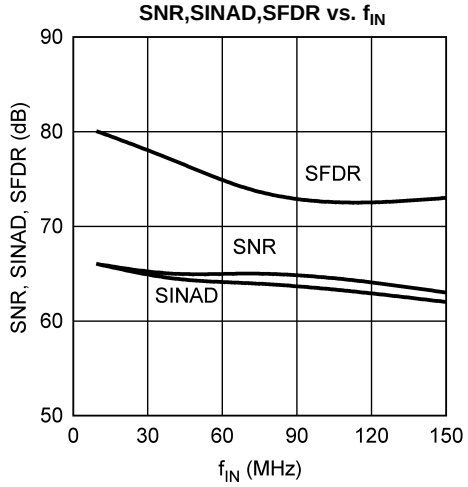

Figure 26.

Distortion vs. f_{IN}

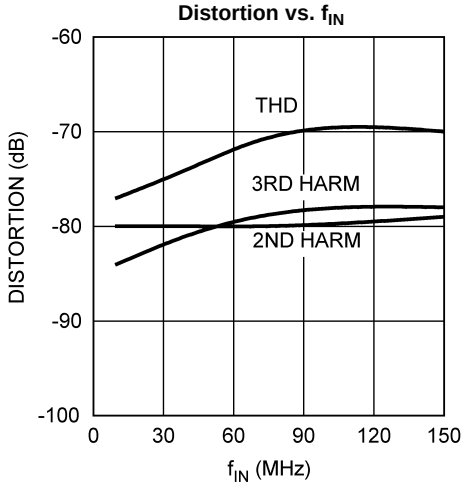

Figure 27.

SNR,SINAD,SFDR vs. Temperature

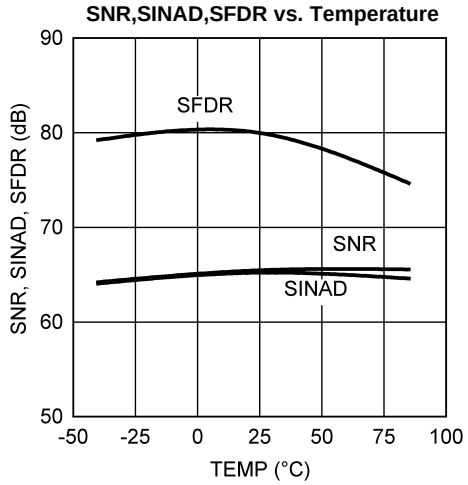

Figure 28.

Distortion vs. Temperature

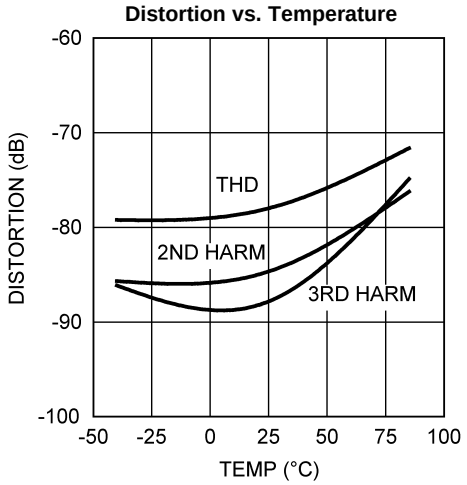

Figure 29.

t_{OD} vs. V_{DR}

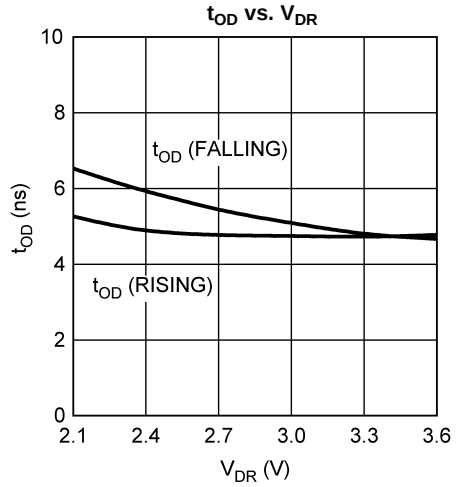

Figure 30.

Spectral Response @ 10 MHz Input

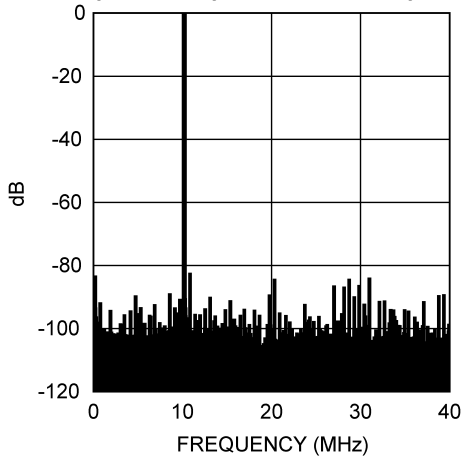

Figure 31.

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Typical Performance Characteristics (continued)

$V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $V_{REF} = 1.0V$ external, $V_{CM} = 1.65V$, $f_{CLK} = 80$ MHz, $f_{IN} = 70$ MHz, unless otherwise stated.

Spectral Response @ 40 MHz Input

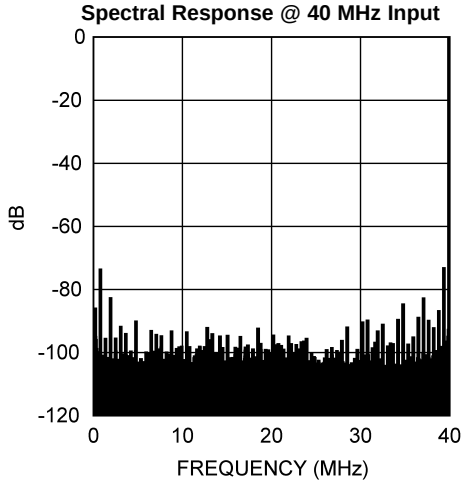

Figure 32.

Spectral Response @ 70 MHz Input

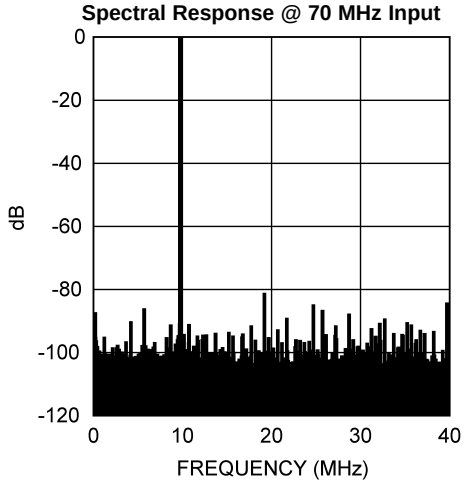

Figure 33.

Spectral Response @ 150 MHz Input

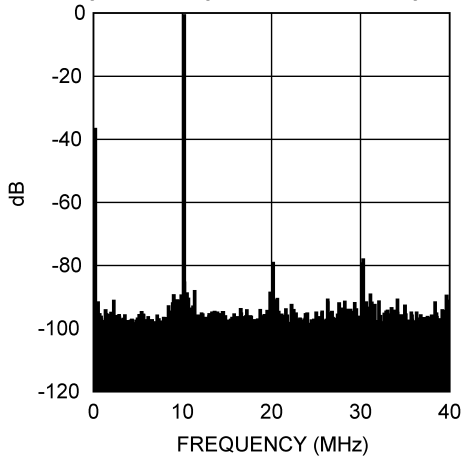

Figure 34.

Intermodulation Distortion, $f_{IN}1$= 19.6 MHz, $f_{IN}2$ = 20.5 MHz

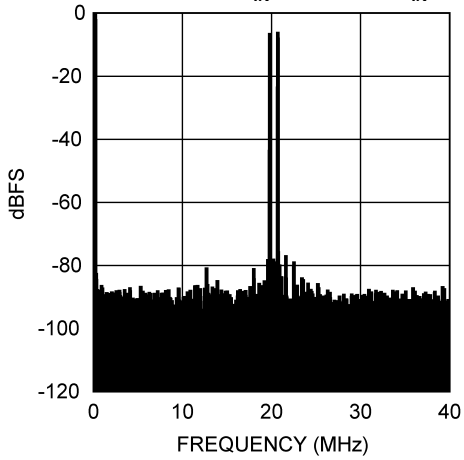

Figure 35.

FUNCTIONAL DESCRIPTION

Operating on a single +3.3V supply, the ADC12L080 uses a pipeline architecture with error correction circuitry to help ensure maximum performance.

Differential analog input signals are digitized to 12 bits. Each analog input signal should have a peak-to-peak voltage equal to the input reference voltage, V_{REF}, be centered around V_{REF} and be 180° out of phase with each other. Table 1 and Table 2 indicate the input to output relationship of the ADC12L080. Although a differential input signal is required for rated operation, single-ended operation is possible with reduced performance if one input is biased to V_{REF} and the other input is driven. If the driven input is presented with its full range signal, there will be a 6 dB reduction of the output range, limiting it to the range of ¼ to ¾ of the minimum output range obtainable if both inputs were driven with complimentary signals. Signal Inputs explains how to avoid this signal reduction.

Table 1. Input to Output Relationship—Differential Input

V_{IN}^+	V_{IN}^-	Output
$V_{CM} - V_{REF}$	$V_{CM} + V_{REF}$	0000 0000 0000
$V_{CM} - 0.5 * V_{REF}$	$V_{CM} + 0.5 * V_{REF}$	0100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000
$V_{CM} + 0.5 * V_{REF}$	$V_{CM} - 0.5 * V_{REF}$	1100 0000 0000
$V_{CM} + V_{REF}$	$V_{CM} - V_{REF}$	1111 1111 1111

Table 2. Input to Output Relationship—Single-Ended Input

V_{IN}^+	V_{IN}^-	Output
$V_{CM} - 2 * V_{REF}$	V_{CM}	0000 0000 0000
$V_{CM} - V_{REF}$	V_{CM}	0100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000
$V_{CM} + V_{REF}$	V_{CM}	1100 0000 0000
$V_{CM} + 2 * V_{REF}$	V_{CM}	1111 1111 1111

The output word rate is the same as the clock frequency, which may be in within the range indicated in the Electrical Tables. The analog input voltage is acquired at the rising edge of the clock and the digital data for that sample is delayed by the pipeline for 6 clock cycles.

A logic high on the power down (PD) pin reduces the converter power consumption to 50 mW.

Applications Information

OPERATING CONDITIONS

We recommend that the conditions in the Operating Table be observed for operation of the ADC12L080.

ANALOG INPUTS

The ADC12L080 has two analog signal inputs, V_{IN}+ and V_{IN}−, which form a differential input pair. There is one reference input pin, V_{REF}.

Reference Pins

The ADC12L080 can be used with the internal 1.0V reference or with an external reference. While designed and specified to operate with a 1.0V reference, the ADC12L080 performs well with reference voltages in the range of indicated in the Operating Ratings table. Lower reference voltages will decrease the signal-to-noise ratio (SNR) of the ADC12L080. Higher reference voltages (and input signal swing) will degrade THD performance for a full-scale input.

An input voltage below 2.0V at pin 1 (V_{REF}) is interpreted to be an external reference and is used as such. Connecting this pin to the analog supply (V_A) will force the use of the internal 1.0V reference.

It is very important that all grounds associated with the reference voltage and the input signal make connection to the analog ground plane at a single, quiet point to minimize the effects of noise currents in the ground path.

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The reference input pin serves two functions. When the input at this pin at or below 2V, this voltage is accepted as the reference for the converter. When this voltage is connected to V_A, then internal 1.0V reference is used. Functionality is undefined with voltages at this pin between 2V and V_A.

The three Reference Bypass Pins (V_{RP}, V_{RM} and V_{RN}) are made available for bypass purposes only. These pins should each be bypassed to ground with a 0.1 µF capacitor, and a 1.0 µF should be connected from V_{RP} to V_{RN}. Higher capacitances will result in a longer power down exit cycle. Lower capacitances may result in degraded dynamic performance. DO NOT LOAD these pins.

Signal Inputs

The signal inputs are V_{IN}+ and V_{IN}−. The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN}^{+}) - (V_{IN}^{-}) \quad (3)$$

Figure 36 shows the expected input signal range. Note that the nominal input common mode voltage, V_{CM}, is $V_A/2$ and the nominal input signals each run between the limits of AGND and V_{REF}. The Peaks of the input signals should never exceed the voltage described as

$$\text{Peak Input Voltage} = V_A - 0.5V \quad (4)$$

to maintain dynamic performance.

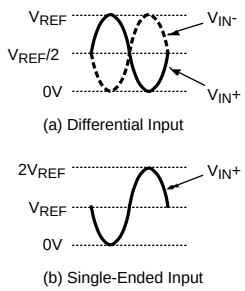

Figure 36. Expected Input Signal Range

The ADC12L080 performs best with a differential input, each of which should be centered around a common mode voltage, V_{CM}. The peak-to-peak voltage swing at both V_{IN}+ and V_{IN}− should not exceed the value of the reference voltage or the output data will be clipped. The two input signals should be exactly 180° out of phase from each other and of the same amplitude. For single frequency inputs, angular errors result in a reduction of the effective full scale input. For a complex waveform, however, angular errors will result in distortion.

The full scale error in LSB for a sine wave input can be described as approximately

$$E_{FS} = 4096 \, (1 - \sin (90° + \text{dev})) \quad (5)$$

Where dev is the angular difference between the two signals having a 180° relative phase relationship to each other (see Figure 37). Drive the analog inputs with a source impedance less than 100Ω.

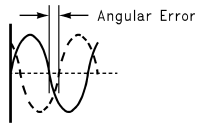

Figure 37. Angular Errors Between the Two Input Signals Will Reduce the Output Level or Cause Distortion

For differential operation, each analog input signal should have a peak-to-peak voltage equal to the input reference voltage, V_{REF}, and be centered around V_{CM}. For single-ended operation (which will result in reduced performance), one of the analog inputs should be connected to the d.c. common mode voltage of the driven input. The peak-to-peak differential input signal should be twice the reference voltage to maximize SNR and SINAD performance (Figure 36*b*). For example, set V_{REF} to 1.0V, bias V_{IN}− to 1.0V and drive V_{IN}+ with a signal range of 0V to 2.0V.

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Because very large input signal swings can degrade distortion performance, better performance with a single-ended input can be obtained by reducing the reference voltage while maintaining a full-range output. Table 1 and Table 2 indicate the input to output relationship of the ADC12L080.

The V_{IN}+ and the V_{IN}− inputs of the ADC12L080 consist of an analog switch followed by a switched-capacitor amplifier. The internal switching action at the analog inputs causes energy to be output from the input pins. As the driving source tries to compensate for this, it adds noise to the signal. To minimize this, use 33Ω series resistors at each of the signal inputs with a 51 pF capacitor to ground, as can be seen in Figure 39 and Figure 40. These components should be placed close to the ADC because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter the input. The 51 pF capacitor value is for Nyquist applications and should be replaced with a smaller capacitor for undersampling applications. The resulting pole should be at 1.7 to 2.0 times the highest input frequency. When determining this capacitor value, take into consideration the 8 pF ADC input capacitance.

Table 3 gives component values for Figure 39 to convert a signals to a range 1.0V ±0.5V at each of the differential input pins of the ADC12L080.

Table 3. Resistor values for Circuit of Figure 39

SIGNAL RANGE	R1	R2	R3	R4	R5, R6
0 - 0.25V	0Ω	open	200Ω	1780Ω	1000Ω
0 - 0.5V	0Ω	open	249Ω	1400Ω	499Ω
±0.5V	100Ω	1210Ω	100Ω	1210Ω	499Ω

DIGITAL INPUTS

Digital inputs consist of CLK, OF and PD. All digital inputs are 3V CMOS compatible.

CLK

The **CLK** signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the range indicated in the Electrical Table with rise and fall times of less than 2 ns. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°.

The **CLK** signal also drives an internal state machine. If the **CLK** is interrupted, or its frequency is too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the minimum sample rate.

The duty cycle of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC12L080 is designed to maintain performance over a range of duty cycles. While it is specified and performance is guaranteed with a 50% clock duty cycle, performance is typically maintained over a clock duty cycle range indicated in the Electrical Table.

The clock line should be terminated at its source in the characteristic impedance of that line. Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 for information on setting characteristic impedance.

It is highly desirable that the the source driving the ADC **CLK** pin only drive that pin. However, if that source is used to drive other things, each driven pin should be a.c. terminated with a series RC to ground, as shown in Figure 38, such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PD} \times L}{Z_o} \tag{6}$$

where t_{PD} is the signal propagation rate down the clock line, "L" is the line length and Z_O is the characteristic impedance of the clock line. This termination should be as close as possible to the ADC clock pin but beyond it as seen from the clock source. Typical t_{PD} is about 150 ps/inch (60 ps/cm) on FR-4 board material. The units of "L" and t_{PD} should be the same (inches or centimeters).

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OF

The OF pin is used to determine the digital data output format. When this pin is high, the output formant is two's complement. When this pin is low the output format is offset binary. Changing this pin while the device is operating will result in uncertainty of the data for a few conversion cycles.

PD

The PD pin, when high, holds the ADC12L080 in a power-down mode to conserve power when the converter is not being used. The power consumption in this state is 50 mW and is not affected by the clock frequency, or by whether there is a clock signal present. The output data pins are undefined and the data in the pipeline is corrupted while in the power down mode.

The Power Down Mode Exit Cycle time is determined by the value of the capacitors on pins 30, 31 and 32. These capacitors loose their charge in the Power Down mode and must be recharged by on-chip circuitry before conversions can be accurate. See Reference Pins.

OUTPUTS

The ADC12L080 has 12 TTL/CMOS compatible Data Output pins. The output data is present at these outputs while the PD pin is low. While the t_{OD} time provides information about output timing, a simple way to capture a valid output is to latch the data on the *rising edge* of the conversion clock (pin 10).

Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can cause on-chip noise and couple into the analog circuitry, degrading dynamic performance. Adequate bypassing, limiting output capacitance and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 15 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could be an apparent reduction in dynamic performance.

To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by connecting buffers between the ADC outputs and any other circuitry (74ACQ541, for example). Only one driven input should be connected to each output pin. Additionally, inserting series 100Ω resistors at the digital outputs, close to the ADC pins, will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. See Figure 38.

While the ADC12L080 will operate with V_{DR} voltages down to 1.8V, t_{OD} increases with reduced V_{DR}. Be careful of external timing when using reduced V_{DR}.

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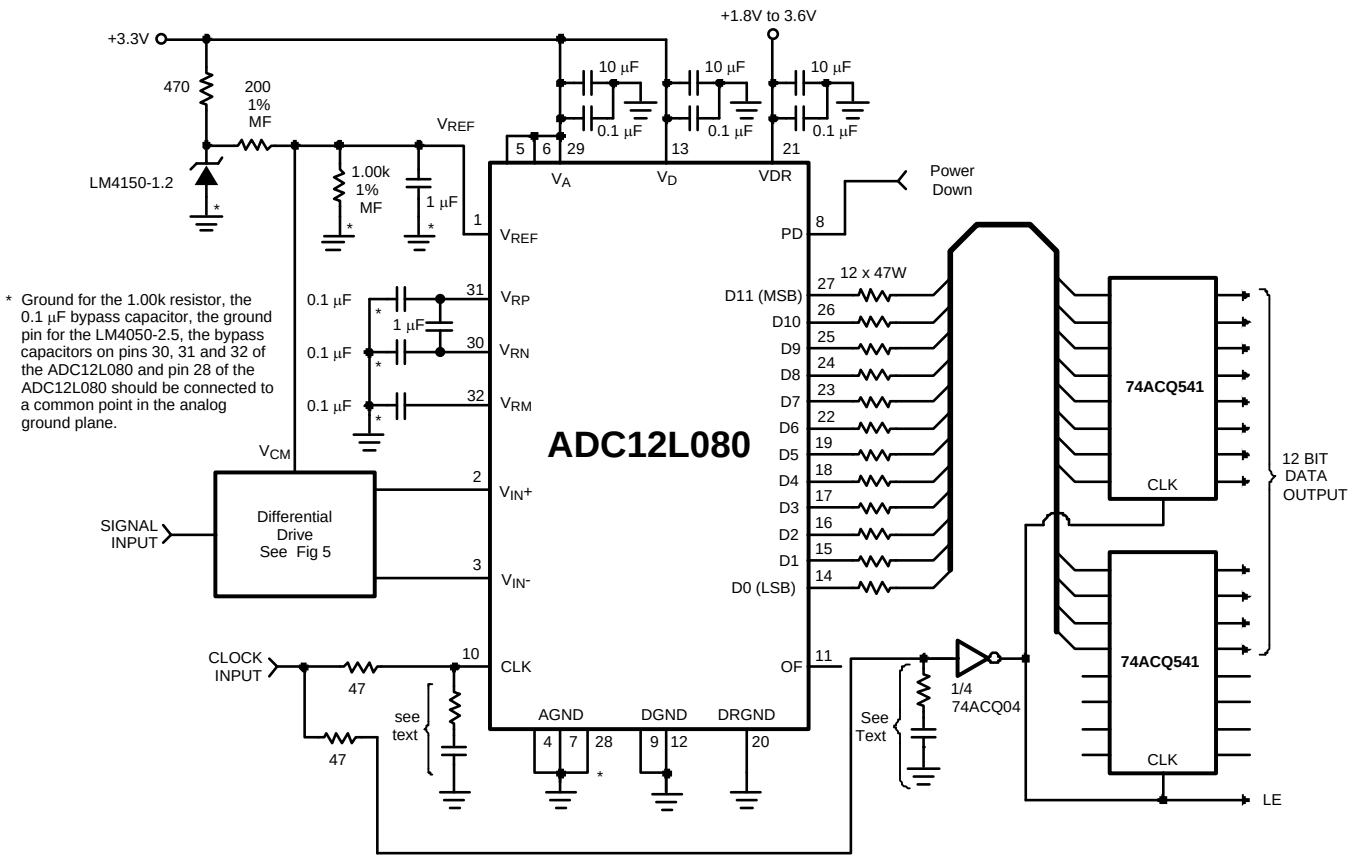

Figure 38. Simple Application Circuit with Single-Ended to Differential Buffer

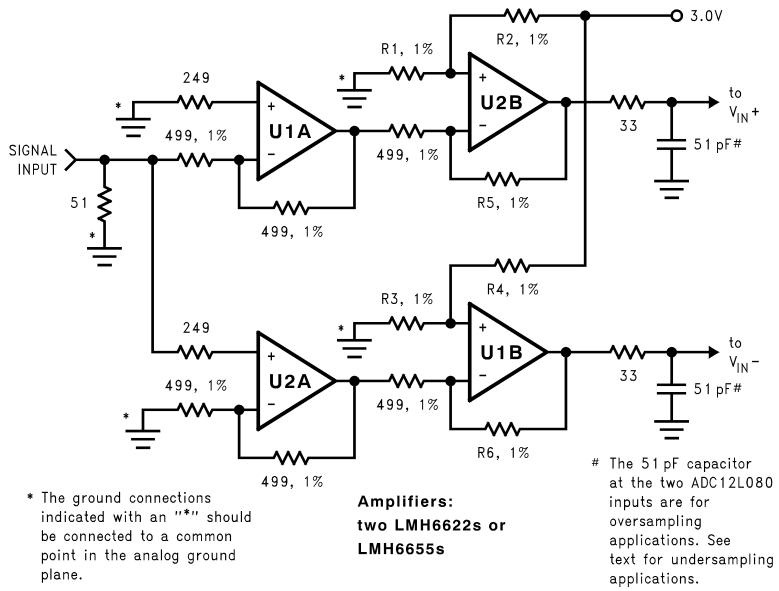

Figure 39. Differential Drive Circuit of Figure 38

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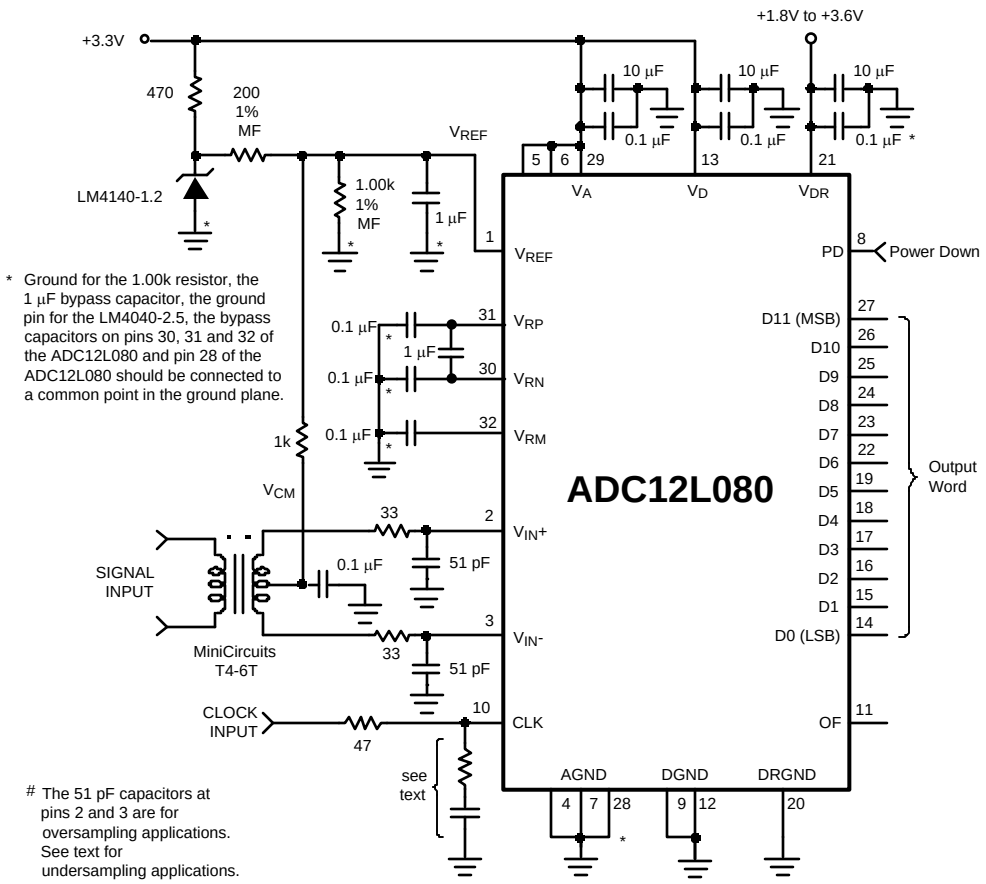

Figure 40. Driving the Signal Inputs with a Transformer

POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 10 µF capacitor and with a 0.1 µF low ESL ceramic chip capacitor within 3 millimeters of each power pin.

As is the case with all high-speed converters, the ADC12L080 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during turn on and turn off of power.

The V_{DR} pin provides power for the output drivers and may be operated from a supply in the range of 1.8V to V_D. This can simplify interfacing to devices and systems operating with supplies less than V_D. **DO NOT operate the V_{DR} pin at a voltage higher than V_D.**

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC12L080 between these areas, is required to achieve specified performance.

The ground return for the data outputs (DR GND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DR GND pins should NOT be connected to system ground in close proximity to any of the ADC12L080's other ground pins.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

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Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS, 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families.

The effects of the noise generated from the ADC output switching can be minimized through the use of 100Ω resistors in series with each data output line. Locate these resistors as close to the ADC output pins as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90° crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should *not* be placed side by side, even with just a small part of their bodies beside each other.

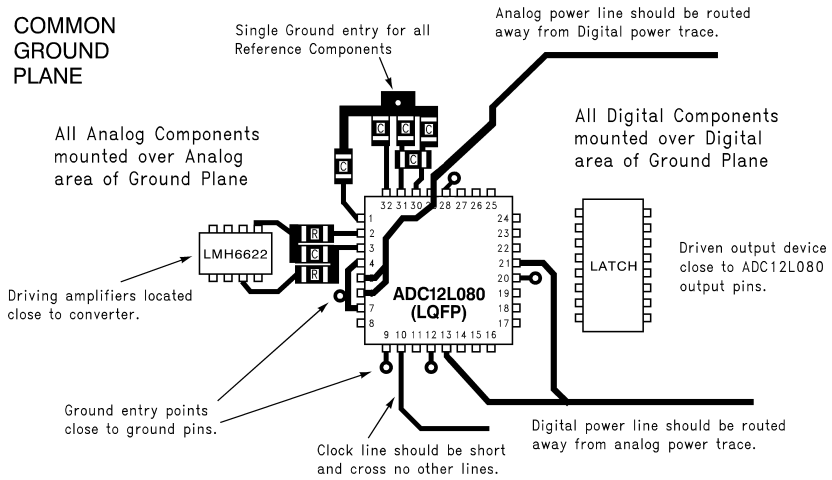

Figure 41. Example of a Suitable Layout

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

Figure 41 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and I/O lines should be placed in the digital area of the board. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single point. All ground connections should have a low inductance path to ground.

Best performance will be obtained with a single ground plane and separate analog and digital power planes. The power planes define analog and digital board areas of the board. Analog and digital components and signal lines should be kept within their own areas.

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DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must be free of jitter. The maximum allowable jitter to avoid the addition of noise to the conversion process is

$$\text{Max Jitter} = 1 / (2^{n+1} \times \pi \times f_{IN}) \quad (7)$$

Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in Figure 42. To avoid adding jitter to the clock signal, the elements of Figure 42 should be capable of toggling at a up to ten times the frequency used.

As mentioned in LAYOUT AND GROUNDING, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

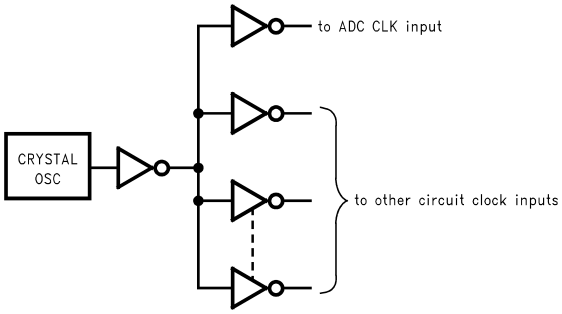

Figure 42. Isolating the ADC Clock from other Circuitry with a Clock Tree

COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 100 mV beyond the supply rails (more than 100 mV below the ground pins or 100 mV above the supply pins). Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital components (e.g., 74F and 74AC devices) to exhibit overshoot or undershoot that goes above the power supply or below ground. A resistor of about 50Ω to 100Ω in series with any offending digital input, close to the signal source, will eliminate the problem.

Do not allow input voltages to exceed the supply voltage, even on a transient basis. Not even during power up or power down.

Be careful not to overdrive the inputs of the ADC12L080 with a device that is powered from supplies outside the range of the ADC12L080 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can couple into the analog circuitry, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital areas on the PC board will reduce this problem.

Additionally, bus capacitance beyond the specified 15 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could, again, be an apparent reduction in dynamic performance.

The digital data outputs should be buffered (with 74ACQ541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC12L080, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 100Ω.

Using an inadequate amplifier to drive the analog input. As explained in Signal Inputs, the sampling input is difficult to drive without degrading dynamic performance.

If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. A small series resistor at each amplifier output and a capacitor at each of the ADC analog inputs to ground (as shown in Figure 39 and Figure 40) will improve performance. The LMH6702, LMH6628, LMH6622 and LMH6655 have been successfully used to drive the analog inputs of the ADC12L080.

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Also, it is important that the signals at the two inputs have exactly the same amplitude and be exactly 180º out of phase with each other. Board layout, including equality of the length of the two traces to the input pins, will affect the effective phase between these two signals. Remember that an operational amplifier operated in the non-inverting configuration will exhibit more time delay than will the same device operating in the inverting configuration.

Operating with the reference pins outside of the specified range. As mentioned in Reference Pins, V_{REF} should be in the range specified in the Operating Ratings table. Operating outside of these limits could lead to performance degradation.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR and SINAD performance.

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REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	26

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC12L080CIVY/NOPB	Active	Production	LQFP (NEY) | 32	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12L0 80CIVY
ADC12L080CIVY/NOPB.A	Active	Production	LQFP (NEY) | 32	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12L0 80CIVY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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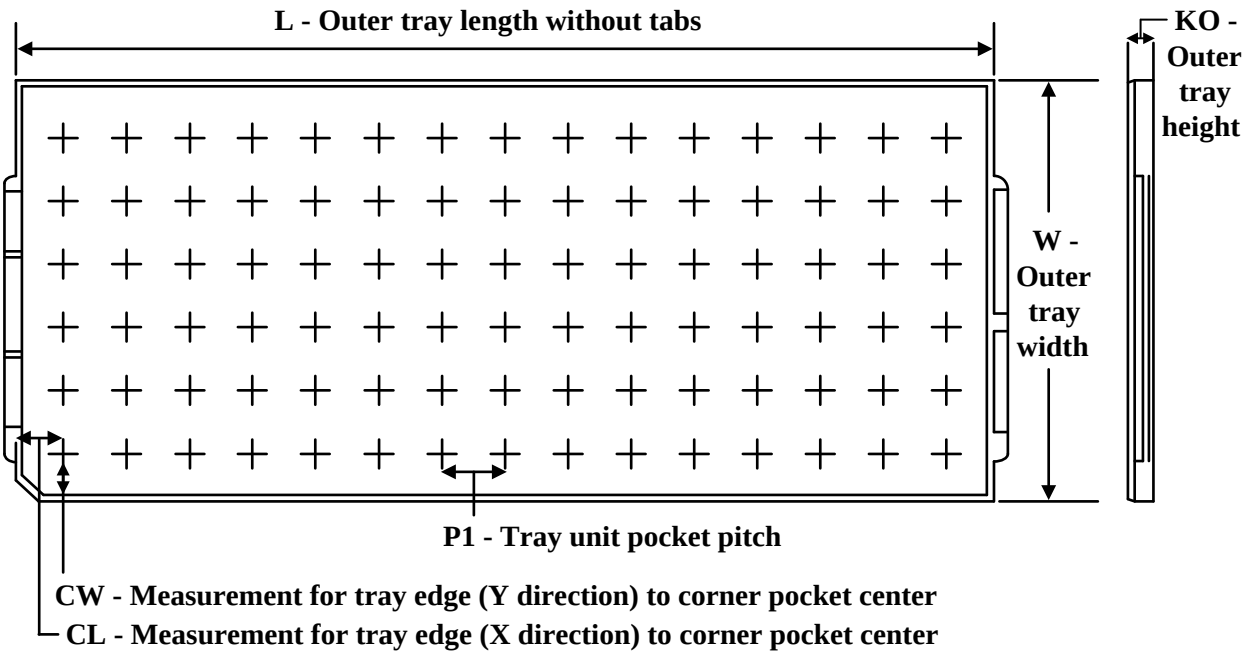
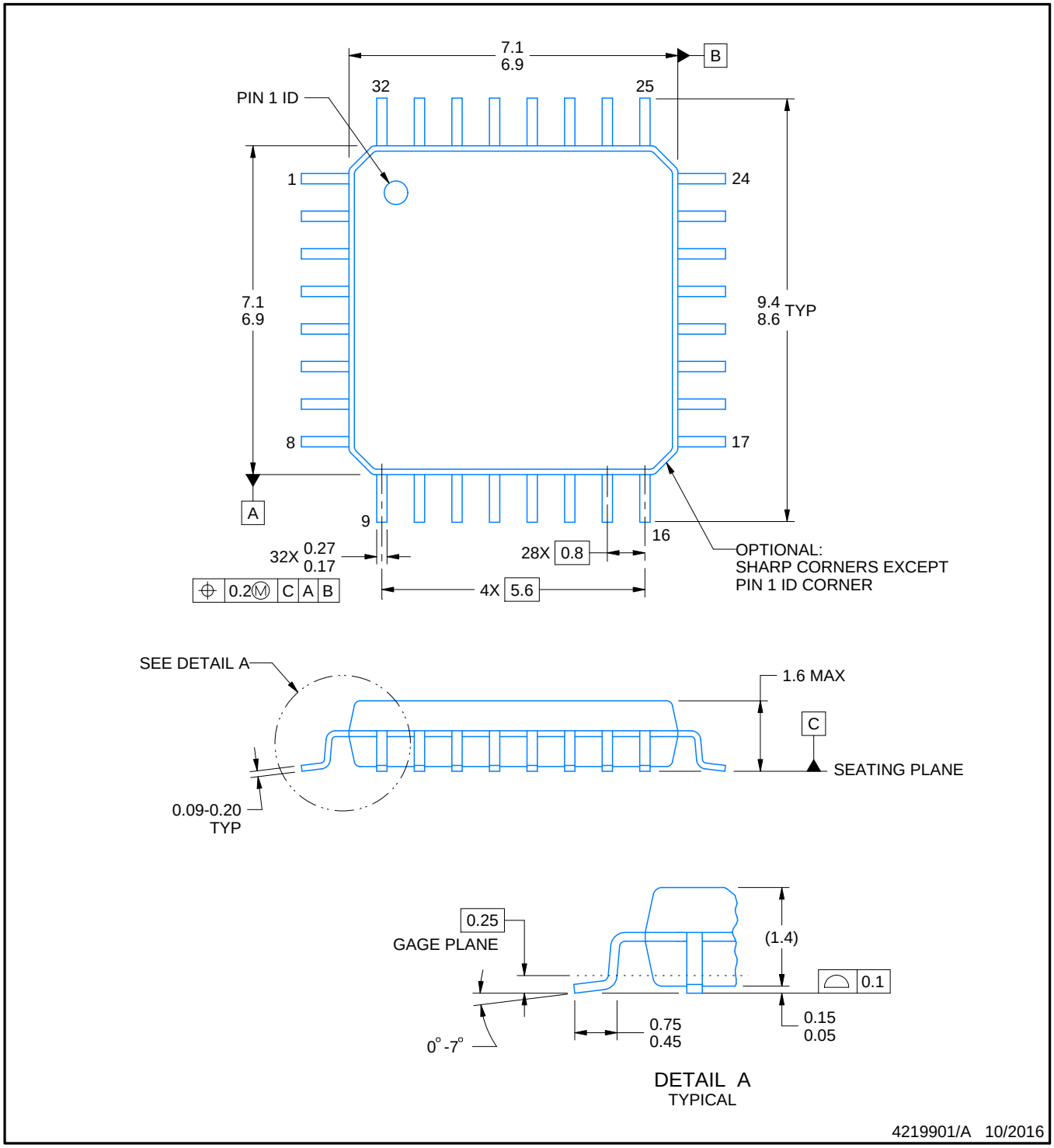
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

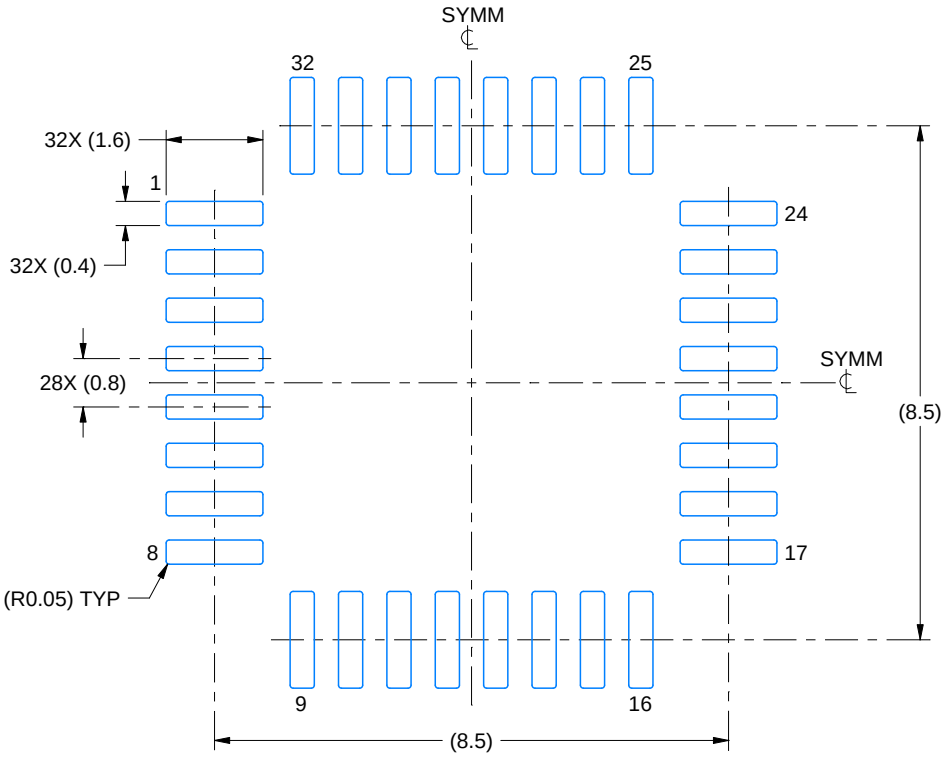
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADC12L080CIVY/NOPB	NEY	LQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
ADC12L080CIVY/ NOPB.A	NEY	LQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

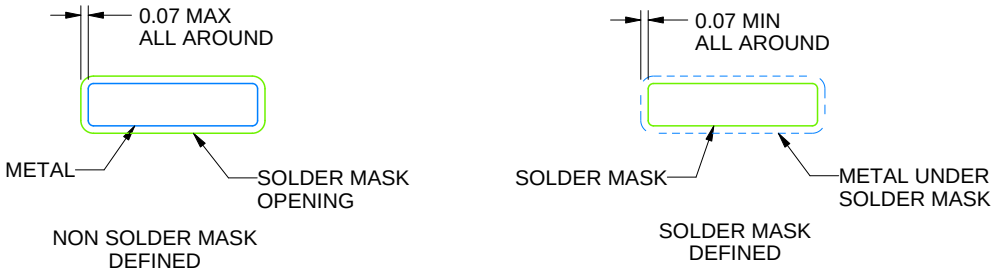


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
SCALE:8X

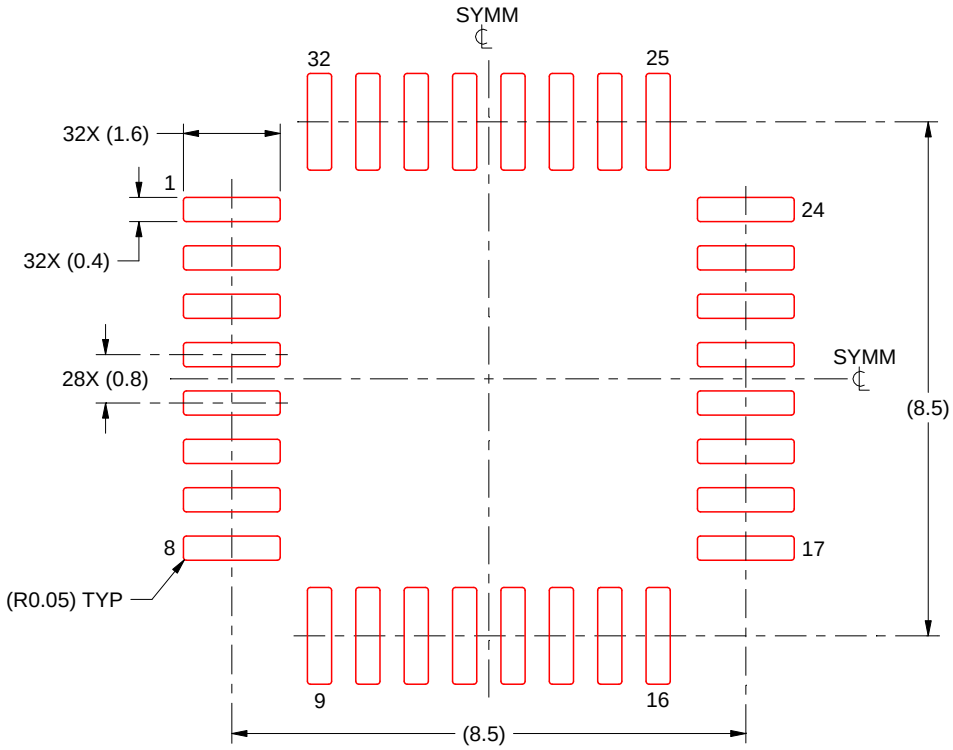


SOLDER MASK DETAILS

4219901/A 10/2016

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE 8X

4219901/A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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