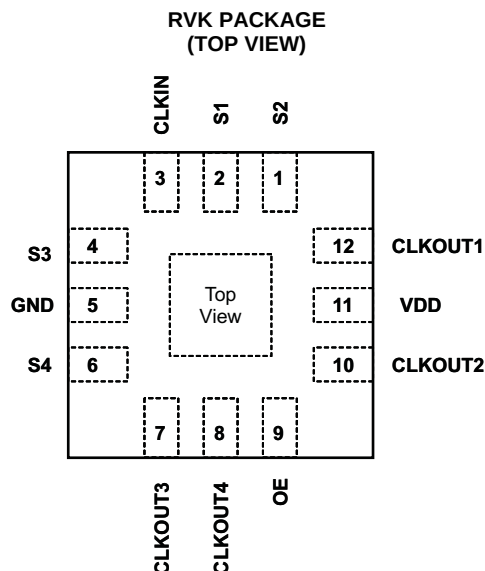


1 to 4 Configurable Clock Buffer for 3D Displays

Check for Samples: [CDC1104](#)

FEATURES

- **Input Reference Clock 120Hz–240Hz**
- **Output Clock (Fin/2) 60Hz–120Hz**
- **Output Buffer Drive Strength: 8mA**
- **4 Clock Outputs**
- **4 Control Pins Select Phases of Clock Outputs**
- **Supply Voltage: 3.8V–5.5V**
- **Operating Temperature Range: –40°C to 85°C**
- **ESD Protection Exceeds JESD 22**
 - **2000-V Human-Body Model (A114-B)**
 - **500-V Charged-Device Model (C101)**
- **Package Offerings**
 - **12-pin QFN (3mm x 3mm)**



DESCRIPTION

The CDC1104 is a 1 to 4 configurable clock buffer. The device accepts an input reference clock and creates 4 buffered output clocks with an output frequency equal to one half the input clock frequency. Four control inputs, S1, S2, S3, S4 configurable phases of the clock outputs.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	RVK	Tape and reel	CDC1104RVKR	ZT

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN FUNCTIONS

NO.	NAME	TYPE ⁽¹⁾	DESCRIPTION
1	S2	I	Output clock select. Refer to Output Clock Selection Table
2	S1	I	Output clock select. Refer to Output Clock Selection Table
3	CLKIN	I	Clock Input
4	S3	I	Output clock select. Refer to Output Clock Selection Table
5	GND	P	Ground
6	S4	I	Not internally connected
7	CLKOUT3	O	Buffered CLK Output. Refer to Output Clock Selection Table
8	CLKOUT4	O	Buffered CLK Output. Refer to Output Clock Selection Table
9	OE	I	Chip Enable
10	CLKOUT2	O	Buffered CLK Output. Refer to Output Clock Selection Table
11	VDD	P	Inverted output. No counter delay
12	CLKOUT1	O	Buffered CLK Output. Refer to Output Clock Selection Table

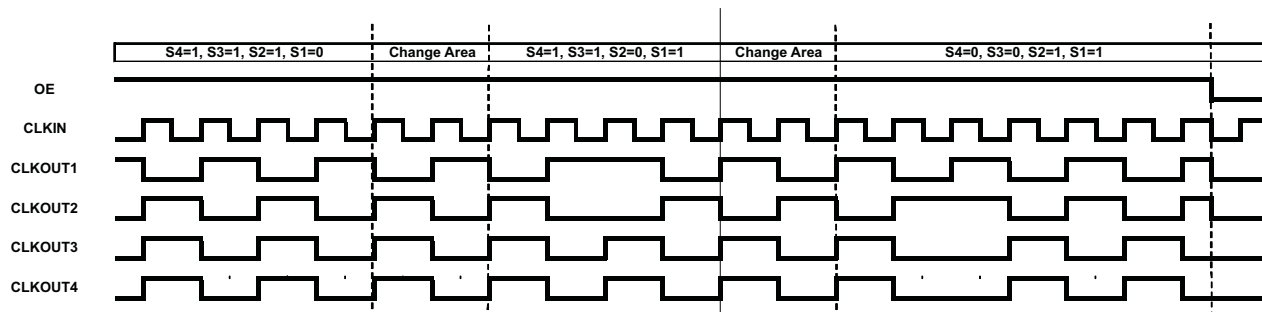
(1) G = Ground, I = Input, O = Output, P = Power

TRUTH TABLE

INPUTS						OUTPUTS			
OE	CLKIN	S4	S3	S2	S1	CLKOUT4	CLKOUT3	CLKOUT2	CLKOUT1
0	CLK	X	X	X	X	L	L	L	L
1	CLK	0	0	0	0	L	L	L	L
1	CLK	0	0	0	1	CLK\	CLK\	CLK\	CLK
1	CLK	0	0	1	0	CLK\	CLK\	CLK	CLK\
1	CLK	0	0	1	1	CLK\	CLK\	CLK	CLK
1	CLK	0	1	0	0	CLK\	CLK	CLK\	CLK\
1	CLK	0	1	0	1	CLK\	CLK	CLK\	CLK
1	CLK	0	1	1	0	CLK\	CLK	CLK	CLK\
1	CLK	0	1	1	1	CLK\	CLK	CLK	CLK
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1	CLK	1	0	0	1	CLK	CLK\	CLK\	CLK
1	CLK	1	0	1	0	CLK	CLK\	CLK	CLK\
1	CLK	1	0	1	1	CLK	CLK\	CLK	CLK
1	CLK	1	1	0	0	CLK	CLK	CLK\	CLK\
1	CLK	1	1	0	1	CLK	CLK	CLK\	CLK
1	CLK	1	1	1	0	CLK	CLK	CLK	CLK\
1	CLK	1	1	1	1	CLK	CLK	CLK	CLK

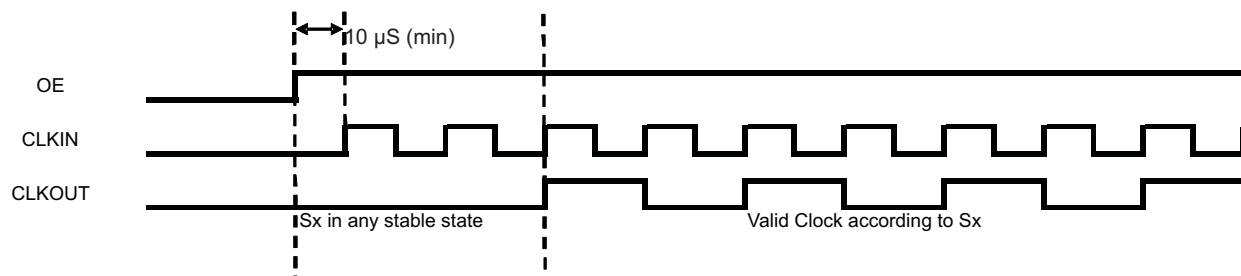
Timing Diagram For Glitch Free Operation

Transition of outputs from any state to any other state



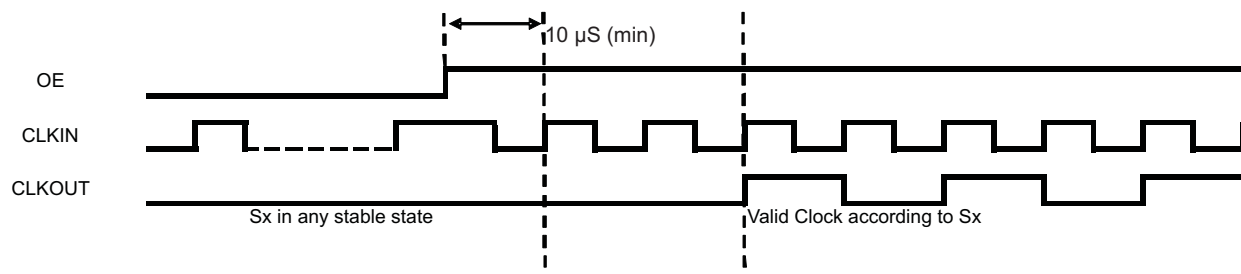
NOTE: Transition to new state will happen after a latency of one output clock cycle after completing the present output clock cycle. Transition to new state will happen after a latency of up to 3 input clock cycles excluding the input cycle where the transition has occurred.

Power Up



NOTE: Transition to new state will happen after a latency of 2 input clock cycles excluding the input cycle where the transition has occurred.

OE Operation



NOTE: Transition to new state will happen after a latency of 2 input clock cycles excluding the input cycle where the transition has occurred.

CDC1104

SCAS921 – SEPTEMBER 2011

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.3	6	V
V _I	Input voltage range ⁽²⁾	–0.3	6	V
V _O	Output voltage range in the high or low state ⁽²⁾	–0.3	6	V
I _{IK}	Input clamp current	V _I < 0		±20 mA
I _{OK}	Output clamp current	V _O < 0		±20 mA
I _{OL}	Continuous output Low current	V _O = 0 to V _{CC}		±20 mA
I _{OH}	Continuous output High current	V _O = 0 to V _{CC}		±20 mA
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
θ _{JA}	Package thermal impedance ⁽¹⁾ RVK Package	72.2	°C/W

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	3.8	5.5	V
V _{IH}	High-Level Input Voltage	1.6	5.5	V
V _{IL}	Low-Level Input Voltage	0	0.8	V
I _{IH}	High-level input current		1	μA
I _{IL}	Low-level input current		1	μA
V _I		0	5.5	V
V _O		0	V _{CC}	V
I _{OH}	High-level output current		–8	mA
I _{OL}	Low-level output current		8	mA
T _A	Operating free-air temperature	–40	85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = –40°C to 85°C			UNIT
			MIN	TYP	MAX	
V _{OH}	I _{OH} = –8 mA	3.8 V	V _{CC} –0.6			V
		5 V	V _{CC} –0.4			V
V _{OL}	I _{OL} = 8 mA	3.8 V	0.40			V
		5 V	0.40			V
I _I (CLKIN, OE, Sx)	V _I = GND to 4 V	5.5 V	1			μA
I _{CC} (Disabled)	V _{IO} = 0 V or 5.5V, OE = Low	3.8 V to 5.5 V	0.5			2 μA
I _{DD} (Dynamic)	OE = 5.5 V; Sx = 0 V, 5.5 V; CLKIN = 0 V, 5.5 V	5.5 V	20			50 μA
	OE = 3.0 V; Sx = 0 V, 3.0 V; CLKIN = 0 V, 3.0 V	5.5 V	20			50 μA
	OE = 1.6 V; Sx = 0 V, 1.6 V; CLKIN = 0 V, 1.6 V	5.5 V	20			50 μA
C _I (CLKIN, OE, Sx)	V _I = V _{CC} or GND		7			pF

SWITCHING CHARACTERISTICS

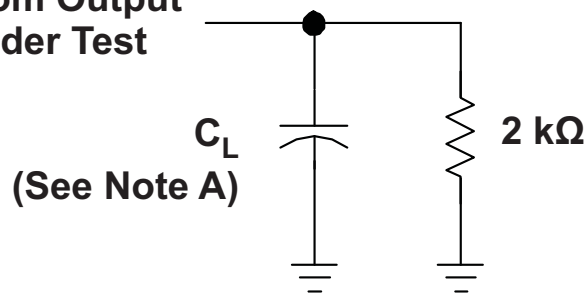
over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT) TO(OUTPUT) V _{CC}	T _A = –40°C to 85°C			UNIT
		MIN	TYP	MAX	
F _{CLKIN}	Input clock frequency	120		240	Hz
F _{CLKOUT}	Output clock frequency	F _{CLKIN} /2		F _{CLKIN} /2	Hz
t _{RISE} / t _{FALL}	Output rise/fall time			10	μs
t _{RISE} / t _{FALL}	Input rise/fall time			50	μs
Input Duty Cycle	Input duty cycle	49%	50%	51%	
Output Duty Cycle	Output duty cycle	49%	50%	5%1	
t _{SU}	Setup time on Sx	60			μs
t _H	Hold time on Sx	60			μs
t _{SKEW}	CLKOUTx skew			10	μs

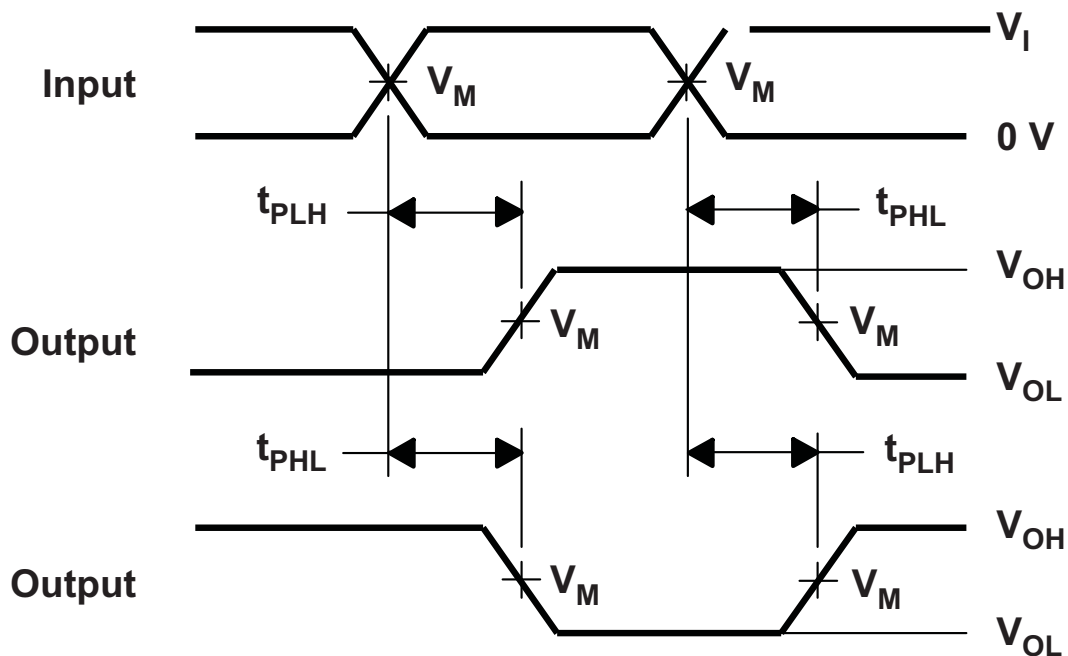
PARAMETER MEASUREMENT INFORMATION

Propagation Delays

From Output Under Test



	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L V_M V_I	15 pF $V_{CC}/2$ V_{CC}



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NON INVERTING OUTPUTS

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, for propagation delays $t_r/t_f = 3\text{ ns}$, for setup and hold times and pulse width $t_r/t_f = 1.2\text{ ns}$.
- The outputs are measured on at a time, with on transition per measurement.
- t_{PLH} and t_{PHL} are the same a t_{pd} .
- All parameters and waveforms are no applicable to all devices.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC1104RVKR	Active	Production	WQFN (RVK) 12	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTH
CDC1104RVKR.B	Active	Production	WQFN (RVK) 12	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTH

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

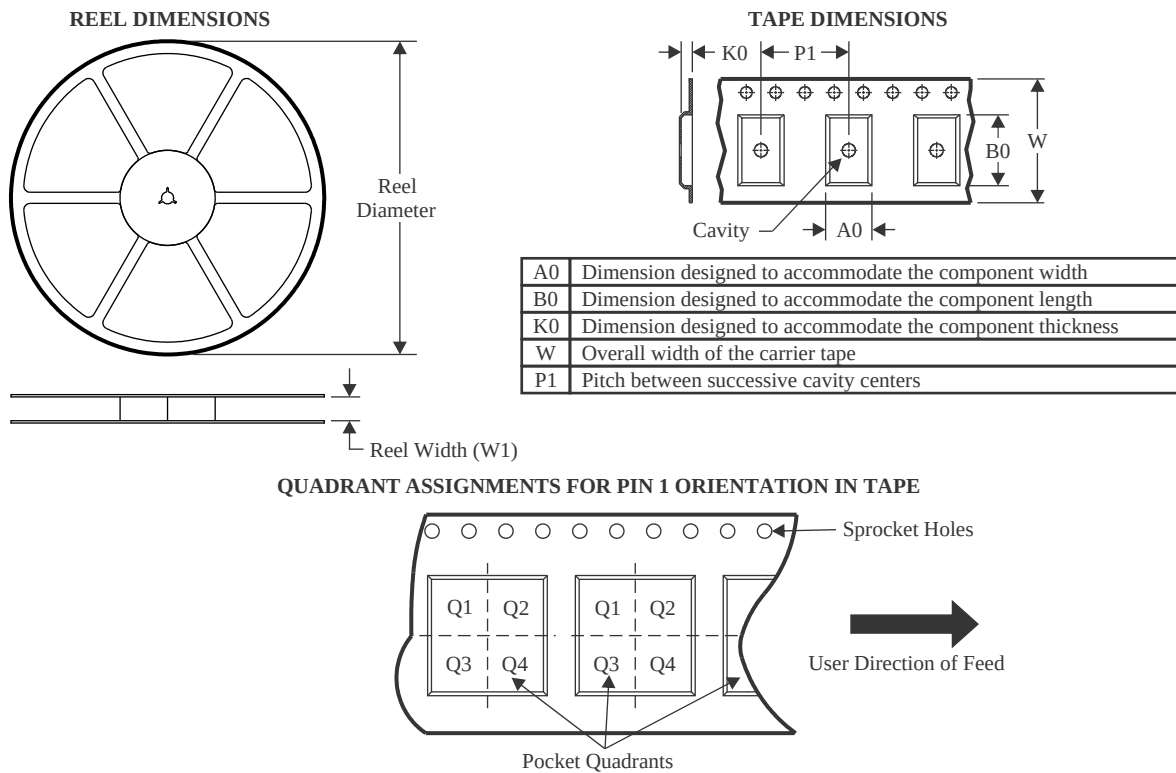
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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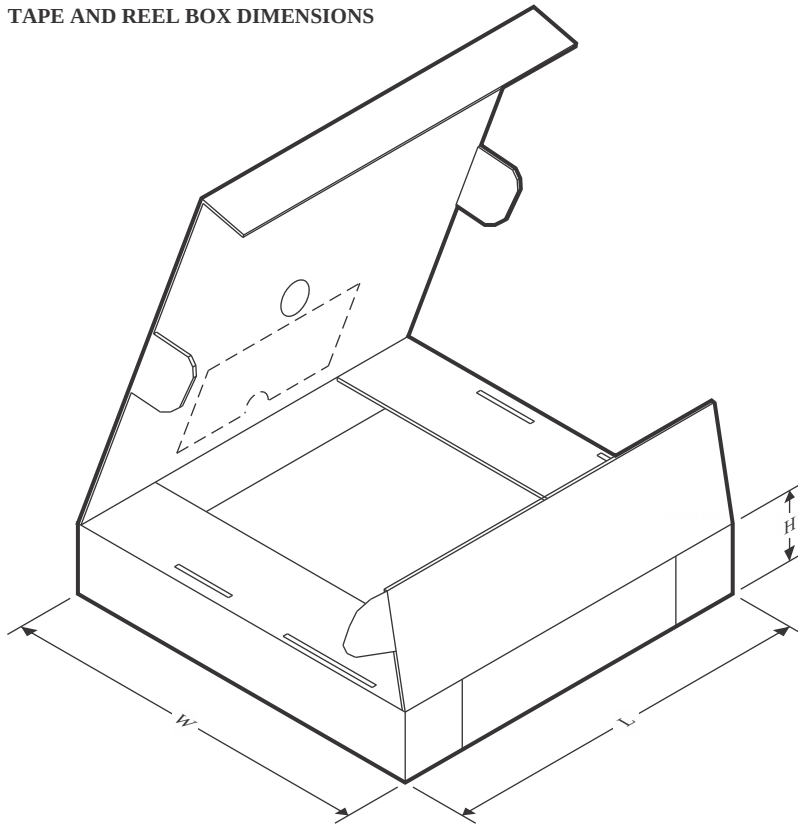
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC1104RVKR	WQFN	RVK	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

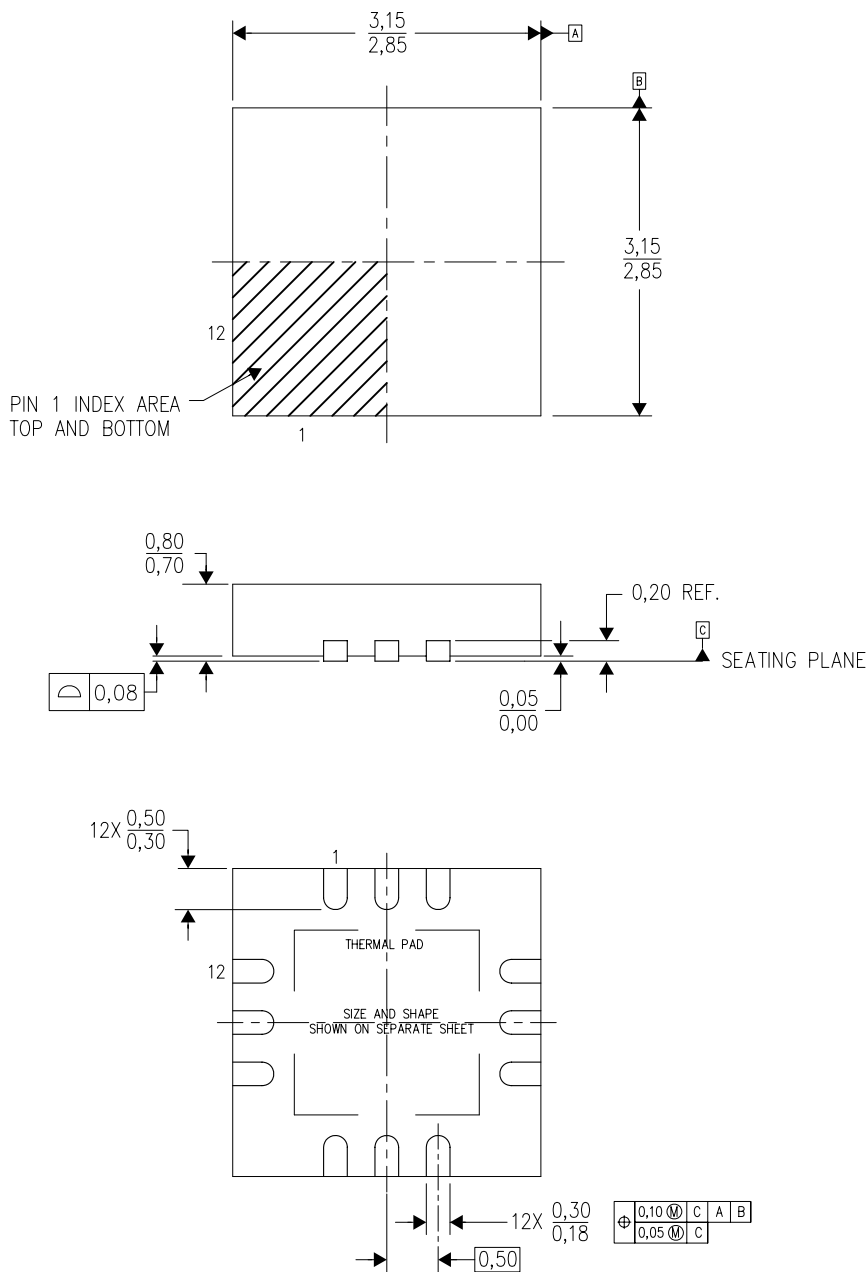


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC1104RVKR	WQFN	RVK	12	3000	346.0	346.0	33.0

RVK (S-PWQFN-N12)

PLASTIC QUAD FLATPACK NO-LEAD



4211889/B 10/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

RVK (S-PWQFN-N12)

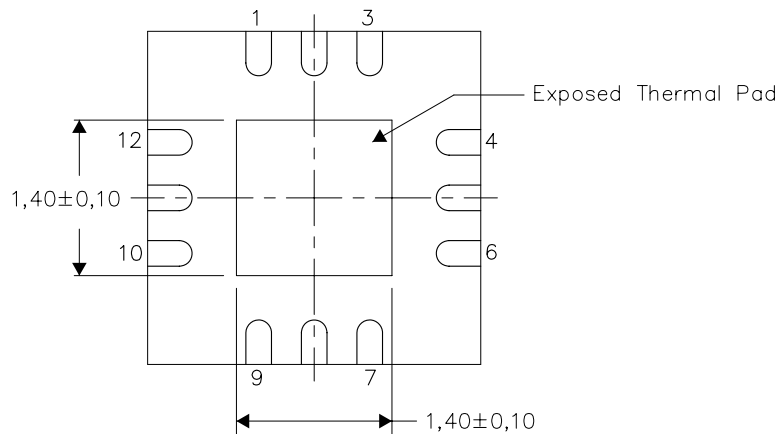
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4211891/A 06/11

NOTE: All linear dimensions are in millimeters

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