

## Dual FET Bus Switch 2.5-V/3.3-V Low-Voltage High-Bandwidth Bus Switch

Check for Samples: [SN74CB3Q3306A](#)

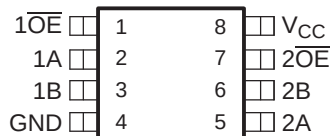
### FEATURES

- High-Bandwidth Data Path (up to 500 MHz<sup>(1)</sup>)
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance ( $r_{on}$ ) Characteristics Over Operating Range ( $r_{on} = 4\ \Omega$  Typ)
- Rail-to-Rail Switching on Data I/O Ports
  - 0- to 5-V Switching With 3.3-V  $V_{CC}$
  - 0- to 3.3-V Switching With 2.5-V  $V_{CC}$
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{io(OFF)} = 3.5\text{ pF}$  Typ)
- Fast Switching Frequency ( $f_{OE} = 20\text{ MHz}$  Max)

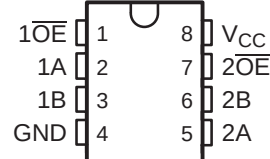
<sup>(1)</sup> For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number [SCDA008](#).

- Data and Control Inputs Provide Undershoot Clamp Diodes
  - Low Power Consumption ( $I_{CC} = 0.25\text{ mA}$  Typ)
  - $V_{CC}$  Operating Range From 2.3 V to 3.6 V
  - Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
  - Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
  - $I_{off}$  Supports Partial-Power-Down Mode Operation
  - Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
  - ESD Performance Tested Per JESD 22
    - 2000-V Human-Body Model (A114-B, Class II)
    - 1000-V Charged-Device Model (C101)
  - Supports Both Digital and Analog
- Applications:** USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating

DCU PACKAGE  
(TOP VIEW)



PW PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING    |
|---------------|------------------------|---------------|-----------------------|---------------------|
| –40°C to 85°C | TSSOP – PW             | Tube          | SN74CB3Q3306APW       | BU306A              |
|               |                        | Tape and reel | SN74CB3Q3306APWR      |                     |
|               | US8-DCU                | Tape and reel | SN74CB3Q3306ADCUR     | GA6R <sup>(2)</sup> |
|               |                        |               | 74CB3Q3306ADCURE4     |                     |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) The last character designates assembly/test site.



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# SN74CB3Q3306A

SCDS113E – DECEMBER 2002 – REVISED JANUARY 2011

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION/ORDERING INFORMATION

The SN74CB3Q3306A is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ( $r_{on}$ ). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3306A provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3306A is organized as two 1-bit switches with separate output-enable ( $\overline{1OE}$ ,  $\overline{2OE}$ ) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When  $\overline{OE}$  is low, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

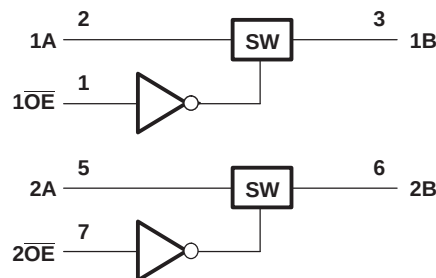
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

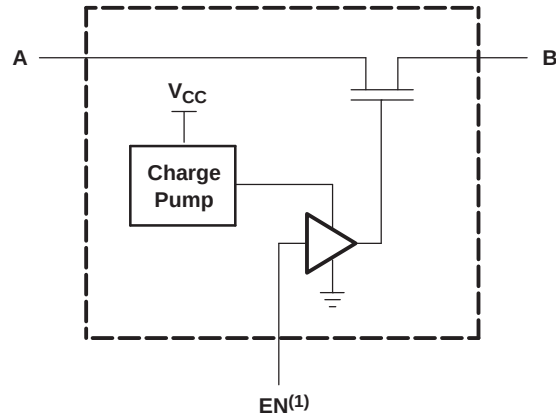
**Table 1. FUNCTION TABLE  
(EACH BUS SWITCH)**

| INPUT<br>$\overline{OE}$ | INPUT/OUTPUT<br>A | FUNCTION        |
|--------------------------|-------------------|-----------------|
| L                        | B                 | A port = B port |
| H                        | Z                 | Disconnect      |

## LOGIC DIAGRAM (POSITIVE LOGIC)



### SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

| Operating free air temperature range (unless otherwise noted) |                                                        |                      | MIN  | MAX  | UNIT |
|---------------------------------------------------------------|--------------------------------------------------------|----------------------|------|------|------|
| V <sub>CC</sub>                                               | Supply voltage range                                   |                      | −0.5 | 4.6  | V    |
| V <sub>IN</sub>                                               | Control input voltage range <sup>(2) (3)</sup>         |                      | −0.5 | 7    | V    |
| V <sub>I/O</sub>                                              | Switch I/O voltage range <sup>(2) (3) (4)</sup>        |                      | −0.5 | 7    | V    |
| I <sub>IK</sub>                                               | Control input clamp current                            | V <sub>IN</sub> < 0  |      | −50  | mA   |
| I <sub>I/OK</sub>                                             | I/O port clamp current                                 | V <sub>I/O</sub> < 0 |      | −50  | mA   |
| I <sub>I/O</sub>                                              | ON-state switch current <sup>(5)</sup>                 |                      |      | ±64  | mA   |
|                                                               | Continuous current through each V <sub>CC</sub> or GND |                      |      | ±100 | mA   |
| θ <sub>JA</sub>                                               | Package thermal impedance <sup>(6)</sup>               | DCU                  |      | TBD  | °C/W |
|                                                               |                                                        | PW                   |      | 88   |      |
| T <sub>stg</sub>                                              | Storage temperature range                              |                      | −65  | 150  | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
- (5)  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

### RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

|                  |                                  |                                  | MIN | MAX | UNIT |
|------------------|----------------------------------|----------------------------------|-----|-----|------|
| V <sub>CC</sub>  | Supply voltage                   |                                  | 2.3 | 3.6 | V    |
| V <sub>IH</sub>  | High-level control input voltage | V <sub>CC</sub> = 2.3 V to 2.7 V | 1.7 | 5.5 | V    |
|                  |                                  | V <sub>CC</sub> = 2.7 V to 3.6 V | 2   | 5.5 |      |
| V <sub>IL</sub>  | Low-level control input voltage  | V <sub>CC</sub> = 2.3 V to 2.7 V | 0   | 0.7 | V    |
|                  |                                  | V <sub>CC</sub> = 2.7 V to 3.6 V | 0   | 0.8 |      |
| V <sub>I/O</sub> | Data input/output voltage        |                                  | 0   | 5.5 | V    |
| T <sub>A</sub>   | Operating free-air temperature   |                                  | −40 | 85  | °C   |

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74CB3Q3306A

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## ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                      |                   | TEST CONDITIONS                                                                                                                     |                                                 | MIN | TYP <sup>(2)</sup> | MAX  | UNIT   |
|--------------------------------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------|-----|--------------------|------|--------|
| $V_{IK}$                       |                   | $V_{CC} = 3.6\text{ V}$ ,<br>$I_I = -18\text{ mA}$                                                                                  |                                                 |     |                    | -1.8 | V      |
| $I_{IN}$                       | Control inputs    | $V_{CC} = 3.6\text{ V}$ ,<br>$V_{IN} = 0\text{ to }5.5\text{ V}$                                                                    |                                                 |     |                    | ±1   | μA     |
| $I_{OZ}$ <sup>(3)</sup>        |                   | $V_{CC} = 3.6\text{ V}$ ,<br>$V_O = 0\text{ to }5.5\text{ V}$ ,<br>$V_I = 0$ ,<br>Switch OFF,<br>$V_{IN} = V_{CC}\text{ or GND}$    |                                                 |     |                    | ±1   | μA     |
| $I_{off}$                      |                   | $V_{CC} = 0$ ,<br>$V_O = 0\text{ to }5.5\text{ V}$ ,<br>$V_I = 0$                                                                   |                                                 |     |                    | 1    | μA     |
| $I_{CC}$                       |                   | $V_{CC} = 3.6\text{ V}$ ,<br>$I_{IO} = 0$ ,<br>Switch ON or OFF,<br>$V_{IN} = V_{CC}\text{ or GND}$                                 |                                                 |     | 0.25               | 0.7  | mA     |
| $\Delta I_{CC}$ <sup>(4)</sup> | Control inputs    | $V_{CC} = 3.6\text{ V}$ ,<br>One input at 3 V,<br>Other inputs at $V_{CC}\text{ or GND}$                                            |                                                 |     |                    | 25   | μA     |
| $I_{CCD}$ <sup>(5)</sup>       | Per control input | $V_{CC} = 3.6\text{ V}$ ,<br>A and B ports open,<br>Control input switching at 50% duty cycle                                       |                                                 |     | 0.03               | 0.1  | mA/MHz |
| $C_{in}$                       | Control inputs    | $V_{CC} = 3.3\text{ V}$ ,<br>$V_{IN} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$                                                     |                                                 |     | 2.5                | 3.5  | pF     |
| $C_{io(OFF)}$                  |                   | $V_{CC} = 3.3\text{ V}$ ,<br>Switch OFF,<br>$V_{IN} = V_{CC}\text{ or GND}$ ,<br>$V_{IO} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$ |                                                 |     | 3.5                | 5    | pF     |
| $C_{io(ON)}$                   |                   | $V_{CC} = 3.3\text{ V}$ ,<br>Switch ON,<br>$V_{IN} = V_{CC}\text{ or GND}$ ,<br>$V_{IO} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$  |                                                 |     | 8                  | 10.5 | pF     |
| $r_{on}$ <sup>(6)</sup>        |                   | $V_{CC} = 2.3\text{ V}$ ,<br>TYP at $V_{CC} = 2.5\text{ V}$                                                                         | $V_I = 0$ ,<br>$I_O = 30\text{ mA}$             |     | 4                  | 8    | Ω      |
|                                |                   |                                                                                                                                     | $V_I = 1.7\text{ V}$ ,<br>$I_O = -15\text{ mA}$ |     | 5                  | 9    |        |
|                                |                   | $V_{CC} = 3\text{ V}$                                                                                                               | $V_I = 0$ ,<br>$I_O = 30\text{ mA}$             |     | 4                  | 6    |        |
|                                |                   |                                                                                                                                     | $V_I = 2.4\text{ V}$ ,<br>$I_O = -15\text{ mA}$ |     | 5                  | 8    |        |

(1)  $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see [Figure 2](#)).

(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| PARAMETER               | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 2.5\text{ V}$<br>$\pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V}$<br>$\pm 0.3\text{ V}$ |     | UNIT |
|-------------------------|-----------------|----------------|-----------------------------------------------|-----|-----------------------------------------------|-----|------|
|                         |                 |                | MIN                                           | MAX | MIN                                           | MAX |      |
| $f_{OE}$ <sup>(1)</sup> | $\overline{OE}$ | A or B         |                                               | 10  |                                               | 20  | MHz  |
| $t_{pd}$ <sup>(2)</sup> | A or B          | B or A         |                                               | 0.2 |                                               | 0.2 | ns   |
| $t_{en}$                | $\overline{OE}$ | A or B         | 1.5                                           | 6.5 | 1.5                                           | 5.5 | ns   |
| $t_{dis}$               | $\overline{OE}$ | A or B         | 1                                             | 6   | 1                                             | 5   | ns   |

(1) Maximum switching frequency for control input ( $V_O > V_{CC}$ ,  $V_I = 5\text{ V}$ ,  $R_L \geq 1\text{ M}\Omega$ ,  $C_L = 0$ )

(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

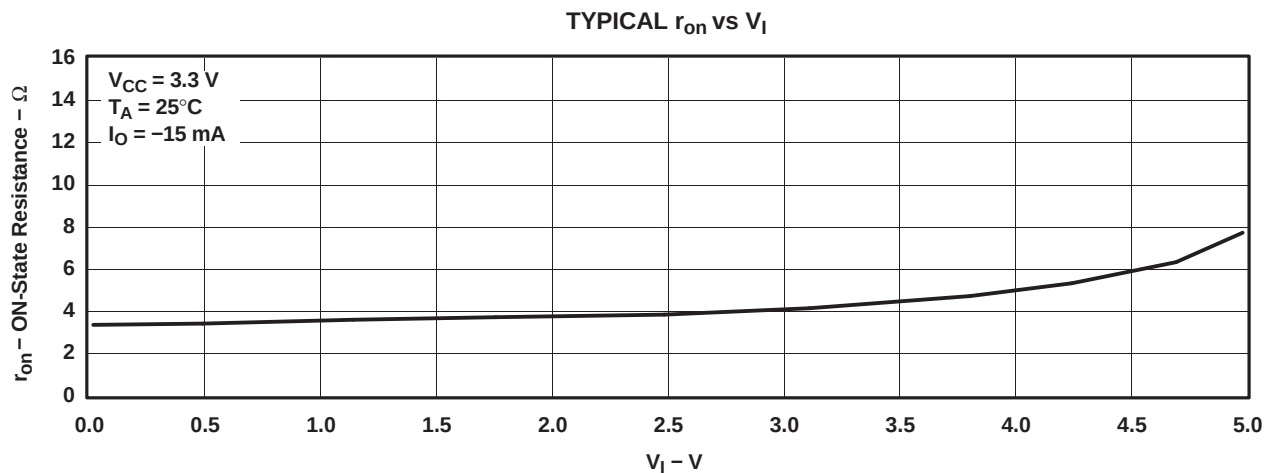


**Figure 1. Typical  $r_{on}$  vs  $V_I$**

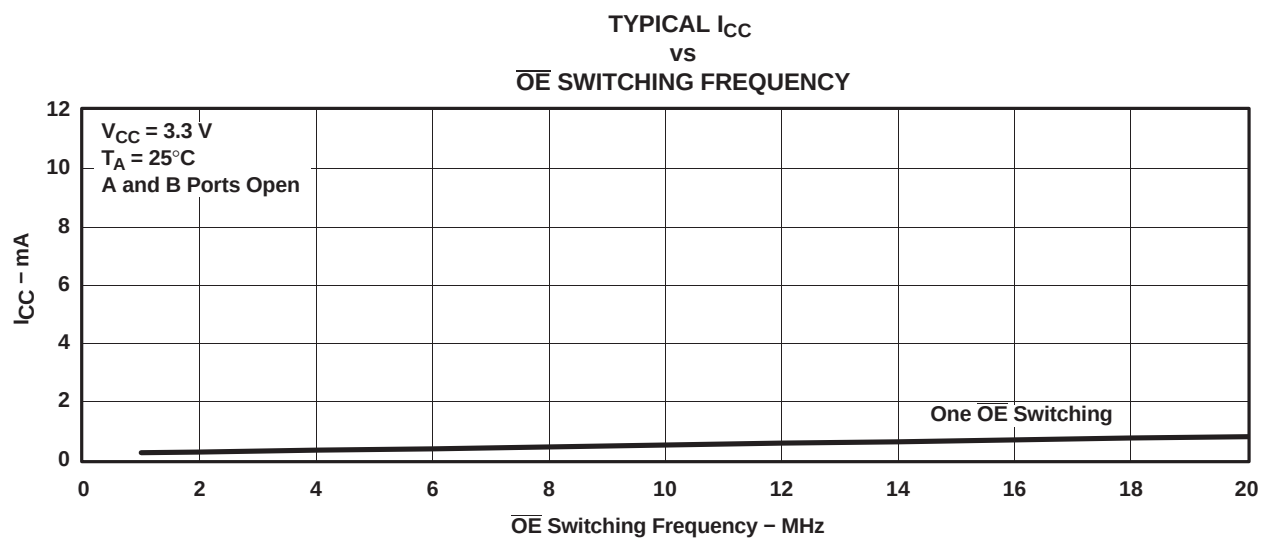
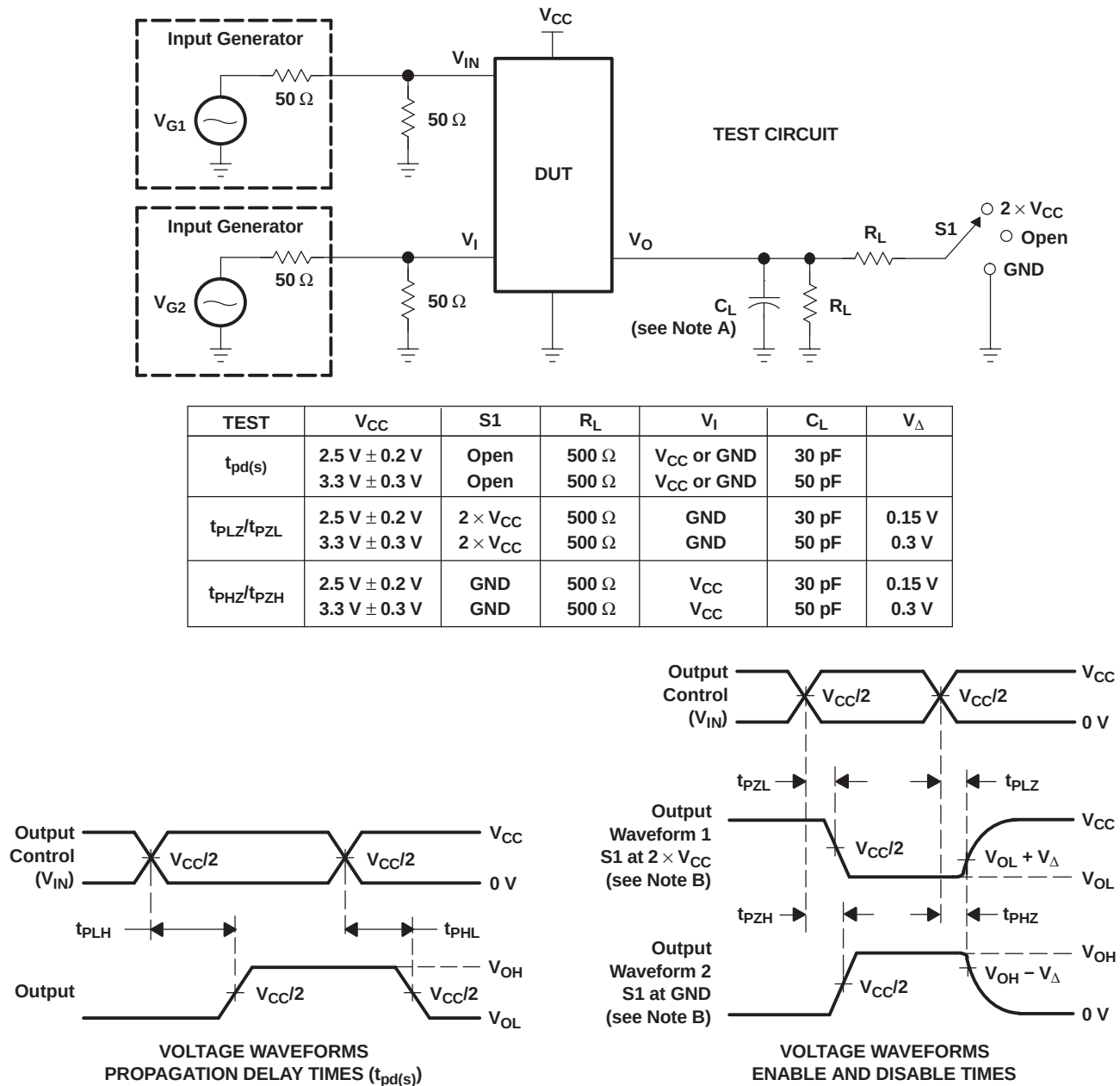


**Figure 2. Typical  $I_{CC}$  vs  $\overline{OE}$  Switching Frequency**

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time, with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - All parameters and waveforms are not applicable to all devices.

**Figure 3. Test Circuit and Voltage Waveforms**

## REVISION HISTORY

| Changes from Revision D (April 2005) to Revision E | Page              |
|----------------------------------------------------|-------------------|
| • Added DCU package ordering information. ....     | <a href="#">1</a> |

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)    |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------|
| 74CB3Q3306ADCURE4                  | Active        | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | GA6R                   |
| <a href="#">74CB3Q3306ADCURG4</a>  | Active        | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | GA6R                   |
| 74CB3Q3306ADCURG4.B                | Active        | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | GA6R                   |
| <a href="#">SN74CB3Q3306ADCUR</a>  | Active        | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | (A6, GA6Q, GA6R)<br>GZ |
| SN74CB3Q3306ADCUR.A                | Active        | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | (A6, GA6Q, GA6R)<br>GZ |
| SN74CB3Q3306ADCUR.B                | Active        | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | (A6, GA6Q, GA6R)<br>GZ |
| <a href="#">SN74CB3Q3306APW</a>    | Obsolete      | Production           | TSSOP (PW)   8  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | BU306A                 |
| <a href="#">SN74CB3Q3306APWR</a>   | Active        | Production           | TSSOP (PW)   8  | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | BU306A                 |
| SN74CB3Q3306APWR.A                 | Active        | Production           | TSSOP (PW)   8  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU306A                 |
| SN74CB3Q3306APWR.B                 | Active        | Production           | TSSOP (PW)   8  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU306A                 |
| <a href="#">SN74CB3Q3306APWRG4</a> | Active        | Production           | TSSOP (PW)   8  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU306A                 |
| SN74CB3Q3306APWRG4.B               | Active        | Production           | TSSOP (PW)   8  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU306A                 |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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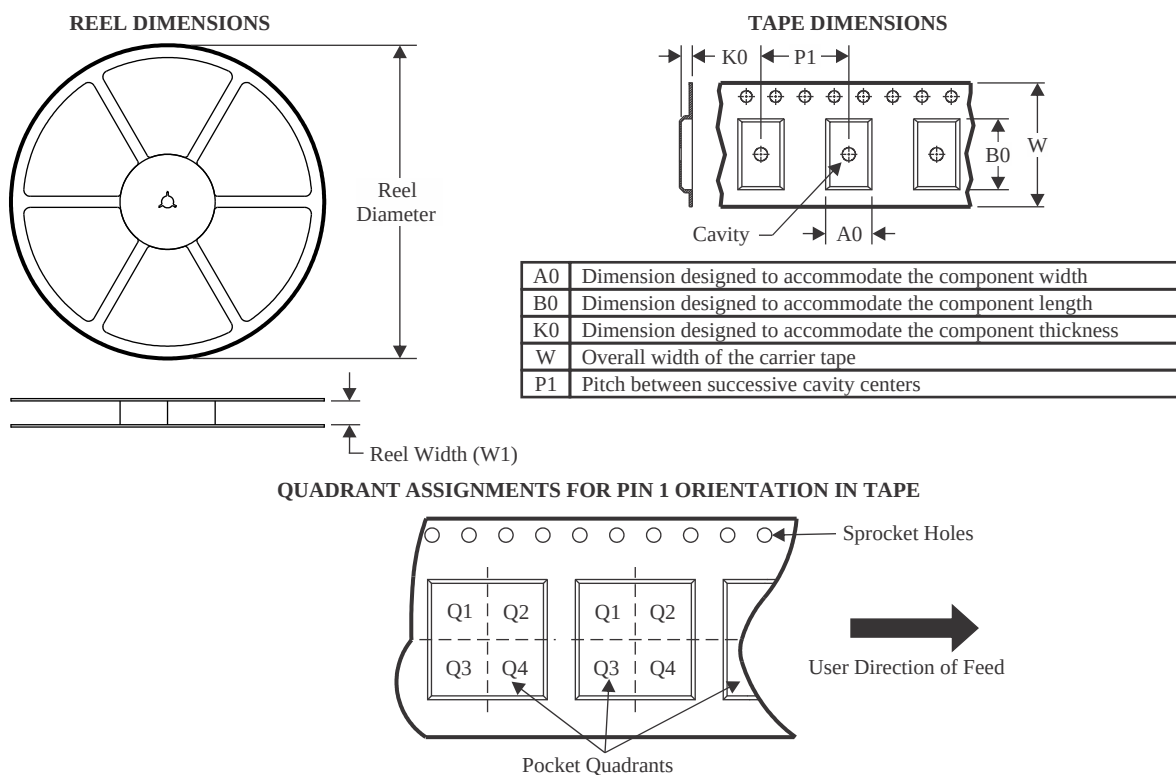
**OTHER QUALIFIED VERSIONS OF SN74CB3Q3306A :**

- Enhanced Product : [SN74CB3Q3306A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

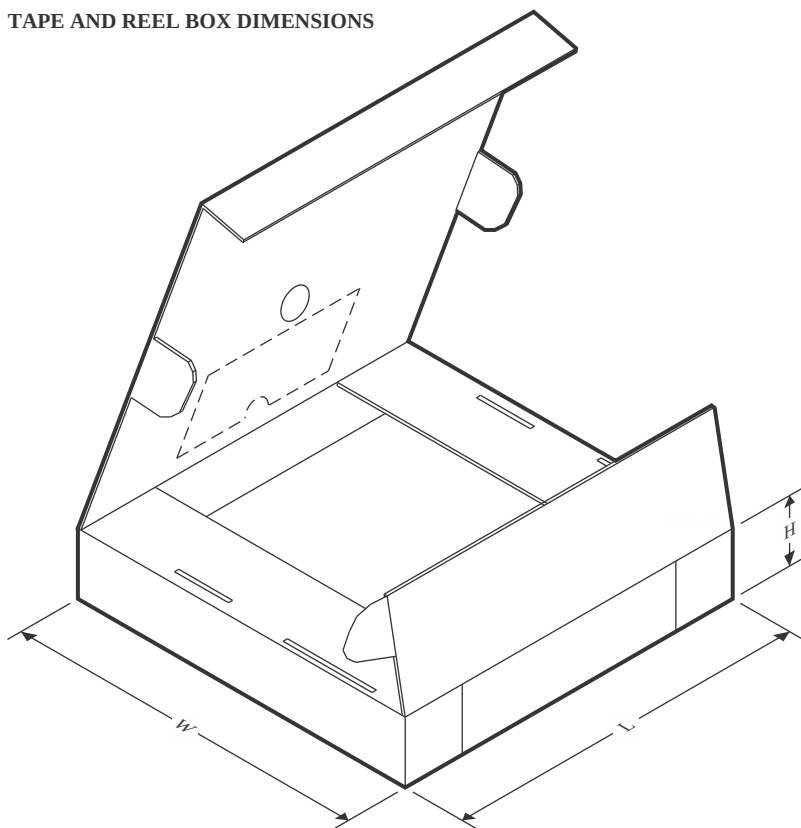
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

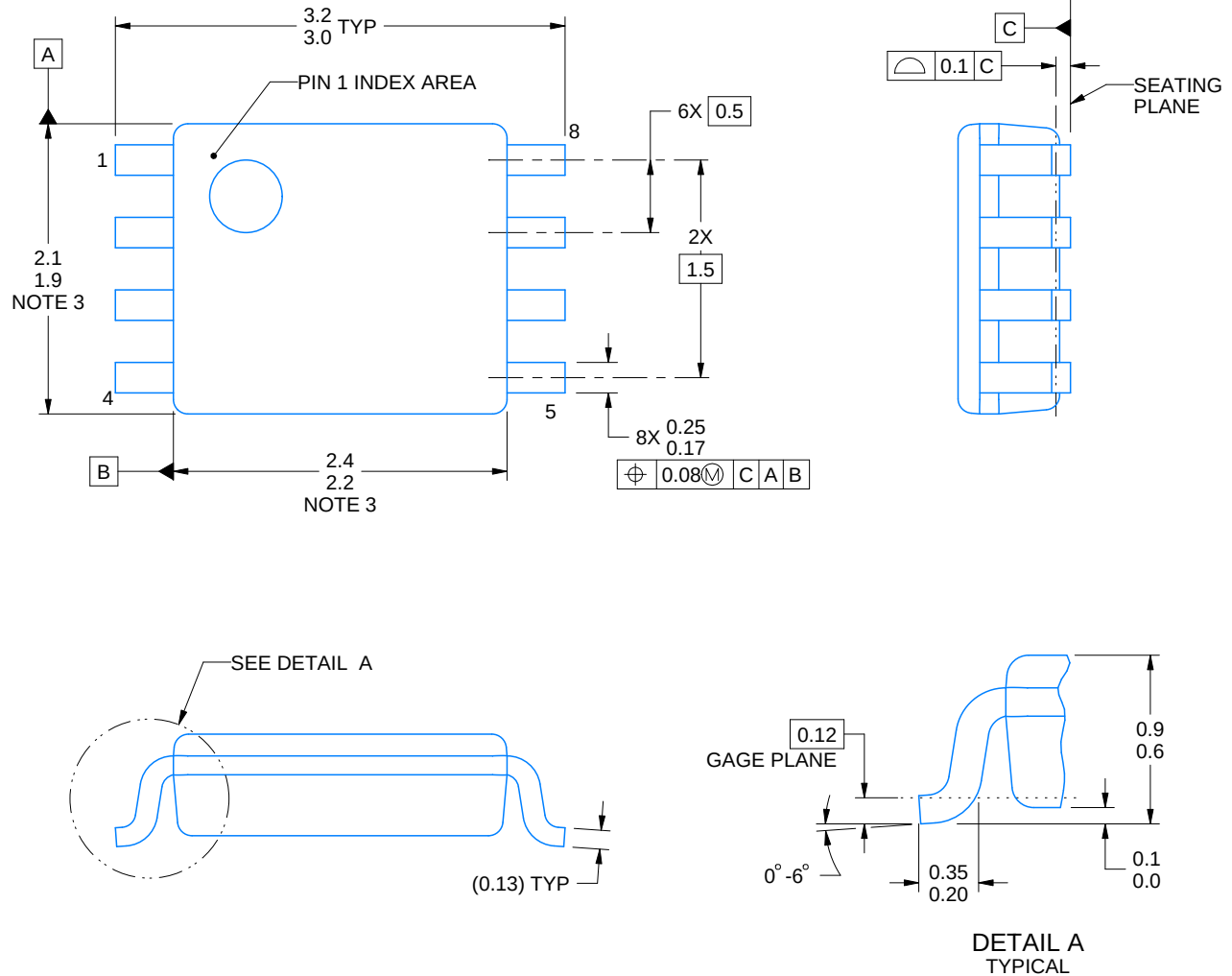
| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74CB3Q3306ADCURG4  | VSSOP        | DCU             | 8    | 3000 | 180.0              | 8.4                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| SN74CB3Q3306ADCUR  | VSSOP        | DCU             | 8    | 3000 | 178.0              | 9.0                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| SN74CB3Q3306APWR   | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CB3Q3306APWRG4 | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74CB3Q3306ADCURG4  | VSSOP        | DCU             | 8    | 3000 | 202.0       | 201.0      | 28.0        |
| SN74CB3Q3306ADCUR  | VSSOP        | DCU             | 8    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74CB3Q3306APWR   | TSSOP        | PW              | 8    | 2000 | 367.0       | 367.0      | 35.0        |
| SN74CB3Q3306APWRG4 | TSSOP        | PW              | 8    | 2000 | 367.0       | 367.0      | 35.0        |



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## NOTES:

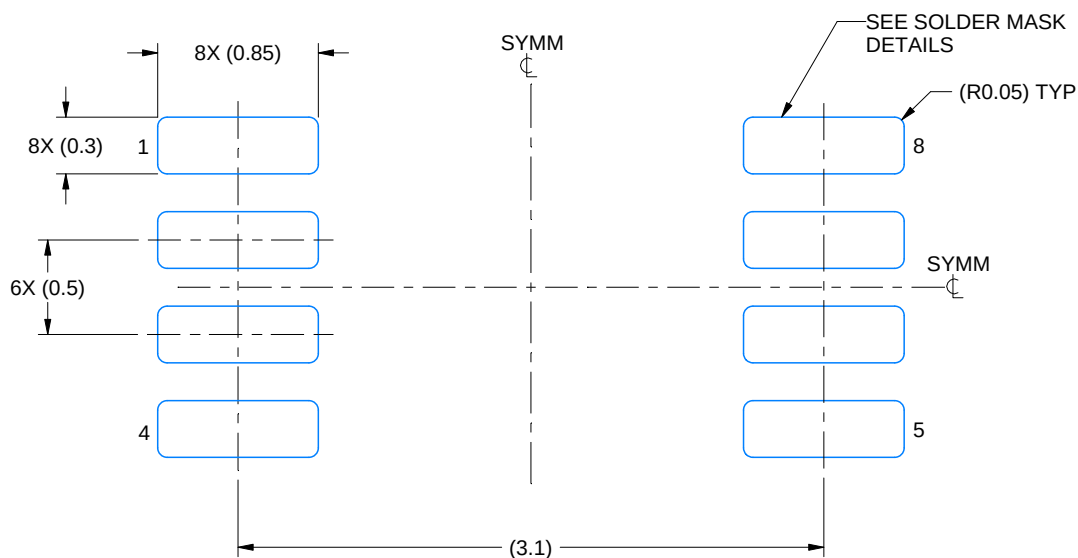
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

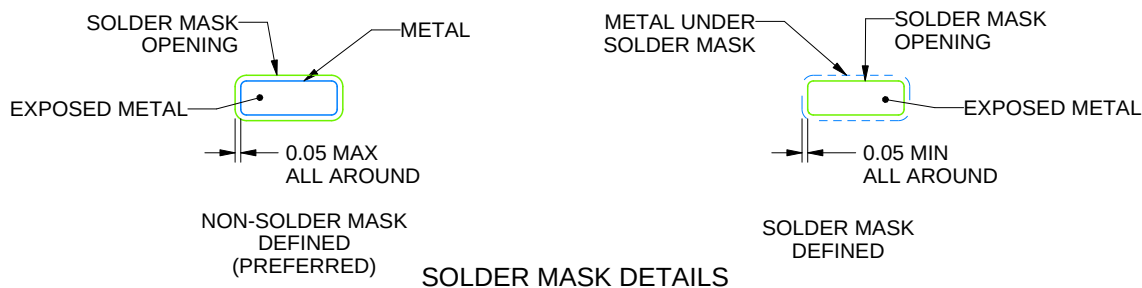
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

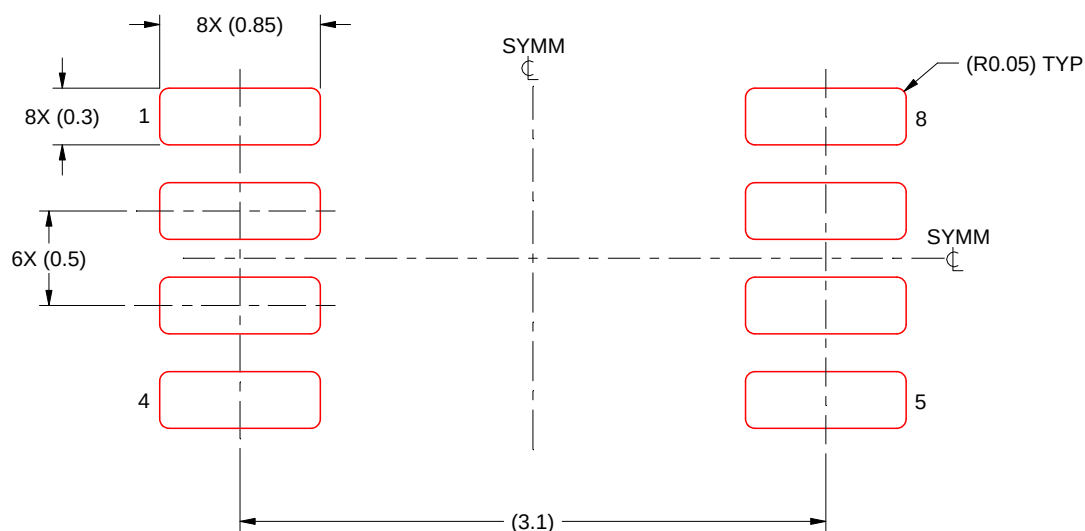
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

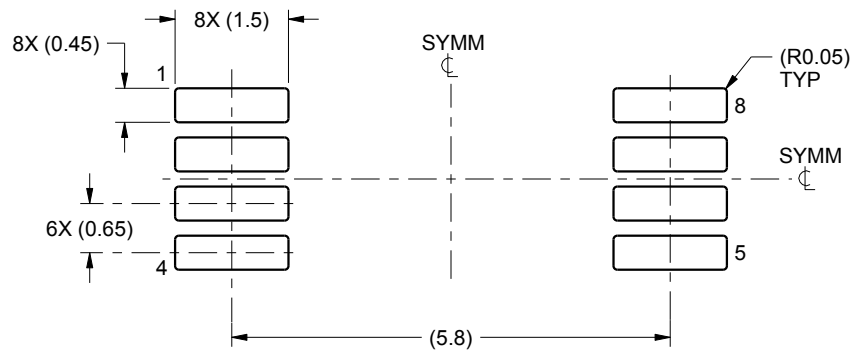


# EXAMPLE BOARD LAYOUT

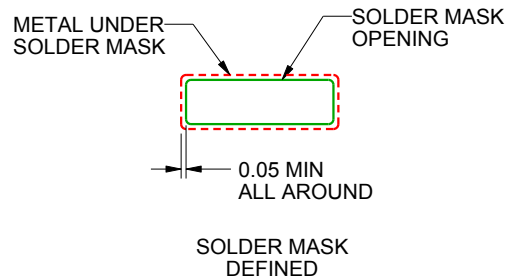
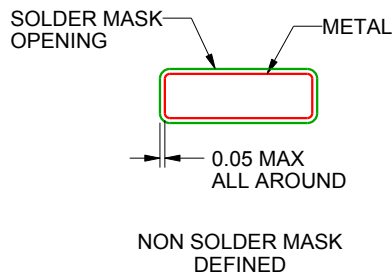
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

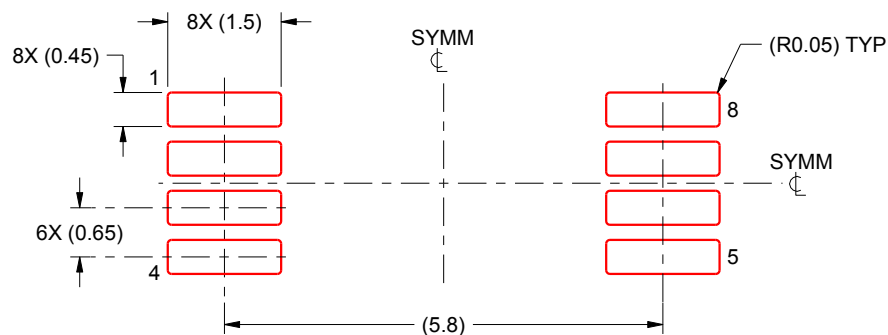
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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