

MAX3221E 3V to 5.5V Single-Channel RS-232 Line Driver and Receiver With $\pm 15\text{kV}$ IEC ESD Protection

1 Features

- ESD protection for RS-232 pins
 - $\pm 15\text{kV}$ Human-body model (HBM)
 - $\pm 8\text{kV}$ (IEC 61000-4-2, Contact discharge)
 - $\pm 15\text{kV}$ (IEC 61000-4-2, Air-gap discharge)
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU v.28 standards
- Operates with 3V to 5.5V V_{CC} supply
- Operates up to 250kbit/s
- One driver and one receiver
- Low standby current: 1 μA typical
- Accepts 5V logic input with 3.3V supply
- Auto-power-down feature automatically disables drivers for power savings
- Alternative high-speed device (1Mbit/s)
 - SN75C3221E and SN65C3221E

2 Applications

- [Industrial PCs](#)
- [Wired networking](#)
- [Data center and enterprise computing](#)
- [Battery-powered systems](#)
- [PDAs](#)
- [Notebooks](#)
- [Laptops](#)
- [Palmtop PCs](#)
- [Hand-held equipment](#)

3 Description

The MAX3221E is a single driver, single receiver RS-232 solution operating from a single V_{CC} supply. The RS-232 pins provide IEC 61000-4-2 ESD protection. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. These devices operate at data signaling rates up to 250kbit/s and a maximum of 30V/ μs driver output slew rate.

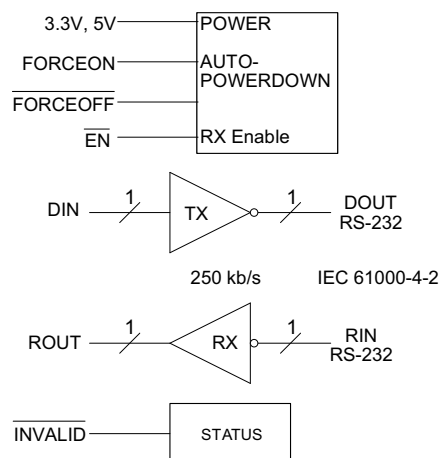
Flexible control options for power management are available. Auto-power down disables driver and charge pump when the receiver is disconnected or the remote driver is power down. The drivers can be manually enabled or disabled. $\overline{\text{INVALID}}$ output goes low when receiver input is unconnected or power off.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
MAX3221E	SSOP (DB, 16)	6.2mm $\times$ 7.8mm
	TSSOP (PW, 16)	5mm $\times$ 6.4mm
	SOT-23-THN (DYY, 16)	4.2mm $\times$ 2mm

(1) For more information, see [Section 11](#).

(2) The package size (length $\times$ width) is a nominal value and includes pins, where applicable.



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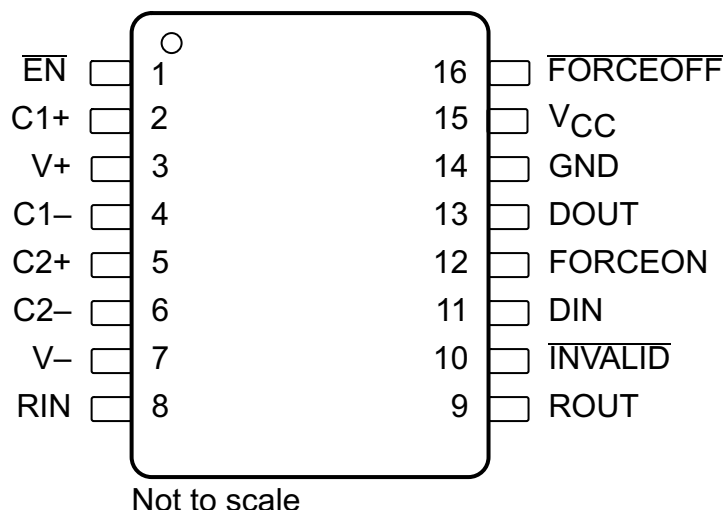
Block Diagram



Table of Contents

1 Features	1	7 Detailed Description	12
2 Applications	1	7.1 Overview.....	12
3 Description	1	7.2 Functional Block Diagram.....	12
4 Pin Configuration and Functions	3	7.3 Feature Description.....	12
5 Specifications	4	7.4 Device Functional Modes.....	13
5.1 Absolute Maximum Ratings.....	4	8 Application and Implementation	14
5.2 ESD Ratings.....	4	8.1 Application Information.....	14
5.3 ESD Ratings - IEC Specifications.....	4	8.2 Typical Application.....	14
5.4 Recommended Operating Conditions.....	5	8.3 Power Supply Recommendations.....	15
5.5 Thermal Information.....	5	8.4 Layout.....	16
5.6 Electrical Characteristics.....	5	9 Device and Documentation Support	17
5.7 Electrical Characteristics: Driver.....	6	9.1 Receiving Notification of Documentation Updates....	17
5.8 Electrical Characteristics: Receiver.....	6	9.2 Support Resources.....	17
5.9 Electrical Characteristics: Auto-Power Down.....	6	9.3 Trademarks.....	17
5.10 Switching Characteristics: Driver.....	7	9.4 Electrostatic Discharge Caution.....	17
5.11 Switching Characteristics: Receiver.....	7	9.5 Glossary.....	17
5.12 Switching Characteristics: Auto-Power Down.....	7	10 Revision History	17
5.13 Typical Characteristics.....	8	11 Mechanical, Packaging, and Orderable Information	18
6 Parameter Measurement Information	9		

4 Pin Configuration and Functions



Not to scale

**Figure 4-1. DB, PW or DYY Package
16-Pin SSOP, TSSOP, or SOT-23-THN
(Top View)**

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	2	—	Positive terminals of the voltage-doubler charge pump capacitors
C2+	5		
C1–	4	—	Negative terminals of the voltage-doubler charge pump capacitors
C2–	6		
DIN	11	I	Driver input
DOUT	13	O	RS-232 driver output
EN	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
FORCEOFF	16	I	Automatic power-down control input
FORCEON	12	I	Automatic power-down control input
GND	14	—	Ground
INVALID	10	O	Invalid output pin. Output low when RIN input is unpowered.
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
V _{CC}	15	—	3V to 5.5V supply voltage
V+	3	O	5.5V supply generated by the charge pump
V–	7	O	–5.5V supply generated by the charge pump

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		−0.3	6	V
V+	Positive output supply voltage ⁽²⁾		−0.3	7	V
V−	Negative output supply voltage ⁽²⁾		0.3	−7	V
V+ − V−	Supply voltage difference ⁽²⁾			13	V
V _I	Input voltage	DIN, FORCEOFF, FORCEON, EN	−0.3	6	V
		RIN	−25	25	
V _O	Output voltage	DOUT	−13.2	13.2	V
		ROUT, INVALID	−0.3	V _{CC} + 0.3	
T _J	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages are with respect to network GND.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Pins 8 and 13	±15000
			All other pins	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	All pins	±1500

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, DOUT and RIN ^{(1) (2)}	±8000	V
		IEC 61000-4-2 Air-Gap Discharge, DOUT and RIN ^{(1) (2)}	±15000	

- (1) A minimum of 1μF capacitor is required between VCC and GND to meet the specified IEC-ESD level.
- (2) For optimized IEC ESD performance for DYY package, the recommendation is to have series resistor (≥ 50Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

5.4 Recommended Operating Conditions

See [Figure 8-1](#) ⁽¹⁾

				MIN	NOM	MAX	UNIT	
Supply voltage			$V_{CC} = 3.3V$	3	3.3	3.6	V	
			$V_{CC} = 5V$	4.5	5	5.5		
V_{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON, $\overline{EN}$	$V_{CC} = 3.3V$	2			V	
			$V_{CC} = 5V$	2.4				
V_{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON, $\overline{EN}$			0.8		V	
V_I	Driver and control input voltage	DIN, FORCEOFF, FORCEON			0		5.5	V
V_I	Receiver input voltage			−25		25		V
T_A	Operating free-air temperature	MAX3221EC			0		70	°C
		MAX3221EI			−40		85	

(1) Test conditions are $C1-C4 = 0.1\mu F$ at $V_{CC} = 3.3V \pm 0.3V$; $C1 = 0.047\mu F$, $C2-C4 = 0.33\mu F$ at $V_{CC} = 5V \pm 0.5V$.

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		MAX3221E			UNIT
		DB (SSOP)	PW (TSSOP)	DYY (SOT-23-THN)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.8	110.9	120.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	41.7	56.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.6	57.2	51.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.1	4.2	2.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	56.8	56.6	50.9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽²⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
I_I	Input leakage current	FORCEOFF, FORCEON, $\overline{EN}$			±0.01	±1	μA
I_{CC}	Supply current	Auto-power down disabled	No load, FORCEOFF and FORCEON at V_{CC}		0.3	1	mA
		Powered off	$V_{CC} = 3.3V$ or $5V$, $T_A = 25^\circ C$		1	10	μA
		Auto-power down enabled	No load, FORCEOFF at V_{CC} , FORCEON at GND, All RIN are open or grounded		1	10	

(1) All typical values are at $V_{CC} = 3.3V$ or $V_{CC} = 5V$, and $T_A = 25^\circ C$.

(2) Test conditions are $C1-C4 = 0.1\mu F$ at $V_{CC} = 3.3V \pm 0.3V$; $C1 = 0.047\mu F$, $C2-C4 = 0.33\mu F$ at $V_{CC} = 5V \pm 0.5V$.

5.7 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽³⁾

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH} High-level output voltage	DOUT at R _L = 3kΩ to GND, DIN = GND	5	5.4		V
V _{OL} Low-level output voltage	DOUT at R _L = 3kΩ to GND, DIN = V _{CC}	–5	–5.4		V
I _{IH} High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL} Low-level input current	V _I = GND		±0.01	±1	μA
I _{OS} Short-circuit output current ⁽²⁾	V _{CC} = 3.6V, V _O = 0V		±35	±60	mA
	V _{CC} = 5.5V, V _O = 0V		±35	±60	
r _o Output resistance	V _{CC} , V ₊ , and V _– = 0V, V _O = ±2V	300	10M		Ω
I _{off} Output leakage current	FORCEOFF = GND	V _O = ±12V, V _{CC} = 3V to 3.6V		±25	μA
		V _O = ±10V, V _{CC} = 4.5V to 5.5V		±25	

(1) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

(3) Test conditions are C1–C4 = 0.1μF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047μF, C2–C4 = 0.33μF at V_{CC} = 5V ± 0.5V.

5.8 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽²⁾

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH} High-level output voltage	I _{OH} = –1mA	V _{CC} – 0.6	V _{CC} – 0.1		V
V _{OL} Low-level output voltage	I _{OL} = 1.6mA			0.4	V
V _{IT+} Positive-going input threshold voltage	V _{CC} = 3.3V		1.6	2.4	V
	V _{CC} = 5V		1.9	2.4	
V _{IT–} Negative-going input threshold voltage	V _{CC} = 3.3V	0.6	1.1		V
	V _{CC} = 5V	0.8	1.4		
V _{hys} Input hysteresis (V _{IT+} – V _{IT–})			0.5		V
I _{off} Output leakage current	EN = V _{CC}		±0.05	±10	μA
r _i Input resistance	V _I = ±3V to ±25V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.

(2) Test conditions are C1–C4 = 0.1μF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047μF, C2–C4 = 0.33μF at V_{CC} = 5V ± 0.5V.

5.9 Electrical Characteristics: Auto-Power Down

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V _{T+(valid)} Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}		2.7	V
V _{T–(valid)} Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	–2.7		V
V _{T(invalid)} Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	–0.3	0.3	V
V _{OH} INVALID high-level output voltage	I _{OH} = –1mA, FORCEON = GND, FORCEOFF = V _{CC}	V _{CC} – 0.6		V
V _{OL} INVALID low-level output voltage	I _{OL} = 1.6mA, FORCEON = GND, FORCEOFF = V _{CC}		0.4	V

5.10 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽³⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
	Maximum data rate	$C_L = 1000\text{pF}$,	$R_L = 3\text{k}\Omega$,	150	250		kbit/s
$t_{sk(p)}$	Pulse skew ⁽²⁾	$C_L = 150\text{pF}$ to 2500pF ,	$R_L = 3\text{k}\Omega$ to $7\text{k}\Omega$, See Figure 6-2		100		ns
$SR(tr)$	Slew rate, transition region (see Figure 6-1)	$V_{CC} = 3.3\text{V}$, $R_L = 3\text{k}\Omega$ to $7\text{k}\Omega$	$C_L = 150\text{pF}$ to 1000pF	6		30	V/ μs
			$C_L = 150\text{pF}$ to 2500pF	4		30	

- (1) All typical values are at $V_{CC} = 3.3\text{V}$ or $V_{CC} = 5\text{V}$, and $T_A = 25^\circ\text{C}$.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are $C1-C4 = 0.1\mu\text{F}$ at $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$; $C1 = 0.047\mu\text{F}$, $C2-C4 = 0.33\mu\text{F}$ at $V_{CC} = 5\text{V} \pm 0.5\text{V}$.

5.11 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽³⁾

PARAMETER		TEST CONDITIONS	TYP ⁽¹⁾	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 150\text{pF}$, See Figure 6-3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output	$C_L = 150\text{pF}$, See Figure 6-3	150	ns
t_{en}	Output enable time	$C_L = 150\text{pF}$, $R_L = 3\text{k}\Omega$, See Figure 6-4	200	ns
t_{dis}	Output disable time	$C_L = 150\text{pF}$, $R_L = 3\text{k}\Omega$, See Figure 6-4	200	ns
$t_{sk(p)}$	Pulse skew ⁽²⁾	See Figure 6-3	50	ns

- (1) All typical values are at $V_{CC} = 3.3\text{V}$ or $V_{CC} = 5\text{V}$, and $T_A = 25^\circ\text{C}$.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are $C1-C4 = 0.1\mu\text{F}$ at $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$; $C1 = 0.047\mu\text{F}$, $C2-C4 = 0.33\mu\text{F}$ at $V_{CC} = 5\text{V} \pm 0.5\text{V}$.

5.12 Switching Characteristics: Auto-Power Down

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TYP ⁽¹⁾	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	μs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	μs
t_{en}	Supply enable time	100	μs

- (1) All typical values are at $V_{CC} = 3.3\text{V}$ or $V_{CC} = 5\text{V}$, and $T_A = 25^\circ\text{C}$.

5.13 Typical Characteristics

$T_A = 25^\circ\text{C}$; $V_{CC} = 3.3\text{V}$

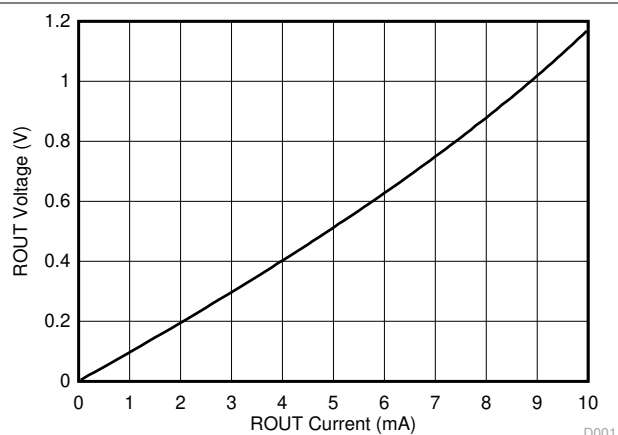


Figure 5-1. Receiver VOL vs Load Current

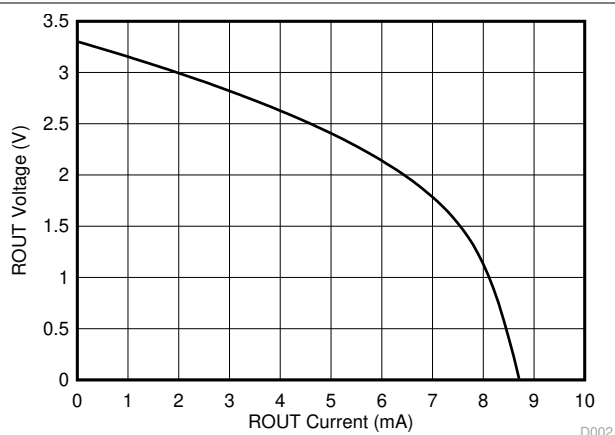


Figure 5-2. Receiver VOH vs Load Current

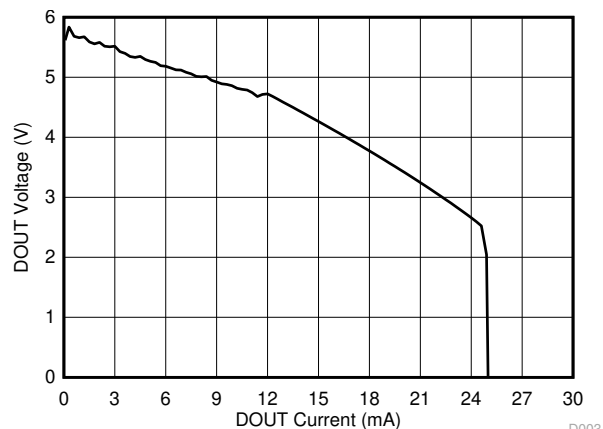


Figure 5-3. Driver VOH vs Load Current

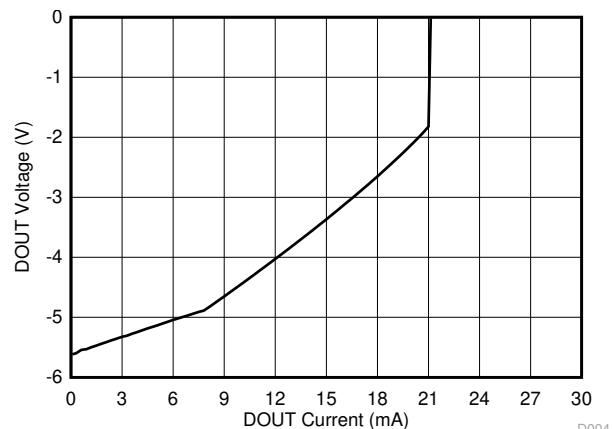
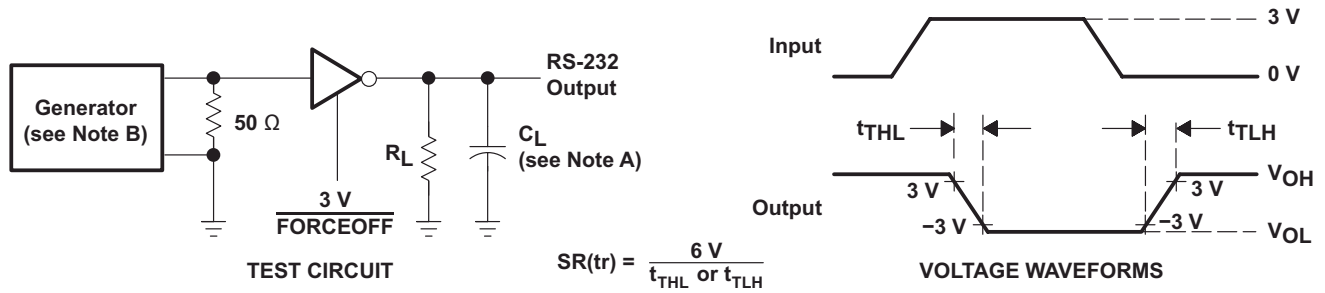


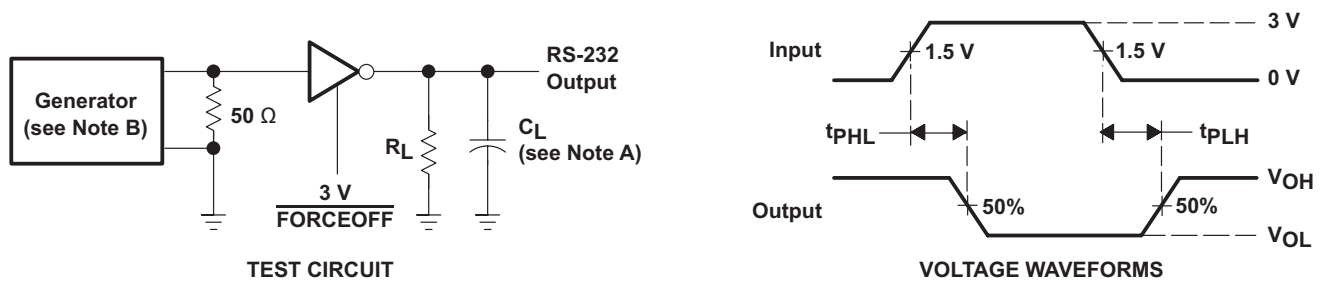
Figure 5-4. Driver VOL vs Load Current

6 Parameter Measurement Information



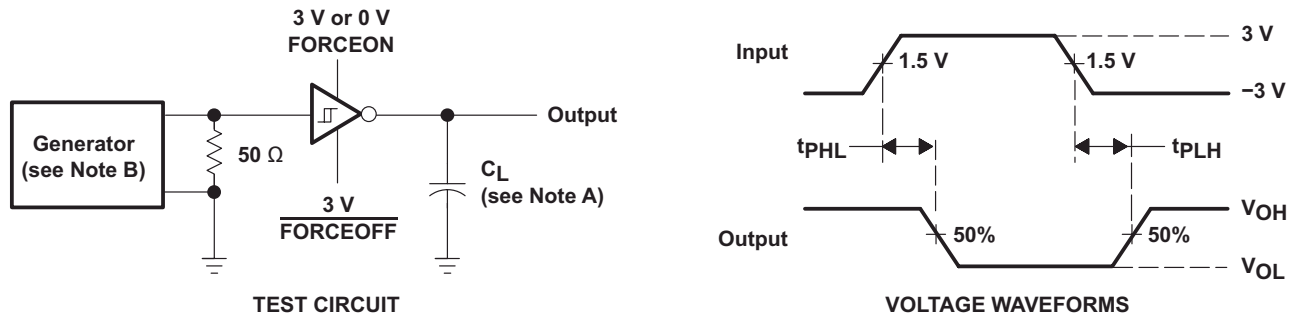
- A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250kbps, $Z_O = 50\Omega$, 50% duty cycle, $t_r \leq 10\text{ns}$, $t_f \leq 10\text{ns}$.

Figure 6-1. Driver Slew Rate



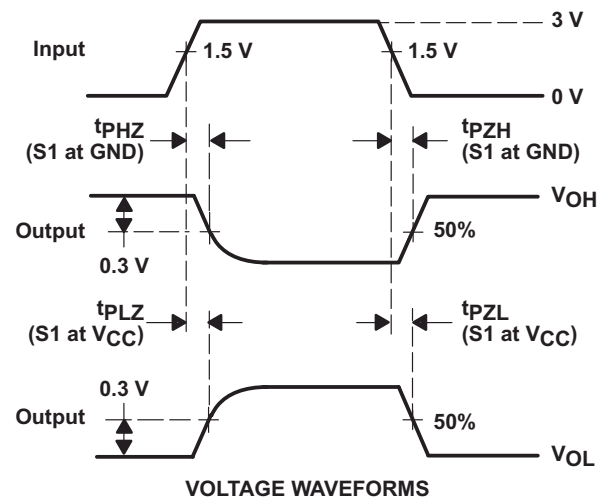
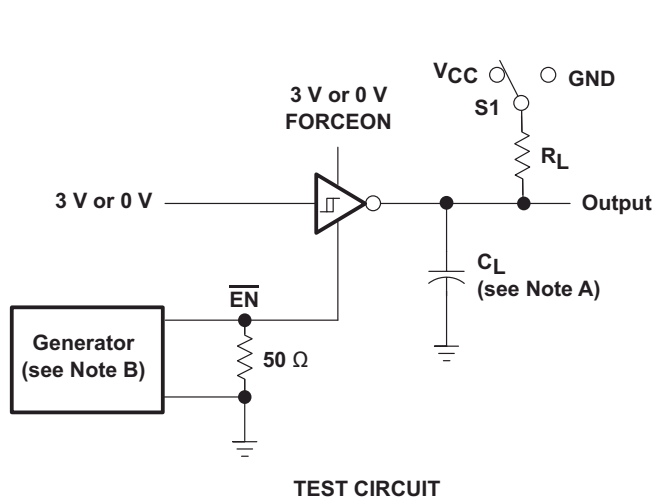
- A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250kbps, $Z_O = 50\Omega$, 50% duty cycle, $t_r \leq 10\text{ns}$, $t_f \leq 10\text{ns}$.

Figure 6-2. Driver Pulse Skew



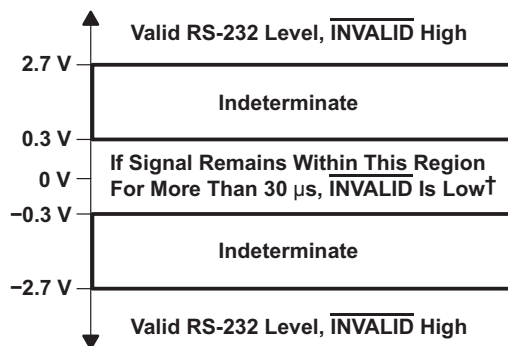
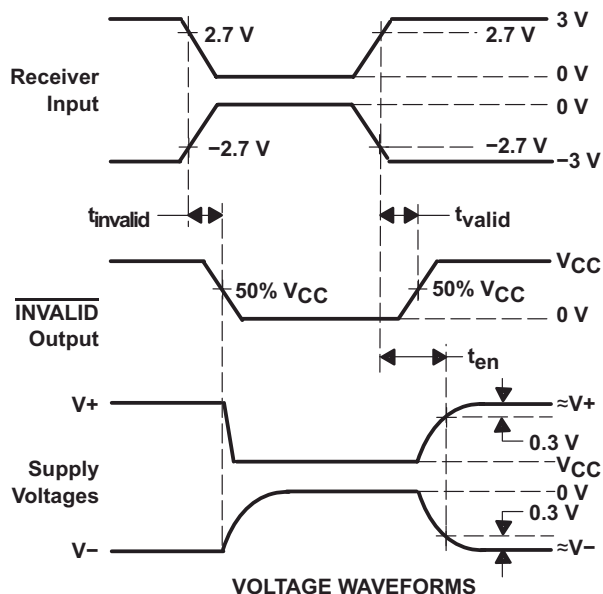
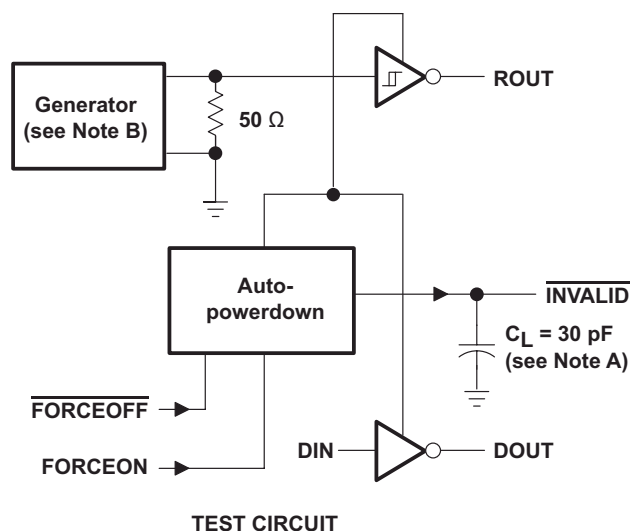
- A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50\Omega$, 50% duty cycle, $t_r \leq 10\text{ns}$, $t_f \leq 10\text{ns}$.

Figure 6-3. Receiver Propagation Delay Times



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\Omega$, 50% duty cycle, $t_r \leq 10\text{ns}$, $t_f \leq 10\text{ns}$.
- C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- D. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 6-4. Receiver Enable and Disable Times



† Auto-powerdown disables drivers and reduces supply current to 1 μ A.

Figure 6-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Driver Enabling Time

7 Detailed Description

7.1 Overview

The MAX3221E is a single driver, single receiver RS-232 solution operating from a single V_{CC} supply. The RS-232 pins provide IEC 61000-4-2 ESD protection. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. These devices operate at data signaling rates up to 250kbit/s and a maximum of 30V/ μ s driver output slew rate.

Flexible control options for power management are available when the serial port is inactive. The auto-power-down feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If $\overline{\text{FORCEOFF}}$ is set low and $\overline{\text{EN}}$ is high, both the driver and receiver are shut off, and the supply current is reduced to 1 μ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-power-down condition to occur. Auto-power down can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-power down enabled, the device is activated automatically when a valid signal is applied to the receiver input. The $\overline{\text{INVALID}}$ output notifies the user if an RS-232 signal is present at the receiver input. $\overline{\text{INVALID}}$ is high (valid data) if the receiver input voltage is greater than 2.7V or less than -2.7V, or has been between -0.3V and 0.3V for less than 30 μ s. $\overline{\text{INVALID}}$ is low (invalid data) if the receiver input voltage is between -0.3V and 0.3V for more than 30 μ s. See [Figure 6-1](#) for receiver input levels.

7.2 Functional Block Diagram

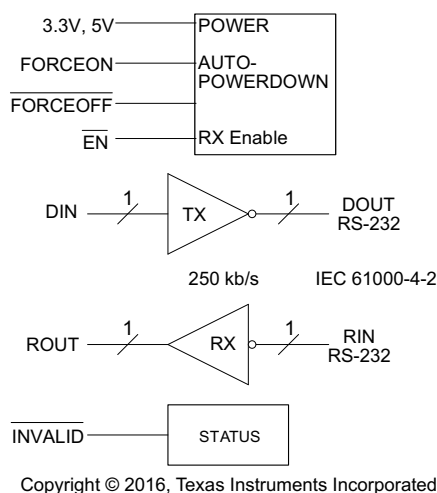


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V- pins using a charge pump that requires four external capacitors. Auto-power-down feature for driver is controlled by FORCEON and $\overline{\text{FORCEOFF}}$ inputs. Receiver is controlled by $\overline{\text{EN}}$ input. When unpowered, the MAX3221E can be safely connected to an active remote RS-232 device.

7.3.2 RS-232 Driver

One driver interfaces standard logic levels to RS-232 levels. DIN input must be valid high or low.

7.3.3 RS-232 Receiver

One receiver interfaces RS-232 levels to standard logic levels. An open input results in a high output on ROUT. RIN input includes an internal standard RS-232 load. A logic high input on the $\overline{\text{EN}}$ pin shuts down the receiver output.

7.3.4 RS-232 Status

The $\overline{\text{INVALID}}$ output goes low when RIN input is unpowered for more than 30 μs . The $\overline{\text{INVALID}}$ output goes high when receiver has a valid input. The $\overline{\text{INVALID}}$ output is active when V_{CC} is powered irregardless of FORCEON and $\overline{\text{FORCEOFF}}$ inputs (see Table 7-3).

7.4 Device Functional Modes

Table 7-1, Table 7-2, and Table 7-3 show the behavior of the driver, receiver, and $\overline{\text{INVALID}}$ features under all possible relevant combinations of inputs.

Table 7-1. Function Tables Each Driver ⁽¹⁾

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-power down disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-power down enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-power down feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Table 7-2. Each Receiver ⁽¹⁾

INPUTS			OUTPUT ROUT
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

Table 7-3. $\overline{\text{INVALID}}$ ⁽¹⁾

INPUTS				OUTPUT
RIN	FORCEON	FORCEOFF	EN	$\overline{\text{INVALID}}$
L	X	X	X	H
H	X	X	X	H
Open	X	X	X	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

8 Application and Implementation

Note

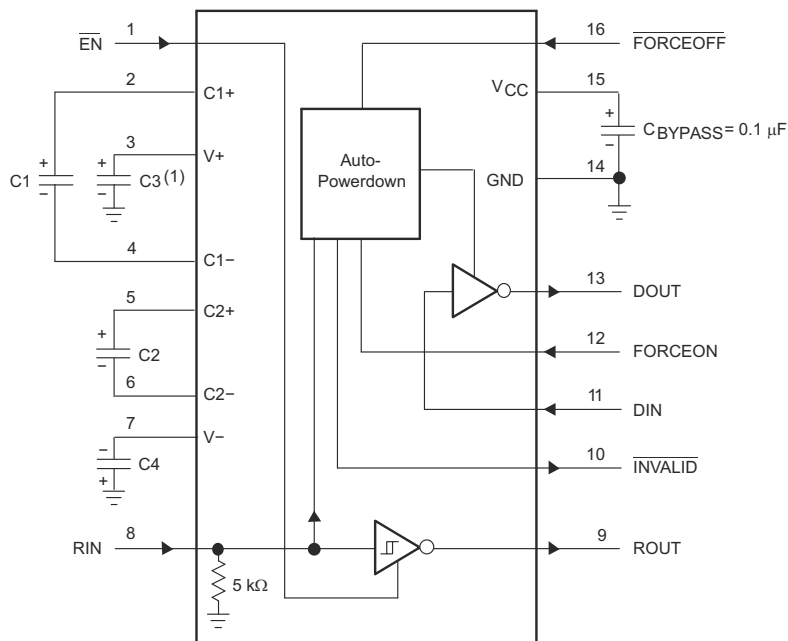
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The MAX3221E line driver and receiver is a specialized device for 3V to 5.5V RS-232 communication applications. This application is a generic implementation of this device with all required external components. For proper operation, add capacitors as shown in [Figure 8-1](#).

8.2 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$ may be connected general purpose logic lines or tied to ground or V_{CC} . $\overline{\text{INVALID}}$ may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS-232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected.



(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V $\pm$ 0.3 V	0.1 μ F	0.1 μ F
5 V $\pm$ 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

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Figure 8-1. Typical Operating Circuit and Capacitor Values

8.2.1 Design Requirements

- Recommended V_{CC} is 3.3V or 5V.
 - 3V to 5.5V is also possible
- Maximum recommended bit rate is 250kbps.
- Use capacitors as shown in [Figure 8-1](#).

8.2.2 Detailed Design Procedure

- DIN, FORCEOFF and FORCEON inputs must be connected to valid low or high logic levels.
- Select capacitor values based on V_{CC} level for best performance.

8.2.3 Application Curves

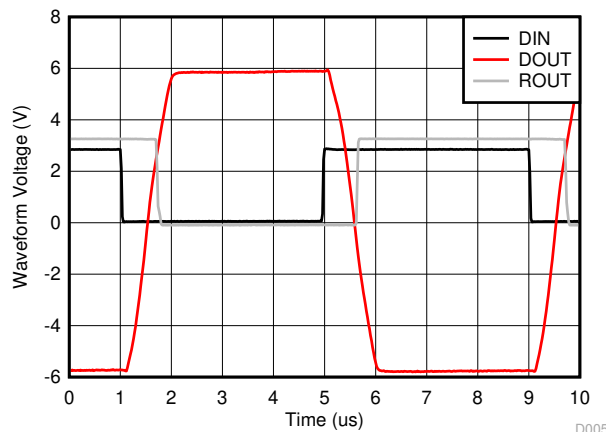


Figure 8-2. Loopback Waveforms $V_{CC} = 3.3V$, Data Rate 250kbit/s

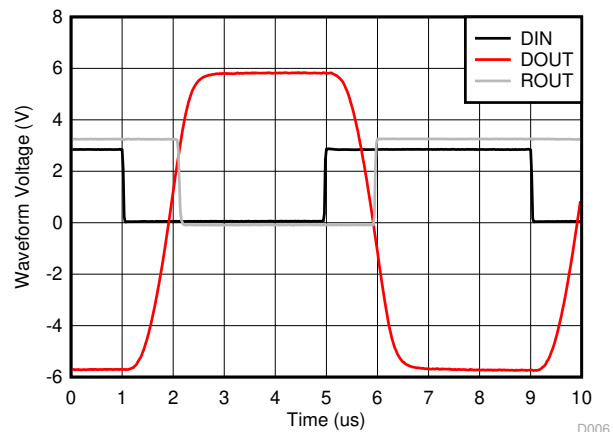


Figure 8-3. Loopback Waveforms with 1nF load $V_{CC} = 3.3V$, Data Rate 250kbit/s

8.3 Power Supply Recommendations

TI recommends a 0.1 μF capacitor to filter noise on the power supply pin. For additional filter capability, a 0.01 μF capacitor may be added in parallel as well. Power supply input voltage is recommended to be any valid level in [Section 5.4](#).

8.4 Layout

8.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. Make the impedance from MAX3221E ground pin and the circuit board ground plane as low as possible for best ESD performance. Use wide metal and multiple vias on both sides of ground pin.

8.4.2 Layout Example

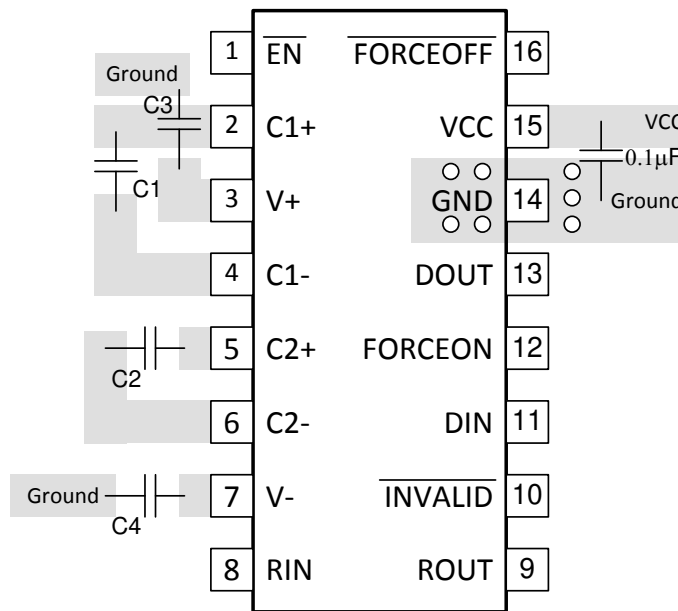


Figure 8-4. MAX3221E Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2024) to Revision E (December 2024)	Page
• Added the SOT-23-THN (DYY) package to the data sheet.....	1
• Added Note 2 to the <i>ESD ratings - IEC Specifications</i>	4
Changes from Revision C (July 2021) to Revision D (July 2024)	Page
• Changed the <i>Device Information</i> table to the <i>Package Information</i> table.....	1
• Changed Pins 8 and 11 to Pins 8 and 13 in the <i>ESD Ratings</i>	4
• Changed Pins 8 and 11 to Pins 8 and 13 in the <i>ESD ratings - IEC Specifications</i>	4
Changes from Revision B (March 2016) to Revision C (July 2021)	Page
• Changed the <i>Applications</i> list.....	1
• Added <i>ESD ratings IEC Specifications</i> table and added a table note for the minimum requirement to meet the IEC ESD level.....	4
• Changed values in the <i>Thermal Information</i> table for DB and PW packages.....	5

Changes from Revision A (May 2006) to Revision B (March 2016)**Page**

-
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
 - Deleted *Ordering Information* table; see the POA at the end of the data sheet 1
 - Changed $R_{\theta JA}$ thermal values: 82 to 92 for DB package and 108 to 100.3 for PW Package..... 5
-

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MAX3221ECDBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC
MAX3221ECDBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC
MAX3221ECDBRG4	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC
MAX3221ECPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC
MAX3221ECPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC
MAX3221ECPWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EC
MAX3221ECPWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EC
MAX3221EIDBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIDBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIDBRG4	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIDYYR	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIDYYR.A	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	MP221EI
MAX3221EIPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIPWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI
MAX3221EIPWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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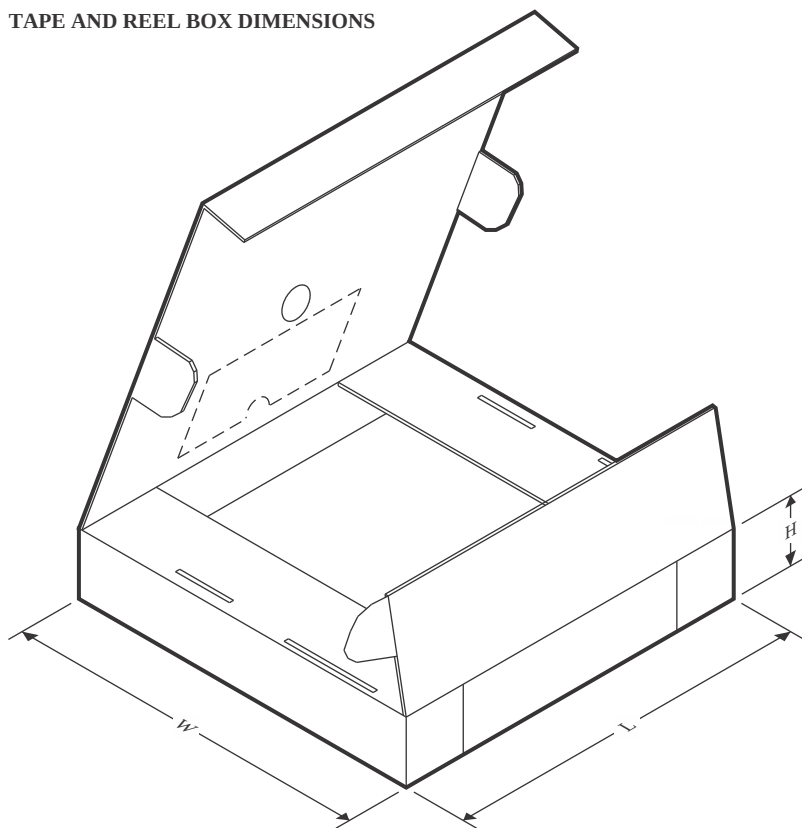
TAPE AND REEL INFORMATION



*All dimensions are nominal

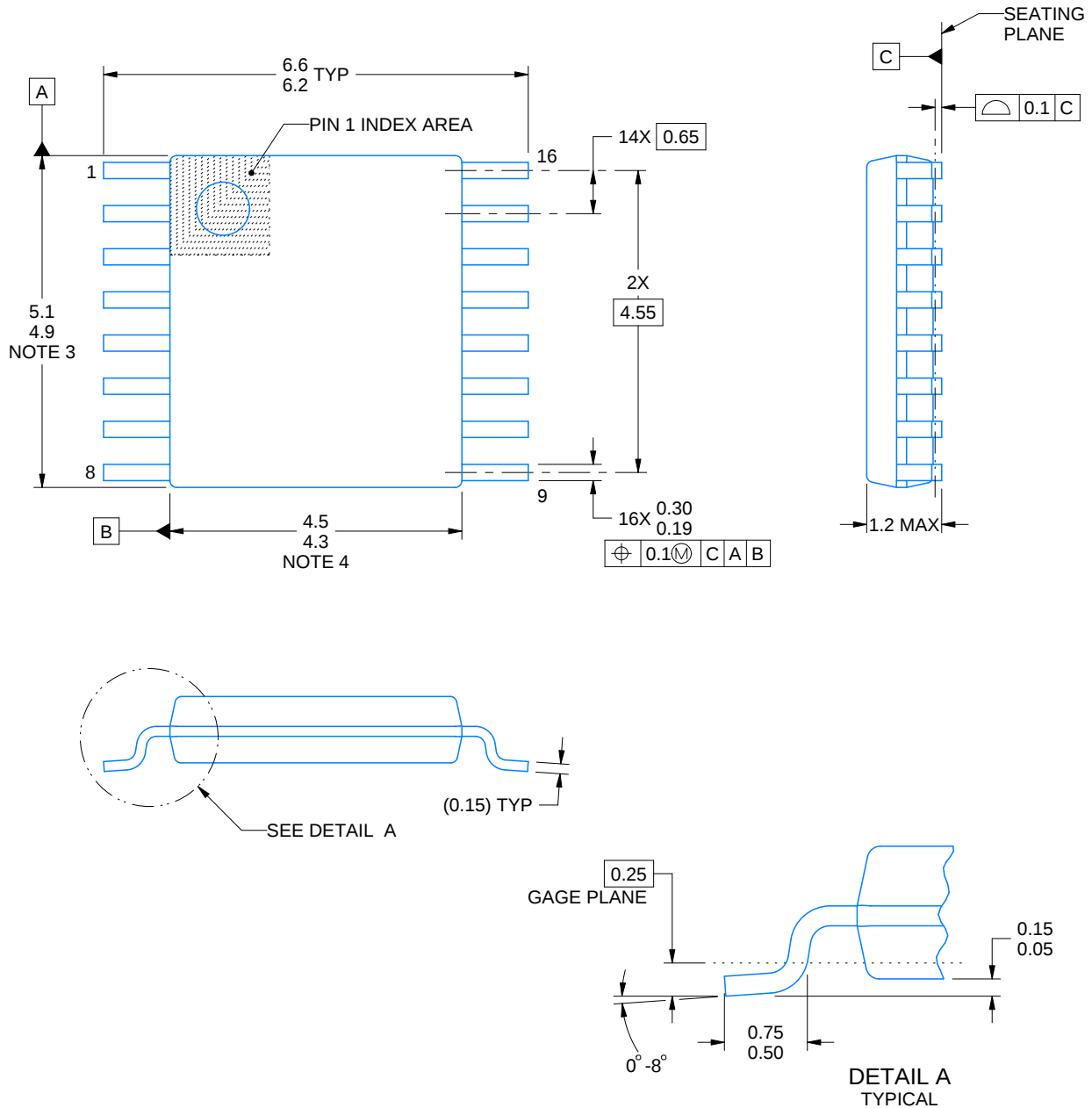
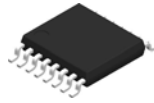
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3221ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221ECPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3221EIDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
MAX3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221EIPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3221ECDBR	SSOP	DB	16	2000	356.0	356.0	35.0
MAX3221ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
MAX3221ECPWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
MAX3221EIDBR	SSOP	DB	16	2000	356.0	356.0	35.0
MAX3221EIDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
MAX3221EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
MAX3221EIPWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0



4220204/A 02/2017

NOTES:

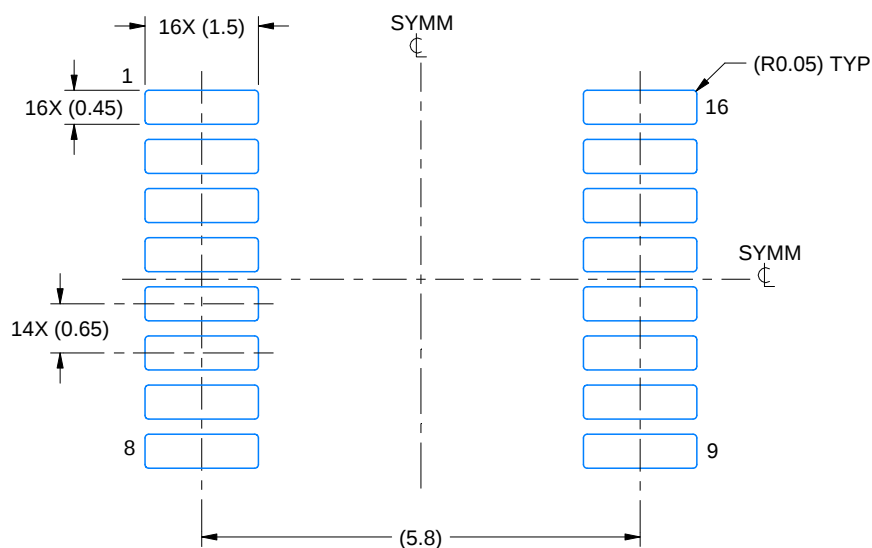
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

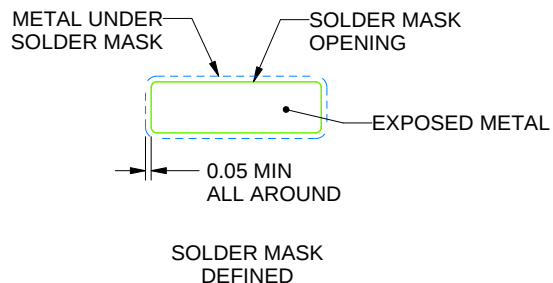
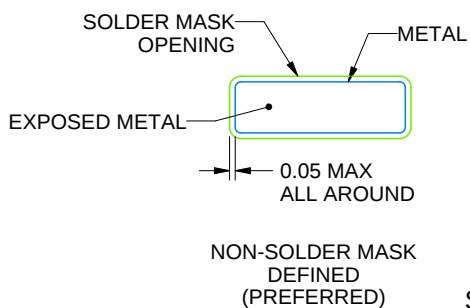
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

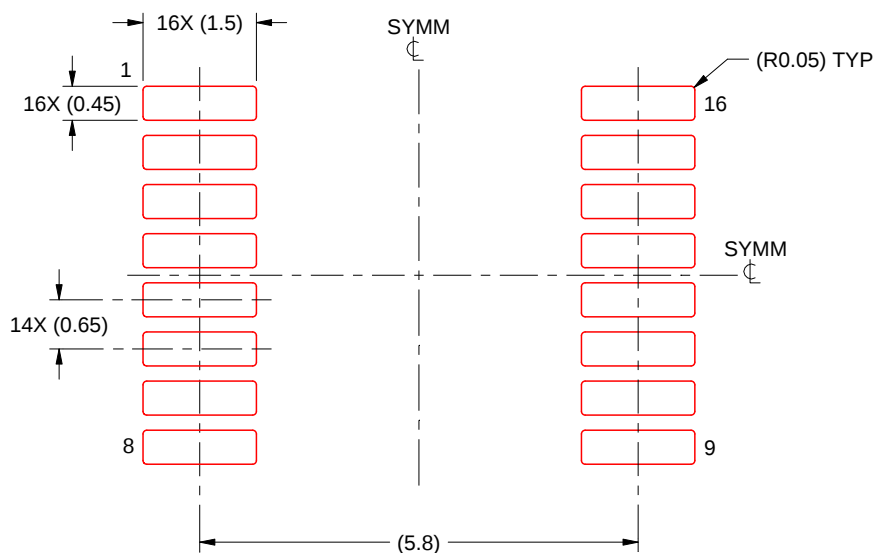
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

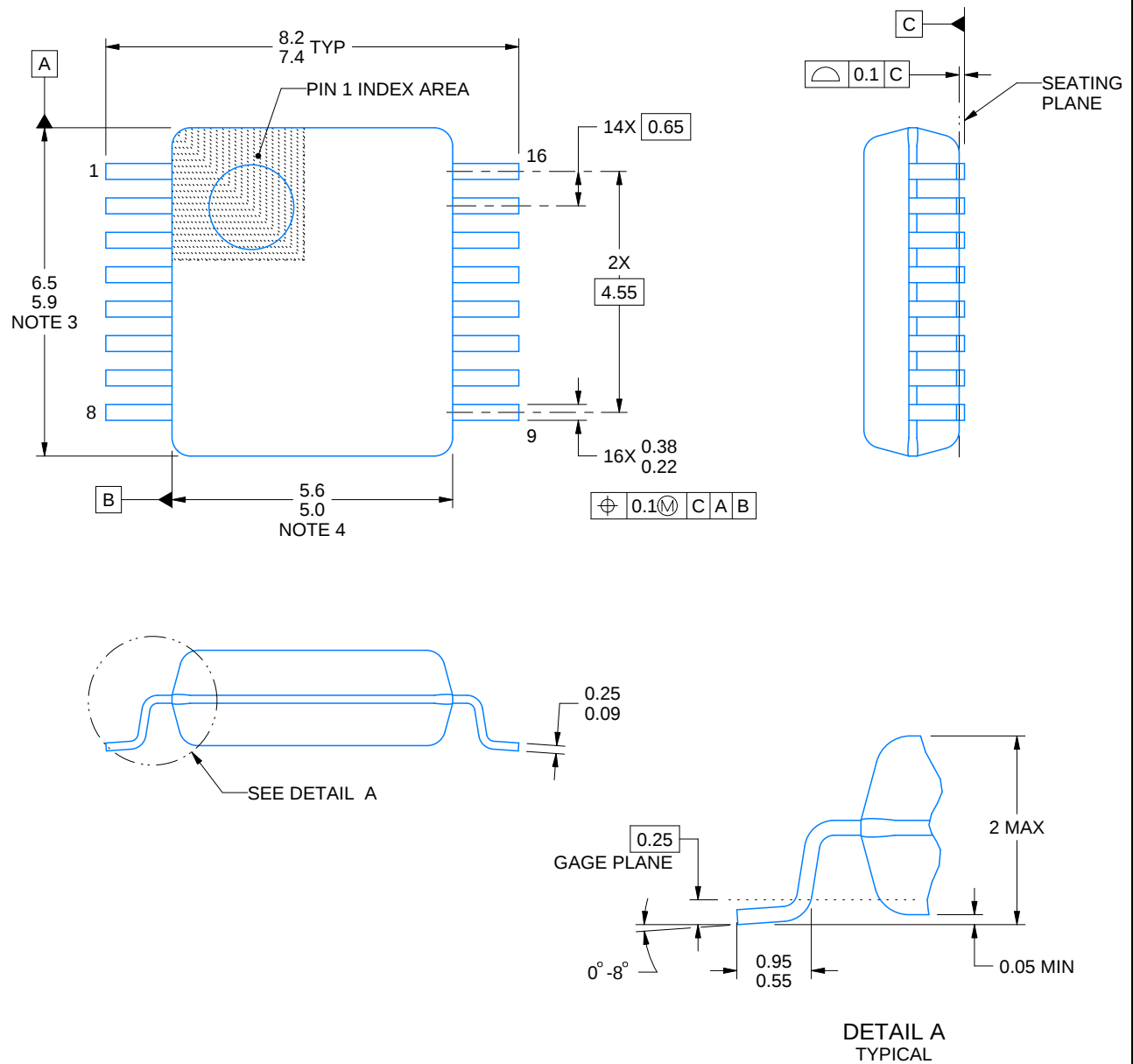


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220763/A 05/2022

NOTES:

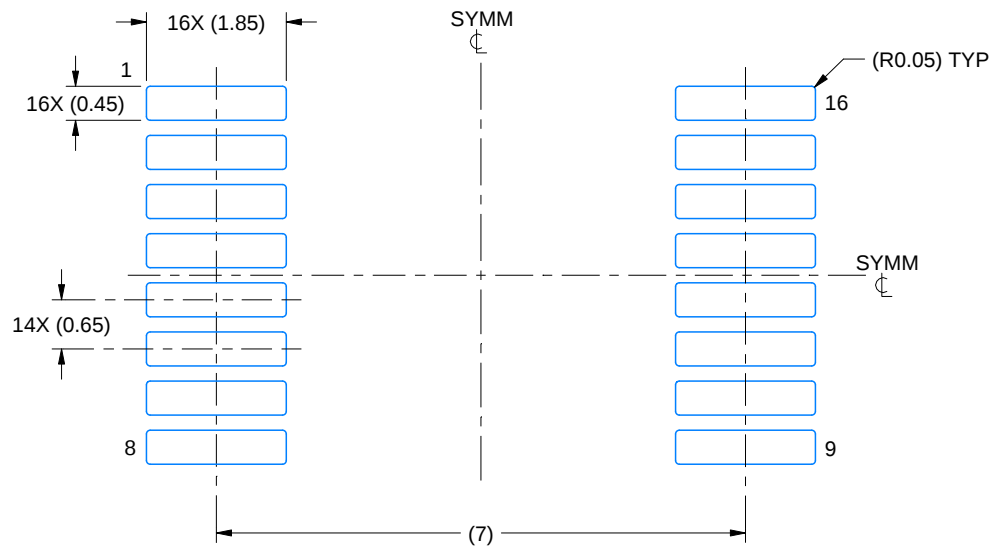
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

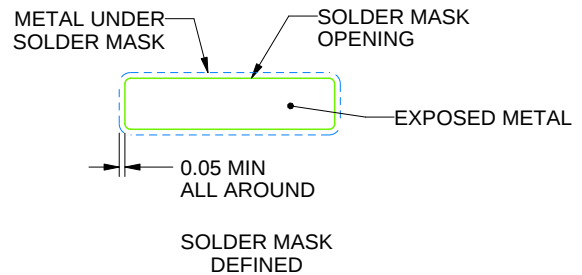
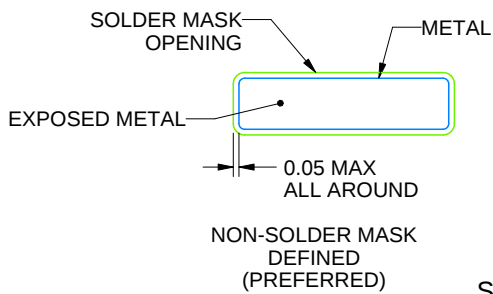
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

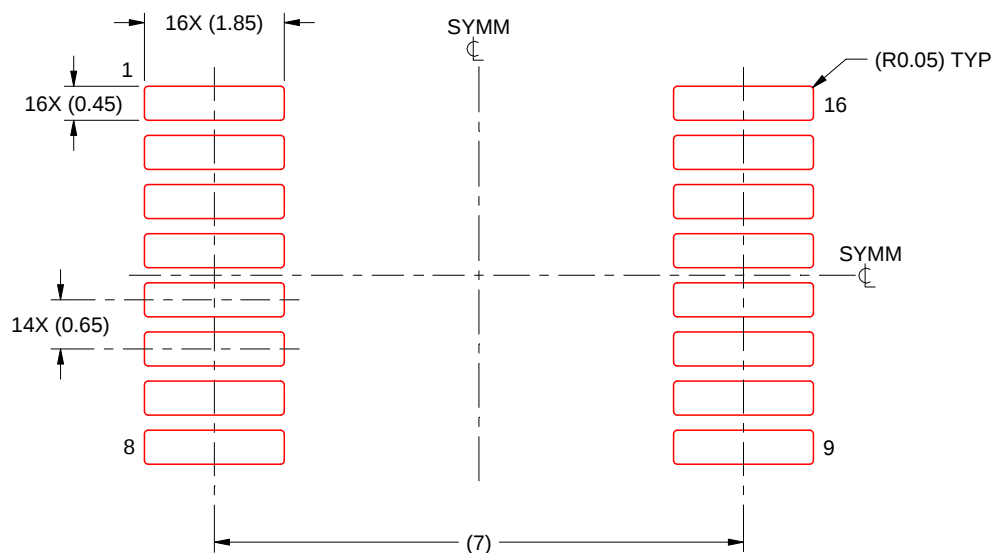
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

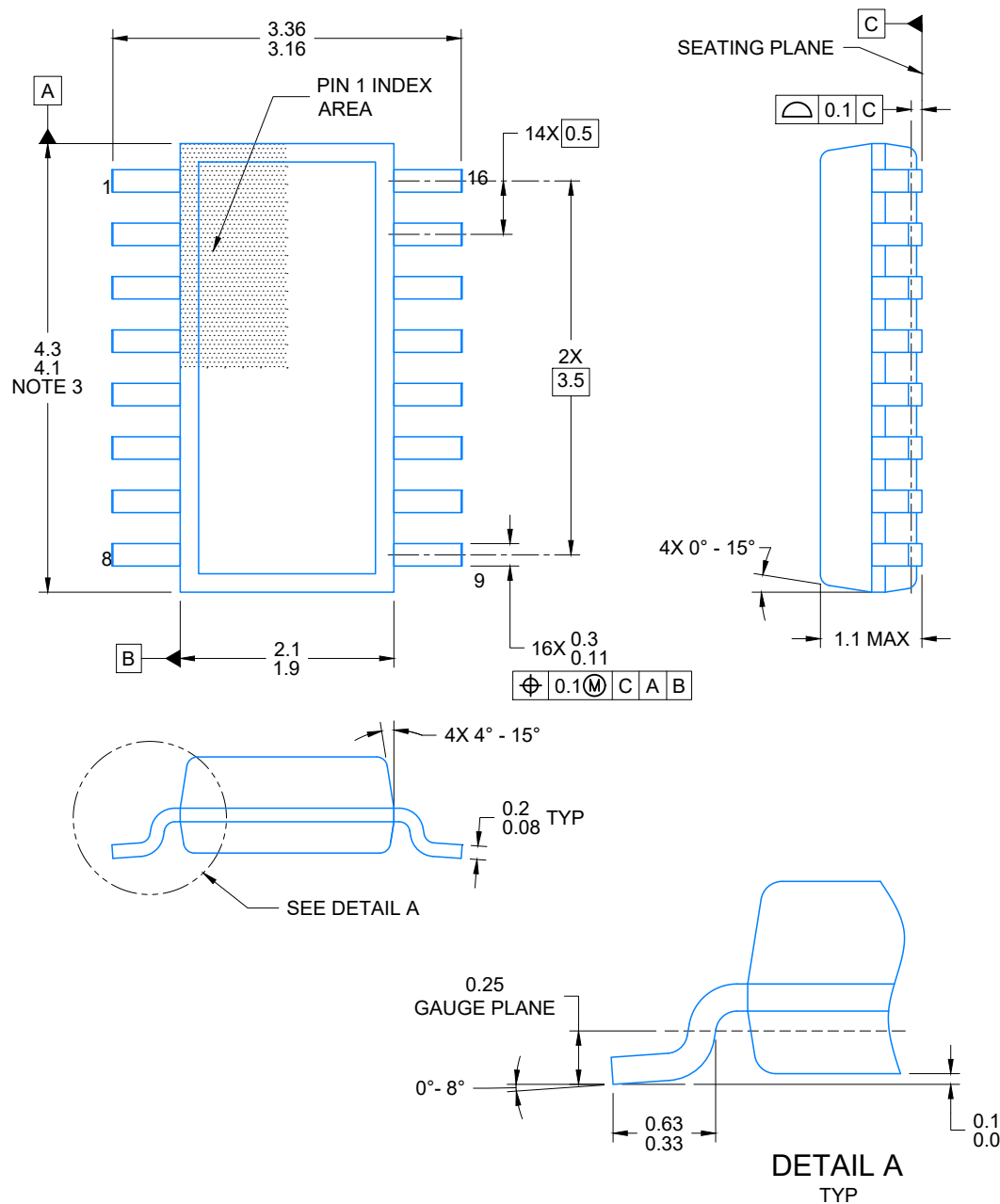


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

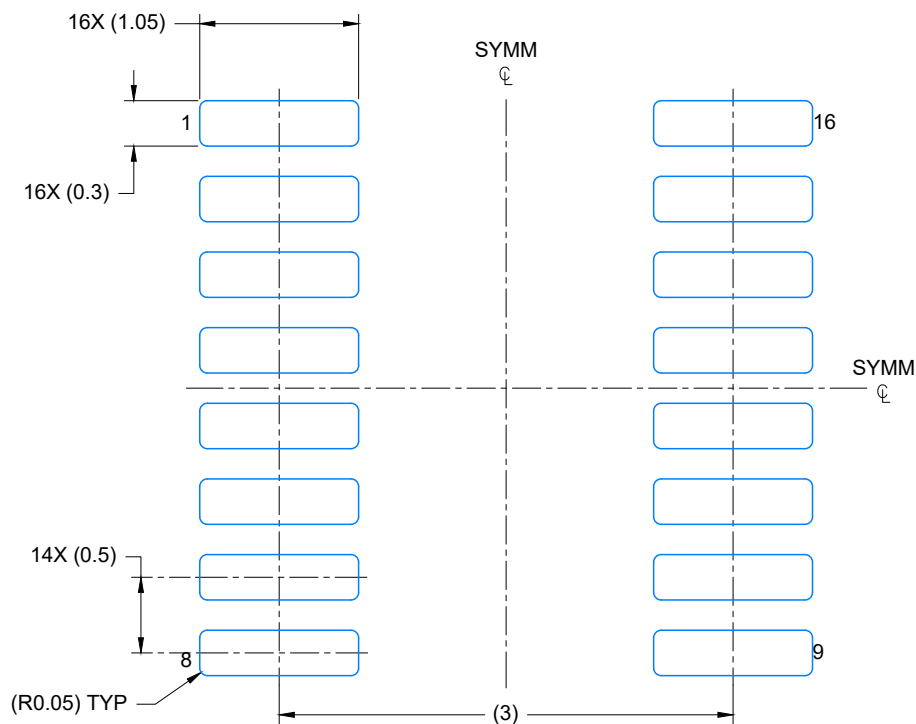
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



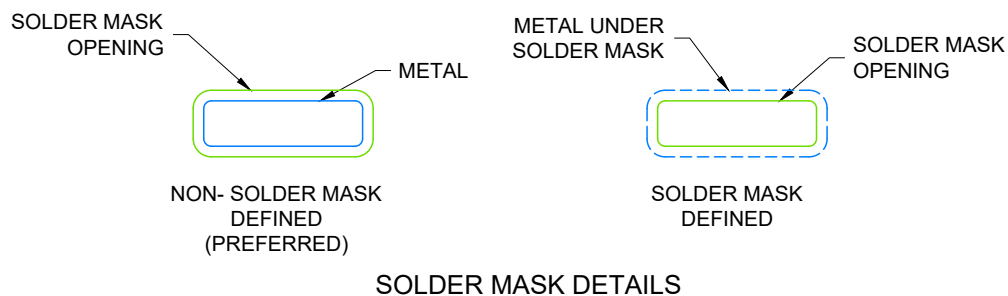
4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



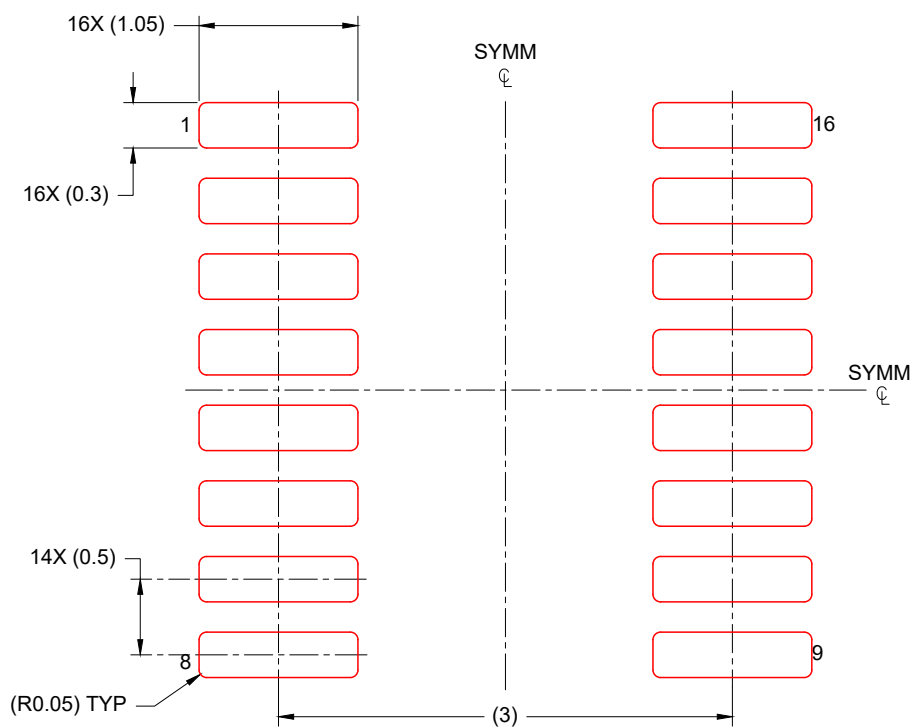
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224642/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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