

OPAx387 Ultra-High Precision, Zero-Drift, Low-Input-Bias-Current Op Amps

1 Features

- Ultra-low offset voltage: $\pm 2 \mu\text{V}$ (maximum, tested)
- Zero drift: $\pm 0.003 \mu\text{V}/^\circ\text{C}$
- Low-input bias current: 150 pA (maximum, tested)
- Low noise: $8.5 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz
- No 1/f noise: $177 \text{ nV}_{\text{PP}}$ (0.1 Hz to 10 Hz)
- Common-mode input range $\pm 100 \text{ mV}$ beyond supply rails
- Gain bandwidth: 5.7 MHz
- Quiescent current: 570 μA per amplifier
- Single supply: 1.7 V to 5.5 V
- Dual supply: $\pm 0.85 \text{ V}$ to $\pm 2.75 \text{ V}$
- EMI and RFI filtered inputs

2 Applications

- [Electronic thermometer](#)
- [Weigh scale](#)
- [Temperature transmitter](#)
- [Ventilators](#)
- [Data acquisition \(DAQ\)](#)
- [Semiconductor test](#)
- [Lab and field instrumentation](#)
- [Merchant network and server PSU](#)
- [Analog input module](#)
- [Pressure transmitter](#)

3 Description

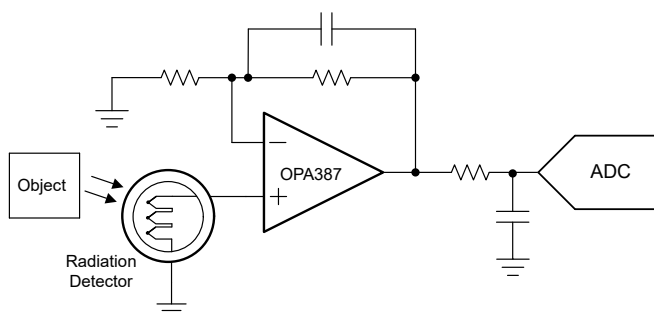
The OPA387, OPA2387, and OPA4387 (OPAx387) family of precision amplifiers offers state-of-the-art performance. With zero-drift technology, the OPAx387 offset voltage and offset drift provide unparalleled long-term stability. With a mere 570 μA of quiescent current, the OPAx387 are able to achieve 5.7 MHz of bandwidth, a broadband noise of $8.5 \text{ nV}/\sqrt{\text{Hz}}$, and a 1/f noise at $177 \text{ nV}_{\text{PP}}$. These specifications are crucial to achieve extremely-high precision and no degradation of linearity in 16-bit to 24-bit analog to digital converters (ADCs). The OPAx387 feature flat bias current over temperature; therefore, little to no calibration is needed in high input impedance applications over temperature.

All versions are specified over the industrial temperature range of -40°C to $+125^\circ\text{C}$.

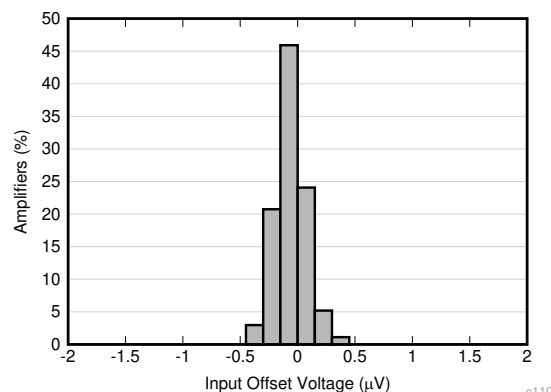
Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE ⁽¹⁾
OPA387	Single	DBV (SOT-23, 5)
OPA2387	Dual	D (SOIC, 8)
		DGK (VSSOP, 8)
		DSG (WSON, 8)
OPA4387	Quad	PW (TSSOP, 14)

- (1) For all available packages, see the package option addendum at the end of the data sheet.



The OPA387 as an Ultra-Low Offset, Low-Noise ADC Driver



Ultra-Low Input Offset Voltage

c110



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (February 2022) to Revision G (September 2023) Page

- Changed OPA2387 D (SOIC-8) package status from preview to production data (active) and added associated thermal information..... **1**
- Changed short-circuit current for OPA2387DGK at $V_S = 1.7\text{ V}$ from $\pm 25\text{ mA}$ to $\pm 15\text{ mA}$ **7**

Changes from Revision E (December 2021) to Revision F (February 2022) Page

- Added OPA2387 DSG (WSO8-8) package and associated content..... **1**

Changes from Revision D (October 2021) to Revision E (December 2021) Page

- Changed OPA4387 device from advanced information (preview) to production data (active)..... **1**

Changes from Revision C (October 2021) to Revision D (October 2021) Page

- Added OPA4387 advanced information (preview) device and associated content..... **1**
- Changed low-input bias current Features bullet from 135 pA to 150 pA..... **1**
- Deleted input offset voltage MAX values for over temperature and common-mode voltage test conditions for clarity..... **7**
- Added input offset voltage over temperature TYP value to represent performance shown in typical characteristics **7**
- Changed maximum input bias current for OPA387 and OPA2387 from 135 pA to 150 pA..... **7**
- Changed maximum input offset current for OPA387 and OPA2387 from 270 pA to 300 pA..... **7**
- Changed maximum open-loop voltage gain for OPA387 and OPA2387 from 132 dB to 135 dB..... **7**
- Changed settling time to 0.01% from 2.5 μs to 5.5 μs **7**
- Changed high linearity output swing from rail for $R_L = 2\text{ k}\Omega$ from 75 mV to 150 mV **7**
- Changed short-circuit current for OPA387 at $V_S = 1.7\text{ V}$ from $\pm 25\text{ mA}$ to $\pm 15\text{ mA}$ **7**
- Added open-loop output impedance at 1 MHz **7**
- Changed Figure 6-13, *PSRR and CMRR vs Frequency*, to fit to CMRR and PSRR specifications in the *Electrical Characteristic* table **9**
- Changed Figure 6-24, *Phase Margin vs Capacitive Load*, to add test condition..... **9**

5 Pin Configuration and Functions

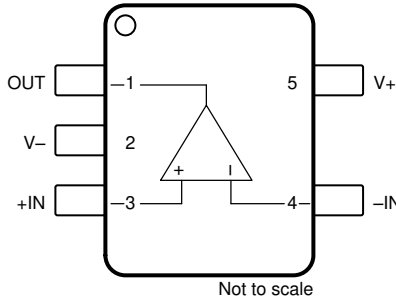


Figure 5-1. OPA387: DBV Package, 5-Pin SOT-23 (Top View)

Table 5-1. Pin Functions: OPA387

PIN		TYPE	DESCRIPTION
NAME	NO.		
-IN	4	Input	Inverting input
+IN	3	Input	Noninverting input
OUT	1	Output	Output
V-	2	Power	Negative (lowest) power supply
V+	5	Power	Positive (highest) power supply

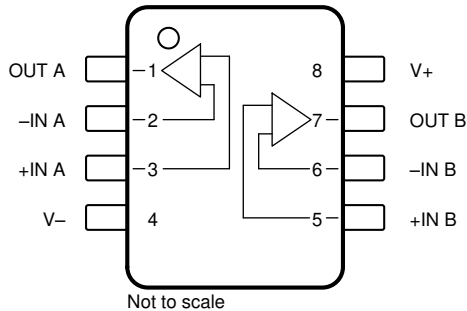


Figure 5-2. OPA2387: D Package, 8-Pin SOIC and DGK Package, 8-Pin VSSOP (Top View)

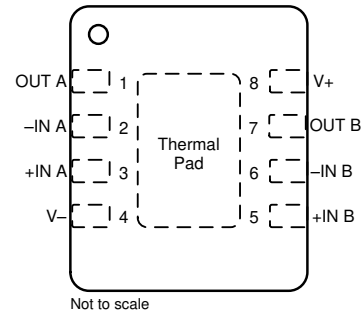


Figure 5-3. OPA2387: DSG Package, 8-Pin WSON With Exposed Thermal (Top View)

Table 5-2. Pin Functions: OPA2387

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SOIC), DGK (VSSOP)	DSG (WSON)		
–IN A	2	2	Input	Inverting input, channel A
–IN B	6	6	Input	Inverting input, channel B
+IN A	3	3	Input	Noninverting input, channel A
+IN B	5	5	Input	Noninverting input, channel B
OUT A	1	1	Output	Output, channel A
OUT B	7	7	Output	Output, channel B
V–	4	4	Power	Negative (lowest) power supply
V+	8	8	Power	Positive (highest) power supply
Thermal Pad	—	Thermal pad	—	Connect thermal pad to V–

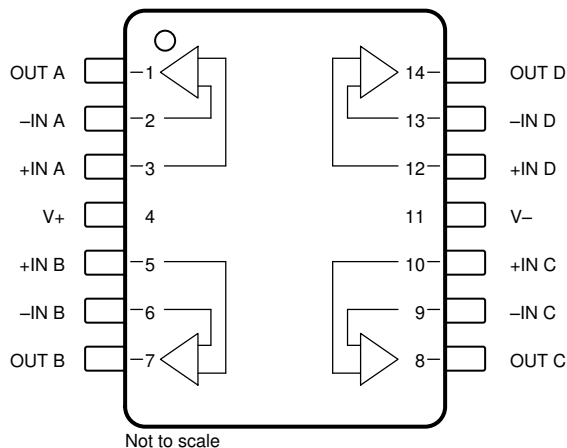


Figure 5-4. OPA4387: PW Package, 14-Pin TSSOP (Top View)

Table 5-3. Pin Functions: OPA4387

PIN		TYPE	DESCRIPTION
NAME	NO.		
-IN A	2	Input	Inverting input, channel A
-IN B	6	Input	Inverting input, channel B
-IN C	9	Input	Inverting input, channel C
-IN D	13	Input	Inverting input, channel D
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V-	11	Power	Negative (lowest) power supply
V+	4	Power	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _S	Supply voltage, V _S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
	Input voltage, all pins	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Input current, all pins			±10	mA
	Output short circuit ⁽²⁾		Continuous	Continuous	
T _A	Operating temperature		–55	150	°C
T _J	Junction temperature		–55	150	°C
T _{stg}	Storage temperature		–65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _S	Supply voltage, V _S = (V+) – (V–)	Single-supply	1.7		5.5	V
		Dual-supply	±0.85		±2.75	
T _A	Specified temperature		–40		125	°C

6.4 Thermal Information: OPA387

THERMAL METRIC ⁽¹⁾		OPA387	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	107.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information: OPA2387

THERMAL METRIC ⁽¹⁾		OPA2387			UNIT
		D (SOIC)	DGK (VSSOP)	DSG (WSON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.9	165	71.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.9	53	88.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.4	87	39.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	21.5	4.9	3.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.7	85	39.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	14.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Thermal Information: OPA4387

THERMAL METRIC ⁽¹⁾		OPA4387	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.7 Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_S = 1.7\text{ V}$ to 5.5 V , $V_{CM} = V_S / 2$, $V_{OUT} = V_S / 2$, and min and max specification established from manufacturing final test (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product			5.7			MHz
SR	Slew rate	4-V step, G = +1		2.8			V/μs
t _s	Settling time	To 0.1%, 1-V step , G = +1		1.5			μs
		To 0.01%, 1-V step , G = +1		5.5			
	Overload recovery time	V _{IN} × G > V _S		500			ns
	Chopping clock frequency ⁽¹⁾			100	150		kHz
THD+N	Total harmonic distortion + noise	V _{OUT} = 1 V _{RMS} , G = +1, f = 1 kHz		0.002 %			
OUTPUT							
	Voltage output swing from rail	No load	OPA387, OPA2387	1	10	mV	
			OPA4387		20		
		R _L = 2 kΩ			5		30
			OPA387, OPA2387	20	60		
			OPA4387		60		
			T _A = −40°C to +125°C ⁽¹⁾				30
	High linearity output swing range ⁽¹⁾	A _{OL} > 120 dB		(V−) + 0.075	(V+) − 0.075	V	
			R _L = 2 kΩ	(V−) + 0.150	(V+) − 0.150		
I _{sc}	Short-circuit current	V _S = 5.5 V		±55		mA	
		V _S = 1.7 V		±15			
	Phase margin	C _L = 100 pF, G = +1		40			degrees
R _O	Open-loop output impedance	f = 1 MHz		250			Ω
POWER SUPPLY							
I _Q	Quiescent current per amplifier	I _O = 0 mA		570	675	μA	
			T _A = −40°C to 125°C ⁽¹⁾		700		
	Turn-on time	At V _S = 5.5 V, V _S ramp rate > 0.3 V/μs, settle to 1%		25	100		μs

(1) Specification established from device population bench system measurements across multiple lots.

6.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.75\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 50\text{ pF}$ (unless otherwise noted)

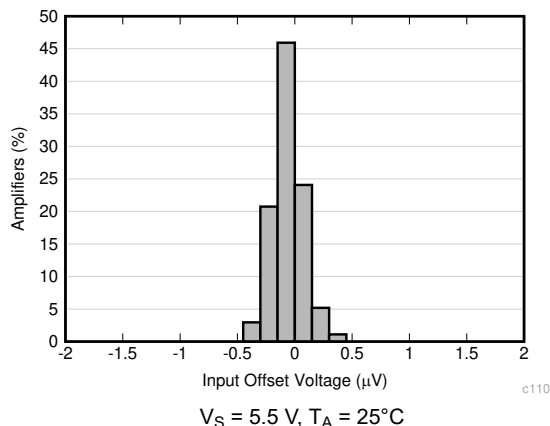


Figure 6-1. Offset Voltage Distribution

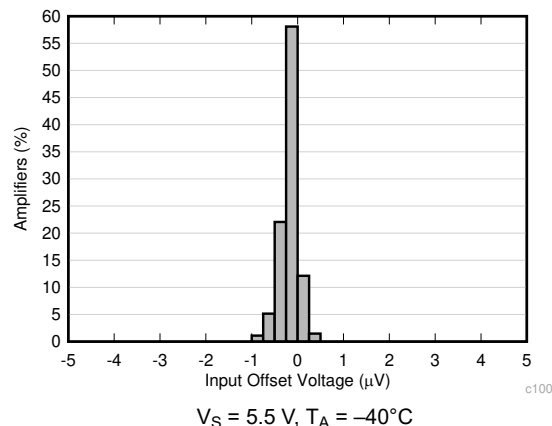


Figure 6-2. Offset Voltage Distribution

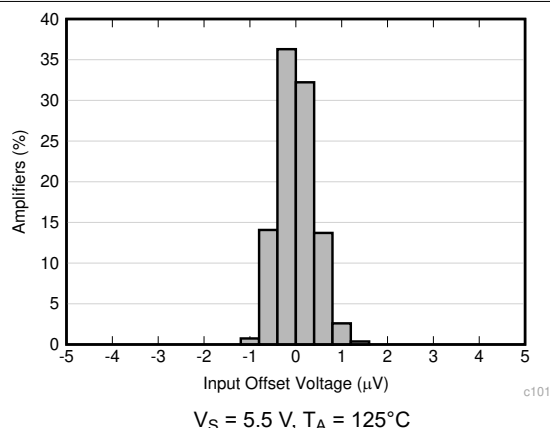


Figure 6-3. Offset Voltage Distribution

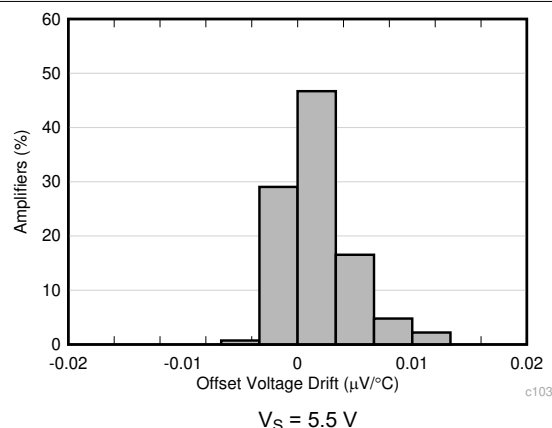


Figure 6-4. Offset Voltage Drift Distribution

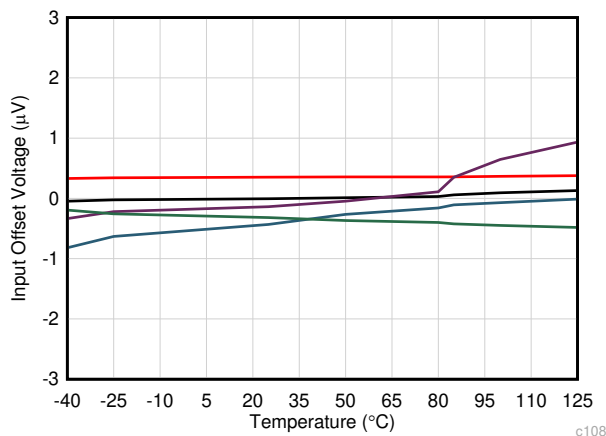


Figure 6-5. Offset Voltage vs Temperature

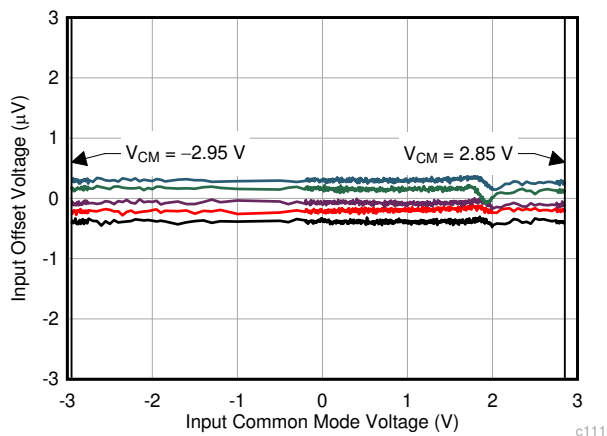


Figure 6-6. Offset Voltage vs Common-Mode Voltage

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.75\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 50\text{ pF}$ (unless otherwise noted)

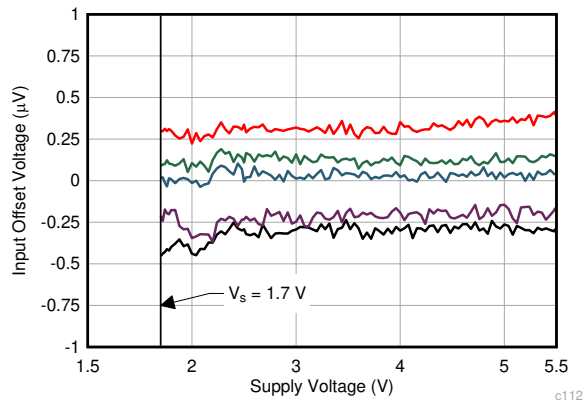


Figure 6-7. Offset Voltage vs Supply Voltage

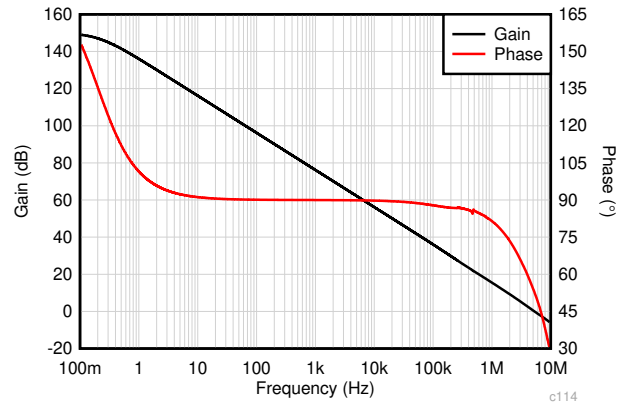


Figure 6-8. Open-Loop Gain and Phase vs Frequency

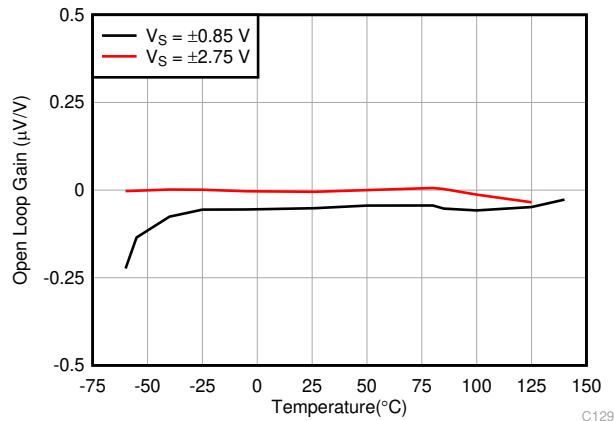


Figure 6-9. Open-Loop Gain vs Temperature

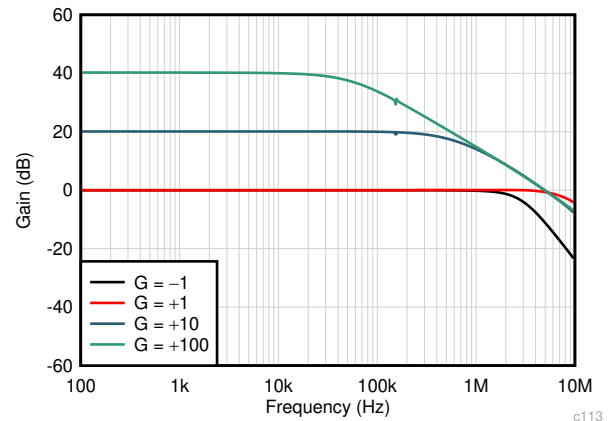


Figure 6-10. Closed-Loop Gain vs Frequency

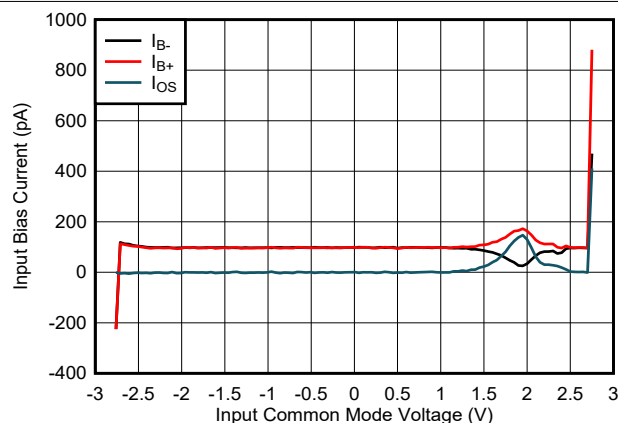


Figure 6-11. Input Bias Current vs Common-Mode Voltage

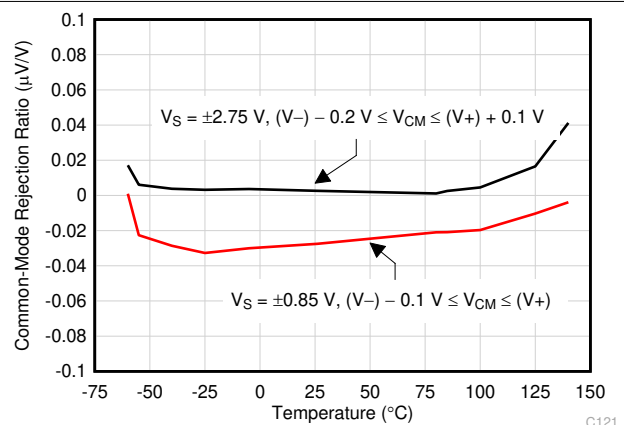


Figure 6-12. CMRR vs Temperature

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.75\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 50\text{ pF}$ (unless otherwise noted)

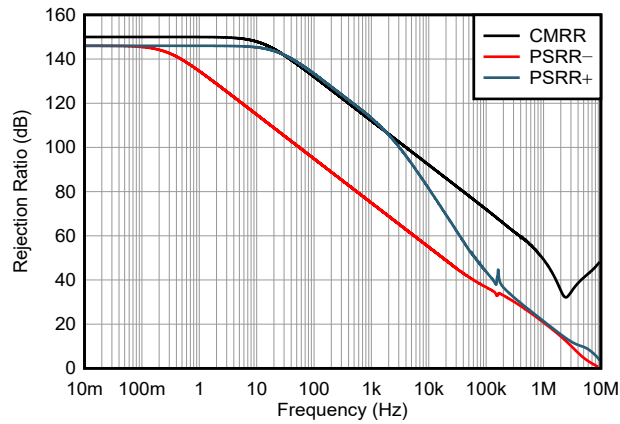


Figure 6-13. PSRR and CMRR vs Frequency

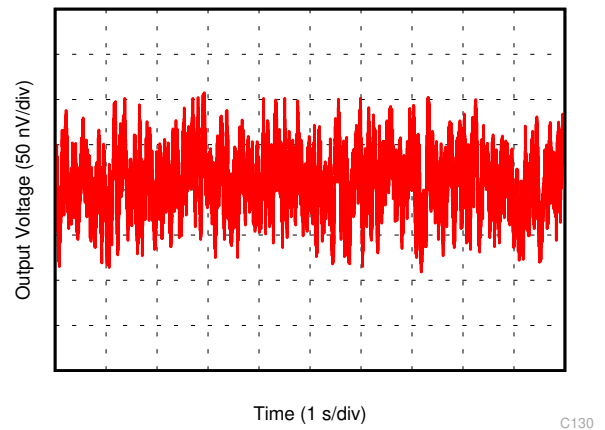


Figure 6-14. 0.1-Hz to 10-Hz Noise

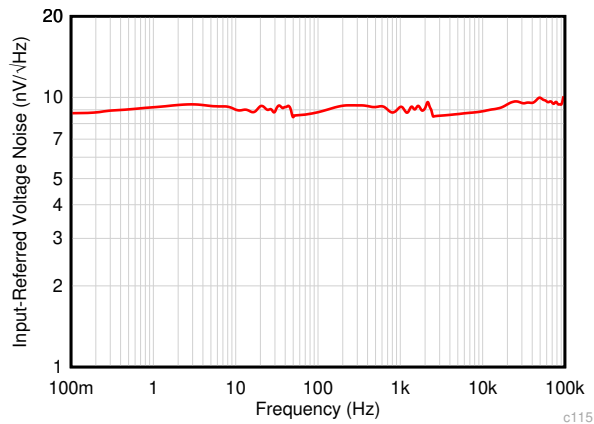


Figure 6-15. Input Voltage Noise Spectral Density vs Frequency

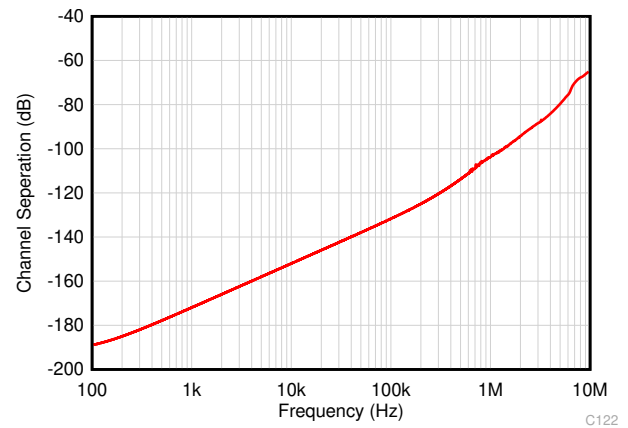


Figure 6-16. Channel-to-Channel Crosstalk

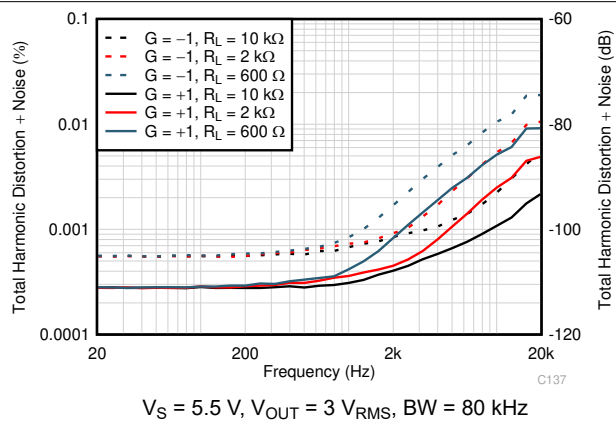


Figure 6-17. THD+N Ratio vs Frequency

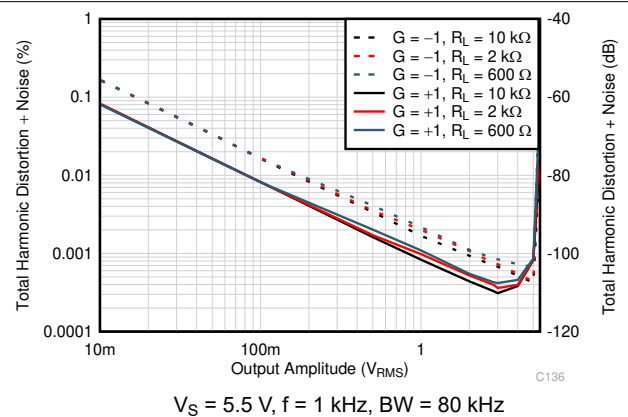


Figure 6-18. THD+N vs Output Amplitude

6.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.75\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 50\text{ pF}$ (unless otherwise noted)

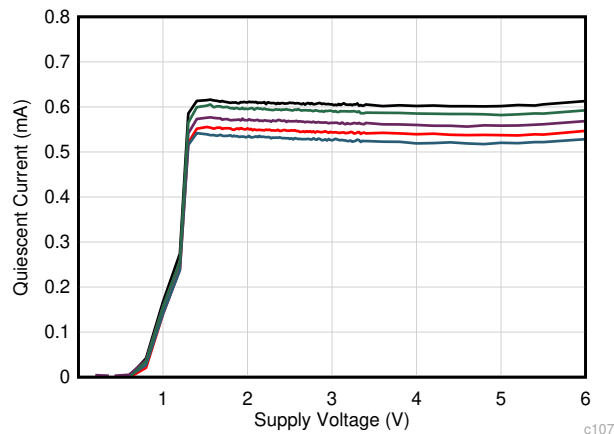


Figure 6-19. Quiescent Current vs Supply Voltage

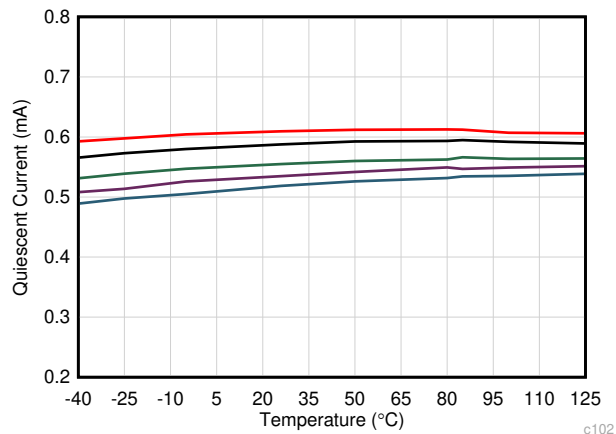


Figure 6-20. Quiescent Current vs Temperature

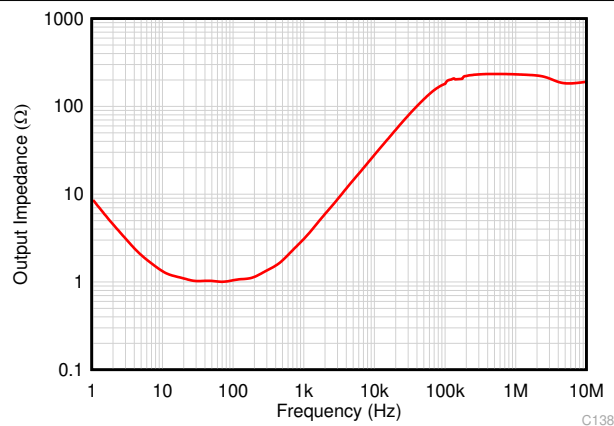


Figure 6-21. Open-Loop Output Impedance vs Frequency

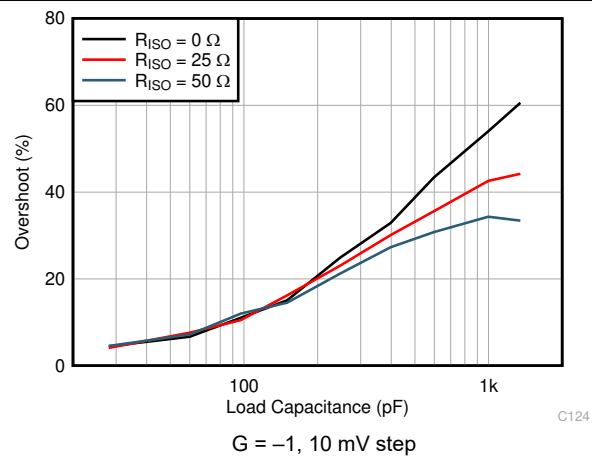


Figure 6-22. Small-Signal Overshoot vs Capacitive Load

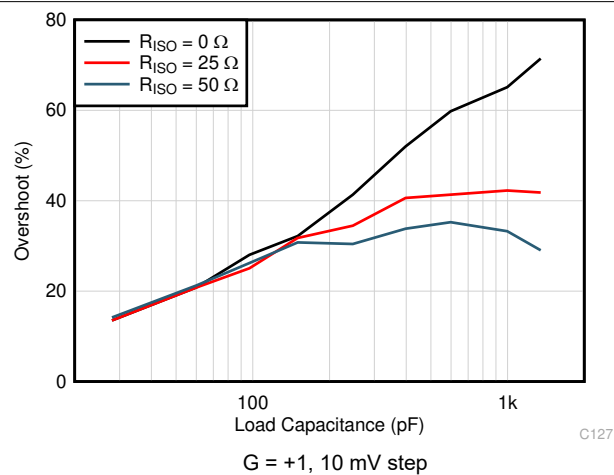


Figure 6-23. Small-Signal Overshoot vs Capacitive Load

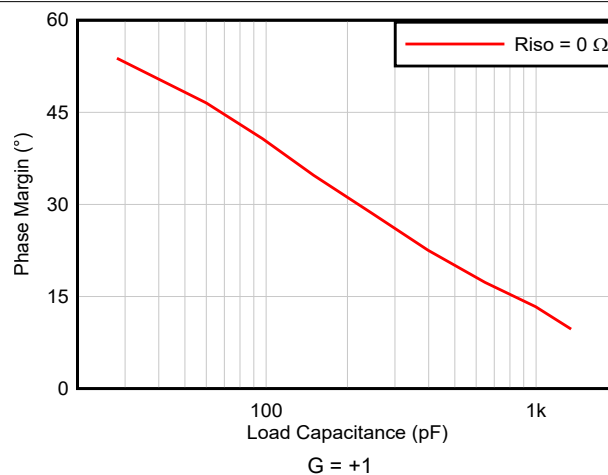
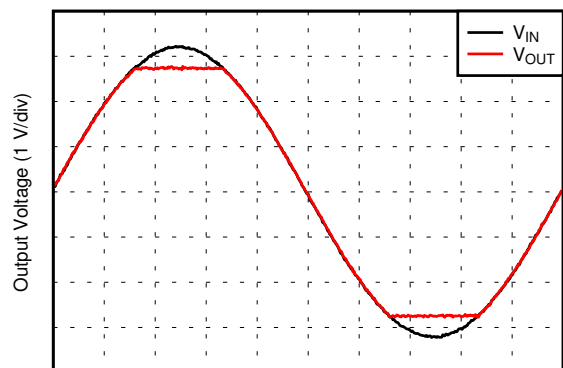


Figure 6-24. Phase Margin vs Capacitive Load

6.8 Typical Characteristics (continued)

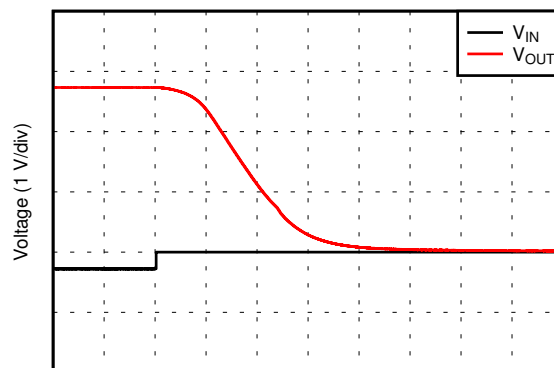
at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.75\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 50\text{ pF}$ (unless otherwise noted)



Time (100 $\mu\text{s}/\text{div}$)

C125

Figure 6-25. No Phase Reversal

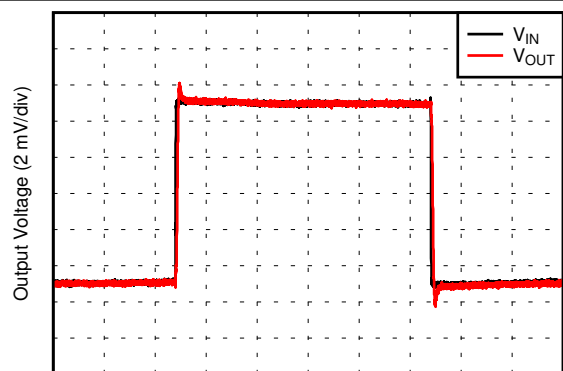


Time (500 ns/div)

C133

$G = -1$

Figure 6-26. Overload Recovery

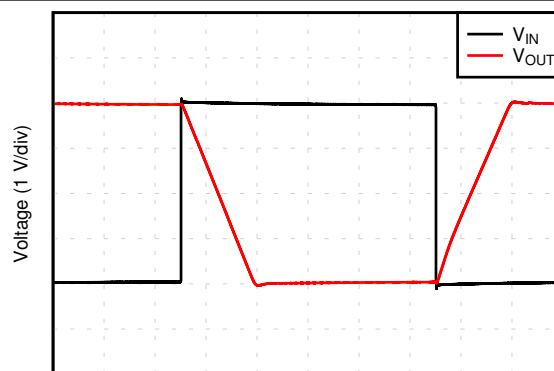


Time (1 $\mu\text{s}/\text{div}$)

C128

$G = +1$

Figure 6-27. Small-Signal Step Response

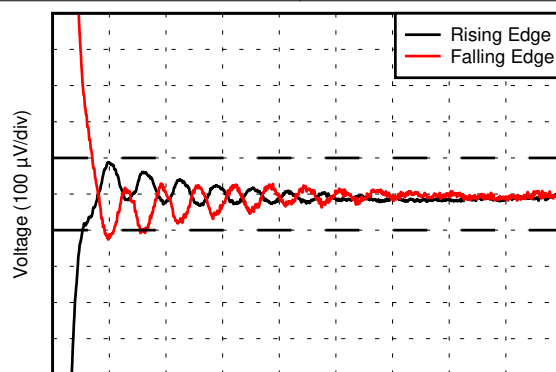


Time (1 $\mu\text{s}/\text{div}$)

C105

4-V step

Figure 6-28. Large-Signal Step Response



Time (10 $\mu\text{s}/\text{div}$)

C135

0.01% settling = $\pm 100\text{ }\mu\text{V}$

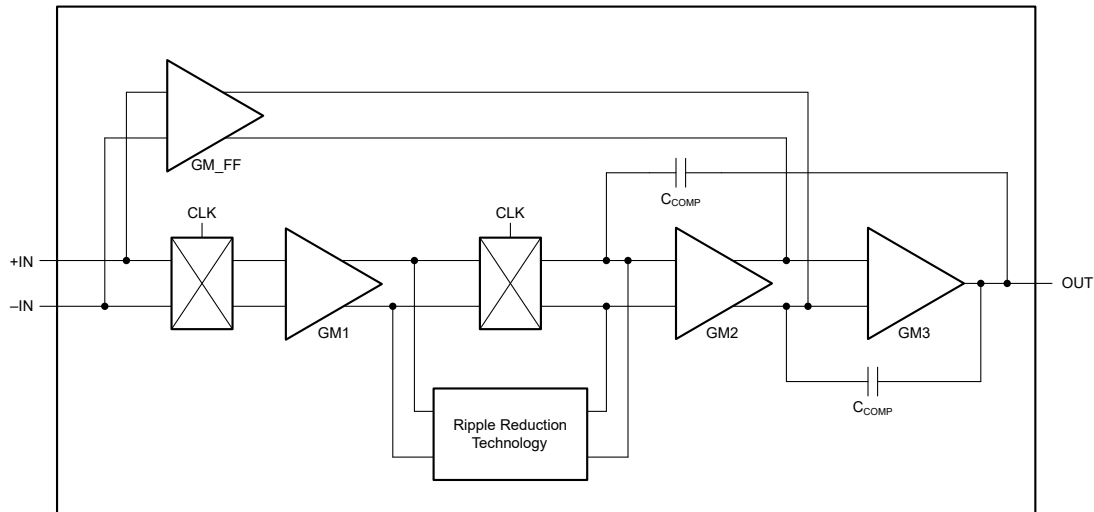
Figure 6-29. Settling Time

7 Detailed Description

7.1 Overview

The OPAx387 family of zero-drift amplifiers is engineered with state-of-the-art, proprietary, precision zero-drift technology. These amplifiers offer ultra-low input offset voltage and drift, and achieve excellent input and output dynamic linearity. The OPAx387 operate from 1.7 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose and precision applications. The OPAx387 strengths also include a 5.7-MHz bandwidth, $8.5\text{-nV}/\sqrt{\text{Hz}}$ noise spectral density, and no $1/f$ noise, making the OPAx387 an excellent choice for interfacing with sensor modules, and buffering high-fidelity, digital-to-analog converters (DACs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Bias Current

During normal operation, the typical input bias current of the OPAx387 is 30 pA. The device exhibits low drift over the full temperature range of -40°C to $+125^{\circ}\text{C}$. There are no antiparallel diodes between the input pins (+IN and -IN); therefore, the differential input maximum voltage is limited only by diodes connected to the supply voltage pins. However, use caution in cases where the input differential voltage exceeds the nominal operating input differential voltage. When inputs are separated, the switching offset-cancellation path internal to the amplifier exceeds normal operating conditions, and can potentially create long settling behavior upon return to normal operation. The equivalent input circuit of OPAx387 is shown in Figure 7-1.

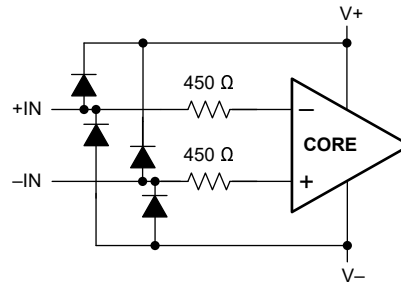


Figure 7-1. Equivalent Input Circuit

7.3.2 EMI Susceptibility and Input Filtering

Operational amplifiers can exhibit sensitivity to electromagnetic interference (EMI). Typically, conducted EMI (that is, EMI that enters the device through conduction) is more commonly observed than radiated EMI (that is, EMI that enters the device through radiation). When conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from the nominal value. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx387 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. The conducted EMI rejection of the OPAx387 is seen in Figure 7-2.

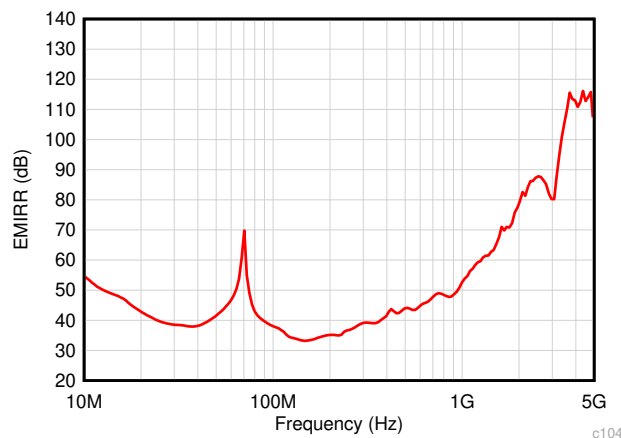


Figure 7-2. EMI Rejection Ratio

7.4 Device Functional Modes

The OPAx387 have a single functional mode and are operational when the power-supply voltage is greater than 1.7 V (± 0.85 V). The maximum specified power-supply voltage for the OPAx387 is 5.5 V (± 2.75 V).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx387 are unity-gain stable, precision, operational amplifiers featuring state-of-the-art, zero-drift technology. The use of proprietary zero-drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lower 1/f noise component. As a result of the high PSRR, the devices work well in applications that run directly from battery power without regulation. The OPAx387 family is optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies without input crossover distortion, and a rail-to-rail output that swings within 5 mV of the supplies under normal test conditions. The OPAx387 precision amplifiers are designed for upstream analog signal-chain applications in low or high gains, as well as downstream signal-chain functions, such as DAC buffering.

8.1.1 Zero-Drift Clocking

The OPAx387 use an advanced zero-drift architecture to achieve ultra-low offset and offset drift. This architecture uses a clock and switches internally to create a dc error-correction path. The clocking is filtered internally, and typically not observable for most configurations. Take the following precautions to minimize clock noise in the signal chain. The clocking creates a small charge-injection pulse at the input of the amplifier; therefore, do not use high-value resistors ($> 100\text{ k}\Omega$) in series with the inputs to avoid higher clock voltage noise at the output. The charge injection pulses are minimized when the impedance to the input pins is matched. If higher value resistors are used, then use matching impedances on both amplifier input pins.

8.2 Typical Applications

8.2.1 Bidirectional Current Sensing

This single-supply, low-side, bidirectional current-sensing design example detects load currents from -1 A to $+1\text{ A}$. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPAx387 because of the device low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage. [Figure 8-1](#) shows the design example schematic.

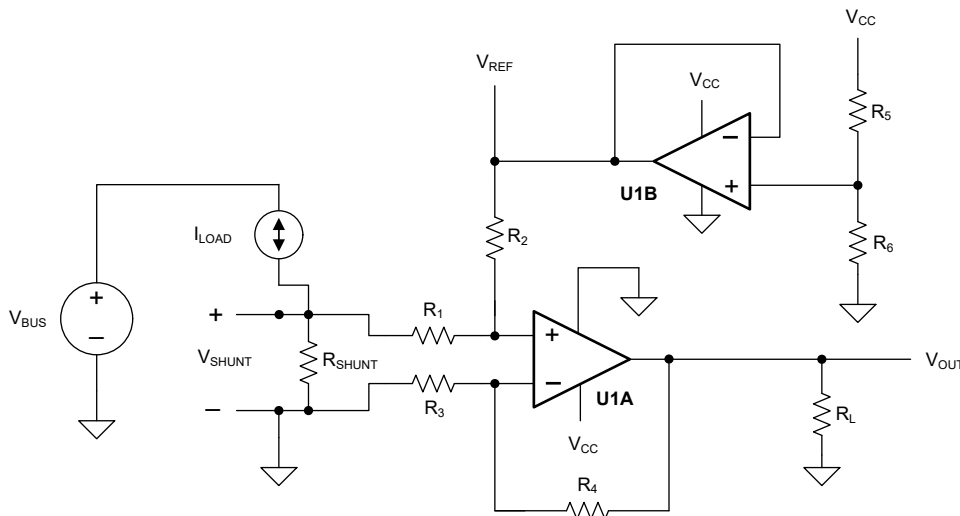


Figure 8-1. Bidirectional Current-Sensing Schematic

8.2.1.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to +1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

8.2.1.2 Detailed Design Procedure

The load current, I_{LOAD} , flows through the shunt resistor, R_{SHUNT} , to develop the shunt voltage, V_{SHUNT} . The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4 . The gain of the difference amplifier is set by the ratio of R_4 to R_3 . To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF} , is supplied by buffering a resistor divider using U1B. The transfer function is given by [Equation 1](#).

$$V_{OUT} = V_{SHUNT} \times \text{Gain}_{\text{Diff_Amp}} + V_{REF} \quad (1)$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $\text{Gain}_{\text{Diff_Amp}} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6} \right)$

There are two types of errors in this design: gain and offset. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1 . Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4 / R_3 matches R_2 / R_1 . The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT} . In this design, the maximum value for V_{SHUNT} is set to 100 mV. [Equation 2](#) calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(\text{Max})} = \frac{V_{SHUNT(\text{Max})}}{I_{LOAD(\text{Max})}} = \frac{100 \text{ mV}}{1 \text{ A}} = 100 \text{ m}\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% is selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100 mV to +100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Make sure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Use an operational amplifier, such as the OPAx387, that has a common-mode range that extends below the negative supply voltage. The offset error is minimal because the OPAx387 has a typical offset voltage of merely ±0.25 µV (±5 µV, maximum).

Given a symmetric load current of –1 A to +1 A, the voltage divider resistors, R_5 and R_6 , must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% is selected. To minimize power consumption, 10-kΩ resistors are used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPAx387 must be considered. [Equation 3](#) and [Equation 4](#) depict the typical common-mode range and maximum output swing, respectively, of the OPAx387 given a 3.3-V supply.

$$-100 \text{ mV} < V_{CM} < 3.4 \text{ V} \quad (3)$$

$$100 \text{ mV} < V_{OUT} < 3.2 \text{ V} \quad (4)$$

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$\text{Gain}_{\text{Diff_Amp}} = \frac{V_{\text{OUT_Max}} - V_{\text{OUT_Min}}}{R_{\text{SHUNT}} \times (I_{\text{MAX}} - I_{\text{MIN}})} = \frac{3.2 \text{ V} - 100 \text{ mV}}{100 \text{ m}\Omega \times [1 \text{ A} - (-1 \text{ A})]} = 15.5 \frac{\text{V}}{\text{V}} \quad (5)$$

The resistor value selected for R_1 and R_3 is 1 k Ω . 15.4 k Ω is selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4 . As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

8.2.1.3 Application Curve

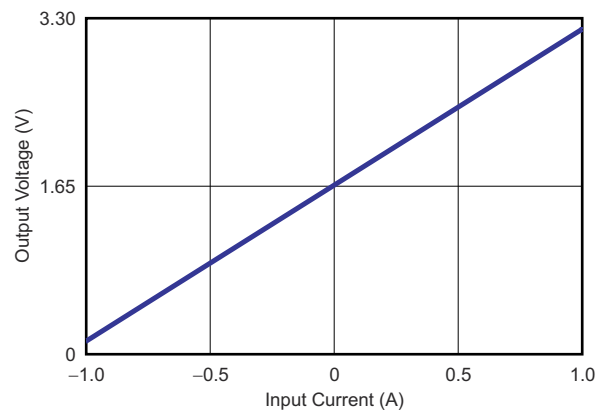


Figure 8-2. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

8.2.2 Load Cell Measurement

Figure 8-3 shows the OPAx387 in a high-CMRR dual-op amp instrumentation amplifier with a trim resistor and six-wire load cell for precision measurement.

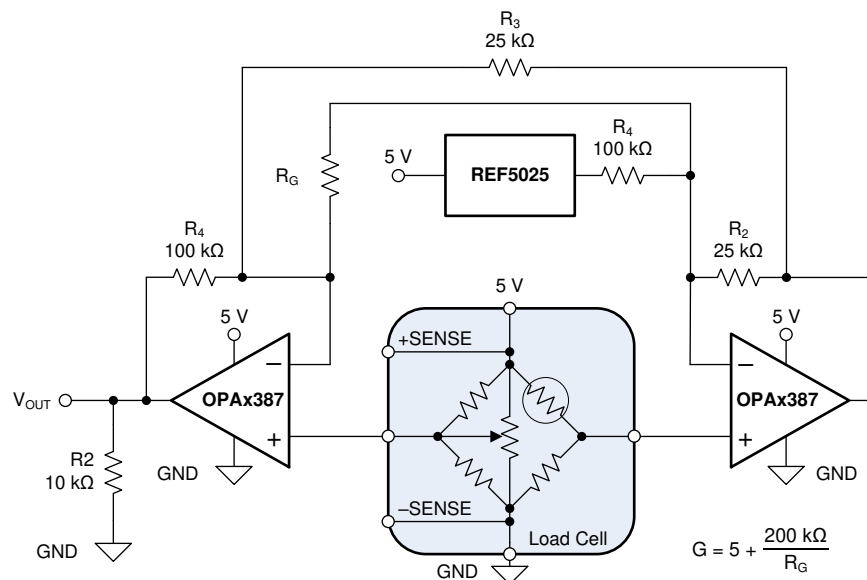


Figure 8-3. Load Cell Measurement Schematic

8.3 Power Supply Recommendations

The OPAx387 family of devices is specified for operation from 1.7 V to 5.5 V for single supplies, and ± 0.85 V to ± 2.75 V for dual supplies. Key parameters that can exhibit significant variance with regard to operating voltage are presented in [Section 6.8](#).

CAUTION

Supply voltages greater than 6 V can permanently damage the device (see [Section 6.1](#)).

8.4 Layout

8.4.1 Layout Guidelines

Pay attention to good layout practice. Keep traces short and, when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1- μ F capacitor close to the supply pins. These guidelines must be applied throughout the analog circuit to improve performance, and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by making sure that the potentials are equal on both input pins. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Follow these guidelines to reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 μ V/ $^{\circ}$ C or higher depending on materials used.

8.4.2 Layout Example

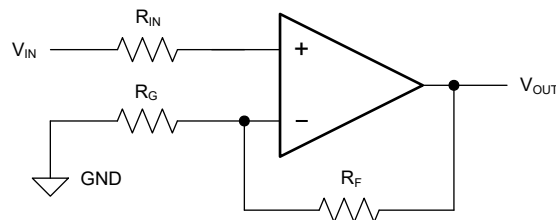


Figure 8-4. Schematic Representation

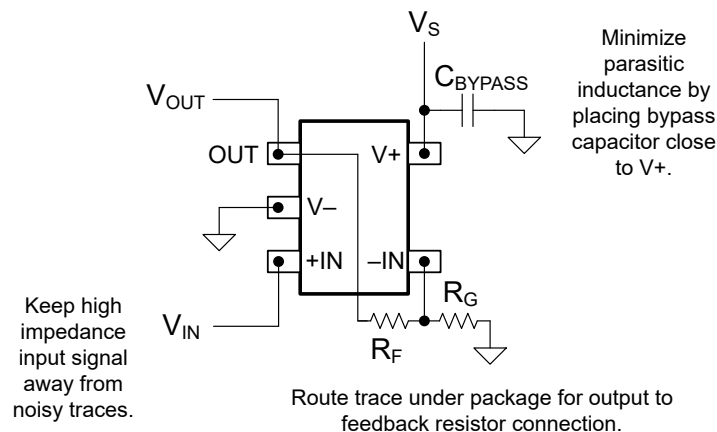


Figure 8-5. Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the [Design tools and simulation](#) web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the [TINA-TI™ software folder](#).

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following: Texas Instruments, [Circuit board layout techniques](#)

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on [Subscribe to updates](#) to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2387DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2B2T
OPA2387DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2B2T
OPA2387DGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2B2T
OPA2387DGKT.A	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2B2T
OPA2387DR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OP2387
OPA2387DR.A	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OP2387
OPA2387DSGR	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2N3H
OPA2387DSGR.A	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2N3H
OPA2387DSGT	Active	Production	WSON (DSG) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2N3H
OPA2387DSGT.A	Active	Production	WSON (DSG) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2N3H
OPA387DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2IMT
OPA387DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2IMT
OPA387DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2IMT
OPA387DBVT.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2IMT
OPA4387PWR	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA4387
OPA4387PWR.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA4387
OPA4387PWT	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA4387
OPA4387PWT.A	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA4387

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

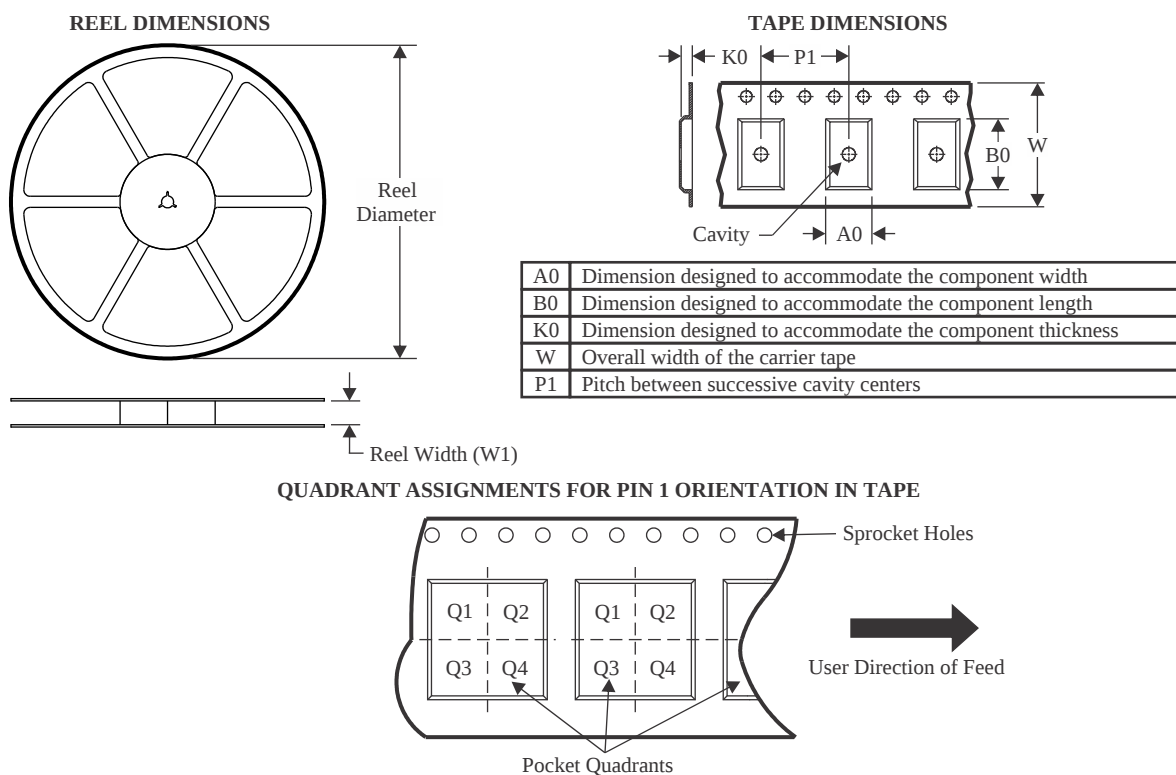
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

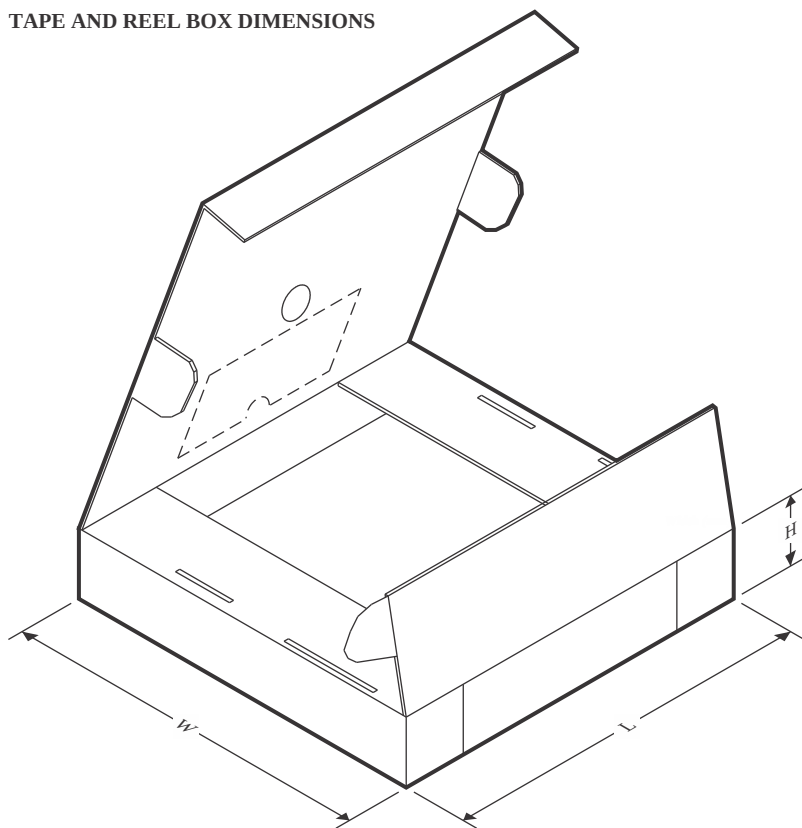
TAPE AND REEL INFORMATION



*All dimensions are nominal

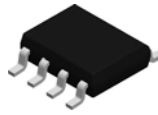
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2387DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2387DGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2387DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2387DSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2387DSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA387DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA387DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA4387PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4387PWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2387DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2387DGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2387DR	SOIC	D	8	3000	356.0	356.0	35.0
OPA2387DSGR	WSO	DSG	8	3000	210.0	185.0	35.0
OPA2387DSGT	WSO	DSG	8	250	210.0	185.0	35.0
OPA387DBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
OPA387DBVT	SOT-23	DBV	5	250	190.0	190.0	30.0
OPA4387PWR	TSSOP	PW	14	3000	356.0	356.0	35.0
OPA4387PWT	TSSOP	PW	14	250	210.0	185.0	35.0

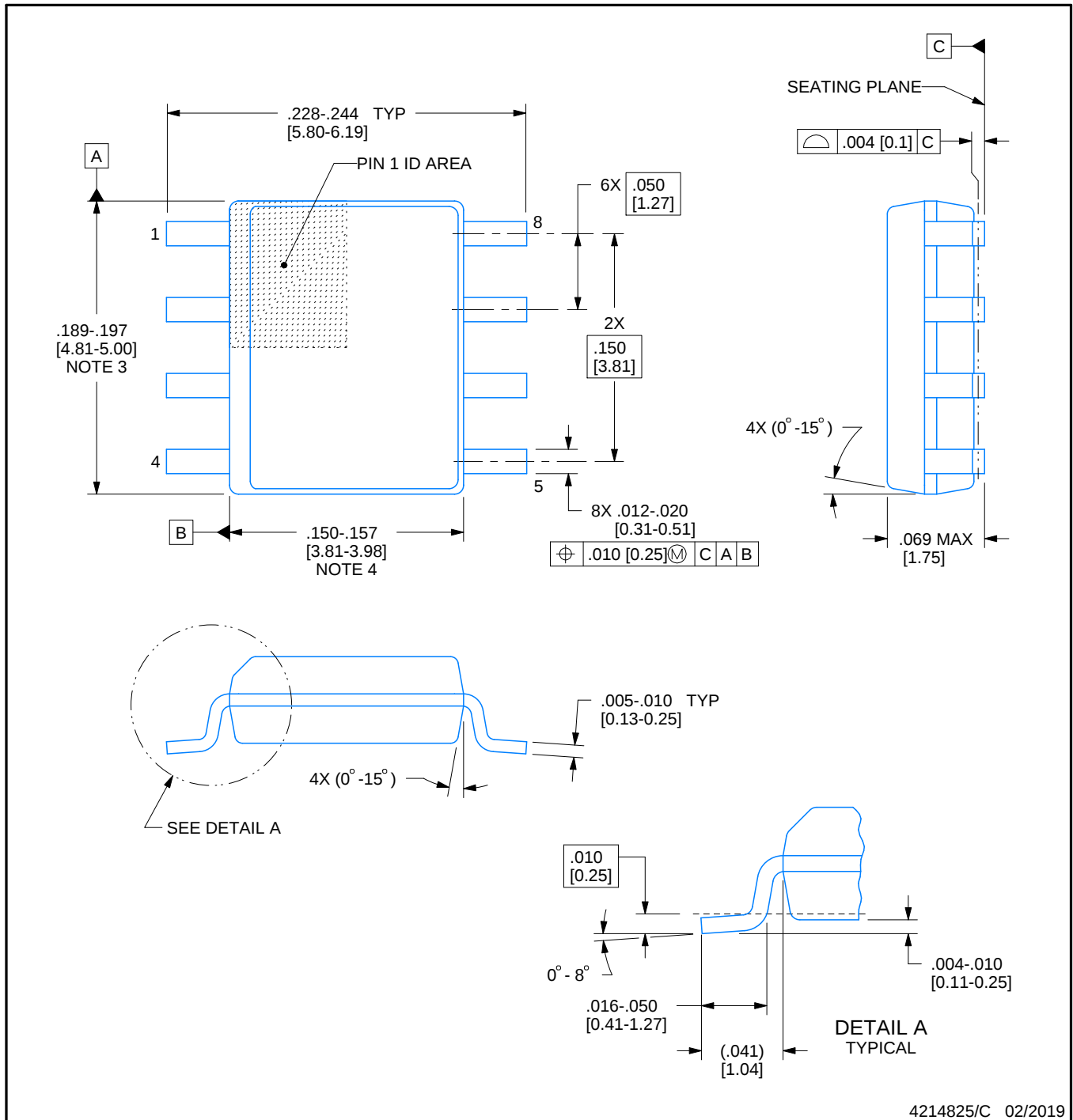


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

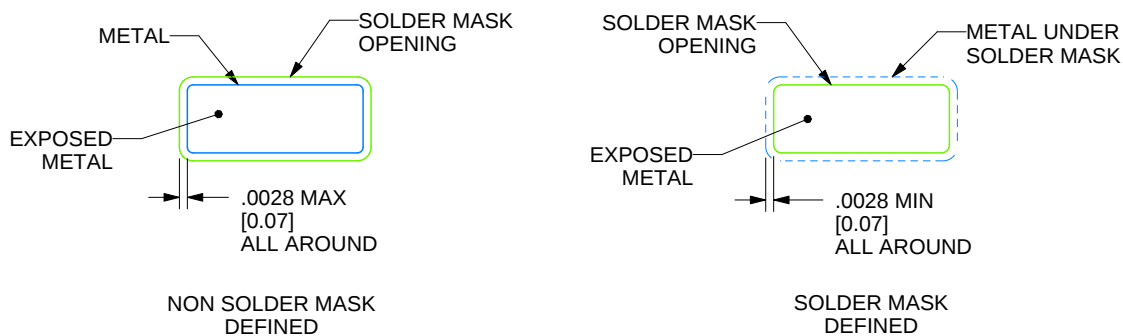
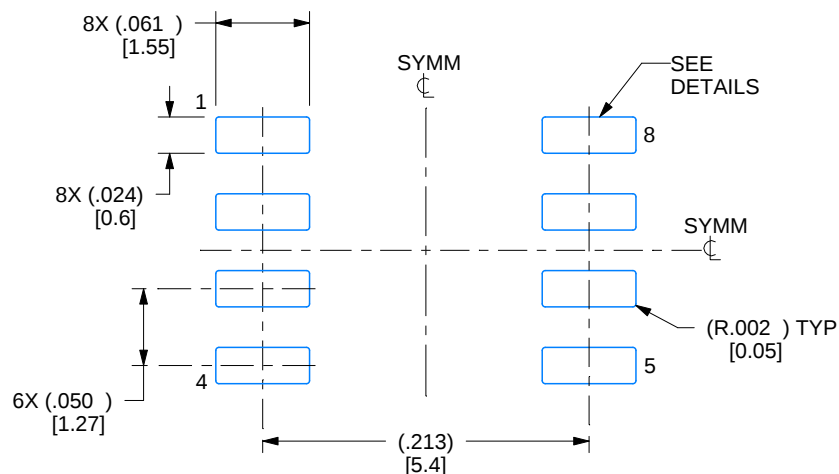
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

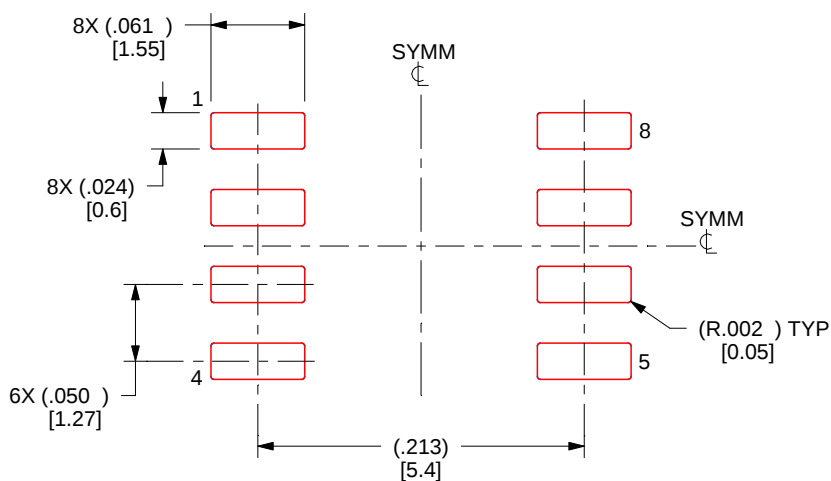
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

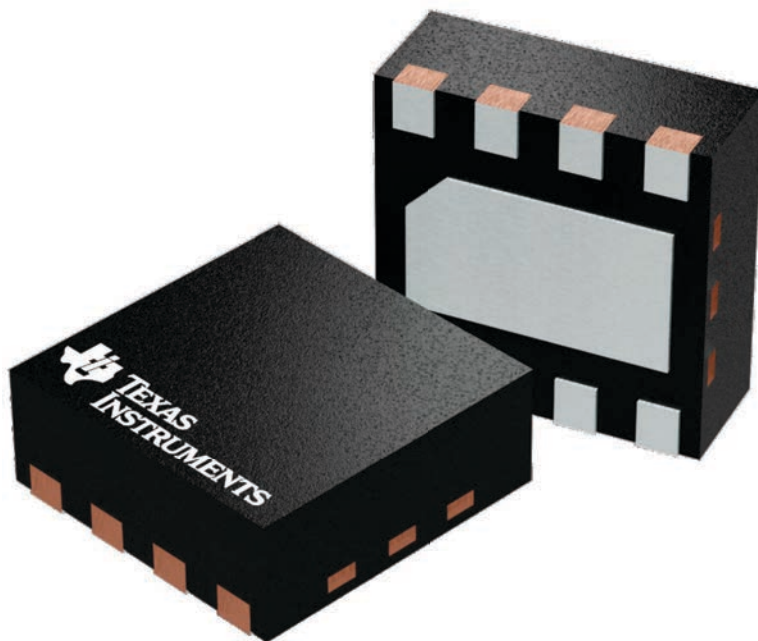
DSG 8

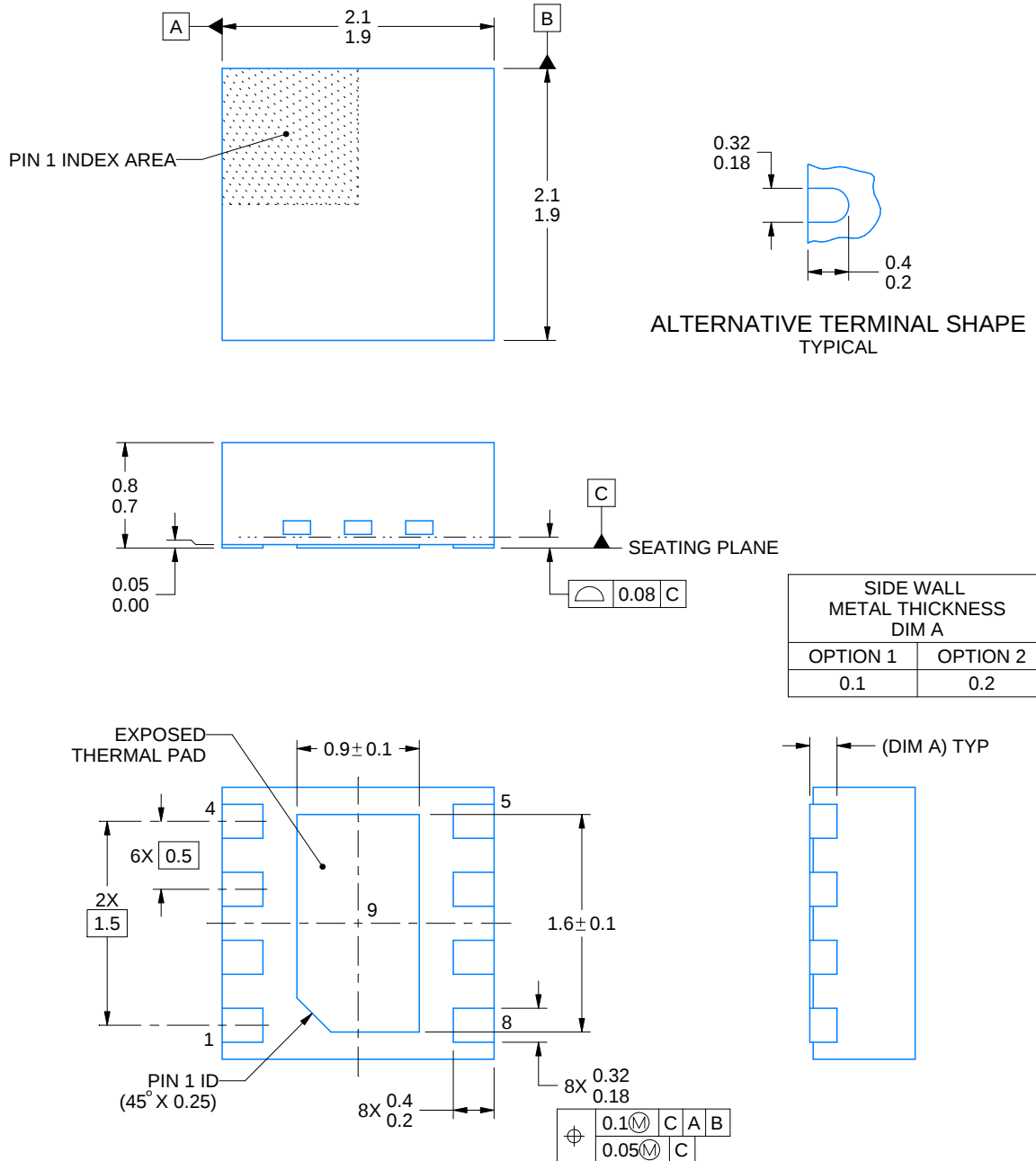
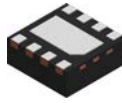
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4218900/E 08/2022

NOTES:

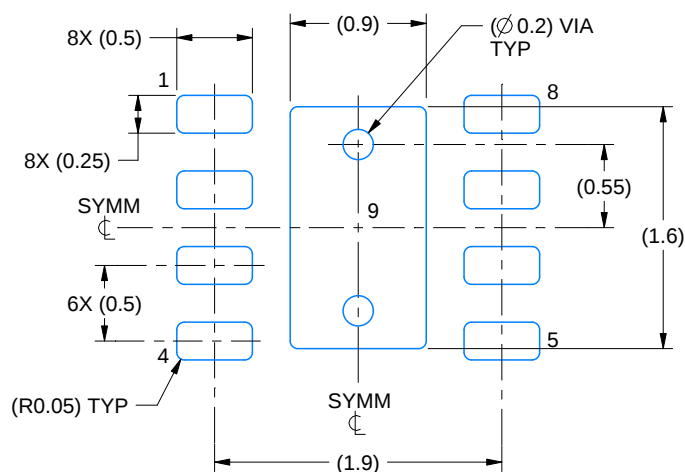
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

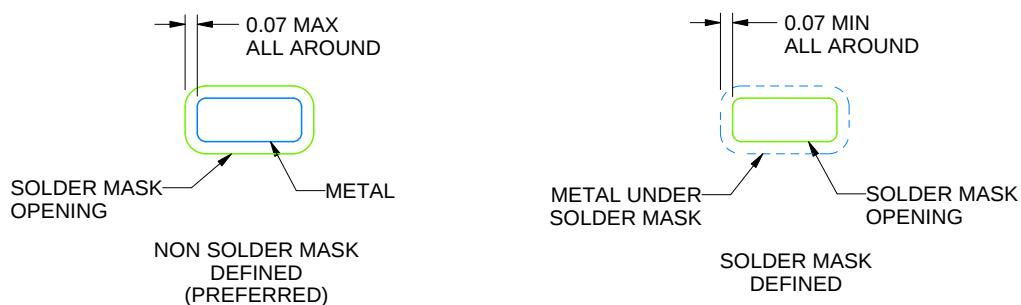
DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

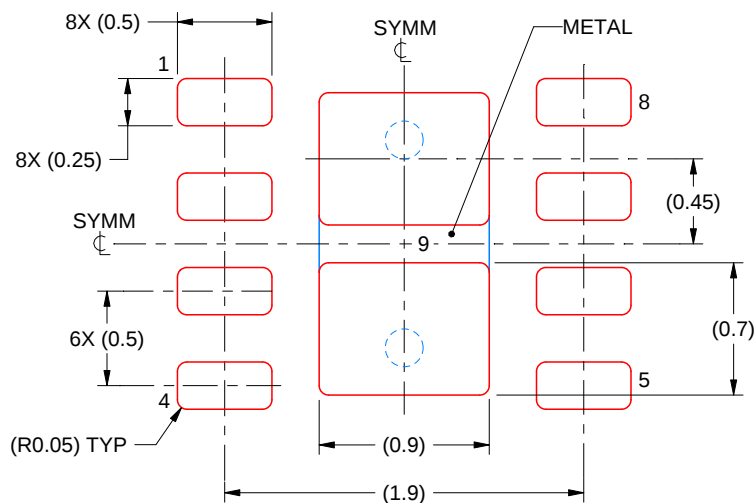
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



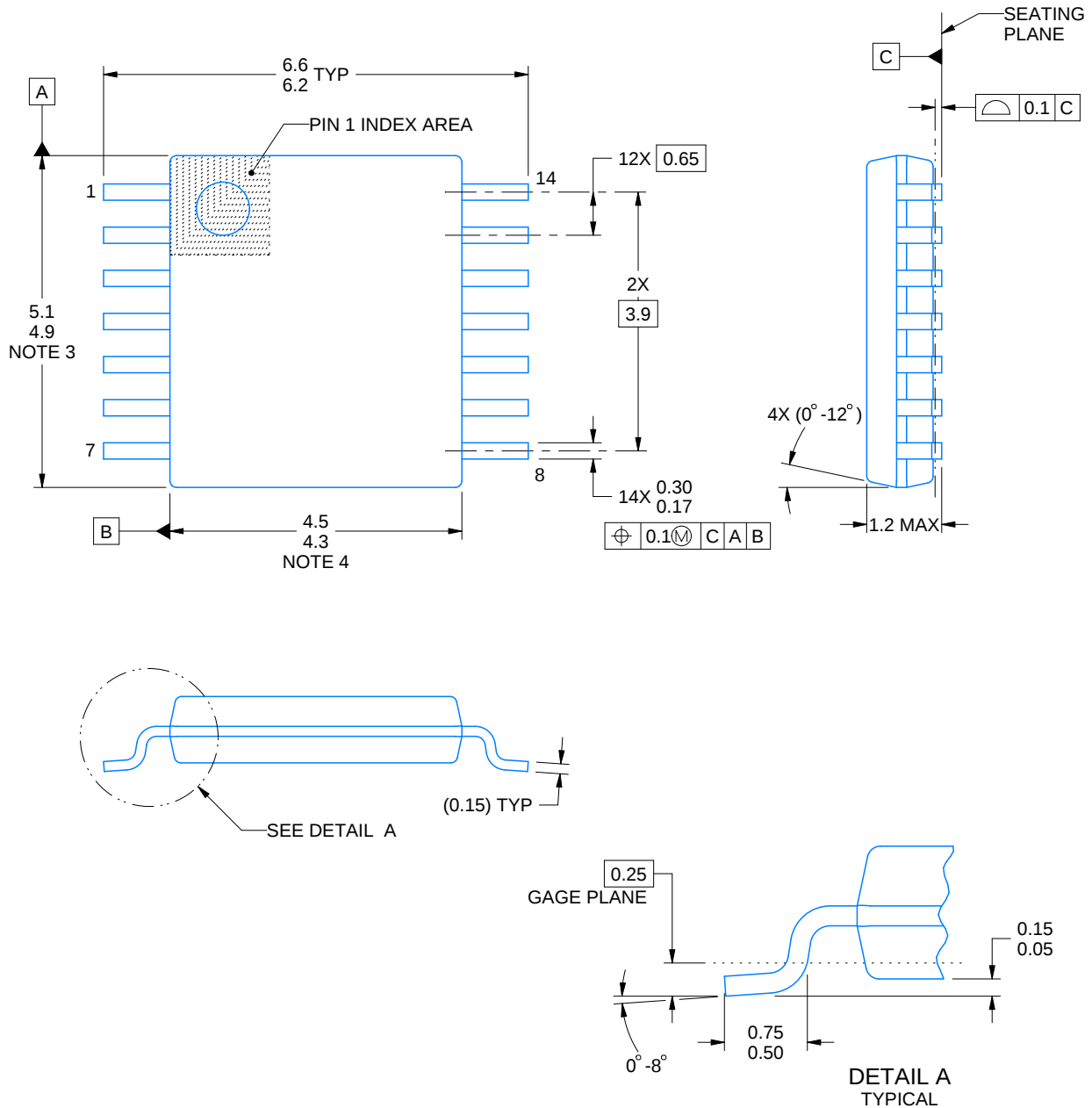
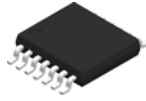
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220202/B 12/2023

NOTES:

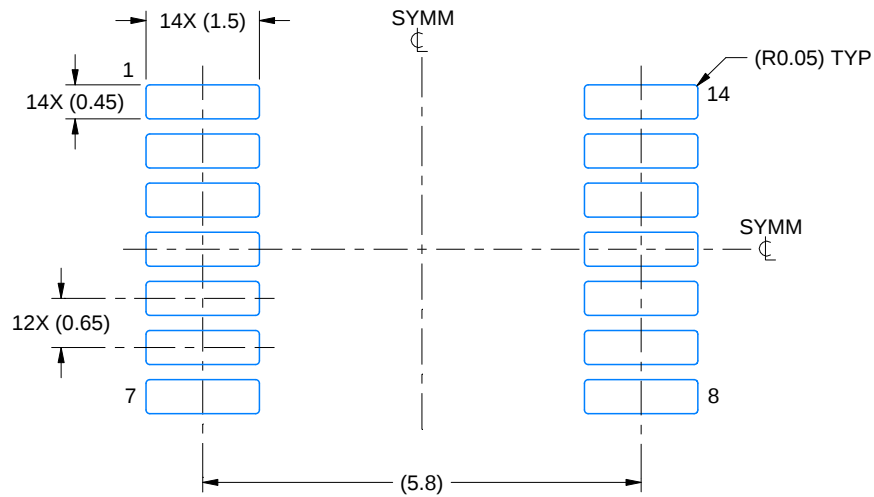
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

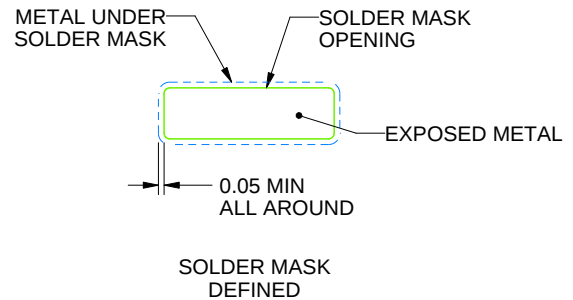
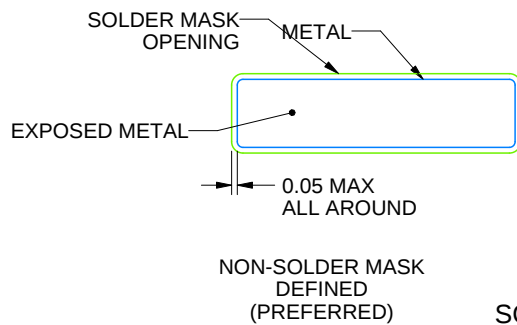
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

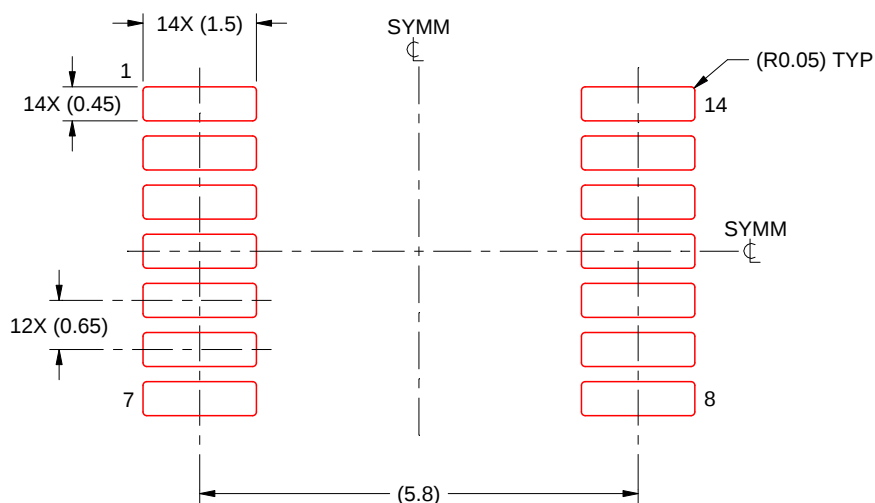
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

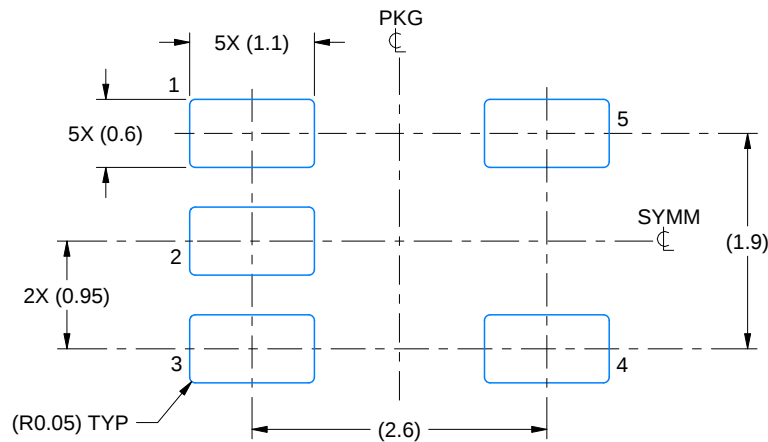
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

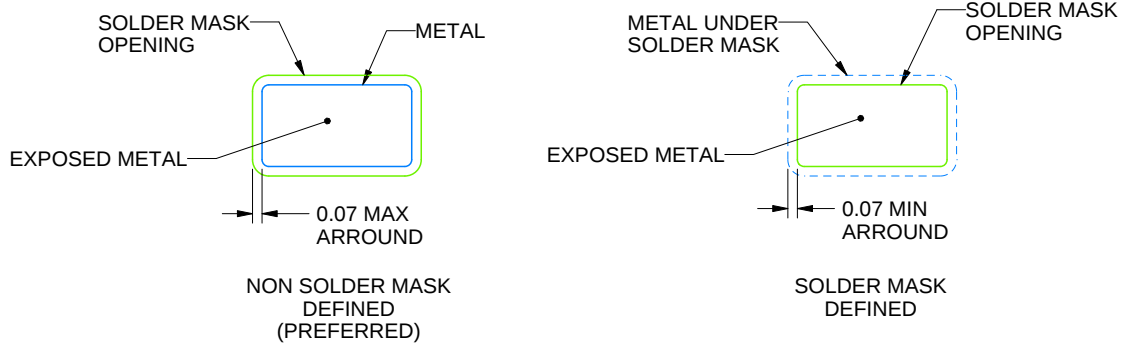
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

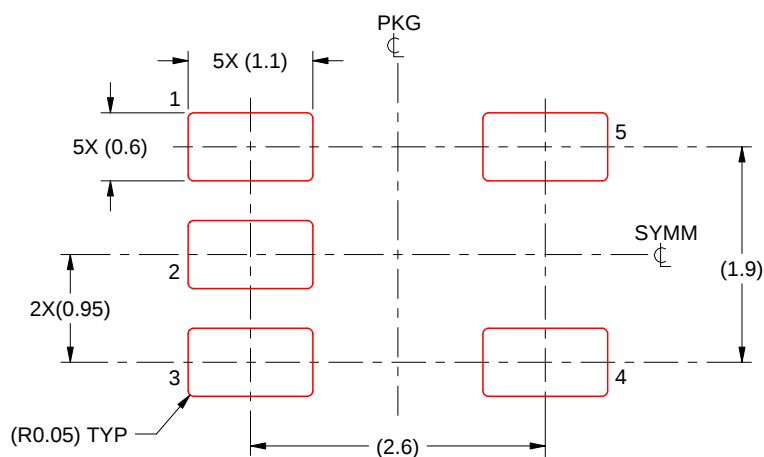
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

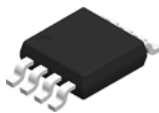


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

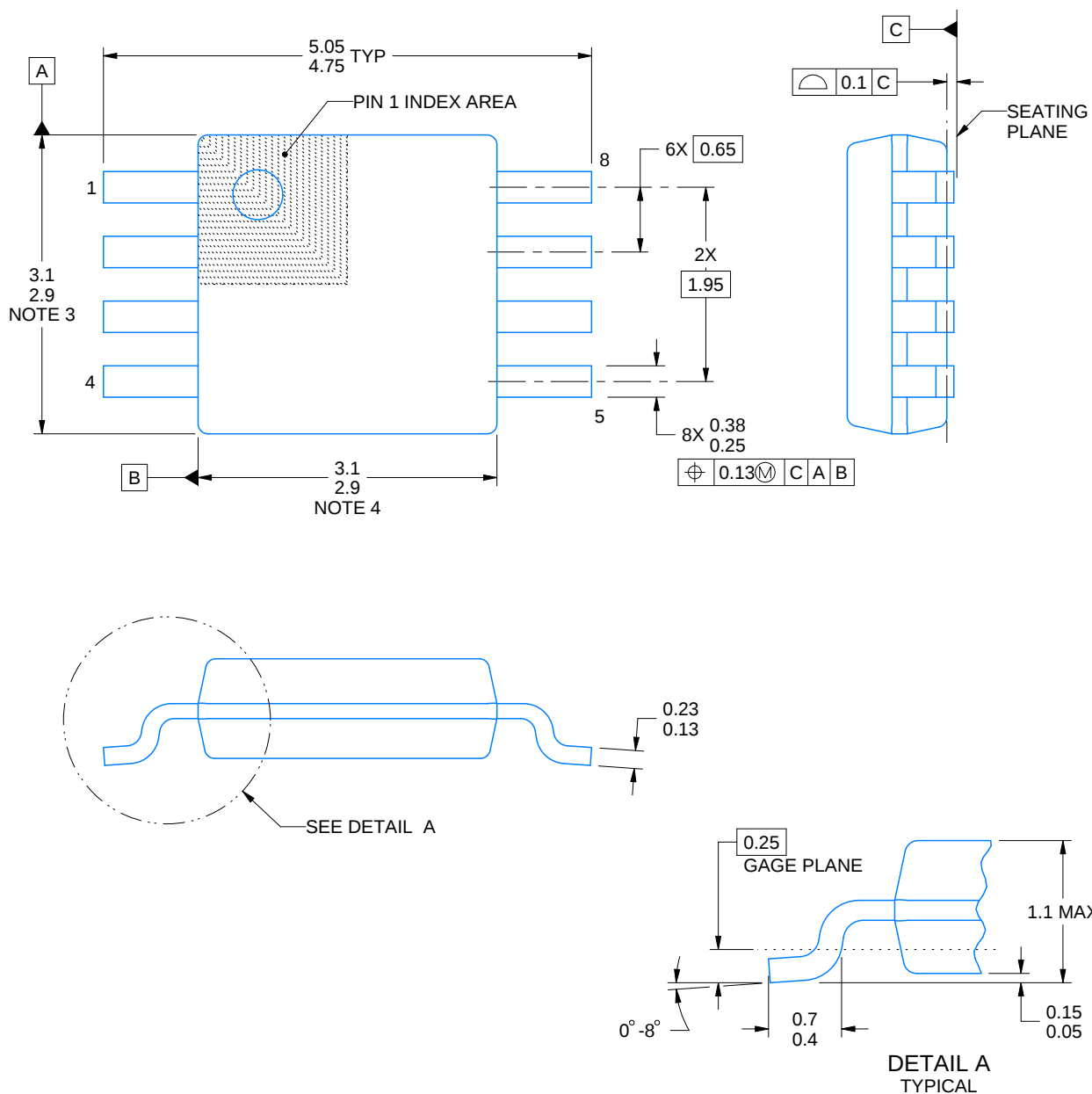
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

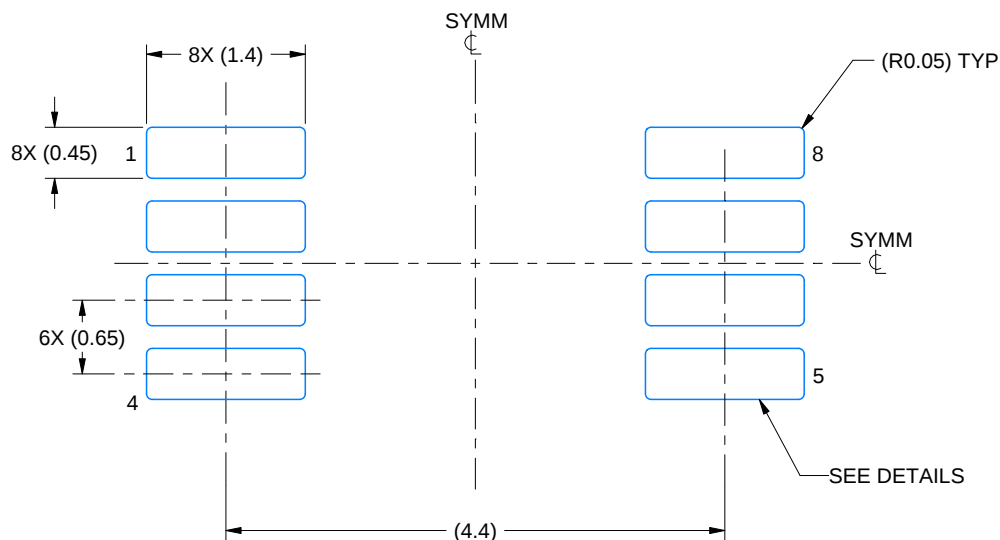
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

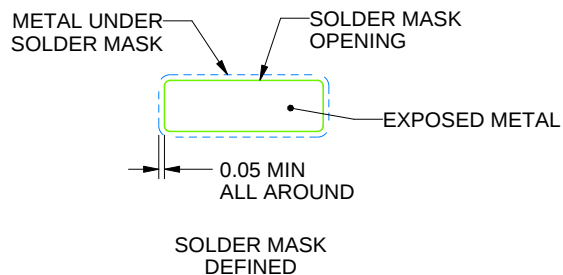
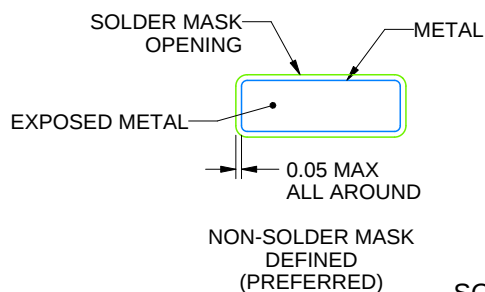
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

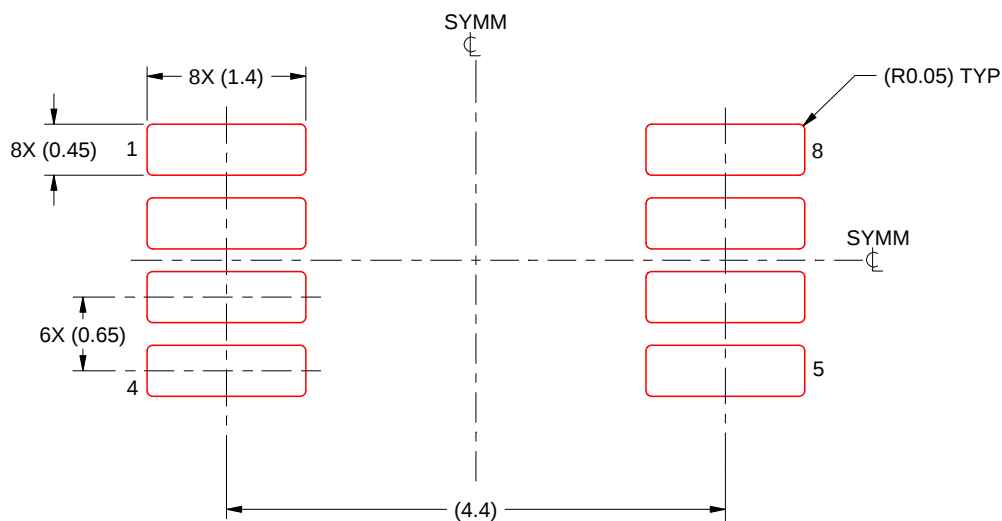
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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