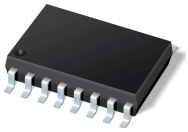


SLLS589C–NOVEMBER 2003–REVISED OCTOBER 2007

DUAL DIFFERENTIAL PECL DRIVER/RECEIVER

FEATURES

- **Functional Replacement for the Agere BTF1A**
- **Driver Features**
  - **Third-State Logic Low Output**
  - **ESD Protection HBM > 3 kV, CDM > 2 kV**
  - **No Line Loading when V_{CC} = 0**
  - **Capable of Driving 50-Ω loads**
  - **2.0-ns Maximum Propagation Delay**
  - **0.2-ns Output Skew (typical)**
- **Receiver Features**
  - **High-Input Impedance Approximately 8 kΩ**
  - **4.0-ns Maximum Propagation Delay**
  - **50-mV Hysteresis**
  - **Slew Rate Limited (1 ns min 80% to 20%)**
  - **ESD Protection HBM > 3 kV, CDM > 2 kV**
  - **-1.1-V to 7.1-V Input Voltage Range**
- **Common Device Features**
  - **Common Enable for Each Driver/Receiver Pair**
  - **Operating Temperature Range: -40°C to 85°C**
  - **Single 5.0 V ± 10% Supply**
  - **Available in Gull-Wing SOIC (JEDEC MS-013, DW) and SOIC (D) Package**

DESCRIPTION

The TB5T1 device is a dual differential driver/receiver circuit that transmits and receives digital data over balanced transmission lines. The dual drivers translate input TTL logic levels to differential pseudo-ECL output levels. The dual receivers convert differential-input logic levels to TTL output levels. Each driver or receiver pair has its own common enable control allowing serial data and a control clock to be transmitted and received on a single integrated circuit. The TB5T1 requires the customer to supply termination resistors on the circuit board.

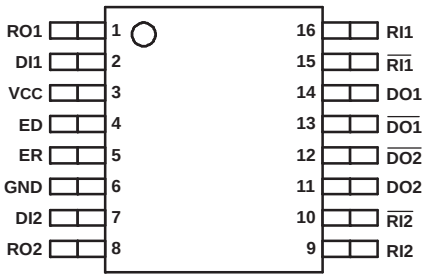
The power-down loading characteristics of the receiver input circuit are approximately 8 kΩ relative to the power supplies; hence, it does not load the transmission line when the circuit is powered down.

In circuits with termination resistors, the line remains impedance- matched when the circuit is powered down. The driver does not load the line when it is powered down.

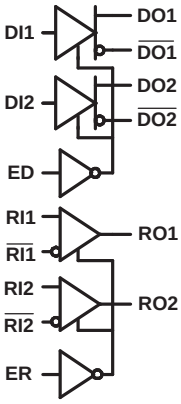
All devices are characterized for operation from -40°C to 85°C.

The logic inputs of this device include internal pull-up resistors of approximately 40 kΩ that are connected to V_{CC} to ensure a logical high level input if the inputs are open circuited.

PIN ASSIGNMENTS
DW AND D PACKAGE
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



Enable Truth Table

ED	ER	D1	D2	R1	R2
0	0	Active	Active	Active	Active
1	0	Disabled	Disabled	Active	Active
0	1	Active	Active	Disabled	Disabled
1	1	Disabled	Disabled	Disabled	Disabled

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	PART MARKING	PACKAGE(1)	LEAD FINISH	STATUS
TB5T1DW	TB5T1	Gull-Wing SOIC	NiPdAu	Production
TB5T1D	TB5T1	SOIC	NiPdAu	Production

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING $T_A \leq 25°C$	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT WITH NO AIR FLOW	DERATING FACTOR (1) $T_A \geq 25°C$	POWER RATING $T_A = 85°C$
D	Low-K(2)	752 mW	132.8°C/W	7.5 mW/°C	301 mW
	High-K(3)	1160 mW	85.8°C/W	11.7 mW/°C	466 mW
DW	Low-K(2)	814 mW	122.7°C/W	8.2 mW/°C	325 mW
	High-K(3)	1200 mW	83.1°C/W	12 mW/°C	481 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted with no air flow.
(2) In accordance with the low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the high-K thermal metric definitions of EIA/JESD51-7.

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to-board thermal resistance	D	48.4	°C/W
		DW	55.2	°C/W
θ_{JC}	Junction-to-case thermal resistance	D	45.1	°C/W
		DW	48.1	°C/W

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

			UNIT
Supply voltage, V_{CC}			0 V to 6 V
Magnitude of differential bus (input) voltage, $\lvert V_{RI1} - V_{\overline{RI1}}\rvert$, $\lvert V_{RI2} - V_{\overline{RI2}}\rvert$			8.4 V
ESD	Human Body Model [2]	All pins	±3 kV
	Charged-Device Model [3]	All pins	±2 kV
Continuous power dissipation			See Dissipation Rating Table
Storage temperature, T_{stg}			-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Bus pin input voltage, V_{RI1}, $V_{\overline{RI1}}$, V_{RI2}, or $V_{\overline{RI2}}$	-1.2[1]		7.2	V
Magnitude of differential input voltage, $\lvert V_{RI1} - V_{\overline{RI1}}\rvert$, $\lvert V_{RI2} - V_{\overline{RI2}}\rvert$	0.1		6	V
Operating free-air temperature, T_A	-40		85	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	Outputs disabled			40	mA
		Outputs enabled			40	mA

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THIRD STATE

A TB5T1 driver produces pseudo-ECL levels and has a third state mode, which is different from a conventional TTL device. When a TB5T1 driver is placed in the third state, the base of the output transistors are pulled low, bringing the outputs below the active-low level of standard PECL devices. (For example: The TB5T1 low output level is typically 2.7 V, while the third state noninverting output level is typically 1.2 V.) In a bidirectional, multipoint bus application, the driver of one device, which is in its third state, can be back driven by another driver on the bus whose voltage in the low state is lower than the 3-stated device. This could be due to differences between individual driver's power supplies. In this case, the device in the third state controls the line, thus clamping the line and reducing the signal swing. If the difference between the driver power supplies is small, this consideration can be ignored. Again using the TB5T1 driver as an example, a typical supply voltage difference between separate drivers of > 2 V can exist without significantly affecting the amplitude of the signal.

DRIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output high voltage(1)			V_{CC} - 1.8	V_{CC} - 1.3	V_{CC} - 0.8	V
V_{OL}	Output low voltage(1)			V_{OH} - 1.4	V_{OH} - 1.2	V_{OH} - 0.7	V
V_{OD}	Differential output voltage, $\|V_{OH} - V_{OL}\|$			0.7	1.1	1.4	V
V_{OH}	Output high voltage(1)		T_A = 0C to 85C	V_{CC} - 1.8	V_{CC} - 1.3	V_{CC} - 0.8	V
V_{OL}	Output low voltage(1)			V_{OH} - 1.4	V_{OH} - 1.1	V_{OH} - 0.5	V
V_{OD}	Differential output voltage, $\|V_{OH} - V_{OL}\|$			0.5	1.1	1.4	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		C_L= 5 pF, See Figure 7		230	600	mV
V_{OZH}	Third state output high voltage(1)	$\overline{DO1}$, $\overline{DO2}$	V_{CC} = 4.5 V	1.4	1.8	2.2	V
V_{OZD}	Third state deferential output voltage(1)	$V_{DOn} - V_{\overline{DOn}}$		-0.47(2)	-0.6		
V_{IL}	Input low voltage(3)		V_{CC} = 5.5 V			0.8	V
V_{IH}	Input high voltage		V_{CC} = 4.5 V	2			V
V_{IK}	Input clamp voltage		V_{CC} = 4.5 V, I_I = -5 mA			-1(2)	V
I_{OS}	Short-circuit output current(4)		V_{CC} = 5.5 V, V_O = 0 V			-250(2)	mA
			V_{CC} = 5.5 V, V_{OD} = 0 V			10(2)	mA
I_{IL}	Input low current		V_{CC} = 5.5 V, V_I = 0.4 V			-400(2)	A
I_{IH}	Input high current		V_{CC} = 5.5 V, V_I = 2.7 V			20	A
I_{IH}	Input reverse current		V_{CC} = 5.5 V, V_I = 5.5 V			100	A
C_{IN}	Input Capacitance				5		pF

(1) Values are with terminations as per Figure 6.
(2) This parameter is listed using a magnitude and polarity/direction convention, rather than an algebraic convention, to match the original Agere data sheet.
(3) The input levels and difference voltage provide no noise immunity and should be tested only in a static, noise-free environment.
(4) Test must be performed one lead at a time to prevent damage to the device. No test circuit attached.

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RECEIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output low voltage		V_{CC} = 4.5 V, I_{OL} = 8.0 mA			0.4	V
V_{OH}	Output high voltage		V_{CC} = 4.5 V, I_{OH} = -400 µA	2.4			V
V_{IL}	Enable input low voltage(1)		V_{CC}= 5.5 V			0.8	V
V_{IH}	Enable input high voltage(1)		V_{CC} = 4.5 V	2			V
V_{IK}	Enable input clamp voltage		V_{CC} = 4.5 V, I_I = -5 mA			-1(2)	V
V_{TH+}	Positive-going differential input threshold voltage(1)	$\|V_{Rin} - V_{\overline{Rin}}\|$	n = 1 or 2			100	mV
V_{TH-}	Negative-going differential input threshold voltage(1)	$\|V_{Rin} - V_{\overline{Rin}}\|$	n = 1 or 2			-100(2)	mV
V_{HYST}	Differential input threshold voltage hysteresis	$(V_{TH+} - V_{TH-})$			50		mV
I_{OZL}	Off-state output low current (high Z)		V_{CC} = 5.5 V, V_O = 0.4 V			-20(2)	µA
I_{OZH}	Off-state output high current (high Z)		V_{CC} = 5.5 V, V_O = 2.4 V			20	µA
I_{OS}	Short circuit output current(3)		V_{CC} = 5.5 V			-100(2)	mA
I_{IL}	Enable input low current		V_{CC} = 5.5 V, V_{IN} = 0.4 V			-400(2)	µA
I_{IH}	Enable input high current		V_{CC} = 5.5 V, V_{IN} = 2.7 V			20	µA
I_{IH}	Enable input reverse current		V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	µA
II_L	Differential input low current		V_{CC} = 5.5V, V_{IN} = -1.2 V			-2(2)	mA
I_{IH}	Differential input high current		V_{CC} = 5.5V, V_{IN} = 7.2 V			1	mA
R_O	Output resistance				20		Ω

(1) The input levels and difference voltage provide no noise immunity and should be tested only in a static, noise-free environment.
(2) This parameter is listed using a magnitude and polarity/direction convention, rather than an algebraic convention, to match the original Agere data sheet.
(3) Test must be performed one lead at a time to prevent damage to the device.

DRIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{P1}	Propagation delay time, input high to output(1)	C_L= 5 pF, See Figure 2 and Figure 6		1.2	2	ns
t_{P2}	Propagation delay time, input low to output(1)			1.2	2	ns
Δt_P	Capacitive delay			0.01	0.03	ns/pF
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	C_L = 5 pF, See Figure 3 and Figure 6		8	12	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			7	12	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			4	12	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			5	12	ns
t_{skew1}	Output skew, $\|t_{P1} - t_{P2}\|$	C_L= 5 pF, See Figure 2 andFigure 6		0.15	0.3	ns
t_{skew2}	Output skew, $\|t_{PHH} - t_{PHL}\|$, $\|t_{PLH} - t_{PLL}\|$			0.15	1.1	ns
$t_{skew(pp)}$	Part-to-part skew(2)			0.1	1	ns
Δt_{skew}	Output skew, difference between drivers				0.3	ns
t_{TLH}	Rise time (20%-80%)			0.7	2	ns
t_{THL}	Fall time (80%-20%)			0.7	2	ns

(1) Parameters t_{P1} and t_{P2} are measured from the 1.5 V point of the input to the crossover point of the outputs (see Figure 2).
(2) $t_{skew(pp)}$ is the magnitude of the difference in propagation delay times between any specified outputs of two devices when both devices operate with the same supply voltage, at the same temperature, and have identical packages and test circuits.

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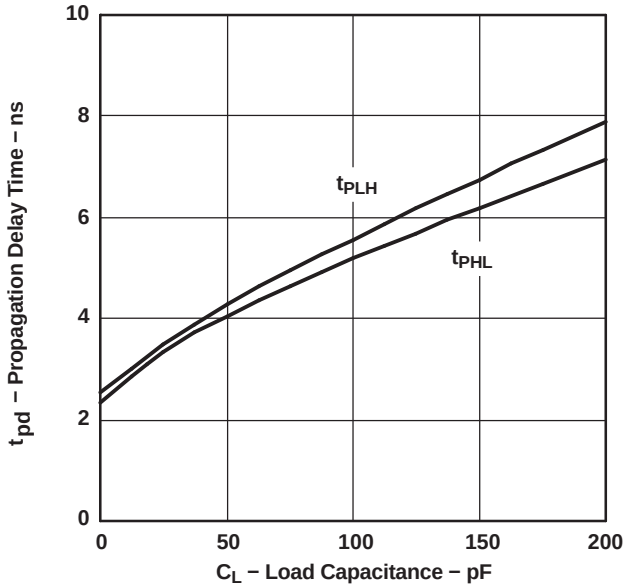
RECEIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 0 pF(1), See Figure 4 and Figure 8		2.5	4	ns
t_{PHL}	Propagation delay time, high-to-low-level output			2.5	4	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 4 and Figure 8		3	5.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3	5.5	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	C_L = 5 pF, See Figure 5 and Figure 9		6	12	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			6	12	ns
t_{skew1}	Pulse width distortion, $\lvert t_{PHL} - t_{PLH} \rvert$	Load capacitance (C_L) = 10 pF, See Figure 4 and Figure 8			0.7	ns
		Load capacitance (C_L) = 150 pF, See Figure 4 and Figure 8			4	ns
$\Delta t_{skew1pp}$	Part-to-part output waveform skew(2)	C_L = 10 pF, T_A = 75°C, See Figure 4 and Figure 8		0.8	1.4	ns
		C_L = 10 pF, T_A = -40°C to 85°C, See Figure 4 and Figure 8			1.5	ns
Δt_{skew}	Same part output waveform skew(2)	C_L = 10 pF, See Figure 4 and Figure 8			0.3	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	C_L = 10 pF, See Figure 5 and Figure 8		3	12	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			4	12	ns
t_{TLH}	Rise time (20%—80%)	C_L = 10 pF, See Figure 5 and Figure 8	1		4	ns
t_{THL}	Fall time (80%—20%)		1		4	ns

(1) The propagation delay values with a 0 pF load are based on design and simulation.
(2) Output waveform skews are when devices operate with the same supply voltage, same temperature, have the same packages and the same test circuits.



NOTE: This graph is included as an aid to the system designers. Total circuit delay varies with load capacitance. The total delay is the sum of the delay due to external capacitance and the intrinsic delay of the device. Intrinsic delay is listed in the table above as the 0 pF load condition. The incremental increase in delay between the 0 pF load condition and the actual total load capacitance represents the extrinsic, or external delay contributed by the load.

Figure 1. Typical Propagation Delay vs Load Capacitance at 25°C

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PARAMETER MEASUREMENT INFORMATION

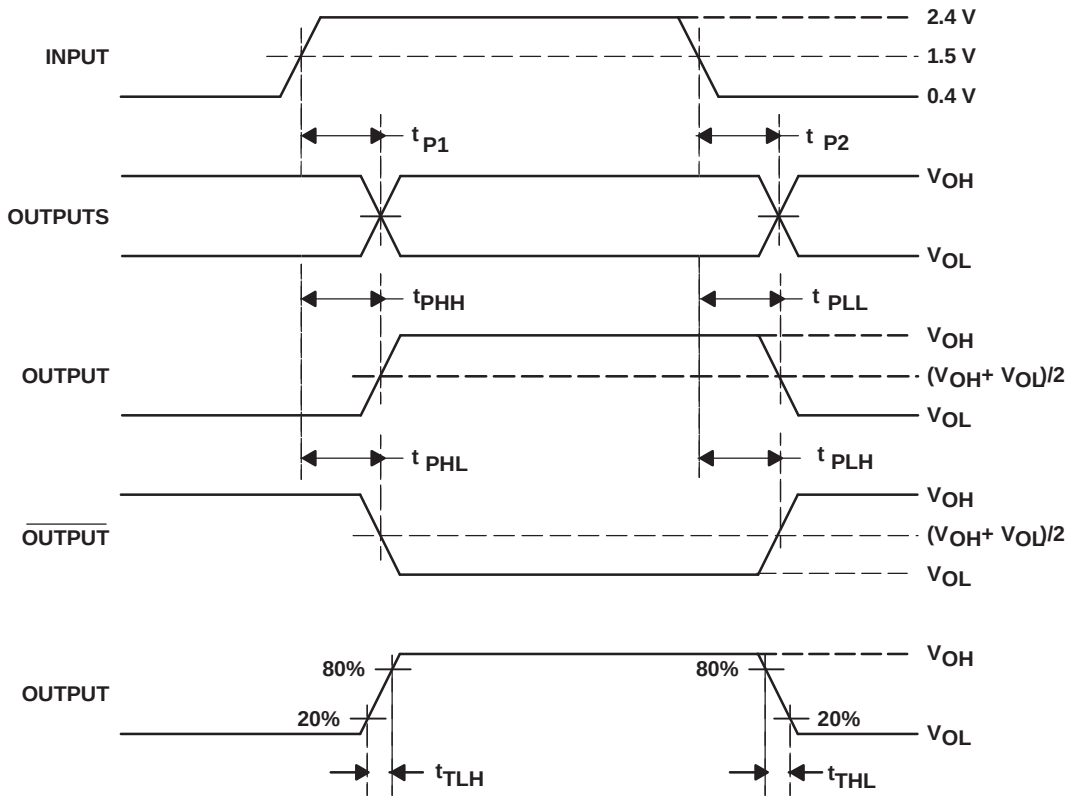
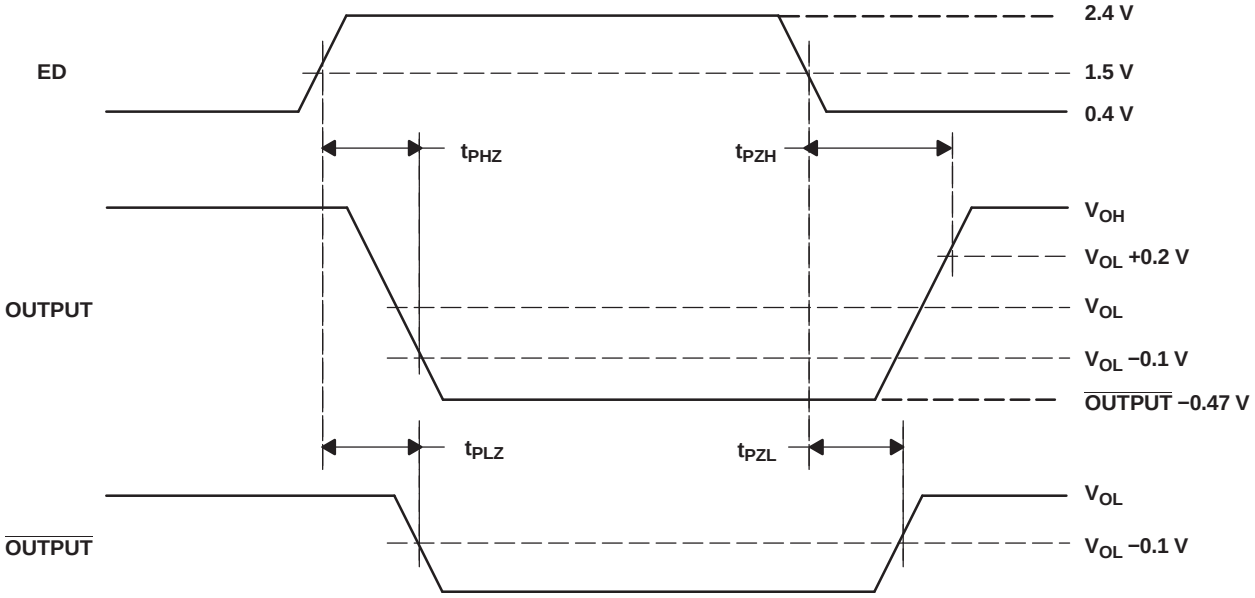


Figure 2. Driver Propagation Delay Times



A. NOTE: In the third state, OUTPUT is 0.47 V (minimum) more negative than $\overline{\text{OUTPUT}}$.

Figure 3. Driver Enable and Disable Delay Times for a High Input

PARAMETER MEASUREMENT INFORMATION (continued)

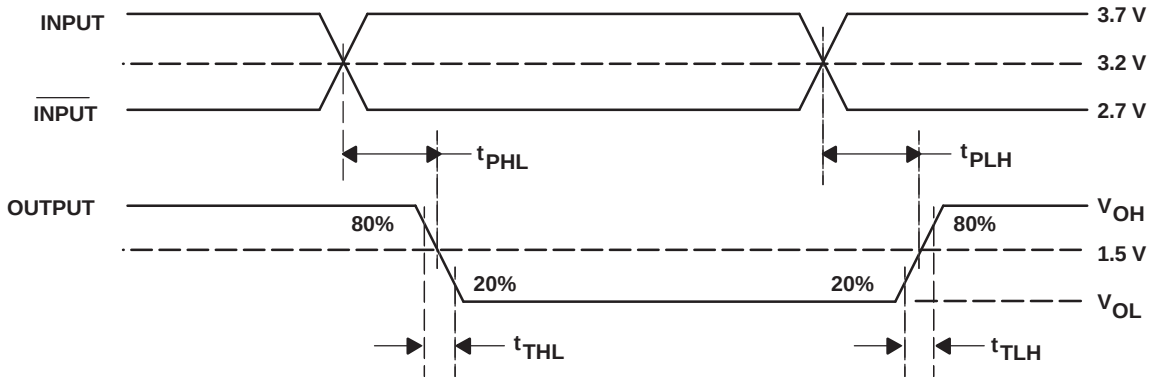


Figure 4. Receiver Propagation Delay Times

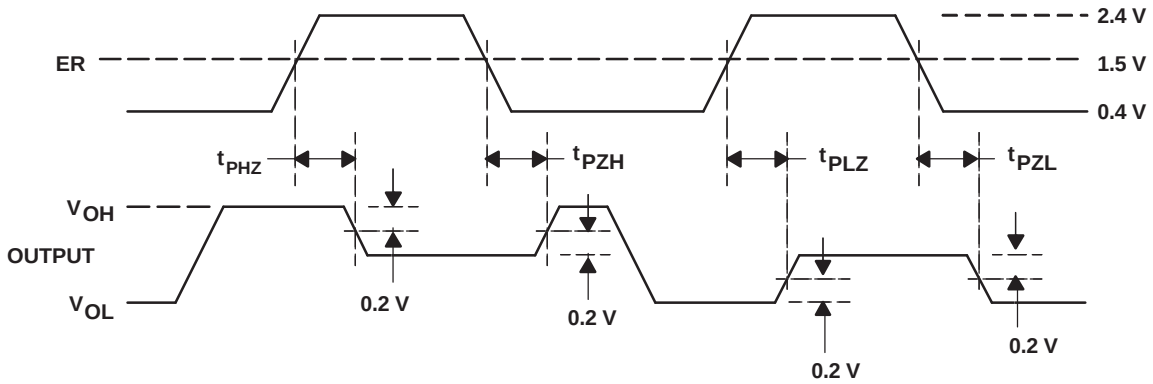
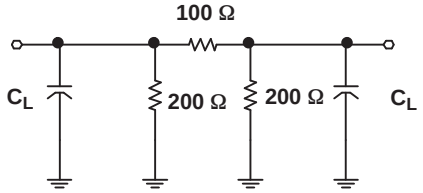


Figure 5. Receiver Enable and Disable Timing

Parametric values specified under the Electrical Characteristics and Timing Characteristics sections for the data transmission driver devices are measured with the following output load circuits.



C_L includes test−fixture and probe capacitance.

Figure 6. Driver Test Circuit

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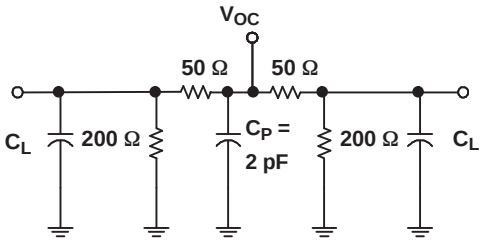
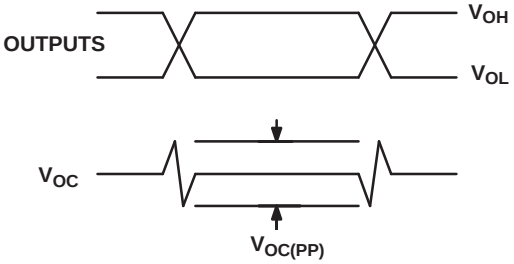
PARAMETER MEASUREMENT INFORMATION (continued)



C_L includes test−fixture and probe capacitance.



A. NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f = 1 ns, pulse repetition rate (PRR) = 0.25 Mbps, pulse width = 500 ± 10 ns. C_P includes the instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OS(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 7. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

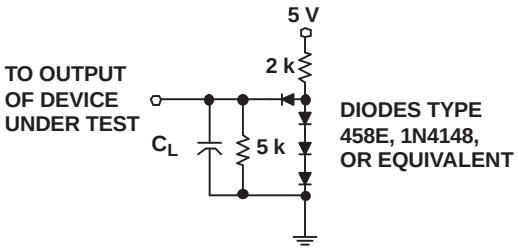


Figure 8. Receiver Propagation Delay Time and Enable Time (t_{PZH}, t_{PZL}) Test Circuit

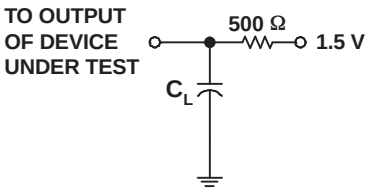


Figure 9. Receiver Disable Time (t_{PHZ}, t_{PLZ}) Test Circuit

TYPICAL CHARACTERISTICS

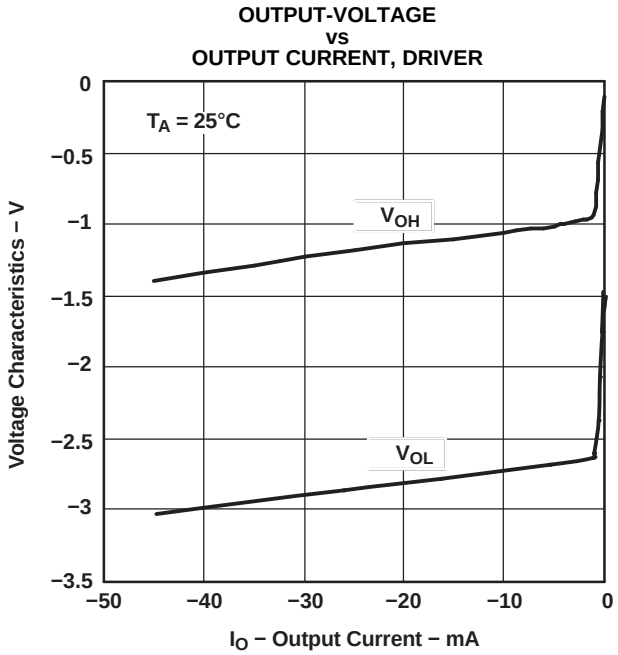


Figure 10.

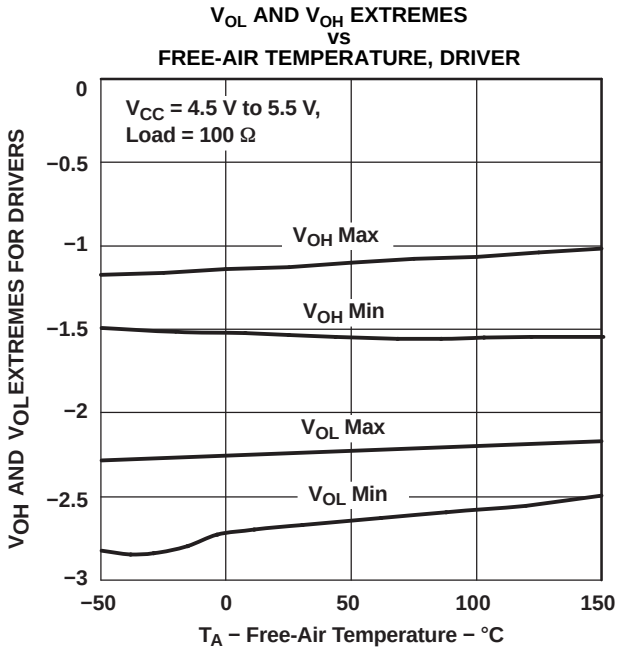


Figure 11.

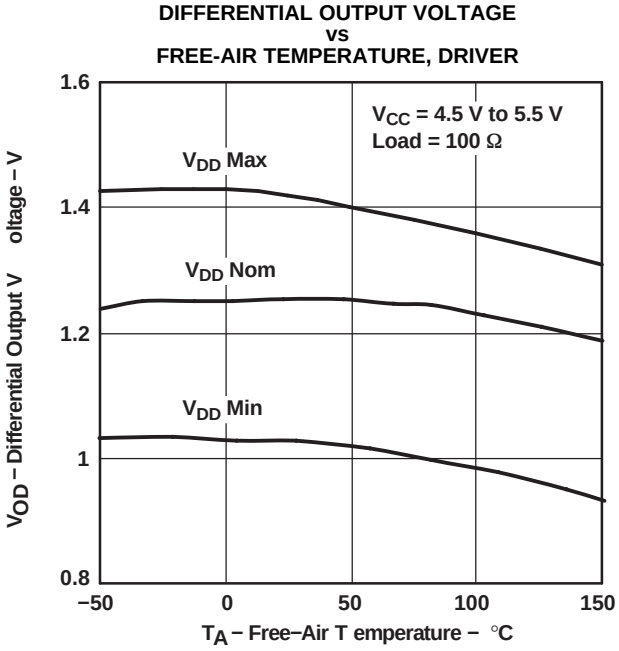


Figure 12.

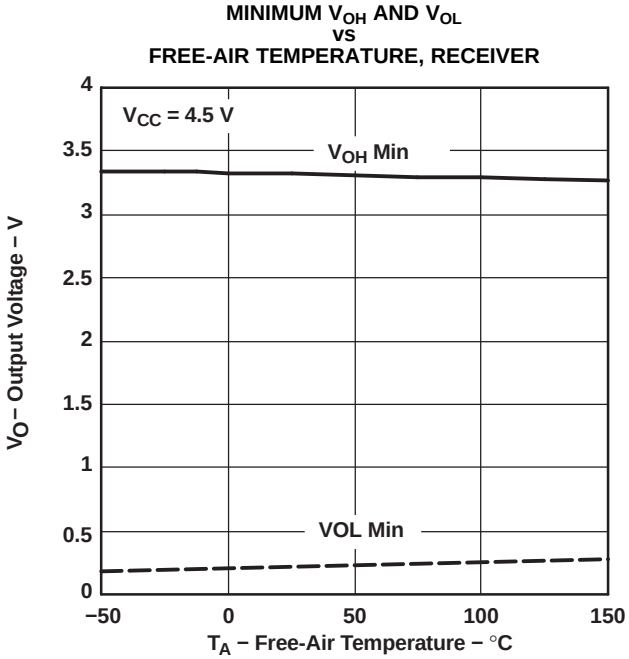


Figure 13.

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TYPICAL CHARACTERISTICS (continued)

PROPAGATION DELAY TIME t_{P1} or t_{P2} vs FREE-AIR TEMPERATURE, DRIVER

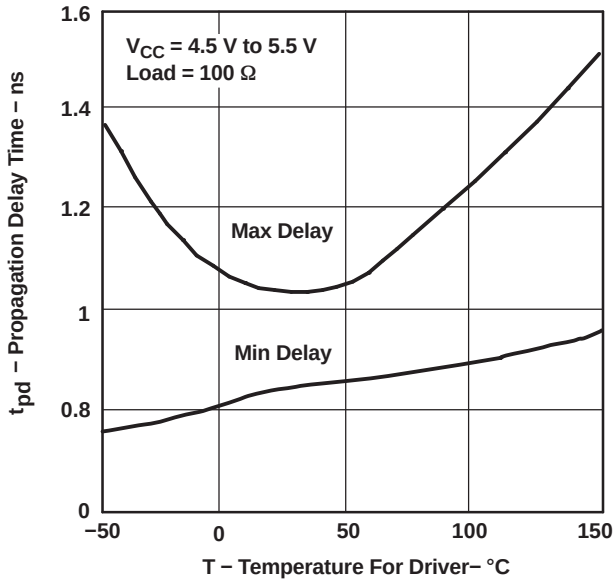

Figure 14.

LOW-TO-HIGH PROPAGATION DELAY vs FREE-AIR TEMPERATURE, RECEIVER

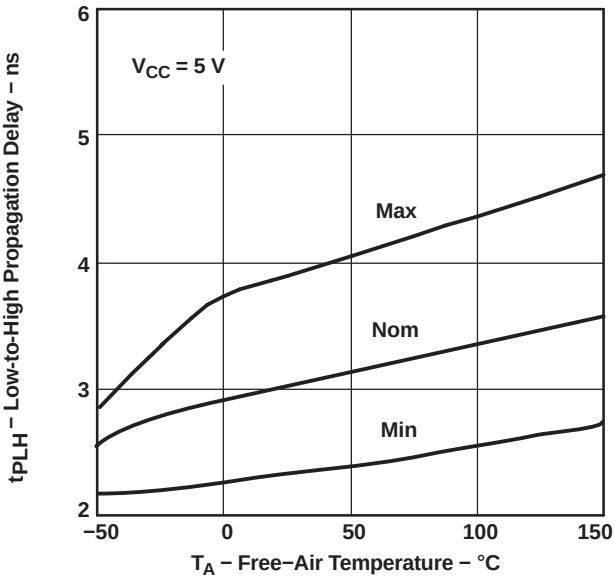

Figure 15.

HIGH-TO-LOW PROPAGATION DELAY vs FREE-AIR TEMPERATURE, RECEIVER

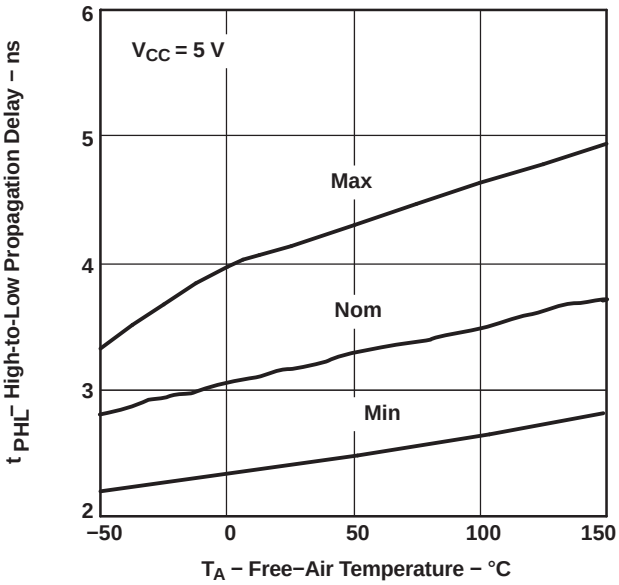

Figure 16.

APPLICATION INFORMATION

Power Dissipation

The power dissipation rating, often listed as the package dissipation rating, is a function of the ambient temperature, T_A, and the airflow around the device. This rating correlates with the device's maximum junction temperature, sometimes listed in the absolute maximum ratings tables. The maximum junction temperature accounts for the processes and materials used to fabricate and package the device, in addition to the desired life expectancy.

There are two common approaches to estimating the internal die junction temperature, T_J. In both of these methods, the device internal power dissipation P_D needs to be calculated This is done by totaling the supply power(s) to arrive at the system power dissipation:

$$\sum(V_{Sn} \times I_{Sn})$$

and then subtracting the total power dissipation of the external load(s):

$$\sum(V_{Ln} \times I_{Ln})$$

The first T_J calculation uses the power dissipation and ambient temperature, along with one parameter: θ_{JA}, the junction-to-ambient thermal resistance, in degrees Celsius per watt.

The product of P_D and θ_{JA} is the junction temperature rise above the ambient temperature. Therefore:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Note that θ_{JA} is highly dependent on the PCB on which the device is mounted and on the airflow over the device and PCB. JEDEC/EIA has defined standardized test conditions for measuring θ_{JA}. Two commonly used conditions are the low-K and the high-K boards, covered by EIA/JESD51-3 and EIA/JESD51-7 respectively. Figure 17 shows the low-K and high-K values of θ_{JA} versus air flow for this device and its package options.

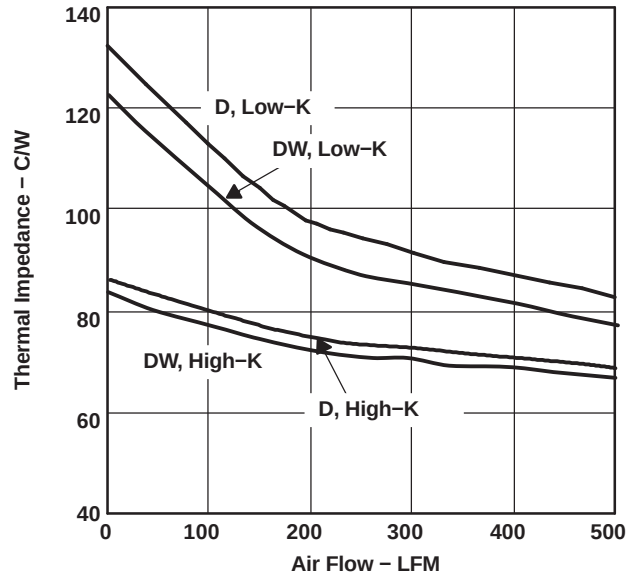

Figure 17. Thermal Impedance vs Air Flow

The standardized θ_{JA} values may not accurately represent the conditions under which the device is used. This can be due to adjacent devices acting as heat sources or heat sinks, to nonuniform airflow, or to the system PCB having significantly different thermal characteristics than the standardized test PCBs. The second method of system thermal analysis is more accurate. This calculation uses the power dissipation and ambient temperature, along with two device and two system-level parameters:

- θ_{JC}, the junction-to-case thermal resistance, in degrees Celsius per watt
- θ_{JB}, the junction-to-board thermal resistance, in degrees Celsius per watt
- θ_{CA}, the case-to-ambient thermal resistance, in degrees Celsius per watt
- θ_{BA}, the board-to-ambient thermal resistance, in degrees Celsius per watt.

In this analysis, there are two parallel paths, one through the case (package) to the ambient, and another through the device to the PCB to the ambient. The system-level junction-to-ambient thermal impedance, $\theta_{JA(S)}$, is the equivalent parallel impedance of the two parallel paths:

$$T_J = T_A + \left(P_D \times \theta_{JA(S)}\right)$$

where

$$\theta_{JA(S)} = \frac{\left[\left(\theta_{JC} + \theta_{CA}\right) \times \left(\theta_{JB} + \theta_{BA}\right)\right]}{\left(\theta_{JC} + \theta_{CA} + \theta_{JB} + \theta_{BA}\right)}$$

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Load Circuits

The test load circuits shown in Figure 6 and Figure 7 are based on a recommended *pi* type of load circuit shown in Figure 18. The 100-Ω differential load resistor R_T at the receiver provide proper termination for the interconnecting transmission line, assuming it has a 100-Ω characteristic impedance. The two resistors R_S to ground at the driver end of the transmission line link provide dc current paths for the emitter follower output transistors. The two resistors to ground normally should not be placed at the receiver end, as they shunt the termination resistor, potentially creating an impedance mismatch with undesirable reflections.

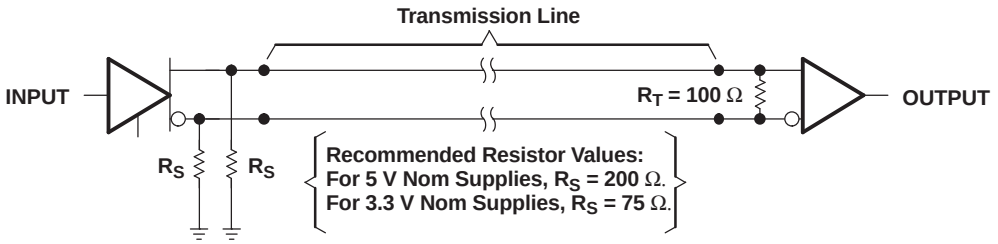

Figure 18. A Recommended pi Load Circuit

Another common load circuit, a Y load, is shown in Figure 19. The receiver-end line termination of R_T is provided by the series combination of the two $R_{T/2}$ resistors, while the dc current path to ground is provided by the single resistor R_S. Recommended values, as a function of the nominal supply voltage range, are indicated in the figure.

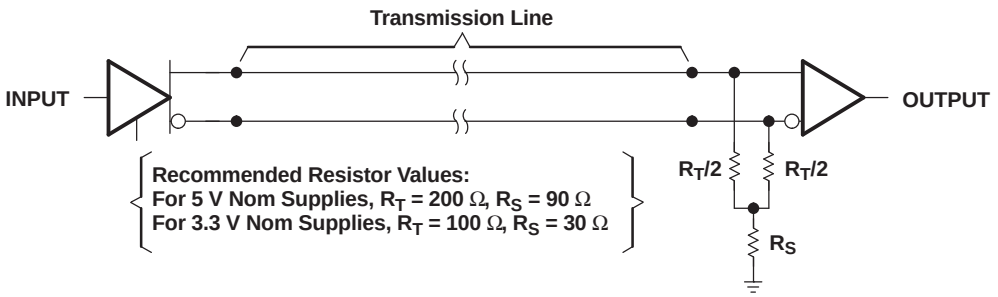

Figure 19. A Recommended Y Load Circuit

An additional load circuit, similar to one commonly used with ECL and PECL, is shown in Figure 20.

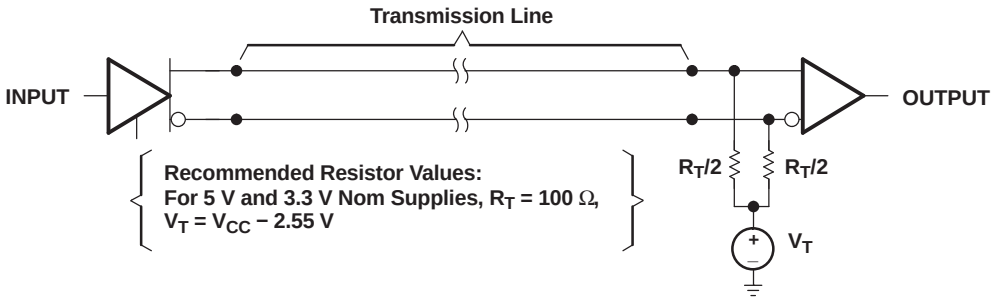

Figure 20. A Recommended PECL-Style Load Circuit

An important feature of all of these recommended load circuits is that they ensure that both of the emitter follower output transistors remain active (conducting current) at all times. When deviating from these recommended values, it is important to make sure that the low-side output transistor does not turn off. Failure to do so increases the t_{skew2} and $V_{OC(PP)}$ values, increasing the potential for electromagnetic radiation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TB5T1D	Last Time Buy	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5T1
TB5T1D.B	Last Time Buy	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5T1
TB5T1D1G4.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5T1
TB5T1DW	Last Time Buy	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TB5T1
TB5T1DW.B	Last Time Buy	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TB5T1
TB5T1DWR	Last Time Buy	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5T1
TB5T1DWR.B	Last Time Buy	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5T1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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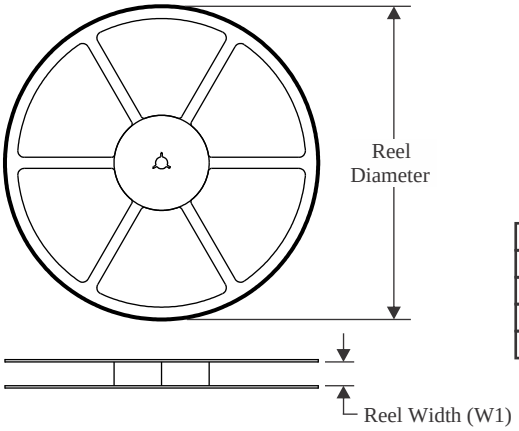
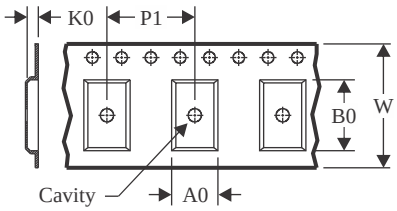
TAPE AND REEL INFORMATION

REEL DIMENSIONS

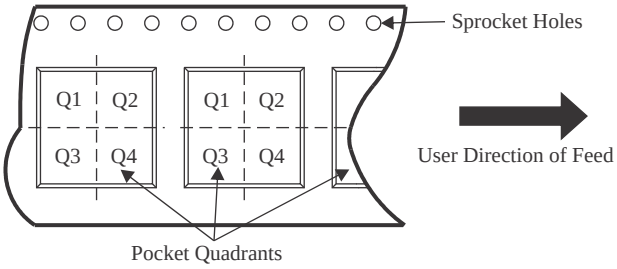


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

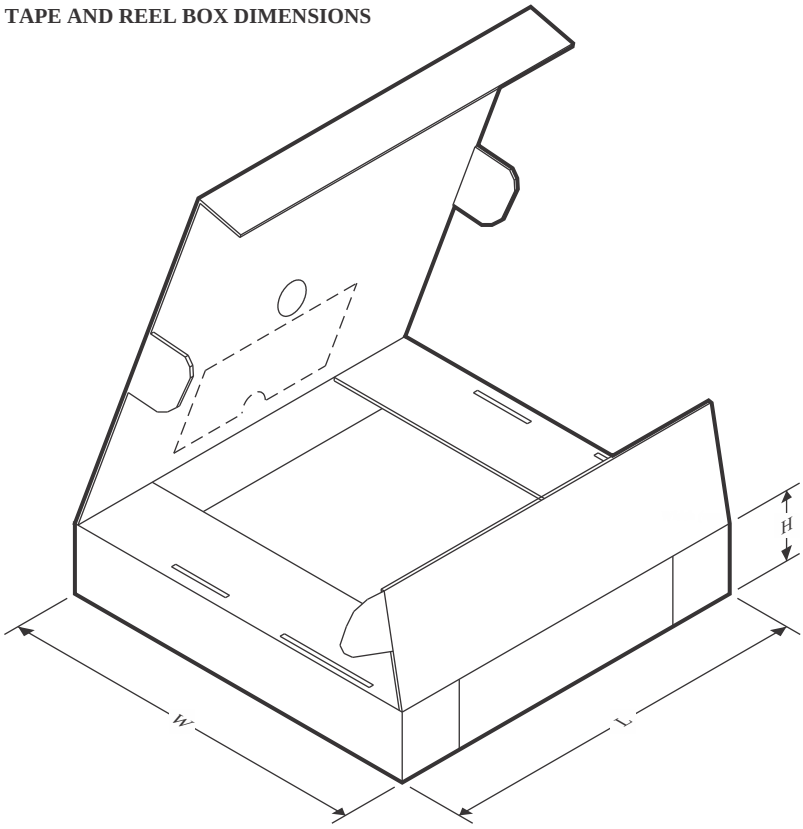
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TB5T1DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

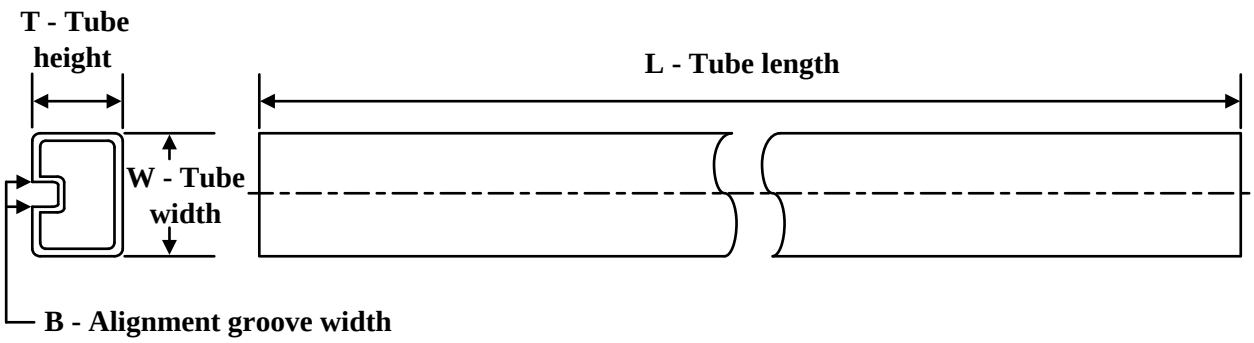
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TB5T1DWR	SOIC	DW	16	2000	350.0	350.0	43.0

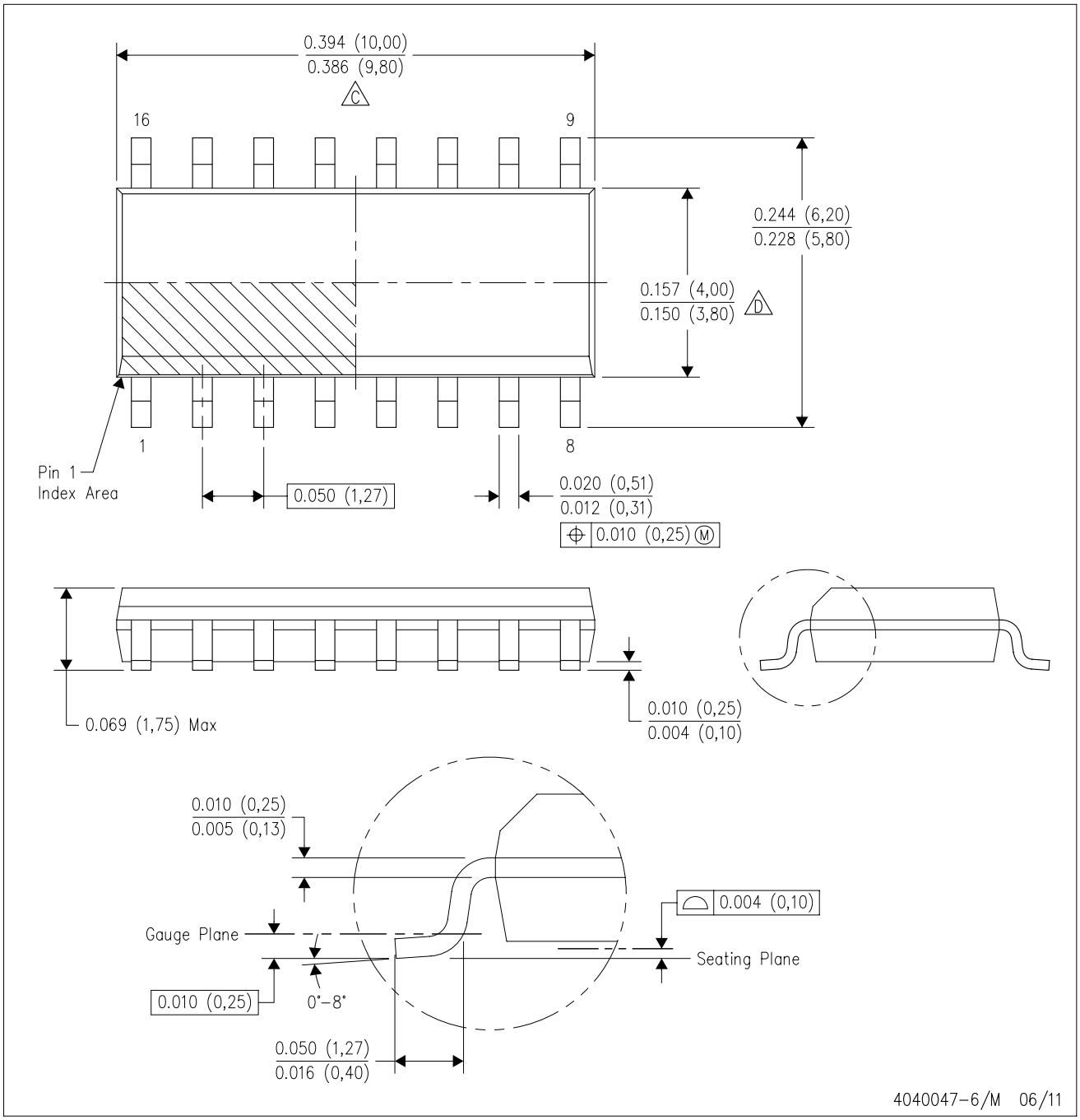
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TB5T1D	D	SOIC	16	40	505.46	6.76	3810	4
TB5T1D.B	D	SOIC	16	40	505.46	6.76	3810	4
TB5T1D1G4.B	D	SOIC	16	40	505.46	6.76	3810	4
TB5T1DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TB5T1DW.B	DW	SOIC	16	40	506.98	12.7	4826	6.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

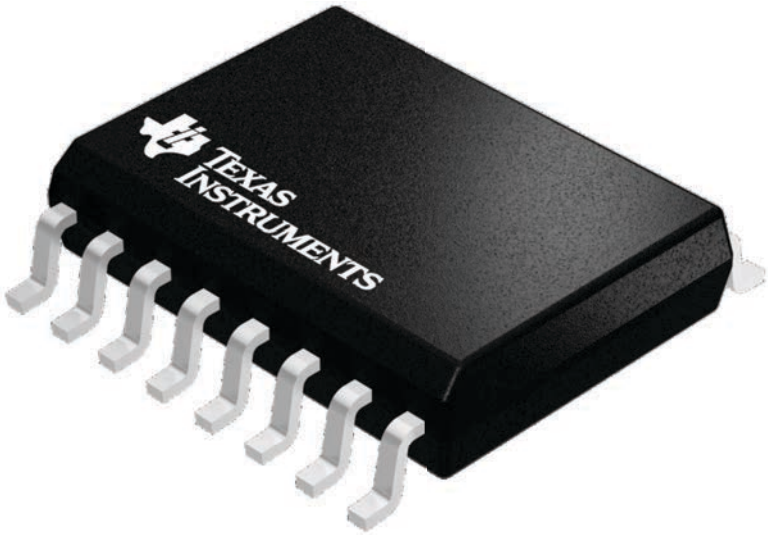
DW 16

SOIC - 2.65 mm max height

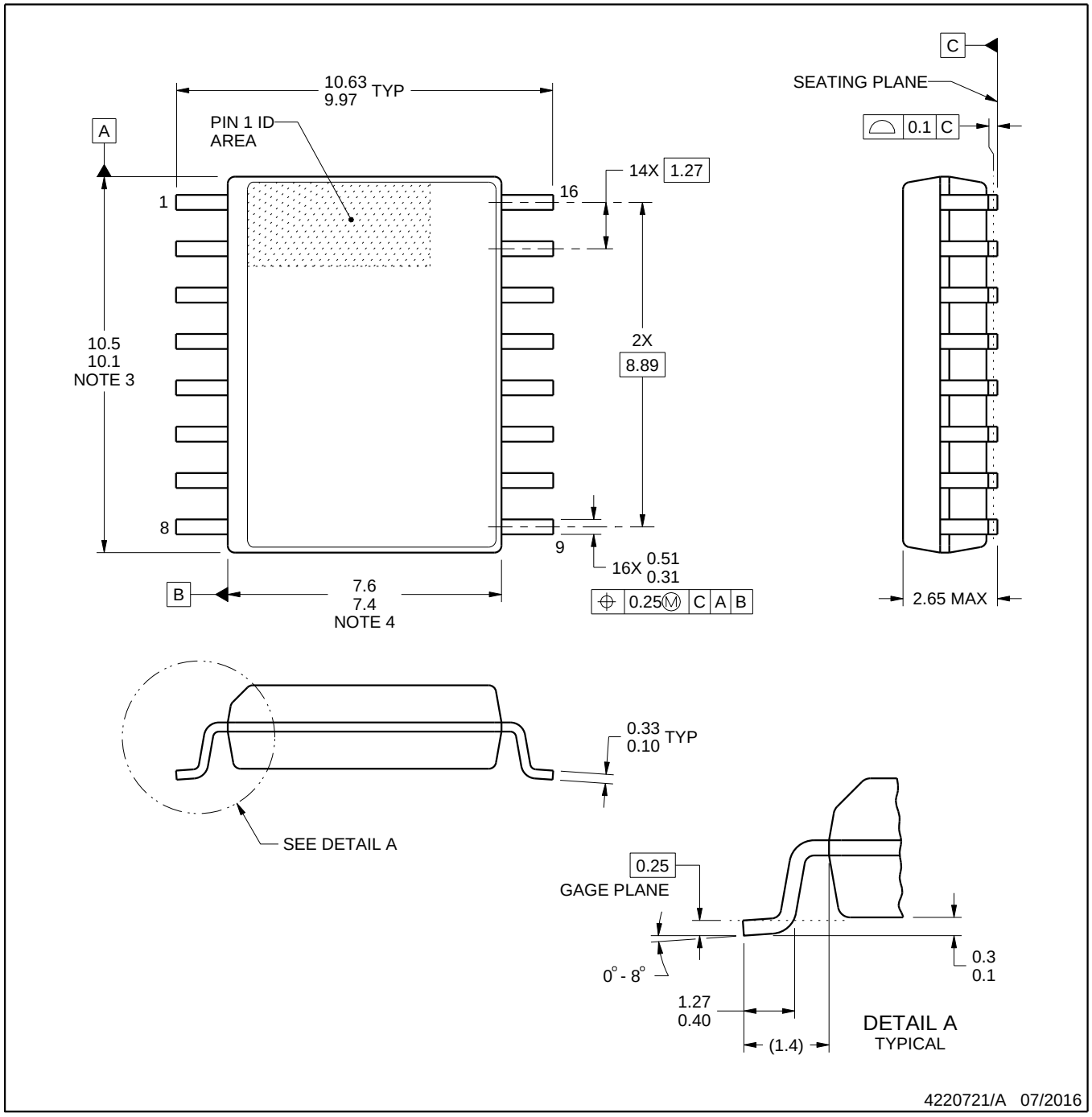
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

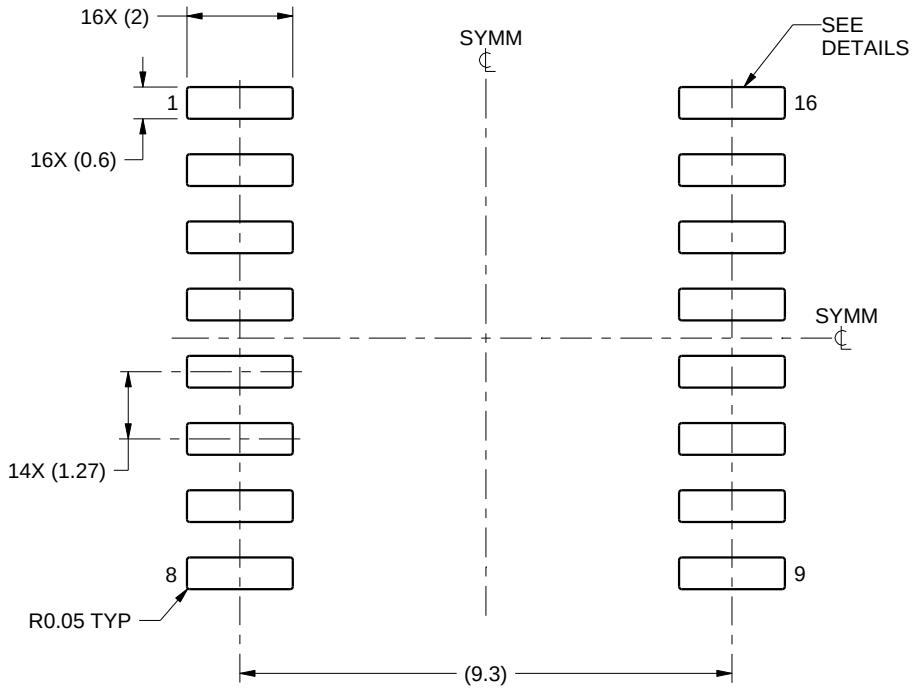


4224780/A

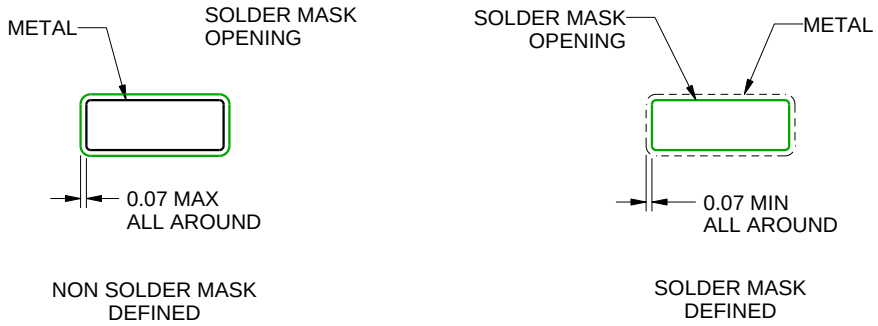


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

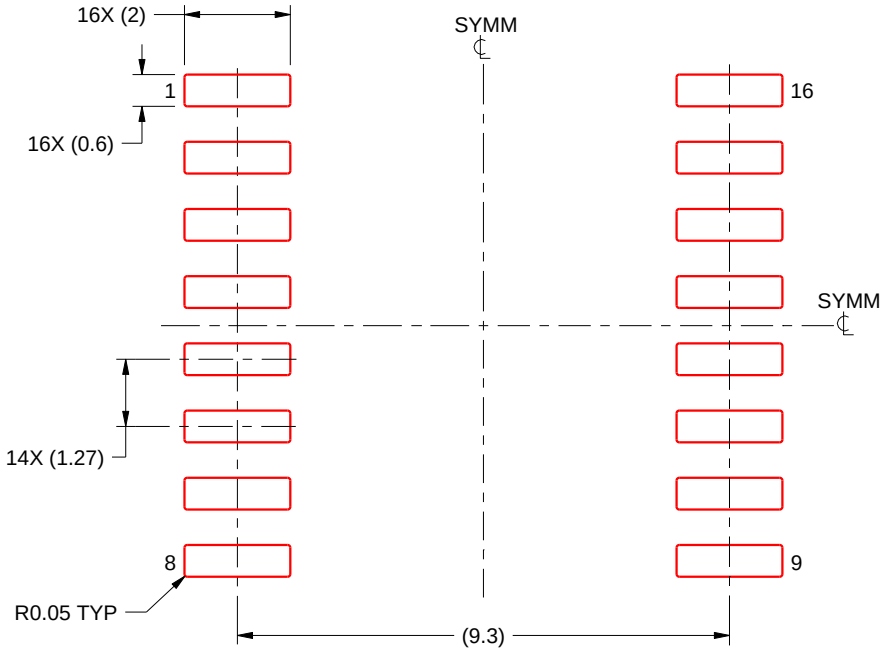


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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