LMK1D210xL Ultra Low Additive Jitter LVDS Buffer

1 Features

- High-performance LVDS clock buffer family: up to 2GHz
  - Dual 1:2 differential buffer
  - Dual 1:4 differential buffer
  - Dual 1:6 differential buffer
  - Dual 1:8 differential buffer
- Supply voltage: 1.71V to 3.465V
- Dual output common mode voltage operation:
  - Output common mode voltage: 0.7V at 1.8V supply voltage.
  - Output common mode voltage: 1.2V at 2.5V/ 3.3V supply voltage
- Low additive jitter:
  - < 17fs RMS typical in 12kHz to 20MHz at 1250.25MHz
  - < 22fs RMS typical in 12kHz to 20MHz at 625MHz
  - < 60fs RMS maximum in 12kHz to 20MHz at 156.25MHz
  - Very low phase noise floor: -164dBc/Hz (typical at 156.25MHz)
- Very low propagation delay: < 575ps maximum
- Output skew:
  - 15ps maximum (LMK1D2102, LMK1D2104)
  - 20ps maximum (LMK1D2106, LMK1D2106)
- Part to Part skew: 150ps
- High-swing LVDS (boosted mode): 500mV VOD typical when AMP_SELA, AMP_SELB= Floating
- Bank enable/disable using AMP_SELA and AMP_SELB Section 8.4.1
- Fail-safe input operation
- Universal inputs accept LVDS, LVPECL, LVCMOS, HCSL and CML signal levels
- LVDS reference voltage, V_{AC_REF}, available for capacitive-coupled inputs
- Extended industrial temperature range: –40°C to 105°C

2 Applications

- Telecommunications and networking
- Medical imaging
- Test and measurement
- Wireless infrastructure
- Pro audio, video and signage

3 Description

The LMK1D210xL is a low noise dual clock buffer which distributes one input to a maximum of 2 (LMK1D2102L), 4 (LMK1D2104L), 6 (LMK1D2106L) or 8 (LMK1D2108L) LVDS outputs. The inputs can either be LVDS, LVPECL, HCSL, CML, or LVCMOS.

The LMK1D210xL is specifically designed for driving 50Ω transmission lines. When driving inputs in single-ended mode, apply the appropriate bias voltage to the unused negative input pin (see Figure 8-8).

LMK1D210xL buffer offers two output common mode operation (0.7V and 1.2V) for different operating supply. The device provides flexibility in design for DC-coupled mode applications.

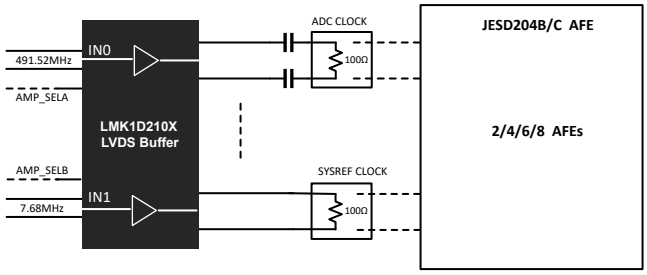
AMP_SELA / AMP_SELB control pin can be used to select different output amplitude LVDS (350mV) or boosted LVDS (500mV). In addition to amplitude selection, outputs can be disabled using the same pin.

The part also supports Fail-Safe Input function for clock and digital input pins. The device further incorporates an input hysteresis which prevents random oscillation of the outputs in the absence of an input signal.

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE(3)
LMK1D2102L	RGT (VQFN, 16)	3.00mm × 3.00mm
LMK1D2104L	RHD (VQFN, 28)	5.00mm × 5.00mm
LMK1D2106L	RHA (VQFN, 40)	6.00mm × 6.00mm
LMK1D2108L(2)	RGZ (VQFN, 48)	7.00mm × 7.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview only.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Example

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Device Comparison....3
5 Pin Configuration and Functions....5
6 Specifications....7
6.1 Absolute Maximum Ratings....7
6.2 ESD Ratings....7
6.3 Recommended Operating Conditions....7
6.4 Thermal Information....8
6.5 Electrical Characteristics....8
6.6 Typical Characteristics....12
7 Parameter Measurement Information....16
7.1 Differential Voltage Measurement Terminology....18
8 Detailed Description....20
8.1 Overview....20
8.2 Functional Block Diagram....20
8.3 Feature Description....21
8.4 Device Functional Modes....21
9 Application and Implementation....24
9.1 Application Information....24
9.2 Typical Application....24
9.3 Power Supply Recommendations....27
9.4 Layout....27
10 Device and Documentation Support....29
10.1 Documentation Support....29
10.2 Receiving Notification of Documentation Updates....29
10.3 Support Resources....29
10.4 Trademarks....29
10.5 Electrostatic Discharge Caution....29
10.6 Glossary....29
11 Revision History....29
12 Mechanical, Packaging, and Orderable Information....29
12.1 Tape and Reel Information....42

Copyright © 2024 Texas Instruments Incorporated

4 Device Comparison

Table 4-1. Device Comparison

DEVICE	DEVICE TYPE	FEATURES	OUTPUT SWING	OUTPUT COMMON MODE	PACKAGE	PACKAGE SIZE
LMK1D2102L	Dual 1:2	Global output bank enable and swing control pin.	350mV	0.7V[(2)]	VQFN (16)	3.00mm × 3.00mm
				1.2V		
			500mV	0.7V[(2)]		
				1V		
LMK1D2104L	Dual 1:4	Global output bank enable and swing control pin.	350mV	0.7V[(2)]	VQFN (28)	5.00mm × 5.00mm
				1.2V		
			500mV	0.7V[(2)]		
				1V		
LMK1D2106L	Dual 1:6	Individual output bank enable and swing control pin.	350mV	0.7V[(2)]	VQFN (40)	6.00mm × 6.00mm
				1.2V		
			500mV	0.7V[(2)]		
				1V		
LMK1D2108L	Dual 1:6	Individual output bank enable and swing control pin.	350mV	0.7V[(2)]	VQFN (48)	7.00mm × 7.00mm
				1.2		
			500mV	0.7V[(2)]		
				1V		
LMK1D2102	Dual 1:2	Global output enable control through pin control	350mV	1.2V	VQFN (16)	3.00mm × 3.00mm
LMK1D2104	Dual 1:4	Global output enable control through pin control	350mV	1.2V	VQFN (28)	5.00mm × 5.00mm
LMK1D2106	Dual 1:6	Global output enable and swing control through pin control	350mV	1.2V	VQFN (40)	6.00mm × 6.00mm
			500mV	1V		
LMK1D2108	Dual 1:8	Global output enable and swing control through pin control	350mV	1.2V	VQFN (48)	7.00mm × 7.00mm
			500mV	1V		
LMK1D1204	2:4	Global clock input selection and output enable control through pin control	350mV	1.2V	VQFN (16)	3.00mm × 3.00mm
LMK1D1204P	2:4	Individual output enable control through pin control	350mV	1.2V	VQFN (28)	5.00mm × 5.00mm
LMK1D1208	2:8	Global clock input selection and output enable control through pin control	350mV	1.2V	VQFN (28)	5.00mm × 5.00mm
LMK1D1208P	2:8	Individual output enable control through pin control	350mV	1.2V	VQGN (40)	6.00mm × 6.00mm
			500mV	1V		
LMK1D1208I	2:8	Individual output enable, swing, bank and clock input selection control through I^2C	350mV	1.2V	VQFN (40)	6.00mm × 6.00mm
			500mV	1V		
LMK1D1212	2:12	Global output enable and swing control through pin control	350mV	1.2V	VQFN (40)	6.00mm × 6.00mm
			500mV	1V		
LMK1D1216	2:16	Global output enable and swing control through pin control	350mV	1.2V	VQFN (48)	7.00mm × 7.00mm
			500mV	1V		

Copyright © 2024 Texas Instruments Incorporated

Table 4-1. Device Comparison (continued)

DEVICE	DEVICE TYPE	FEATURES	OUTPUT SWING	OUTPUT COMMON MODE	PACKAGE	PACKAGE SIZE
LMK1D1204I[1]	2:4	Individual output enable, swing, bank and clock input selection control through I^2C	350mV	1.2V	VQFN (16)	3.00mm × 3.00mm
			500mV	1V		
LMK1D1212I[1]	2:12	Individual output enable, swing, bank and clock input selection control through I^2C	350mV	1.2V	VQFN (40)	6.00mm × 6.00mm
			500mV	1V		
LMK1D1216I[1]	2:16	Individual output enable, swing, bank and clock input selection control through I^2C	350mV	1.2V	VQFN (48)	7.00mm × 7.00mm
			500mV	1V		
LMK1D1204L[1]	2:4	Global output bank enable and swing control pin.	350mV	0.7V[2]	VQFN (16)	3.00mm × 3.00mm
				1.2V		
LMK1D1208L[1]	2:8	Global output bank enable and swing control pin.	350mV	0.7V[2]	VQFN (28)	5.00mm × 5.00mm
				1.2V		
LMK1D1208PL[1]	2:8	Individual output enable control through pin control	350mV	0.7V[2]	VQFN (40)	6.00mm × 6.00mm
				1.2V		
			500mV	0.7V[2]		
				1V		
LMK1D1212L[1]	2:12	Individual output bank enable and swing control pin.	350mV	0.7V[2]	VQFN (40)	6.00mm × 6.00mm
				1.2V		
			500mV	0.7V[2]		
				1V		
LMK1D1216L[1]	2:16	Individual output bank enable and swing control pin.	350mV	0.7V[2]	VQFN (48)	7.00mm × 7.00mm
				1.2V		
			500mV	0.7V[2]		
				1V		
LMK1D1212IL[1]	2:12	Individual output enable, swing, bank and clock input selection control through I^2C	350mV	0.7V[2]	VQFN (40)	6.00mm × 6.00mm
				1V		
			500mV	0.7V[2]		
				1V		
LMK1D1216IL[1]	2:16	Individual output enable, swing, bank and clock input selection control through I^2C	350mV	0.7V[2]	VQFN (48)	7.00mm × 7.00mm
				1.2V		
			500mV	0.7V[2]		
				1V		

(1) Contact TI for more information on the device.
(2) 0.7V output common mode is only supported for VDD = 1.8V ± 5%.

Copyright © 2024 Texas Instruments Incorporated

5 Pin Configuration and Functions

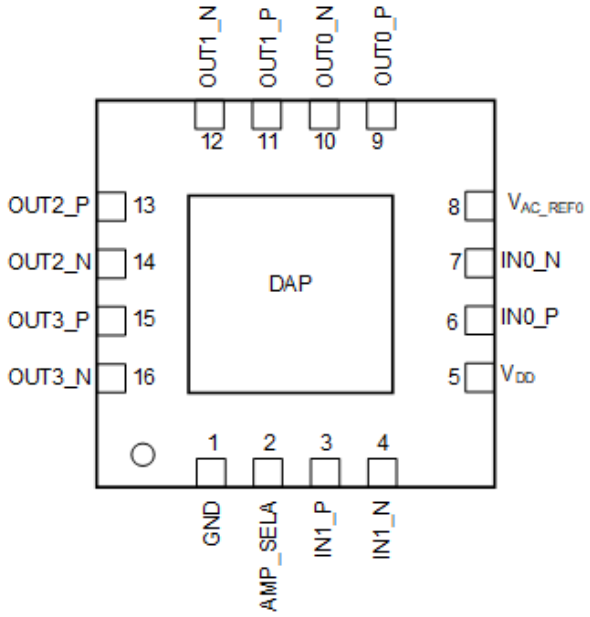


Figure 5-1. LMK1D2102L: RGT Package 16-Pin VQFN Top View

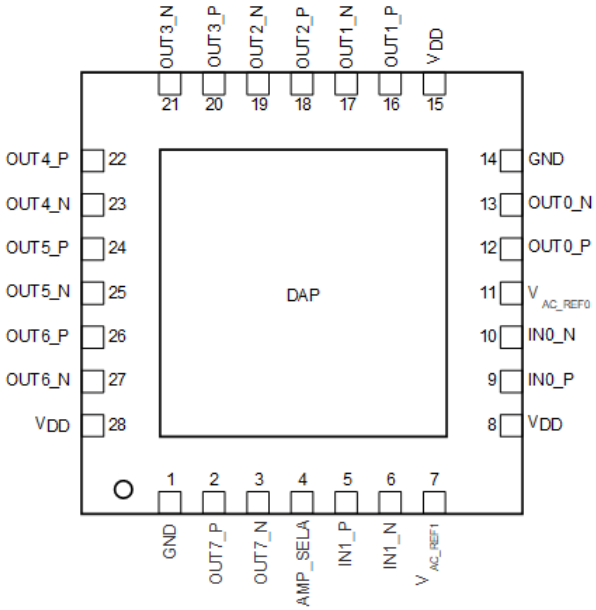


Figure 5-2. LMK1D2104L: RHD Package 28-Pin VQFN Top View

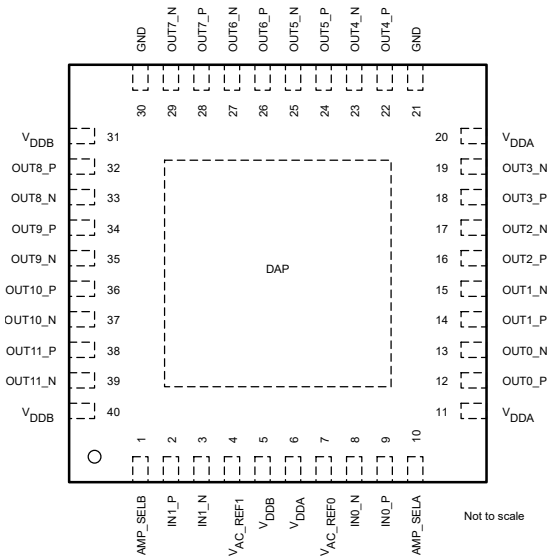


Figure 5-3. LMK1D2106L: RHA Package 40-Pin VQFN Top View

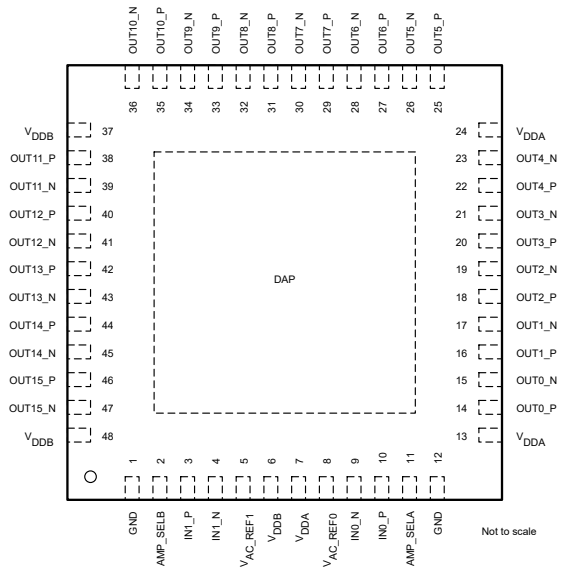


Figure 5-4. LMK1D2108L: RGZ Package 48-Pin VQFN Top View

Table 5-1. Pin Functions

PIN					TYPE[1]	DESCRIPTION
NAME	LMK1D2102L	LMK1D2104L	LMK1D2106L	LMK1D2108L		
DIFFERENTIAL/SINGLE-ENDED CLOCK INPUT						
IN0_P, IN0_N	6, 7	9, 10	9, 8	10, 9	I	Primary: Differential input pair or single-ended input
IN1_P, IN1_N	3, 4	5, 6	2, 3	3, 4	I	Secondary: Differential input pair or single-ended input Note that INP0, INN0 are used indistinguishably with IN0_P, IN0_N.
BANK ENABLE AND AMPLITUDE SELECT						
AMP_SELA	2	4	10	11	I	Output bank enable/disable with an internal 500kΩ pullup and 320kΩ pulldown; (See Section 8.4.1)
AMP_SELB	-	-	1	2	I	Output bank enable/disable with an internal 500kΩ pullup and 320kΩ pulldown; (See Section 8.4.1)
BIAS VOLTAGE OUTPUT						
V_{AC_REF0}	8	11	7	8	O	Bias voltage output for capacitive coupled inputs. If used, TI recommends using a 0.1µF capacitor to GND on this pin.
V_{AC_REF1}	-	-	4	5	O	Bias voltage output for capacitive coupled inputs. If used, TI recommends using a 0.1µF capacitor to GND on this pin.
DIFFERENTIAL CLOCK OUTPUT						
OUT0_P, OUT0_N	9, 10	12, 13	12, 13	14, 15	O	Differential LVDS output pair number 0
OUT1_P, OUT1_N	11, 12	16, 17	14, 15	16, 17	O	Differential LVDS output pair number 1
OUT2_P, OUT2_N	13, 14	18, 19	16, 17	18, 19	O	Differential LVDS output pair number 2
OUT3_P, OUT3_N	15, 16	20, 21	18, 19	20, 21	O	Differential LVDS output pair number 3
OUT4_P, OUT4_N	-	22, 23	22, 23	22, 23	O	Differential LVDS output pair number 4
OUT5_P, OUT5_N	-	24, 25	24, 25	25, 26	O	Differential LVDS output pair number 5
OUT6_P, OUT6_N	-	26, 27	26, 27	27, 28	O	Differential LVDS output pair number 6
OUT7_P, OUT7_N	-	2, 3	28, 29	29, 30	O	Differential LVDS output pair number 7
OUT8_P, OUT8_N	-	-	32, 33	31, 32	O	Differential LVDS output pair number 8
OUT9_P, OUT9_N	-	-	34, 35	33, 34	O	Differential LVDS output pair number 9
OUT10_P, OUT10_N	-	-	36, 37	35, 36	O	Differential LVDS output pair number 10
OUT11_P, OUT11_N	-	-	38, 39	38, 39	O	Differential LVDS output pair number 11
OUT12_P, OUT12_N	-	-	-	40, 41	O	Differential LVDS output pair number 12
OUT13_P, OUT13_N	-	-	-	42, 43	O	Differential LVDS output pair number 13
OUT14_P, OUT14_N	-	-	-	44, 45	O	Differential LVDS output pair number 14
OUT15_P, OUT15_N	-	-	-	46, 47	O	Differential LVDS output pair number 15
SUPPLY VOLTAGE						
V_{DD}	5	8, 15, 28	-	-	P	Device power supply (1.8V, 2.5V, or 3.3V) for Bank 0 and Bank 1
V_{DDA}	-	-	6, 11, 20	7, 13, 24	P	Device power supply (1.8V, 2.5V, or 3.3V) for Bank 0
V_{DDB}	-	-	5, 31, 40	6, 37, 48	P	Device power supply (1.8V, 2.5V, or 3.3V) for Bank 1
GROUND						
GND	1	1, 14	21, 30	1, 12	G	Ground
MISC						

Copyright © 2024 Texas Instruments Incorporated

Table 5-1. Pin Functions (continued)

PIN					TYPE[1]	DESCRIPTION
NAME	LMK1D2102L	LMK1D2104L	LMK1D2106L	LMK1D2108L		
DAP	DAP	DAP	DAP	DAP	G	Die Attach Pad. Connect to the printed circuit board (PCB) ground plane for heat dissipation.

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.3	3.6	V
V_{IN}	Input voltage	–0.3	3.6	V
V_O	Output voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input current	–20	20	mA
I_O	Continuous output current	–50	50	mA
T_J	Junction temperature		135	°C
T_{stg}	Storage temperature [2]	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Device unpowered

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Core supply voltage	3.3V supply	3.135	3.3	3.465	V
		2.5V supply	2.375	2.5	2.625	
		1.8V supply	1.71	1.8	1.89	
Supply Ramp	Supply voltage ramp	Requires monotonic ramp (10-90% of V_{DD})	0.1		20	ms
T_A	Operating free-air temperature		–40		105	°C
T_J	Operating junction temperature		–40		135	°C

6.4 Thermal Information

THERMAL METRIC [1]		LMK1D2102L	LMK1D2104L	LMK1D2106L	LMK1D2108L	UNIT
		VQFN	VQFN	VQFN	VQFN	
		16 PINS	28 PINS	40 PINS	48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.7	38.9	30.3	30.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	32.1	21.6	21.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.6	18.7	13.1	12.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.6	1	0.4	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23.6	18.7	13	12.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.6	8.2	4.5	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

VDD = 1.8V, 2.5V, 3.3V ± 5%, –40°C ≤ T_A ≤ 105°C. Typical values are at VDD = 1.8V, 2.5V, 3.3V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY CHARACTERISTICS						
IDD_{100M}	LMK1D2102L	All-outputs enabled, R_L = 100Ω, f =100MHz, AMP_SELA = 0		70	80	mA
IDD_{100M}	LMK1D2104L	All-outputs enabled, R_L = 100Ω, f =100MHz, AMP_SELA = 0		80	105	mA
IDD_{100M}	LMK1D2106L	All-outputs enabled, R_L = 100Ω, f =100MHz, AMP_SELA and AMP_SELB = 0		113	140	mA
IDD_{100M}	LMK1D2108L	All-outputs enabled, R_L = 100Ω, f =100MHz, AMP_SELA and AMP_SELB = 0		134	160	mA
IDD_{100M}	LMK1D2102L	All-outputs enabled, R_L = 100Ω, f =100MHz, AMP_SELA = Float		75	87	mA
IDD_{100M}	LMK1D2104L	All-outputs enabled, R_L = 100Ω, f =100MHz, AMP_SELA = Float		85	115	mA
IDD_{100M}	LMK1D2106L	All-outputs enabled, R_L = 100Ω, f =100MHz, AMP_SELA and AMP_SELB = Float		134	160	mA
IDD_{100M}	LMK1D2108L	All-outputs enabled, R_L = 100Ω, f =100MHz, AMP_SELA and AMP_SELB = Float		155	180	mA
$IDD_{POWER\ DOWN}$	LMK1D2102L	All-outputs disabled and unterminated, AMP_SELA = 1		50		mA
$IDD_{POWER\ DOWN}$	LMK1D2102L	All-outputs disabled, R_L = 100Ω, AMP_SELA = 1		65		mA
$IDD_{POWER\ DOWN}$	LMK1D2104L	All-outputs disabled and unterminated, AMP_SELA = 1		55		mA
$IDD_{POWER\ DOWN}$	LMK1D2104L	All-outputs disabled, R_L = 100Ω, AMP_SELA = 1		80		mA
$IDD_{POWER\ DOWN}$	LMK1D2106L	All-outputs disabled and unterminated, AMP_SELA and AMP_SELB = 1		75		mA

Copyright © 2024 Texas Instruments Incorporated

VDD = 1.8V, 2.5V, 3.3V ± 5%, –40°C ≤ T_A ≤ 105°C. Typical values are at VDD = 1.8V, 2.5V, 3.3V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$IDD_{POWER\ DOWN}$	LMK1D2106L	All-outputs disabled, R_L = 100Ω, AMP_SELA and AMP_SELB = 1		110		mA
$IDD_{POWER\ DOWN}$	LMK1D2108L	All-outputs disabled and unterminated, AMP_SELA and AMP_SELB = 1		80		mA
$IDD_{POWER\ DOWN}$	LMK1D2108L	All-outputs disabled, R_L = 100Ω, AMP_SELA and AMP_SELB = 1		130		mA
AMP_SELA / AMP_SELB INPUT CHARACTERISTICS						
Vd_{I3}	3-state input	Open / floating		0.4*V_{CC}		V
V_{IH}	Input high voltage	Minimum input voltage for a logical "1" state	0.7*V_{CC}		V_{CC} + 0.3	V
V_{IL}	Input low voltage	Maximum input voltage for a logical "0" state	–0.3		0.3*V_{CC}	V
I_{IH}	Input high current	V_{DD} can be 1.8V/2.5V/3.3V with V_{IH} = V_{DD}			30	µA
I_{IL}	Input low current	V_{DD} can be 1.8V/2.5V/3.3V with V_{IH} = V_{DD}	–30			µA
$R_{pull\text{-}up}$	Input pullup resistor (AMP_SELA, AMP_SELB)			500		kΩ
$R_{pull\text{-}down}$	Input pulldown resistor (AMP_SELA, AMP_SELB)			320		kΩ
SINGLE-ENDED LVCMOS/LVTTL CLOCK INPUT						
f_{IN}	Input frequency	Clock input	DC		250	MHz
$V_{IN_S\text{-}E}$	Single-ended Input Voltage Swing	Assumes a square wave input with two levels	0.4		3.465	V_{PP}
dVIN/dt	Input Slew Rate (20% to 80% of the amplitude)		0.05			V/ns
I_{IH}	Input high current	V_{DD} = 3.465V, V_{IH} = 3.465V			50	µA
I_{IL}	Input low current	V_{DD} = 3.465V, V_{IL} = 0V	-30			µA
C_{IN_SE}	Input capacitance	at 25°C		3.5		pF
DIFFERENTIAL CLOCK INPUT						
f_{IN}	Input frequency	Clock input			2	GHz
$V_{IN,DIFF(p\text{-}p)}$	Differential input voltage peak-to-peak {2*(V_{INP}-V_{INN})}	V_{ICM} = 1V (V_{DD} = 1.8V)	0.3		2.4	V_{PP}
		V_{ICM} = 1.25V (V_{DD} = 2.5V/3.3V)	0.3		2.4	
V_{ICM}	Input common mode voltage	$V_{IN,DIFF(P\text{-}P)}$ > 0.4V (V_{DD} = 1.8V/ 2.5V/3.3V)	0.25		2.3	V
I_{IH}	Input high current	V_{DD} = 3.465V, V_{INP} = 2.4V, V_{INN} = 1.2V			30	µA
I_{IL}	Input low current	V_{DD} = 3.465 V, V_{INP} = 0V, V_{INN} = 1.2V	–30			µA
$C_{IN_S\text{-}E}$	Input capacitance (Single-ended)	at 25°C		3.5		pF
LVDS DC OUTPUT CHARACTERISTICS						
|VOD|	Differential output voltage magnitude | V_{OUTP} - V_{OUTN}|	$V_{IN,DIFF(P\text{-}P)}$ = 0.3V_{PP}, R_L = 100Ω, AMP_SELA, AMP_SELB = 0	250	350	450	mV
|VOD|	Differential output voltage magnitude | V_{OUTP} - V_{OUTN}|	$V_{IN,DIFF(P\text{-}P)}$ = 0.3V_{PP}, R_L = 100Ω, AMP_SELA, AMP_SELB = Float	400	500	650	mV

VDD = 1.8V, 2.5V, 3.3V ± 5%, –40°C ≤ T_A ≤ 105°C. Typical values are at VDD = 1.8V, 2.5V, 3.3V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔVOD	Change in differential output voltage magnitude. Per output, defined as the difference between VOD in logic hi/lo states.	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, AMP_SELA, AMP_SELB = 0	–15		15	mV
ΔVOD	Change in differential output voltage magnitude	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, AMP_SELA, AMP_SELB = Float	–20		20	mV
$V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, V_{DD} = 1.8V, AMP_SELA, AMP_SELB = 0	0.6	0.7	0.8	V
$V_{OC(SS)}$	Steady-state common mode output voltage (LMK1D2104L, LMK1D2106L, LMK1D2108L)	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, V_{DD} = 1.8V, AMP_SELA, AMP_SELB = Float	0.6	0.7	0.8	V
$V_{OC(SS)}$	Steady-state common mode output voltage (LMK1D2102L)	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, V_{DD} = 1.8V, AMP_SELA, AMP_SELB = Float, T_A = -40°C to 105°C	0.6	0.7	0.82	V
$V_{OC(SS)}$	Steady-state common mode output voltage (LMK1D2102L)	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, V_{DD} = 1.8V, AMP_SELA, AMP_SELB = Float, T_A = -40°C to 85°C	0.6	0.7	0.8	V
$V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, V_{DD} = 2.5V/3.3V, AMP_SELA, AMP_SELB = 0	1.1		1.375	V
$V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, V_{DD} = 2.5V/3.3V, AMP_SELA, AMP_SELB = Float	0.9		1.15	V
$\Delta_{VOC(SS)}$	Change in steady-state common mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, AMP_SELA, AMP_SELB = 0	–15		-15	mV
$\Delta_{VOC(SS)}$	Change in steady-state common mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, AMP_SELA, AMP_SELB = Float	–20		20	mV
LVDS AC OUTPUT CHARACTERISTICS						
V_{ring}	Output overshoot and undershoot	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, f_{OUT} ≤ 491.52MHz	–0.1		0.1	V_{OD}
V_{OS}	Output AC common mode	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, AMP_SELA, AMP_SELB = 0		50	100	mV_{pp}
V_{OS}	Output AC common mode	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω, AMP_SELA, AMP_SELB = Float		75	150	mV_{pp}
V_{OS}	Output AC common mode	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω		50	100	mV_{pp}
I_{OS}	Short-circuit output current (differential)	V_{OUTP} = V_{OUTN}	–12		12	mA
$I_{OS(cm)}$	Short-circuit output current (common-mode)	V_{OUTP} = V_{OUTN} = 0	–24		24	mA
t_{PD}	Propagation delay	$V_{IN,DIFF(P-P)}$ = 0.3V_{PP}, R_L = 100Ω (1)	0.3		0.575	ns
$t_{SK, O}$	Output skew	Skew between outputs with the same load conditions			20	ps
$t_{SK, b}$	Output bank skew	Skew between the outputs within the same bank (2102L/2104L) (2)			15	ps
$t_{SK, b}$	Output bank skew	skew between the outputs within the same bank (2106L/2108L) (2)			17.5	ps

Copyright © 2024 Texas Instruments Incorporated

VDD = 1.8V, 2.5V, 3.3V ± 5%, –40°C ≤ T_A ≤ 105°C. Typical values are at VDD = 1.8V, 2.5V, 3.3V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SK, PP}$	Part-to-part skew	Skew between outputs on different parts subjected to the same operating conditions with the same input and output loading.			150	ps
$t_{SK, P}$	Pulse skew	50% duty cycle input, crossing point-to-crossing-point distortion (2)	–20		20	ps
$t_{RJIT(ADD)}$	Random additive Jitter (rms)	f_{IN} = 156.25MHz with 50% duty-cycle, Input slew rate = 1.5V/ns, Integration range = 12kHz - 20MHz, with output load R_L = 100Ω		45	60	fs, RMS
Phase noise	Phase Noise for a carrier frequency of 156.25MHz with 50% duty-cycle, Input slew rate = 1.5V/ns with output load R_L= 100Ω	PN_{1kHz}		–143		dBc/Hz
		PN_{10kHz}		-152		
		PN_{100kHz}		-157		
		PN_{1MHz}		-160		
		PN_{floor}		–164		
MUX_{ISO}	Mux Isolation	f_{IN} = 156.25MHz. The difference in power level at f_{IN} when the selected clock is active and the unselected clock is static versus when the selected clock is inactive and the unselected clock is active.		80		dB
SPUR	Spurious suppression between dual banks	Differential inputs with F_{IN0} = 491.52MHz, F_{IN1} = 61.44MHz; Measured between neighboring outputs		–60		dB
		Different inputs with F_{IN0} = 491.52MHz, F_{IN1} = 15.36MHz; Measured between neighboring outputs		–70		
ODC	Output duty cycle	With 50% duty cycle input	45		55	%
t_R/t_F	Output rise and fall time	20% to 80% with R_L = 100Ω			300	ps
V_{AC_REF}	Reference output voltage	VDD = 2.5V, I_{LOAD} = 100µA	0.9	1.25	1.375	V
POWER SUPPLY NOISE REJECTION (PSNR) V_{DD} = 2.5V / 3.3V						
PSNR	Power Supply Noise Rejection ($f_{carrier}$ = 156.25MHz)	10kHz, 100mVpp ripple injected on V_{DD}		–95		dBc
		1MHz, 100mVpp ripple injected on V_{DD}		–75		

(1) Measured between single-ended/differential input crossing point to the differential output crossing point.
(2) Defined as the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

6.6 Typical Characteristics

LMK1D210xL buffer typical characteristics are shown for current consumption, phase noise performance and timing diagrams and output common mode operation.

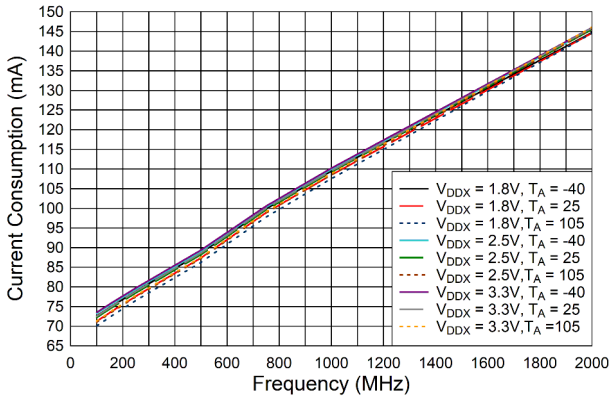


Figure 6-1. LMK1D2102L Current Consumption vs. Frequency, AMP_SELA = 0

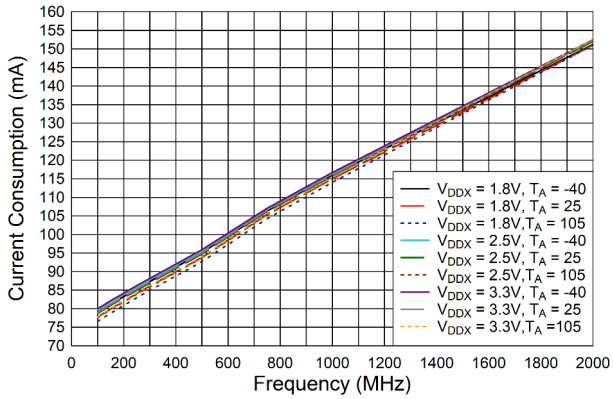


Figure 6-2. LMK1D2102L Current Consumption vs. Frequency, AMP_SELA = Floating

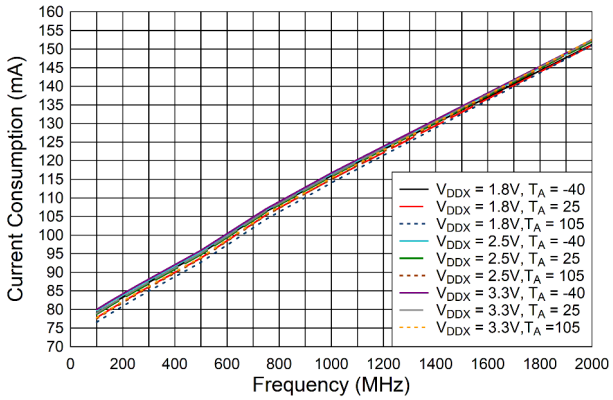


Figure 6-3. LMK1D2104L Current Consumption vs. Frequency, AMP_SELA = 0

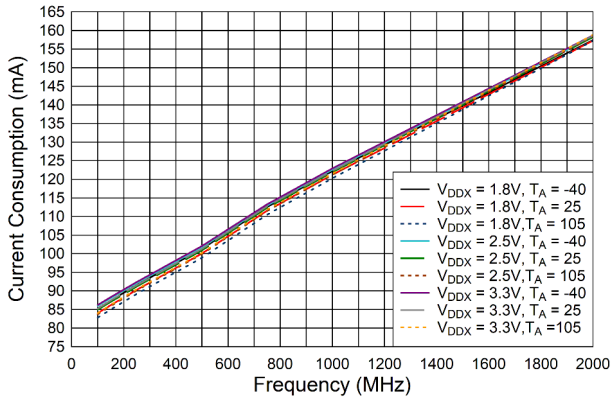


Figure 6-4. LMK1D2104L Current Consumption vs. Frequency, AMP_SELA = Floating

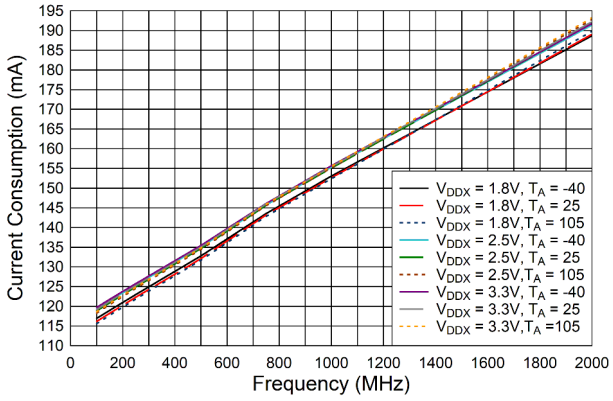


Figure 6-5. LMK1D2106L Current Consumption vs. Frequency, AMP_SELA and AMP_SELB = 0

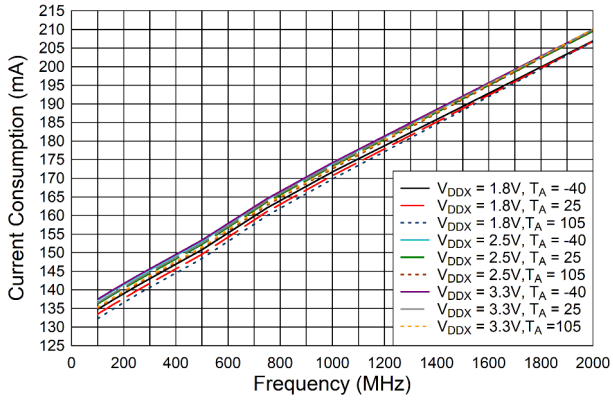


Figure 6-6. LMK1D2106L Current Consumption vs. Frequency, AMP_SELA and AMP_SELB = Floating

Copyright © 2024 Texas Instruments Incorporated

6.6 Typical Characteristics (continued)

LMK1D210xL buffer typical characteristics are shown for current consumption, phase noise performance and timing diagrams and output common mode operation.

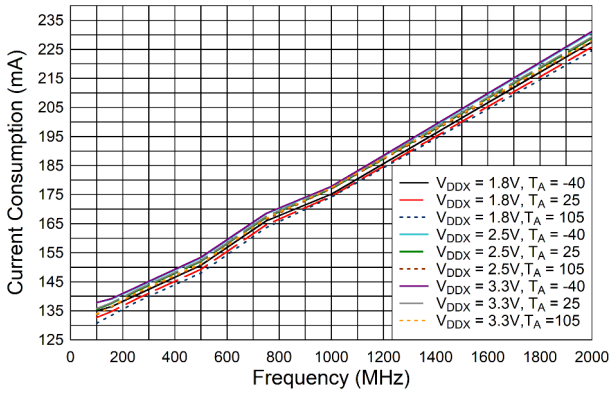


Figure 6-7. LMK1D2108L Current Consumption vs. Frequency, AMP_SELA and AMP_SELB = 0

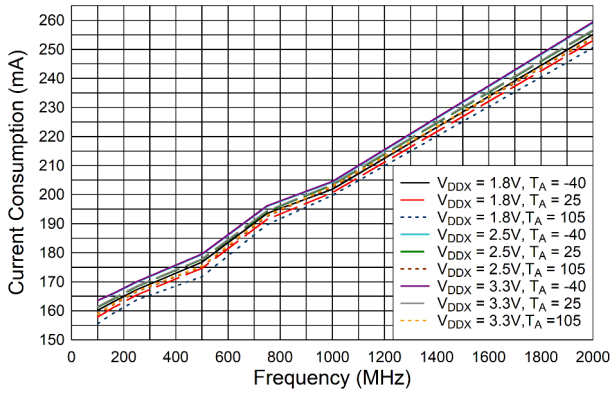


Figure 6-8. LMK1D2108L Current Consumption vs. Frequency, AMP_SELA and AMP_SELB = Floating

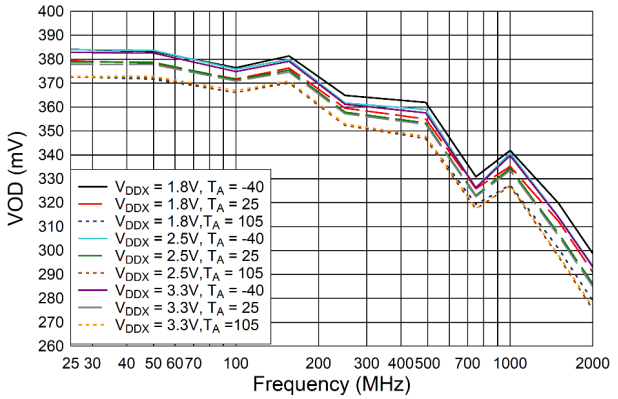


Figure 6-9. LMK1D210xL VOD vs. Frequency, AMP_SELA / AMP_SELB = 0

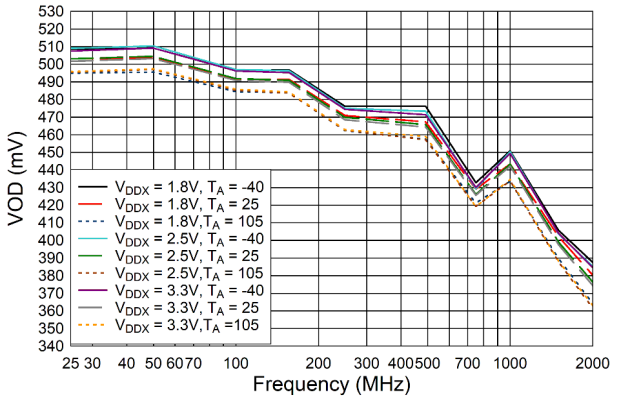


Figure 6-10. LMK1D210xL VOD vs. Frequency, AMP_SELA / AMP_SELB = Floating

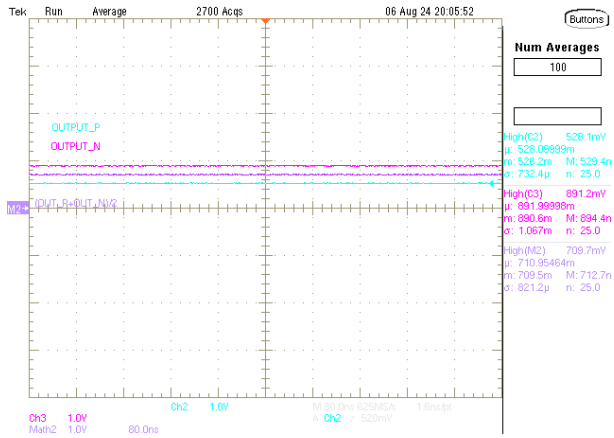


Figure 6-11. LMK1D210xL DC Output Common Mode at 1.8V Supply Condition, Differential Low (AMP_SELA / AMP_SELB = 0)

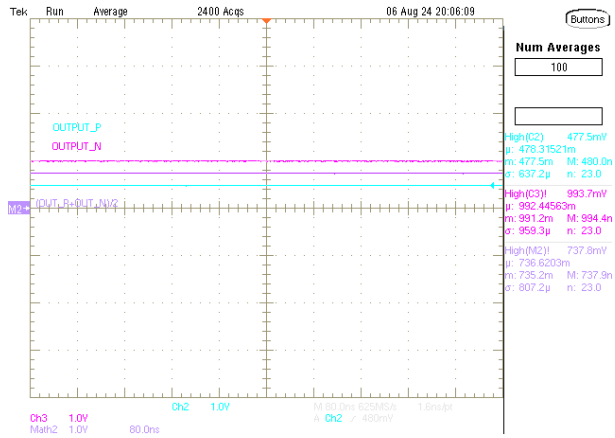


Figure 6-12. LMK1D210xL DC Output Common Mode at 1.8V Supply Condition, Differential Low (AMP_SELA / AMP_SELB = Float)

6.6 Typical Characteristics (continued)

LMK1D210xL buffer typical characteristics are shown for current consumption, phase noise performance and timing diagrams and output common mode operation.

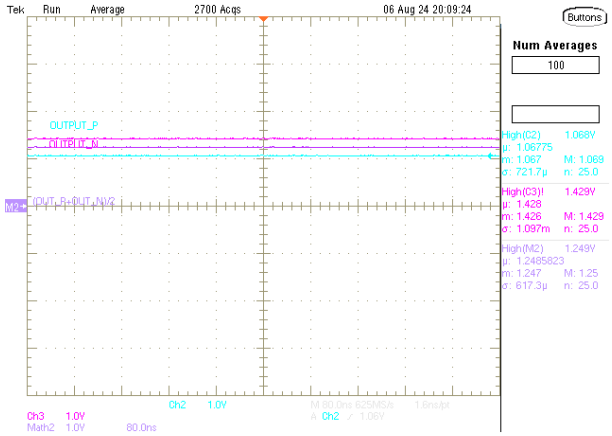


Figure 6-13. LMK1D210xL DC Output Common Mode at 2.5V/3.3V Supply Condition, Differential Low (AMP_SELA / AMP_SELB = 0)

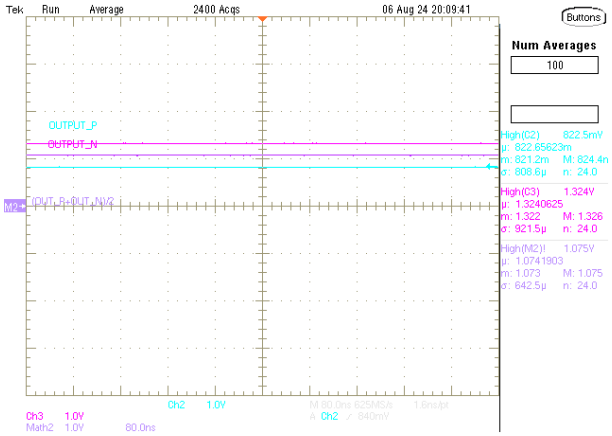


Figure 6-14. LMK1D210xL DC Output Common Mode at 2.5V/3.3V Supply Condition, Differential Low (AMP_SELA / AMP_SELB = Float)

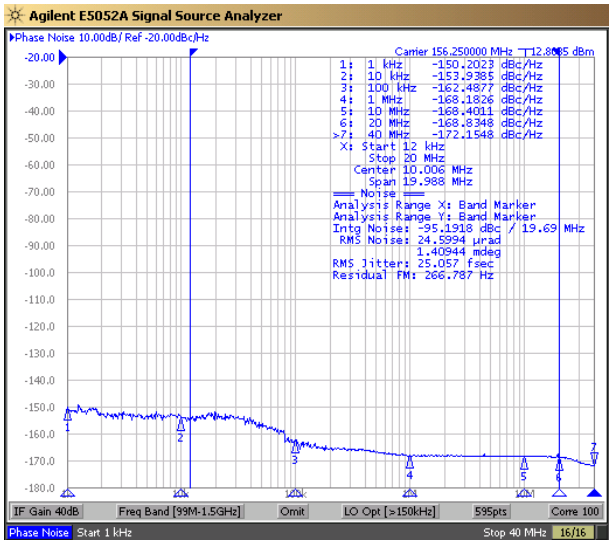
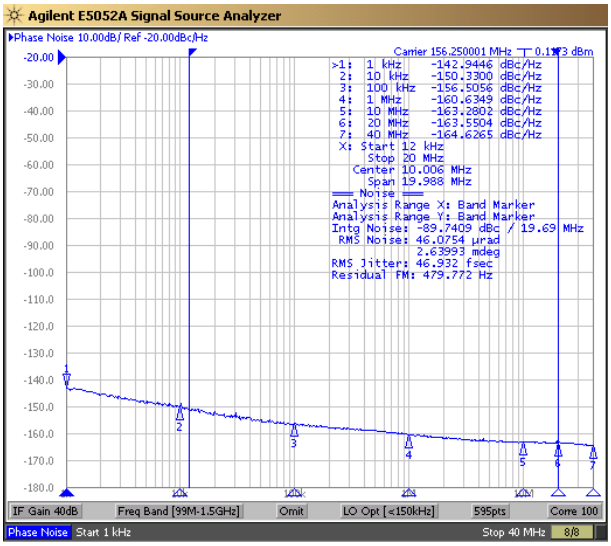


Figure 6-15. Input Source at 156.25MHz (12kHz - 20MHz)



See Note 1 and 2 in Graph Notes table

Figure 6-16. LMK1D210xL Phase Noise / Output Jitter at 156.25MHz (12kHz - 20MHz), Input Slew Rate = 1.5V/ns

Copyright © 2024 Texas Instruments Incorporated

6.6 Typical Characteristics (continued)

LMK1D210xL buffer typical characteristics are shown for current consumption, phase noise performance and timing diagrams and output common mode operation.

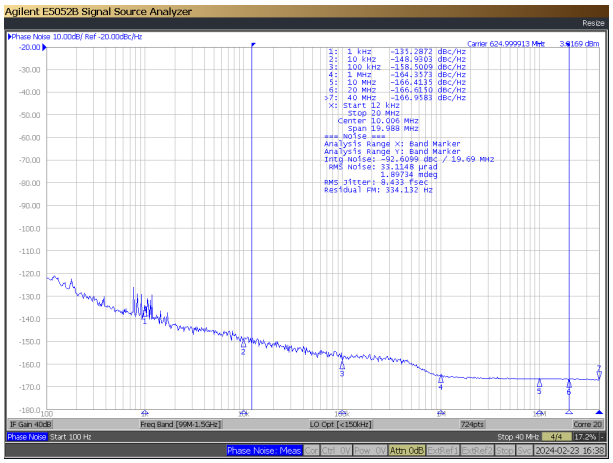
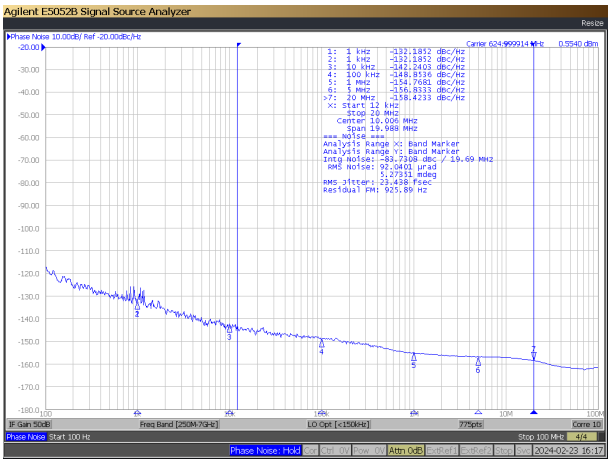


Figure 6-17. Input Source at 625MHz (12kHz - 20MHz)



See Note 1 and 3 in Graph Notes table

Figure 6-18. LMK1D210XL Phase Noise / Output Jitter at 625MHz (12kHz - 20MHz), Input Slew Rate >3V/ns

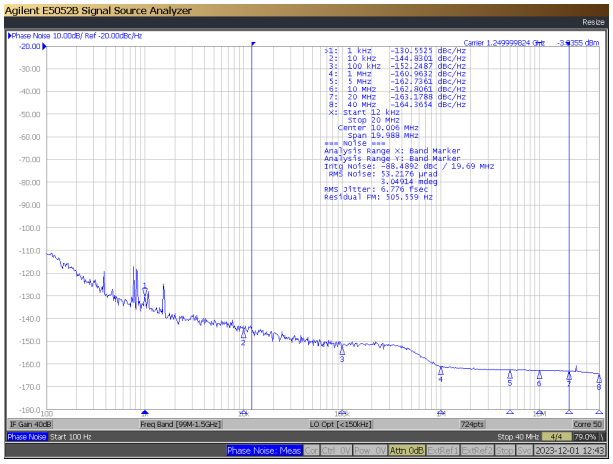
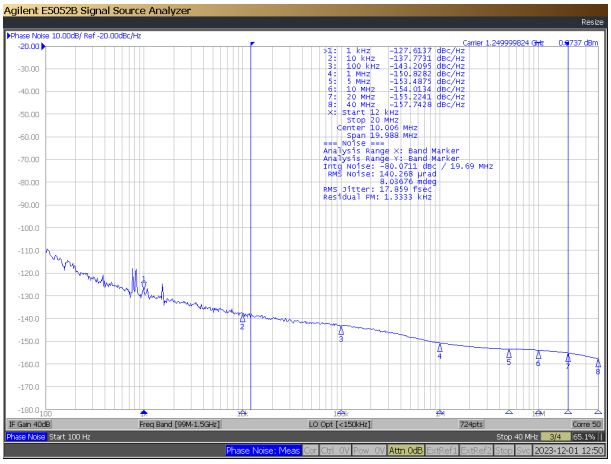


Figure 6-19. Input Source at 1250MHz (12kHz - 20MHz)



See Note 1 and 4 in Graph Notes table

Figure 6-20. LMK1D210XL Phase Noise / Output Jitter at 1250MHz (12kHz-20MHz), Input Slew Rate > 3V/ns

Table 6-1. Graph Notes

NOTE	
(1)	The typical RMS jitter values in the plots show the total output RMS jitter (J_{OUT}) for each frequency and the source clock RMS jitter (J_{SOURCE}). From these values, the Additive RMS Jitter can be calculated as: J_{ADD} = SQRT($J_{OUT}{}^2 - J_{SOURCE}{}^2$).
(2)	J_{ADD} at 156.25MHz = SQRT(46.932^2- 25.057^2) = 39.68fs.
(3)	J_{ADD} at 625MHz = SQRT(23.438^2- 8.433^2) = 21.87fs.
(4)	J_{ADD} at 1250MHz = SQRT(17.859^2- 6.776^2) = 16.52fs.

7 Parameter Measurement Information

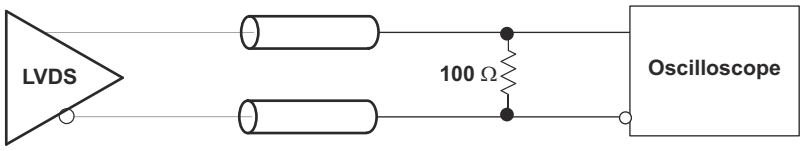


Figure 7-1. LVDS Output DC Configuration During Device Test

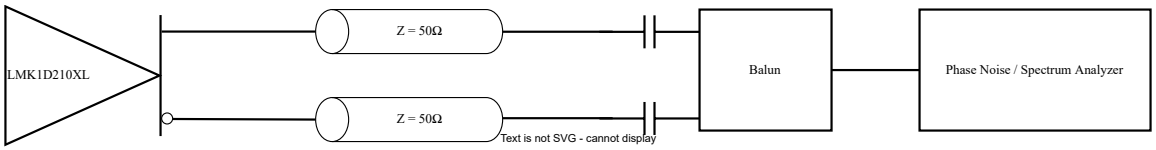


Figure 7-2. LVDS Output AC Configuration During Device Test

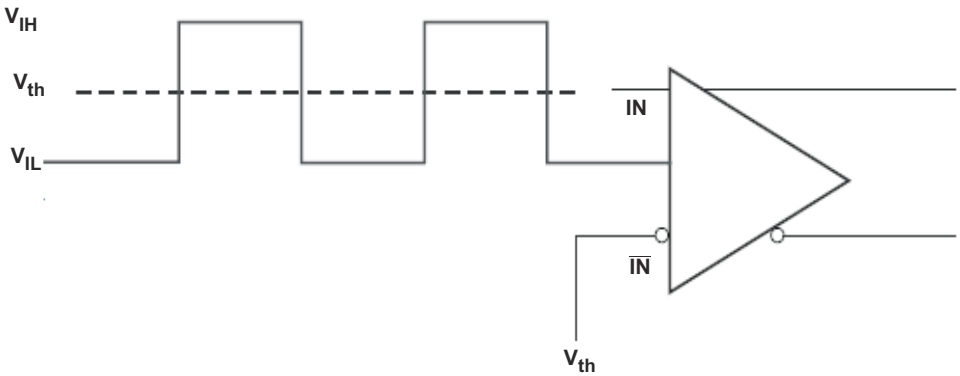


Figure 7-3. DC-Coupled LVCMOS Input During Device Test

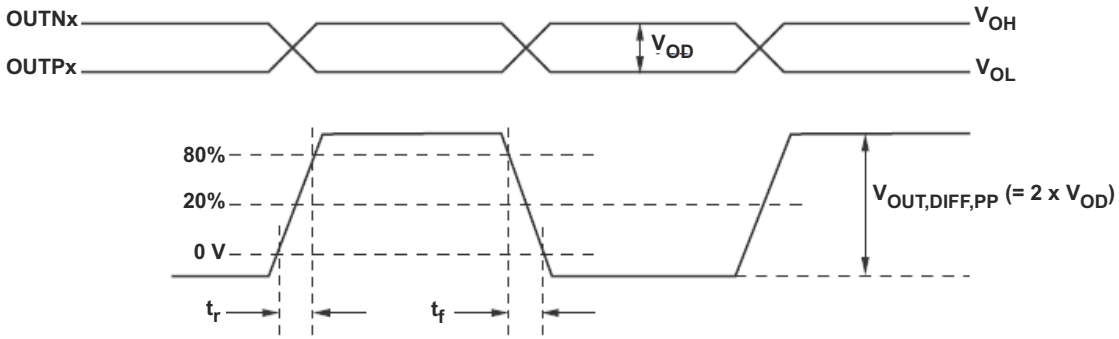
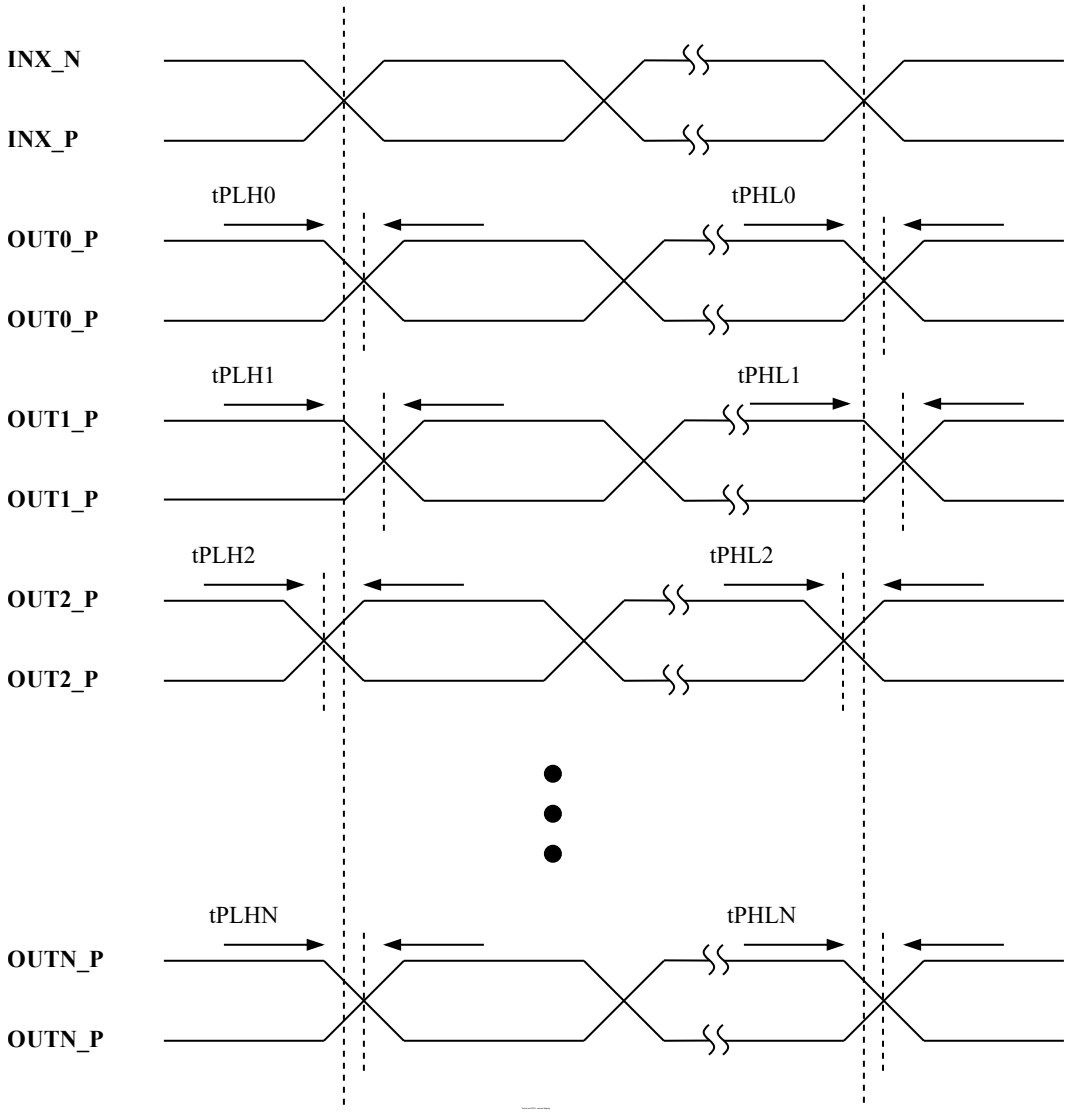


Figure 7-4. Output Voltage and Rise/Fall Time

Copyright © 2024 Texas Instruments Incorporated



A. Output skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1, 2, ..N)

B. Part-to-part skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} across multiple devices (n = 0, 1, 2, ..N)

Figure 7-5. Output Skew and Part-to-Part Skew

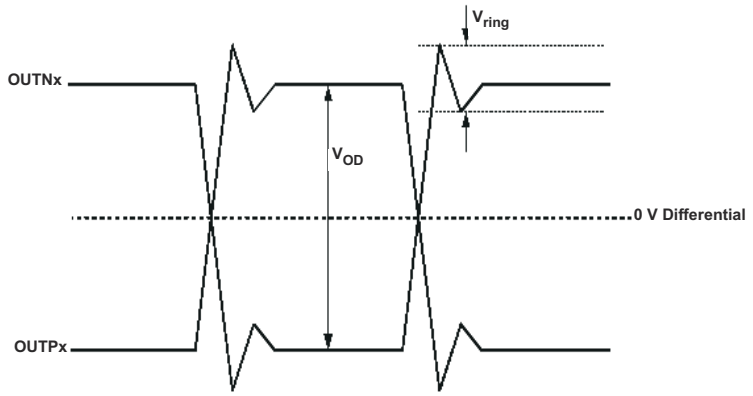


Figure 7-6. Output Overshoot and Undershoot

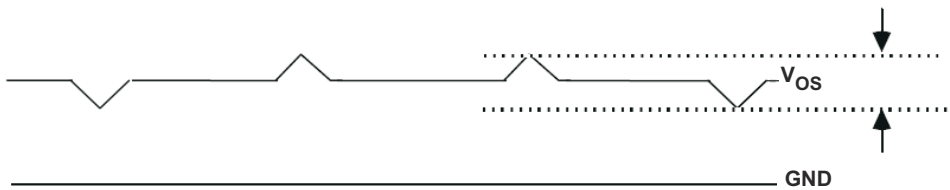


Figure 7-7. Output AC Common Mode

7.1 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading data sheets or communicating with other engineers. This section addresses the measurement and description of a differential signal so that the reader is able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and non-inverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the non-inverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, this signal only exists in reference to the differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

Figure 7-8 illustrates the two different definitions side-by-side for inputs and Figure 7-9 illustrates the two different definitions side-by-side for outputs. The V_{ID} (or V_{OD}) definition show the DC levels, V_{IH} and V_{OL} (or V_{OH} and V_{OL}), that the non-inverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the non-inverting signal voltage potential is now increasing and decreasing above and below the non-inverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

Copyright © 2024 Texas Instruments Incorporated

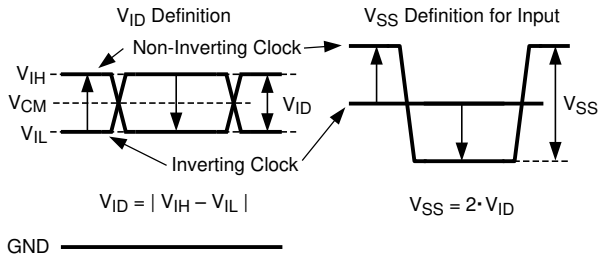


Figure 7-8. Two Different Definitions for Differential Input Signals

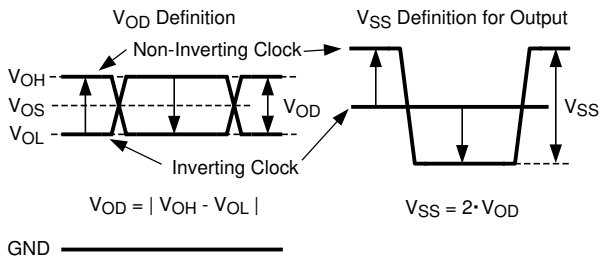


Figure 7-9. Two Different Definitions for Differential Output Signals

See also the AN-912 Common Data Transmission Parameters and their Definitions application note.

8 Detailed Description

8.1 Overview

The LMK1D210xL LVDS drivers use CMOS transistors to control the output current. Therefore, proper biasing and termination are required to provide correct operation of the device and to maximize signal integrity.

The proper LVDS termination for signal integrity over two 50Ω lines is 100Ω between the outputs on the receiver end. Either DC-coupled termination or AC-coupled termination can be used for LVDS outputs. TI recommends placing a termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common-mode voltage of the LMK1D210xL, AC coupling must be used. If the LVDS receiver has internal 100Ω termination, external termination must be omitted.

8.2 Functional Block Diagram

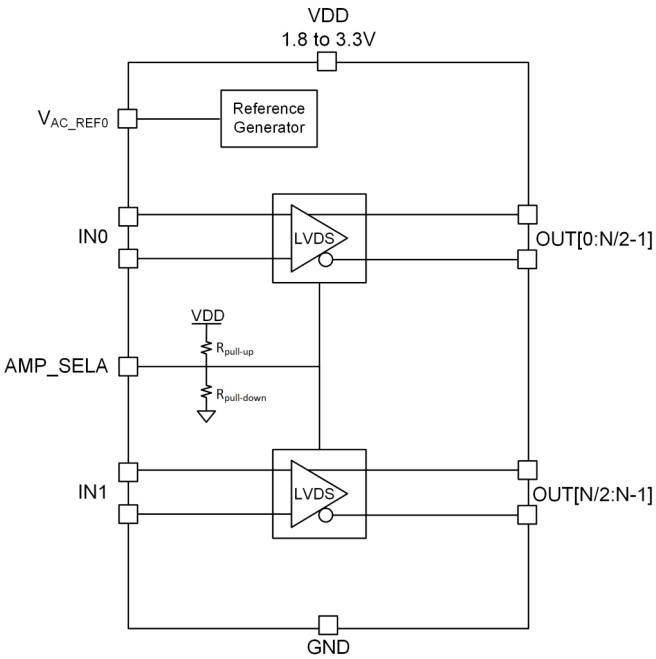


Figure 8-1. LMK1D2102 and LMK1D2104 Functional Block Diagram

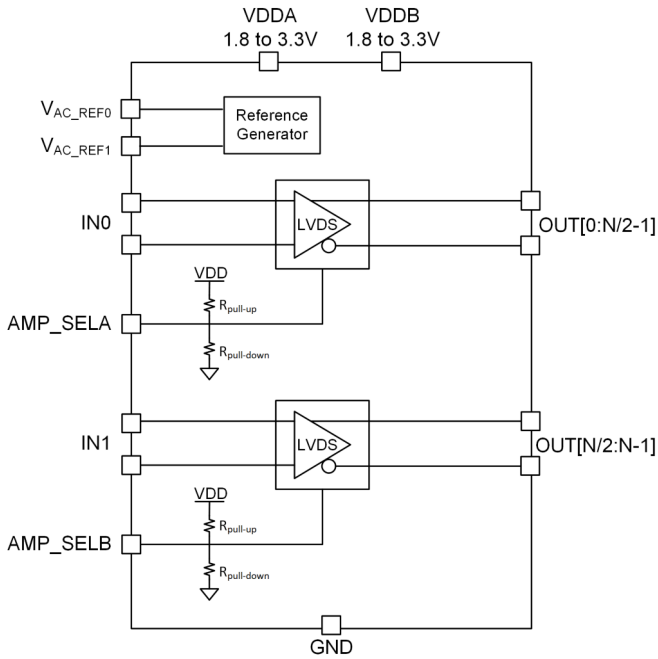


Figure 8-2. LMK1D2106 and LMK1D2108 Functional Block Diagram

Copyright © 2024 Texas Instruments Incorporated

8.3 Feature Description

The LMK1D210xL is a low additive jitter LVDS fan-out buffer that can generate up to 2 (LMK1D2102L), 4 (LMK1D2104L), 6 (LMK1D2106L) or 8 (LMK1D2108L) LVDS copies of a single input that is either LVDS, LVPECL, HCSL, CML, or LVCMOS on each of the banks. The device has two banks, therefore this translates to a total of 4 (LMK1D2102L), 8 (LMK1D2104L), 12 (LMK1D2106L) or 16 (LMK1D2108L) pairs of outputs. Refer to the Table 8-1 for output bank mapping. The reference clock frequencies can go up to 2GHz.

Table 8-1. Output Bank

Bank	LMK1D2102	LMK1D2104	LMK1D2106	LMK1D2108
0	OUT0 to OUT1	OUT0 to OUT3	OUT0 to OUT5	OUT0 to OUT7
1	OUT2 to OUT3	OUT4 to OUT7	OUT6 to OUT11	OUT8 to OUT15

8.3.1 Output Common Mode

LMK1D210xL family of buffer have multiple output common mode operations for flexibility in DC-coupled applications. Desired output common mode can be selected through supply. For LMK1D2106L and LMK1D2108L, VDDA and VDDB bank supplies needs to have same supply voltage for correct output common mode operation.Table 8-2 provides details on the output common mode over different supply options.

Table 8-2. LMK1D210xL Output Common Mode Operation

VDD = VDDA = VDDB ± 5% (V)	Output Amplitude (mV)	Output Common Mode (V)
1.8	350	0.7
2.5/3.3		1.2
1.8	500	0.7
2.5/3.3		1

8.3.2 Fail-Safe Input

The LMK1D210xL family of devices is designed to support fail-safe input operation. This feature allows the user to drive the device inputs before VDD is applied without damaging the device. Refer to the *Section 6.1* for more information on the maximum input supported by the device. The device also incorporates an input hysteresis, which prevents random oscillation in absence of an input signal, allowing the input pins to be left open.

8.4 Device Functional Modes

The output banks of the LMK1D210xL can be selected through the control pin (see Section 8.4.1). Unused inputs can be left floating to reduce overall component cost. Both AC- and DC-coupling schemes can be used with the LMK1D210xL to provide greater system flexibility.

8.4.1 Output Enable / Disable and Amplitude Selection

AMP_SELA and AMP_SELB pins can select different output swing and disable the outputs. LMK1D2102L and LMK1D2104L have only AMP_SELA pin to control both output banks globally while LMK1D2106L and LMK1D2108L have two pins (AMP_SELA, AMP_SELB) to control individual output banks.

Table 8-3. LMK1D2102L and LMK1D2104L Bank 0 and 1 AMP_SELA

AMP_SELA	Bank 0 and Bank 1 Output Amplitude (mV)
0	350
Float (default)	500
1	Outputs Disable (power-down)

Table 8-4. LMK1D2106L and LMK1D2108L Bank 0 AMP_SELA

AMP_SELA	Bank 0 Output Amplitude (mV)
0	350
Float (default)	500
1	Outputs Disable (power-down)

Table 8-5. LMK1D2106L and LMK1D2108L Bank 1 AMP_SELB

AMP_SELB	Bank 1 Output Amplitude (mV)
0	350
Float (default)	500
1	Outputs Disable (power-down)

8.4.2 LVDS Output Termination

TI recommends unused outputs to be terminated differentially with a 100Ω resistor for optimum performance, although unterminated outputs are also okay but results in slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

The LMK1D210xL can be connected to LVDS receiver inputs with DC and AC coupling as shown in Figure 8-3 and Figure 8-4, respectively.

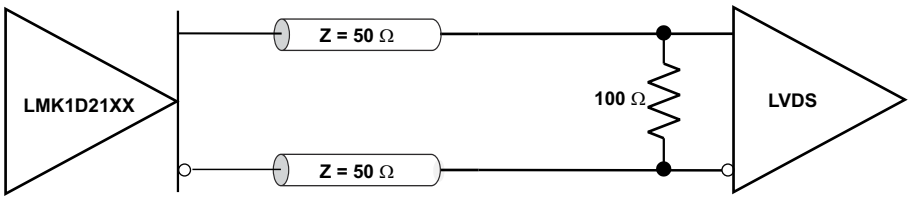


Figure 8-3. Output DC Termination

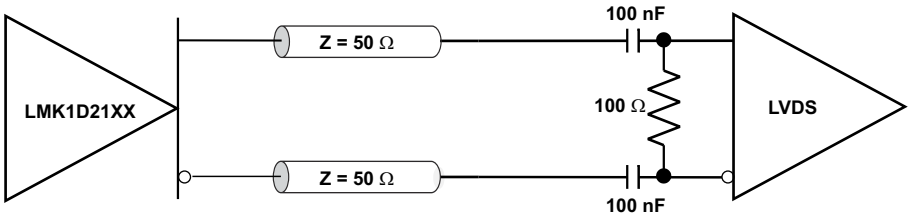


Figure 8-4. Output AC Termination (With the Receiver Internally Biased)

8.4.3 Input Termination

The LMK1D210xL inputs can be interfaced with LVDS, LVPECL, HCSL, or LVCMOS drivers.

LVDS drivers can be connected to LMK1D210xL inputs with DC and AC coupling as shown Figure 8-5 and Figure 8-6, respectively.

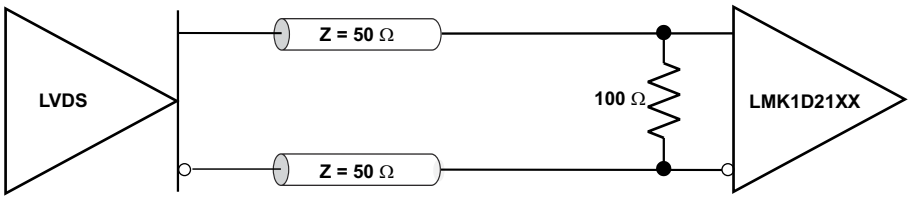


Figure 8-5. LVDS Clock Driver Connected to LMK1D210xL Input (DC-Coupled)

Copyright © 2024 Texas Instruments Incorporated

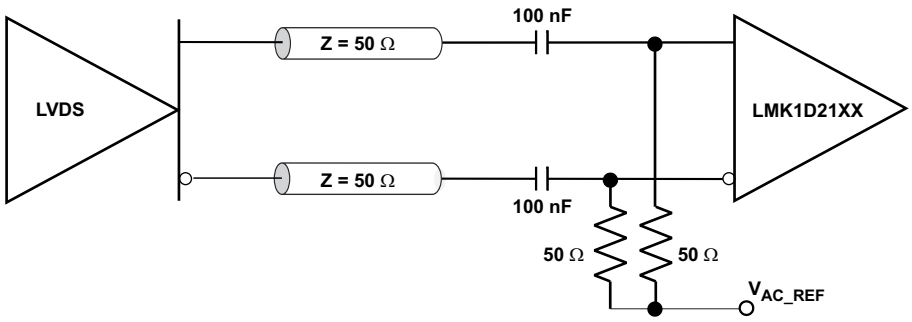


Figure 8-6. LVDS Clock Driver Connected to LMK1D210xL Input (AC-Coupled)

Figure 8-7 shows how to connect LVPECL inputs to the LMK1D210xL. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6V_{PP}.

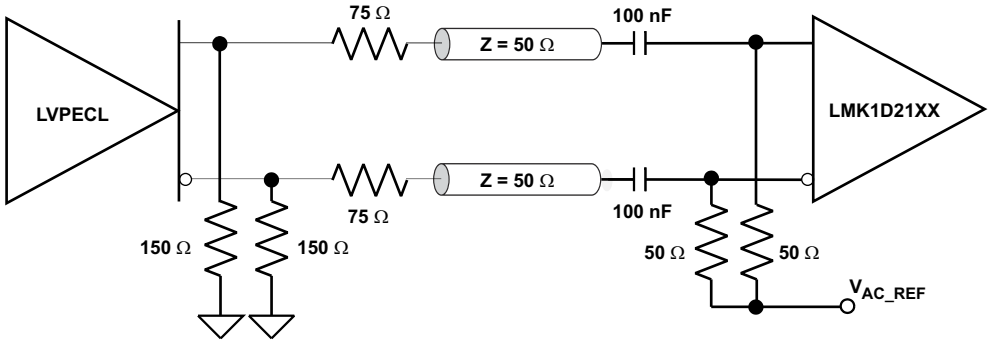


Figure 8-7. LVPECL Clock Driver Connected to LMK1D210xL Input

Figure 8-8 shows how to couple a LVCMOS clock input to the LMK1D210xL directly.

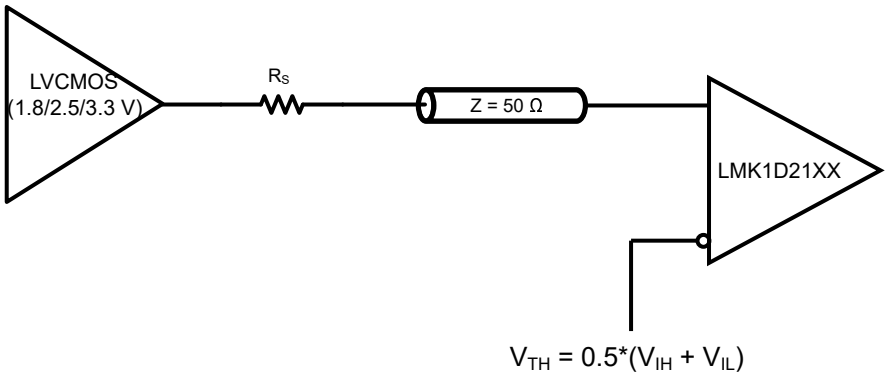


Figure 8-8. 1.8V, 2.5V, or 3.3V LVCMOS Clock Driver Connected to LMK1D210xL Input

For unused input, TI recommends grounding both input pins (INP, INN) using 1kΩ resistors.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMK1D210xL is a low additive jitter universal to LVDS fan-out buffer with dual inputs which fan-out to dual outputs bank. The small package size, 1.8-V power supply operation, low output skew, and low additive jitter is designed for applications that require high-performance clock distribution as well as for low-power and space-constraint applications.

9.2 Typical Application

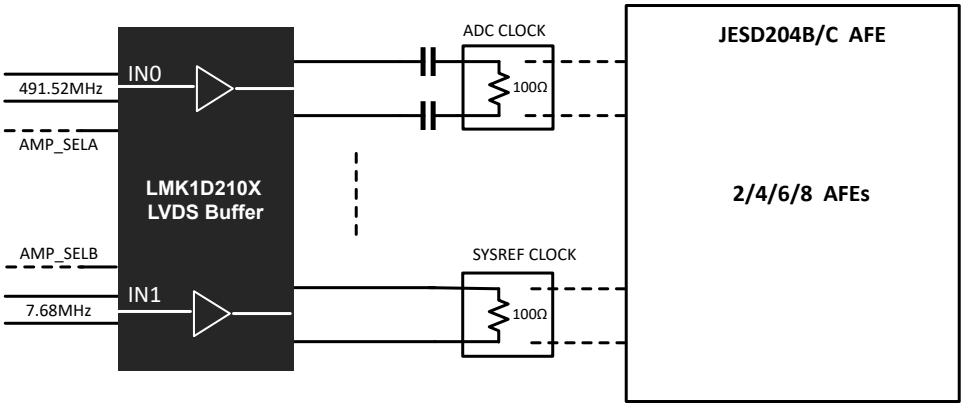


Figure 9-1. Fan-Out Buffer for ADC Device Clock and SYSREF Distribution

9.2.1 Design Requirements

The LMK1D210xL shown in Figure 9-1 is configured to fan-out an ADC clock on the first output bank and SYSREF clock on the second output bank for a system using the JESD204B/C ADC. The low output-to-output skew, very low additive jitter and superior spurious suppression between dual banks makes the LMK1D210xL a simple, robust and low-cost solution for distributing various clocks to JESD204B/C AFE systems. The configuration example can drive up to 2 to 8 ADC clocks and 2 to 8 SYSREF clocks for a JESD204B/C receiver with the following properties:

- The ADC clock receiver module is typically AC-coupled with an LVDS driver such as the LMK1D210xL due to differences in common-mode voltage between the driver and receiver. Depending on the receiver, there can an option for internal 100Ω differential termination in which case an external termination is not be required for the LMK1D210xL.
- The SYSREF clock receiver module is typically DC-coupled provided the common-mode voltage of the LMK1D210xL outputs match with the receiver. An external termination is not always necessary in case of an internal termination in the receiver.
- Unused outputs of the LMK1D210xL device are terminated differentially with a 100Ω resistor for optimum performance.

Copyright © 2024 Texas Instruments Incorporated

9.2.2 Detailed Design Procedure

See *Input Termination* for proper input terminations, dependent on single-ended or differential inputs.

See *LVDS Output Termination* for output termination schemes depending on the receiver application.

TI recommends unused outputs to be terminated differentially with a 100Ω resistor for optimum performance, although unterminated outputs are also okay but result in slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

In this application example, the ADC clock and SYSREF clocks require different output interfacing schemes. Power-supply filtering and bypassing is critical for low-noise applications.

LMK1D210xL offers multiple output common range to meet receiver requirement for an ADC or AFEs. In case of common-mode mismatch between the output voltage of the LMK1D210xL and the receiver, use AC coupling to fix the mismatch. AC coupling adds settling time associated with this AC-coupling network (High-pass filter), which can result in non-deterministic behavior during the initial transients. For such applications, DC-coupling the outputs is necessary and thus requires a scheme which can overcome the inherent mismatch between the common-mode voltage of the driver and receiver.

The application note *Interfacing LVDS Driver With a Sub-LVDS Receiver* discusses how to interface between a LVDS driver and sub-LVDS receiver. The same concept can be applied to interface the LMK1D210xL outputs to a receiver which has a lower common-mode voltage.

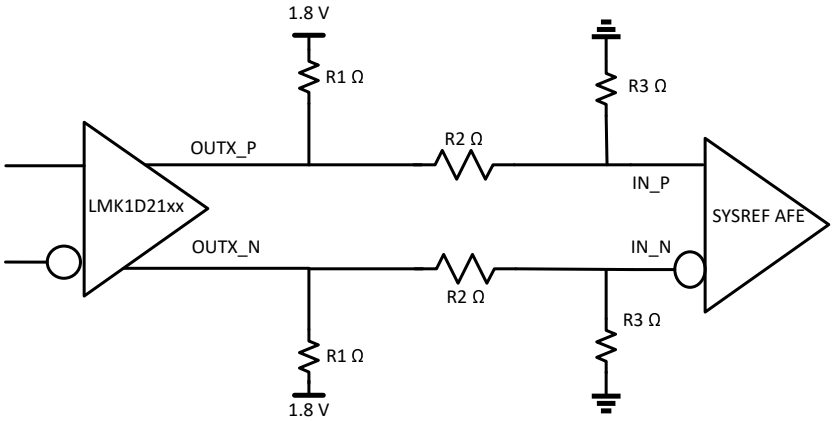
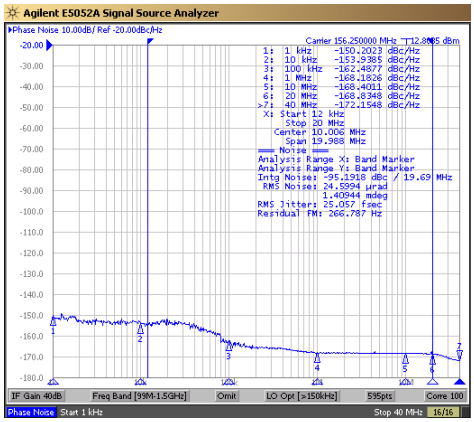


Figure 9-2. Schematic for DC-Coupling LMK1D210x With Lower Common-Mode Receiver

Figure 9-2 shows the resistor divider network for stepping down the common-mode voltage as explained in the previously mentioned application note. The resistors R1, R2 and R3 are selected according to the input common-mode voltage requirements of the receiver. As highlighted before, verify that the reduced swing is able to meet the requirements of the receiver. Higher swing mode (boosted LVDS swing mode) can be selected using the AMP_SEL pin highlighted in Section 8.4.1 to compensate for the reduced swing as the result of the resistor voltage divider.

9.2.3 Application Curves

The low additive noise of the LMK1D210xL. The low noise 156.25MHz source with 25fs RMS jitter, shown in Figure 9-3, drives the LMK1D210xL, resulting in 46.9fs RMS when integrated from 12kHz to 20MHz (Figure 9-4). The resultant additive jitter is a low 39.7-fs RMS for this configuration.



Note: Reference signal is a low-noise Rhode and Schwarz SMA100B

Figure 9-3. LMK1D210xL Reference Phase Noise, 156.25MHz, 25fs RMS (12kHz to 20MHz)

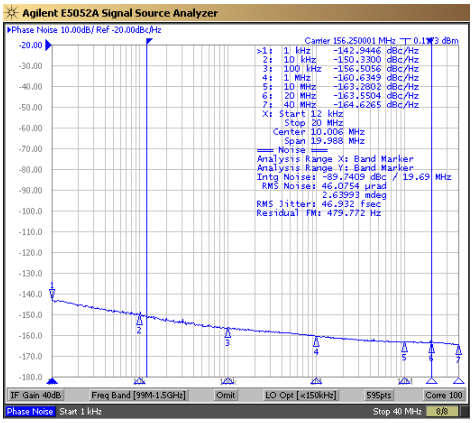


Figure 9-4. LMK1D210xL Output Phase Noise, 156.25MHz, 46.9fs RMS (12kHz to 20MHz)

Copyright © 2024 Texas Instruments Incorporated

9.3 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Reducing noise from the system power supply is essential, especially when jitter or phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly use the bypass capacitors, the capacitors must be placed close to the power-supply pins and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1µF) bypass capacitors as there are supply pins in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver. These ferrite beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low DC resistance because providing adequate isolation between the board supply and the chip supply is imperative, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

Figure 9-5 shows this recommended power-supply decoupling method.

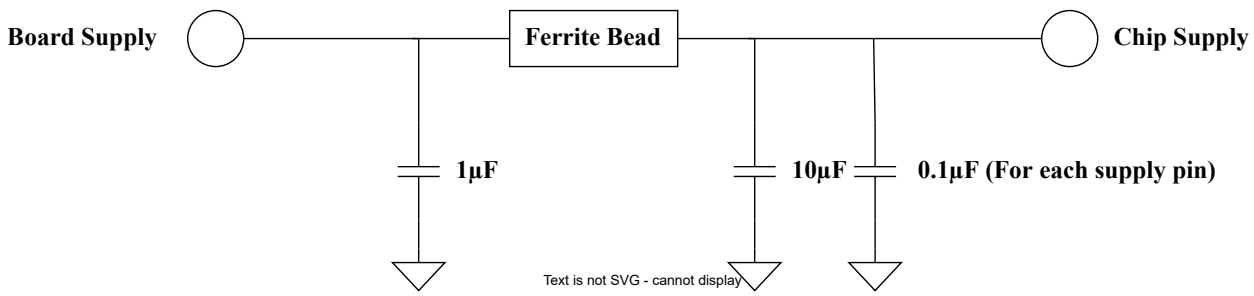


Figure 9-5. Power Supply Decoupling

9.4 Layout

9.4.1 Layout Guidelines

For reliability and performance reasons, the die temperature must be limited to a maximum of 135°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to provide adequate heat conduction to of the package. Section 9.4.2 show the recommended top layer and via patterns for the different packages.

9.4.2 Layout Examples

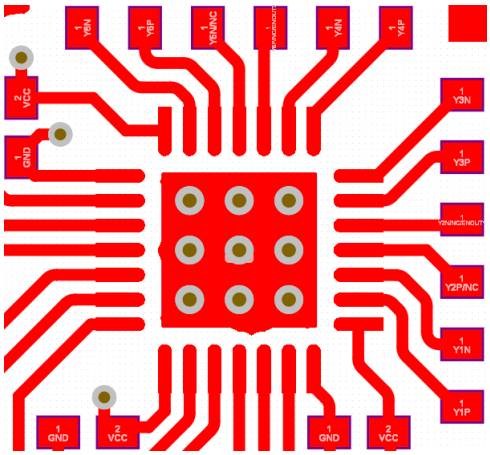


Figure 9-6. PCB Layout Example for LMK1D2104L, Top Layer

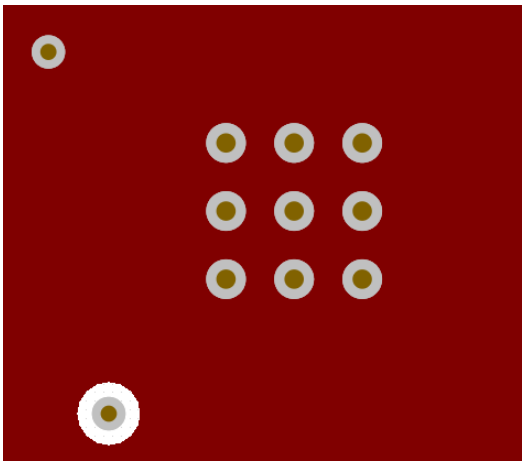


Figure 9-7. PCB Layout Example for LMK1D2104L, GND Layer

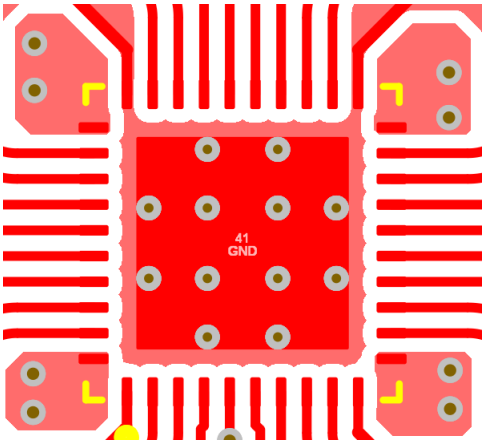


Figure 9-8. PCB Layout Example for LMK1D2106L, Top Layer

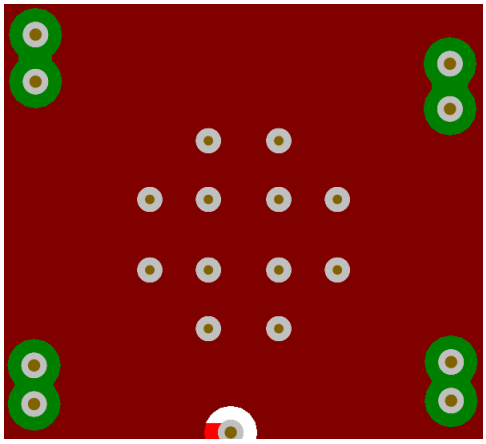


Figure 9-9. PCB Layout Example for LMK1D2106L, GND layer

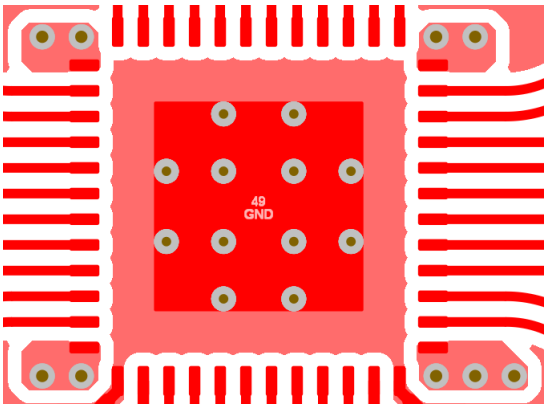


Figure 9-10. PCB Layout Example for LMK1D2108L, Top Layer

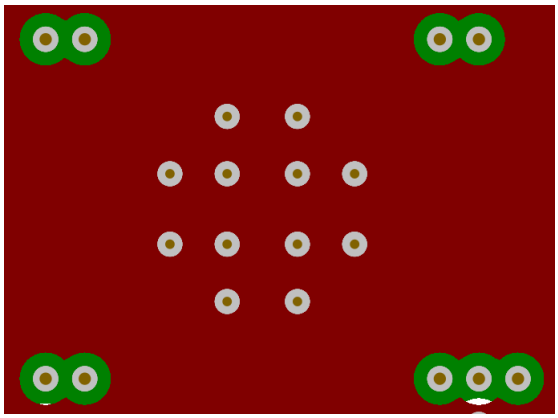


Figure 9-11. PCB Layout Example for LMK1D2108L, GND Layer

Copyright © 2024 Texas Instruments Incorporated

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board*, user's guide
- Texas Instruments, *Power Consumption of LVPECL and LVDS*, Analog design journal
- Texas Instruments, *Using Thermal Calculation Tools for Analog Components*, application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

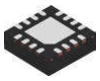
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September) to Revision A (November 2024)	Page

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

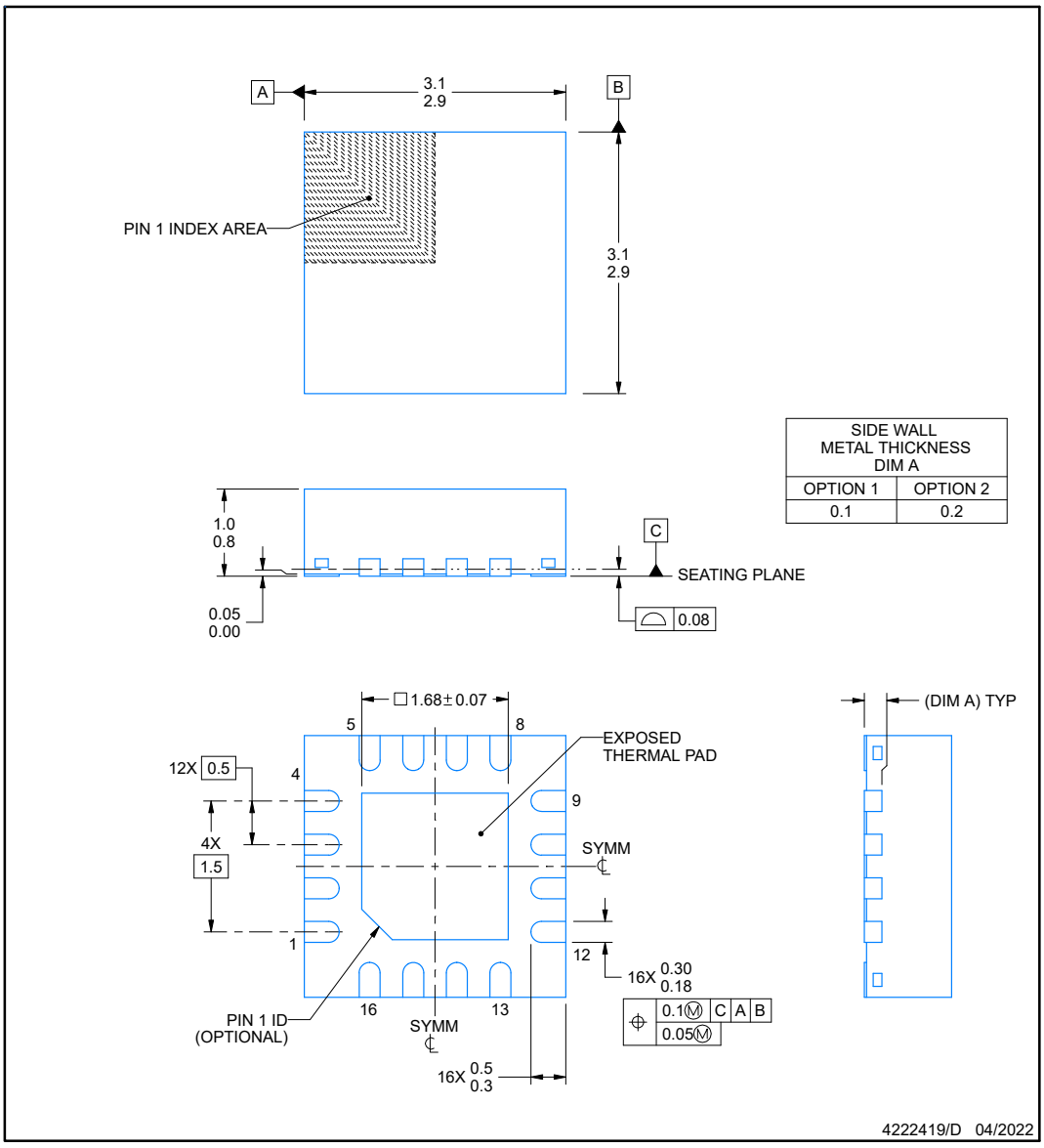
RGT0016C



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

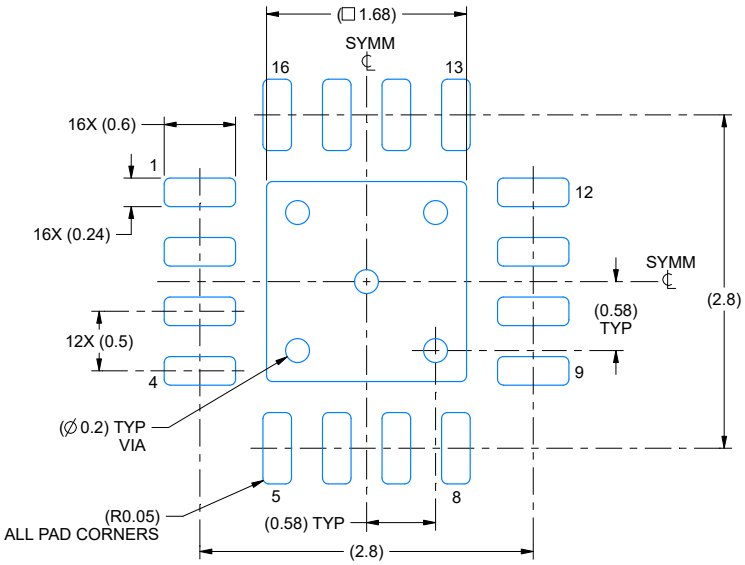
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

Copyright © 2024 Texas Instruments Incorporated

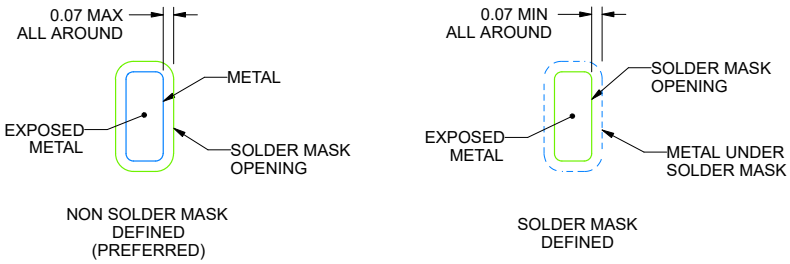
EXAMPLE BOARD LAYOUT

RGT0016C **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

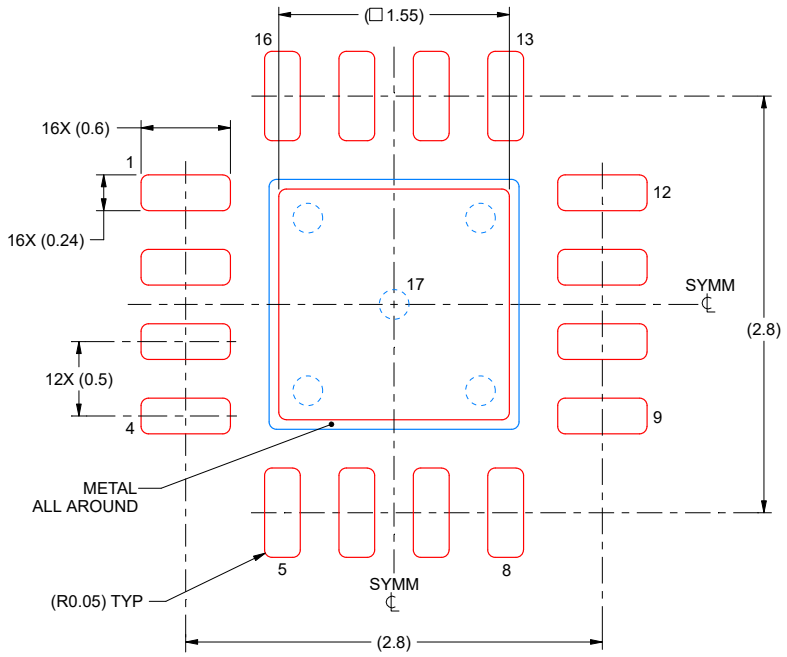
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

Copyright © 2024 Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

RGT0016C **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

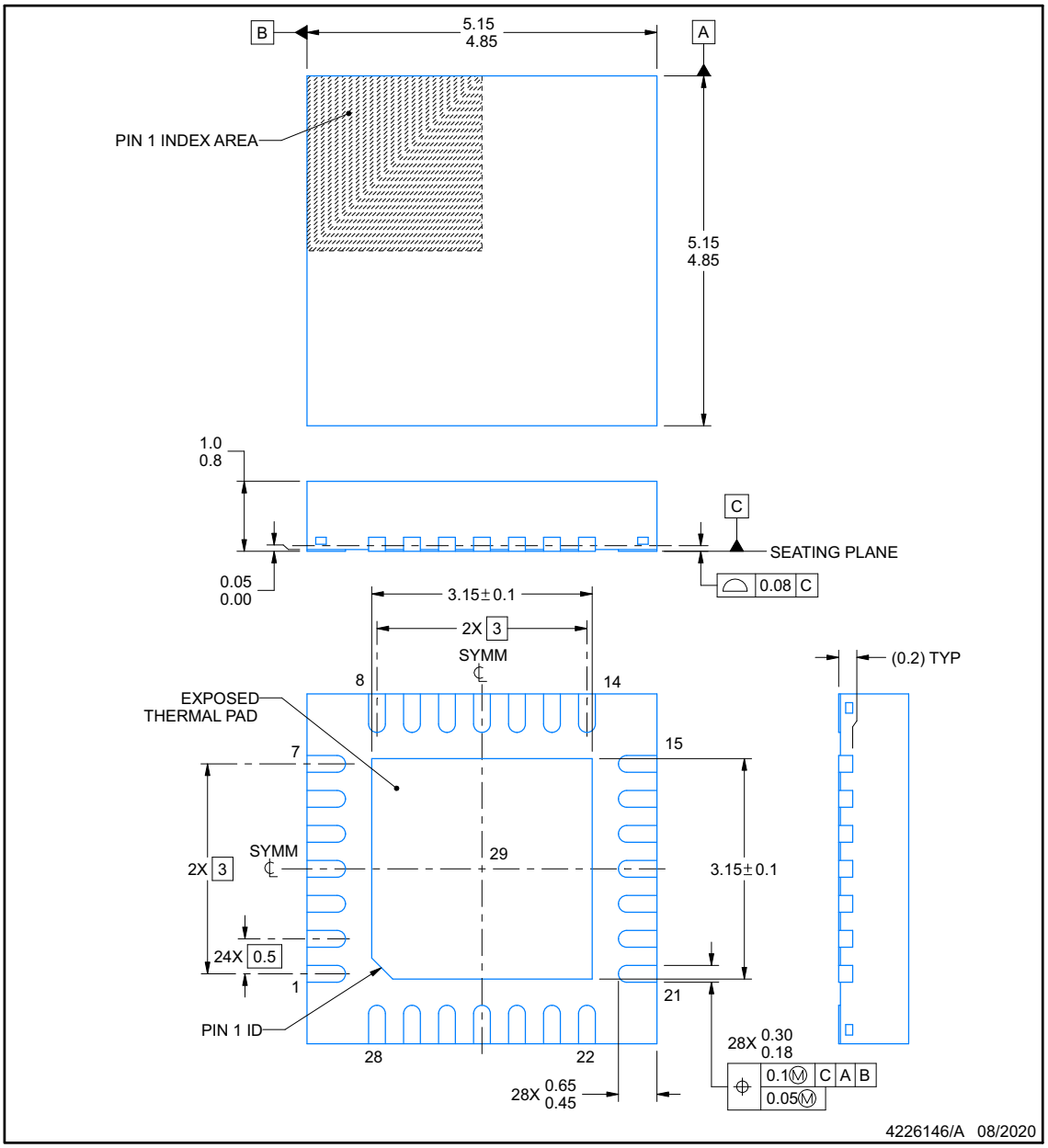
Copyright © 2024 Texas Instruments Incorporated

PACKAGE OUTLINE

RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

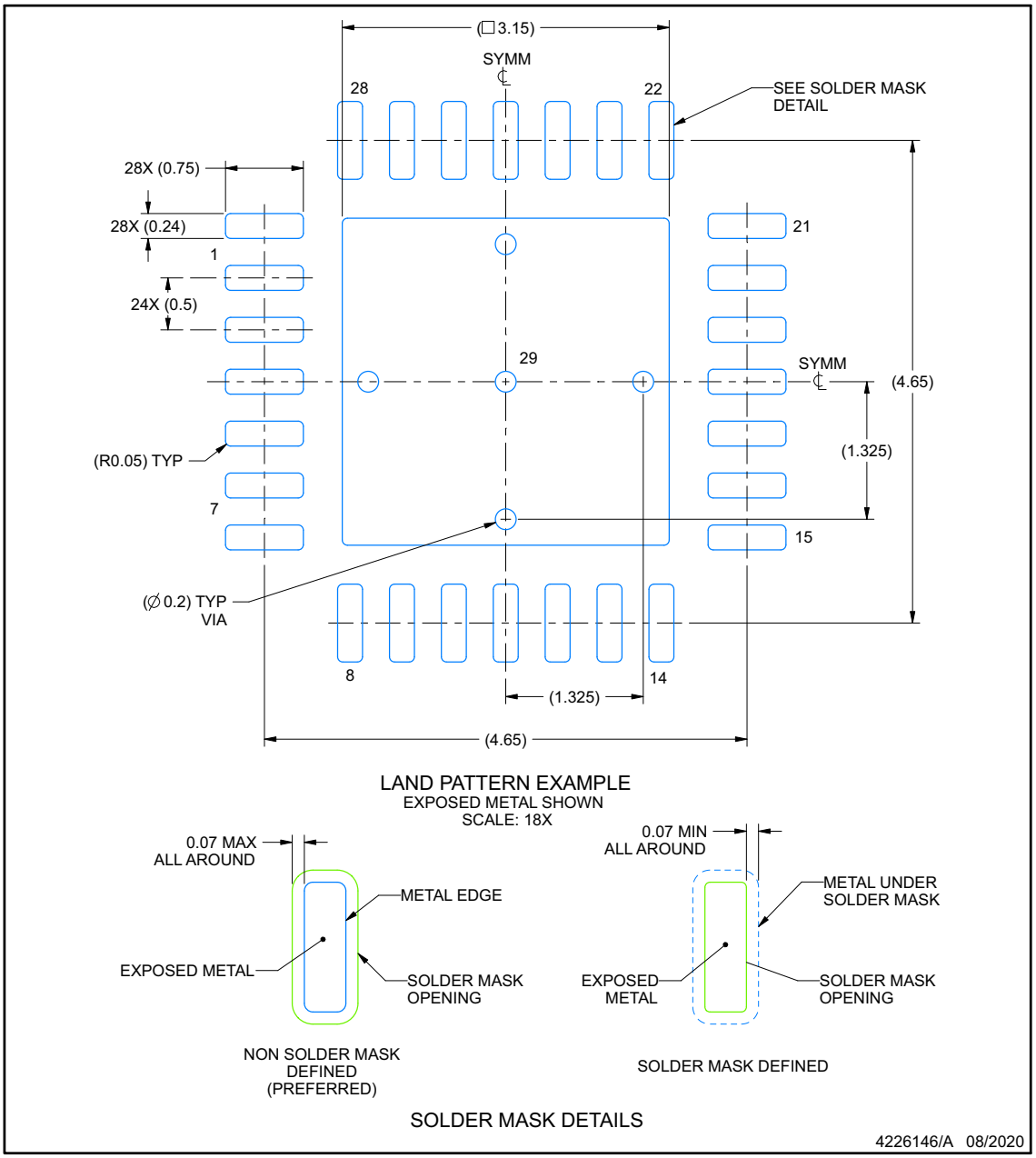
Copyright © 2024 Texas Instruments Incorporated

EXAMPLE BOARD LAYOUT

RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

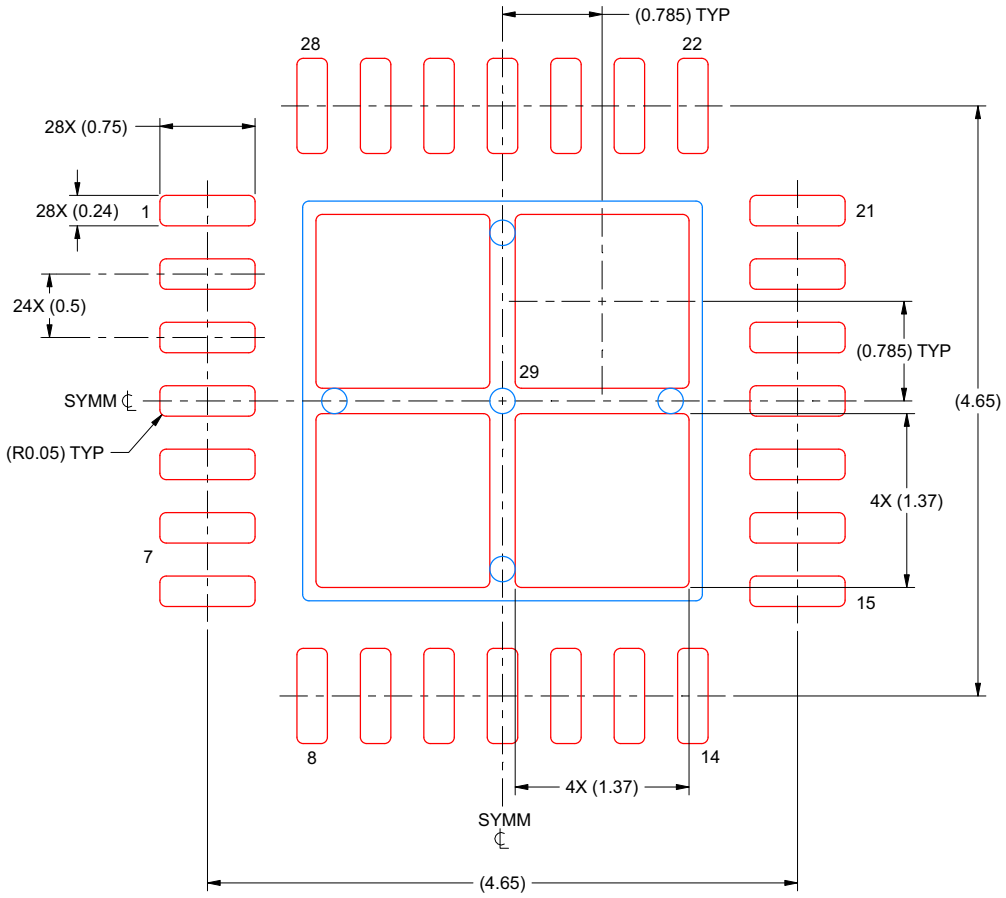
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

Copyright © 2024 Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

RHD0028B **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 29
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4226146/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

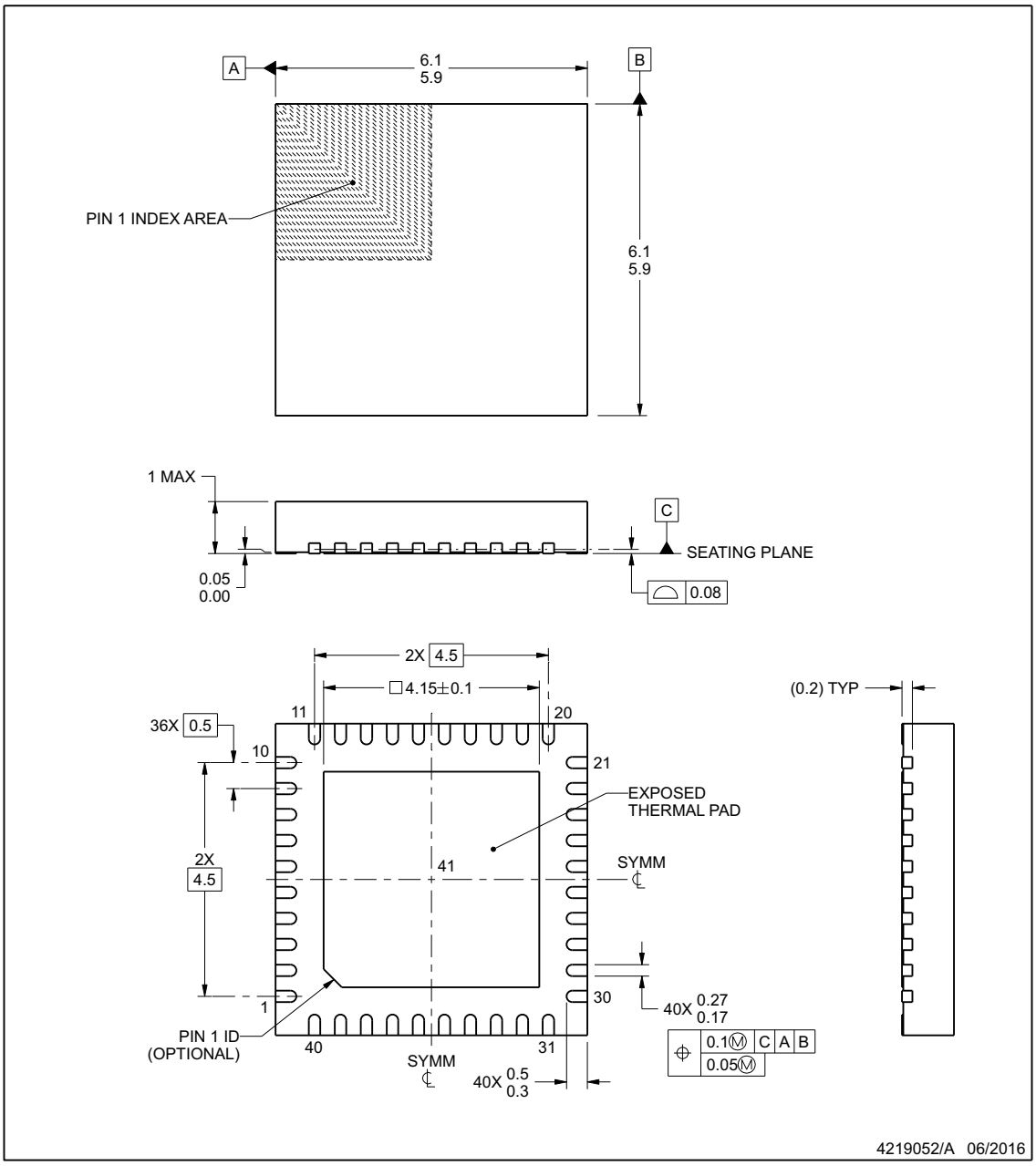
Copyright © 2024 Texas Instruments Incorporated

PACKAGE OUTLINE

RHA0040B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

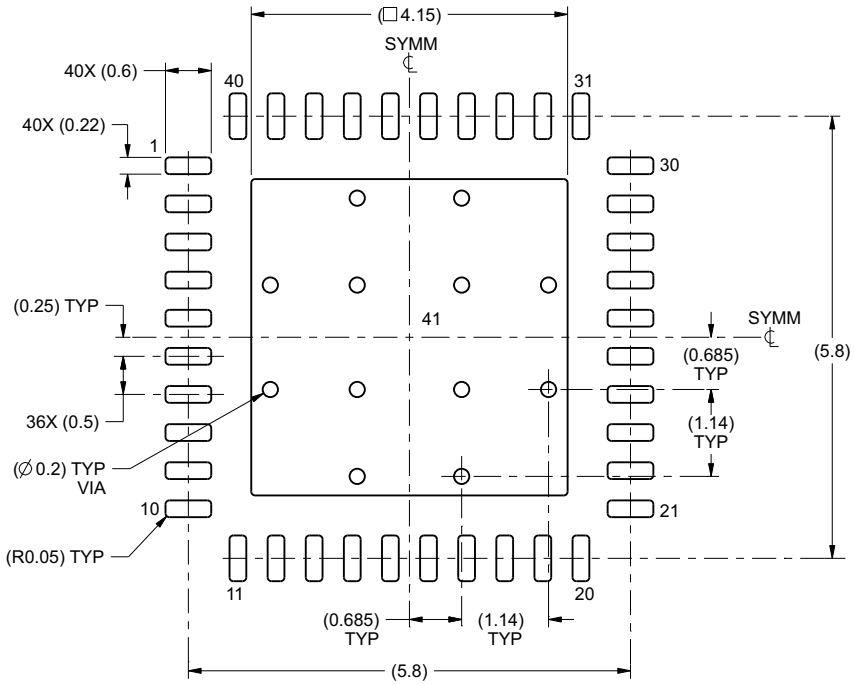
www.ti.com

Copyright © 2024 Texas Instruments Incorporated

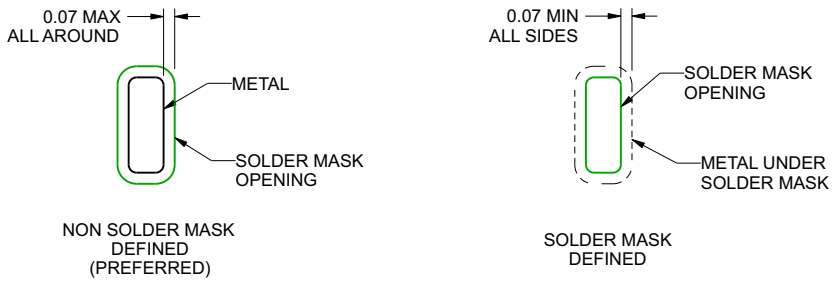
EXAMPLE BOARD LAYOUT

RHA0040B **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

4219052/A 06/2016

NOTES: (continued)

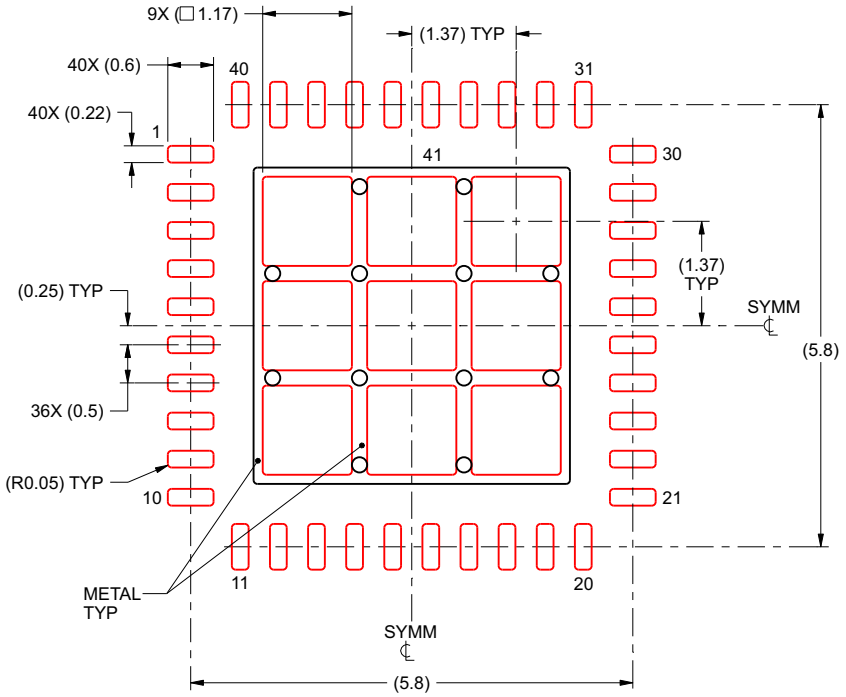
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

Copyright © 2024 Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

RHA0040B **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4219052/A 06/2016

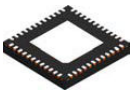
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Copyright © 2024 Texas Instruments Incorporated

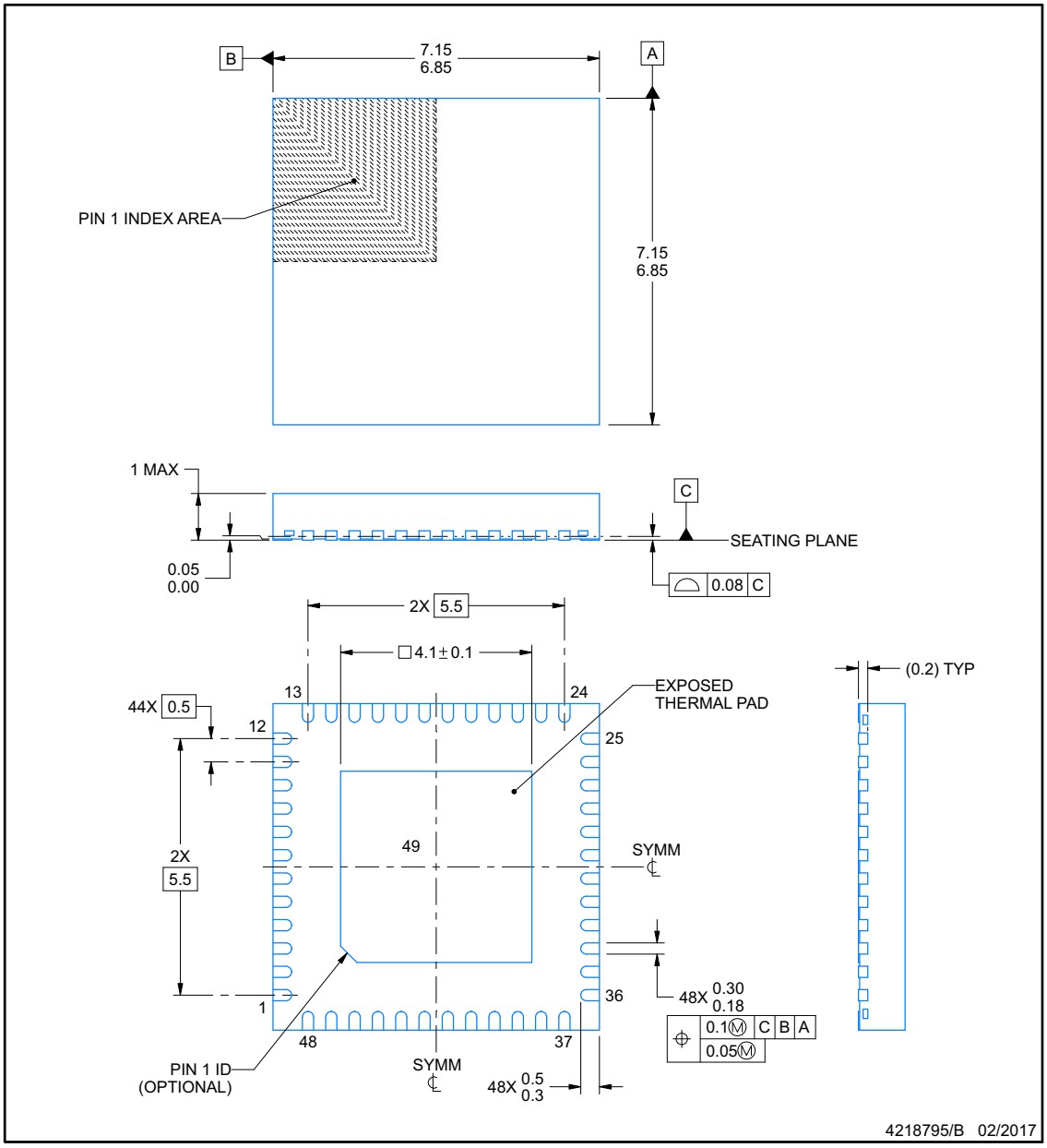
PACKAGE OUTLINE

RGZ0048B



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

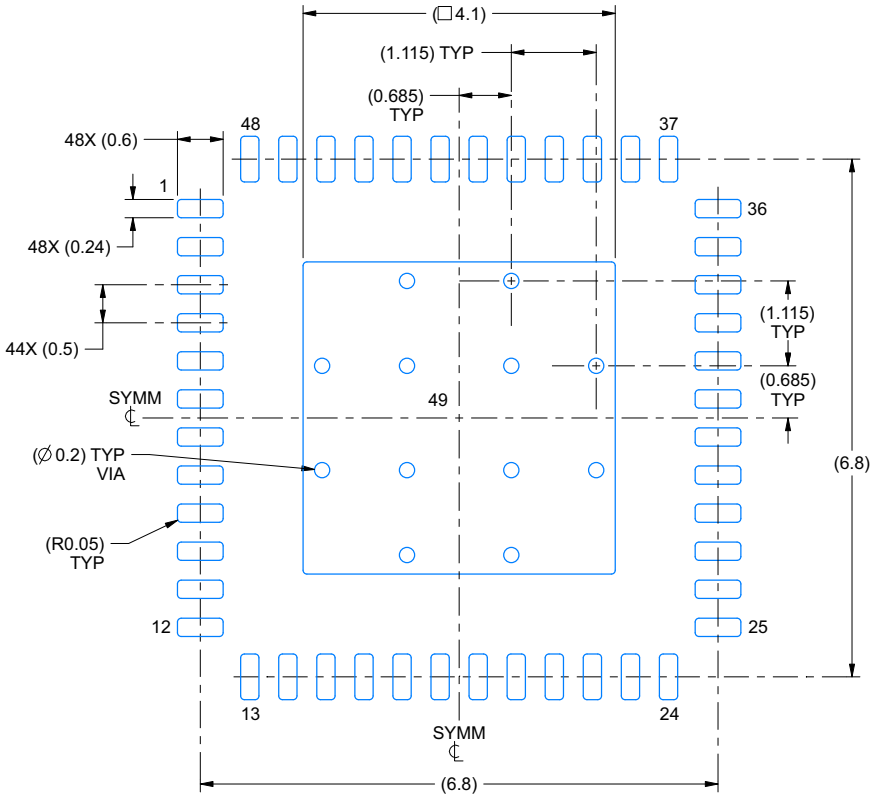
Copyright © 2024 Texas Instruments Incorporated

EXAMPLE BOARD LAYOUT

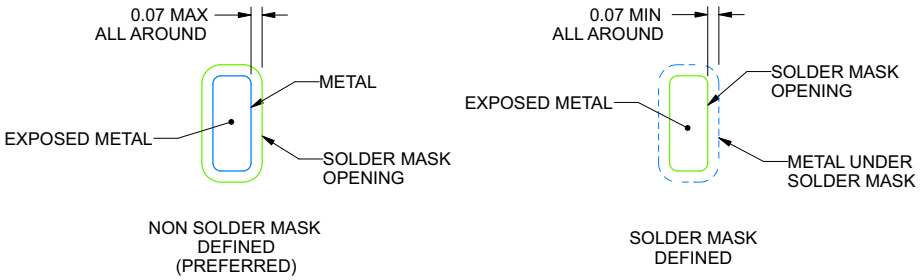
RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

4218795/B 02/2017

NOTES: (continued)

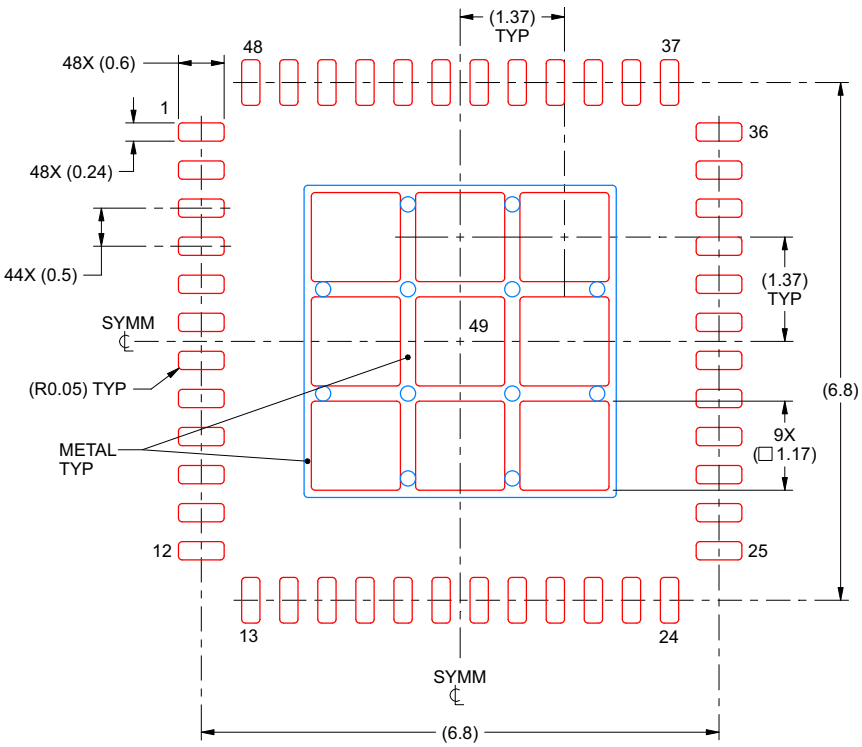
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

Copyright © 2024 Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

RGZ0048B **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

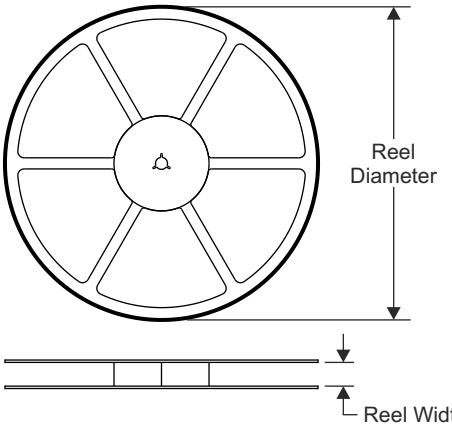
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

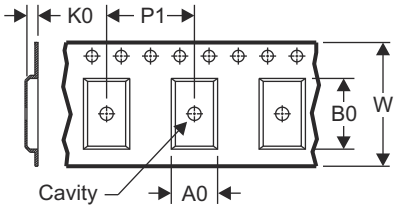
Copyright © 2024 Texas Instruments Incorporated

12.1 Tape and Reel Information

REEL DIMENSIONS

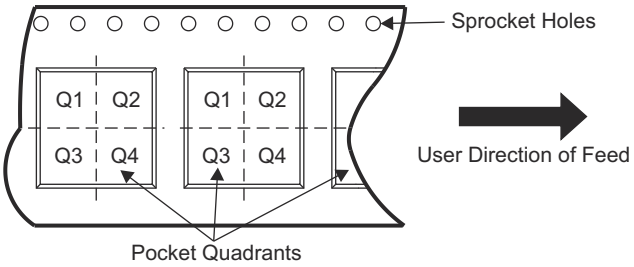


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

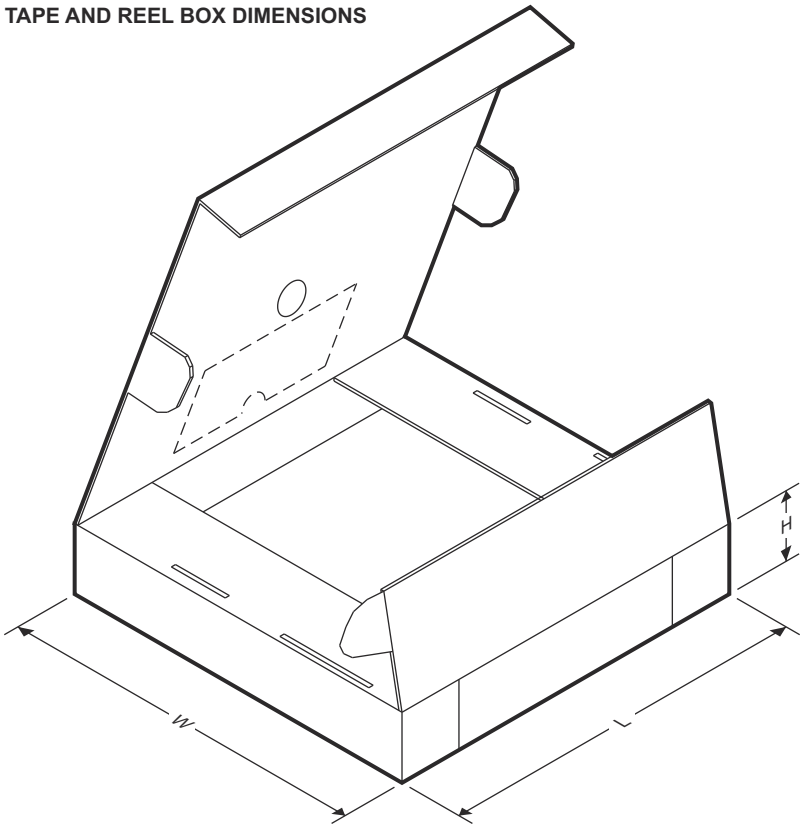
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK1D2102LRGTR	VQFN	RGT	16	3000	330	12.4	3.3	3.3	1.1	8	12	Q2
LMK1D2102LRGTT	VQFN	RGT	16	250	180	12.4	3.3	3.3	1.1	8	12	Q2
LMK1D2106LRHAR	VQFN	RHA	40	4000	330	16.4	6.3	6.3	1.1	12	16	Q2
LMK1D2106LRHAT	VQFN	RHA	40	250	330	16.4	6.3	6.3	1.1	12	16	Q2

Copyright © 2024 Texas Instruments Incorporated

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK1D2102LRGTR	VQFN	RGT	16	3000	367	367	35
LMK1D2102LRGTT	VQFN	RGT	16	250	210	185	35
LMK1D2106LRHAR	VQFN	RHA	40	4000	353	353	32
LMK1D2106LRHAT	VQFN	RHA	40	250	353	353	32

Copyright © 2024 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK1D2102LRGTR	Active	Production	VQFN (RGT) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L2102
LMK1D2102LRGTR.B	Active	Production	VQFN (RGT) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See LMK1D2102LRGTR	L2102
LMK1D2102LRGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L2102
LMK1D2102LRGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See LMK1D2102LRGTT	L2102
LMK1D2104LRHDR	Active	Production	VQFN (RHD) | 28	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L2104
LMK1D2104LRHDR.B	Active	Production	VQFN (RHD) | 28	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L2104
LMK1D2104LRHDT	Active	Production	VQFN (RHD) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L2104
LMK1D2104LRHDT.B	Active	Production	VQFN (RHD) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L2104
LMK1D2106LRHAR	Active	Production	VQFN (RHA) | 40	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L2106
LMK1D2106LRHAR.B	Active	Production	VQFN (RHA) | 40	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See LMK1D2106LRHAR	L2106
LMK1D2106LRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L2106
LMK1D2106LRHAT.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See LMK1D2106LRHAT	L2106

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated