TLK10002 10-Gbps, Dual-Channel, Multi-Rate Transceiver

1 Features

- Dual-Channel, 10-Gbps, Multi-Rate Transceiver
- Supports All CPRI and OBSAI Data Rates From 1 Gbps to 10 Gbps
- Integrated Latency Measurement Function, Accuracy up to 814 ps
- Supports SERDES Operation With up to 10-Gbps Data Rate on the High-Speed Side and up to 5G bps on the Low-Speed Side
- Differential CML I/Os on Both High-Speed and Low-Speed Sides
- Shared or Independent Reference Clock Per Channel
- Loopback Capability on Both High-Speed and Low-Speed Sides, OBSAI Compliant
- Supports Data Retime Operation
- Supports PRBS 2^7-1, 2^{23}-1 and 2^{31}-1 and High-Frequency, Low-Frequency, Mixed-Frequency, and CRPAT Long and Short Pattern Generation and Verification
- Two Power Supplies: 1-V Core, and 1.5-V or 1.8-V I/O
- Transmit De-Emphasis and Receive Adaptive Equalization to Allow Extended Backplane or Cable Reach on Both High-Speed and Low-Speed Sides
- Programmable Transmit Output Swing on Both High-Speed and Low-Speed Sides.
- Minimum Receiver Differential Input Threshold of 100 mV_{pp}
- Loss-of-Signal (LOS) Detection
- Interface to Backplanes, Passive and Active Copper Cables, or SFP/SFP+ Optical Modules
- Hot Plug Protection
- JTAG; IEEE 1149.1 Test Interface
- MDIO; IEEE 802.3 Clause-22 Support
- 65-nm Advanced CMOS Technology
- Industrial Ambient Operating Temperature (–40°C to 85°C) at Full Rate
- Power Consumption: 1.6 W Typical
- Device Package: 13-mm × 13-mm, 144-pin PBGA, 1-mm Ball-Pitch

2 Applications

- Wireless Infrastructure CPRI and OBSAI Links
- High-Speed Video Applications
- Proprietary Cable or Backplane Links
- High-Speed Point-to-Point Transmission Systems

3 Description

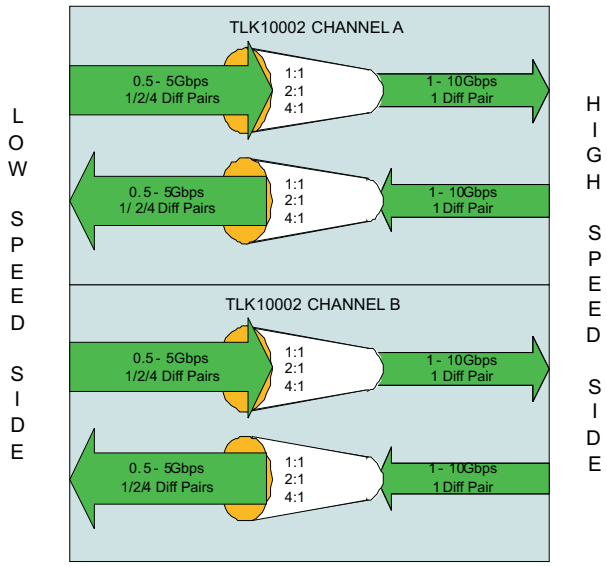
The TLK10002 device is a dual-channel, multi-rate transceiver intended for use in high-speed bidirectional point-to-point data transmission systems. It has special support for the wireless base station Remote Radio Head (RRH) application, but may also be used in other high-speed applications. It supports all the CPRI and OBSAI rates from 1.2288 Gbps to 9.8304 Gbps.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLK10002	FCBGA (144)	13.00 mm × 13.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2013) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

Changes from Original (May 2011) to Revision A	Page
• Changed Feature From: Supports all CPRI and OBSAI Data Rates To: Supports all CPRI and OBSAI Data Rates From 1Gbps to 10Gbps	1
• Changed Feature From: JTAG; IEEE 1149.1 /1149.6 Test Interface To: JTAG; IEEE 1149.1 Test Interface	1
• Changed J_{T1} and J_{D1} Parameters From: (CPRI LV/LV-II and OBSAI Rates) To: (CPRI LV/LV-II/ LV-III and OBSAI Rates)	15
• Changed JT2 and JD2 Parameters From: (CPRI E.6/12.HV) To: (CPRI E.12.HV)	15
• Deleted the R_{IN} - Differential input impedance, MIN = 80 Ω and MAX = 120 Ω values	16
• Changed *Functional Block Diagram* text, From: 8B/10B Decoder Lane Align Master To: 8B/10B Encoder Lane Align Master	20
• Changed text in the Lane Alignment Slave (LAS) section From: Resides in the TLK10002 LS transmitter To: Resides in the TLK10002 LS receiver	22
• Changed values in the text and in list item 1, From: 1.485Gbps To: 1.987Gbps and From: 2.97Gbps To: 3.974Gbps	27
• Changed list item 1 text From: "supported in the quarter rate mode (RateScale = 1)" To: "supported in the quarter rate mode (RateScale = 0.5)"	27
• Changed list item 4 text From: "clock frequencies can be selected: 148.5MHz, 185.625MHz, 247.5MHz, 297MHz, and 371.25MHz." To: "clock frequencies can be selected: 397.4MHz, 331.167MHz, 248.375MHz, 198.7MHz, 165.583MHz, 158.96MHz, and 132.467MHz."	27
• Changed Table 7	28
• Added list items for latency measurement	33

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- Changed LOOPBACK_TP_CONTROL, BIT B.0 From: 1 = Enable shallow remote loopback mode To: Enable shallow local loopback mode 55
- Changed LAS_CONFIG_CONTROL BIT C.2 ACCESS From: RW To: RW SC[(1)] 55
- Deleted list item from the HS/LS Data Rate Setting section: "Write 1'B1 to 9.9 HS_PEAK_DISABLE (HS_OVERLAY_CONTROL = 0x0B00)." 63
- Changed list item in the HS Serial Configuration Changed section From: 4.11:10 (HS_CDRFMULT[1:0]), 4.9:8 (HS_CDRTHR[1:0]) To: 4.11:10 (HS_CDRFMULT[1:0]), 4.9:8 (HS_CDRTHR[1:0]), 4.5 (H1CDRMODE) 64
- Changed the HS/LS Data Rate Setting section: From: Refer to Table 3 To: Refer to Table 2 66
- Changed the HS/LS Data Rate Setting section: list item text 66

5 Description (continued)

The TLK10002 performs 1:1, 2:1 and 4:1 serialization of the 8B/10B encoded data streams presented on its low-speed (LS) side data inputs. The serialized 8B/10B encoded data is presented on the high-speed (HS) side outputs. Likewise, the TLK10002 performs 1:1, 1:2 and 1:4 deserialization of 8B/10B encoded data streams presented on its high-speed side data inputs. The deserialized 8B/10B encoded data is presented on the low-speed side outputs. Depending on the serialization or deserialization ratio, the low-speed side data rate can range from 0.5 Gbps to 5 Gbps and the high-speed side data rate can range from 1 Gbps to 10 Gbps. Both low-speed and high-speed side data inputs and outputs are of differential current mode logic (CML) type with integrated termination resistors. In the 1:1 mode, the input can be raw (non-8B/10B encoded) data, allowing for transmission of PRBS data through the device.

The TLK10002 performs data serialization or deserialization and clock extraction as a physical layer interface device. Flexible clocking schemes are provided to support various operations. They include the support for clocking with an externally-jitter-cleaned clock recovered from the high-speed side.

The TLK10002 provides two low-speed side and two high-speed side loopback modes for self-test and system diagnostic purposes.

The TLK10002 has built-in pattern generation and verification to help in system tests. The low speed side supports generation and verification of PRBS 2^7-1, 2^{23}-1, and 2^{31}-1 patterns. In addition to those PRBS patterns, the high-speed side supports High, Low, Mixed, and CRPAT long and short pattern generation and verification.

The TLK10002 has an integrated loss-of-signal (LOS) detection function on both high-speed and low-speed sides. LOS is asserted in conditions where the input differential voltage swing is less than the LOS assert threshold. The input differential voltage swing must exceed the de-assert threshold for the LOS condition to be cleared.

Lane alignment for each channel is achieved through a proprietary lane alignment scheme implemented on the low-speed side interface. The interfaced upstream link partner device needs to implement the lane alignment scheme for the correct link operation. Normal link operation resumes only after lane alignment is achieved.

The two TLK10002 channels are fully independent. They can be operated with different reference clocks, at different data rates, and with different serialization or deserialization ratios.

The low-speed side of the TLK10002 is ideal for interfacing with an FPGA or ASIC located on the same local physical system. The high-speed side is ideal for interfacing with remote systems through an optical fiber, an electrical cable, or a backplane interface. The TLK10002 supports operation with SFP and SFP+ optical modules.

6 Pin Configuration and Functions

CTR Package
144-Pin FCBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	INA1P	VSS	INA0N	INA0P	VSS	OUTA0P	OUTA0N	PDTRXA_N	CLKOUTBP	CLKOUTBN	VSS	HSRXAN
B	INA1N	INA2P	VSS	VSS	OUTA1P	OUTA1N	VSS	TMS	PRBSEN	LS_OK_IN_A	VSS	HSRXAP
C	VSS	INA2N	VDDRA_LS	OUTA2P	OUTA2N	VSS	VDDO0	TDI	CLKOUTAP	CLKOUTAN	AMUXA	VSS
D	INA3P	VDDA_LS	VSS	AMUXB	VSS	TDO	VPP	TCK	LS_OK_OUT_A	VSS	VSS	HSTXAP
E	INA3N	VSS	OUTA3N	VSS	TRST_N	VDDD	DVDD	VDDD	LOSA	PRTAD0	VDDRA_HS	HSTXAN
F	VSS	VDDA_LS	OUTA3P	VDDT_LS	VSS	VDDD	DVDD	VSS	VDDT_HS	VSS	VDDA_HS	VSS
G	VSS	VDDA_LS	VSS	VDDT_LS	VSS	DVDD	VSS	DVDD	PRTAD1	VDDA_HS	VSS	HSRXBN
H	INB0P	VSS	OUTB0N	VSS	RESET_N	VDDD	DVDD	VDDD	LS_OK_OUT_B	REFCLKB_SEL	VSS	HSRXBP
J	INB0N	VDDA_LS	OUTB0P	PDTRXB_N	VSS	PRTAD3	MDIO	MDC	PRBS_PASS	GPI0	VDDRB_HS	VSS
K	VSS	INB1P	VDDRB_LS	OUTB1N	OUTB1P	VSS	VDDO1	LOSB	REFCLK1P	REFCLK1N	VSS	HSTXBP
L	INB2P	INB1N	VSS	VSS	OUTB2N	OUTB2P	VSS	LS_OK_IN_B	PRTAD2	TESTEN	VSS	HSTXBN
M	INB2N	VSS	INB3P	INB3N	VSS	OUTB3N	OUTB3P	PRTAD4	REFCLKA_SEL	REFCLK0P	REFCLK0N	VSS

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Pin Functions

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	NO.		
CHANNEL A			
HSTXAP HSTXAN	D12 E12	Output CML VDDA_HS	**Serial Transmit Channel A Output.** HSTXAP and HSTXAN comprise the high speed side transmit direction Channel A differential serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC-coupled.
HSRXAP HSRXAN	B12 A12	Input CML VDDA_HS	**Serial Receive Channel A Input.** HSRXAP and HSRXAN comprise the high speed side receive direction Channel A differential serial input signal. These CML input signals must be AC-coupled.
INA[3:0]P/N	D1/E1 B2/C2 A1/B1 A4/A3	Input CML VDDA_LS	**Parallel Channel A Inputs.** INAP and INAN comprise the low speed side transmit direction Channel A differential input signals. Only INA[0] is used in the 1:1 mode, and only INA[1:0] are used in the 2:1 mode. These signals must be AC-coupled.
OUTA[3:0]P/N	F3/E3 C4/C5 B5/B6 A6/A7	Output CML VDDA_LS	**Parallel Channel A Outputs.** OUTAP and OUTAN comprise the low speed side receive direction Channel A differential output signals. During device reset (RESET_N asserted low) these pins are driven differential zero. Only OUTA[0] is used in the 1:1 mode, and only OUTA[1:0] are used in the 2:1 mode. These signals must be AC-coupled.
LOSA	E9	Output LVCMOS 1.5V/1.8V VDDO0 40Ω Driver	**Channel A Receive Loss Of Signal (LOS) Indicator.** LOSA=0: Signal detected. LOSA=1: Loss of signal. Loss of signal detection is based on the input signal level. When HSRXAP/N has a differential input signal swing of <75 mVpp, LOSA will be asserted (if enabled). Once asserted, the input signal has to be > 150 mVpp for this LOS to be deasserted. Other functions can be observed on LOSA in real-time, configured through MDIO. During device reset (RESET_N asserted low) this pin is driven low. During pin-based power down (PDTRXA_N asserted low), this pin is floating. During register-based power down (1.15 asserted high), this pin is floating. NOTE: TI highly recommends that LOSA be brought to an easily accessible point on the application board (header), in the event that debug is required.
REFCLKA_SEL	M9	Input LVCMOS 1.5V/1.8V VDDO0	**Reference Clock Select Channel A.** This input, when low, selects REFCLK0P/N as the clock reference to Channel A SERDES. When high, REFCLK1P/N is selected as the clock reference to Channel A SERDES. If software control is desired (register bit 1.1), this input signal should be tied low. See Figure 13 for more detail. Default reference clock for Channel A is REFCLK0P/N.
CLKOUTAP/N	C9/C10	Output CML DVDD	**Channel A High Speed Side Output Clock.** By default, this output is enabled and outputs the high speed side Channel A recovered byte clock (high speed line rate divided by 20). Optionally it can be configured to output the VCO clock divided by 2. Additional MDIO-selectable divide ratios of 1, 2, 4, 5, 8, 10, 16, 20, and 25 are available. See Figure 13. This CML output must be AC-coupled. During device reset (RESET_N asserted low) these pins are driven differential zero. During pin-based power down (PDTRXA_N and PDTRXB_N asserted low), these pins are floating. During register-based power down (1.15 asserted high both channels), these pins are floating. Channel A high speed side recovered byte clock can also be directed to CLKOUTBP/N pins through the MDIO interface.
LS_OK_IN_A	B10	Input LVCMOS 1.5V/1.8V VDDO0	**Channel A Receive Lane Alignment Status Indicator.** Lane alignment status signal received from a Lane Alignment Slave on the link partner device. LS_OK_IN_A=0: Channel A Link Partner Receive lanes not aligned. LS_OK_IN_A=1: Channel A Link Partner Receive lanes aligned
LS_OK_OUT_A	D9	Output LVCMOS 1.5V/1.8V VDDO0 40Ω Driver	**Channel A Transmit Lane Alignment Status Indicator.** Lane alignment status signal sent to a Lane Alignment Master on the link partner device. LS_OK_OUT_A=0: Channel A Transmit lanes not aligned. LS_OK_OUT_A=1: Channel A Transmit lanes aligned.

Pin Functions (continued)

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	NO.		
PDTRXA_N	A8	Input LVCMOS 1.5V/1.8V VDDO0	**Transceiver Power Down.** When this pin is held low (asserted), Channel A is placed in power down mode. When deasserted, Channel A operates normally. After deassertion, a software data path reset must be issued through the MDIO interface.
CHANNEL B			
HSTXBP HSTXBN	K12 L12	Output CML VDDA_HS	**Serial Transmit Channel B Output.** HSTXBP and HSTXBN comprise the high speed side transmit direction Channel B differential serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC-coupled.
HSRXBP HSRXBN	H12 G12	Input CML VDDA_HS	**Serial Receive Channel B Input.** HSRXBP and HSRXBN comprise the high-speed side receive direction Channel B differential serial input signal. These CML input signals must be AC-coupled.
INB[3:0]P/N	M3/M4 L1/M1 K2/L2 H1/J1	Input CML VDDA_LS	**Parallel Channel B Inputs.** INBP and INBN comprise the low speed side transmit direction Channel B differential input signals. Only INB[0] is used in the 1:1 mode, and only INB[1:0] are used in the 2:1 mode. These signals must be AC-coupled.
OUTB[3:0]P/N	M7/M6 L6/L5 K5/K4 J3/H3	Output CML VDDA_LS	**Parallel Channel B Outputs.** OUTBP and OUTBN comprise the low-speed side receive direction Channel B differential output signals. During device reset (RESET_N asserted low) these pins are driven differential zero. Only OUTB[0] is used in the 1:1 mode, and only OUTB[1:0] are used in the 2:1 mode. These signals must be AC-coupled.
LOSB	K8	Output LVCMOS 1.5V/1.8V VDDO1 40Ω Driver	**Channel B Receive Loss Of Signal (LOS) Indicator.** LOSB=0: Signal detected. LOSB=1: Loss of signal. Loss of signal detection is based on the input signal level. When HSRXBP/N has a differential input signal swing of <75 mVpp, LOSB will be asserted (if enabled). Once asserted, the input signal has to be > 150 mVpp for this LOS to be deasserted Other functions can be observed on LOSB in real-time, configured through MDIO. During device reset (RESET_N asserted low) this pin is driven low. During pin-based power down (PDTRXB_N asserted low), this pin is floating. During register-based power down (1.15 asserted high), this pin is floating. TI highly recommends that LOSB be brought to an easily accessible point on the application board (header), in the event that debug is required.
REFCLKB_SEL	H10	Input LVCMOS 1.5V/1.8V VDDO1	Reference Clock Select Channel B. This input, when low, selects REFCLK0P/N as the clock reference to Channel B SERDES. When high, REFCLK1P/N is selected as the clock reference to Channel B SERDES. If software control is desired (register bit 1.1), this input signal should be tied low. See Figure 13 for more detail. Default reference clock for Channel B is REFCLK0P/N.
CLKOUTBP/N	A9/A10	Output CML DVDD	**Channel B High Speed Side Output Clock.** By default, this output is enabled and outputs the high-speed side Channel B recovered byte clock (high speed line rate divided by 20). Optionally it can be configured to output the VCO clock divided by 2. Additional MDIO-selectable divide ratios of 1, 2, 4, 5, 8, 10, 16, 20, and 25 are available. See Figure 13. This CML output must be AC-coupled. During device reset (RESET_N asserted low) these pins are driven differential zero. During pin-based power down (PDTRXA_N and PDTRXB_N asserted low), these pins are floating. During register-based power down (1.15 asserted high both channels), these pins are floating. Channel B high-speed side recovered byte clock can also be directed to CLKOUTAP/N pins through the MDIO interface.
LS_OK_IN_B	L8	Input LVCMOS 1.5V/1.8V VDDO1	**Channel B Receive Lane Alignment Status Indicator.** Lane alignment status signal received from a Lane Alignment Slave on the link partner device. LS_OK_IN_B=0: Channel B Link Partner Receive lanes not aligned. LS_OK_IN_B=1: Channel B Link Partner Receive lanes aligned
LS_OK_OUT_B	H9	Output LVCMOS 1.5V/1.8V VDDO1 40Ω Driver	**Channel B Transmit Lane Alignment Status Indicator.** Lane alignment status signal sent to a Lane Alignment Master on the link partner device. LS_OK_OUT_B=0: Channel B Transmit lanes not aligned. LS_OK_OUT_B=1: Channel B Transmit lanes aligned.

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Pin Functions (continued)

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	NO.		
PDTRXB_N	J4	Input LVCMOS 1.5V/1.8V VDDO1	**Transceiver Power Down.** When this pin is held low (asserted), Channel B is placed in power-down mode. When deasserted, Channel B operates normally. After deassertion, a software data path reset must be issued through the MDIO interface.
REFERENCE CLOCKS AND CONTROL AND MONITORING SIGNALS			
REFCLK0P/N	M10/M11	Input LVDS/ LVPECL DVDD	**Reference Clock Input Zero.** This differential input is a clock signal used as a reference to one or both channels. The reference clock selection is done through MDIO or REFCLKA_SEL and REFCLKB_SEL pins. This input signal **must** be AC-coupled. If unused, REFCLK0P/N must be pulled down to GND through a shared 100-Ω resistor.
REFCLK1P/N	K9/K10	Input LVDS/ LVPECL DVDD	**Reference Clock Input One.** This differential input is a clock signal used as a reference to one or both channels. The reference clock selection is done through MDIO. This input signal **must** be AC-coupled. If unused, REFCLK1P/N must be pulled down to GND through a shared 100-Ω resistor.
PRBSEN	B9	Input LVCMOS 1.5V/1.8V VDDO0	**Enable PRBS:** When this pin is asserted high, the internal PRBS generator and verifier circuits are enabled on both transmit and receive data paths on high-speed and low-speed sides of both channels. This signal is logically OR'd with MDIO register bits B.7:6, and B.13:12. PRBS 2^{31}-1 is selected by default, and can be changed through MDIO.
PRBS_PASS	J9	Output LVCMOS 1.5V/1.8V VDDO1 40Ω Driver	**Receive PRBS Error Free (Pass) Indicator.** When PRBS test is enabled (PRBSEN=1): PRBS_PASS=1 indicates that PRBS pattern reception is error free. PRBS_PASS=0 indicates that a PRBS error is detected. The channel, high-speed or low-speed side, and lane (for low-speed side) that this signal refers to is chosen through MDIO register bits 0.3:0. During device reset (RESET_N asserted low) this pin is driven low. During pin-based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is floating. During register-based power down, this pin is floating. TI highly recommends that PRBS_PASS be brought to easily accessible point on the application board (header), in the event that debug is required.
PRTAD[4:0]	M8 J6 L9 G9 E10	Input LVCMOS 1.5V/1.8V VDDO[1:0]	**MDIO Port Address.** Used to select the MDIO port address. PRTAD[4:1] selects the MDIO port address. The TLK10002 has two different MDIO port addresses. Selecting a unique PRTAD[4:1] per TLK10002 device allows 16 TLK10002 devices per MDIO bus. Each channel can be accessed by setting the appropriate port address field within the serial interface protocol transaction. The TLK10002 will respond if the 4 MSB's of the port address field on MDIO protocol (PA[4:1]) matches PRTAD[4:1]. The LSB of port address field (PA[0]) determines which TLK10002 channel responds. Channel A responds when PA[0]=0 and Channel B responds when PA[0]=1. PRTAD[0] is not used functionally, but is present for device testability and compatibility with other devices in the family of products. PRTAD[0] must be grounded on the application board.
RESET_N	H5	Input LVCMOS 1.5V/1.8V VDDO1	**Low True Device Reset.** RESET_N must be held asserted (low logic level) for at least 10 µs after device power stabilization.
MDC	J8	Input LVCMOS with Hysteresis 1.5V/1.8V VDDO1	**MDIO Clock Input.** Clock input for the Clause 22 MDIO interface. Note that an external pullup is generally not required on MDC.

Pin Functions (continued)

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	NO.		
MDIO	J7	Input/Output LVCMOS 1.5V/1.8V VDDO1 25Ω Driver	**MDIO Data I/O.** MDIO interface data input/output signal for the Clause 22 MDIO interface. **This signal must be externally pulled up to VDDO, using a 2-kΩ resistor.** During device reset (RESET_N asserted low) this pin is floating. During register-based power down the management interface remains active for control register writes and reads. Certain status bits are not deterministic as their generating clock source may be disabled as a result of asserting either power down input signal. During pin-based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is floating. During register-based power down (1.15 asserted high both channels), this pin is driven normally.
TDI	C8	Input LVCMOS 1.5V/1.8V VDDO0 (Internal Pullup)	**JTAG Input Data.** TDI is used to serially shift test data and test instructions into the device during the operation of the test port. In system applications where JTAG is not implemented, this input signal may be left floating. During pin based power down (PDTRXA_N **and** PDTRXB_N asserted low), this pin is not pulled up. During register based power down (1.15 asserted high both channels), this pin is pulled up.
TDO	D6	Output LVCMOS 1.5V/1.8V VDDO0 50Ω Driver	JTAG Output Data. TDO is used to serially shift test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high impedance state. During device reset (RESET_N asserted low) this pin is floating. During pin-based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is floating. During register-based power down (1.15 asserted high both channels), this pin is floating.
TMS	B8	Input LVCMOS 1.5V/1.8V VDDO0 (Internal Pullup)	**JTAG Mode Select.** TMS is used to control the state of the internal test-port controller. In system applications where JTAG is not implemented, this input signal can be left unconnected. During pin based power down (PDTRXA_N **and** PDTRXB_N asserted low), this pin is not pulled up. During register-based power down (1.15 asserted high both channels), this pin is pulled up.
TCK	D8	Input LVCMOS with Hysteresis 1.5V/1.8V VDDO0	**JTAG Clock.** TCK is used to clock state information and test data into and out of the device during boundary scan operation. In system applications where JTAG is not implemented, this input signal must be grounded.
TRST_N	E5	Input LVCMOS 1.5V/1.8V VDDO0 (Internal Pulldown)	**JTAG Test Reset.** TRST_N is used to reset the JTAG logic into system operational mode. This input can be left unconnected in the application and is pulled down internally, disabling the JTAG circuitry. If JTAG is implemented on the application board, this signal must be deasserted (high) during JTAG system testing, and otherwise asserted (low) during normal operation mode. During pin-based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is not pulled down. During register-based power down (1.15 asserted high both channels), this pin is pulled down.
TESTEN	L10	Input LVCMOS 1.5V/1.8V VDDO1	**Test Enable.** This signal is used during the device manufacturing process. It must be grounded through a resistor in the device application board. The application board must allow the flexibility of easily reworking this signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO).
GPI0	J10	Input LVCMOS 1.5V/1.8V VDDO1	**General Purpose Input Zero.** This signal is used during the device manufacturing process. It must be grounded through a resistor on the device application board. The application board must also allow the flexibility of easily reworking this signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO).
AMUXA	C11	Analog I/O	**SERDES Channel A Analog Testability I/O.** This signal is used during the device manufacturing process. It must be left unconnected in the device application.
AMUXB	D4	Analog I/O	**SERDES Channel B Analog Testability I/O.** This signal is used during the device manufacturing process. It must be left unconnected in the device application.

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Pin Functions – Power Pins[(1)]

PIN		Type	DESCRIPTION
SIGNAL	BGA		
VDDA_LS/HS	D2, F2, G2, J2 / F11, G10	Power	**SERDES Analog Power.** VDDA_LS and VDDA_HS provide supply voltage for the analog circuits on the low-speed and high-speed sides respectively. 1 V nominal. Can be tied together on the application board.
VDDT_LS/HS	F4, G4 / F9	Power	**SERDES Analog Power.** VDDT_LS and VDDT_HS provide termination and supply voltage for the analog circuits on the low-speed and high-speed sides respectively. 1 V nominal. Can be tied together on the application board.
VDDD	E6, E8, F6, H6, H8	Power	**SERDES Digital Power.** VDDD provides supply voltage for the digital circuits internal to the SERDES. 1 V nominal.
DVDD	E7, F7, G6, G8, H7	Power	**Digital Core Power.** DVDD provides supply voltage to the digital core. 1 V nominal.
VDDRA_LS/HS	C3/E11	Power	**SERDES Analog Regulator Power.** VDDRA_LS and VDDRA_HS provide supply voltage for the internal PLL regulator for Channel A low-speed and high-speed sides respectively. 1.5 V or 1.8 V nominal.
VDDRB_LS/HS	K3/J11	Power	**SERDES Analog Regulator Power**. VDDRB_LS and VDDRB_HS provide supply voltage for the internal PLL regulator for Channel B low-speed and high-speed sides respectively. 1.5 V or 1.8 V nominal.
VDDO[1:0]	K7/C7	Power	**LVCMOS I/O Power.** VDDO0 and VDDO1 provide supply voltage for the LVCMOS inputs and outputs. 1.5 V or 1.8 V nominal. Can be tied together on the application board.
VPP	D7	Power	**Factory Program Voltage.** Used during device manufacturing. The application must connect this power supply directly to DVDD.
VSS	A2, A5, A11, B3, B4, B7, B11, C1, C6, C12, D3, D5, D10, D11, E2, E4, F1, F5, F8, F10, F12, G1, G3, G5, G7, G11, H2, H4, H11, J5, J12, K1, K6, K11, L3, L4, L7, L11, M2, M5, M12	Ground	**Ground.** Common analog and digital ground.

(1) External AC-coupling is not needed if already included in the SFP+ module

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	DVDD, VDDA_LS/HS, VDDT_LS/HS, VPP, VDDD	–0.3	1.4	V
Supply voltage	VDDRA_LS/HS, VDDRB_LS/HS, VDDO[1:0]	–0.3	2.2	V
Input voltage	V_I, (LVCMOS/LVDS/LVPECL/CML/Analog)	–0.3	Supply + 0.3	V
Characterized free-air operating temperature		–40	85	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

					MIN	NOM	MAX	UNIT
	Digital / Analog supply voltages	VDDD, VDDA_LS/HS, DVDD, VDDT_LS/HS, VPP			0.95	1.00	1.05	V
	SERDES PLL regulator voltage	VDDRA_LS/HS VDDRB_LS/HS		1.5 V nominal	1.425	1.5	1.575	V
				1.8 V nominal	1.71	1.8	1.89	V
	LVCMOS I/O supply voltage	VDDO[1:0]		1.5 V nominal	1.425	1.5	1.575	V
				1.8 V nominal	1.71	1.8	1.89	V
I_{DD}	Supply current	VDDD		10 Gbps			375	mA
		VDDA_LS/HS					460	
		DVDD + VPP					220	
		VDDT_LS/HS					540	
		VDDRA_LS					50	
		VDDRA_HS					20	
		VDDRB_LS					50	
		VDDRB_HS					20	
		VDDO[1:0] (1.5-V /1.8-V Mode)	1.5-V mode				6	
			1.8-V mode				8	
P_D	All supplies worst case						1.75[1]	W
I_{SD}	Shutdown current	VDDD		PD* Asserted			80	mA
		VDDA					25	
		DVDD + VPP					15	
		VDDT					45	
		VDDRA_HS/LS + VDDRB_HS/LS	1.5-V mode				0.5	
			1.8-V mode				0.5	
		VDDO	1.5-V mode				5	
			1.8-V mode				5	

(1) Total worst case power is not a sum of the individual power supply worst case as the individual power is taken from multiple modes. These modes are mutually exclusive and therefore used only for power supply requirements.

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7.4 Thermal Information

THERMAL METRIC[1]			TLK10002 CTR (FCBGA) 144 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance		24.5	°C/W
		EVM Board (5in. x 7in., 14 layer, 1-oz. copper)	24.5	
		JEDEC High-K PCB	25.5	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		2.8	°C/W
		EVM Board (5in. x 7in., 14 layer, 1-oz. copper)		
		JEDEC High-K PCB		
$R_{\theta JB}$	Junction-to-board thermal resistance		15.2	°C/W
		EVM Board (5in. x 7in., 14 layer, 1-oz. copper)	12	
		JEDEC High-K PCB	18	
ψ_{JT}	Junction-to-top characterization parameter		0.9	°C/W
		EVM Board (5in. x 7in., 14 layer, 1-oz. copper)	0.9	
		JEDEC High-K PCB	1.8	
ψ_{JB}	Junction-to-board characterization parameter		14.0	°C/W
		EVM Board (5in. x 7in., 14 layer, 1-oz. copper)	11	
		JEDEC High-K PCB	13.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 10-Gbps Power Characteristics – 1.0 V

at V_{max}, 1.0 V Core, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply voltage	VDDA_LS/HS, VDDT_LS/HS, VDDD, DVDD, VPP	2 Ch Mode, 4:1 at 10 Gpbs	0.95	1	1.05	V
		2 Ch Mode, 2:1 at 10 Gpbs				
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs				
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs				
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs				
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs				
Power supply current	VDDA_LS/HS	2 Ch Mode, 4:1 at 10 Gpbs			0.407	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.411	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0.222	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0.22	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0.229	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0.228	
	VDDT_LS/HS	2 Ch Mode, 4:1 at 10 Gpbs			0.489	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.347	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0.268	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0.197	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0.273	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0.199	
	DVDD+VPP	2 Ch Mode, 4:1 at 10 Gpbs			0.1743	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.1887	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0.1375	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0.1407	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0.1356	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0.1414	
	VDDD	2 Ch Mode, 4:1 at 10 Gpbs			0.3151	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.333	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0.21	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0.2136	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0.209	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0.2165	

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7.6 10-Gbps Power Characteristics – 1.5 V

at V_{max}, 1.5 V I/O, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply voltage	VDDRA_LS/HS, VDDRB_LS/HS, VDDO	2 Ch Mode, 4:1 at 10 Gpbs	1.425	1.5	1.575	V
		2 Ch Mode, 2:1 at 10 Gpbs				
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs				
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs				
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs				
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs				
Power supply current	VDDRA_LS	2 Ch Mode, 4:1 at 10 Gpbs			0.0191	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.0371	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0.019	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0.0371	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0	
	VDDRA_HS	2 Ch Mode, 4:1 at 10 Gpbs			0.0152	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.0152	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0.0153	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0.0153	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0	
	VDDRB_LS	2 Ch Mode, 4:1 at 10 Gpbs			0.0192	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.0374	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0.0192	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0.0374	
	VDDRB_HS	2 Ch Mode, 4:1 at 10 Gpbs			0.0155	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.0155	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0.0156	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0.0156	
	VDDO[1:0]	2 Ch Mode, 4:1 at 10 Gpbs			0.0037	A
		2 Ch Mode, 2:1 at 10 Gpbs				
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs				
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs				
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs				
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs				

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7.7 10-Gbps Power Characteristics – 1.8 V

at V_{max}, 1.8 V I/O, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply voltage	VDDRA_LS/HS, VDDRB_LS/HS, VDDO	2 Ch Mode, 4:1 at 10 Gpbs	1.71	1.8	1.89	V
		2 Ch Mode, 2:1 at 10 Gpbs				
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs				
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs				
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs				
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs				
Power supply current	VDDRA_LS	2 Ch Mode, 4:1 at 10 Gpbs			0.0191	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.0372	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0.0191	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0.0372	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0	
	VDDRA_HS	2 Ch Mode, 4:1 at 10 Gpbs			0.0151	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.0151	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0.0151	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0.0151	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0	
	VDDRB_LS	2 Ch Mode, 4:1 at 10 Gpbs			0.0194	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.0376	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0.0193	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0.0376	
	VDDRB_HS	2 Ch Mode, 4:1 at 10 Gpbs			0.0154	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.0154	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0.0155	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0.0155	
	VDDO[1:0]	2 Ch Mode, 4:1 at 10 Gpbs			0.0047	A
		2 Ch Mode, 2:1 at 10 Gpbs			0.0047	
		1 Ch Mode, Ch A on, Ch B off, 4:1 at 10 Gpbs			0.0046	
		1 Ch Mode, Ch A on, Ch B off, 2:1 at 10 Gpbs			0.0047	
		1 Ch Mode, Ch A off, Ch B on, 4:1 at 10 Gpbs			0.0046	
		1 Ch Mode, Ch A off, Ch B on, 2:1 at 10 Gpbs			0.0047	

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7.8 Transmitter and Receiver Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-SPEED SIDE SERIAL TRANSMITTER						
$V_{OD(pp)}$	TX Output differential peak-to-peak voltage swing	SWING (3.15:12) = 0000	50	130	220	mV_{pp}
		SWING (3.15:12) = 0001	110	220	320	
		SWING (3.15:12) = 0010	180	300	430	
		SWING (3.15:12) = 0011	250	390	540	
		SWING (3.15:12) = 0100	320	480	650	
		SWING (3.15:12) = 0101	390	570	770	
		SWING (3.15:12) = 0110	460	660	880	
		SWING (3.15:12) = 0111	530	750	1000	
		SWING (3.15:12) = 1000	590	830	1100	
		SWING (3.15:12) = 1001	660	930	1220	
		SWING (3.15:12) = 1010	740	1020	1320	
		SWING (3.15:12) = 1011	820	1110	1430	
		SWING (3.15:12) = 1100	890	1180	1520	
		SWING (3.15:12) = 1101	970	1270	1610	
		SWING (3.15:12) = 1110	1060	1340	1680	
		SWING (3.15:12) = 1111	1090	1400	1740	
V_{CMT}	TX Output common-mode voltage	100-Ω differential termination, DC-coupled		V_{DDT}- (0.25*$V_{OD(pp)}$)		mV
t_{skew}	Intra-pair output skew	SWING(3.15:12) = 0110			0.09	UI
t_r, t_f	Differential output signal rise, Fall time (20% to 80%) Differential load = 100Ω		20			ps
J_{T1}	Serial output total jitter (CPRI LV/LV-II/LV-III and OBSAI Rates)	Serial Rate ≤ 3.072 Gbps (Not Applicable to LV-II/LV-III)			0.35	UI
		Serial Rate > 3.072 Gbps (And All LV-II/LV-III Rates)			0.30	
J_{D1}	Serial output deterministic jitter (CPRI LV/LV-II/ LV-III and OBSAI Rates)	Serial Rate ≤ 3.072 Gbps (Not Applicable to LV-II/LV-III)			0.17	UI
		Serial Rate > 3.072 Gbps (And All LV-II/LV-III Rates)			0.15	
J_{T2}	Serial output total jitter (CPRI E.12.HV)	CPRI E.12.HV (0.6144 and 1.2288 Gbps)			0.279	UI
J_{D2}	Serial output deterministic jitter (CPRI E.12.HV)				0.14	
S_{cc22}	Common-mode output return loss	100MHz < f < 1.0 GHz			7	dB
		1.0GHz < f < 5.0 GHz			5	
$T_{(LATENCY)}$	Transmit path latency	See Figure 19				UI
HIGH-SPEED SIDER SERIAL RECEIVER						
V_{ID}	RX Input differential voltage |RXP – RXN|	Full Rate AC-Coupled	50		600	mV
		Half/Quarter/Eighth Rate AC-Coupled	50		800	
$V_{ID(pp)}$	RX Input differential peak-to-peak voltage swing 2 * |RXP – RXN|	Full Rate AC-Coupled	100		1200	mV_{pp}
		Half/Quarter/Eighth Rate AC-Coupled	100		1600	
C_I	RX Input capacitance				2	pF
J_{TOL}	Jitter tolerance, total jitter at serial input (DJ + RJ) (BER 10^{-15})	Zero crossing Half/Quarter/Eighth Rate			0.66	UI_{pp}
		Zero crossing Full Rate	0.65			
J_{DR}	Serial input deterministic jitter (BER 10^{-15})	Zero crossing Half/Quarter/Eighth Rate			0.50	UI_{pp}
		Zero crossing Full Rate	0.35			
SDD11	Differential input return loss	100 MHz < f < 0.75*[Serial Bit Rate]		8		dB
		0.75 × [Serial Bit Rate] < f < [Serial Bit Rate]		See (1)		
t_{skew}	Intra-pair input skew				0.23	UI
$t_{(LATENCY)}$	Receive path latency	See Figure 19				UI

(1) Differential input return loss, SDD11 = 8 – 16.6 log10(f / (0.75 × [Serial Bit Rate])) dB

Transmitter and Receiver Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW-SPEED SIDE SERIAL TRANSMITTER CHARACTERISTICS						
$V_{OD(pp)}$	Transmitter output differential peak-to-peak voltage swing	SWING (7:14:12) = 000	110	190	280	mV_{pp}
		SWING (7:14:12) = 001	280	380	490	
		SWING (7:14:12) = 010	420	560	700	
		SWING (7:14:12) = 011	560	710	870	
		SWING (7:14:12) = 100	690	850	1020	
		SWING (7:14:12) = 101	760	950	1150	
		SWING (7:14:12) = 110	800	1010	1230	
		SWING (7:14:12)= 111	830	1050	1270	
V_{CMT}	Transmitter output common mode voltage	100-Ω differential termination, DC-coupled		V_{DDT} - (0.5*$V_{OD(pp)}$)		mV
t_{skew}	Intra-pair output skew				0.045	UI
t_R, t_F	Differential output signal rise, fall time (20% to 80%) Differential Load = 100Ω		30	-	-	ps
J_T	Serial output total jitter				0.35	UI
J_D	Serial output deterministic jitter				0.17	UI
LOW-SPEED SIDE SERIAL RECEIVER CHARACTERISTICS						
V_{ID}	Receiver input differential voltage| INP – INN|	Full Rate AC-Coupled	50		600	mV
		Half/Quarter Rate AC-Coupled	50		800	
$V_{ID(pp)}$	Receiver input differential peak-to-peak voltage swing 2 × |INP – INN|	Full Rate AC-Coupled	100		1200	mV_{dfpp}
		Half/Quarter Rate AC-Coupled	100		1600	
C_I	Receiver input capacitance				2	pF
J_{TOL}	Jitter tolerance, total jitter at serial input (DJ + RJ)(BER 10^{-15})	Zero crossing Half/Quarter Rate			0.66	UI_{pp}
		Zero crossing Full Rate			0.65	
J_{DR}	Serial input deterministic jitter(BER 10^{-15})	Zero crossing Half/Quarter Rate			0.50	UI_{pp}
		Zero crossing Full Rate			0.35	
S_{dd11}	Differential input return loss	625 MHz < f < 2.5 GHz			8	dB
t_{skew}	Intra-pair input skew				0.23	UI
$t_{lane-skew}$	Lane-to-lane input skew				30	UI
REFERENCE CLOCK CHARACTERISTICS (REFCLK0P/N, REFCLK1P/N)						
F	Frequency		122.88		425	MHz
FHS_{offset}	Accuracy	Relative to Nominal HS Serial Data Rate	–100		100	ppm
		Relative to Incoming HS Serial Data Rate	–200		200	
FLS_{offset}	Accuracy to LS serial data	Synchronous (Multiple/Divide)	0	0	0	ppm
DC	Duty cycle	High Time	45%	50%	55%	
V_{ID}	Differential input voltage		250		2000	mVpp
C_{IN}	Input capacitance				1	pF
R_{IN}	Differential input impedance			100		Ω
T_{RISE}	Rise/fall time	10% to 90%	50		350	ps
J_R	Random jitter	12 kHz to 20 MHz			4	ps-RMS
DIFFERENTIAL OUTPUT CLOCK CHARACTERISTICS (CLKOUTAP/N, CLKOUTBP/N)						
V_{OD}	Differential Output Voltage	Peak to peak	1000		2000	mV_{pp}
T_{RISE}	Output Rise Time	10% to 90%, 2pF lumped capacitive load, AC-Coupled			350	ps
R_{TERM}	Output Termination	CLKOUTA/BP/N to DVDD	40	50	60	Ω
F	Output Frequency		0		500	MHz
LVCMOS ELECTRICAL CHARACTERISTICS (VDDO)						
V_{OH}	High-level output voltage	I_{OH} = 2 mA, Driver Enabled (1.8 V)	VDDO – 0.45		VDDO	V
		I_{OH} = 2 mA, Driver Enabled (1.5 V)	0.75 × VDDO		VDDO	

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Transmitter and Receiver Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = –2 mA, Driver Enabled (1.8 V)	0		0.45	V
		I_{OL} = –2 mA, Driver Enabled (1.5 V)	0		0.25 × VDDO	
V_{IH}	High-level input voltage		0.65 × VDDO		VDDO + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.35 × VDDO	V
I_{IH}, I_{IL}	Low/high input current	Receiver only			±170	µA
I_{OZ}	High-impedance output current	Driver disabled			±25	µA
		Driver disabled with pullup or pulldown enabled			±195	
C_{IN}	Input capacitance				3	pF

7.9 MDIO Timing Requirements

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{period}	MDC period	See Figure 4	100			ns
t_{setup}	MDIO setup to ↑ MDC	See Figure 4	10			ns
t_{hold}	MDIO hold to ↑ MDC	See Figure 4	10			ns
t_{valid}	MDIO valid from MDC ↑		0		40	ns

7.10 JTAG Timing Requirements

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PERIOD}	TCK period	See Figure 5	66.67			ns
t_{SETUP}	TDI/TMS/TRST_N setup to ↑ TCK	See Figure 5	3			ns
t_{HOLD}	TDI/TMS/TRST_N hold from ↑ TCK	See Figure 5	5			ns
t_{VALID}	TDO delay from TCK falling	See Figure 5	0		10	ns

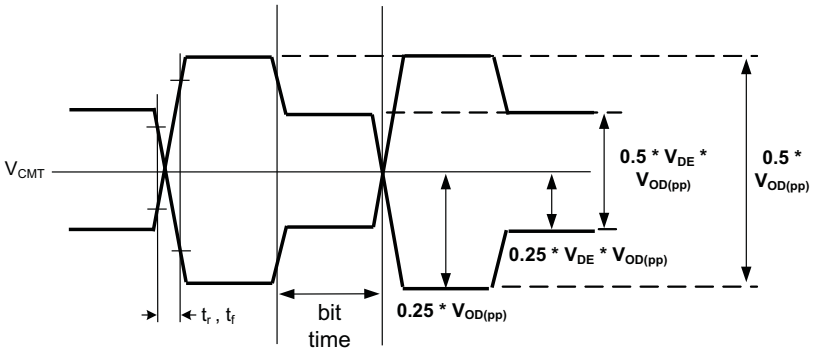
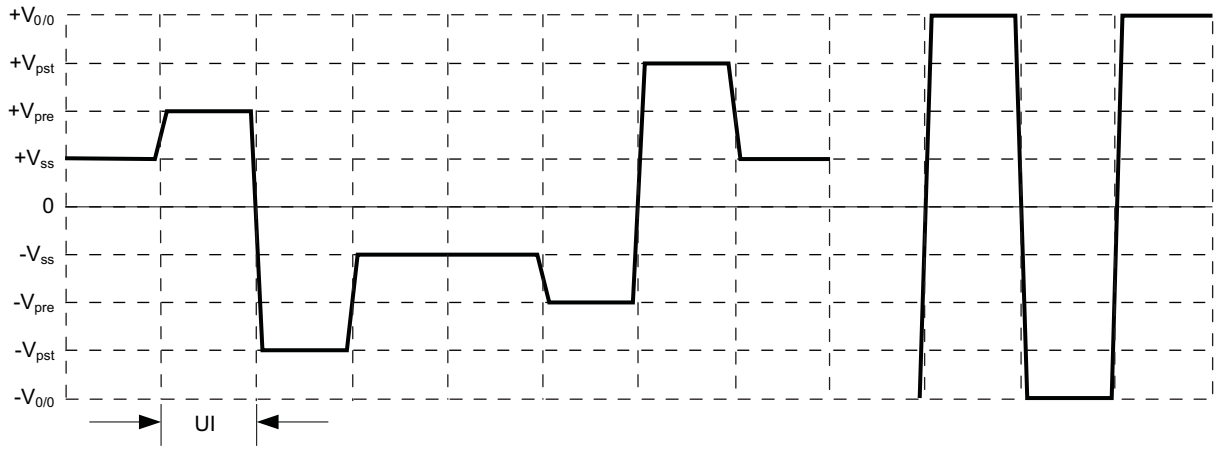


Figure 1. Transmit Output Waveform Parameter Definitions



h_{-1} = TWPRE (0% → -17.5% for typical application) setting

h_1 = TWPOST1 (0% → -37.5% for typical application) setting

$h_0 = 1 - |h_1| - |h_{-1}|$

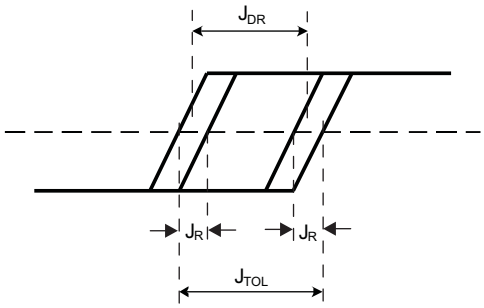
$V_{0/0}$ = Output Amplitude with TWPRE = 0%, TWPOST = 0%.

V_{ss} = Steady State Output Voltage = $V_{0/0} * | h_1 + h_0 + h_{-1}|$

V_{pre} = PreCursor Output Voltage = $V_{0/0} * | -h_1 – h_0 + h_{-1}|$

V_{pst} = PostCursor Output Voltage = $V_{0/0} * | -h_1 + h_0 + h_{-1}|$

Figure 2. Pre/Post Cursor Swing Definitions



NOTE: $J_{TOL} = J_R + J_{DR}$, where J_{TOL} is the receive jitter tolerance, J_{DR} is the received deterministic jitter, and J_R is the Gaussian random edge jitter distribution at a maximum BER = 10^{-12} for CPRI link and BER = 10^{-15} for OBSAI (RP3) link.

Figure 3. Input Jitter Definition

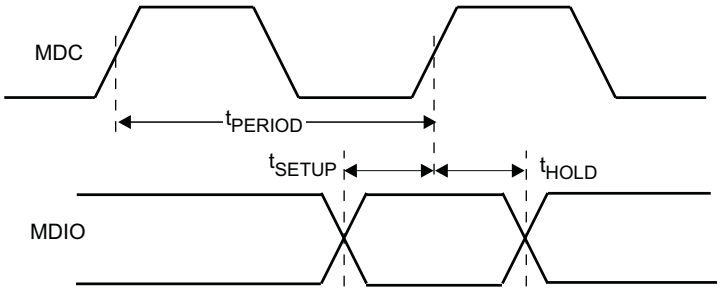


Figure 4. MDIO Read/Write Timing

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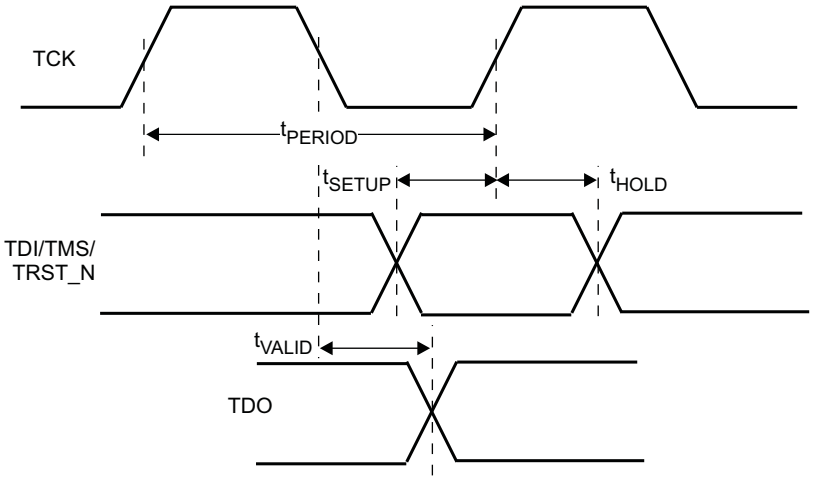
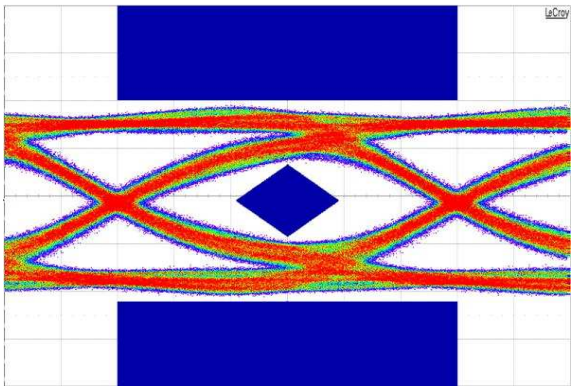


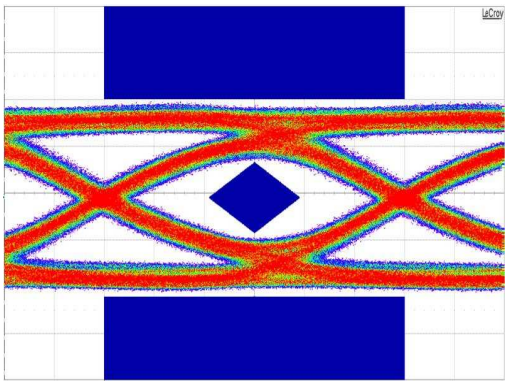
Figure 5. JTAG Timing

7.11 Typical Characteristics



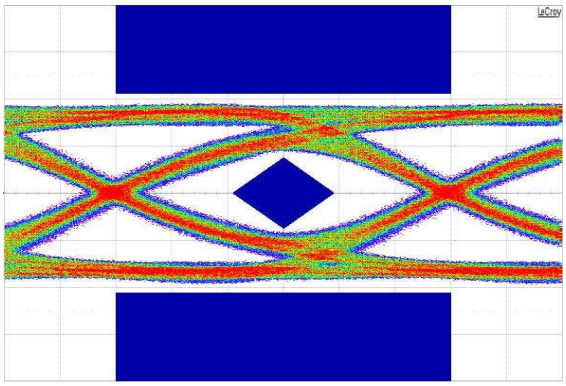
Total Jitter = .298 UI, PRBS 27-1, 4:1 Mode, RefClk=122.88MHz, Swing = 1260 mVpp, PRE = -5, POST1 = -10, POST2 = -7.5, AC-coupled

Figure 6. Transmitter Output (4-Inch FR-4 Trace)



Total Jitter = .339 UI, PRBS 27-1, 4:1 Mode, RefClk=122.88MHz, Swing = 1260 mVpp, PRE = -2.5, POST1 = -17.5, POST2 = 0, AC-coupled

Figure 7. Transmitter Output (8-Inch FR-4 Trace)



Total Jitter = .339 UI, PRBS 27-1, 4:1 Mode, RefClk=122.88MHz, Swing = 1260 mVpp, PRE = -2.5, POST1 = -17.5, POST2 = 0, AC-coupled

Figure 8. Transmitter Output (12-Inch FR-4 Trace)

8 Detailed Description

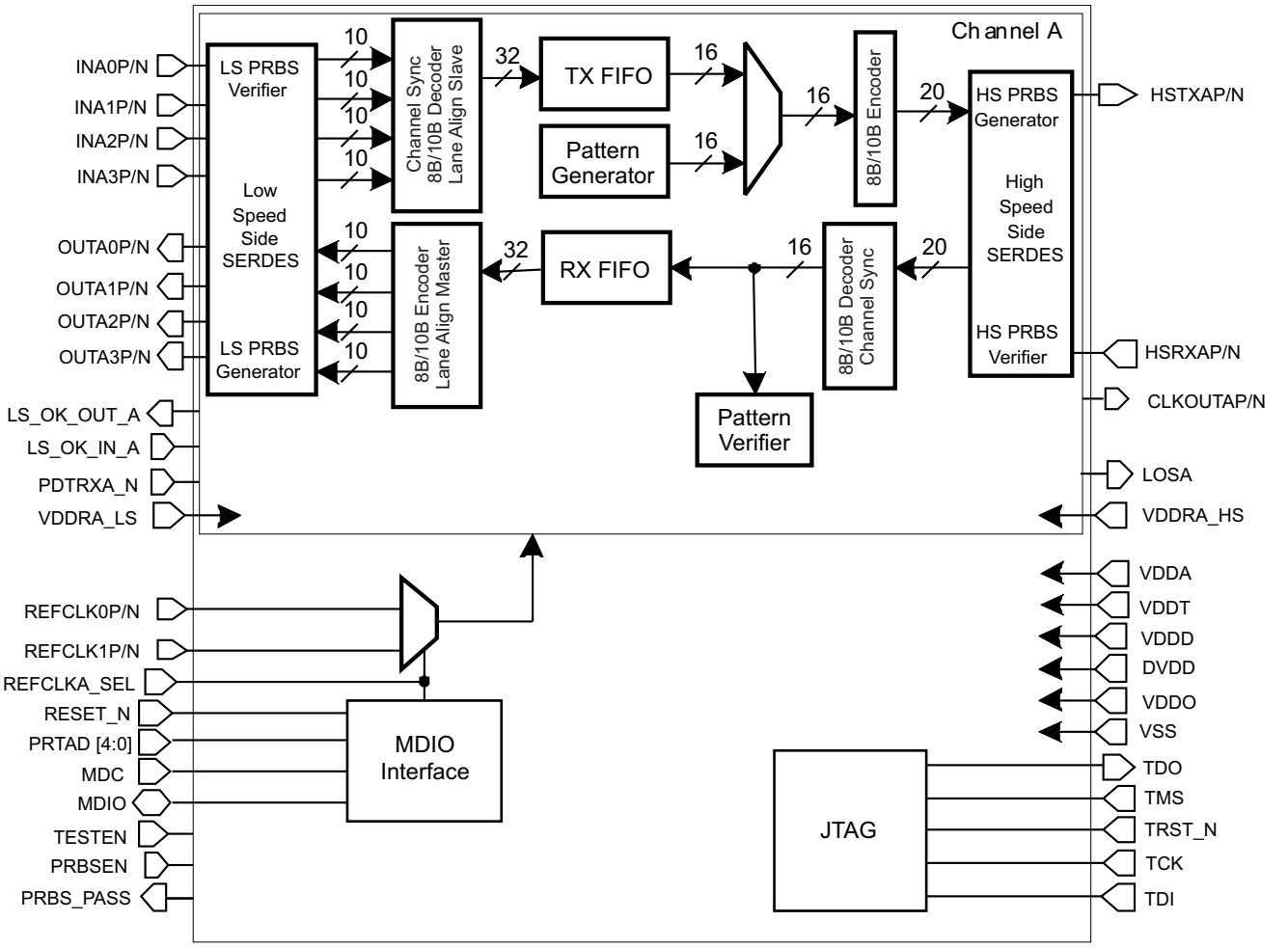
8.1 Overview

The TLK10002 is a versatile high-speed transceiver device that is designed to perform various physical layer functions. It is equipped with a number of functions and testability features that make it easy to integrate the device in high-speed communications systems, especially in wireless infrastructure. The details of those features are discussed in *Feature Description*.

A simplified block diagram of the TLK10002 device is shown in the *Functional Block Diagram* section for Channel A which is identical to Channel B. This low-power transceiver consists of two serializer/deserializer (SERDES) blocks, one on the low speed side and the other on the high speed side. The core logic block that lies between the two SERDES blocks carries out all the logic functions including channel synchronization, lane alignment, 8B/10B encoding/decoding, as well as test pattern generation and verification.

The TLK10002 provides a management data input/output (MDIO) interface as well as a JTAG interface for device configuration, control, and monitoring. Detailed description of the TLK10002 pin functions is provided in *Pin Configuration and Functions*.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 High-Speed Side Receiver Jitter Tolerance

The peak-to-peak total jitter tolerance for the RP3 receiver is 0.65 UI. This total jitter is composed of three components; deterministic jitter, random jitter, and an additional sinusoidal jitter.

The deterministic jitter tolerance is 0.37 UI minimum. The sum of deterministic and random jitter is 0.55 UI minimum. The additional sinusoidal jitter which the receiver must tolerate will have frequencies and amplitudes conforming to the mask presented in the Figure 9 and Table 1.

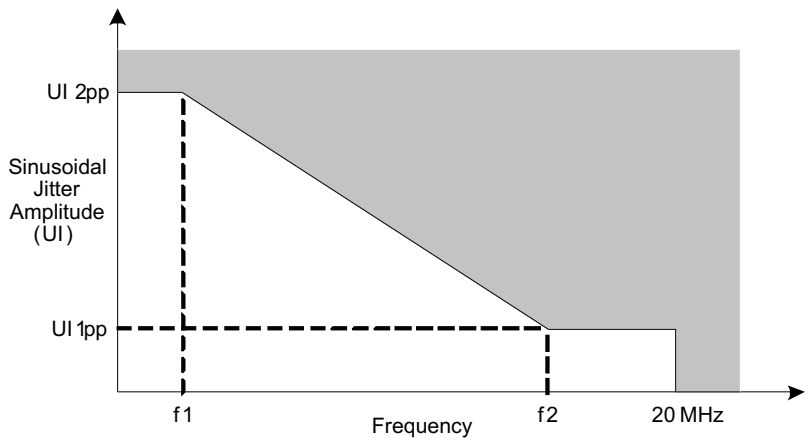

Figure 9. OBSAI Sinusoidal Jitter Mask

Table 1. Sinusoidal Jitter Mask Values

Frequency (MBaud)	f1 (kHz)	f2 (kHz)	UI 1pp	UI 2pp
768	5.4	460.8	0.1	8.5
1536	10.9	921.6	0.1	8.5
3072	21.8	1843.2	0.1	8.5
6144	36.9	3686	0.05	5
9830.4	59	5897.6	0.05	5

8.3.2 Lane Alignment Scheme

Lower rate multi-lane serial signals per channel must be byte aligned and lane aligned such that high-speed multiplexing (proper reconstruction of higher rate signal) is possible. For that reason, the TLK10002 implements a special lane alignment scheme on the low-speed (LS) side.

During lane alignment, a proprietary pattern (or a custom comma compliant data stream) is sent by the LS transmitter to the LS receiver on each active lane. This pattern allows the LS receiver to both delineate byte boundaries within a lower speed lane and align bytes across the lanes (2 or 4) such that the original higher rate data ordering is restored.

Lane alignment completes successfully when the LS receiver asserts a *Link Status OK* signal monitored by the LS transmitter on the link partner device such as an FPGA. The TLK10002 sends out the *Link Status OK* signals through the LS_OK_OUT_A/B output pins, and monitors the *Link Status OK* signals from the link partner device through the LS_OK_IN_A/B input pins. If the link partner device does not need the TLK10002 Lane Align Master (LAM) to send proprietary lane alignment pattern, LS_OK_IN_A/B can be tied high on the application board.

The lane alignment scheme is activated under any of the following conditions:

- Device/System power up (after configuration/provisioning)
- Loss of channel synchronization assertion on any enabled LS lane
- Loss of signal assertion on any enabled LS lane
- LS SERDES PLL Lock indication deassertion

- After device configuration change
- After software determined LS 8B/10B decoder error rate threshold exceeded
- After device reset is deasserted
- Anytime the LS receiver deasserts *Link Status OK*.
- Presence of reoccurring higher level / protocol framing errors

The block diagram of the lane alignment scheme is shown in Figure 10.

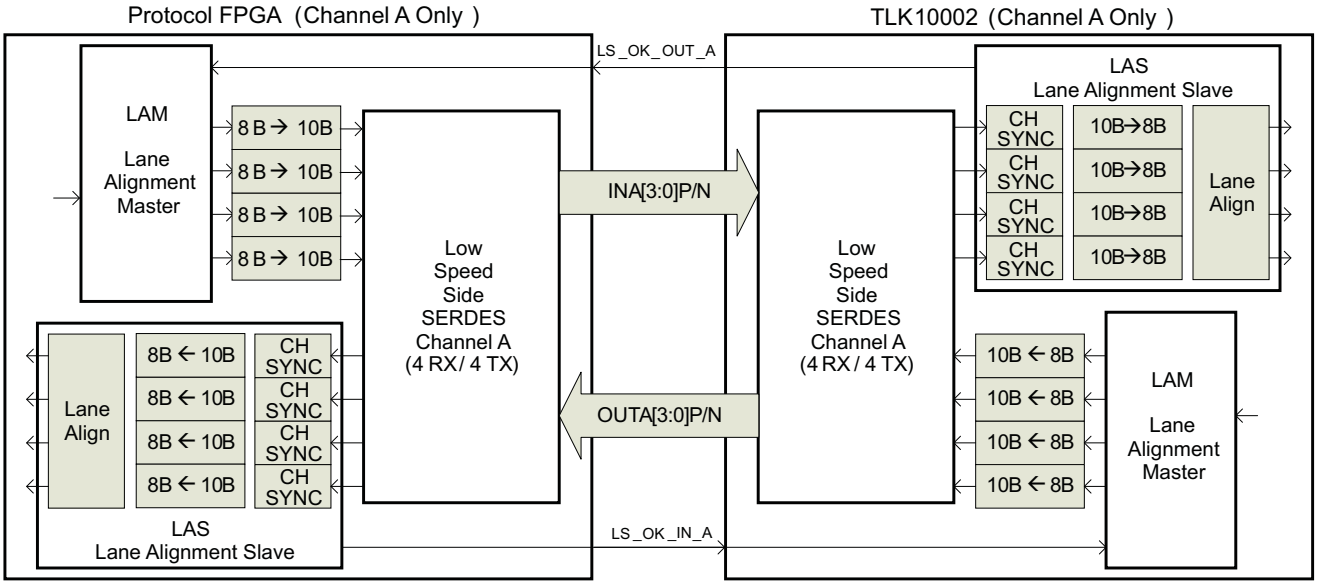

Figure 10. Block Diagram of the Lane Alignment Scheme

8.3.3 Lane Alignment Components

- Lane Alignment Master (LAM)
  - Responsible for generating proprietary LS lane alignment initialization pattern
  - Resides in the TLK10002 LS receiver (one instance in Channel A, one instance in Channel B)
    - Responsible for bringing up LS receive link for the data sent from the TLK10002 to a link partner device
    - Monitors the LS_OK_IN_A/B pins for *Link Status OK* signals sent from the Lane Alignment Slave (LAS) of the link partner device
  - Resides in the link partner device (one instance in Channel A, one instance in Channel B)
    - Responsible for bringing up LS transmit link for the data sent from the link partner device to the TLK10002
    - Monitors the *Link Status OK* signals sent from the LS_OK_OUT_A/B pins of the Lane Alignment Slave (LAS) of the TLK10002
- Lane Alignment Slave (LAS)
  - Responsible for monitoring the LS lane alignment initialization pattern
  - Performs channel synchronization per lane (2 or 4 lanes) through byte rotation
  - Performs lane alignment and realignment of bytes across lanes
  - Resides in the TLK10002 LS receiver (one instance in Channel A, one instance in Channel B)
    - Generates the *Link Status OK* signal for the LAM on the link partner device
  - Resides in the link partner device (one instance in Channel A, one instance in Channel B)
    - Generates the *Link Status OK* signal for the LAM on the TLK10002 device.

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8.3.4 Lane Alignment Operation

During lane alignment, the LS transmitter (LAM) sends a repeating pattern of 49 characters (control + data) simultaneously across all enabled LS lanes. These simultaneous streams are then encoded by 8B/10B encoders in parallel. The proprietary lane alignment pattern consists of the following characters:

/K28.5/ (CTL=1, Data=0xBC)

Repeat the following sequence of 12 characters four times:

/D30.5/ (CTL=0, Data=0xBE)
/D23.6/ (CTL=0, Data=0xD7)
/D3.1/ (CTL=0, Data=0x23)
/D7.2/ (CTL=0, Data=0x47)
/D11.3/ (CTL=0, Data=0x6B)
/D15.4/ (CTL=0, Data=0x8F)
/D19.5/ (CTL=0, Data=0xB3)
/D20.0/ (CTL=0, Data=0x14)
/D30.2/ (CTL=0, Data=0x5E)
/D27.7/ (CTL=0, Data=0xFB)
/D21.1/ (CTL=0, Data=0x35)
/D25.2/ (CTL=0, Data=0x59)

The above 49-character sequence is repeated until LS_OK_IN_A/B is asserted. Once LS_OK_IN_A/B is asserted, the LAM resumes transmitting traffic received from the high speed side SERDES immediately.

The TLK10002 performs lane alignment across the lanes similar in fashion to the IEEE 802.3ae-2002 (XAUI) specification. XAUI only operates across 4 lanes while LAS operates with 2 or 4 lanes. The lane alignment state machine is shown in Figure 11. The comma (K28.5) character is used for lane to lane alignment instead of XAUI's /A/ character.

Lane alignment checking is not performed by the LAS after lane alignment is achieved. After LAM detects that the LS_OK_IN_A/B signal is asserted, normal system traffic is carried instead of the proprietary lane alignment pattern.

Channel Synchronization is performed during lane alignment and normal system operation.

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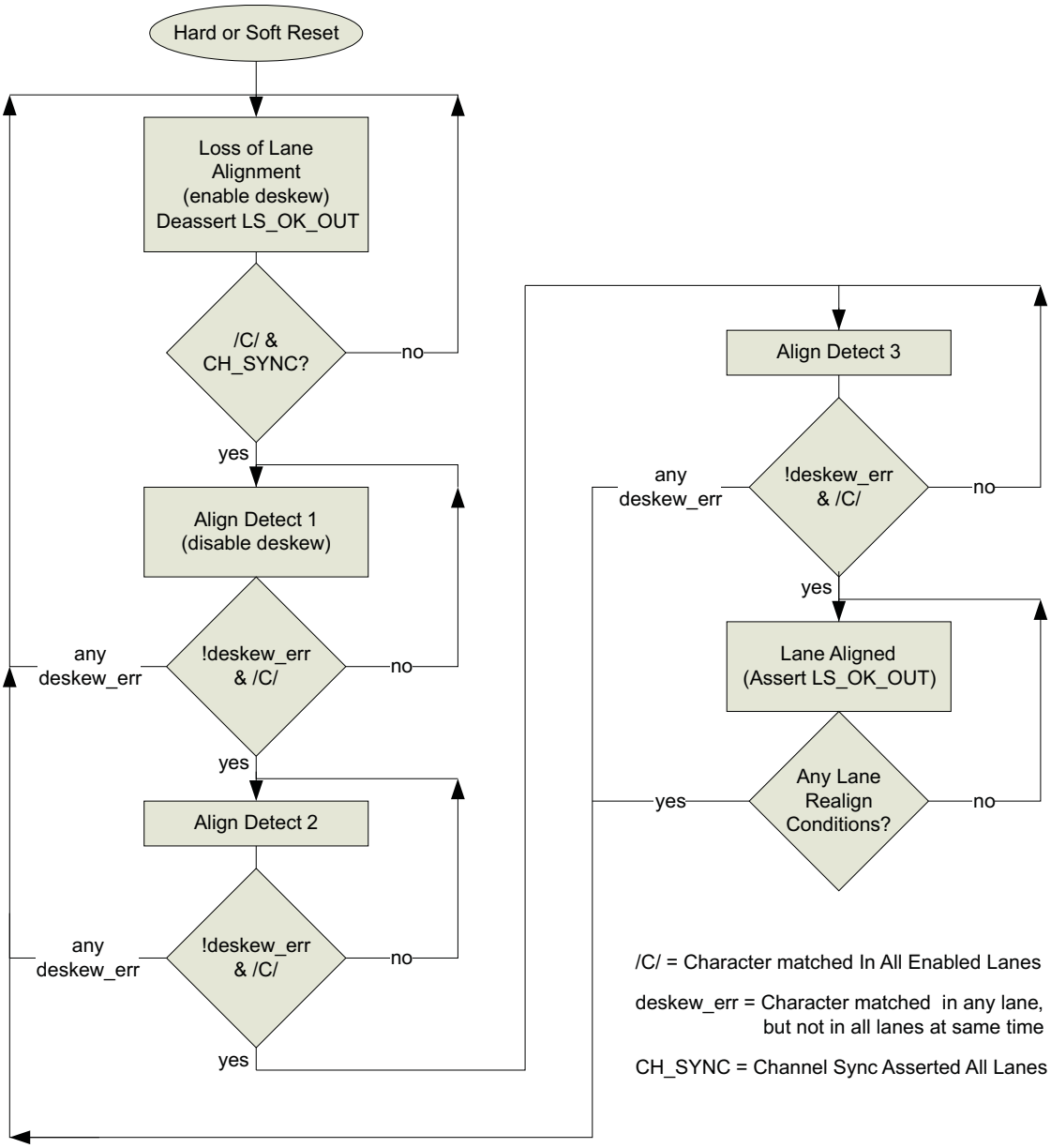

Figure 11. Lane Alignment State Machine

8.3.5 Channel Synchronization

The TLK10002 performs channel synchronization per lane as per IEEE802.3-2002 Figure 36–9 Synchronization state diagram and as shown in the flowchart of Figure 12.

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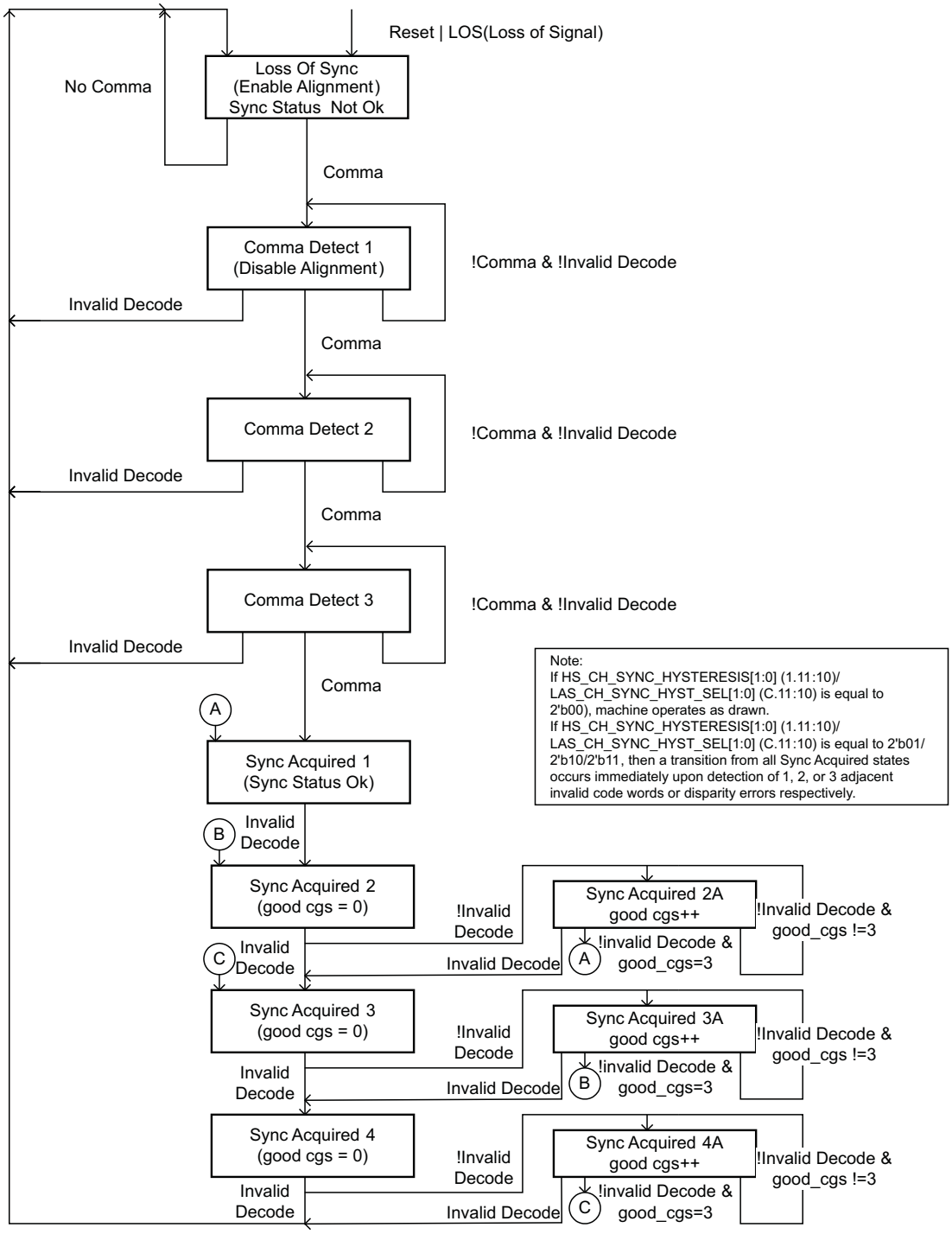

Figure 12. Channel Synchronization Flowchart

8.3.6 Line Rate, SERDES PLL Settings, and Reference Clock Selection

The TLK10002 includes internal low-jitter high quality oscillators that are used as frequency multipliers for the low-speed and high-speed SERDES and other internal circuits of the device. Specific MDIO registers are available for SERDES rate and PLL multiplier selection to match line rates and reference clock (REFCLK0/1) frequencies for various applications.

The external differential reference clock has a large operating frequency range allowing support for many different applications. The reference clock frequency must be within 200 PPM of the incoming serial data rate (±100 PPM of nominal data rate), and have less than 40 ps of jitter. Table 2 shows a summary of line rates and reference clock frequencies used for CPRI/OBSAI for the 1:1, 2:1, and 4:1 operation modes.

Table 2. Specific Line Rate Selection for the 1:1 Operation Mode

LOW-SPEED SIDE					HIGH-SPEED SIDE			
LINE RATE (Mbps)	SERDES PLL MULTIPLIER	RATE	REFCLKP/N (MHz)		LINE RATE (Mbps)	SERDES PLL MULTIPLIER	RATE	REFCLKP/N (MHz)
4915.2	20	Full	122.88		4915.2	20	Half	122.88
3840	12.5	Full	153.6		3840	12.5	Half	153.6
3072	10	Full	153.6		3072	10	Half	153.6
2457.6	8/10	Full	153.6/122.88		2457.6	16/20	Quarter	153.6/122.88
1920	12.5	Half	153.6		1920	12.5	Quarter	153.6
1536	10	Half	153.6		1536	10	Quarter	153.6
1228.8	8/10	Half	153.6/122.88		1228.8	16/20	Eighth	153.6/122.88

Table 3. Specific Line Rate Selection for the 2:1 Operation Mode

LOW-SPEED SIDE					HIGH-SPEED SIDE			
LINE RATE (Mbps)	SERDES PLL MULTIPLIER	RATE	REFCLKP/N (MHz)		LINE RATE (Mbps)	SERDES PLL MULTIPLIER	RATE	REFCLKP/N (MHz)
4915.2	20	Full	122.88		9830.4	20	Full	122.88
3840	12.5	Full	153.6		7680	12.5	Full	153.6
3072	10	Full	153.6		6144	10	Full	153.6
2457.6	8/10	Full	153.6/122.88		4915.2	16/20	Half	153.6/122.88
1920	12.5	Half	153.6		3840	12.5	Half	153.6
1536	10	Half	153.6		3072	10	Half	153.6
1228.8	8/10	Half	153.6/122.88		2457.6	16/20	Quarter	153.6/122.88
768	10	Quarter	153.6		1536	10	Quarter	153.6
614.4	8/10	Quarter	153.6/122.88		1228.8	16/20	Eighth	153.6/122.88

Table 4. Specific Line Rate Selection for the 4:1 Operation Mode

LOW-SPEED SIDE					HIGH SPEED-SIDE			
LINE RATE (Mbps)	SERDES PLL MULTIPLIER	RATE	REFCLKP/N (MHz)		LINE RATE (Mbps)	SERDES PLL MULTIPLIER	RATE	REFCLKP/N (MHz)
2457.6	8/10	Full	153.6/122.88		9830.4	16/20	Full	153.6/122.88
1536	10	Half	153.6		6144	10	Full	153.6
1228.8	8/10	Half	153.6/122.88		4915.2	16/20	Half	153.6/122.88
768	10	Quarter	153.6		3072	10	Half	153.6
614.4	8/10	Quarter	153.6/122.88		2457.6	16/20	Quarter	153.6/122.88

Table 2, Table 3, and Table 4 indicate two possible reference clock frequencies for CPRI/OBSAI applications: 153.6 MHz and 122.88 MHz, which can be used based on the application preference. The SERDES PLL Multiplier (MPY) has been given for each reference clock frequency respectively. For each channel, the low-speed side and the high-speed side SERDES use the same reference clock frequency. Note that Channel A and B are independent and their application rates and references clocks are separate.

For other line rates not shown in Table 3 and Table 4, valid reference clock frequencies can be selected with the help of the information provided in Table 5 and Table 6 for the low-speed side and high-speed side SERDES. **The reference clock frequency has to be the same for the two SERDES and must be within the specified valid ranges for different PLL multipliers.**

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Table 5. Line Rate and Reference Clock Frequency Ranges for the Low-Speed Side SERDES

SERDES PLL MULTIPLIER (MPY)	REFERENCE CLOCK (MHz)		FULL RATE (Gbps)		HALF RATE (Gbps)		QUARTER RATE (Gbps)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
4	250	425	2	3.4	1	1.7	0.5	0.85
5	200	425	2	4.25	1	2.125	0.5	1.0625
6	166.667	416.667	2	5	1	2.5	0.5	1.25
8	125	312.5	2	5	1	2.5	0.5	1.25
10	122.88	250	2.4576	5	1.2288	2.5	0.6144	1.25
12	122.88	208.333	2.94912	5	1.47456	2.5	0.73728	1.25
12.5	122.88	200	3.072	5	1.536	2.5	0.768	1.25
15	122.88	166.667	3.6864	5	1.8432	2.5	0.9216	1.25
20	122.88	125	4.9152	5	2.4576	2.5	1.2288	1.25
RateScale: Full Rate = 0.5, Half Rate = 1, Quarter Rate = 2								

Table 6. Line Rate and Reference Clock Frequency Ranges for the High-Speed Side SERDES

SERDES PLL MULTIPLIER (MPY)	REFERENCE CLOCK (MHz)		FULL RATE (Gbps)		HALF RATE (Gbps)		QUARTER RATE (Gbps)		EIGHTH RATE (Gbps)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
4	375	425	6	6.8	3	3.4	1.5	1.7		
5	300	425	6	8.5	3	4.25	1.5	2.125	1	1.0625
6	250	416.667	6	10	3	5	1.5	2.5	1	1.25
8	187.5	312.5	6	10	3	5	1.5	2.5	1	1.25
10	150	250	6	10	3	5	1.5	2.5	1	1.25
12	125	208.333	6	10	3	5	1.5	2.5	1	1.25
12.5	153.6	200	7.68	10	3.84	5	1.92	2.5	1	1.25
15	122.88	166.667	7.3728	10	3.6864	5	1.8432	2.5	1	1.25
16	122.88	156.25	7.864	10	3.932	5	1.966	2.5	1	1.25
20	122.88	125	9.8304	10	4.9152	5	2.4576	2.5	1.2288	1.25
RateScale: Full Rate = 0.25, Half Rate = 0.5, Quarter Rate = 1, Eighth Rate = 2										

For example, in the 2:1 operation mode, if the low-speed side line rate is 1.987 Gbps, the high-speed side line rate is 3.974 Gbps. The following steps can be taken to make a reference clock frequency selection:

1. Determine the appropriate SERDES rate modes that support the required line rates. Table 5 shows that the 1.987 Gbps line rate on the low-speed side is only supported in the half rate mode (RateScale = 1). Table 6 shows that the 3.974 Gbps line rate on the high-speed side is only supported in the half rate mode (RateScale = 0.5).
2. For each SERDES side, and for all available PLL multipliers (MPY), compute the corresponding reference clock frequencies using the formula:

   Reference Clock Frequency = (LineRate x RateScale)/MPY

   The computed reference clock frequencies are shown in Table 7 along with the valid minimum and maximum frequency values.
3. Mark all the common frequencies that appear on both SERDES sides. Note and discard all those that fall outside the allowed range. In this example, the common frequencies are highlighted in Table 7.
4. Select any of the remaining marked common reference clock frequencies. Higher reference clock frequencies are generally preferred. In this example, any of the reference clock frequencies in Table 7 can be selected: 397.4 MHz, 331.167 MHz, 248.375 MHz, 198.7 MHz, 165.583 MHz, 158.96 MHz, and 132.467 MHz.

Table 7. Reference Clock Frequency Selection Example

LOW-SPEED SIDE SERDES					HIGH-SPEED SIDE SERDES			
SERDES PLL MULTIPLIER	REFERENCE CLOCK FREQUENCY (MHz)				SERDES PLL MULTIPLIER	REFERENCE CLOCK FREQUENCY (MHz)		
	COMPUTED	MIN	MAX			COMPUTED	MIN	MAX
4	496.750	250	425		4	496.750	250	425
5	397.400	200	425		5	397.400	200	425
6	331.167	166.667	416.667		6	331.167	166.667	416.667
8	248.375	125	312.5		8	248.375	125	312.5
10	198.700	122.88	250		10	198.700	122.88	250
12	165.583	122.88	208.333		12	165.583	122.88	208.333
12.5	158.960	122.88	200		12.5	158.960	122.88	200
15	132.467	122.88	166.667		15	132.467	122.88	166.667
20	99.350	122.88	125		20	99.350	122.88	125

8.3.7 Clocking Architecture

A simplified clocking architecture for the TLK10002 is captured in Figure 13. Each channel (Channel A or Channel B) has an option of operating with a differential reference clock provided either on pins REFCLK0P/N or REFCLK1P/N. The choice is made either through MDIO or through REFCLKA_SEL and REFCLKB_SEL pins. The reference clock frequencies for those two clock inputs can be different as long as they fall under the valid ranges shown in Table 6. For each channel, the low-speed side SERDES, high-speed side SERDES and the associated part of the digital core operate from the same reference clock.

The clock and data recovery (CDR) function of the high-speed side receiver recovers the clock from the incoming serial data. The high-speed side SERDES makes available two versions of clocks for further processing:

1. HS_RXBCLK_A/B: recovered byte clock synchronous with incoming serial data and with a frequency matching the incoming line rate divided by 20.
2. VCO_CLOCK_A/B_DIV2: VCO frequency divided by 2. (VCO frequency = REFCLK x PLL Multiplier).

The above-mentioned clocks can be output through the differential pins, CLKOUTAP/N and CLKOUTBP/N, with optional frequency division ratios of 1, 2, 4, 5, 8, 10, 16, 20, or 25. The clock output options are software controlled through the MDIO interface register bits 1.3:2, and 1.7:4. The maximum CLKOUT frequency is 500 MHz.

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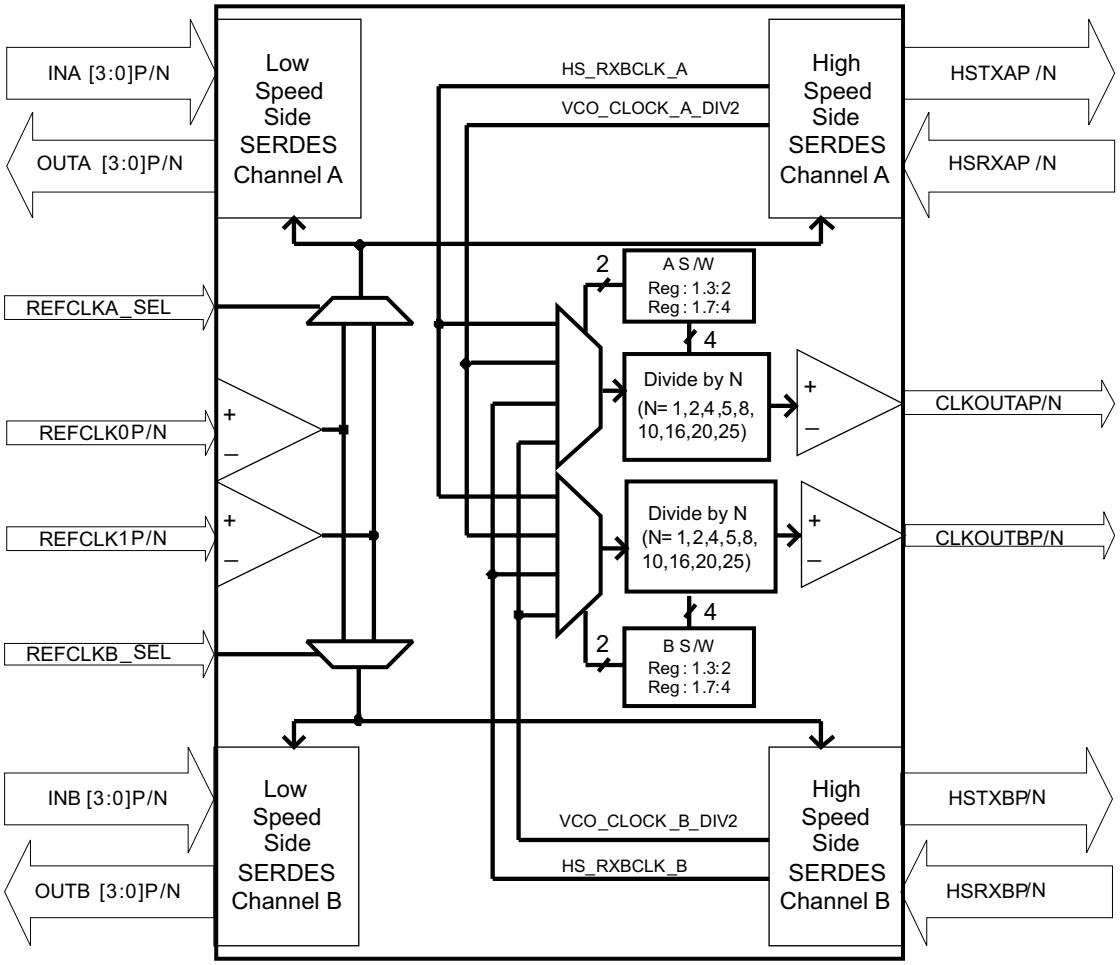

Figure 13. Clocking Architecture

8.3.8 Loopback Modes

The TLK10002 provides two high-speed side (remote) and two low-speed side (local) loopback modes for self-test and system diagnostic purposes. The details of those loopback modes are discussed below.

8.3.9 Deep Remote Loopback

The deep remote loopback is as shown Figure 14 for Channel A. The configuration is the same for Channel B. The loopback mode is activated and configured through the MDIO interface. In this loopback mode, the data is accepted on the high-speed side receive SERDES pins (HSRXAP/N or HSRXBP/N), traverses the entire receive data path excluding the CML driver and receive sense amps on the low-speed side SERDES, returned through the entire transmit data path and sent out through the high-speed side transmit SERDES pins (HSTXAP/N or HSTXBP/N).

The low-speed side outputs on OUTA*P/N or OUTB*P/N pins are still available for monitoring. See MDIO register bit 6.7 in Table 21 for more information. The OUTA*P/N and OUTB*P/N pins must be correctly terminated.

The link partner connected through INA*P/N or INB*P/N pins must be electrically idle at differential zero with P and N signals at the same voltage. The TLK10002 device needs some time for lane alignment before passing traffic. The LS_OK_IN_A/B signal is ignored as the device is internally listening to the local LS_OK_OUT_A/B.

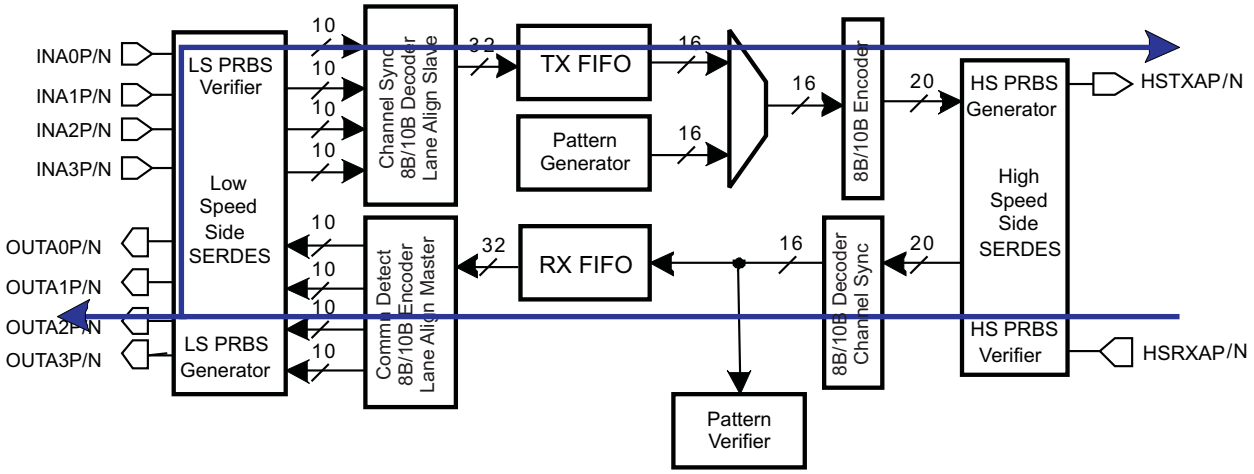

Figure 14. Deep Remote Loopback

8.3.10 Shallow Remote Loopback and Serial Retime

The shallow remote loopback is as shown in Figure 15 for Channel A. The configuration is the same for Channel B. The loopback mode is activated and configured through the MDIO interface. In this loopback mode, the data is accepted on the high-speed side receive SERDES pins (HSRXAP/N or HSRXBP/N), traverses the receive data path and looped back before the low-speed SERDES, returned through the transmit data path and sent out through the high-speed side transmit SERDES pins (HSTXAP/N or HSTXBP/N).

The low-speed side transmit path SERDES can be optionally enabled or disabled but the PLL needs to be enabled to provide the required clock.

The low-speed side outputs on OUTA*P/N or OUTB*P/N pins are still available for monitoring. The OUTA*P/N and OUTB*P/N pins must be correctly terminated. The TLK10002 device needs some time for lane alignment before passing traffic. The LS_OK_IN_A/B signal is ignored as the device is internally listening to the local LS_OK_OUT_A/B.

This loopback mode can be used for high-speed serial retime operation.

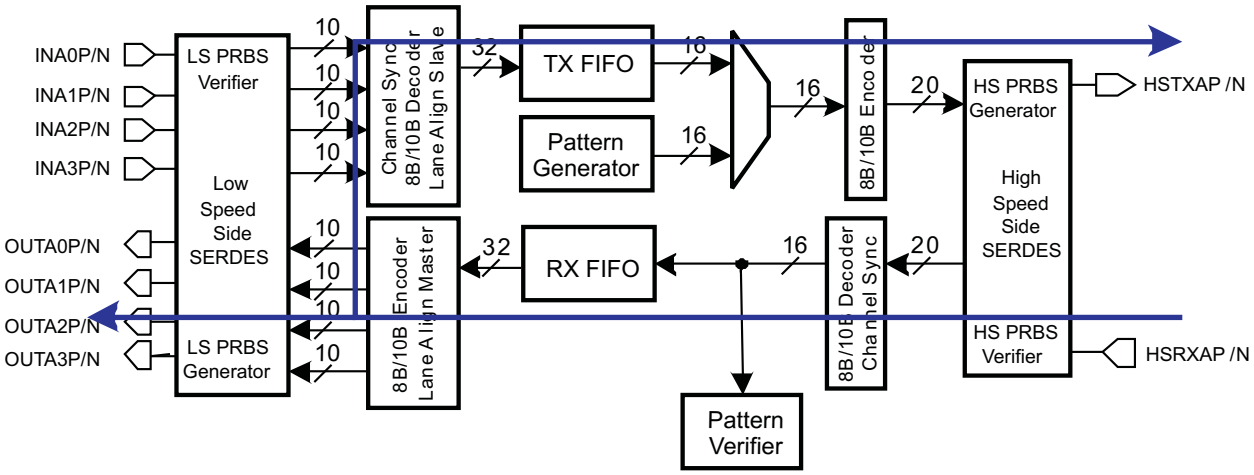

Figure 15. Shallow Remote Loopback

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8.3.11 Deep Local Loopback

The deep local loopback mode is as shown in Figure 16 for Channel A. The configuration is the same for Channel B. The loopback mode is activated and configured through the MDIO interface. In this loopback mode, the data is accepted on the low-speed side SERDES pins (INA*P/N or INB*P/N), traverses the entire transmit data path excluding the CML driver, returned through the entire receive data path and sent out through the low-speed side SERDES pins (OUTA*P/N or OUTB*P/N). The TLK10002 device needs some time for lane alignment before passing traffic. The high-speed side outputs on HSTXAP/N or HSTXBP/N pins are available for monitoring.

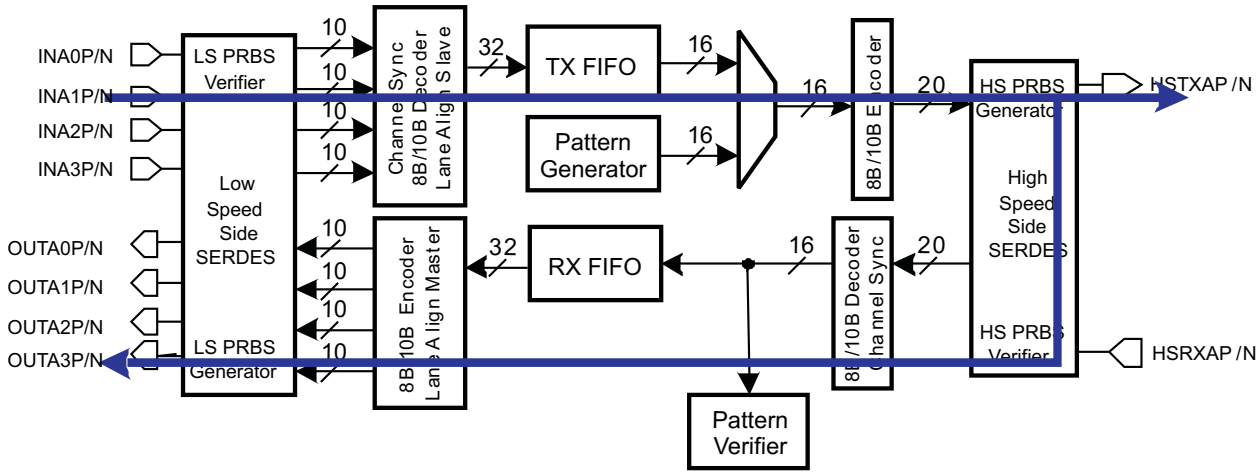

Figure 16. Deep Local Loopback

8.3.12 Shallow Local Loopback

The shallow local loopback mode is as shown in Figure 17 for Channel A. The configuration is the same for Channel B. The loopback mode is activated and configured through the MDIO interface. In this loopback mode, the data is accepted on the low-speed side SERDES pins (INA x P/N or INB x P/N), traverses the entire transmit data path excluding the high-speed side SERDES, returned through the entire receive data path and sent out through the low-speed side SERDES pins (OUTA x P/N or OUTB x P/N). The TLK10002 device needs some time for lane alignment before passing traffic. The high-speed side outputs on HSTXAP/N or HSTXBP/N pins are available for monitoring.

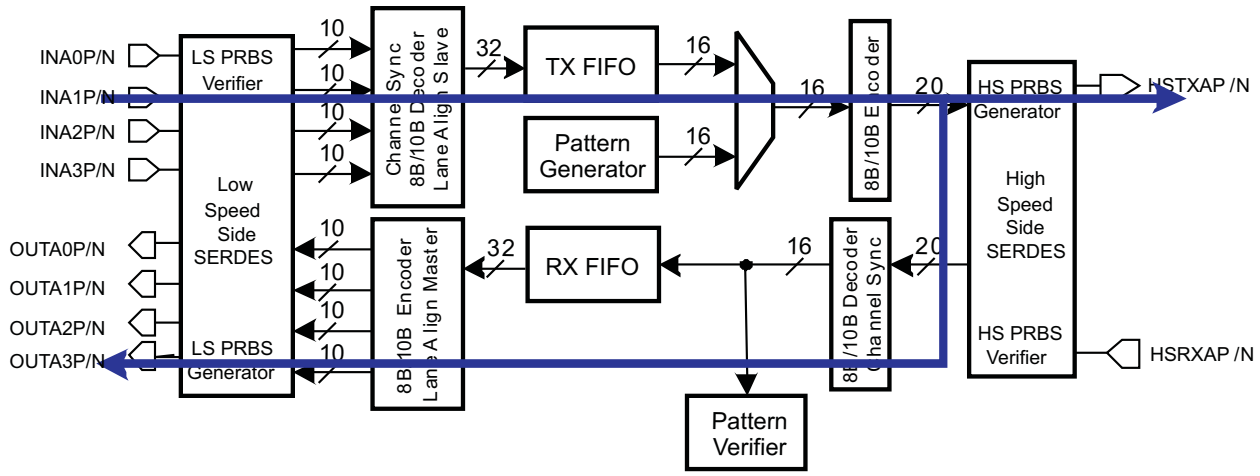

Figure 17. Shallow Local Loopback

8.3.13 Test Pattern Generation and Verification

The TLK10002 has an extensive suite of built-in test functions to support system diagnostic requirements. Each channel has sets of internal test pattern generators and verifiers.

Several patterns can be selected through the MDIO interface that offer extensive test coverage. The low-speed side supports generation and verification of pseudo-random bit sequence (PRBS) 2^7-1, 2^{23}-1, and 2^{31}-1 patterns. In addition to those PRBS patterns, the high-speed side supports High-frequency (HF), Low-frequency (LF), Mixed-frequency (MF), and continuous random test pattern (CRPAT) long/short pattern generation and verification as defined in Annex 48A of the IEEE Standard 802.3ae-2002. Use of CRPAT verifier requires checking TPsync (MDIO register bit F.15).

The TLK10002 provides two pins: PRBSEN and PRBS_PASS, for additional and easy control and monitoring of PRBS pattern generation and verification. When the PRBSEN is asserted high, the internal PRBS generator and verifier circuits are enabled on both transmit and receive data paths on high-speed and low-speed sides of both channels. This signal is logically OR'd with an MDIO register bits B.7:6 and B.13:12.

PRBS 2^{31}-1 is selected by default, and can be changed through MDIO.

When PRBS test is enabled (PRBSEN=1):

- PRBS_PASS=1 indicates that PRBS pattern reception is error free.
- PRBS_PASS=0 indicates that a PRBS error is detected. The channel, the side (high speed or low speed), and the lane (for low-speed side) that this signal refers to is chosen through MDIO register bit 0.3:0.

8.3.14 Latency Measurement Function

The TLK10002 includes a latency measurement function to support CPRI and OBSAI base station applications. There are two start and two stop locations for the latency counter as shown in Figure 18 for Channel A. The start and stop locations are selectable through MDIO register bits 0x16.7 and 0x16.6 respectively. The elapsed time from a comma detected at an assigned counter start location of a particular channel to a comma detected at an assigned counter stop location of the same channel is measured and reported through the MDIO interface. The function operates on one channel at a time. The following three control characters (containing commas) are monitored:

1. K28.1 (control = 1, data = 0x3C)
2. K28.5 (control = 1, data = 0xBC)
3. K28.7 (control = 1, data = 0xFC).

The first comma found at the assigned counter start location starts up the latency counter. The first comma detected at the assigned counter stop location stops the latency counter. The 20-bit latency counter result of this measurement is readable through the MDIO interface through register bits 0x17.3:0 and 0x18.15:0. The accuracy of the measurement is a function of the serial bit rate at which the channel being measured is operating. The register will return a value of 0xFFFF if the duration between transmit and receive comma detection exceeds the depth of the counter. Only one measurement value is stored internally until the 20-bit results counter is read. The counter will return zero in cases where a transmit comma was never detected (indicating the results counter never began counting).

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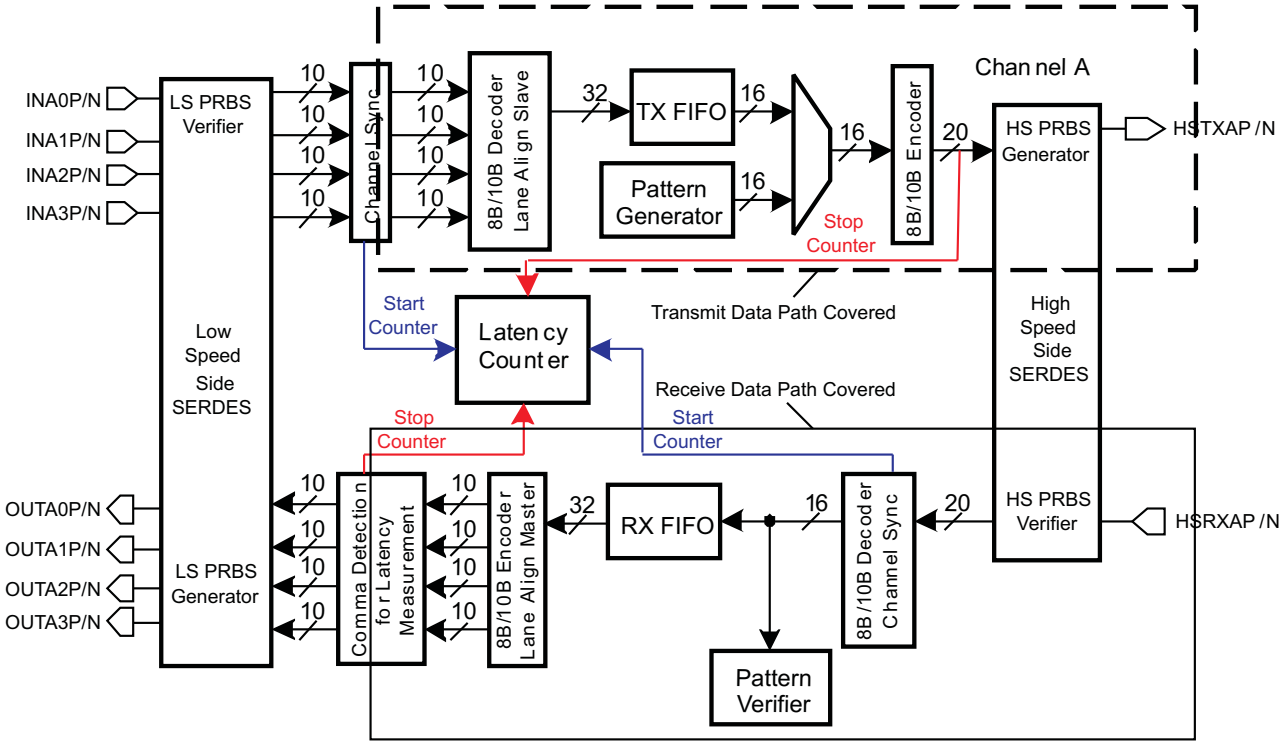


Figure 18. Location of TX and RX Comma Character Detection (Only Channel A Shown)

In high-speed side SERDES full rate mode, the latency measurement function runs off of an internal clock whose rate is equal to the transmit serial bit rate divided by 8. In half rate mode, the latency measurement function runs off of an internal clock whose rate is equal to the serial bit rate divided by 4. In quarter rate mode, the latency measurement function runs off of an internal clock whose rate is equal to the serial bit rate divided by 2. In eighth rate mode, the latency measurement function runs off of a clock whose rate is equal to the serial bit rate.

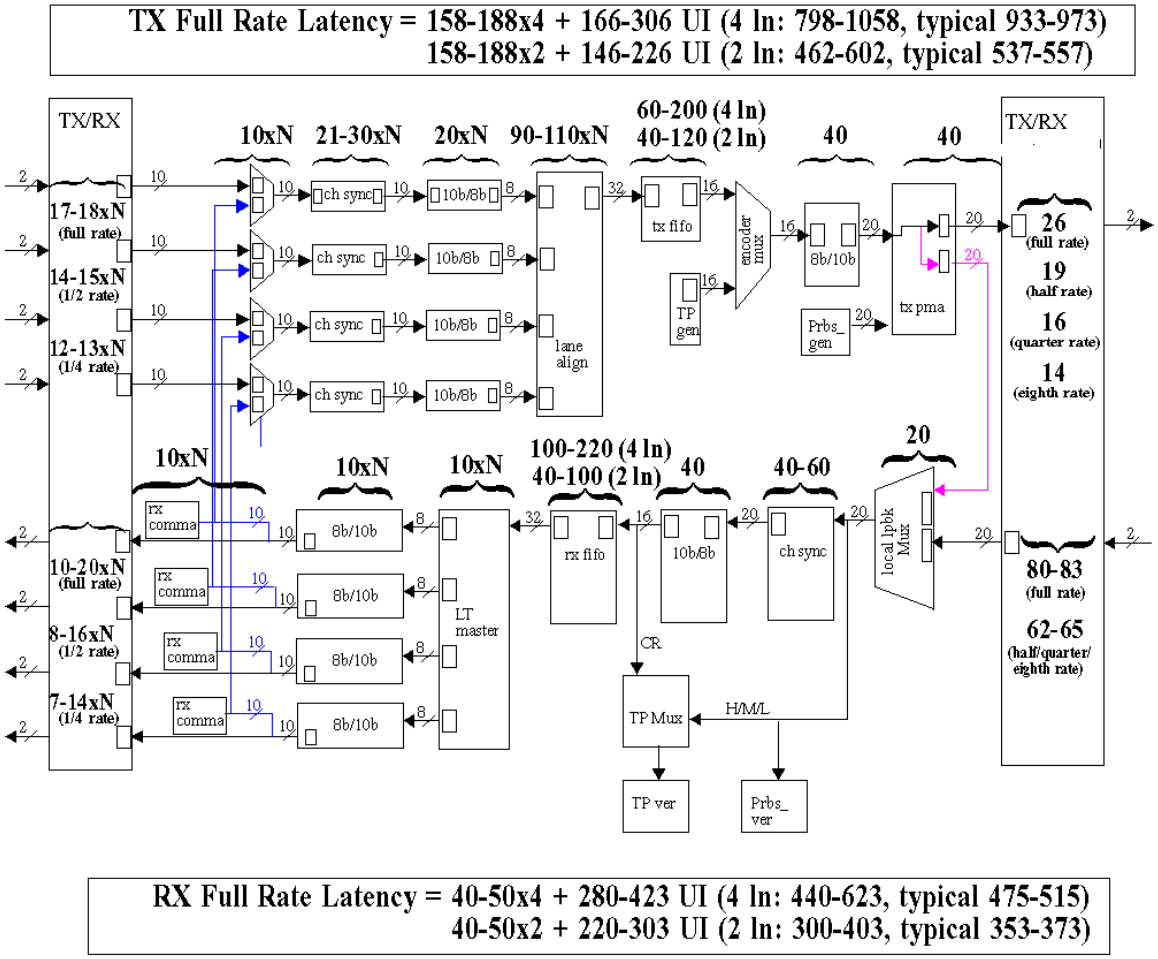
The latency measurement does not include the low-speed side transmit SERDES blocks contribution as well as part of the channel synchronization block. The latency introduced by these blocks can be estimated to be up to (18 + 10) x N high-speed side unit intervals (UIs), where the multiplex factor N is equal to 2 (in 2:1 mode) or 4 (in 4:1 mode). The latency measurement also doesn't account for the low-speed side receive SERDES contribution which is estimated to be up to 20 x N high-speed side UIs. The latency contributions of various sections of the TLK10002 device are shown in Figure 17. Overall, the transmit data path full rate latency contribution is estimated to be between 462UI and 602UI for the 2:1 mode, and between 798UI and 1058UI for the 4:1 mode. The respective numbers for the receive data path are between 300UI and 403UI for the 2:1 mode and between 440UI and 623UI for the 4:1 mode.

The latency measurement accuracy in all cases is equal to plus or minus one latency measurement clock period. The measurement clock can be divided down if a longer duration measurement is required, in which case the accuracy of the measurement is accordingly reduced. The high-speed latency measurement clock is divided by either 1, 2, 4, or 8 via register 0x16 bits 5:4. The measurement clock used is always selected by the channel under test. The high-speed latency measurement clock may only be used when operating at one of the serial rates specified in the CPRI/OBSAI specifications. It is also possible to run the latency measurement function off of the recovered byte clock for the channel under test (and gives a latency measurement clock frequency equal to the serial bit rate divided by 20) through register 0x16 bit 2 (where the register 0x16 bits 5:4 divider value setting is ignored).

The accuracy for the standard based CPRI/OBSAI application rates is shown in Table 8, and assumes the latency measurement clock is not divided down per user selection (division is required to measure a duration greater than 682 µs). For each division of two in the measurement clock, the accuracy is also reduced by a factor of two.

To use the latency measurement feature, follow this procedure:

1. Provision stopwatch clock frequency (divide by N), channel select, and start or stop location through the LATENCY_MEASURE_CONTROL register (0x16) and enable the stopwatch clock. In choosing a divider, note that the frequency of the divided clock must not be slower than the internal high speed byte clock.
2. Read status register 18.15:0 to clear and reset delay stopwatch.
3. Send comma pattern (after lane alignment has been achieved and the link status is OK).
4. Poll bit 17.4 until it is asserted.
5. Read the start and stop comma location and the lane align pointer values indicating relative skew among the lanes of the selected channel. These may need to be processed together with the stopwatch counter values for more accurate latency analysis.
6. Read counter status values. The four MSB in bits 17.3:0 should be read first, followed by the LSBs in 18.15:0. If the value is 0, then the comma was never detected. If the value is at its maximum, the delay was too long for the counter's range. If this happens, decrease the measurement clock frequency and repeat the measurement.
7. Once the lower 16 bits at 18.15:0 are read, the delay stopwatch is reset and 17.4 is cleared. The comma location latch registers are cleared too. To do a new measurement, start again from step (3) for the same channel and from step (1) if a different channel is desired.
8. Take the counter value and multiply it with the latency clock period divided by 2. This will provide the absolute latency period.



NOTE: Latency numbers represent no external skew between lanes. External lane skew will increase overall latency. TX Datapath latency includes 20xN UI of variance due to deserialization and channel sync.

Figure 19. Latency Variance and Contributions (Only Channel A Shown)

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Table 8. CPRI/OBSAI Latency Measurement Function Accuracy (Undivided Measurement Clock)

LINE RATE (Gbps)	RATE	LATENCY CLOCK FREQUENCY (GHz)	ACCURACY (± ns)
1.2288	Eighth	1.2288	0.8138
1.536	Quarter	0.768	1.302
2.4576	Quarter	1.2288	0.8138
3.072	Half	0.768	1.302
3.84	Half	0.96	1.0417
4.9152	Half	1.2288	0.8138
6.144	Full	0.768	1.302
7.68	Full	0.96	1.0417
9.8304	Full	1.2288	0.8138

8.3.15 Power-Down Mode

The TLK10002 can be put in power down either through device inputs pins or through MDIO control register (1.15).

PDTRXA_N: Active low, powers down channel A.
PDTRXB_N: Active low, powers down channel B.

The MDIO management serial interface remains operational when in register-based, power-down mode (1.15 asserted for both channels), but status bits may not be valid since the clocks are disabled. The low-speed side and high-speed side SERDES outputs are high impedance when in power-down mode. See the detailed per pin description for the behavior of each device I/O signal during pin-based and register-based power down.

8.3.16 High Speed CML Output

The high-speed data output driver is implemented using Current Mode Logic (CML) with integrated pullup resistors, requiring no external components. The transmit outputs must be AC-coupled.

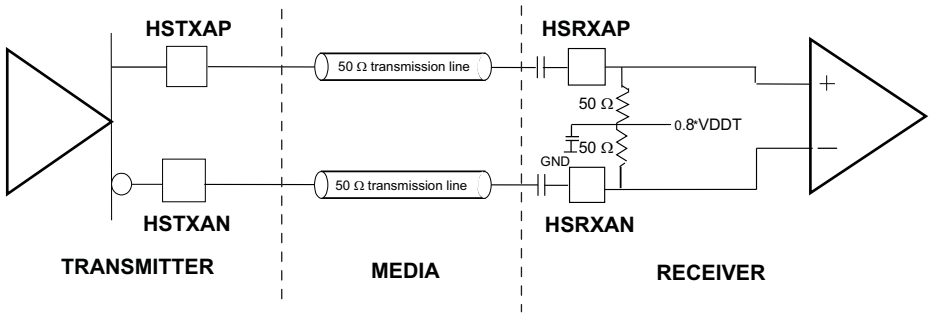

Figure 20. Example of High-Speed I/O AC-Coupled Mode (Channel A HS Side is Shown)

Current Mode Logic (CML) drivers often require external components. The disadvantage of the external component is a limited edge rate due to package and line parasitic. The CML driver on TLK10002 has on-chip 50-Ω termination resistors terminated to VDDT, providing optimum performance for increased speed requirements. The transmitter output driver is highly configurable allowing output amplitude and de-emphasis to be tuned to a channel's individual requirements. Software programmability allows for very flexible output amplitude control. Only AC-coupled output mode is supported.

When transmitting data across long lengths of PCB trace or cable, the high-frequency content of the signal is attenuated due to the skin effect of the media. This causes a *smearing* of the data eye when viewed on an oscilloscope. The net result is reduced timing margins for the receiver and clock recovery circuits. In order to provide equalization for the high frequency loss, 3-tap finite impulse response (FIR) transmit de-emphasis is implemented. A highly configurable output driver maximizes flexibility in the end system by allowing de-emphasis and output amplitude to be tuned to a channel's individual requirements. Output swing is controlled via MDIO.

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Figure 2 illustrates the output waveform flexibility. The level of de-emphasis is programmable through the MDIO interface through control registers (5.7:4 and 5.12:8) through pre-cursor and post-cursor settings. Users can control the strength of the de-emphasis to optimize for a specific system requirement.

8.3.17 High Speed Receiver

The high-speed receiver is differential CML with internal termination resistors. The receiver requires AC coupling. The termination impedances of the receivers are configured as 100 Ω with the center tap weakly tied to 0.8 × VDDT with a capacitor to create an AC ground.

TLK10002 serial receivers incorporate adaptive equalizers. This circuit compensates for channel insertion loss by amplifying the high frequency components of the signal, reducing inter-symbol interference. Equalization can be enabled or disabled through register settings. Both the gain and bandwidth of the equalizer are controlled by the receiver equalization logic.

8.3.18 Loss of Signal Indication (LOS)

Loss of input signal detection is based on the voltage level of each serial input signal INA x P/N, INB x P/N, HSRXAP/N, and HSRXBP/N. When LOS indication is enabled and a channel's differential serial receive input level is < 75 mVpp, that channel's respective LOS indicator (LOSA or LOSB) is asserted (high true). If the input signal is >150 mVpp, the LOS indicator is deasserted (low false). Outside of these ranges, the LOS indication is undefined. The LOS indicators are also directly readable through the MDIO interface.

The following additional critical status conditions can be combined with the loss of signal condition enabling additional real-time status signal visibility on the LOSA and LOSB outputs per channel:

1. Loss of Channel Synchronization Status – Logically OR'd with LOS condition(s) when enabled. Loss of channel synchronization can be optionally logically OR'd (disabled by default) with the internally generated LOS condition (per channel).
2. Loss of PLL Lock Status on LS and HS sides – Logically OR'd with LOS condition(s) when enabled. The internal PLL loss of lock status bit is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
3. Receive 8B/10B Decode Error (Invalid Code Word or Running Disparity Error) – Logically OR'd with LOS condition(s) when enabled. The occurrence of an 8B/10B decode error (invalid code word or disparity error) is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
4. AGCLOCK (Active Gain Control Currently Locked) – Inverted and Logically OR'd with LOS condition(s) when enabled. HS RX SERDES adaptive gain control unlocked indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
5. AZDONE (Auto Zero Calibration Done) – Inverted and Logically OR'd with LOS conditions(s) when enabled. HS RX SERDES auto-zero not done indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).

Figure 21 shows the detailed implementation of the LOSA signal along with the associated MDIO control registers.

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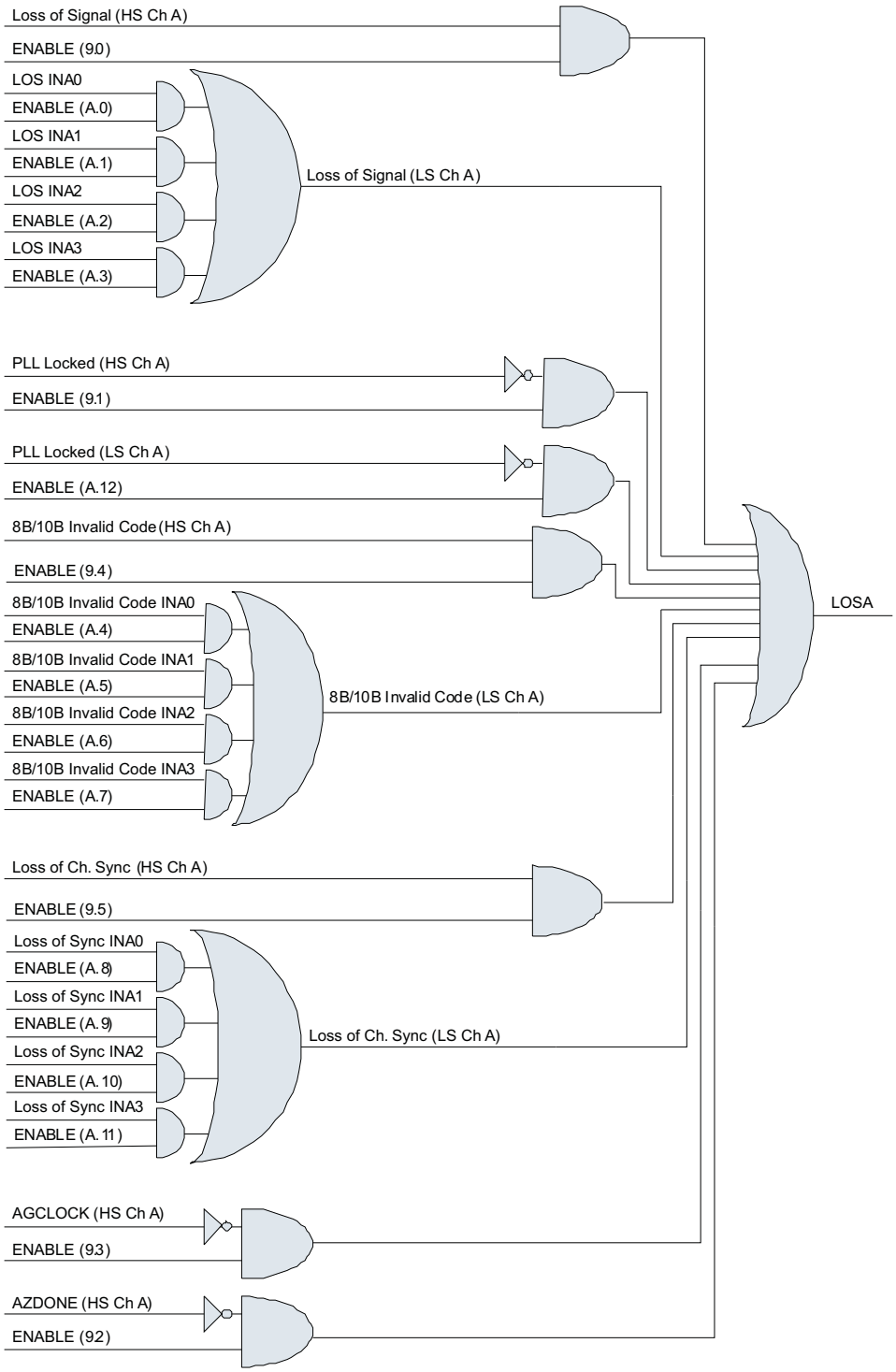


NOTE: LOSA is asserted (driven high) during a failing condition, and deasserted (driven low) otherwise. Any combinations of status signals may be enabled onto LOSA/B on MDIO register bits indicated above. LOSB circuit is similar.

Figure 21. LOSA – Logic Circuit Implementation

8.3.19 MDIO Management Interface

The TLK10002 supports the Management Data Input/Output (MDIO) Interface as defined in Clause 22 of the IEEE 802.3 Ethernet specification. The MDIO allows register-based management and control of the serial links.

The MDIO Interface consists of a bidirectional data path (MDIO) and a clock reference (MDC). The port address is determined by control pins PRTAD[4:0] as described in Pin Configuration and Functions.

In Clause 22, the top 4 control pins PRTAD[4:1] determine the device port address. In this mode the 2 individual channels in TLK10002 are classified as 2 different ports. So for any PRTAD[4:1] value there are 2 ports per TLK10002.

TLK10002 responds if the 4 MSB's of PHY address field on MDIO protocol (PA[4:1]) matches PRTAD[4:1]. The LSB of PHY address field (PA[0]) determines which channel/port within TLK10002 to respond to.

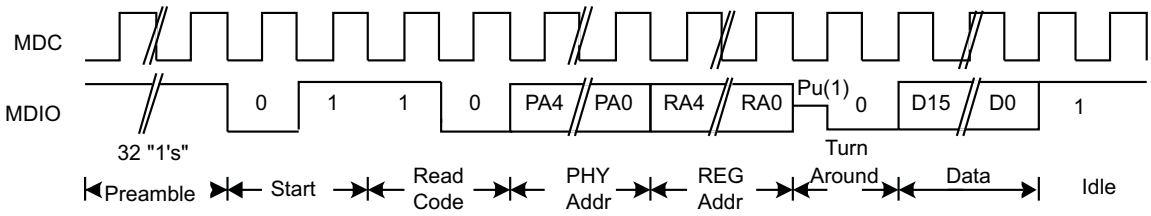
If PA[0] = 1'b0, TLK10002 Channel A will respond.

If PA[0] = 1'b1, TLK10002 Channel B responds.

Write transactions which address an invalid register or device, or a read-only register, are ignored. Read transactions which address an invalid register return a 0.

8.3.20 MDIO Protocol Timing

The Clause 22 timing required to read from the internal registers is shown in Figure 22. The Clause 22 timing required to write to the internal registers is shown in Figure 23.



(1) Note that the 1 in the Turn Around section is externally pulled up, and driven to Z by TLK10002.

Figure 22. CL22 - Management Interface Read Timing

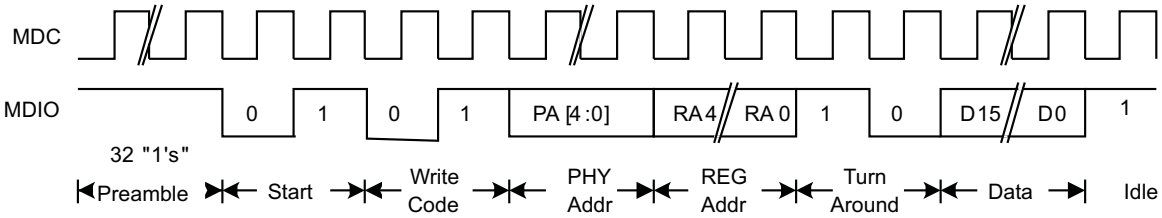


Figure 23. CL22 - Management Interface Write Timing

8.3.21 Clause 22 Indirect Addressing

The TLK10002 Register space is divided into two register groups. One register group can be addressed directly through Clause 22, and one register group can be addressed indirectly through Clause 22. The register group which can be addressed through Clause 22 indirectly is implemented in the vendor specific register space (16'h8000 onwards). Due to Clause 22 register space limitations, an indirect addressing method is implemented so that this extended register space can be accessed through Clause 22. To access this register space (16'h8000 onwards), an address control register (Reg 30, 5'h1E) must be written with the register address followed by a read or write transaction to address data register (Reg 31, 5'h1F) to access the contents of the address specified in address control register.

Figure 24 and Figure 25 illustrate an example write transaction to Register 16'h8000 using indirect addressing in Clause 22.

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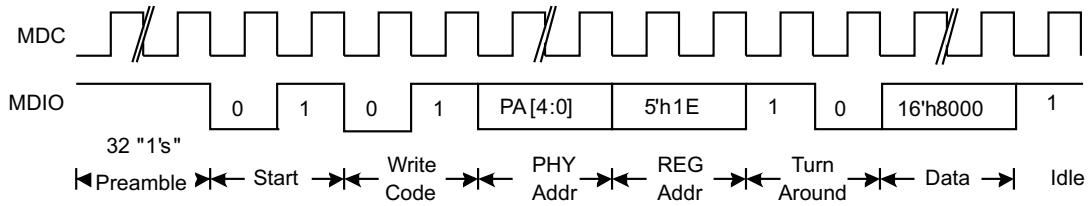


Figure 24. CL22 – Indirect Address Method – Address Write

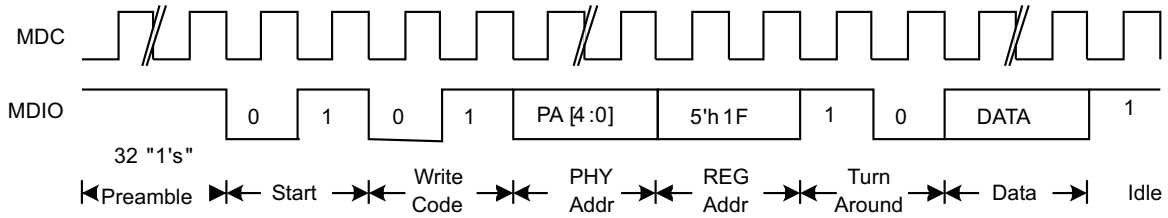


Figure 25. CL22 - Indirect Address Method – Data Write

Figure 26 and Figure 27 illustrate an example read transaction to read contents of Register 16'h8000 using indirect addressing in Clause 22.

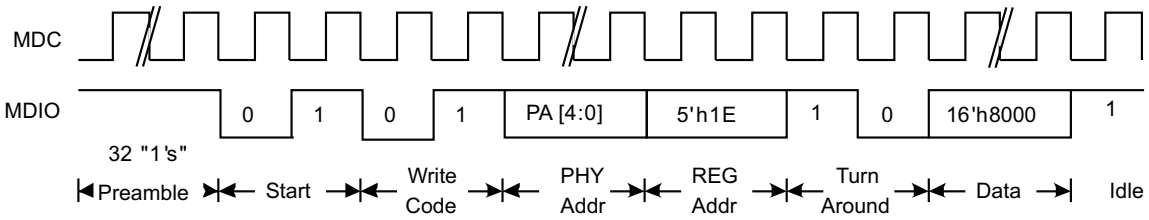
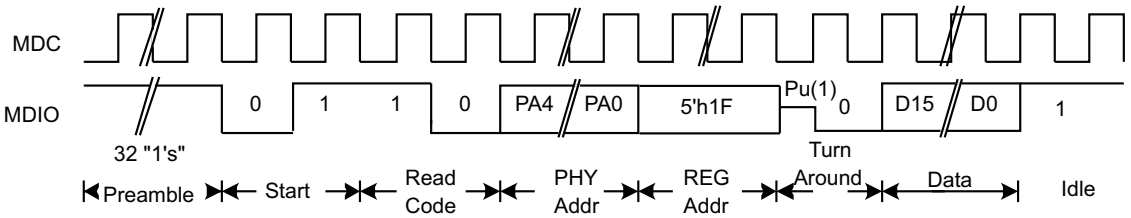


Figure 26. CL22 - Indirect Address Method – Address Write



(1) Note that the 1 in the Turn Around section is externally pulled up, and driven to Zero by TLK10002.

Figure 27. CL22 - Indirect Address Method – Data Read

The IEEE 802.3 Clause 22 specification defines many of the registers, and additional registers have been implemented for expanded functionality.

8.4 Device Functional Modes

8.4.1 Transmit (Low Speed to High Speed) Data Path

The TLK10002 transmit data path with the device configured to operate in the normal transceiver (mission) mode is as shown in Figure 28 and Figure 29. In this mode, 8B/10B encoded serial data (IN*P/N) in 2 or 4 lanes is received by the low-speed side SERDES and deserialized into 10-bit parallel data for each lane. The data in each individual lane is then byte aligned (channel synchronized) and then 8B/10B decoded into 8-bit parallel data for each lane. The lane data is then lane aligned by the Lane Alignment Slave. 32-bits of lane aligned parallel data is subsequently fed into a transmit FIFO which delivers it to an 8B/10B encoder, 16 data bits at a time. The resulting 20-bit 8B/10B encoded parallel data is handed to the high-speed side SERDES for serialization and output through the HSTX*P/N pins. This process is exactly the same for both Channel A and Channel B.

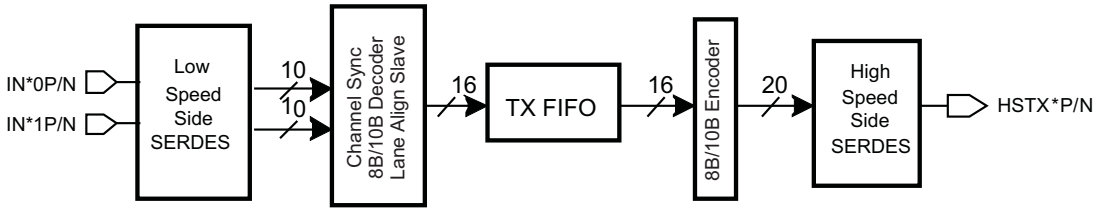


Figure 28. Transmit Data Path for the 2:1 Mode

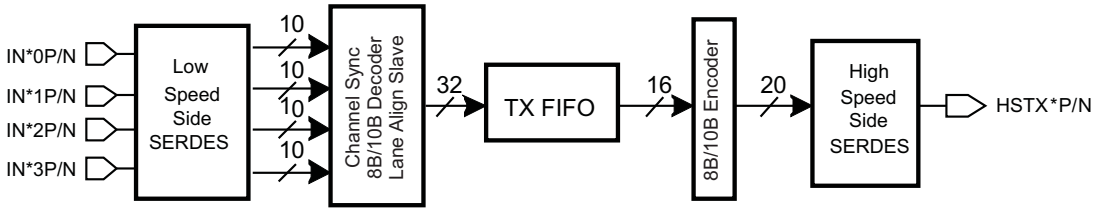


Figure 29. Transmit Data Path for the 4:1 Mode

8.4.2 Receive (High Speed to Low Speed) Data Path

With the device configured to operate in the normal transceiver (mission) mode, the receive data path is as shown in Figure 31. 8B/10B encoded serial data (HSRX*P/N) is received by the high-speed side SERDES and deserialized into 20-bit parallel data. The data is then byte aligned, 8B/10B decoded into 16-bit parallel data, and then delivered to a receive FIFO. The receive FIFO in turn delivers 32-bit parallel data to the Lane Alignment Master which splits the data into the same number of lanes as configured on the transmit data path. The lane data is then 8B/10B encoded and the resulting 10-bit parallel data for each lane is fed into the low-speed side SERDES for serialization and output through the OUT*P/N pins. This process is exactly the same for both Channel A and Channel B.

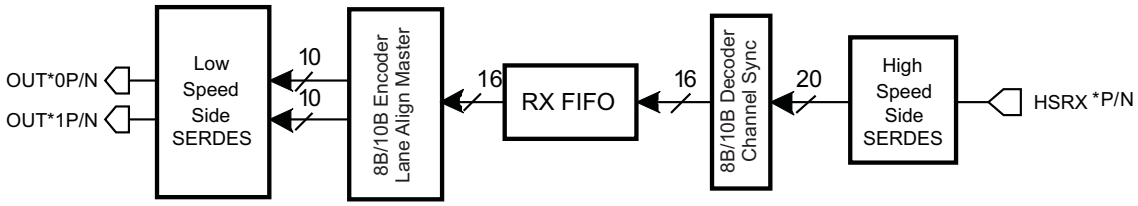


Figure 30. Receive Data Path for the 2:1 Modes

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Device Functional Modes (continued)

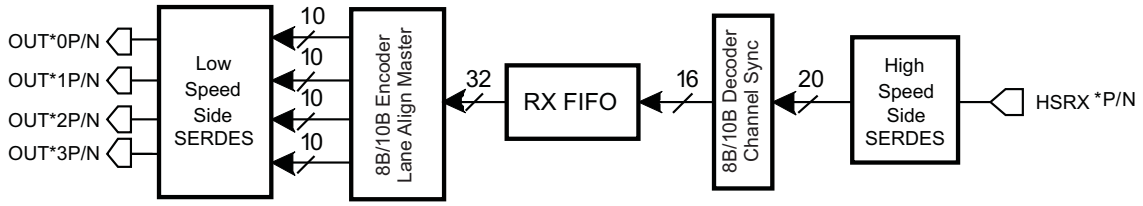

Figure 31. Receive Data Path for the 4:1 Modes

8.4.3 1:1 Retime Mode

In the 1:1 Retime mode shown in Figure 32, the lane alignment and 8B/10B encoding/decoding blocks are not included in the data path. In the transmit data path, low-speed side data received on the IN*0P/N pins is deserialized, phase corrected by the transmit FIFO, and serialized again before it is output through the HSTX*P/N pins. In the receive data path, high-speed side data received on the HSRX*P/N pins is deserialized, phase corrected by the receive FIFO, and serialized again before it is output through the OUT*0P/N pins. All SERDES controls such as preemphasis, swing, equalizer in registers HS/LS_SERDES_CONTROL_*, and loopback modes are supported as in the 2:1 and 4:1 modes.

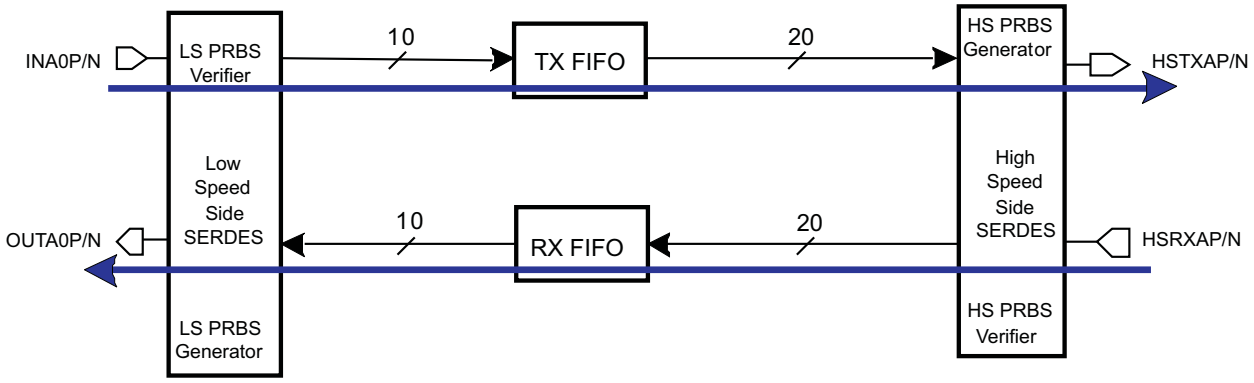

Figure 32. 1:1 Mode Transmit and Receive Data Paths

The 1:1 mode only uses lane 0 on the low-speed side and is enabled by setting TX_MODE_SEL and RX_MODE_SEL to 1 (1.13:12 = 2'b11) per channel. The maximum data rate supported in the 1:1 mode is 5Gbps. The minimum data rate supported is 1Gbps. LS_OK_OUT_* status pin must be ignored. If needed for monitoring the link status, only PLL lock and LOS are relevant.

The latency measurement function is not supported in the 1:1 mode. In the 1:1 mode, the High-Speed Channel Sync (register F.10) and Low-Speed Lane 0 Channel Sync (register 15.8) are not part of their respective data paths.

In the 1:1 mode, the data path supports non-8B/10B encoded data, for example, PRBS.

In this mode, any registers related to lane 1, 2, or 3 are not used or do not apply. In addition, the following registers do not apply:

- 1.11:8
- 9.8:4
- C, D, 15(except 15.10), 16, 17, 18, 1D
- F.14, F.10, F.8, F.3:2

8.5 Programming

Registers for the TLK10002 can be addressed directly through MDIO Clause 22. Channel identification is based on PHY (Port) address field. Channel A can be accessed by setting LSB of PHY address to 0. Channel B can be accessed by setting LSB of PHY address to 1. Control registers 0x01 through 0x0E are specific to the channel addressed. Status registers 0x0F through 0x15, and 0x1D report the status of the channel addressed. The rest are global control or status registers and are channel independent.

NOTE

The N.x:y register numbering format is used in this document, where N is a hexadecimal register number, and x:y is a register bit number range in decimal format. For example, B.10:8 denotes bits 10, 9, and 8 of register address 0x0B.

8.5.1 Power Sequencing Guidelines

The TLK10002 allows either the core or I/O power supply to be powered up for an indefinite period of time while the other supply is not powered up, if all of the following conditions are met:

1. All maximum ratings and recommended operating conditions are followed.
2. Bus contention while 1.5-V or 1.8-V power is applied (> 0 V) must be limited to 100 hours over the projected lifetime of the device.
3. Junction temperature is less than 105°C during device operation. Note: Voltage stress up to the absolute maximum voltage values for up to 100 hours of lifetime operation at a junction temperature of 105°C or lower will minimally impact reliability.

The TLK10002 inputs are not failsafe (that is, cannot be driven with the I/O power disabled). TLK10002 inputs must not be driven high until their associated power supplies are active.

8.6 Register Maps

RW: Read-Write User can write 0 or 1 to this register bit. Reading this register bit returns the same value that has been written.

RW/SC: Read-Write Self-Clearing User can write 0 or 1 to this register bit. Writing a 1 to this register creates a high pulse. Reading this register bit always returns 0.

RO: Read-Only This register can only be read. Writing to this register bit has no effect. Reading from this register bit returns its current value.

RO/LH: Read-Only Latched High This register can only be read. Writing to this register bit has no effect. Reading a 1 from this register bit indicates that either the condition is occurring or it has occurred since the last time it was read. Reading a 0 from this register bit indicates that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched high register, when read high, must be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read low. If it is still occurring, the second read reads high. Reading this register bit automatically resets its value to 0.

RO/LL: Read-Only Latched Low This register can only be read. Writing to this register bit has no effect. Reading a 0 from this register bit indicates that either the condition is occurring or it has occurred since the last time it was read. Reading a 1 from this register bit indicates that the condition is not occurring presently, and it has not occurred because the last time the register was read. A latched low register, when read low, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read reads high. If it is still occurring, the second read reads low. Reading this register bit automatically sets its value to 1.

COR: Clear-On-Read This register can only be read. Writing to this register bit has no effect. Reading from this register bit returns its current value, then resets its value to 0.

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Register Maps (continued)

Table 9. GLOBAL_CONTROL_1 — Address: 0x00 Default: 0x0600

BIT(s)	NAME	DESCRIPTION	ACCESS
0.15	GLOBAL_RESET	Global reset (Channel A & B). 0 = Normal operation (Default 1'b0) 1 = Resets TX and RX datapath including MDIO registers. Equivalent to asserting RESET_N.	RW SC(1)
0.11	GLOBAL_WRITE	Global write enable. 0 = Control settings written to Registers 0x01-0x0E are specific to channel addressed (Default 1'b0) 1 = Control settings written to Registers 0x01-0x0E are applied to both Channel A and Channel B regardless of channel addressed	RW
0.10:8	RESERVED	For TI use only (Default 3'b110)	RW
0.7	RESERVED	For TI use only (Default 1'b0)	RW
0.3:0	PRBS_PASS_OVERLAY [3:0]	PRBS_PASS pin status selection. Applicable only when PRBS test pattern verification is enabled on HS side or LS side. PRBS_PASS pin reflects PRBS verification status on selected Channel HS/LS side 0000 = Status from Channel A HS SERDES side(Default 4'b0000) 0001 = Reserved 001x = Reserved 0100 = Status from Channel A LS SERDES side Lane 0 0101 = Status from Channel A LS SERDES side Lane 1 0110 = Status from Channel A LS SERDES side Lane 2 0111 = Status from Channel A LS SERDES side Lane 3 1000 = Status from Channel B HS SERDES side 1001 = Reserved 101x = Reserved 1100 = Status from Channel B LS SERDES side Lane 0 1101 = Status from Channel B LS SERDES side Lane 1 1110 = Status from Channel B LS SERDES side Lane 2 1111 = Status from Channel B LS SERDES side Lane 3	R/W

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 10. CHANNEL_CONTROL_1 — Address: 0x01 Default: 0x0300

BIT(s)	NAME	DESCRIPTION	ACCESS
1.15	POWERDOWN	Setting this bit high powers down entire data path with the exception that MDIO interface stays active. 0 = Normal operation (Default 1'b0) 1 = Power Down mode is enabled.	RW
1.13	RX_MODE_SEL	RX mode selection 0 = RX mode dependent upon RX_DEMUX_SEL (1.9) (Default 1'b0) 1 = Enables 1 to 1 mode on receive channel	RW
1. 12	TX_MODE_SEL	TX mode selection 0 = TX mode dependent upon TX_DEMUX_SEL (1.8) (Default 1'b0) 1 = Enables 1 to 1 mode on transmit channel	RW

Table 10. CHANNEL_CONTROL_1 — Address: 0x01 Default: 0x0300 (continued)

BIT(s)	NAME	DESCRIPTION	ACCESS
1.11:10	HS_CH_SYNC_ HYSTERESIS[1:0]	Channel synchronization hysteresis control on the HS receive channel. 00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the unsynchronized state (Default 2'b00) 01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to unsync 10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync 11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync	RW
1.9	RX_DEMUX_SEL	RX De-Mux selection control for lane de-serialization on receive channel. Valid only when RX_MODE_SEL (1.13) is LOW 0 = 1 to 2 1 = 1 to 4 (Default 1'b1)	RW
1. 8	TX_MUX_SEL	TX Mux selection control for lane serialization on transmit channel. Valid only when TX_MODE_SEL (1.12) is LOW 0 = 2 to 1 1 = 4 to 1 (Default 1'b1)	RW
1.7:4	CLKOUT_DIV[3:0]	Output clock divide setting. This value is used to divide selected clock (Selected using CLKOUT_SEL (1.3:2)) before giving it out onto CLKOUTxP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25 See Figure 13. Clocking Architecture	RW
1.3:2	CLKOUT_SEL[1:0]	Output clock select. Selected Recovered clock sent out on CLKOUTxP/N pins 00 = Selects Channel A HSRX recovered byte clock as output clock (Default 2'b00) 01 = Selects Channel B HSRX recovered byte clock as output clock 10 = Selects Channel A HSRX VCO divide by 2 clock as output clock 11 = Selects Channel B HSRX VCO divide by 2 clock as output clock See Figure 13. Clocking Architecture	RW
1.1	REFCLK_ SEL	Channel Reference clock selection. Applicable only when REFCLKx_SEL pin is LOW. 0 = Selects REFCLK_0_P/N as clock reference to Channel x (Default 1'b0) 1 = Selects REFCLK_1_P/N as clock reference to Channel x See Figure 13. Clocking Architecture	RW
1.0	RESERVED	For TI use only (Default 1'b0)	RW

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Table 11. HS_SERDES_CONTROL_1 — Address: 0x02 Default: 0x811D

BIT(s)	NAME	DESCRIPTION	ACCESS
2.15:10	RESERVED	For TI use only (Default 6'b100000)	RW
2.9:8	HS_LOOP_BANDWIDTH[1:0]	HS SERDES PLL Loop Bandwidth settings 00 = Reserved 01 = Applicable when external JC_PLL is NOT used (Default 2'b01) 10 = Applicable when external JC_PLL is used 11 = Reserved	RW
2.7	RESERVED	For TI use only (Default 1'b0)	RW
2.6	HS_VRANGE	HS SERDES PLL VCO range selection. This bit needs to be set HIGH if VCO frequency (REFCLK * HS_PLL_MULT) is below 2.5GHz 0 = VCO runs at higher end of frequency range (Default 1'b0) 1 = VCO runs at lower end of frequency range	RW
2.5	RESERVED	For TI use only (Default 1'b0)	RW
2.4	HS_ENPLL	HS SERDES PLL enable control. HS SERDES PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables PLL in HS SERDES 1 = Enables PLL in HS SERDES (Default 1'b1)	RW
2.3:0	HS_PLL_MULT[3:0]	HS SERDES PLL multiplier setting (Default 4'b1101). Refer to Table 12 See *Line Rate, SERDES PLL Settings, and Reference Clock Selection* for more information on PLL multiplier settings	RW

Table 12. High-Speed Side SERDES PLL Multiplier Control

2.3:0		2.3:0	
VALUE	PLL MULTIPLIER FACTOR	VALUE	PLL MULTIPLIER FACTOR
0000	Reserved	1000	12x
0001	Reserved	1001	12.5x
0010	4x	1010	15x
0011	5x	1011	16x
0100	6x	1100	16.5x
0101	8x	1101	20x
0110	8.25x	1110	25x
0111	10x	1111	Reserved

Table 13. HS_ SERDES_CONTROL_2 — Address: 0x03 Default: 0xA444

BIT(s)	NAME	DESCRIPTION	ACCESS
3.15:12	HS_SWING[3:0]	Transmitter Output swing control for HS SERDES. (Default 4'b1010) Refer to Table 14	RW
3.11	RESERVED	For TI use only (Default 1'b0)	RW
3.10	HS_ENTX	HS SERDES transmitter enable control. HS SERDES transmitter is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables HS SERDES transmitter 1 = Enables HS SERDES transmitter (Default 1'b1)	RW
3.9:8	HS_RATE_TX [1:0]	HS SERDES TX rate settings 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Eighth rate	RW

Table 13. HS_ SERDES_CONTROL_2 — Address: 0x03 Default: 0xA444 (continued)

BIT(s)	NAME	DESCRIPTION	ACCESS
3.7:6	HS_AGCCTRL[1:0]	Adaptive gain control loop 00 = Attenuator will not change after lock has been achieved, even if AGC becomes unlocked 01 = Attenuator will not change when in lock state, but could change when AGC becomes unlocked (Default 2'b01) 10 = Force the attenuator off. 11 = Force the attenuator on	RW
3.5:4	HS_AZCAL[1:0]	Auto zero calibration. 00 = Auto zero calibration initiated when receiver is enabled (Default 2'b00) 01 = Auto zero calibration disabled 10 = Forced with automatic update. 11 = Forced without automatic update	RW
3.3	HS_ENUNSD	0 = Disable use of unscrambled data in HS Serdes Rx (Recommended setting for Full Rate) (Default 1'b0) 1 = Enable use of unscrambled data in HS Serdes Rx (Recommended setting for Half, Quarter and Eighth Rates)	RW
3.2	HS_ENRX	HS SERDES receiver enable control. HS SERDES receiver is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables HS SERDES receiver 1 = Enables HS SERDES receiver (Default 1'b1)	RW
3.1:0	HS_RATE_RX [1:0]	HS SERDES RX rate settings 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Eighth rate	RW

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Table 14. High-Speed Side SERDES AC Mode Output Swing Control

VALUE [15:12]	AC MODE TYPICAL AMPLITUDE (mVdfpp)
0000	130
0001	220
0010	300
0011	390
0100	480
0101	570
0110	660
0111	750
1000	830
1001	930
1010	1020
1011	1110
1100	1180
1101	1270
1110	1340
1111	1400

Table 15. HS_ SERDES_CONTROL_3 — Address: 0x04 Default: 0xB820

BIT(s)	NAME	DESCRIPTION	ACCESS
4.15	HS_ENTRACK	HSRX ADC Track mode 0 = Normal operation 1 = Forces ADC into track mode (Default 1'b1)	RW
4.14:12	HS_EQPRE[2:0]	SERDES Rx precursor equalizer selection 000 = 1/9 cursor amplitude 001 = 3/9 cursor amplitude 010 = 5/9 cursor amplitude 011 = 7/9 cursor amplitude (Default 3'b011) 100 = 9/9 cursor amplitude 101 = 11/9 cursor amplitude 110 = 13/9 cursor amplitude 111 = Disable	RW
4.11:10	HS_CDRFMULT[1:0]	Clock data recovery algorithm frequency multiplication selection 00 = First order. Frequency offset tracking disabled 01 = Second order. 1x mode 10 = Second order. 2x mode (Default 2'b10) 11 = Reserved	RW
4.9:8	HS_CDRTHR[1:0]	Clock data recovery algorithm threshold selection 00 = Four vote threshold (Default 2'b00) 01 = Eight vote threshold 10 = Sixteen vote threshold 11 = Thirty two vote threshold	RW
4.7	HS_EQLIM	HSRX Equalizer limit control 0 = Normal operation (Default 1'b0) 1 = Limits equalizer DFE tap weights	RW
4.6	HS_EQHLD	HSRX Equalizer hold control 0 = Normal operation (Default 1'b0) 1 = Holds equalizer and long tail correction in their current state	RW
4.5	HS_H1CDRMODE	0 = CDR locks to h(-1) 1 = CDR locks to h(+1)	RW
4.4:0	HS_TWCRF[4:0]	Cursor Reduction Factor (Default 5'b00000) Refer to Table 16	RW

Table 16. High-Speed Side SERDES Cursor Reduction Factor Weights

4.4:0		4.4:0	
VALUE	CURSOR REDUCTION (%)	VALUE	CURSOR REDUCTION (%)
00000	0	10000	17
00001	2.5	10001	20
00010	5.0	10010	22
00011	7.5	10011	25
00100	10.0	10100	27
00101	12	10101	30
00110	15	10110	32
00111	Reserved	10111	35
01000		11000	37
01001		11001	40
01010		11010	42
01011		11011	45
01100		11100	47
01101		11101	50
01110		11110	52
01111		11111	55

Table 17. HS_ SERDES_CONTROL_4— Address: 0x05 Default: 0x2000

BIT(s)	NAME	DESCRIPTION	ACCESS
5.15	HS_RX_INVPAIR	Receiver polarity. 0 = Normal polarity. HSRXxP considered positive data. HSRXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSRXxP considered negative data. HSRXxN considered positive data	RW
5.14	HS_TX_INVPAIR	Transmitter polarity. 0 = Normal polarity. HSTXxP considered positive data and HSTXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSTXxP considered negative data and HSTXxN considered positive data	RW
5.13	HS_FIRUPT	HS SERDES Tx pre/post cursor filter update control 0 = Holds last state; any changes to TWCRF, TWPRE, TWPOST1/2 will not take effect until FIRUPT goes high. 1 = Pre/Post cursor fields can be updated by changing respective fields (Default 1'b1)	RW
5.12:8	HS_TWPOST1[4:0]	Adjacent post cursor1 Tap weight. Selects TAP settings for TX waveform. (Default 5'b00000) Refer to Table 18	RW
5.7:4	HS_TWPRE[3:0]	Precursor Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000) Refer to Table 20	RW
5.3:0	HS_TWPOST2[3:0]	Adjacent post cursor2 Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000) Refer to Table 19	RW

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Table 18. High-Speed Side SERDES Post-Cursor1 Transmit Tap Weights

5.12:8		5.12:8	
VALUE	TAP WEIGHT (%)	VALUE	TAP WEIGHT (%)
00000	0	10000	0
00001	+2.5	10001	–2.5
00010	+5.0	10010	–5.0
00011	+7.5	10011	–7.5
00100	+10.0	10100	–10.0
00101	+12.5	10101	–12.5
00110	+15.0	10110	–15.0
00111	+17.5	10111	–17.5
01000	+20.0	11000	–20.0
01001	+22.5	11001	–22.5
01010	+25.0	11010	–25.0
01011	+27.5	11011	–27.5
01100	+30.0	11100	–30.0
01101	+32.5	11101	–32.5
01110	+35.0	11110	–35.0
01111	+37.5	11111	–37.5

Table 19. High-Speed Side SERDES Post-Cursor2 Transmit Tap Weights

5.3:0		5.3:0	
VALUE	TAP WEIGHT (%)	VALUE	TAP WEIGHT (%)
0000	0	1000	0
0001	+2.5	1001	–2.5
0010	+5.0	1010	–5.0
0011	+7.5	1011	–7.5
0100	+10.0	1100	–10.0
0101	+12.5	1101	–12.5
0110	+15.0	1110	–15.0
0111	+17.5	1111	–17.5

Table 20. High-Speed Side SERDES Pre-Cursor Transmit Tap Weights

5.7:4		5.7:4	
VALUE	TAP WEIGHT (%)	VALUE	TAP WEIGHT (%)
0000	0	1000	0
0001	+2.5	1001	–2.5
0010	+5.0	1010	–5.0
0011	+7.5	1011	–7.5
0100	+10.0	1100	–10.0
0101	+12.5	1101	–12.5
0110	+15.0	1110	–15.0
0111	+17.5	1111	–17.5

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Table 21. LS_ SERDES_CONTROL_1 — Address: 0x06 Default: 0xF115

BIT(s)	NAME	DESCRIPTION	ACCESS
6.15:12	LS_LN_CFG_EN[3:0]	Configuration control for LS SERDES Lane settings (Default 4'b1111) [3] corresponds to LN3, [2] corresponds to LN2 [1] corresponds to LN1, [0] corresponds to LN0 0 = Writes to LS_SERDES_CONTROL_2 (register 0x07) and LS_SERDES_CONTROL_3 (register 0x08) control registers do not affect respective LS SERDES lane 1 = Writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 control registers affect respective LS SERDES lane For example, if subsequent writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 registers need to affect the settings in Lanes 0 and 1, LS_LN_CFG_EN[3:0] should be set to 4'b0011 Read values in LS_SERDES_CONTROL_2 & LS_SERDES_CONTROL_3 reflect the settings value for Lane selected through LS_LN_CFG_EN[3:0]. To read settings for Lane 0, LS_LN_CFG_EN[3:0] should be set to 4'b0001 To read settings for Lane 1, LS_LN_CFG_EN[3:0] should be set to 4'b0010 To read settings for Lane 2, LS_LN_CFG_EN[3:0] should be set to 4'b0100 To read settings for Lane 3, LS_LN_CFG_EN[3:0] should be set to 4'b1000 Read values of LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 registers are not valid for any other LS_LN_CFG_EN[3:0] combination	RW
6.11:10	RESERVED	For TI use only(Default 2'b00)	RW
6.9:8	LS_LOOP_BANDWIDTH[1:0]	LS SERDES PLL Loop Bandwidth settings 00 = Reserved 01 = Applicable when external JC_PLL is NOT used (Default 2'b01) 10 = Applicable when external JC_PLL is used 11 = Reserved	RW
6.7	DEEP_REMOTE_LPBK_CTRL	Deep remote loopback control. Works in conjunction with DEEP_REMOTE_LPBK(B:3). Requires setting of LS_TX_ENTEST(8.3) and LS_RX_ENTEST(8.2) for desired lane on the LS side (default 1'b0). 00= Deep Remote Loopback Disabled 01= Deep Remote Loopback through pad. The loopback path includes the transmit CML driver and receive sense amps. The link partner connected through INA*P/N or INB*P/N pins must be electrically idle at differential zero with P and N signals at the same voltage. 10= Deep Remote Loopback with CML Driver Disabled. The loopback path is fully digital and excludes the transmit CML driver and receive sense amps. If monitoring OUT* pins is not required, this mode can save power. 11= Deep Remote Loopback with CML Driver Enabled. As above, but the CML driver operates normally.	RW
6.6:5	RESERVED	For TI use only (Default 2'b00)	RW
6.4	LS_ENPLL	LS SERDES PLL enable control. LS SERDES PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables PLL in LS SERDES 1 = Enables PLL in LS SERDES (Default 1'b1)	RW
6.3:0	LS_MPY[3:0]	LS SERDES PLL multiplier setting (Default 4'b0101). Refer to Table 22 See *Line Rate, SERDES PLL Settings, and Reference Clock Selection* for more information on PLL multiplier settings	RW

Table 22. Low-Speed Side SERDES PLL Multiplier Control

6.3:0		6.3:0	
VALUE	PLL MULTIPLIER FACTOR	VALUE	PLL MULTIPLIER FACTOR
0000	4x	1000	15x
0001	5x	1001	20x
0010	6x	1010	25x
0011	Reserved	1011	Reserved
0100	8x	1100	Reserved

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Table 22. Low-Speed Side SERDES PLL Multiplier Control (continued)

6.3:0		6.3:0	
VALUE	PLL MULTIPLIER FACTOR	VALUE	PLL MULTIPLIER FACTOR
0101	10x	1101	50x
0110	12x	1110	65x
0111	12.5x	1111	Reserved

Table 23. LS_ SERDES_CONTROL_2 — Address: 0x07 Default: 0xDC04

BIT(s)	NAME	DESCRIPTION	ACCESS
7.15	RESERVED	For TI use only. (Default 1'b1)	RW
7.14:12	LS_SWING[2:0]	Output swing control on LS SERDES side. (Default 3'b101) Refer to Table 24.	RW
7.11	LS_LOS	LS SERDES LOS detector control 0 = Disable Loss of signal detection on LS SERDES lane inputs 1 = Enable Loss of signal detection on LS SERDES lane inputs (Default 1'b1)	RW
7.10	LS_IN_EN	LS SERDES input enable control. LS SERDES per input lane is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. Input lanes 3 and 2 are automatically disabled when in 2 to 1 mode 0 = Disables LS SERDES lane 1 = Enables LS SERDES lane (Default 1'b1)	RW
7.9:8	LS_IN_RATE [1:0]	LS SERDES input lane rate settings 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Reserved	RW
7.7:4	LS_DE[3:0]	LS SERDES output de-emphasis settings. (Default 4'b0000) Refer to Table 25	RW
7.3	RESERVED	For TI use only . (Default 1'b0)	RW
7.2	LS_OUT_EN	LS SERDES output lane enable control. LS SERDES per output lane is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. Output lanes 3 and 2 are automatically disabled when in 1 to 2 mode. 0 = Disables LS SERDES lane 1 = Enables LS SERDES lane (Default 1'b1)	RW
7.1:0	LS_OUT_RATE [1:0]	LS SERDES output lane rate settings 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Reserved	RW

Table 24. Low-Speed Side SERDES AC Mode Output Swing Control

VALUE 7.14:12	AC MODE TYPICAL AMPLITUDE (mVdfpp)
000	190
001	380
010	560
011	710
100	850
101	950
110	1010
111	1050

Table 25. Low-Speed Side SERDES Output De-Emphasis

7.7:4			7.7:4		
VALUE	AMPLITUDE REDUCTION		VALUE	AMPLITUDE REDUCTION	
	(%)	dB		(%)	dB
0000	0	0	1000	38.08	4.16
0001	4.76	0.42	1001	42.85	4.86
0010	9.52	0.87	1010	47.61	5.61
0011	14.28	1.34	1011	52.38	6.44
0100	19.04	1.83	1100	57.14	7.35
0101	23.8	2.36	1101	61.9	8.38
0110	28.56	2.92	1110	66.66	9.54
0111	33.32	3.52	1111	71.42	10.87

Table 26. LS_ SERDES_CONTROL — Address: 0x08 Default: 0x0001

BIT(s)	NAME	DESCRIPTION	ACCESS
8.15	LS_OUT_INVPAIR	LS SERDES output lane polarity. (x = Channel A or B, y = Lane 0 or 1 or 2 or 3) 0 = Normal polarity. OUTxyP considered positive data. OUTxyN considered negative data (Default 1'b0) 1 = Inverted polarity. OUTxyP considered negative data. OUTxyN considered positive data	RW
8.14	LS_IN_INVPAIR	LS SERDES input lane polarity. (x = Channel A or B, y = Lane 0 or 1 or 2 or 3) 0 = Normal polarity. INxyP considered positive data and INxyN considered negative data (Default 1'b0) 1 = Inverted polarity. INxyP considered negative data and INxyP considered positive data	RW
8.13:12	RESERVED	For TI use only (Default 2'b00)	RW
8.11:8	LS_EQ[3:0]	LS SERDES Equalization control (Default 4'b0000). Refer to Table 27.	RW
8.7	RESERVED	For TI use only (Default 1'b0)	RW
8.6:4	LS_CDR[2:0]	LS SERDES CDR control (Default 3'b000) 000 – 1st Order. Threshold of 1 001 – 1st Order. Threshold of 17 010 – 2nd Order. High precision. Threshold of 1 011 – 2nd Order. High precision. Threshold of 17 100 – 1st Order. Low precision. Threshold of 1 101 – 2nd Order. Low precision. Threshold of 17 11x – Reserved	RW
8.3	LS_TX_ENTEST	LS SERDES test mode control on the channel input 0 = Normal operation (Default 1'b0) 1 = Enable test mode	RW

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Table 26. LS_ SERDES_CONTROL — Address: 0x08 Default: 0x0001 (continued)

BIT(s)	NAME	DESCRIPTION	ACCESS
8.2	LS_RX_ENTEST	LS SERDES test mode control on the channel output 0 = Normal operation (Default 1'b0) 1 = Enable test mode	RW
8.1:0	RESERVED	For TI use only (Default 2'b01)	RW

Table 27. Low-Speed Side SERDES Equalization

8.11:8			8.11:8		
VALUE	LOW FREQ GAIN	ZERO FREQ	VALUE	LOW FREQ GAIN	ZERO FREQ
0000	Maximum		1000	Adaptive	365 MHz
0001	Adaptive		1001		275 MHz
0010	Reserved		1010		195 MHz
0011			1011		140 MHz
0100			1100		105 MHz
0101			1101		75 MHz
0110			1110		55 MHz
0111			1111		50 MHz

Table 28. HS_OVERLAY_CONTROL — Address: 0x09 Default: 0x0900

BIT(s)	NAME	DESCRIPTION	ACCESS
9.15:10	RESERVED	For TI use only. (Default 6'b000010)	RW
9.9	HS_PEAK_DISABLE	HS Serdes PEAK_DISABLE control 0 = Track-and-hold has peaking for bandwidth extension 1 = Track-and-hold is without peaking; has flat AC response	RW
9.8	HS_LOS_MASK	0 = HS SERDES LOS status is used to generate HS channel synchronization status. If HS SERDES indicates LOS, channel synchronization indicates synchronization is not achieved 1 = HS SERDES LOS status is not used to generate HS channel synchronization status (Default 1'b1)	RW
9.5	HS_CH_SYNC_OVERLAY	0 = LOSx pin does not reflect receive channel loss of channel synchronization status (Default 1'b0) 1 = Allows channel loss of synchronization to be reflected on LOSx pin	RW
9.4	HS_INVALID_CODE_OVERLAY	0 = LOSx pin does not reflect receive channel invalid code word error (Default 1'b0) 1 = Allows invalid code word error to be reflected on LOSx pin	RW
9.3	HS_AGCLOCK_OVERLAY	0 = LOSx pin does not reflect HS SERDES AGC unlock status (Default 1'b0) 1 = Allows HS SERDES AGC unlock status to be reflected on LOSx pin	RW
9.2	HS_AZDONE_OVERLAY	0 = LOSx pin does not reflect HS SERDES auto zero calibration not done status (Default 1'b0) 1 = Allows auto zero calibration not done status to be reflected on LOSx pin	RW
9.1	HS_PLL_LOCK_OVERLAY	0 = LOSx pin does not reflect loss of HS SERDES PLL lock status (Default 1'b0) 1 = Allows HS SERDES loss of PLL lock status to be reflected on LOSx pin	RW
9.0	HS_LOS_OVERLAY	0 = LOSx pin does not reflect HS SERDES Loss of signal condition (Default 1'b0) 1 = Allows HS SERDES Loss of signal condition to be reflected on LOSx pin	RW

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Table 29. LS_OVERLAY_CONTROL — Address: 0x0A Default: 0x4000

BIT(s)	NAME	DESCRIPTION	ACCESS
A.15:14	RESERVED	For TI use only	RW
A.13	BER_TIMER_CLK_EN	0 = Disable BER timer clock (Default 1'b0) 1 = Enable BER timer clock	RW
A.12	LS_PLL_LOCK_OVERLAY	0 = LOSx pin does not reflect loss of LS SERDES PLL lock status (Default 1'b0) 1 = Allows LS SERDES loss of PLL lock status to be reflected on LOSx pin	RW
A.11:8	LS_CH_SYNC_OVERLAY_LN[3:0]	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS SERDES lane loss of synchronization condition (Default 1'b0) 1 = Allows LS SERDES lane loss of synchronization condition to be reflected on LOSx pin	RW
A.7:4	LS_INVALID_CODE_OVERLAY_LN[3:0]	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS SERDES lane invalid code condition (Default 1'b0) 1 = Allows LS SERDES lane invalid code condition to be reflected on LOSx pin	RW
A.3:0	LS_LOS_OVERLAY_LN[3:0	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS SERDES lane Loss of signal condition (Default 1'b0) 1 = Allows LS SERDES lane Loss of signal condition to be reflected on LOSx pin	RW

Table 30. LOOPBACK_TP_CONTROL — Address: 0x0B Default: 0x0700

BIT(s)	NAME	DESCRIPTION	ACCESS
B.15:14	RESERVED	For TI use only	RW
B.13	HS_TP_GEN_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits B.10:8	RW
B.12	HS_TP_VERIFY_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern verification selected by bits B.10:8	RW
B.10:8	HS_TEST_PATT_SEL[2:0]	Test Pattern Selection. Note that for CRPAT, TPsync must be high to be valid. See MDIO bit F.15 in Table 34. 000 = High Frequency Test Pattern 001 = Low Frequency Test Pattern 010 = Mixed Frequency Test Pattern 011 = CRPAT Short 100 = CRPAT Long 101 = 2^7 - 1 PRBS pattern 110 = 2^{23} - 1 PRBS pattern 111 = 2^{31} - 1 PRBS pattern (Default 3'b111) Errors can be checked by reading HS_ERROR_COUNTER register (0x10)	RW
B.7	LS_TP_GEN_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits B.5:4 on the LS side Requires setting of LS_RX_ENTEST (8.2) for desired lane on the LS side	RW
B.6	LS_TP_VERIFY_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern verification selected by bits B.5:4 on the LS side Requires setting of LS_TX_ENTEST (8.3) for desired lane on the LS side	RW

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Table 30. LOOPBACK_TP_CONTROL — Address: 0x0B Default: 0x0700 (continued)

BIT(s)	NAME	DESCRIPTION	ACCESS
B.5:4	LS_TEST_PATT_SEL[1:0]	Test Pattern Selection 00 = 2^{31} - 1 PRBS pattern (Default 2'b00) 01 = Alternating 0/1 pattern with a period of 2 UI (LS side bit UI) 10 = 2^{7} - 1 PRBS pattern 11 = 2^{23} - 1 PRBS pattern	RW
B.3	DEEP_REMOTE_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable deep remote loopback mode Requires setting of LS_TX_ENTEST(8.3) and LS_RX_ENTEST (8.2) for desired lane on the LS side. See Figure 14 and MDIO bit 6.7 for additional controls.	RW
B.2	SHALLOW_REMOTE_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable shallow remote loopback mode/serial retime mode See Figure 15	RW
B.1	DEEP_LOCAL_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable deep remote loopback mode See Figure 16	RW
B.0	SHALLOW_LOCAL_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable shallow local loopback mode See Figure 17	RW

Table 31. LAS_CONFIG_CONTROL — Address: 0x0C Default: 0x03F0

BIT(s)	NAME	DESCRIPTION	ACCESS
C.15:14	RESERVED	For TI use only. (Default 2'b0)	RW
C.13:12	LAS_STATUS_CFG[1:0]	Selects selected lane status to be reflected in LAS_STATUS_1 register (0x15) 00 = Lane 0 (Default 2'b00) 01 = Lane 1 10 = Lane 2 11 = Lane 3	RW
C.11:10	LAS_CH_SYNC_HYS_SEL[1:0]	Lane alignment slave Channel synchronization hysteresis selection 00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the LOS state (Default 2'b00) 01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to LOS 10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS 11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS	RW
C.9:8	LAS_LA_COL_CFG[1:0]	Minimum distance between align character in Lane alignment slave 00 = 8 01 = 16 1x = 24 (Default 2'b11)	RW
C.7	LS_DECODE_ERR_MASK	0 = LS side decode errors of enabled lanes are used to generate link status if error rate exceeds threshold. Valid only when hardware BER function is enabled by setting A.13 to 1'b1. 1 = LS side decode errors of any lane are not used to generate link status (Default 1'b1)	RW
C.6	RESERVED	For TI use only.	RW
C.5	LS_LOS_MASK	0 = LS SERDES LOS status of enabled lanes is used to generate link status 1 = LS SERDES LOS status of enabled lanes is not used to generate link status (Default 1'b1)	RW

Table 31. LAS_CONFIG_CONTROL — Address: 0x0C Default: 0x03F0 (continued)

BIT(s)	NAME	DESCRIPTION	ACCESS
C.4	LS_PLL_LOCK_MASK	0 = LS SERDES PLL Lock status is used to generate link status 1 = LS SERDES PLL Lock status is not used to generate link status (Default 1'b1)	RW
C.2	FORCE_LM_REALIGN	0 = Normal operation (Default 1'b0) 1 = Force lane realignment in Link status monitor	RW SC(1)
C.1:0	LAS_BER_THRESH[1:0]	Threshold setting for 8b/10b error rate checking. Valid only when hardware BER function is enabled by setting A.13 to 1'b1. 00 = Link Ok if <1 error when timer expires (Default 2'b00) 01 = Link Ok if <15 error when timer expires 10 = Link Ok if <127 error when timer expires 11 = Link Ok if <1023 error when timer expires	RW

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 32. LAS_BER_TMER_CONTROL — Address: 0x0D Default: 0xFFFF

BIT(s)	NAME	DESCRIPTION	ACCESS
D.15:0	LAS_BER_TIMER[15:0]	16 bit value to configure 8b/10b error rate checking on the link monitor (Default 16'hFFFF). Valid only when hardware BER function is enabled by setting A.13 to 1'b1.	RW

Table 33. RESET_CONTROL — Address: 0x0E Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
E.3	DATAPATH_RESET	Channel datapath reset control. Required once the desired functional mode is configured. 0 = Normal operation. (Default 1'b0) 1 = Resets channel logic excluding MDIO registers. (Resets both Tx and Rx datapath)	RW SC(1)
E.2	TXFIFO_RESET	Transmit FIFO reset control 0 = Normal operation. (Default 1'b0) 1 = Resets transmit datapath FIFO.	RW SC(1)
E.1	RXFIFO_RESET	Receive FIFO reset control 0 = Normal operation. (Default 1'b0) 1 = Resets receive datapath FIFO.	RW SC(1)

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 34. CHANNEL_STATUS_1 — Address: 0x0F Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
F.15	HS_TP_ STATUS	Test Pattern status for High/Low/Medium/CRPAT test patterns 0 = Alignment has not achieved 1 = Alignment has been determined and correct pattern has been received. Any bit errors are reflected in HS_ERROR_COUNTER register (0x10)	RO
F.14	LA_SLAVE_STATUS	Lane alignment slave status 0 = Lane alignment is not achieved on the slave side 1 = Lane alignment is achieved on the slave side	RO/LL
F.13	HS_LOS	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on HS serial receive inputs	RO/LH
F.12	HS_AZ_DONE	Auto zero complete indicator. When high, indicates auto zero calibration is complete	RO/LL
F.11	HS_AGC_LOCKED	Adaptive gain control loop lock indicator. When high, indicates AGC loop is in locked state	RO/LL
F.10	HS_CHANNEL_SYNC	Channel synchronization status indicator. When high, indicates channel synchronization has achieved	RO/LL

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Table 34. CHANNEL_STATUS_1 — Address: 0x0F Default: 0x0000 (continued)

BIT(s)	NAME	DESCRIPTION	ACCESS
F.9	RESERVED	For TI use only. (Default 1'b0).	RO/LH
F.8	HS_DECODE_INVALID	Valid when decoder is enabled and during CRPAT test pattern verification. When high, indicates decoder received an invalid code word, or a 8b/10b disparity error. In functional mode, number of DECODE_INVALID errors are reflected in HS_ERROR_COUNTER register (0x10)	RO/LH
F.7	TX_FIFO_UNDERFLOW	When high, indicates underflow has occurred in the transmit datapath FIFO.	RO/LH
F.6	TX_FIFO_OVERFLOW	When high, indicates overflow has occurred in the transmit datapath FIFO.	RO/LH
F.5	RX_FIFO_UNDERFLOW	When high, indicates underflow has occurred in the receive datapath FIFO.	RO/LH
F.4	RX_FIFO_OVERFLOW	When high, indicates overflow has occurred in the receive datapath FIFO.	RO/LH
F.3	RX_LS_OK	Receive link status indicator from LS side. When high, indicates receive link status is achieved on the LS side	RO/LL
F.2	TX_LS_OK	Link status indicator from Link training slave inside TLK10002 When high, indicates Link training slave has achieved sync and alignment	RO/LL
F.1	LS_PLL_LOCK	LS SERDES PLL lock indicator When high, indicates LS SERDES PLL is locked to the selected incoming REFCLK0/1_P/N	RO/LL
F.0	HS_PLL_LOCK	HS SERDES PLL lock indicator When high, indicates HS SERDES PLL is locked to the selected incoming REFCLK0/1_P/N	RO/LL

Table 35. HS_ERROR_COUNTER — Address: 0x10 Default: 0xFFFD

BIT(s)	NAME	DESCRIPTION	ACCESS
10.15:0	HS_ERR_COUNT [15:0]	In functional mode, this counter reflects number of invalid code words (including disparity errors) received by decoder. In HS test pattern verification mode, this counter reflects error count for the test pattern selected through B.10:8 When PRBSEN pin is set, this counter reflects error count for selected PRBS pattern. Counter value cleared to 16'h0000 when read.	COR

Table 36. LS_LN0_ERROR_COUNTER — Address: 0x11 Default: 0xFFFD

BIT(s)	NAME	DESCRIPTION	ACCESS
11.15:0	LS_LN0_ERR_COUNT [15:0]	Lane 0 Error counter In functional mode, this counter reflects number of invalid code words (including disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode, this counter reflects error count for the test pattern selected through B.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 37. LS_LN1_ERROR_COUNTER — Address: 0x12 Default: 0xFFFD

BIT(s)	NAME	DESCRIPTION	ACCESS
12.15:0	LS_LN1_ERR_COUNT [15:0]	Lane 1 Error counter In functional mode, this counter reflects number of invalid code words (including disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode, this counter reflects error count for the test pattern selected through B.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 38. LS_LN2_ERROR_COUNTER — Address: 0x13 Default: 0xFFFD

BIT(s)	NAME	DESCRIPTION	ACCESS
13.15:0	LS_LN2_ERR_COUNT [15:0]	Lane 2 Error counter In functional mode, this counter reflects number of invalid code words (including disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode, this counter reflects error count for the test pattern selected through B.5:4 Counter value cleared to 16'h0000 when read.	COR

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Table 39. LS_LN3_ERROR_COUNTER — Address: 0x14 Default: 0xFFFD

BIT(s)	NAME	DESCRIPTION	ACCESS
14.15:0	LS_LN3_ERR_COUNT [15:0]	Lane 3 Error counter In functional mode, this counter reflects number of invalid code words (including disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode, this counter reflects error count for the test pattern selected through B.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 40. LAS_STATUS_1 — Address: 0x15 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
15.15	LAS_LN_ALIGN_FIFO_ERR	LAS Lane alignment FIFO error status 0 = FIFO error not detected 1 = FIFO error detected	RO/LH
15.14:12	RESERVED	For TI use only	RO
15.11	LAM_ ALIGN_SEQ_ST	LAM Lane align sequence state 0 = Sending normal traffic 1 = Sending lane align sequence	RO
15.10	LS_LOS	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on LS serial receive inputs for selected lane. Lane can be selected through LAS_STATUS_CFG[1:0] (register C.13:12)	RO/LH
15.9	RESERVED	For TI use only. (Default 1'b0).	RO/LL
15.8	LAS_CH_SYNC_STATUS	LAS Channel sync status for selected lane. Lane can be selected through LAS_STATUS_CFG[1:0] (register C.13:12)	RO/LL
15.6:4	RESERVED	For TI use only. (Default 2'b000).	RO
15.3	LAS_INVALID_DECODE	LAS Invalid decode error for selected lane. Lane can be selected through LAS_STATUS_CFG[1:0] (register C.13:12). Error count for each lane can also be monitored through respective LS_LNx_ERROR_COUNTER registers (0x11, 0x12, 0x13, and 0x14)	RO/LH
15.2:0	RESERVED	For TI use only. (Default 2'b000).	RO

Table 41. LATENCY_MEASURE_CONTROL — Address: 0x16 Default: 0x7F00

BIT(s)	NAME	DESCRIPTION	ACCESS
16.15:8	RESERVED	For TI use only (Default 8'b11111111)	RW
16.7	LATENCY_MEAS_START_SEL	Latency measurement start point selection 0 = Selects LS TX as start point (Default 1'b0) 1 = Selects HS RX as start point	RW
16.6	LATENCY_MEAS_STOP_SEL	Latency measurement stop point selection 0 = Selects LS RX as stop point (Default 1'b0) 1 = Selects HS TX as stop point	RW
16.5:4	LATENCY_MEAS_CLK_DIV[1:0]	Latency measurement clock divide control. Valid only when bit 16.2 is 0. Divides clock to needed resolution. Higher the divide value, lesser the latency measurement resolution. In choosing a divider, note that the frequency of the divided clock should not be slower than the internal high speed byte clock. 00 = Divide by 1 (Default 2'b00) (Most Accurate Measurement) 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8 (Longest Measurement Capability) See Table 8	RW
16.2	LATENCY_MEAS_CLK_SEL	Latency measurement clock selection. 0 = Selects clock listed in Table 8. Bits 16.5:4 can be used to divide this clock to achieve needed resolution. (Default 1'b0) 1 = Selects respective channel recovered byte clock (Frequency = Serial bit rate/ 20).	RW

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Table 41. LATENCY_MEASURE_CONTROL — Address: 0x16 Default: 0x7F00 (continued)

BIT(s)	NAME	DESCRIPTION	ACCESS
16.1	LATENCY_MEAS_EN	Latency measurement enable 0 = Disable Latency measurement (Default 1'b0) 1 = Enable Latency measurement	RW
16.0	LATENCY_MEAS_CH_SEL	Latency measurement channel selection 0 = Selects Latency measurement for channel A (Default 1'b0) 1 = Selects Latency measurement for channel B	RW

Table 42. LATENCY_COUNTER_2 — Address: 0x17 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
17.15:12	LATENCY_MEAS_START_COMMA[3:0]	Latency measurement start comma location status. 1 indicates comma found at the start location. If LS TX is selected as start point (16.7 = 0), [3:0] indicates status for lane3, lane2, lane1, lane0. If HS RX is selected as start point (16.7 = 1), [0] indicates status for data[9:0], [1] indicates status for data[19:10]. [3:2] is unused.	RO/LH (1)
17.11:8	LATENCY_MEAS_STOP_COMMA[3:0]	Latency measurement stop comma location status. 1 indicates comma found at the stop location. If LS RX is selected as stop point (16.6 = 0), [3:0] indicates status for lane3, lane2, lane1, lane0. If HS TX is selected as stop point (16.6 = 1), [0] indicates status for data[9:0], [1] indicates status for data[19:10]. [3:2] is unused.	RO/LH (1)
17.4	LATENCY_ MEAS_READY	Latency measurement ready indicator 0 = Indicates latency measurement not complete. 1 = Indicates latency measurement is complete and value in latency measurement counter (LATENCY_MEAS_COUNT[19:0]) (in registers 17.3:0 and 18.15:0) is ready to be read.	RO/LH (1)
17.3:0	LATENCY_MEAS_COUNT[19:16]	Bits[19:16] of 20 bit wide latency measurement counter. Latency measurement counter value represents the latency in number of clock cycles. This counter will return 20'h00000 if it is read before a comma is received at the stop point. If latency is more than 20'hFFFFF clock cycles then this counter returns 20'hFFFFF.	COR (1)

(1) User has to make sure Register 0x17 has to be read first before reading Register 0x18. Latency measurement counter value resets to 20'h00000 when Register 0x18 is read. Start and Stop Comma (17.15:12 and 17.11:8) and count valid (17.4) bits are also cleared when Register 0x18 is read.

Table 43. LATENCY_COUNTER_1 — Address: 0x18 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
18.15:0	LATENCY_MEAS_COUNT[15:0]	Bits[15:0] of 20-bit wide latency measurement counter.	COR (1)

(1) User has to make sure Register 0x17 has to be read first before reading Register 0x18. Latency measurement counter value resets to 20'h00000 when Register 0x18 is read. Start and Stop Comma (17.15:12 and 17.11:8) and count valid (17.4) bits are also cleared when Register 0x18 is read.

Table 44. TI_RESERVED_CONTROL_1 — Address: 0x19 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
19.10	RESERVED	For TI use only. (Default 1'b0)	RW
19.9	RESERVED	For TI use only. (Default 1'b0)	RW
19.8	RESERVED	For TI use only. (Default 1'b0)	RW
19.6	RESERVED	For TI use only. (Default 1'b0)	RW
19.5:4	RESERVED	For TI use only. (Default 2'b00)	RW
19.3:0	RESERVED	For TI use only. (Default 4'b0000)	RW

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Table 45. TI_RESERVED_CONTROL_2 — Address: 0x1A Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
1A.15:0	RESERVED	For TI use only.	RW

Table 46. TI_RESERVED_STATUS_1 — Address: 0x1B Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
1B.15:0	RESERVED	For TI use only.	RO

Table 47. MISC_CONTROL_3 — Address: 0x1C Default: 0x3000

BIT(s)	NAME	DESCRIPTION	ACCESS
1C.15	RESERVED	For TI use only. (Default 1'b0)	RW
1C.14	RESERVED	For TI use only. (Default 1'b0)	RW
1C.13	CLKOUT_B_EN	Output clock enable 0 = Holds CLKOUTBP/N output to a fixed value 1 = Allows CLKOUTBP/N output to toggle normally (Default 1'b1)	RW
1C.12	CLKOUT_A_EN	Output clock enable 0 = Holds CLKOUTAP/N output to a fixed value 1 = Allows CLKOUTAP/N output to toggle normally (Default 1'b1)	RW
1C.9:0	RESERVED	For TI use only. (Default 10'b0000000000)	RW

Table 48. LAS_STATUS_2 — Address: 0x1D Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
1D.15:12	LAS_LN3_ALIGN_PTR[3:0]	LAS Lane align FIFO character location for lane 3.	RO
1D.11:8	LAS_LN2_ALIGN_PTR[3:0]	LAS Lane align FIFO character location for lane 2.	RO
1D.7:4	LAS_LN1_ALIGN_PTR[3:0]	LAS Lane align FIFO character location for lane 1.	RO
1D.3:0	LAS_LN0_ALIGN_PTR[3:0]	LAS Lane align FIFO character location for lane 0.	RO

Table 49. EXT_ADDRESS_CONTROL — Address: 0x1E Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
1E.15:0	EXT_ADDR_CONTROL[15:0]	This register must be written with the extended register address to be written/read. Contents of address written in this register can be accessed from Register 0x1F. (Default 4'h0000)	RW

Table 50. EXT_ADDRESS_DATA — Address: 0x1F Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
1F.15:0	EXT_ADDR_DATA[15:0]	This register contains the data associated with the register address written in Register 0x1E	RO

Table 51. TI_ RESERVED_STATUS_2 — Address: 0x8000 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
8000.15:0	RESERVED	For TI use only.	RO

Table 52. TI_RESERVED_STATUS_3 — Address: 0x8001 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
8001.15:0	RESERVED	For TI use only.	RO

Table 53. TI_RESERVED_STATUS_4 — Address: 0x8002 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
8002.15:0	RESERVED	For TI use only.	RO

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Table 54. TI_RESERVED_STATUS_5 — Address: 0x8003 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
8003.15:0	RESERVED	For TI use only.	RO

Table 55. TI_RESERVED_STATUS_6 — Address: 0x8004 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
8004.15:0	RESERVED	For TI use only.	RO

Table 56. TI_RESERVED_STATUS_7 — Address: 0x8005 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
8005.15:0	RESERVED	For TI use only.	RO

Table 57. TI_RESERVED_STATUS_8 — Address: 0x8006 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
8006.15:0	RESERVED	For TI use only.	RO

Table 58. TI_RESERVED_STATUS_9 — Address: 0x8007 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
8007.15:0	RESERVED	For TI use only.	RO

Table 59. TI_RESERVED_STATUS_10 — Address: 0x8008 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
8008.15:0	RESERVED	For TI use only.	RO

Table 60. TI_RESERVED_STATUS_11 — Address: 0x8009 Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
8009.15:0	RESERVED	For TI use only.	RO

Table 61. TI_RESERVED_STATUS_12 — Address: 0x800A Default: 0x0000

BIT(s)	NAME	DESCRIPTION	ACCESS
800A.15:0	RESERVED	For TI use only.	RO

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLK10002 device can be used to support 10-Gbps data transmission over a backplane, for example, between a network processor or MAC and switch ASIC located on separate cards within a router chassis. A block diagram of this application is shown in Figure 33.

9.2 Typical Application

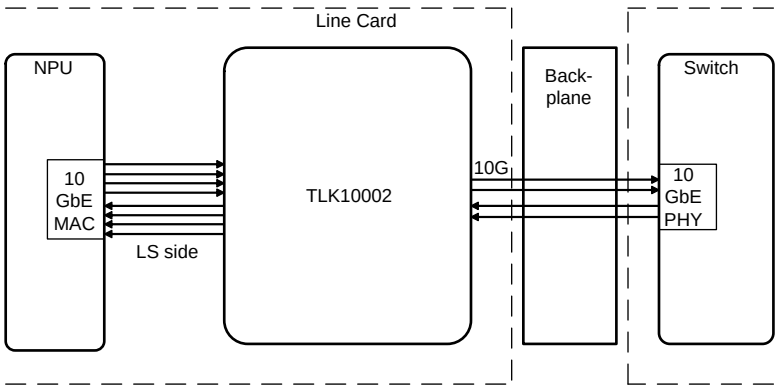

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Figure 33. Typical Application Circuit

9.2.1 Design Requirements

Table 62 lists the design parameters of this example.

Table 62. Design Parameters

PARAMETER	VALUE
Signaling	9.8304 Gbps
Encoding	8b/10b
REFCLK	122.88 MHz
AC-coupling caps	0.1 µF
Swing	1260 mVpp
Total jitter (max)	0.298 UI

9.2.2 Detailed Design Procedure

The TLK10031 must be powered through a 1-V (nominal) supply on the VDDD, VDDA, DVDD, VDDT, and VPP rails, and by a 1.5-V or 1.8-V (nominal) supply on the VDDR and VDDO rails. The power supply accuracy must be 5% or better, and the user must be careful that resistive losses across the application PCB's power distribution network do not cause the voltage present at the TLK10002 BGA balls to be below specification. If a switched-mode power supply is used, take care to ensure low supply ripple.

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Table 63. Device Configuration

PARAMETER	VALUE
Mode	4:1
PRE	–5
POST1	–10
POST2	–7.5

9.2.3 Application Curve

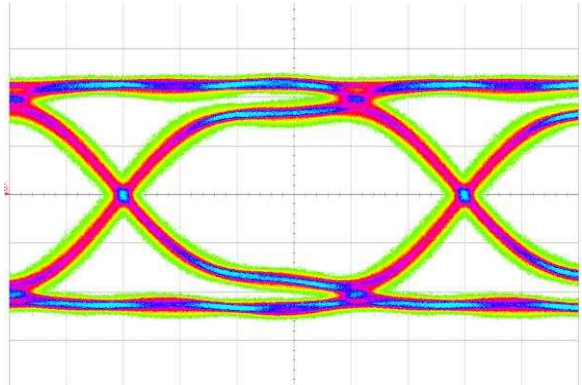

Figure 34. Clean TX Output from TLK10002

9.3 Initialization Setup

The following sequence must be performed to initialize and ensure proper operation of the TLK10002 device. This procedure is optimized for electrical connection on HS serial side.

9.3.1 4:1 Mode (9.8304 Gbps on HS Side, 2.4576 Gbps Per Lane on LS Side)

Note: Assume both channel A and channel B have the same setup.

REFCLK frequency = 122.88 MHz, Mode = Transceiver, 4 to 1 serialization on LS side inputs and 1 to 4 deserialization on HS side inputs.

- Device Pin Setting(s) – Pin settings allow for maximum software configurability.
  - Ensure PD_TRXA_N input pin is High.
  - Ensure PD_TRXB_N input pin is High.
  - Ensure PRBSEN input pin is Low.
  - Ensure REFCLKA_SEL input pin is Low to enable software control.
  - Ensure REFCLKB_SEL input pin is Low to enable software control.
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 µs -or- Write 1’b1 to 0.15 GLOBAL_RESET) after power supply stabilization.
- Enable MDIO global write so that each MDIO write affects both channels to shorten provisioning time
  - Write 1’b1 to 0.11 GLOBAL_WRITE
- Clock Configuration and Mode control
  - Write 1’b1 to 1.9 RX_DEMUX_SEL to select 1 to 4 on the receive side
  - Write 1’b1 to 1.8 TX_MUX_SEL to select 4 to 1 on the transmit side
  - Select respective Channel SERDES REFCLK input (Default = REFCLK0P/N)
    - If REFCLK0P/N used – Write 1’b0 to 1.1 REFCLK_ SEL
    - If REFCLK1P/N used – Write 1’b1 to 1.1 REFCLK_ SEL
- HS/LS Data Rate Setting (Refer to Table 3 for more CPRI/OBSAI Rates)
  - Write 4’b1101 to 2.3:0 HS_PLL_MULT[3:0], write 2’b00 to 3.9:8 HS_RATE_RX[1:0], write 2’b00 to 3.1:0

Initialization Setup (continued)

HS_RATE_TX[1:0], to select FULL rate and 20x MPY on HS side (HS_SERDES_CONTROL_1 = 0x811D, HS_SERDES_CONTROL_2 = 0xA444).
  - Write 4'b0101 to 6.3:0 LS_MPY[3:0], write 2'b00 to 7.9:8 LS_IN_RATE[1:0], write 2'b00 to 7.1:0 LS_OUT_RATE [1:0], to select FULL rate and 10x MPY on LS side (LS_SERDES_CONTROL_1 = 0xF115, LS_SERDES_CONTROL_2 = 0xDC04).
- HS Serial Configuration Changed
  - Configure the following bits per the desired application:
    - 2.9:8 (HS_LOOP_BANDWIDTH[1:0]), 2.6 (HS_VRANGE)
    - 3.15:12 (HS_SWING[3:0]), 3.7:6 (HS_AGCCTRL[1:0])
    - 3.5:4 (HS_AZCAL[1:0]), 4.14:12 (HS_EQPRE[2:0])
    - 4.11:10 (HS_CDRFMULT[1:0]), 4.9:8 (HS_CDRTHR[1:0]), 4.5 (H1CDRMODE)
    - 4.4:0 (HS_TWCRF[4:0]), 5.12:8 (HS_TWPOST1[4:0])
    - 5.7:4 (HS_TWPRE[3:0]), 5.3:0 (HS_TWPOST2[3:0])
- LS Serial Configuration
  - Configure the following bits per the desired application:
    - 7.14:12 (LS_SWING[2:0]), 7.7:4 (LS_DE[3:0])
    - 8.11:8 (LS_EQ [3:0]), 8.6:4 (LS_CDR [2:0])
- Toggle HS_ENRX
  - Write 1'b0 to 3.2 (HS_SERDES_CONTROL_2 = 0xA440)
  - Write 1'b1 to 3.2 (HS_SERDES_CONTROL_2 = 0xA444)
- Wait 10ms
- Check SERDES PLL Status for Locked State
  - Poll F.1 LS_PLL_LOCK (per channel) until it is asserted (high)
  - Poll F.0 HS_PLL_LOCK (per channel) until it is asserted (high)
- Issue Data path Reset
  - Write 1'b1 to E.3 DATAPATH_RESET
- Clear Latched Registers
  - Read 0x0F CHANNEL_STATUS_1 to clear (per channel)
- Device provisioning has completed at this point
- Periodically Check Device Operational Mode Status (Non-Errored Read Values Shown Below):
  - Read 0x0F CHANNEL_STATUS_1 and verify the following bits:
    - F.14 LA_SLAVE_STATUS (1'b1) (per channel)
    - F.13 HS_LOS (1'b0) (per channel)
    - F.12 HS_AZ_DONE (1'b1) (per channel)
    - F.11 HS_AGC_LOCKED (1'b1) (per channel)
    - F.10 HS_CHANNEL_SYNC (1'b1) (per channel)
    - F.8 HS_DECODE_INVALID (1'b0) (per channel)
    - F.7 TX_FIFO_UNDERFLOW (1'b0) (per channel)
    - F.6 TX_FIFO_OVERFLOW (1'b0) (per channel)
    - F.5 RX_FIFO_UNDERFLOW (1'b0) (per channel)
    - F.4 RX_FIFO_OVERFLOW (1'b0) (per channel)
    - F.3 RX_LS_OK (1'b1) (per channel).
    - F.2 TX_LS_OK (1'b1) (per channel).
    - F.1 LS_PLL_LOCK (1'b1) (per channel)
    - F.0 HS_PLL_LOCK (1'b1) (per channel)

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Initialization Setup (continued)

9.3.2 2:1 Mode (9.8304 Gbps on HS Side, 4.9152 Gbps Per Lane on LS Side, Only Lanes 0 and 1 on LS Side Active)

Note: Assume both channel A and channel B have the same setup.

REFCLK frequency = 122.88MHz, Mode = Transceiver, 2 to 1 serialization on LS side inputs and 1 to 2 deserialization on HS side inputs.

- Device Pin Setting(s) – Pin settings allow for maximum software configurability.
  - Ensure PD_TRXA_N input pin is High.
  - Ensure PD_TRXB_N input pin is High.
  - Ensure PRBSEN input pin is Low.
  - Ensure REFCLKA_SEL input pin is Low to enable software control.
  - Ensure REFCLKB_SEL input pin is Low to enable software control.
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 µs -or- Write 1’b1 to 0.15 GLOBAL_RESET) after power supply stabilization.
- Enable MDIO global write so that each MDIO write affects both channels to shorten provisioning time
  - Write 1’b1 to 0.11 GLOBAL_WRITE
- Clock Configuration and Mode control
  - Write 1’b0 to 1.9 RX_DEMUX_SEL to select 1 to 2 on the receive side
  - Write 1’b0 to 1.8 TX_MUX_SEL to select 2 to 1 on the transmit side
  - Select respective Channel SERDES REFCLK input (Default = REFCLK0P/N)
    - If REFCLK0P/N used – Write 1’b0 to 1.1 REFCLK_ SEL
    - If REFCLK1P/N used – Write 1’b1 to 1.1 REFCLK_ SEL
- HS/LS Data Rate Setting (Refer to Table 3 for more CPRI/OBSAI Rates)
  - Write 4’b1101 to 2.3:0 HS_PLL_MULT[3:0], write 2’b00 to 3.9:8 HS_RATE_RX[1:0], write 2’b00 to 3.1:0 HS_RATE_TX[1:0], to select FULL rate and 20x MPY on HS side (HS_SERDES_CONTROL_1 = 0x811D, HS_SERDES_CONTROL_2 = 0xA444).
  - Write 1'b1 to 9.9 HS_PEAK_DISABLE (HS_OVERLAY_CONTROL = 0x0B00)
  - Write 4’b1001 to 6.3:0 LS_MPY[3:0], write 2’b00 to 7.9:8 LS_IN_RATE[1:0], write 2’b00 to 7.1:0 LS_OUT_RATE [1:0], to select FULL rate and 20x MPY on LS side (LS_SERDES_CONTROL_1 = 0XF119, LS_SERDES_CONTROL_2 = 0xDC04).
- HS Serial Configuration
  - Configure the following bits per the desired application:
    - 2.9:8 (HS_LOOP_BANDWIDTH[1:0]), 2.6 (HS_VRANGE)
    - 3.15:12 (HS_SWING[3:0]), 3.7:6 (HS_AGCCTRL[1:0])
    - 3.5:4 (HS_AZCAL[1:0]), 4.14:12 (HS_EQPRE[2:0])
    - 4.11:10 (HS_CDRFMULT[1:0]), 4.9:8 (HS_CDRTHR[1:0])
    - 4.4:0 (HS_TWCRF[4:0]), 5.12:8 (HS_TWPOST1[4:0])
    - 5.7:4 (HS_TWPRE[3:0]), 5.3:0 (HS_TWPOST2[3:0])
- LS Serial Configuration
  - Configure the following bits per the desired application:
    - 7.14:12 (LS_SWING[2:0]), 7.7:4 (LS_DE[3:0])
    - 8.11:8 (LS_EQ [3:0]), 8.6:4 (LS_CDR [2:0])
- Toggle HS_ENRX
  - Write 1'b0 to 3.2 (HS_SERDES_CONTROL_2 = 0xA440)
  - Write 1'b1 to 3.2 (HS_SERDES_CONTROL_2 = 0xA444)
- Wait 10ms
- Check SERDES PLL Status for Locked State
  - Poll F.1 LS_PLL_LOCK (per channel) until it is asserted (high)
  - Poll F.0 HS_PLL_LOCK (per channel) until it is asserted (high)

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Initialization Setup (continued)

- Issue Data path Reset
  - Write 1'b1 to E.3 DATAPATH_RESET
- Clear Latched Registers
  - Read 0x0F CHANNEL_STATUS_1 to clear (per channel)
- Device provisioning has completed at this point
- Periodically Check Device Operational Mode Status (Non-Errored Read Values Shown Below):
  - Read 0x0F CHANNEL_STATUS_1 and verify the following bits:
    - F.14 LA_SLAVE_STATUS (1'b1) (per channel)
    - F.13 HS_LOS (1'b0) (per channel)
    - F.12 HS_AZ_DONE (1'b1) (per channel)
    - F.11 HS_AGC_LOCKED (1'b1) (per channel)
    - F.10 HS_CHANNEL_SYNC (1'b1) (per channel)
    - F.8 HS_DECODE_INVALID (1'b0) (per channel)
    - F.7 TX_FIFO_UNDERFLOW (1'b0) (per channel)
    - F.6 TX_FIFO_OVERFLOW (1'b0) (per channel)
    - F.5 RX_FIFO_UNDERFLOW (1'b0) (per channel)
    - F.4 RX_FIFO_OVERFLOW (1'b0) (per channel)
    - F.3 RX_LS_OK (1'b1) (per channel).
    - F.2 TX_LS_OK (1'b1) (per channel).
    - F.1 LS_PLL_LOCK (1'b1) (per channel)
    - F.0 HS_PLL_LOCK (1'b1) (per channel)

9.3.3 1:1 Mode (4.9152 Gbps on HS Side, 4.9152Gbps on LS side, Only Lane 0 on LS Side Active)

Note: Assume both channel A and channel B have the same setup.

REFCLK frequency = 122.88 MHz, Mode = Transceiver, 1 to 1 serialization on LS side inputs and 1 to 1 deserialization on HS side inputs.

- Device Pin Setting(s) – Pin settings allow for maximum software configurability.
  - Ensure PD_TRXA_N input pin is High.
  - Ensure PD_TRXB_N input pin is High.
  - Ensure PRBSEN input pin is Low.
  - Ensure REFCLKA_SEL input pin is Low to enable software control.
  - Ensure REFCLKB_SEL input pin is Low to enable software control.
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 µs -or- Write 1'b1 to 0.15 GLOBAL_RESET) after power supply stabilization.
- Enable MDIO global write so that each MDIO write affects both channels to shorten provisioning time
  - Write 1'b1 to 0.11 GLOBAL_WRITE
- Clock Configuration and Mode control
  - Write 1'b1 to 1.13 RX_MODE_SEL to select 1 to 1 on the receive side
  - Write 1'b1 to 1.12 TX_MODE_SEL to select 2 to 1 on the transmit side
  - Select respective Channel SERDES REFCLK input (Default = REFCLK0P/N)
    - If REFCLK0P/N used – Write 1'b0 to 1.1 REFCLK_ SEL
    - If REFCLK1P/N used – Write 1'b1 to 1.1 REFCLK_ SEL
- HS/LS Data Rate Setting (Refer to Table 2 for more CPRI/OBSAI Rates)
  - Write 4'b1101 to 2.3:0 HS_PLL_MULT[3:0], write 2'b01 to 3.9:8 HS_RATE_RX[1:0], write 2'b01 to 3.1:0 HS_RATE_TX[1:0], to select HALF rate and 20x MPY on HS side (HS_SERDES_CONTROL_1 = 0x811D, HS_SERDES_CONTROL_2 = 0xA545).
  - Write 4'b1001 to 6.3:0 LS_MPY[3:0], write 2'b00 to 7.9:8 LS_IN_RATE[1:0], write 2'b00 to 7.1:0

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Initialization Setup (continued)

LS_OUT_RATE [1:0], to select FULL rate and 20x MPY on LS side (LS_SERDES_CONTROL_1 = 0xF119, LS_SERDES_CONTROL_2 = 0xDC04).

- HS Serial Configuration
  - Configure the following bits per the desired application:
    - 2.9:8 (HS_LOOP_BANDWIDTH[1:0]), 2.6 (HS_VRANGE)
    - 3.15:12 (HS_SWING[3:0]), 3.7:6 (HS_AGCCTRL[1:0])
    - 3.5:4 (HS_AZCAL[1:0]), 4.14:12 (HS_EQPRE[2:0])
    - 4.11:10 (HS_CDRFMULT[1:0]), 4.9:8 (HS_CDRTHR[1:0])
    - 4.4:0 (HS_TWCRF[4:0]), 5.12:8 (HS_TWPOST1[4:0])
    - 5.7:4 (HS_TWPRE[3:0]), 5.3:0 (HS_TWPOST2[3:0])
- LS Serial Configuration
  - Configure the following bits per the desired application:
    - 7.14:12 (LS_SWING[2:0]), 7.7:4 (LS_DE[3:0])
    - 8.11:8 (LS_EQ [3:0]), 8.6:4 (LS_CDR [2:0])
- Toggle HS_ENRX
  - Write 1'b0 to 3.2 (HS_SERDES_CONTROL_2 = 0xA449)
  - Write 1'b1 to 3.2 (HS_SERDES_CONTROL_2 = 0xA44D)
- Wait 10ms
- Check SERDES PLL Status for Locked State
  - Poll F.1 LS_PLL_LOCK (per channel) until it is asserted (high)
  - Poll F.0 HS_PLL_LOCK (per channel) until it is asserted (high)
- Issue Data path Reset
  - Write 1’b1 to E.3 DATAPATH_RESET
- Clear Latched Registers
  - Read 0x0F CHANNEL_STATUS_1 to clear (per channel)
- Device provisioning has completed at this point
- Periodically Check Device Operational Mode Status (Non-Errored Read Values Shown Below):
  - Read 0x0F CHANNEL_STATUS_1 and verify the following bits:
    - F.13 HS_LOS (1’b0) (per channel)
    - F.12 HS_AZ_DONE (1’b1) (per channel)
    - F.11 HS_AGC_LOCKED (1’b1) (per channel)
    - F.7 TX_FIFO_UNDERFLOW (1’b0) (per channel)
    - F.6 TX_FIFO_OVERFLOW (1’b0) (per channel)
    - F.5 RX_FIFO_UNDERFLOW (1’b0) (per channel)
    - F.4 RX_FIFO_OVERFLOW (1’b0) (per channel)
    - F.1 LS_PLL_LOCK (1’b1) (per channel)
    - F.0 HS_PLL_LOCK (1’b1) (per channel)

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10 Power Supply Recommendations

The TLK10002 allows either the core or I/O power supply to be powered up for an indefinite period of time while the other supply is not powered up, if all of the following conditions are met:

1. All maximum ratings and recommending operating conditions are followed.
2. Bus contention while 1.5-V or 1.8-V power is applied (> 0 V) must be limited to 100 hours over the projected lifetime of the device.
3. Junction temperature is less than 105°C during device operation. Note: Voltage stress up to the absolute maximum voltage values for up to 100 hours of lifetime operation at a T_J of 105°C or lower will minimally impact reliability.

The TLK10002 LVCMOS I/O are not failsafe (that is, cannot be driven with the I/O power disabled). TLK10002 inputs must not be driven high until their associated power supply is active.

11 Layout

11.1 Layout Guidelines

Both *low-speed* side and *high-speed* side serial signals are referred to as *high-speed* signals for the purpose of this document as they support very high data rates. For that reason, take care to realize them on a printed-circuit board with signal integrity in mind. The high-speed data path CML input pins INA[3:0]P/INA[3:0]N, INB[3:0]P/INB[3:0]N, HSRXAP/HSRXAN, and HSRXBP/HSRXBN, and the CML output pins OUTA[3:0]P/OUTA[3:0]N, OUTB[3:0]P/OUTB[3:0]N, HSTXAP/HSTXAN, and HSTXBP/HSTXBN, have to be connected with loosely-coupled 100-Ω differential transmission lines. Differential intra-pair skew needs to be minimized to within ±1 mil. Inter-pair (lane-to-lane) skew for the low-speed signals can be as high as 30 UI. An example of FR-4 printed-circuit board (PCB) realization of such differential transmission lines in microstrip format is shown in Figure 35.

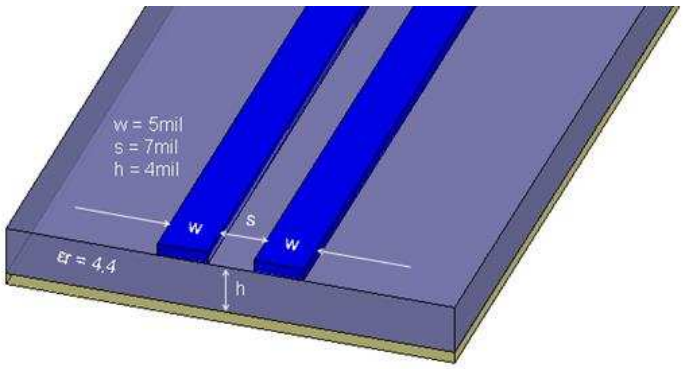

Figure 35. Differential Microstrip PCB Trace Geometry Example

To avoid impedance discontinuities the high-speed serial signals must be routed on a PCB on either the top or bottom PCB layers in microstrip format with no vias. If vias are unavoidable, an absolute minimum number of vias need to be used. The vias must be made to stretch through the entire PCB thickness (as shown in Figure 35) to connect microstrip traces on the top and bottom layers of the PCB so as to leave no via stubs that can severely impact the performance. If stripline traces are absolutely necessary, and if via back-drilling is not possible, then the routing layers should be chosen so as to have via stubs that are shorter than 10 mils.

All unused internal layer via pads on high-speed signal vias must be removed to further improve impedance matching. On the high-speed side, the HSRXAP/HSRXAN and HSRXBP/HSRXBN signals are more sensitive to impedance discontinuities introduced by vias than HSTXAP/HSTXAN and HSTXBP/HSTXBN signals. For that reason, if only some of those signals need to be routed with vias, then the latter must be routed with vias and the former with no vias.

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Layout Guidelines (continued)

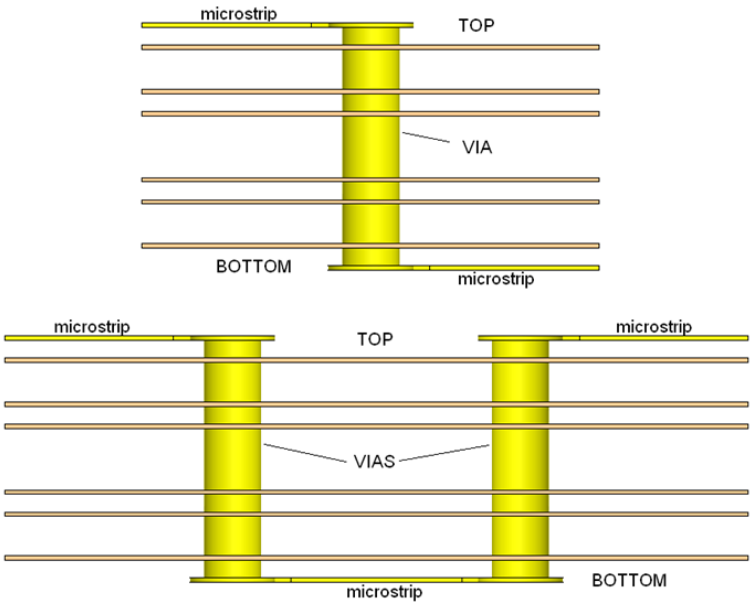

Figure 36. Examples of High-Speed PCB Traces With Vias that Have No Via Stubs and No Via Pads on Internal Layers

To further improve on impedance matching, differential vias with neighboring ground vias can be used as shown in Figure 37. The optimum dimensions of such a differential via structure depend on various parameters such as the trace geometry, dielectric material, as well as the PCB layer stack-up. A 3D electromagnetic field solver can be used to find the optimum via dimensions.

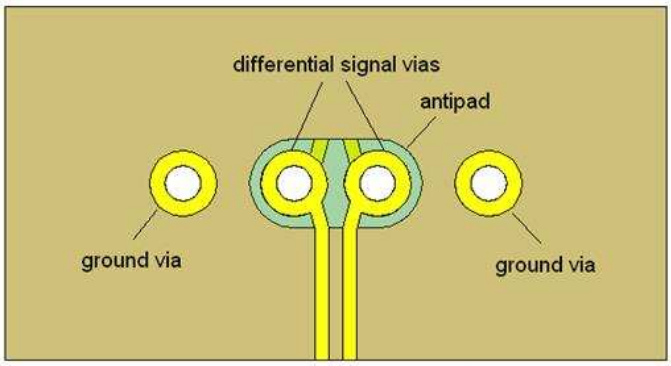

Figure 37. A Differential PCB Via Structure (Top View)

PCB traces connected to the HSRXAP/HSRXAN and HSRXBP/HSRXBN pins must have differential insertion loss of less than 25 dB at 5 GHz.

Surface-mount connector pads such as those used with the SFP/SFP+ module connectors are wider and hence have characteristic impedance that is lower than the regular high-speed PCB traces. If the pads are more than 2 times wider than the PCB traces, the pads' impedance needs to be increased to minimize impedance discontinuities. The easy way of increasing the pads' impedance is to cut out the reference plane immediately under those pads as shown in Figure 38 so as to have the pads refer to a reference plane on lower layers while maintaining 100-Ω differential characteristic impedance.

Layout Guidelines (continued)

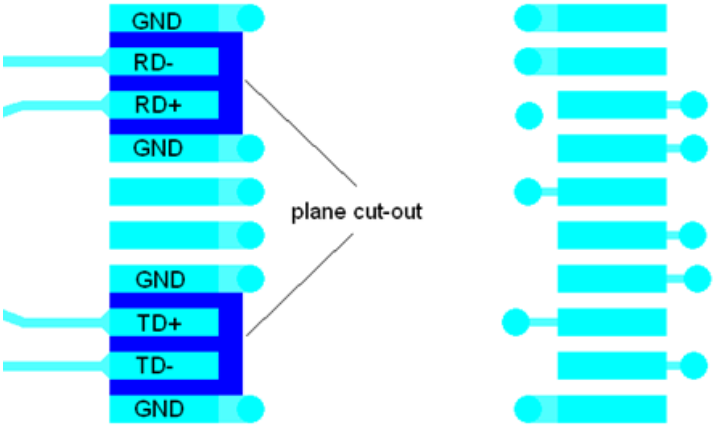

Figure 38. Reference Plane Cut-Out Under SFP/SFP+ Module Connector Pads

11.1.1 AC Coupling

A 0.1-µF series AC-coupling capacitor must be connected to each of the high-speed data path pins INA[3:0]P/INA[3:0]N, INB[3:0]P/INB[3:0]N, HSRXAP/HSRXAN, HSRXBP/HSRXBN, OUTA[3:0]P/OUTA[3:0]N, OUTB[3:0]P/OUTB[3:0]N, HSTXAP/HSTXAN, and HSTXBP/HSTXBN. If the TLK10002 high-speed side data path pins are connected to SFP/SFP+ optical modules with internal AC-coupling capacitors, then no external capacitors should be used. Adding additional series capacitors may severely impact the performance.

To avoid impedance discontinuities, TI strongly recommends where possible to make the transmission line trace width closely match the AC-coupling capacitor pad size. Smaller capacitor packages such as 0201 make it easy to meet that condition.

11.1.2 TLK10002 Clocks: REFCLK, CLKOUT – General Information

The TLK10002 device requires a low-jitter reference clock to work. The reference clock can be provided on the REFCLK0P/N or REFCLK1P/N pins. Both reference clock input pins have internal 100-Ω differential terminations, so they do not need any external terminations. Both reference clock inputs must be AC-coupled with preferably 0.1-µF capacitors. The two channels (A and B) can have same or different reference clocks.

The TLK10002 serial receiver recovers clock and data from the incoming serial data. The recovered byte clock is made available on the CLKOUTAP/N and/or CLKOUTBP/N pins. The CLKOUTxP/N CML output pins must be AC-coupled with 0.1-µF AC-coupling capacitors.

11.1.3 External Clock Connections

An external clock jitter cleaner, such as Texas Instruments CDCE72010 or CDCM7005, may be used when needed to provide a low jitter reference clock. An example external clock jitter cleaner connection for channel A is shown in Figure 39.

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Layout Guidelines (continued)

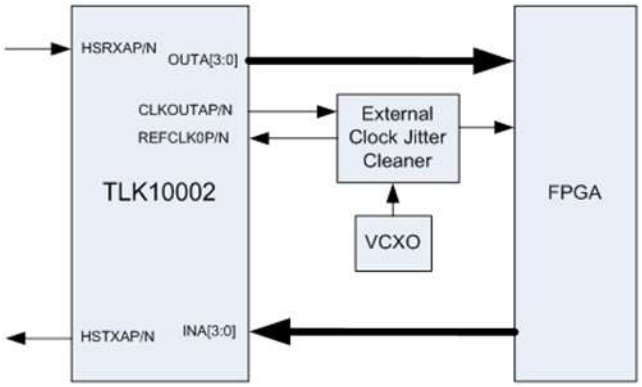

Figure 39. An External Clock Jitter Cleaner Connection Example for Channel A

11.1.4 TLK10002 Control Pins and Interfaces

The TLK10002 device features a number of control pins and interfaces, some of which are described below.

11.1.4.1 MDIO Interface

The TLK10002 supports the Management Data Input/Output (MDIO) Interface as defined in Clause 22 of the IEEE 802.3 Ethernet specification. The MDIO allows register-based management and control of the serial links.

The MDIO Management Interface consists of a bidirectional data path (MDIO) and a clock reference (MDC). The port address is determined by the PRTAD[4:0] control pins.

The MDIO pin requires a pullup to VDDO[1:0]. No pullup is needed on the MDC pin if driven with a push-pull MDIO master, but a pullup to VDDO[1:0] is needed if driven with an open-drain MDIO master.

11.1.4.2 JTAG Interface

The JTAG interface is mostly used for device test. The JTAG interface operates through the TDI, TDO, TMS, TCK, and TRST_N pins. If not used, all the pins can be left unconnected except TDI and TCK which have to be grounded.

11.1.4.3 Unused Pins

As a general guideline, any unused LVCMOS input pin needs to be grounded and any unused LVCMOS output pin can be left unconnected. Unused CML differential output pins can be left unconnected. Unused CML differential input pins should be tied to ground through a shared 100-Ω resistor.

11.2 Layout Example

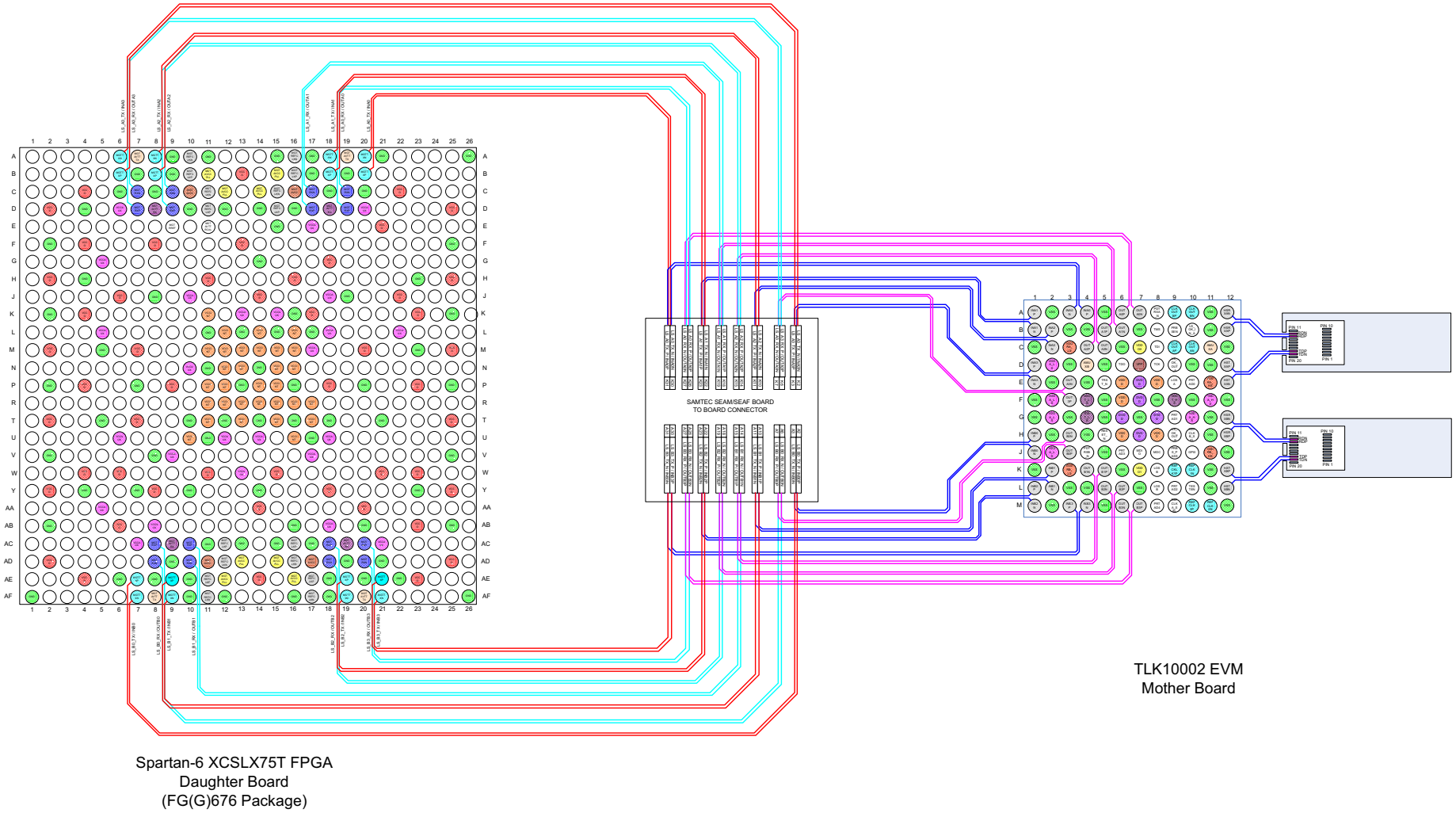

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Figure 40. Board-to-Board Connector Pinout and Routing

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLK10002CTR	Active	Production	FCBGA (CTR) | 144	119 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-4-260C-72 HR	-40 to 85	TLK10002
TLK10002CTR.A	Active	Production	FCBGA (CTR) | 144	119 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-4-260C-72 HR	-40 to 85	TLK10002

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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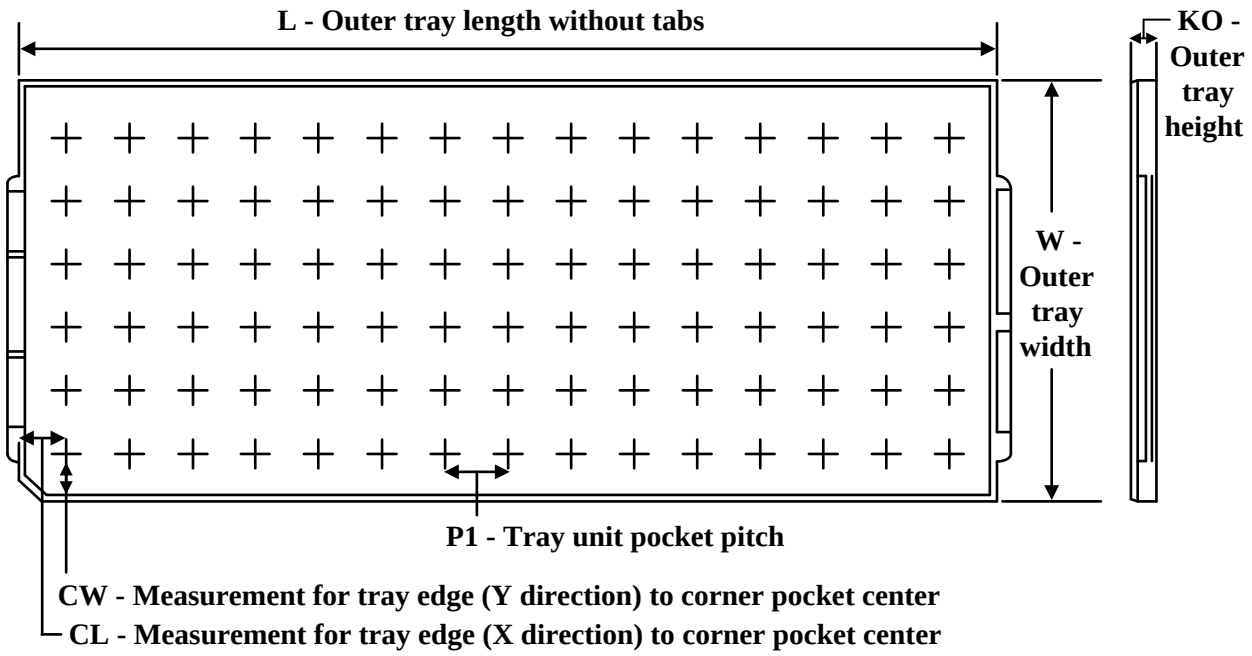
TRAY

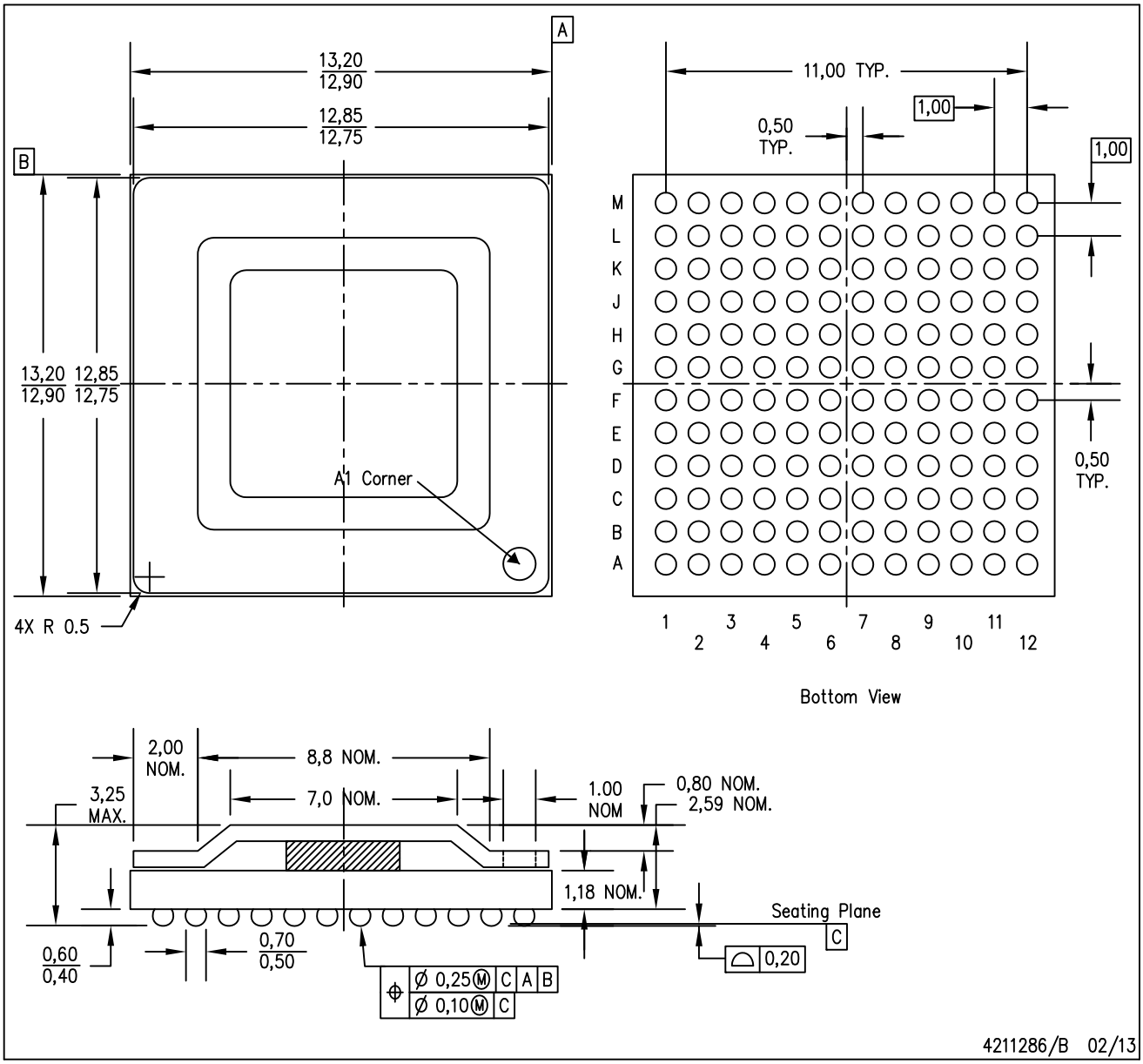


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TLK10002CTR	CTR	FCBGA	144	119	7x17	150	315	135.9	7620	18.1	12.7	12.9
TLK10002CTR.A	CTR	FCBGA	144	119	7x17	150	315	135.9	7620	18.1	12.7	12.9

CTR (S–PBGA–N144) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free die bump and solder ball.

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