

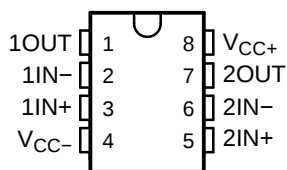
## FEATURES

- Operating Voltage... $\pm 2$  V to  $\pm 18$  V
- Low Offset Voltage...1 mV Max at 25°C, TL5580A
- Wide GBW...12 MHz Typ
- Slew Rate...5 V/ $\mu$ s Typ
- Low THD...0.0005% Typ
- Low-Noise Voltage...7 nV/ $\sqrt{\text{Hz}}$  at 1 kHz Typ

## APPLICATIONS

- Audio
- Test Equipment
- Industrial Process Controls
- Data-Acquisition Systems
- Active Filters
- Power-Supply Regulation

D, P, OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The TL5580 is a dual bipolar operational amplifier that combines both high dc and ac performance with its low offset voltage, high-gain bandwidth, low harmonic distortion, and low-noise characteristics. In addition, its output is capable of driving 600- $\Omega$  loads. All these characteristics make the device ideally suited for use in audio, active filtering, and industrial measurement applications.

### ORDERING INFORMATION

| $T_A$         | $V_{IO}$<br>(25°C, MAX)  | PACKAGE <sup>(1)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|--------------------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 85°C | Standard grade<br>1.5 mV | PDIP – P               | Tube of 50   | TL5580IP              | TL5580IP         |
|               |                          | SOIC – D               | Tube of 75   | TL5580ID              | Z5580            |
|               |                          |                        | Reel of 2500 | TL5580IDR             |                  |
|               |                          | TSSOP – PW             | Tube of 150  | TL5580IPW             | Z5580            |
|               |                          |                        | Reel of 2000 | TL5580IPWR            |                  |
|               | A grade<br>1 mV          | PDIP – P               | Tube of 50   | TL5580AIP             | TL5580AIP        |
|               |                          | SOIC – D               | Tube of 75   | TL5580AID             | Z5580A           |
|               |                          |                        | Reel of 2500 | TL5580AIDR            |                  |
|               |                          | TSSOP – PW             | Tube of 150  | TL5580AIPW            | Z5580A           |
|               |                          |                        | Reel of 2000 | TL5580AIPWR           |                  |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



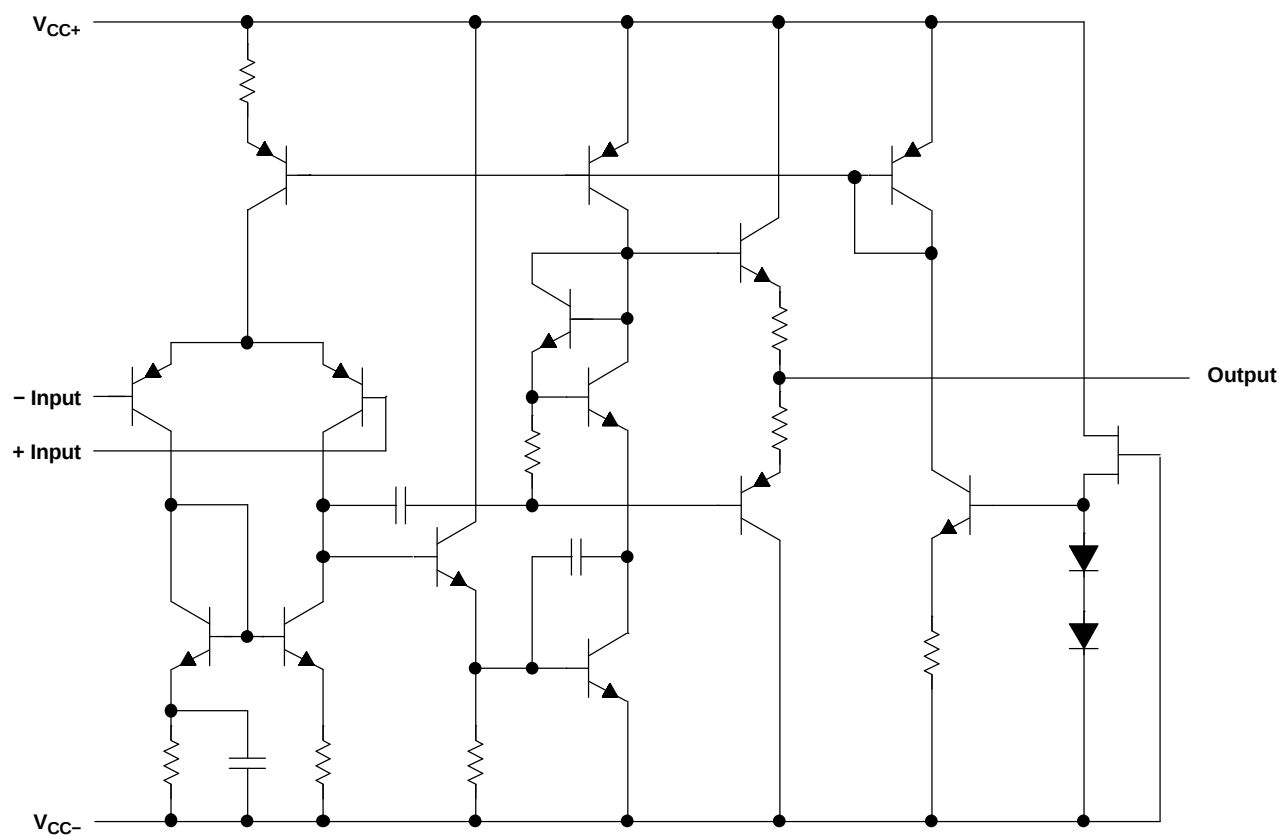
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# TL5580, TL5580A

## DUAL LOW-NOISE WIDE-BANDWIDTH PRECISION AMPLIFIER

SLOS477A–JUNE 2005–REVISED JULY 2005

### EQUIVALENT SCHEMATIC



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|               |                                             | MIN        | MAX | UNIT |
|---------------|---------------------------------------------|------------|-----|------|
| $V_{CC\pm}$   | Supply voltage                              |            | ±18 | V    |
| $V_I$         | Input voltage (any input)                   |            | ±15 | V    |
| $V_{ID}$      | Differential input voltage                  |            | ±30 | V    |
| $I_O$         | Output current                              |            | ±50 | mA   |
| $\theta_{JA}$ | Package thermal impedance <sup>(2)(3)</sup> | D package  | 97  | °C/W |
|               |                                             | P package  | 85  |      |
|               |                                             | PW package | 149 |      |
| $T_J$         | Operating virtual junction temperature      |            | 150 | °C   |
| $T_{stg}$     | Storage temperature range                   | –60        | 125 | °C   |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions

|           |                                | MIN | MAX | UNIT |
|-----------|--------------------------------|-----|-----|------|
| $V_{CC+}$ | Supply voltage                 | 2   | 16  | V    |
| $V_{CC-}$ |                                | –2  | –16 |      |
| $T_A$     | Operating free-air temperature | –40 | 85  | °C   |

# TL5580, TL5580A

## DUAL LOW-NOISE WIDE-BANDWIDTH PRECISION AMPLIFIER

SLOS477A–JUNE 2005–REVISED JULY 2005



### Electrical Characteristics

$V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

| PARAMETER       |                                                         | TEST CONDITIONS                                                            | $T_A$         | MIN | TYP              | MAX        | UNIT                         |
|-----------------|---------------------------------------------------------|----------------------------------------------------------------------------|---------------|-----|------------------|------------|------------------------------|
| $V_{IO}$        | Input offset voltage                                    | $R_S \leq 10\text{ k}\Omega$                                               | 25°C          |     | 0.3              | 1          | mV                           |
|                 |                                                         |                                                                            | –40°C to 85°C |     |                  | 1.35       |                              |
|                 |                                                         |                                                                            | 25°C          |     | 0.3              | 1.5        |                              |
|                 |                                                         |                                                                            | –40°C to 85°C |     |                  | 2          |                              |
| $\alpha V_{IO}$ | Average temperature coefficient of input offset voltage |                                                                            | –40°C to 85°C |     | 1.8              | 5          | $\mu\text{V}/^\circ\text{C}$ |
| $I_{IO}$        | Input offset current                                    |                                                                            | 25°C          |     | 5                | 75         | nA                           |
|                 |                                                         |                                                                            | –40°C to 85°C |     |                  | 100        |                              |
| $I_{IB}$        | Input bias current                                      |                                                                            | 25°C          |     | 100              | 500        | nA                           |
|                 |                                                         |                                                                            | –40°C to 85°C |     |                  | 800        |                              |
| $A_{VD}$        | Large-signal differential-voltage amplification         | $R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}$                      | 25°C          |     | 90               | 110        | dB                           |
|                 |                                                         |                                                                            | –40°C to 85°C |     | 87               |            |                              |
| $V_{OM}$        | Output voltage swing                                    | $R_L \geq 2\text{ k}\Omega$                                                | 25°C          |     | 12.75<br>– 12.25 | $\pm 13.5$ | V                            |
|                 |                                                         |                                                                            | –40°C to 85°C |     | 12.5<br>– 12     |            |                              |
| $V_{ICR}$       | Common-mode input voltage range                         |                                                                            | 25°C          |     | $\pm 13$         | $\pm 13.5$ | V                            |
|                 |                                                         |                                                                            | –40°C to 85°C |     | $\pm 12$         |            |                              |
| CMRR            | Common-mode rejection ratio                             | $R_S \leq 10\text{ k}\Omega$ ,<br>$V_{ICR} = -12\text{ V to } 12\text{ V}$ | 25°C          |     | 90               | 110        | dB                           |
|                 |                                                         |                                                                            | –40°C to 85°C |     | 85               |            |                              |
| $k_{SVR}^{(1)}$ | Supply-voltage rejection ratio                          | $R_S \leq 10\text{ k}\Omega$                                               | 25°C          |     | 85               | 110        | dB                           |
|                 |                                                         |                                                                            | –40°C to 85°C |     | 83               |            |                              |
| $I_{CC}$        | Supply current (all amplifiers)                         |                                                                            | 25°C          |     | 6                | 9          | mA                           |
|                 |                                                         |                                                                            | –40°C to 85°C |     |                  | 12         |                              |

(1) Measured with  $V_{CC\pm}$  varied simultaneously

### Operating Characteristics

$V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER |                                | TEST CONDITIONS                                                                              | TYP    | UNIT                   |
|-----------|--------------------------------|----------------------------------------------------------------------------------------------|--------|------------------------|
| SR        | Slew rate at unity gain        | $R_L \geq 2\text{ k}\Omega$                                                                  | 5      | V/ $\mu\text{s}$       |
| GBW       | Gain bandwidth product         | $f = 10\text{ kHz}$                                                                          | 12     | MHz                    |
| THD       | Total harmonic distortion      | $V_O = 5\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $f = 1\text{ kHz}$ , $A_{VD} = 20\text{ dB}$ | 0.0005 | %                      |
| $V_n$     | Equivalent input noise voltage | $f = 1\text{ kHz}$                                                                           | 7      | nV/ $\sqrt{\text{Hz}}$ |

## TYPICAL CHARACTERISTICS

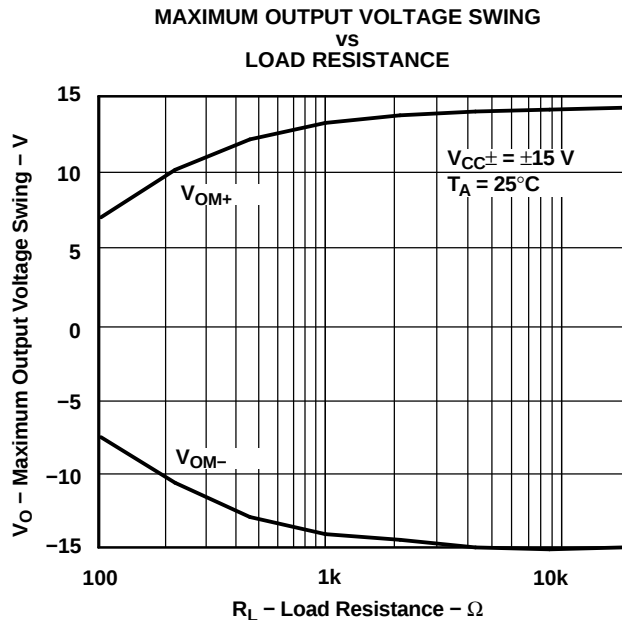


Figure 1.

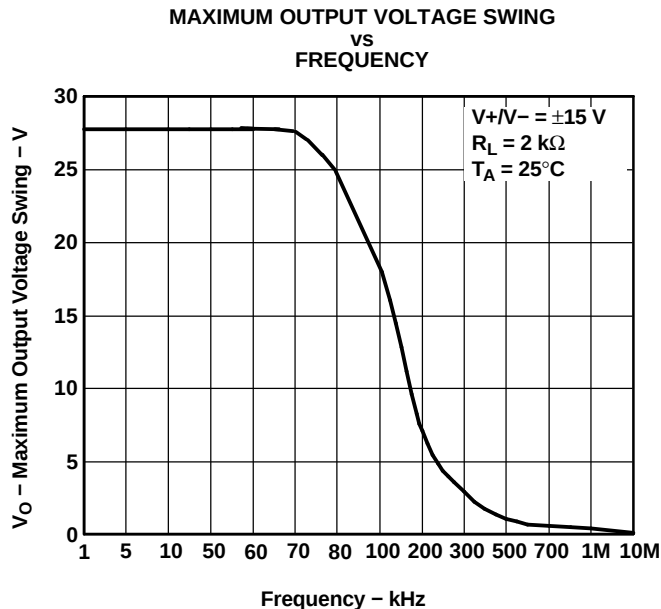


Figure 2.

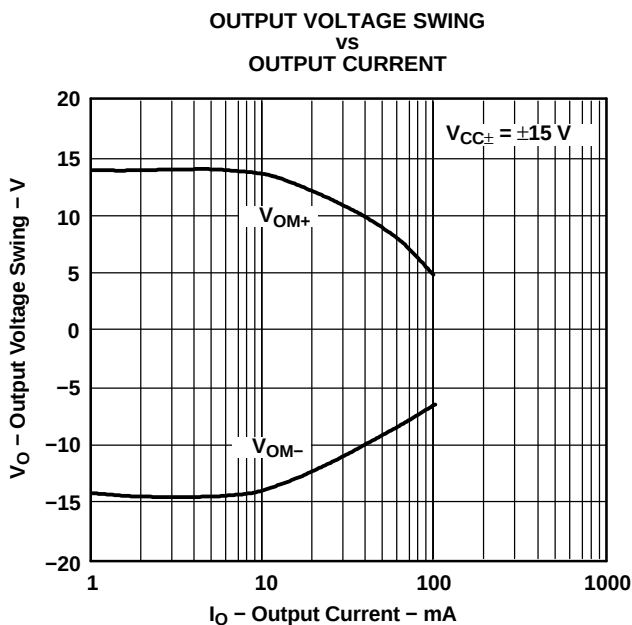


Figure 3.

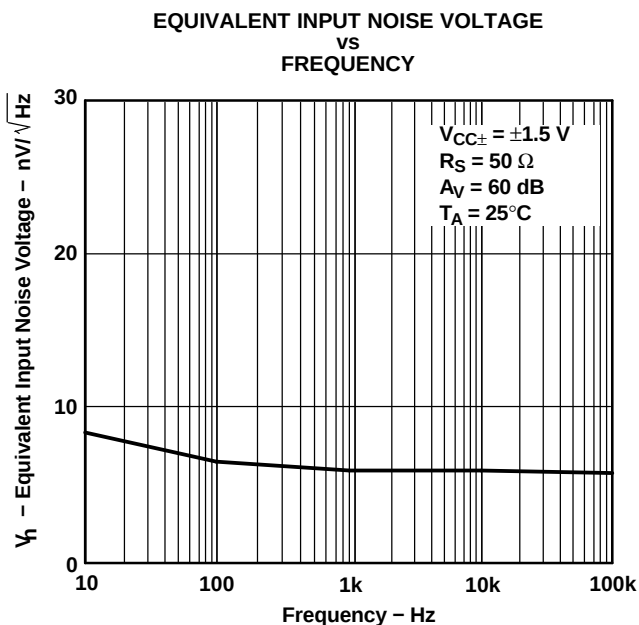


Figure 4.

## TYPICAL CHARACTERISTICS (continued)

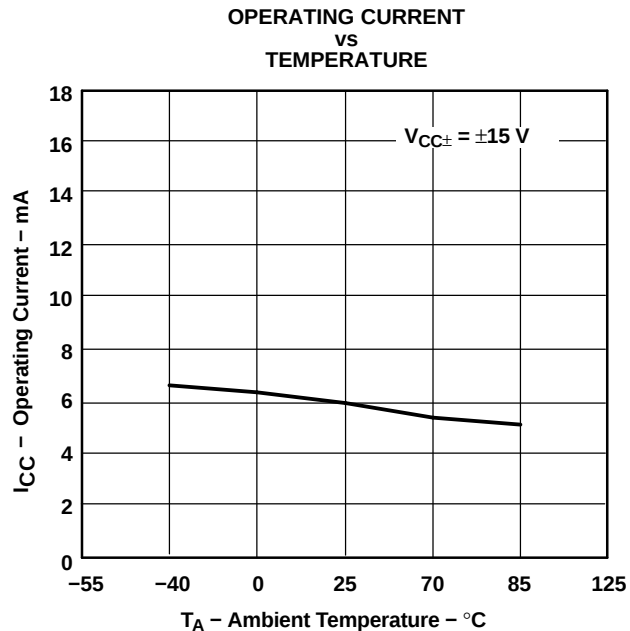


Figure 5.

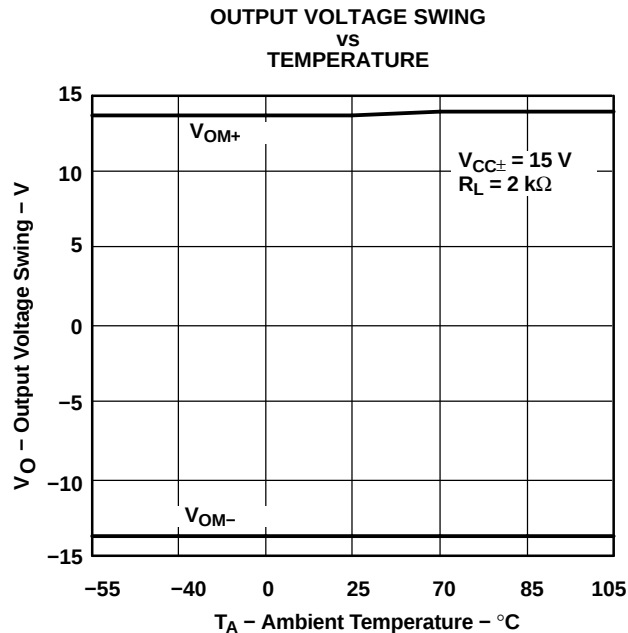


Figure 6.

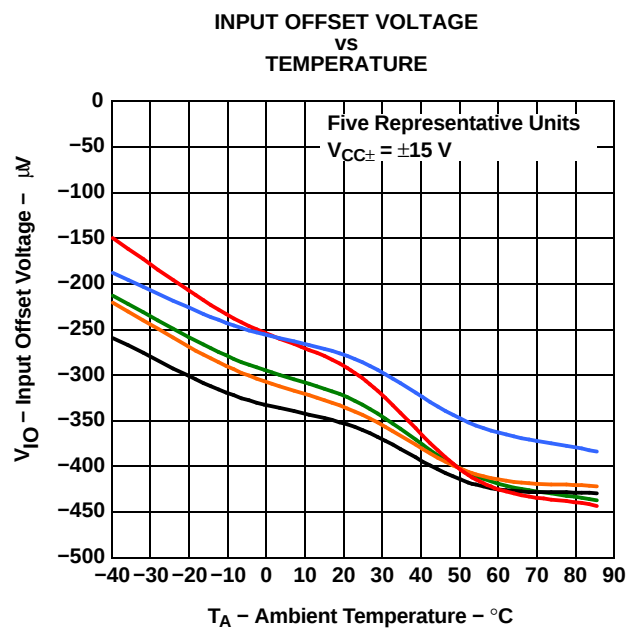


Figure 7.

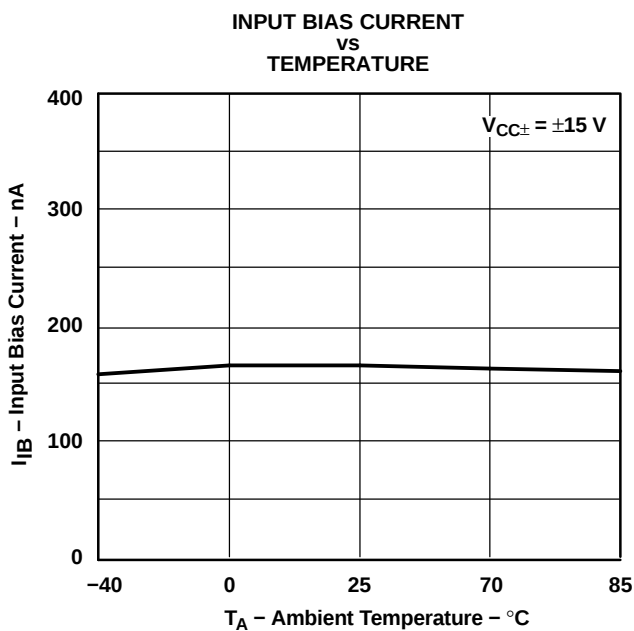


Figure 8.

## TYPICAL CHARACTERISTICS (continued)

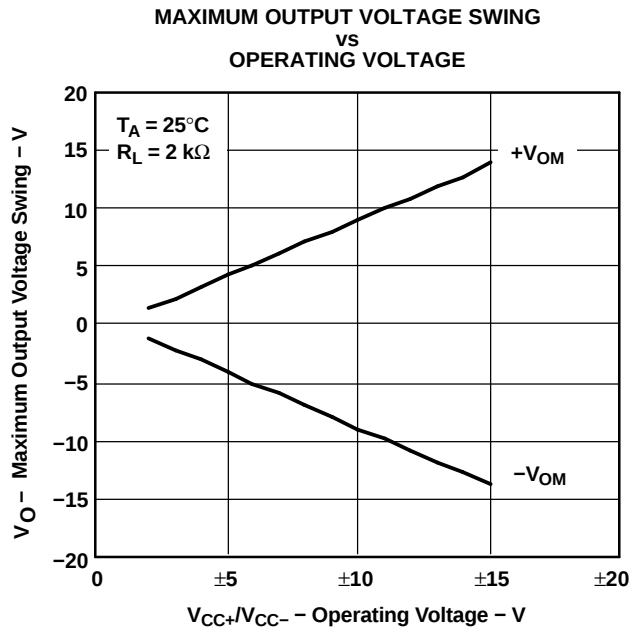


Figure 9.

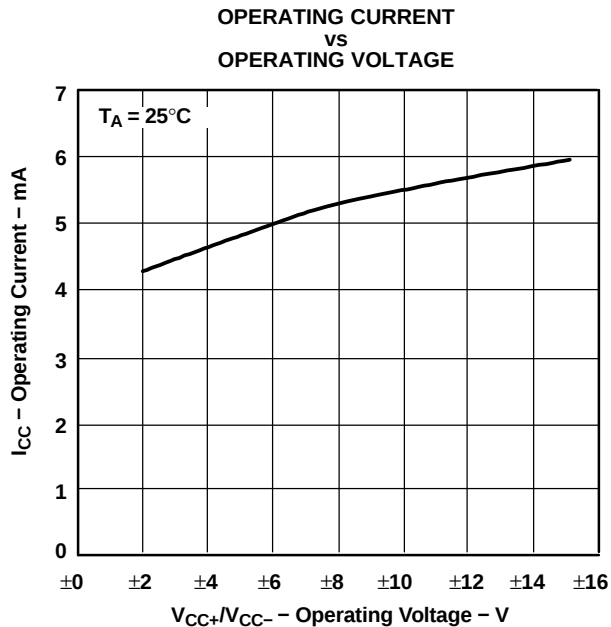


Figure 10.

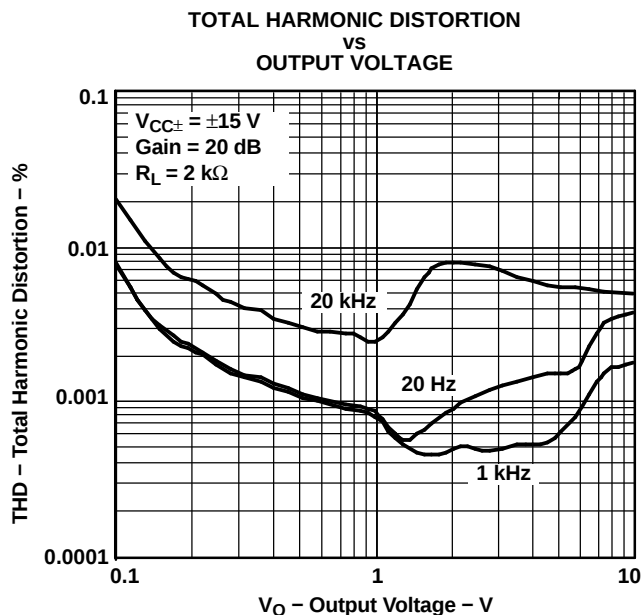


Figure 11.

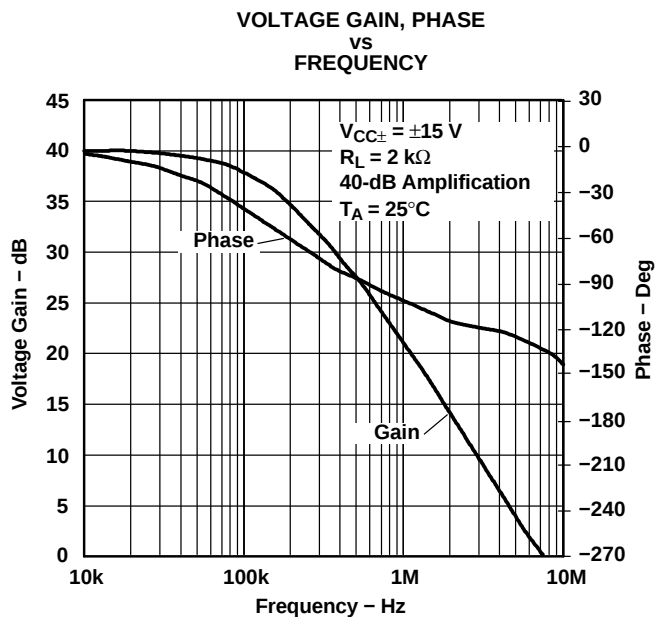


Figure 12.

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TL5580AID</a>   | Obsolete      | Production           | SOIC (D)   8   | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | Z5580A              |
| <a href="#">TL5580AIDR</a>  | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | Z5580A              |
| TL5580AIDR.A                | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | Z5580A              |
| <a href="#">TL5580AIP</a>   | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | TL5580AIP           |
| TL5580AIP.A                 | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | TL5580AIP           |
| <a href="#">TL5580AIPWR</a> | Active        | Production           | TSSOP (PW)   8 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | Z5580A              |
| TL5580AIPWR.A               | Active        | Production           | TSSOP (PW)   8 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | Z5580A              |
| <a href="#">TL5580IDR</a>   | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | Z5580               |
| TL5580IDR.A                 | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | Z5580               |
| <a href="#">TL5580IP</a>    | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | TL5580IP            |
| TL5580IP.A                  | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | TL5580IP            |
| <a href="#">TL5580IPWR</a>  | Active        | Production           | TSSOP (PW)   8 | 2000   LARGE T&R      | Yes         | NIPDAU   NIPDAU                      | Level-1-260C-UNLIM                | -40 to 85    | Z5580               |
| TL5580IPWR.A                | Active        | Production           | TSSOP (PW)   8 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | Z5580               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

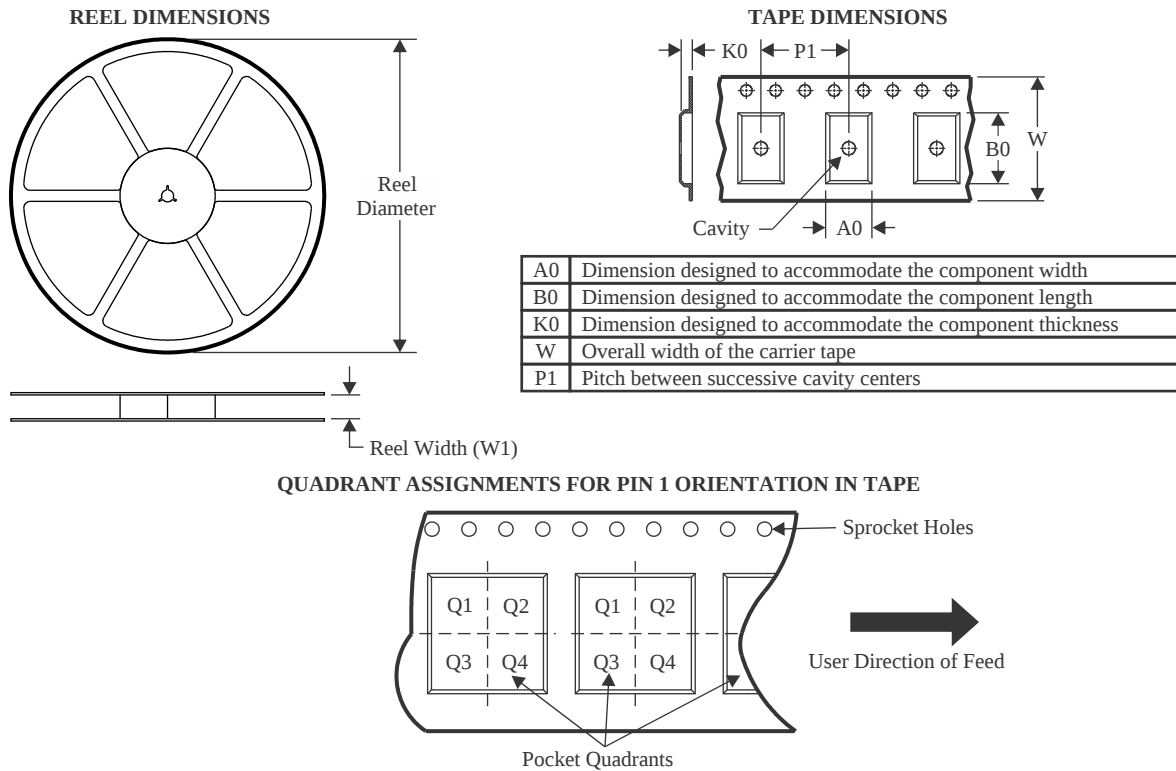
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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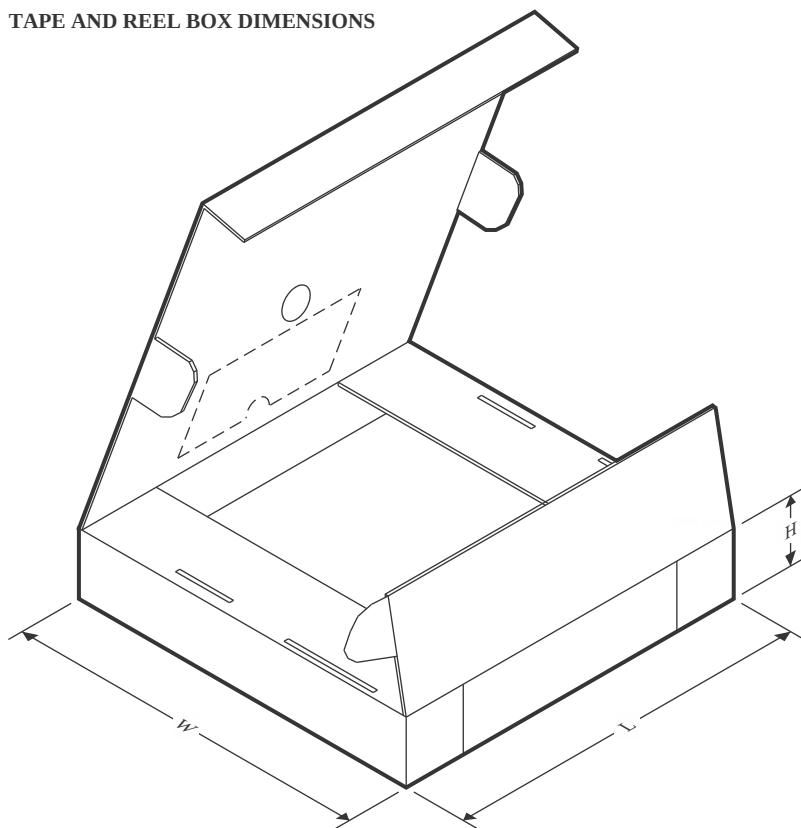
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL5580AIDR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL5580AIPWR | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TL5580IDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL5580IPWR  | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TL5580IPWR  | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL5580AIDR  | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| TL5580AIPWR | TSSOP        | PW              | 8    | 2000 | 356.0       | 356.0      | 35.0        |
| TL5580IDR   | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| TL5580IPWR  | TSSOP        | PW              | 8    | 2000 | 356.0       | 356.0      | 35.0        |
| TL5580IPWR  | TSSOP        | PW              | 8    | 2000 | 353.0       | 353.0      | 32.0        |

## TUBE

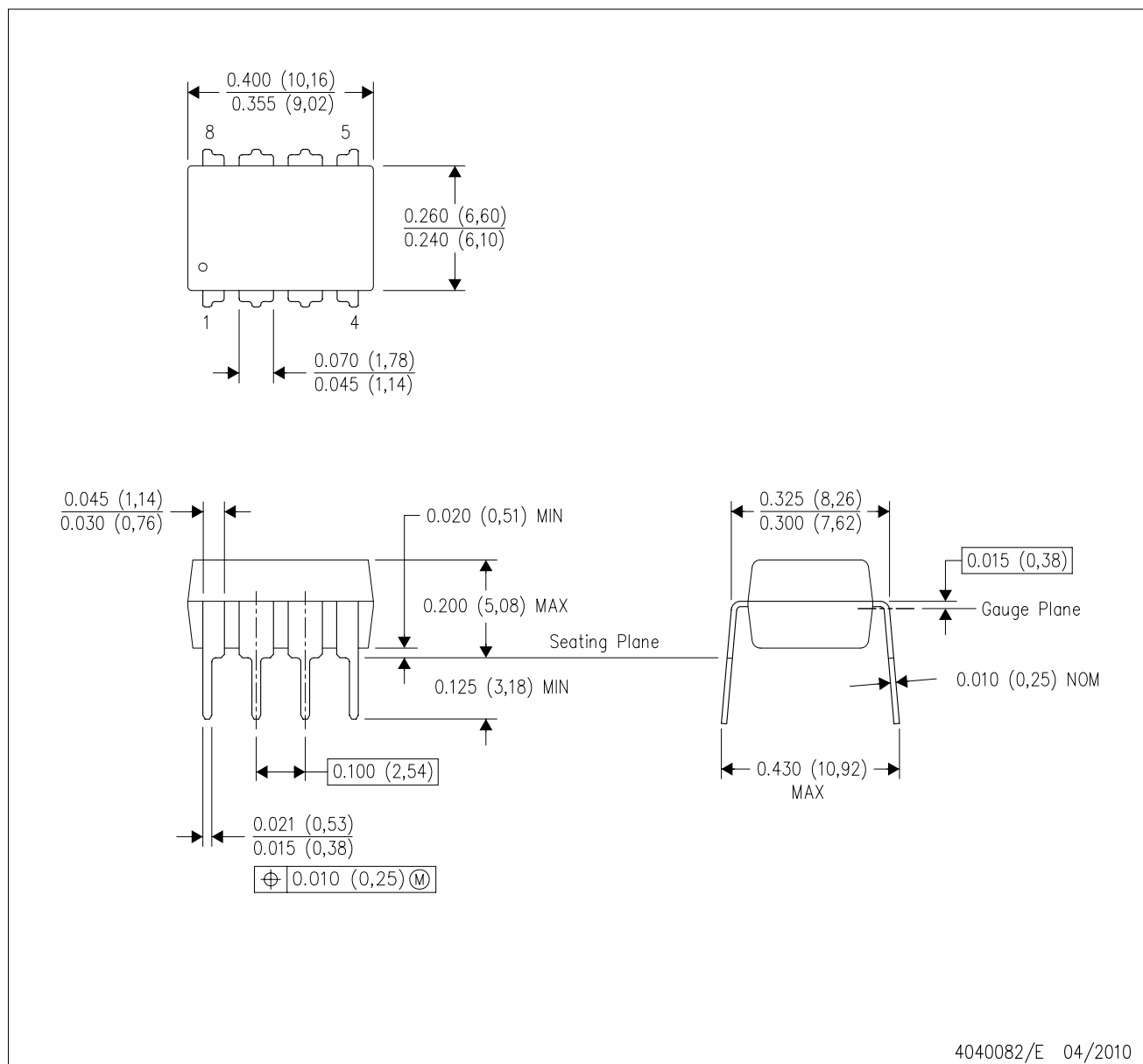


\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TL5580AIP   | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| TL5580AIP.A | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| TL5580IP    | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| TL5580IP.A  | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

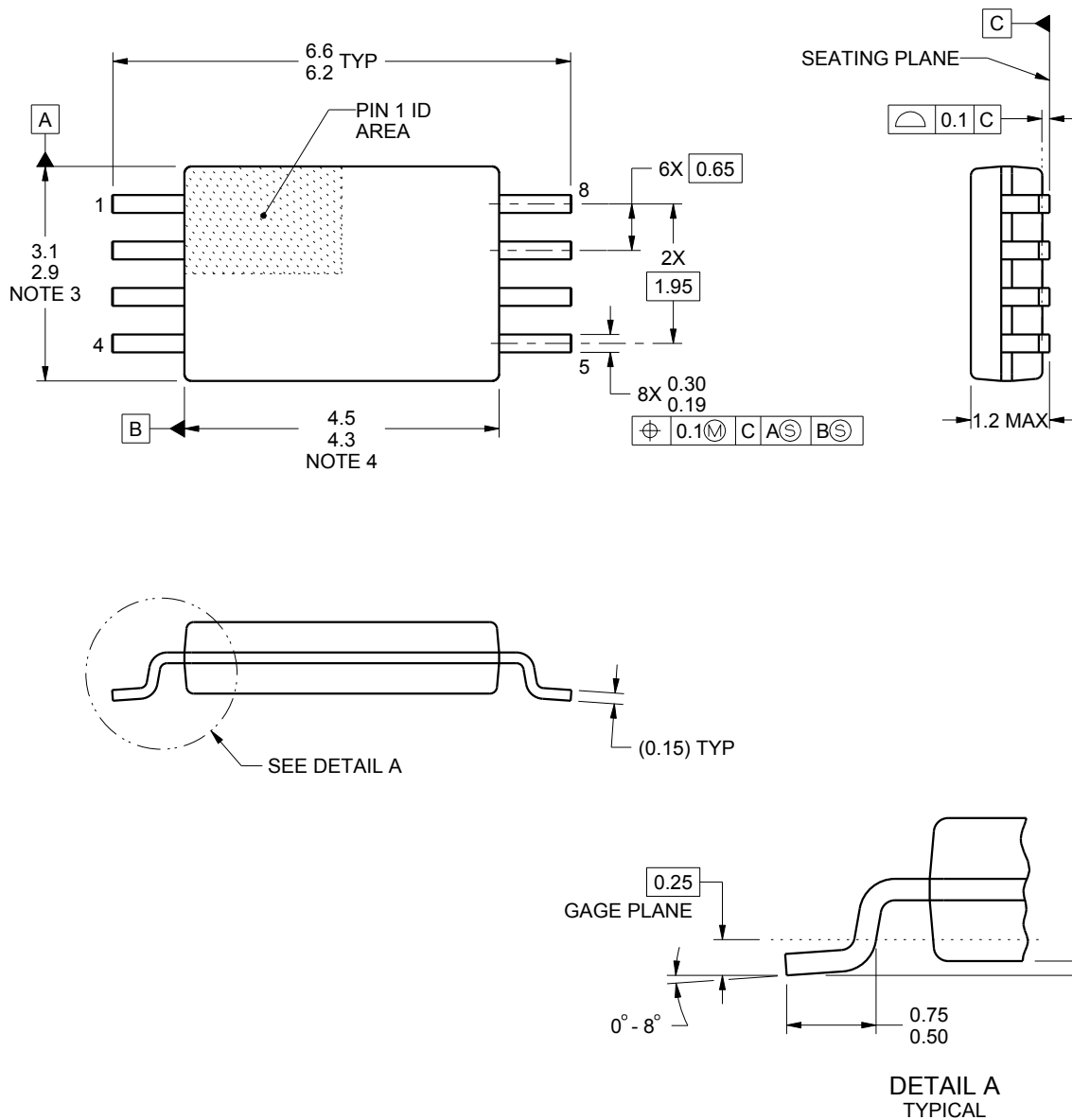
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

### NOTES:

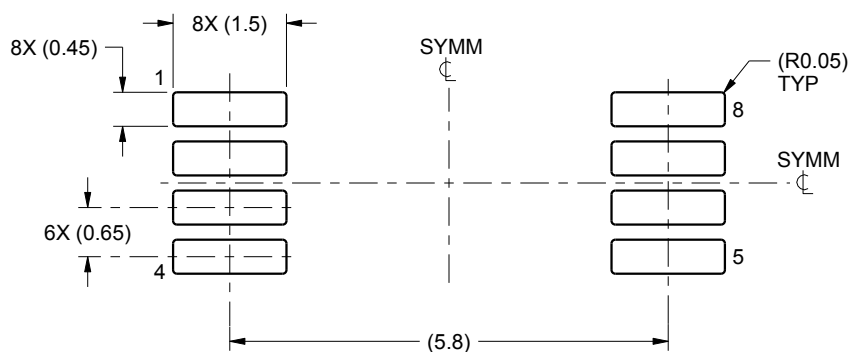
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

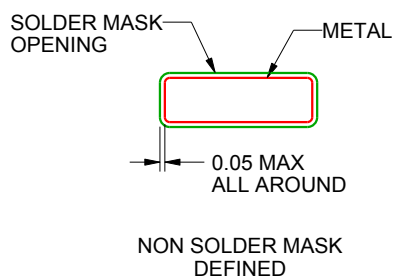
PW0008A

TSSOP - 1.2 mm max height

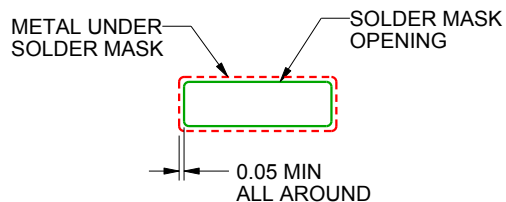
SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

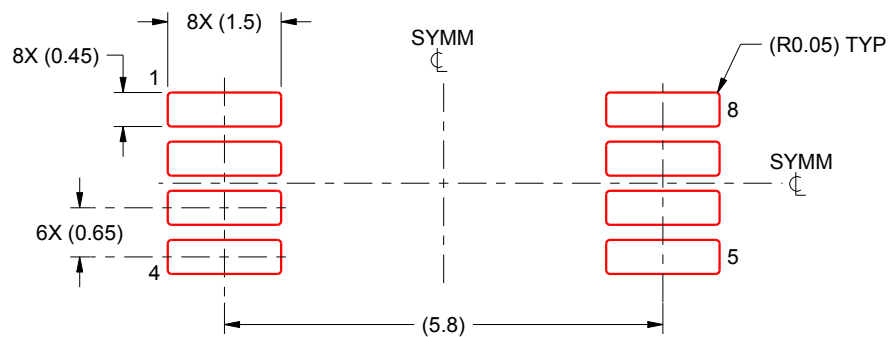
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



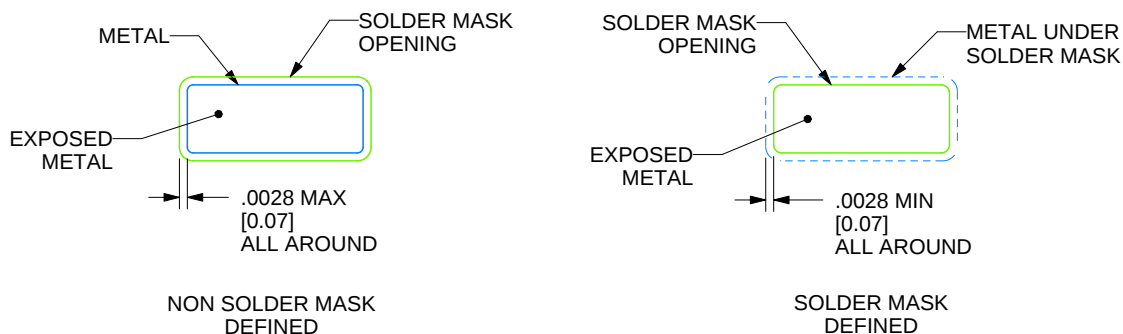
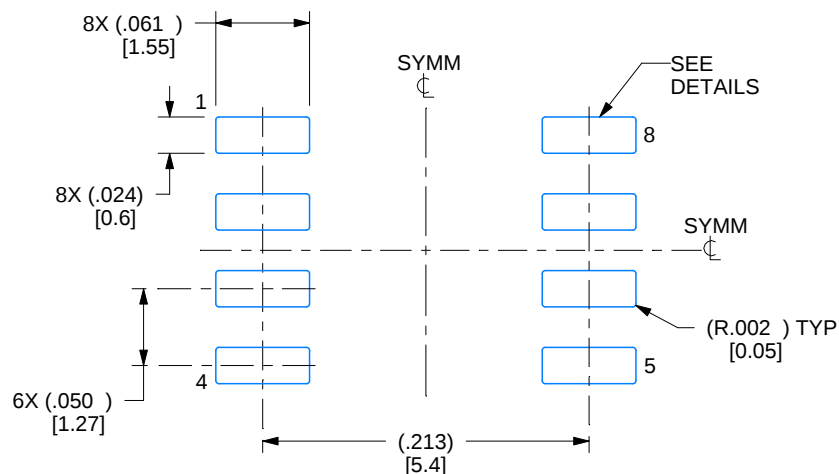
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

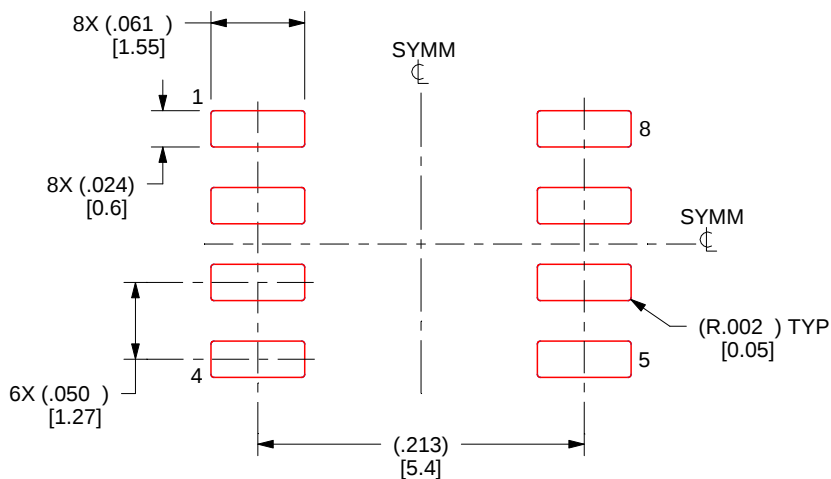
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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