TLC5971 12-Channel, 16-Bit, Enhanced Spectrum, PWM, RGB, LED Driver With 3.3-V Linear Regulator

1 Features

- 12 Constant-Current Sink Output Channels
- Current Capability: 60 mA Per Channel
- Grayscale (GS) Control With Enhanced Spectrum PWM:
  16-Bit (65536 Steps)
- Global Brightness Control (BC):
  7-Bit (128 Steps) for Each Color Group
- Power-Supply Voltage Range:
  - Internal Linear Regulator: 6 V to 17 V
  - Direct Power Supply: 3 V to 5.5 V
- LED Supply Voltage: Up to 17 V
- Constant-Current Accuracy:
  - Channel-to-Channel = ±1% (Typical)
  - Device-to-Device = ±1% (Typical)
- Data Transfer Rate: 20 MHz
- Linear Voltage Regulator: 3.3 V
- Auto Display Repeat Function
- Display Timing Reset Function
- Internal and External Selectable GS Clock
- Thermal Shutdown (TSD) With Auto Restart
- Unlimited Device Cascading
- Operating Temperature Range: –40°C to +85°C

2 Applications

RGB LED Cluster Lamp Displays

3 Description

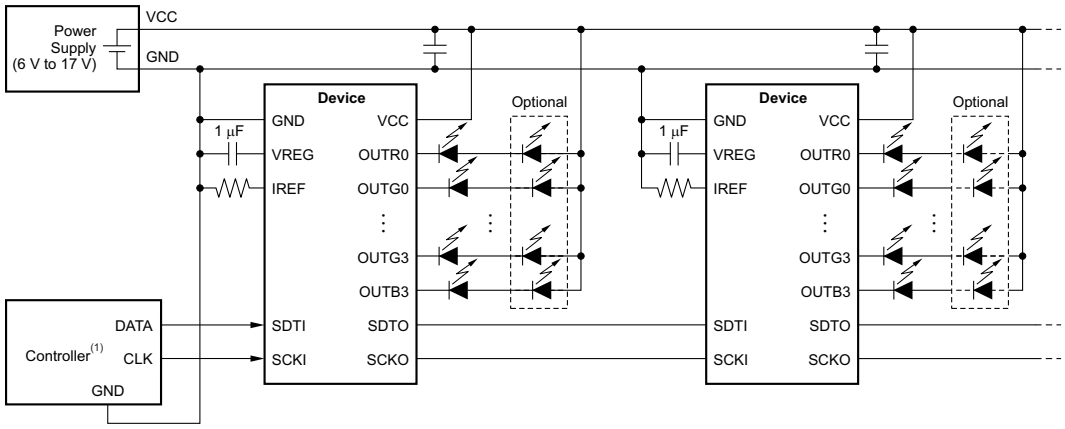
The TLC5971 device is a 12-channel, constant-current sink driver. Each output channel has individually adjustable currents with 65536 PWM grayscale (GS) steps. Also, each color group can be controlled by 128 constant-current sink steps with the global brightness control (BC) function. GS control and BC are accessible through a two-wire signal interface. The maximum current value for each channel is set by a single external resistor. All constant-current outputs are turned off when the IC is in an overtemperature condition.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC5971	HTSSOP (20)	6.50 mm × 4.40 mm
	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit Example (Internal Linear Regulator Using V_{CC} = 6 V to 17 V)



(1) The output voltage range is from 0 V to 3.3 V.

NOTE: The number of LEDs in series changes, depending on the VCC voltage.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2012) to Revision D — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (June 2012) to Revision C — **Page**

- Changed typical application circuit (internal linear regulator), added footnote 1 ... 1
- Changed typical application circuit (direct power), added footnote 1 ... 31
- Added typical application circuit example (direct power supplying V_{CC} = 3 V to 5.5 V, V_{LED} = 15 V), added footnote 1 ... 31

Changes from Revision A (December 2010) to Revision B — **Page**

- Changed I_{OLKG} parameter test conditions in *Electrical Characteristics* table ... 5
- Updated Figure 23 ... 15
- Changed bit 217 description in Table 5 ... 24

Changes from Original (August 2010) to Revision A — **Page**

- Changed Global Brightness Control bullet in *Features* ... 1
- Changed typical application circuit (internal linear regulator) ... 1
- Moved *Thermal Shutdown* and *Noise Reduction* sections ... 18
- Updated bit names for BCR, BCG, and BCB in Table 5 ... 24
- Changed typical application circuit (direct power) ... 31

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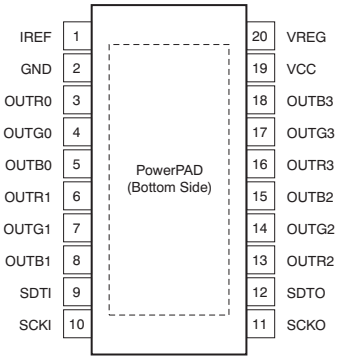
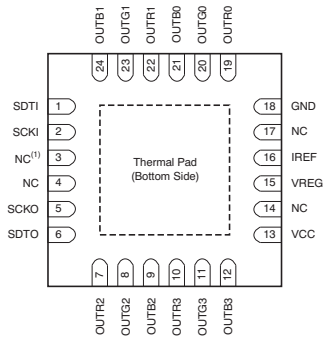
5 Pin Configuration and Functions

PWP Package
20-Pin HTSSOP
Bottom View



RGE Package
24-Pin VQFN
Bottom View



NC = not connected

Pin Functions

PIN			I/O	DESCRIPTION
NAME	PWP	RGE		
SDTI	9	1	I	Serial data input for the 224-bit shift register
SCKI	10	2	I	Serial data shift clock input. Data present on SDTI are shifted to the LSB of the 224-bit shift register with the SCKI rising edge Data in the shift register are shifted toward the MSB at each SCKI rising edge. The MSB data of the shift register appear on SDTO.
SDTO	12	6	O	Serial data output of the 224-bit shift register. SDTO is connected to the MSB of the 224-bit shift register. Data are clocked out at the SCKI rising edge.
SCKO	11	5	O	Serial data shift clock output. The input shift clock signal from SCKI is adjusted to the timing of the serial data output for SDTO and the signal is then output at SCKO.
VREG	20	15	I/O	Internal linear voltage regulator output. A decoupling capacitor of 1 µF must be connected. This output can be used for external devices as a 3.3-V power supply. This terminal can be connected with the VREG terminal of other devices to increase the supply current. Also, this pin can be supplied with 3 V to 5.5 V from an external power supply by connecting it to VCC.
IREF	1	16	I/O	Maximum current programming terminal. A resistor connected between IREF and GND sets the maximum current for every constant-current output. When this terminal is directly connected to GND, all outputs are forced off. The external resistor should be placed close to the device.
OUTR0	3	19	O	RED constant-current outputs. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
OUTR1	6	22	O	
OUTR2	13	7	O	
OUTR3	16	10	O	
OUTG0	4	20	O	GREEN constant-current outputs. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
OUTG1	7	23	O	
OUTG2	14	8	O	
OUTG3	17	11	O	
OUTB0	5	21	O	BLUE constant-current outputs. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
OUTB1	8	24	O	
OUTB2	15	9	O	
OUTB3	18	12	O	
VCC	19	13	—	Power-supply terminal

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Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	PWP	RGE		
GND, PowerPAD (PWP)	2	—	—	Power ground terminal
GND, exposed thermal pad (RGE)	—	18	—	
NC	—	3, 4, 14, 17	—	No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted.(1)(2)

		MIN	MAX	UNIT
Supply voltage, VCC		–0.3	18	V
Input voltage	IREF	–0.3	VREG + 0.3	V
	SDTI, SCKI	–0.3	VREG + 0.6	V
Output voltage	OUTR0 to OUTR3, OUTG0 to OUTG3, OUTB0 to OUTB3	–0.3	18	V
	SDTO, SCKO	–0.3	VREG + 0.3	V
	VREG	–0.3	6	V
Output current (DC)	OUTR0 to OUTR3, OUTG0 to OUTG3, OUTB0 to OUTB3		75	mA
	VREG		–30	mA
Operating junction temperature, $T_{J\ (max)}$			150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

at T_A = –40°C to +85°C, and VCC = 6 V to 17 V or VCC = VREG = 3 V to 5.5 V, unless otherwise noted.

		MIN	NOM	MAX	UNIT
DC CHARACTERISTICS					
VCC	Supply voltage, internal voltage regulator used	6		17	V
VREG	Supply voltage, VREG connected to VCC	3	3.3	5.5	V
V_O	Voltage applied to output (OUTR0 to OUTR3, OUTG0 to OUTG3, OUTB0 to OUTB3)			17	V
V_{IH}	High-level input voltage (SDTI, SCKI)	0.7 × VREG		VREG	V
V_{IL}	Low-level input voltage (SDTI, SCKI)	GND		0.3 × VREG	V
V_{IHYS}	Input voltage hysteresis (SDTI, SCKI)		0.2 × VREG		V
I_{OH}	High-level output current (SDTO)			–2	mA
I_{OL}	Low-level output current (SDTO)			2	mA
I_{OLC}	Constant output sink current (OUTR0 to OUTR3, OUTG0 to OUTG3, OUTB0 to OUTB3)			60	mA

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Recommended Operating Conditions (continued)

at T_A = –40°C to +85°C, and VCC = 6 V to 17 V or VCC = VREG = 3 V to 5.5 V, unless otherwise noted.

		MIN	NOM	MAX	UNIT
I_{REG}	Voltage regulator output current (VREG)			–25	mA
T_A	Operating free temperature range	–40		85	°C
T_J	Operating junction temperature	–40		125	°C
AC CHARACTERISTICS					
$f_{CLK\ (SCKI)}$	Data clock frequency and GS control clock frequency, SCKI	0.007		20	MHz
t_{WH}/t_{WL}	Pulse duration, SCKI	10			ns
t_{SU}	Setup time, SDTI – SCKI↑	5			ns
t_H	Hold time, SDTI – SCKI↑	3			ns

6.4 Thermal Information

THERMAL METRIC(1)		TLC5971		UNIT
		PWP (HTSSOP)	RGE (VQFN)	
		20 PINS	24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	68.6	38	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.2	40.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	19.3	10.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.7	10	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.8	2.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = –40°C to +85°C, V_{CC} = 6 V to 17 V or VCC = VREG = 3 V to 5.5 V, VLED = 5 V, and C_{VREG} = 1 µF, unless otherwise noted. Typical values are at T_A = 25°C and VCC = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, SDTO/SCKO	I_{OH} = –2 mA	VREG – 0.4		VREG	V
V_{OL}	Low-level output voltage, SDTO/SCKO	I_{OL} = 2 mA	0		0.4	V
I_I	Input current, SDTI/SCKI	V_I = VREG or GND	–1		1	µA
I_{CC}	Supply current	SDTI/SCKI = low, BLANK = 1, GSn = FFFFh, BCX = 7Fh, V_{OUTXn} = 1 V, R_{IREF} = 24 kΩ (I_{OLCMax} = 2 mA)		2	4	mA
I_{CC1}		SDTI/SCKI = low, BLANK = 1, GSn = FFFFh, BCX = 7Fh, V_{OUTXn} = 1 V, R_{IREF} = 1.6 kΩ (I_{OLCMax} = 30 mA)		6	9	mA
I_{CC2}		SDTI = 10 MHz, SCKI = 20 MHz, BLANK = 0, auto repeat enable, external GS clock selected, GSn = FFFFh, BCX = 7Fh, V_{OUTXn} = 1 V, R_{IREF} = 1.6 kΩ (I_{OLCMax} = 30 mA)		14	22	mA
I_{CC3}		SDTI = 10 MHz, SCKI = 20 MHz, BLANK = 0, auto repeat enable, external GS clock selected, GSn = FFFFh, BCX = 7Fh, V_{OUTXn} = 1 V, R_{IREF} = 0.82 kΩ (I_{OLCMax} = 60 mA)		21	36	mA
I_{OLC}	Constant output current, OUTXn	All OUTXn on, BCX = 7Fh, V_{OUTXn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 0.82 kΩ (I_{OLCMax} = 60 mA)	56.3	60.5	64.7	mA
I_{OLKG}	Leakage output current, OUTXn	All OUTXn off, BCX = 7Fh, V_{OUTXn} = 17 V, V_{OUTfix} = 17 V, R_{IREF} = 0.82 kΩ (I_{OLCMax} = 60 mA)			0.1	µA

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Electrical Characteristics (continued)

At T_A = –40°C to +85°C, V_{CC} = 6 V to 17 V or VCC = VREG = 3 V to 5.5 V, VLED = 5 V, and C_{VREG} = 1 µF, unless otherwise noted. Typical values are at T_A = 25°C and VCC = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔI_{OLC}	Constant-current error(1) (channel-to-channel in same color group), OUTXn	All OUTXn on, BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 1 V, R_{IREF} = 0.82 kΩ (I_{OLCMax} = 60 mA)	–3%	±1%	3%	
ΔI_{OLC1}	Constant current error(2) (device-to-device in same color group), OUTXn	All OUTXn on, BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 1V, R_{IREF} = 0.82 kΩ (I_{OLCMax} = 60 mA), at same grouped color output of OUTR0-3, OUTG0-3, and OUTB0-3	–4%	±1	4%	
ΔI_{OLC2}	Line regulation of constant-current output, OUTXn(3)	All OUTn on, BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 1 V, R_{IREF} = 0.82 kΩ (I_{OLCMax} = 60 mA)	–1	±0.5	1	%/V

(1)
The deviation of each output in the same color group (OUTR0-OUTR3 or OUTG0-OUTG3 or OUTB0-OUTB3) from the average current from the same color group. Deviation is calculated by Equation 1:

$$\Delta\,(\%) = \left(\frac{I_{OLCXn}}{\frac{(I_{OLCX0} + I_{OLCX1} + I_{OLCX2} + I_{OLCX3})}{4}} - 1 \right) \times 100$$

where
(a) X = R/G/B,
(b) n = 0-3. (1)

(2)
The deviation of each color group constant-current average from the ideal constant-current value. Deviation is calculated by Equation 2:

$$\Delta\,(\%) = \left(\frac{\frac{(I_{OLCX0} + I_{OLCX1} + I_{OLCX2} + I_{OLCX3})}{4} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

where
(a) X = R/G/B. (2)

Ideal current is calculated by Equation 3 for the OUTRn and OUTGn groups:

$$I_{OLCXn(IDEAL)}\,(mA) = 41 \times \left(\frac{1.21}{R_{IREF}\,(\Omega)} \right)$$

where
(a) X = R/G/B. (3)

(3)
Line regulation is calculated by Equation 4:

$$\Delta\,(\%/V) = \left(\frac{(I_{OLCXn} \text{ at VCC} = 5.5\text{ V}) - (I_{OLCXn} \text{ at VCC} = 3\text{ V})}{(I_{OLCXn} \text{ at VCC} = 3\text{ V})} \right) \times \frac{100}{5.5\text{ V} - 3\text{ V}}$$

where
(a) X = R/G/B,
(b) n = 0-3. (4)

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Electrical Characteristics (continued)

At T_A = –40°C to +85°C, V_{CC} = 6 V to 17 V or VCC = VREG = 3 V to 5.5 V, VLED = 5 V, and C_{VREG} = 1 µF, unless otherwise noted. Typical values are at T_A = 25°C and VCC = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔI_{OLC3}	Load regulation of constant-current output, OUTXn[4]	All OUTn on, BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 1 V, R_{IREF} = 0.82 kΩ (I_{OLCMax} = 60 mA)	–3	±1	3	%/V
T_{TSD}	Thermal shutdown temperature	Junction temperature[5]	150	165	180	°C
T_{HYS}	Thermal shutdown hysteresis	Junction temperature[5]	5	10	20	°C
V_{IREF}	Reference voltage output, IREF	R_{IREF} = 0.82 kΩ	1.18	1.21	1.24	V
V_{REG}	Linear regulator output voltage, VREG	VCC = 6 V to 17 V, IREG = 0 mA to –25 mA	3.1	3.3	3.5	V
ΔV_{REG}	Line regulation of linear regulator, VREG	VCC = 6 V to 17 V, IREG = 0 mA			90	mV
ΔV_{REG1}	Load regulation of linear regulator, VREG	VCC = 12 V, IREG = 0 mA to –25 mA			120	mV
V_{STR}	Undervoltage lockout release, VREG		2.5	2.7	2.9	V
V_{HYS}	Undervoltage lockout hysteresis, VREG		300	400	500	mV

(4)

Load regulation is calculated by Equation 5:

$$\Delta\ (\%/V) = \left(\frac{(I_{OLCXn} \text{ at } V_{OUTXn} = 3\ V) - (I_{OLCXn} \text{ at } V_{OUTXn} = 1\ V)}{(I_{OLCXn} \text{ at } V_{OUTXn} = 1\ V)} \right) \times \frac{100}{3\ V - 1\ V}$$

where
(a) X = R/G/B,
(b) n = 0-3. (5)

(5) Not tested, specified by design.

6.6 Switching Characteristics

At T_A = –40°C to +85°C, V_{CC} = 6 V to 17 V or VCC = VREG = 3 V to 5.5 V, C_{VREG} = 1 µF, C_L = 15 pF, R_L = 68 Ω, and VLED = 5 V, unless otherwise noted. Typical values are at T_A = 25°C and VCC = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{R0}	Rise time, SDTO/SCKO			3	10	ns
t_{R1}	Rise time, OUTXn	BCX = 7Fh		5	15	ns
t_{F0}	Fall time, SDTO/SCKO			3	10	ns
t_{F1}	Fall time, OUTXn	BCX = 7Fh		15	25	ns
t_{D0}	Propagation delay	SCKI↑ to SDTO↑↓	10	25	60	ns
t_{D1}		SCKI↑ to SCKO↑	5	15	40	ns
t_{D2}[1]		SCKO↑ to SDTO↑↓	5	10	20	ns
t_{D3}		SCKI↑ to OUTRn↑↓, BLANK = 0, BCXn = 7Fh, OUTTMG = 1 Or SCKI↓ to OUTRn↑↓, BLANK = 0, BCXn = 7Fh, OUTTMG = 0	10	25	60	ns
t_{D4}		SCKI↑ to OUTGn↑↓, BLANK = 0, BCXn = 7Fh, OUTTMG = 1 Or SCKI↓ to OUTGn↑↓, BLANK = 0, BCXn = 7Fh, OUTTMG = 0	25	50	90	ns
t_{D5}		SCKI↑ to OUTBn↑↓, BLANK = 0, BCXn = 7Fh, OUTTMG = 1 Or SCKI↓ to OUTBn↑↓, BLANK = 0, BCXn = 7Fh, OUTTMG = 0	40	75	120	ns
t_{D6}[2]		Last SCKI↑ to internal latch pulse genaration	$8/f_{OSC}$		$16384/f_{OSC}$	s
$t_{W(SCKO)}$	Shift clock output one pulse width	SCKO↑ to SCKO↓	12	25	35	ns
f_{OSC}	Internal oscillator frequency		6	10	12	MHz

(1) The propagation delays are calculated by $t_{D2} = t_{D0} - t_{D1}$.
(2) The generation timing of the internal latch pulse changes depending on the SCKI clock frequency; see the *Internal Latch Pulse Generation Timing* section.

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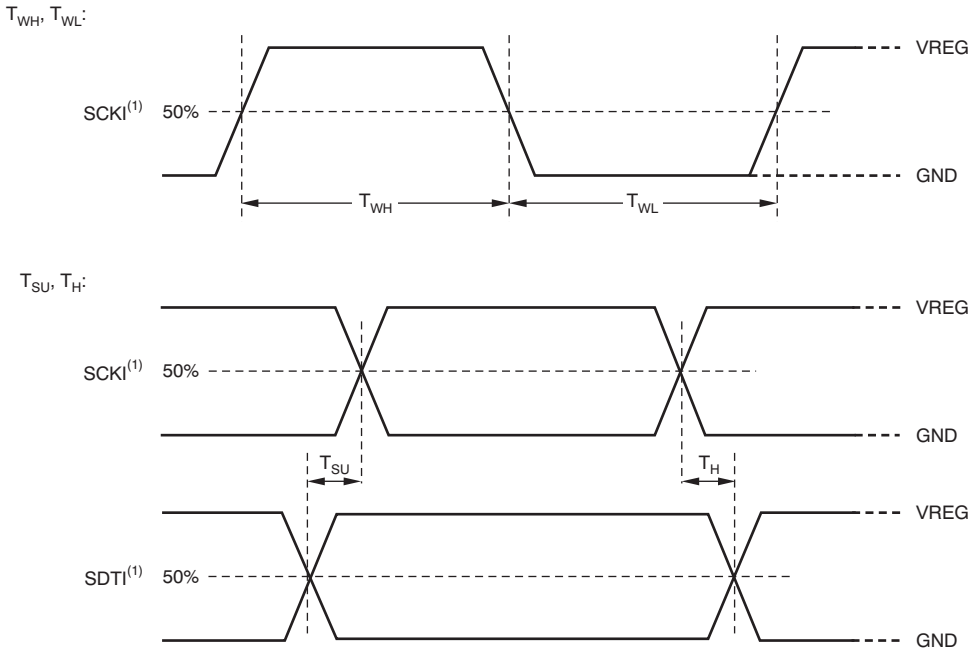
6.7 Dissipation Ratings

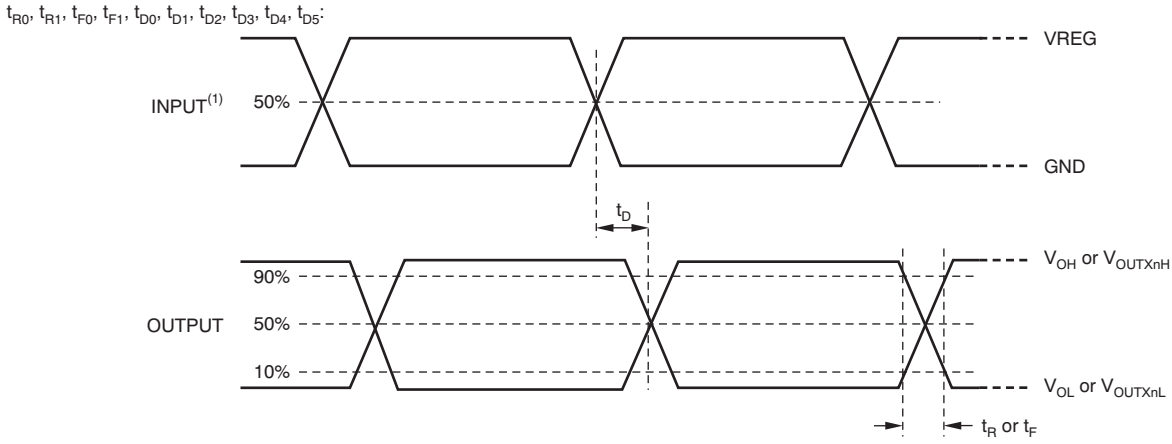
PACKAGE	DERATING FACTOR ABOVE T_A = 25°C	POWER RATING T_A < 25°C	POWER RATING T_A = 70°C	POWER RATING T_A = 85°C
HTSSOP 20-pin with PowerPAD soldered(1)	25.7 mW/°C	3121 mW	1998 mW	1623 mW
QFN 24-pin exposed thermal pad soldered(2)	24.8 mW/°C	3106 mW	1988 mW	1615 mW

(1) With PowerPAD soldered onto copper area on TI recommended printed circuit board (PCB); 2-oz. copper. For more information, see application report *PowerPAD Thermally-Enhanced Package* (SLMA002) available for download at www.ti.com.
(2) The package thermal impedance is calculated in accordance with JESD51-5.



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 1. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 2. Output Timing

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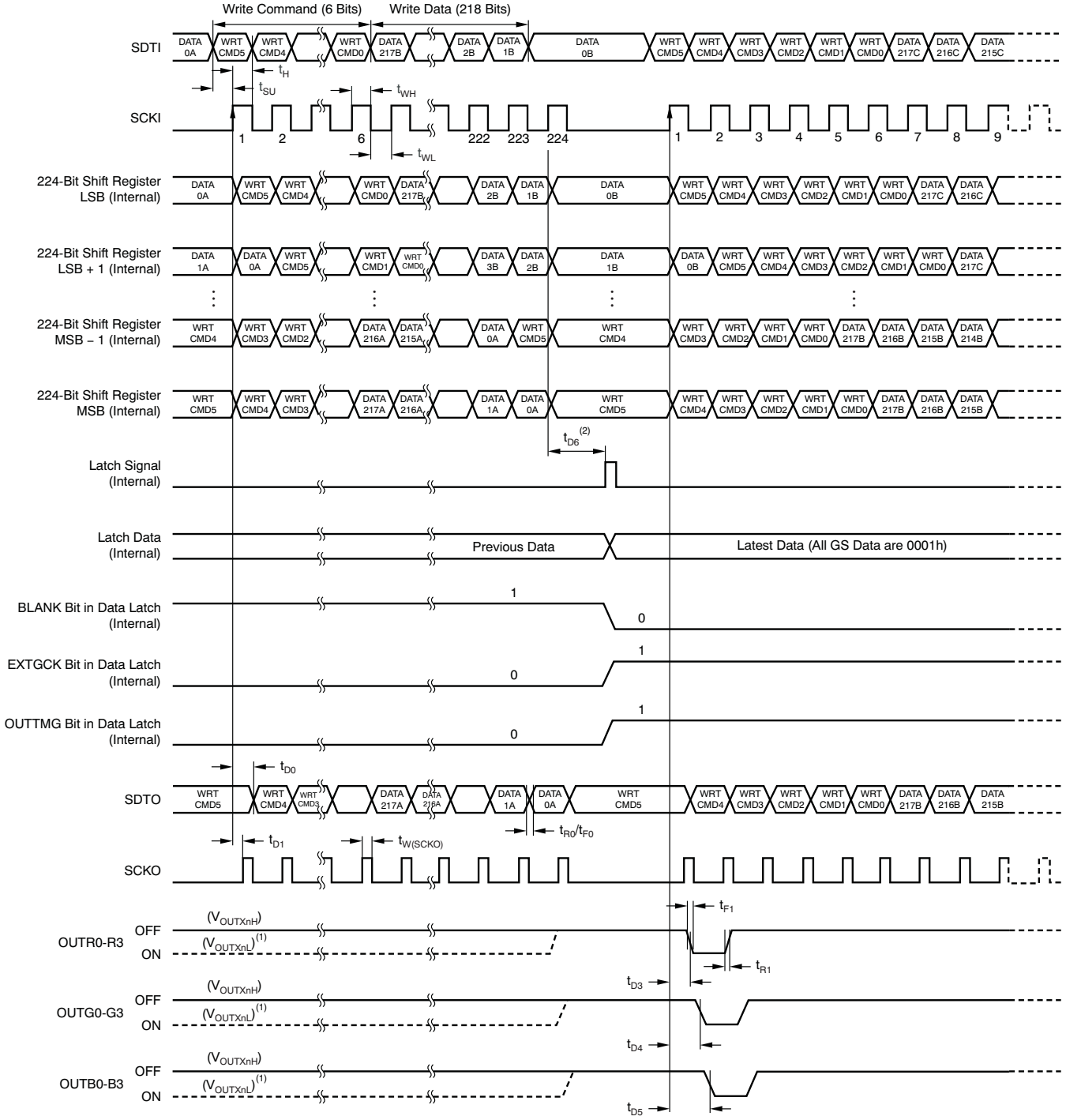
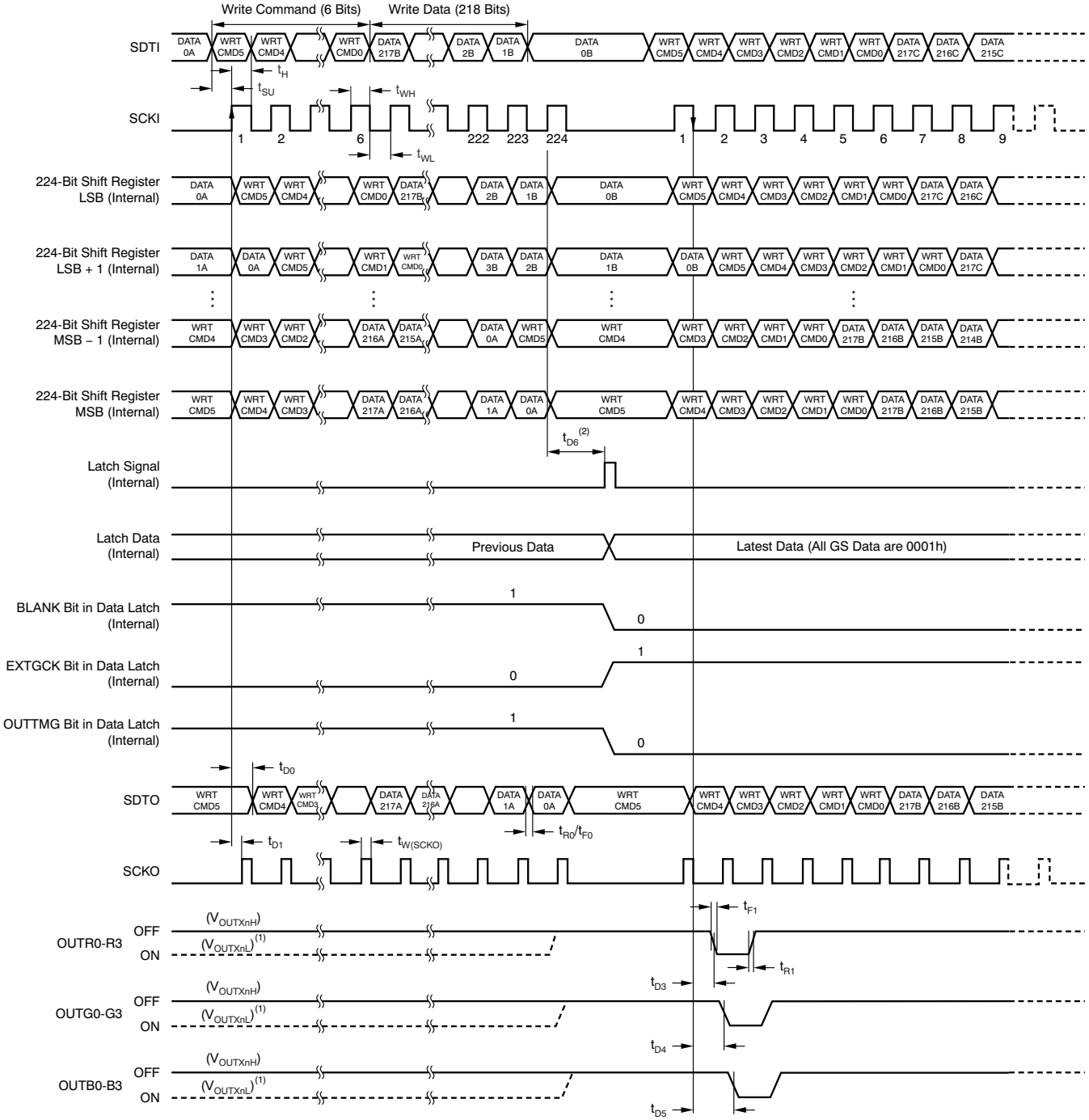


(1) OUTXn ON-OFF timing depends on previous GS data in the 218-bit data latch.

(2) The propagation delay time shows the period from the rising edge of the last SCKI, not the 224th SCKI to the internal latch signal generation.

Figure 3. Data Write and OUTXn Switching Timing (OUTTMG = 1)



(1) OUTXn ON-OFF timing depends on previous GS data in the 218-bit data latch.

(2) The propagation delay time shows the period from the rising edge of the last SCKI, not the 224th SCKI to the internal latch signal generation.

Figure 4. Data Write and OUTXn Switching Timing (OUTTMG = 0)

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6.8 Typical Characteristics

At T_A = 25°C and VCC = 24 V, unless otherwise noted.

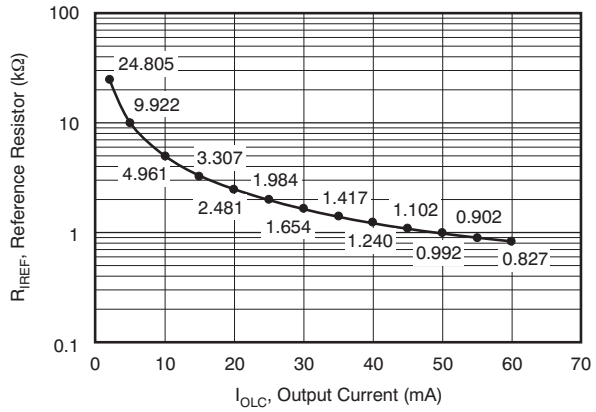

Figure 5. Reference Resistor vs Output Current

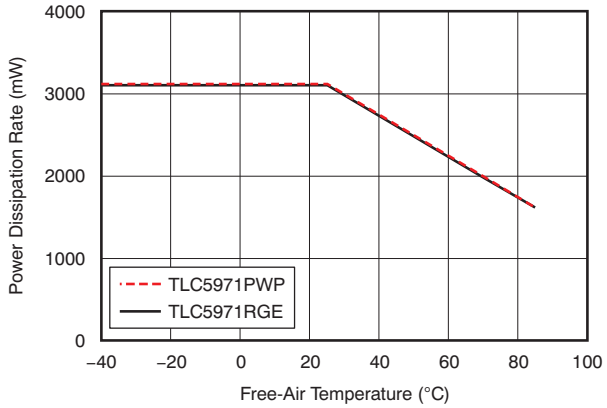

Figure 6. Power Dissipation vs Temperature

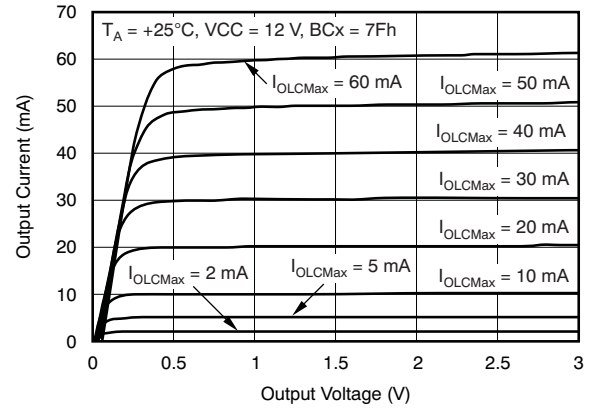

Figure 7. Output Current vs Output Voltage

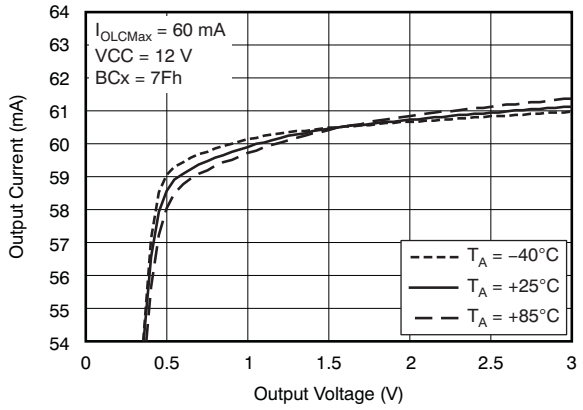

Figure 8. Output Current vs Output Voltage

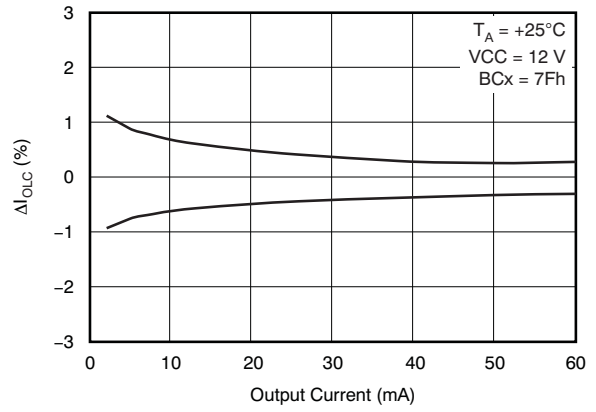

Figure 9. Constant-Current Error vs Output Current (Channel-to-Channel in Color Group)

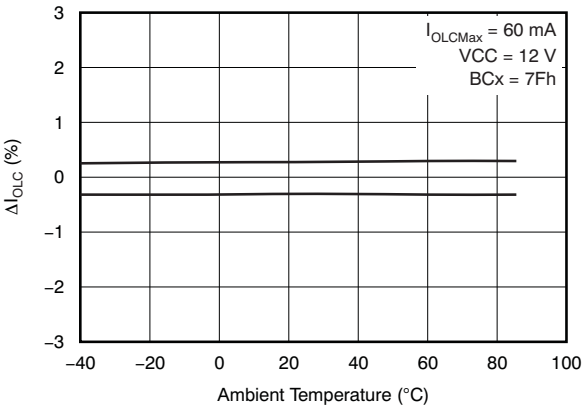

Figure 10. Constant-Current Error vs Ambient Temperature (Channel-to-Channel in Color Group)

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Typical Characteristics (continued)

At T_A = 25°C and VCC = 24 V, unless otherwise noted.

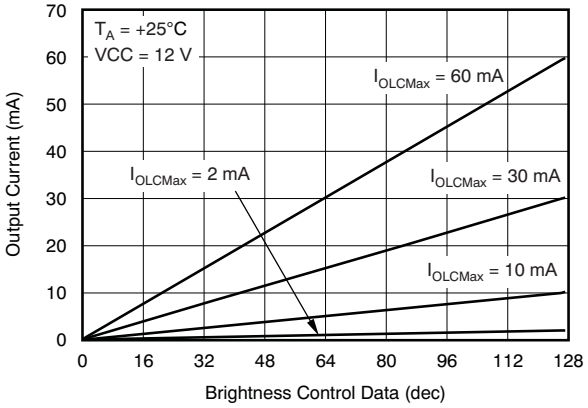

Figure 11. Global Brightness Control Linearity

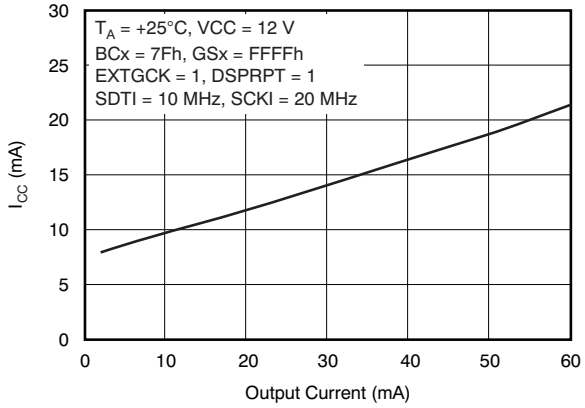

Figure 12. Supply Current vs Output Current

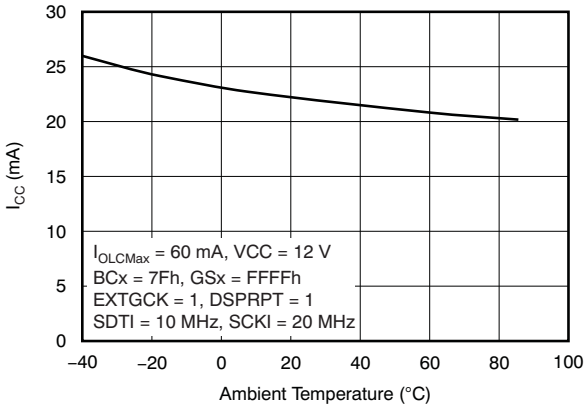

Figure 13. Supply Current vs Ambient Temperature

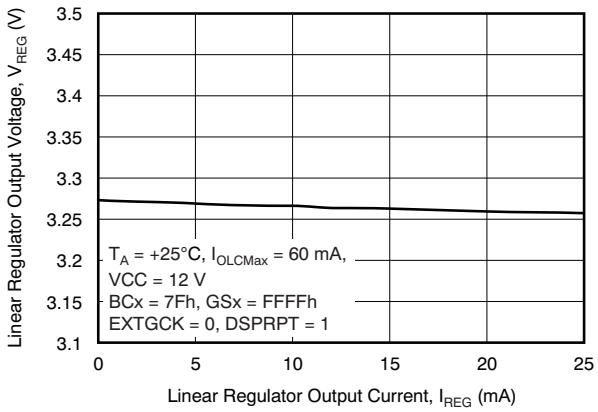

Figure 14. Linear Regulator Output Voltage vs Linear Regulator Output Current

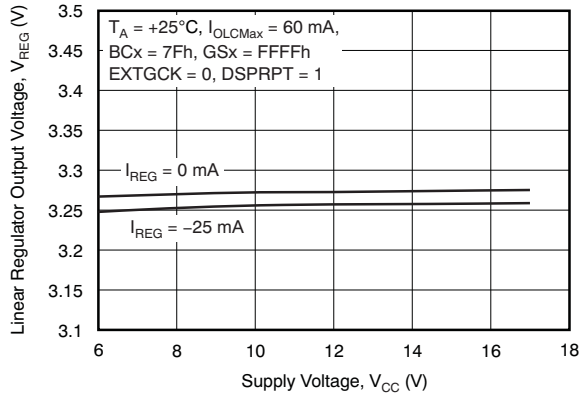

Figure 15. Linear Regulator Output Voltage vs Supply Voltage

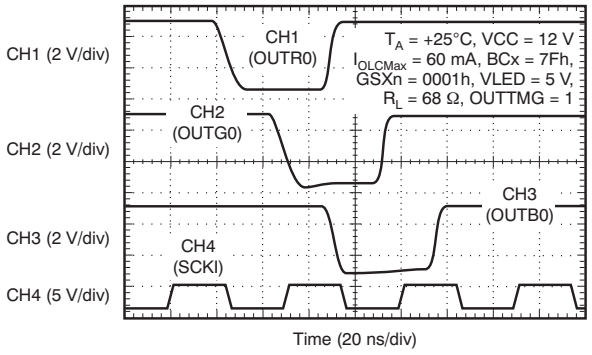

Figure 16. Constant-Current Output Voltage Waveform

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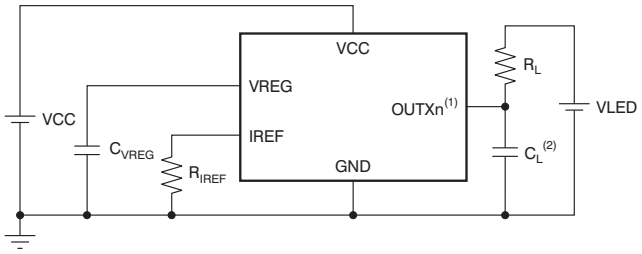
7 Parametric Measurement Information

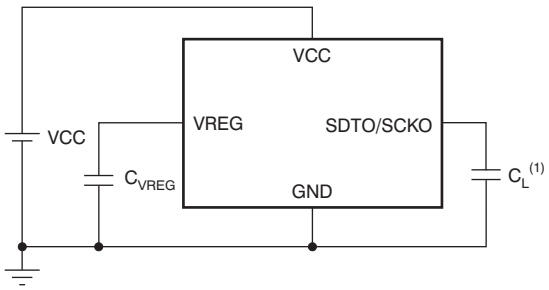
7.1 Test Circuits



(1) X = R/G/B, n = 0-3.

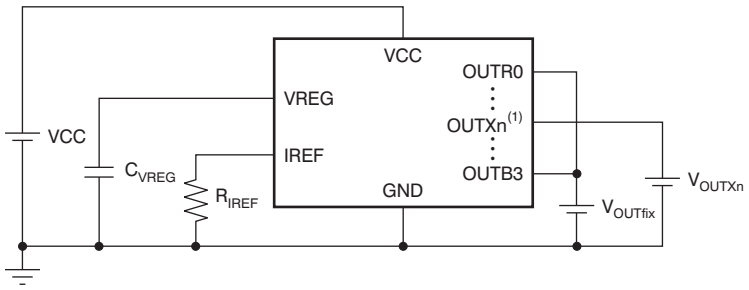
(2) C_L includes measurement probe and stray capacitance.

Figure 17. Rise/Fall Time Test Circuit for OUTXn



(1) C_L includes measurement probe and stray capacitance.

Figure 18. Rise/Fall Time Test Circuit for SDTO/SCKO



(1) X = R/G/B, n = 0-3.

Figure 19. Constant-Current Test Circuit for OUTXn

7.2 Pin Equivalent Input and Output Schematics

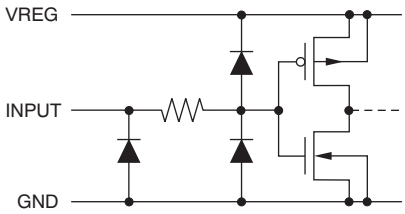


Figure 20. SDTI/SCKI

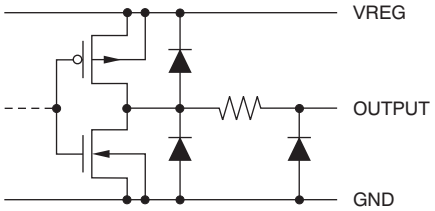
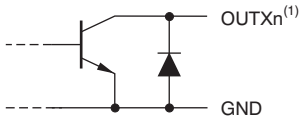


Figure 21. SDTO/SCKO



(1) X = R/G/B, n = 0-3.

Figure 22. OUTR0 Through OUTB3

8 Detailed Description

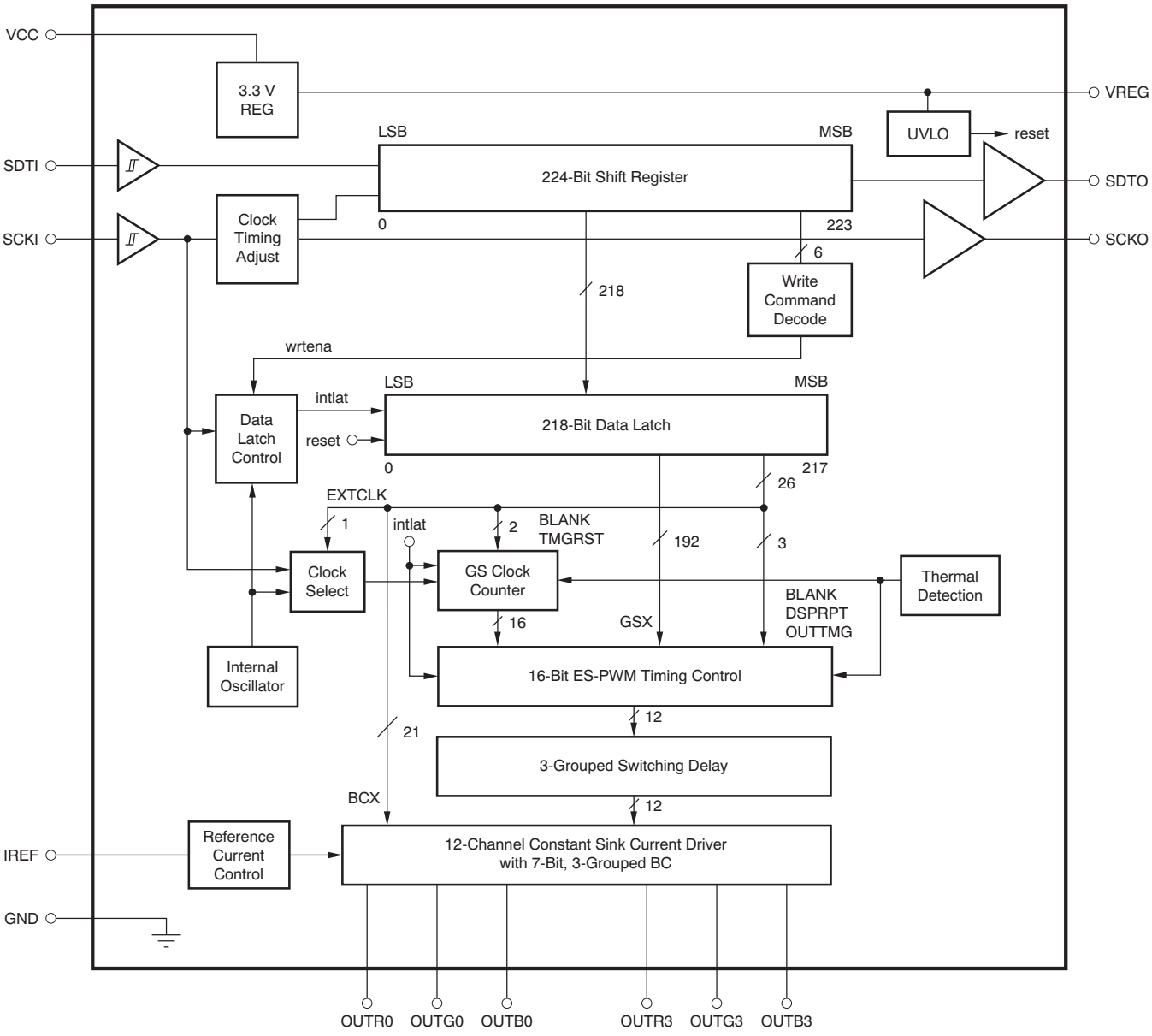
8.1 Overview

The TLC5971 is a 12-channel constant current sink driver. Each channel has an individually-adjustable, 65535-step, pulse width modulation (PWM) grayscale (GS) control. Each color has a 128-step brightness control (BC). GS data and BC data are input through a serial single-wire interface port.

The TLC5971 has a 60-mA current capability. The maximum current value of each channel is determined by the external resistor. The TLC5971 can work without external CLK signals since it can select to use internal oscillator or external GS clock.

The TLC5971 is integrated with a linear regulator that can be used for higher VCC power-supply voltage from 6 V to 17 V.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Auto Display Repeat Function

This function repeats the total display period without a BLANK bit change, as long as the GS reference clock is available. This function can be enabled or disabled with DSPRPT (bit 214) in the data latch. When the DSPRPT bit is 1, this function is enabled and the entire display period repeats without a BLANK bit data change. When the DSPRPT bit is 0, this function is disabled and the entire display period executes only once after the BLANK bit is set to 0 or the internal latch pulse is generated when the display timing reset function is enabled. Figure 23 shows the auto display repeat operation timing.

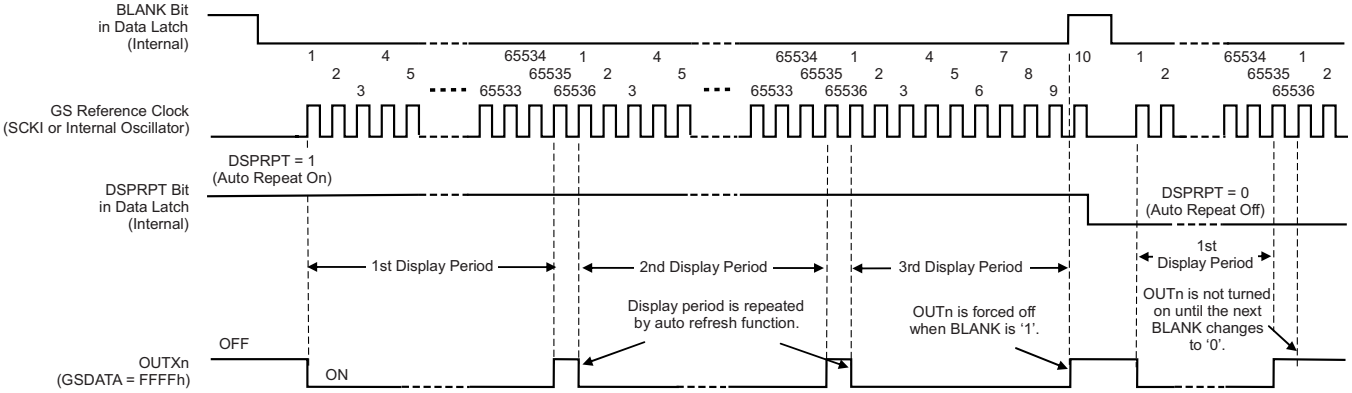

Figure 23. Auto Repeat Display Function

8.3.2 Display Timing Reset Function

This function allows the display timing to be initialized using the internal latch pulse, as shown in Figure 24. This function can be enabled or disabled by TMGRST (bit 215) in the data latch. When the TMGRST bit is 1, the GS counter is reset to 0 and all outputs are forced off when the internal latch pulse is generated. This function is the same when the BLANK bit changes (such as from 0 to 1 and from 1 to 0). Therefore, the BLANK bit does not need to be controlled from an external controller to restart the PWM control from the next GS reference clock rising edge. When this bit is 0, the GS counter is not reset and no output is forced off even if the internal latch pulse is generated. Figure 24 shows the display timing reset operation.

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Feature Description (continued)

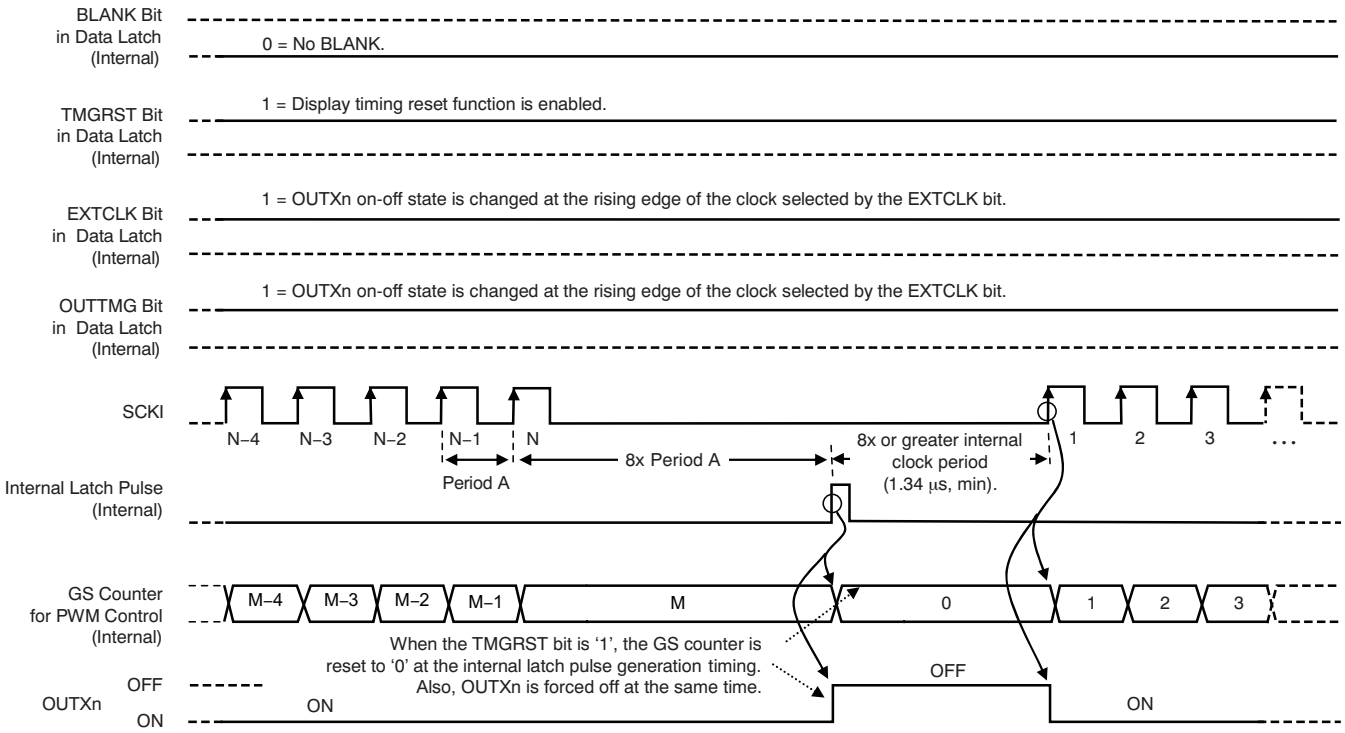

Figure 24. Display Timing Reset Function

8.3.3 Output Timing Select Function

This function selects the ON-OFF change timing of the constant-current outputs (OUTXn) set by OUTTMG (bit 217) in the data latch. When this bit is 1, OUTXn are turned on or off at the rising edge of the selected GS reference clock. When this bit is 0, OUTXn are turned on or off at the falling edge of the selected clock. Electromagnetic interference (EMI) of the total system can be reduced using this bit setting. For example, when the odd number of devices in the system have this bit set to 0 and the even number of devices in the system have this bit set to 1, EMI is reduced because the devices change the OUTXn status at a deferent timing. Figure 25 and Figure 26 show the output switching timing when the OUTTMG bit is 1 and 0, respectively.

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Feature Description (continued)

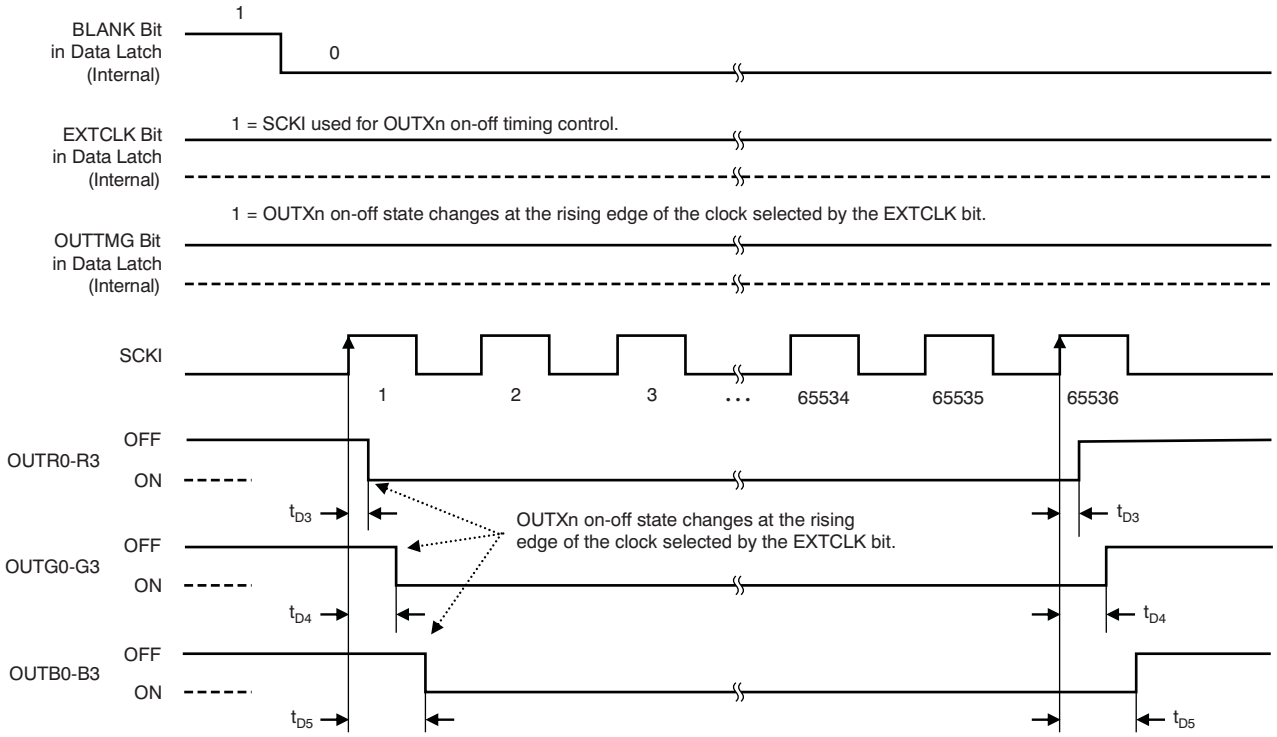

Figure 25. Output ON-OFF Timing With Four-Channel Grouped Delay (OUTTMG = 1)

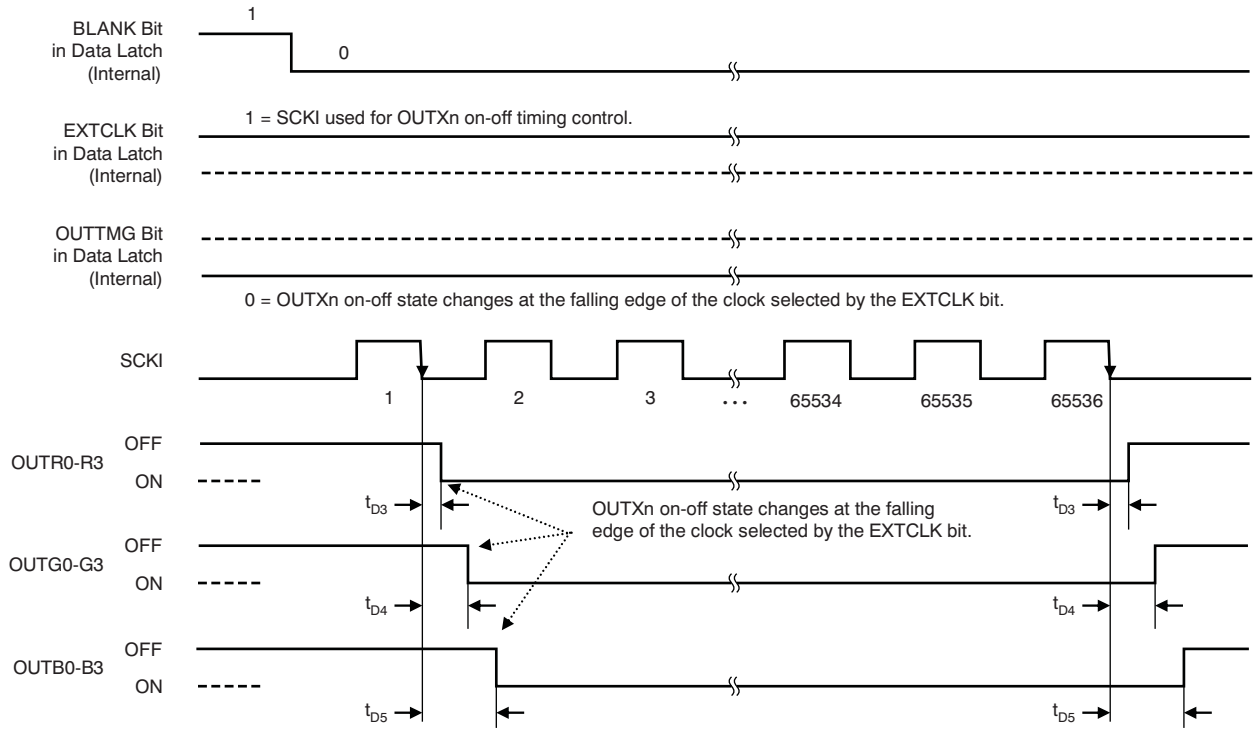

Figure 26. Output ON-OFF Timing With Four-Channel Grouped Delay (OUTTMG = 0)

Feature Description (continued)

8.3.4 Thermal Shutdown

The thermal shutdown (TSD) function turns off all IC constant-current outputs when the junction temperature (T_J) exceeds the threshold (T_{TSD} = 165°C, typical). When the junction temperature drops below (T_{TSD} – T_{HYS}), the output control starts at the first GS clock in the next display period.

8.3.5 Noise Reduction

Large surge currents may flow through the IC and the board if all 12 outputs turn on simultaneously at the start of each GS cycle. These large current surges could induce detrimental noise and EMI into other circuits. The TLC5971 turns on the outputs for each color group independently with a 25 ns (typical) rise time. The output current sinks are grouped into three groups. The first group that is turned on/off are OUTR0-3; the second group that is turned on/off are OUTG0-3; and the third group is OUTB0-3. However, the state of each output is controlled by the selected GS clock; see the *Output Timing Select Function* section.

8.4 Device Functional Modes

8.4.1 Maximum Constant Sink Current Setting

The maximum constant sink current value for each channel, I_{OLCMax}, is programmed through a single resistor, R_{IREF}, placed between IREF and GND. The desired value can be calculated with Equation 6:

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLCMax}\ (mA)} \times 41 \quad (6)$$

where:

V_{IREF} = the internal reference voltage on the IREF pin (1.21 V, typically, when the the global brightness control data are at maximum),

I_{OLCMax} = 2 mA to 60 mA.

I_{OLCMax} is the maximum current for each output. Each output sinks the I_{OLCMax} current when it is turned on and global brightness control data (BC) are set to the maximum value of 7Fh (127d).

R_{IREF} must be between 0.82 kΩ and 24.8 kΩ to hold I_{OLCMax} between 60 mA (typical) and 2 mA (typical). Otherwise, the output may be unstable. Output currents lower than 2 mA can be achieved by setting I_{OLCMax} to 2 mA or higher and then using global brightness control to lower the output current. The constant-current sink values for specific external resistor values are shown in Figure 5 and Table 1.

Table 1. Maximum Constant-Current vs External Resistor Value

I_{OLCMax} (mA)	R_{IREF} (kΩ, Typical)
60	0.827
55	0.902
50	0.992
45	1.1
40	1.24
35	1.42
30	1.65
25	1.98
20	2.48
15	3.31
10	4.96
5	9.92
2	24.8

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8.5 Programming

8.5.1 Global Brightness Control (BC) Function (Sink Current Control)

The TLC5971 has the capability to adjust all output currents of each color group (OUTR0-3, OUTG0-3, and OUTB0-3) to the same current value. This function is called *global brightness (BC) control*. The BC data are seven bits long, which allows each color group output current to be adjusted in 128 steps from 0% to 100% of the maximum output current, I_{OLCMax}. The BC data are set through the serial interface. When the BC data are changed, the output current is changed immediately.

When the IC is powered on, all outputs are forced off by BLANK (bit 213). BLANK initializes in the data latch but the data in the 224-bit shift register and the 218-bit data latch are not set to a default value, except for the BLANK bit. Therefore, BC data must be written to the data latch when BLANK is set to 0.

Equation 7 determines each color group maximum output sink current:

$$I_{OUT}\ (mA) = I_{OLCMax}\ (mA) \times \left[\frac{BCX}{127d}\right] \quad (7)$$

Where:

I_{OLCMax} = the maximum channel current for each channel determined by R_{IREF}

BC = the global brightness control value in the data latch for the specific color group

(BCX = 0d to 127d, X = R/G/B)

Table 2 summarizes the BC data value versus the output current ratio and set current value.

Table 2. BC Data vs Current Ratio and Set Current Value

BC DATA (BINARY)	BC DATA (DECIMAL)	BC DATA (HEX)	OUTPUT CURRENT RATIO TO I_{OLCMax} (%, TYPICAL)	60 mA I_{OLCMax} (mA, TYPICAL)	2 mA I_{OLCMax} (mA, TYPICAL)
000 0000	0	00	0	0	0
000 0001	1	01	0.8	0.47	0.02
000 0010	2	02	1.6	0.94	0.03
—	—	—	—	—	—
111 1101	125	7D	98.4	59.06	1.97
111 1110	126	7E	99.2	59.53	1.98
111 1111	127	7F	100	60	2

8.5.2 Grayscale (GS) Function (PWM Control)

The TLC5971 can adjust the brightness of each output channel using the enhanced spectrum pulse width modulation (ES-PWM) control scheme. The PWM bit length for each output is 16 bits. The use of the 16-bit length results in 65536 brightness steps from 0% to 100% brightness.

The PWM operation for all color groups is controlled by a 16-bit grayscale (GS) counter. The GS counter increments on each rising or falling edge of the external or internal GS reference clock that is selected by OUTTMG (bit 217) and EXTGCK (bit 216) in the data latch. When the external GS clock is selected, the GS counter uses the SCKI clock as the grayscale clock. The GS counter is reset to 0000h and all outputs are forced off when BLANK (bit 213) is set to 1 in the data latch and the counter value is held at 0 while BLANK is 1, even if the GS reference clock is toggled in between.

Equation 8 calculates each output (OUTXn) total on-time (t_{OUT_ON}):

$$t_{OUT_ON}\ (ns) = t_{GSCLK}\ (ns) \times GSXn \quad (8)$$

Where:

t_{GSCLK} = one period of the selected GS reference clock

(internal clock = 100ns typical, external clock = the period of SCKI)

GSXn = the programmed GS value for OUTXn (0d to 65535d)

Table 3 summarizes the GS data values versus the output total ON-time and duty cycle. When the IC is powered up, BLANK (bit 213) is set to 1 to force all outputs off; however, the 224-bit shift register and the 218-bit data latch are not set to default values. Therefore, the GS data must be written to the data latch when BLANK (bit 213) is set to 0.

Table 3. Output Duty Cycle and Total On-Time versus GS Data

GS DATA (DECIMAL)	GS DATA (HEX)	ON-TIME DUTY (%)	GS DATA (DECIMAL)	GS DATA (HEX)	ON-TIME DUTY (%)
0	0	0	32768	8000	50.001
1	1	0.002	32769	8001	50.002
2	2	0.003	32770	8002	50.004
3	3	0.005	32771	8003	50.005
—	—	—	—	—	—
8191	1FFF	12.499	40959	9FFF	62.499
8192	2000	12.5	40960	A000	62.501
8193	2001	12.502	40961	A001	62.502
—	—	—	—	—	—
16383	3FFF	24.999	49149	BFFF	74.997
16384	4000	25	49150	C000	74.998
16385	4001	25.002	49151	C001	75
—	—	—	—	—	—
24575	5FFF	37.499	57343	DFFF	87.5
24576	6000	37.501	57344	E000	87.501
24577	6001	37.502	57345	E001	87.503
—	—	—	—	—	—
32765	7FFD	49.996	65533	FFFD	99.997
32766	7FFE	49.998	65534	FFFE	99.998
32767	7FFF	49.999	65535	FFFF	100

8.5.3 Enhanced Spectrum (ES) PWM Control

Enhanced spectrum (ES) PWM has the total display period divided into 128 display segments. The total display period refers the period between the first grayscale clock input to the 65536th grayscale clock input after BLANK (bit 213) is set to 0. Each display period has 512 grayscale values, maximum. Each output on-time changes depending on the grayscale data. Refer to Table 4 for sequence information and Figure 27 for timing information.

Table 4. ES-PWM Drive Turnon Time Length

GS DATA (DEC)	GS DATA (HEX)	OUTn DRIVER OPERATION
0	0000h	Does not turn on
1	0001h	Turns on during one GS clock period in the 1st display period
2	0002h	Turns on during one GS clock period in the 1st and 65th display period
3	0003h	Turns on during one GS clock period in the 1st, 33rd, and 65th display period
4	0004h	Turns on during one GS clock period in the 1st, 33rd, 65th, and 97th display period
5	0005h	Turns on during one GS clock period in the 1st, 17th, 33rd, 65th, and 97th display period
6	0006h	Turns on during one GS clock period in the 1st, 17th, 33rd, 65th, 81st, and 97th display period
—	—	The number of display periods that OUTXn is turned on during one GS clock is incremented by the GS data increasing in the following order. The order of display periods that the output turns on are: 1, 65, 33, 97, 17, 81, 49, 113, 9, 73, 41, 105, 25, 89, 57, 121, 5, 69, 37, 101, 21, 85, 53, 117, 13, 77, 45, 109, 29, 93, 61, 125, 3, 67, 35, 99, 19, 83, 51, 115, 11, 75, 43, 107, 27, 91, 59, 123, 7, 71, 39, 103, 23, 87, 55, 119, 15, 79, 47, 111, 31, 95, 63, 127, 2, 66, 34, 98, 18, 82, 50, 114, 10, 74, 42, 106, 26, 90, 58, 122, 6, 70, 38, 102, 22, 86, 54, 118, 14, 78, 46, 110, 30, 94, 62, 126, 4, 68, 36, 100, 20, 84, 52, 116, 12, 76, 44, 108, 28, 92, 60, 124, 8, 72, 40, 104, 24, 88, 56, 120, 16, 80, 48, 112, 32, 96, 64, and 128.

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Table 4. ES-PWM Drive Turnon Time Length (continued)

GS DATA (DEC)	GS DATA (HEX)	OUTn DRIVER OPERATION
127	007Fh	Turns on during one GS clock period in the 1st to 127th display period, but does not turn on in the 128th display period
128	0080h	Turns on during one GS clock period in all display periods (1st to 128th)
129	0081h	Turns on during two GS clock periods in the 1st display period and one GS clock period in the next display period
—	—	The number of display periods where OUTn is turned on for two GS clocks is incremented by the increased GS data similar to the previous case where the GS value is 1 trough 127
255	00FFh	Turns on during two GS clock periods in the 1st to 127th display period, but only turns on during one GS clock period in the 128th display period
256	0100h	Turns on during two GS clock periods in all display periods (1st to 128th)
257	0101h	Turns on during three GS clock periods in the 1st display period and two GS clock periods in the next display period
—	—	Display periods with OUTn turned on is incremented by the increased GS datasimilar to 0101h operation
65478	FEFFh	Turns on during 511 GS clock periods in the 1st to 127th display period, but only turns on 510 GS clock periods in the 128th display period
65280	FF00h	Turns on during 511 GS clock periods in all display periods (1st to 128th)
65281	FF01h	Turns on during 512 GS clock periods in the 1st display period and 511 GS clock periods in the 2nd to 128th display periods
—	—	—
65534	FFFEh	Turns on during 512 GS clock periods in the 1st to 63th and 65th to 127th display periods, and turns on 511 GS clock periods in the 64th and 128th display periods
65535	FFFFh	Turns on during 512 GS clock periods in the 1st to 127th display period, but only turns on 511 GS clock periods in the 128th display period

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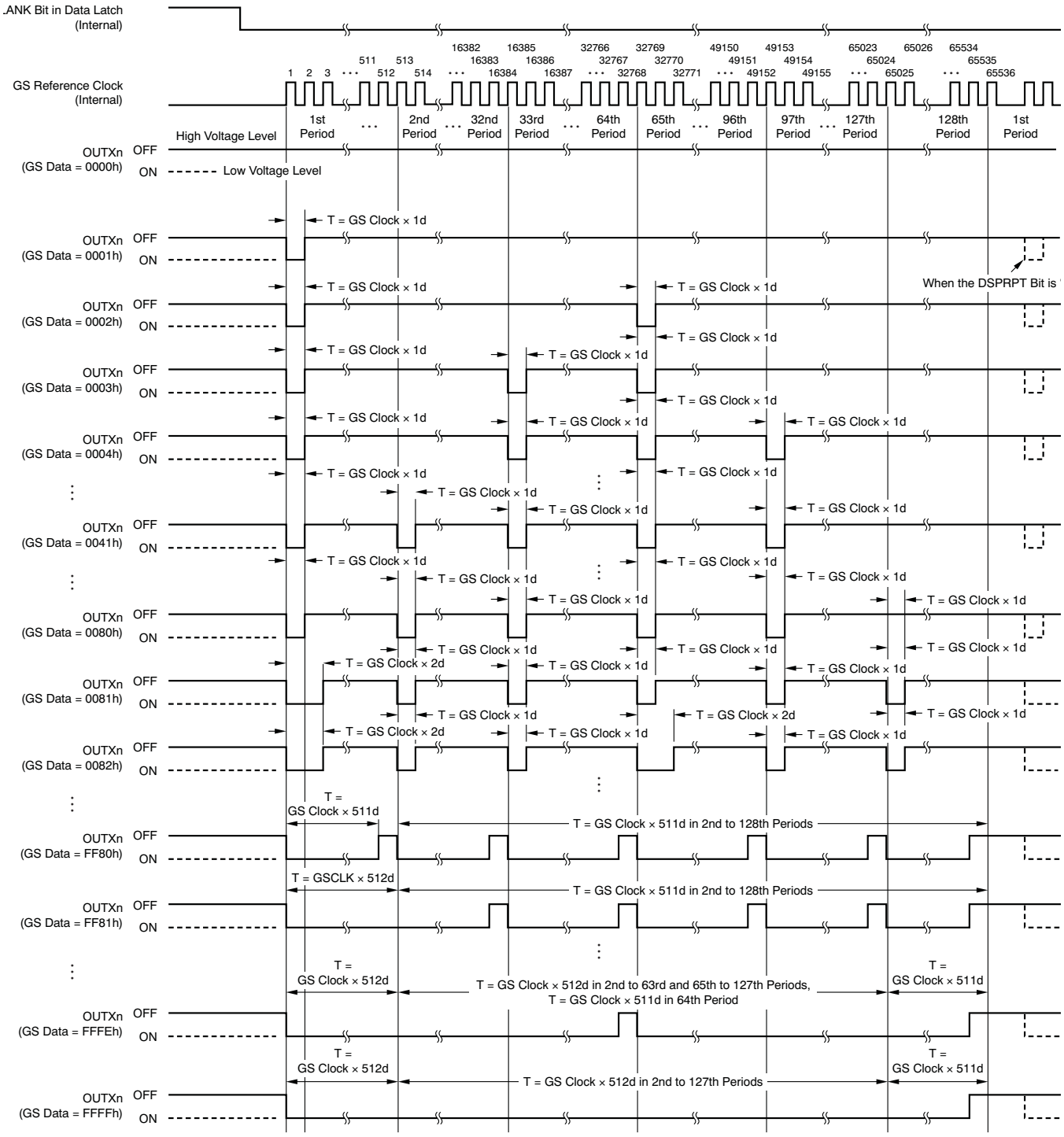

Figure 27. ES-PWM Operation

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8.5.4 Register and Data Latch Configuration

The TLC5971 has a 224-bit shift register and a 218-bit data latch that set grayscale (GS) data, global brightness control (BC), and function control (FC) data into the device. When the internal latch pulse is generated and the data of the six MSBs in the shift register are 25h, the 218 following data bits in the shift register are copied into the 218-bit data latch. If the data of the six MSBs is not 25h, the 218 data bits are not copied into the 218-bit data latch. The data in the data latch are used for GS, BC, and FC functions. Figure 28 shows the shift register and the data latch configuration.

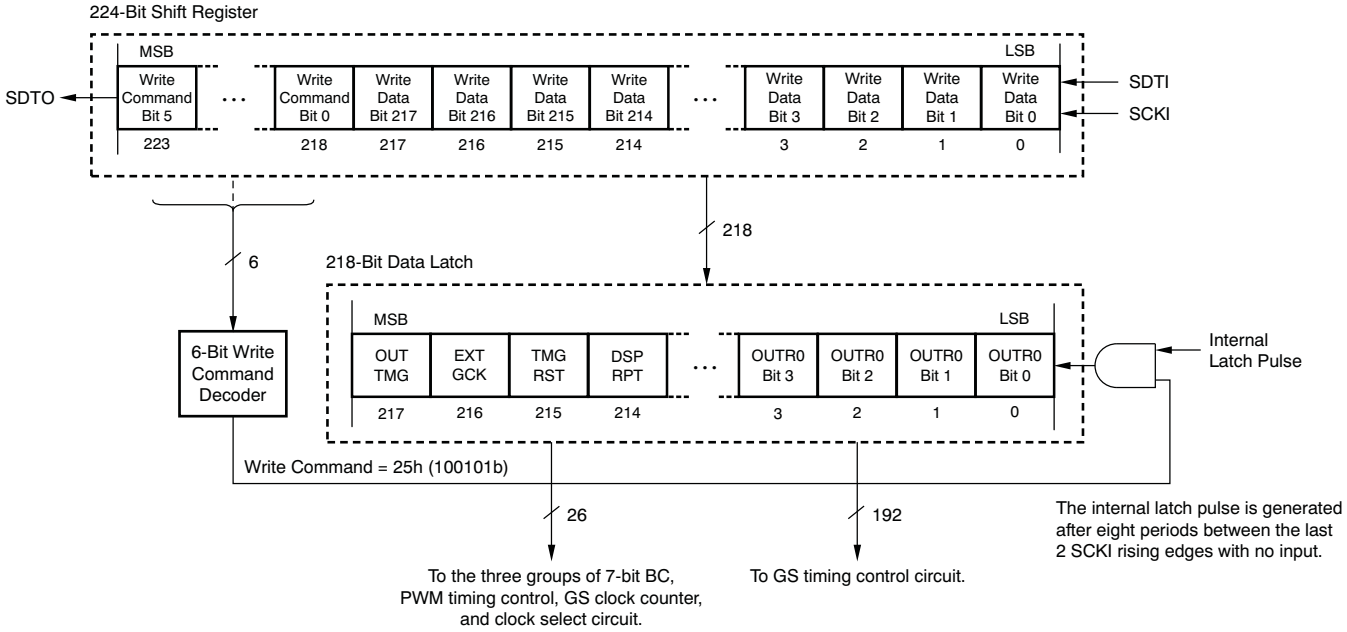

Figure 28. Common Shift Register and Control Data Latch Configuration

8.5.4.1 224-Bit Shift Register

The 224-bit shift register is used to input data from the SDTI pin with the SCKI clock into the TLC5971. The shifted data in this register is used for GS, BC, and FC. The six MSBs are used for the write command. The LSB of the register is connected to the SDTI pin and the MSB is connected to the SDTO pin. On each SCKI rising edge, the data on SDTI are shifted into the register LSB and all 224 bits are shifted towards the MSB. The register MSB is always connected to SDTO. When the device is powered up, the data in the 224-bit shift register is not set to any default value.

8.5.4.2 218-Bit Data Latch

The 218-bit data latch is used to latch the GS, BC, and FC data. The 218 LSBs in the 244-bit shift register are copied to the data latch when the internal latch pulse is generated with the 6-bit write command, 25h (100101b). When the device is powered up, the data in the latch are not reset except for BLANK (bit 213) which is set to 1 to force all outputs off. Therefore, GS, BC, and FC data must be set to the proper values before BLANK is set to 0. The 218-bit data latch configuration is shown in Figure 29 and the data bit assignment is shown in Table 5.

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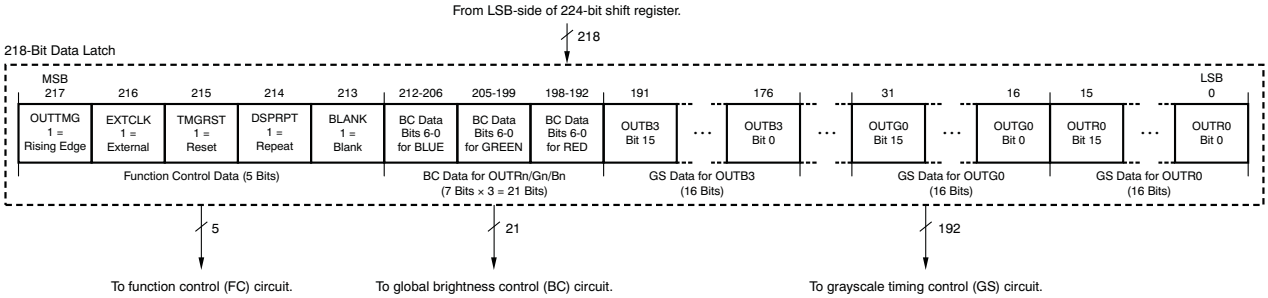

Figure 29. 218-Bit Data Latch Configuration

Table 5. Data Latch Bit Assignment

BIT NUMBER	BIT NAME	CONTROLLED CHANNEL/FUNCTIONS
15-0	GSR0	GS data bits 15 to 0 for OUTR0
31-16	GSG0	GS data bits 15 to 0 for OUTG0
47-32	GSB0	GS data bits 15 to 0 for OUTB0
63-48	GSR1	GS data bits 15 to 0 for OUTR1
79-64	GSG1	GS data bits 15 to 0 for OUTG1
95-80	GSB1	GS data bits 15 to 0 for OUTB1
111-96	GSR2	GS data bits 15 to 0 for OUTR2
127-112	GSG2	GS data bits 15 to 0 for OUTG2
143-128	GSB2	GS data bits 15 to 0 for OUTB2
159-144	GSR3	GS data bits 15 to 0 for OUTR3
175-160	GSG3	GS data bits 15 to 0 for OUTG3
191-176	GSB3	GS data bits 15 to 0 for OUTB3
198-192	BCR	BC data bits 6 to 0 for OUTR0-3
205-199	BCG	BC data bits 6 to 0 for OUTG0-3
212-206	BCB	BC data bits 6 to 0 for OUTB0-3
213	BLANK	Constant-current output enable bit in FC data (0 = output control enabled, 1 = blank). When this bit is 0, all constant-current outputs (OUTR0-OUTB3) are controlled by the GS PWM timing controller. When this bit is 1, all constant-current outputs are forced off. The GS counter is reset to 0, and the GS PWM timing controller is initialized. When the IC is powered on, this bit is set to 1.
214	DSPRPT	Auto display repeat mode enable bit in FC data (0 = disabled, 1 = enabled). When this bit is 0, the auto repeat function is disabled. Each constant-current output is only turned on once, according the GS data after BLANK is set to 0 or after the internal latch pulse is generated with the TMGRST bit set to 1. When this bit is 1, each output turns on and off according to the GS data every 65536 GS reference clocks.
215	TMGRST	Display timing reset mode enable bit in FC data (0 = disabled, 1 = enabled). When this bit is 1, the GS counter is reset to 0 and all constant-current outputs are forced off when the internal latch pulse is generated for data latching. This function is the same when BLANK is set to 0. Therefore, BLANK does not need to be controlled by an external controller when this mode is enabled. When this bit is 0, the GS counter is not reset and no output is forced off even if the internal latch pulse is generated.
216	EXTGCK	GS reference clock select bit in FC data (0 = internal oscillator clock, 1 = SCKI clock). When this bit is 1, PWM timing refers to the SCKI clock. When this bit is 0, PWM timing refers to the internal oscillator clock.
217	OUTTMG	GS reference clock edge select bit for OUTXn on-off timing control in FC data (0 = falling edge, 1 = rising edge). When this bit is 1, OUTXn are turned on or off at the rising edge of the selected GS reference clock. When this bit is 0, OUTXn are turned on or off at the falling edge of the selected clock.

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8.5.5 Internal Latch Pulse Generation Timing

The internal latch pulse is generated when the SCKI rising edge does not change for 8x the period between the last SCKI rising edge and the second to last SCKI rising edge if the data of the six MSBs in the 244-bit shift register are the command code 25h. The generation timing changes as a result of the SCKI frequency with the time range between 16384 times the internal oscillator period (2.74 ms), maximum, and 8x the internal oscillator period (666 ns), minimum. Figure 30 shows the internal latch pulse generation timing.

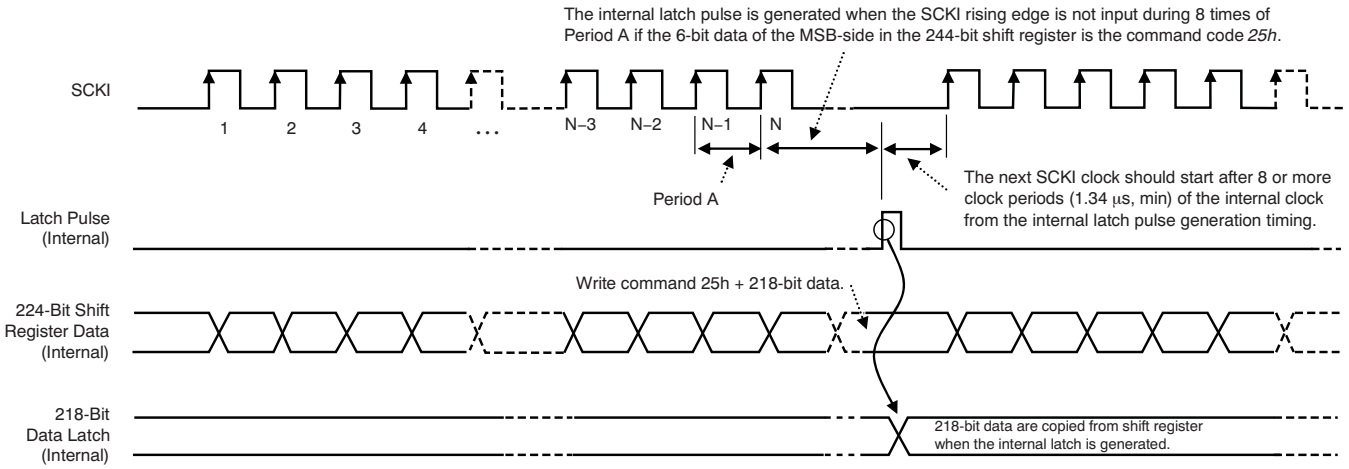


Figure 30. Data Latch Pulse Generation Timing

9 Application and Implementation

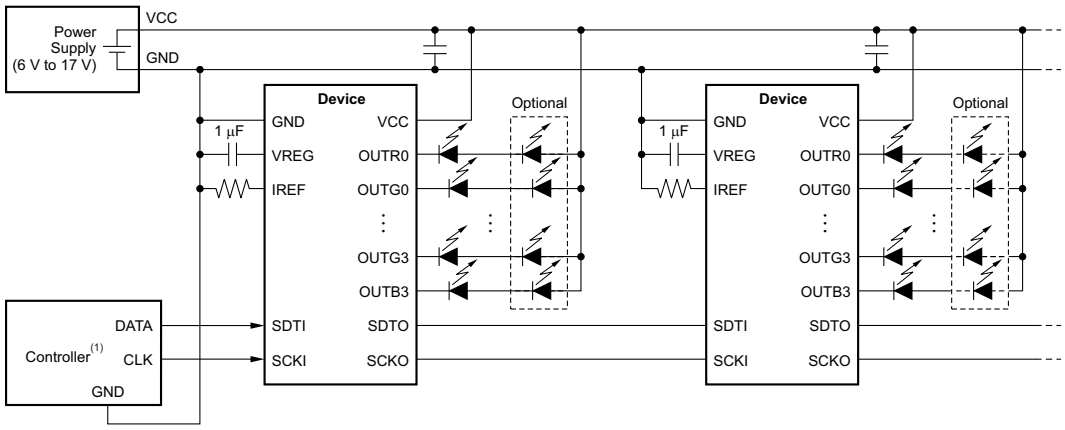
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The device is a 12-channel, constant sink current, LED driver. This device can be connected in series to drive many LED lamps with only a few controller ports. Functional control data and PWM control data can be written from the SDI and SCK input terminal. The PWM timing reference clock can be chosen from the internal oscillation or external SCK signal.

9.2 Typical Application



The output voltage range is from 0 V to 3.3 V.

NOTE: The number of LEDs in series changes, depending on the VCC voltage.

Figure 31. Typical Application Circuit Example (Internal Linear Regulator Using VCC = 6 V to 17 V)

9.2.1 Design Requirements

For this design example, use Table 6 as the input parameters.

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VCC Input Voltage Range	3 V to 5.5 V
LED Lamp (V_{LED}) Input Voltage Range	Maximum 17 V
SIN, SCLK, LAT and GSCLK Voltage Range	Low Level = GND, High Level = VCC

9.2.2 Detailed Design Procedure

9.2.2.1 Define Basic Parameters

To begin the design process, a few parameters must be decided as following"

- Maximum output constant-current value for each color LED lamp
- Maximum LED forward voltage (Vf) and maximum V_{LED}
- Total LEDs and Cascaded IC Number

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9.2.2.2 Data Input Sequence

224-bit data packets are sent through single-wire interface for the PWM control of three output channels. Select the BC data, FC data and write the GS data to the register following the signal timing.

9.2.2.3 How to Control the TLC5971

To set each function mode, BC color, GS output, 6-bit write command, 5-bit FC data, 21-bit BC data for each color group, and 192-bit GS data for OUTXn, a total number of 224 bits must be written into the device. Figure 32 shows the 224-bit data packet configuration.

When *N* units of the TLC5971 are cascaded (as shown in Figure 33), N × 224 bits must be written from the controller into the first device to control all devices. The number of cascaded devices is not limited as long as the proper voltage is supplied to the device at VCC. The packets for all devices must be written again whenever the data in one packet is changed.

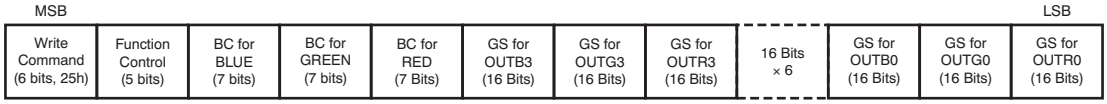

Figure 32. 224-Bit Data Packet Configuration

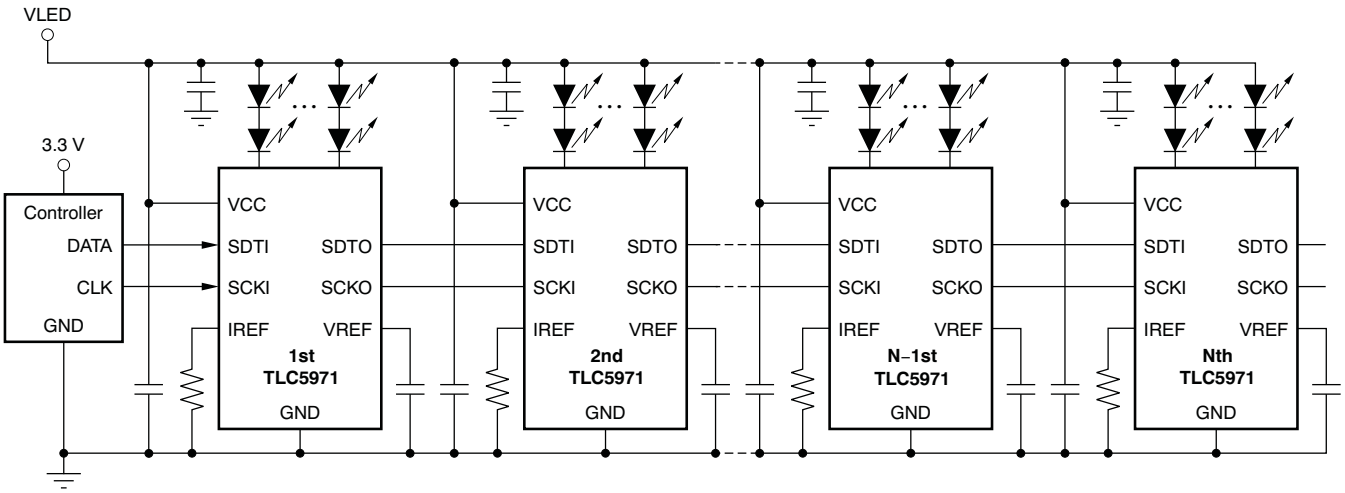

Figure 33. Cascading Connection of *N* TLC5971 Units

9.2.2.3.1 Data Write and PWM Control with Internal Grayscale Clock Mode

When the EXTCLK bit is 0, the internal oscillator clock is used for PWM control of OUTXn (X = R/G/B and n = 0-3) as the GS reference clock. This mode is ideal for illumination applications that change the display image at low frequencies. The data and clock timing is shown in Figure 3 and Figure 34. A writing procedure for the function setting and display control follows:

1. Power up VCC (VLED); all OUTXn are off because BLANK is set to 1.
2. Write the 224-bit data packet (with MSB bit first) for the Nth TLC5971 using the SDTI and SCKI signals. The first six bits of the 224-bit data packet are used as the write command. The write command must be 25h (100101b); otherwise, the 218-bit data in the 224-bit shift register are not copied to the 218-bit data latch. The EXTCLK bit must be set to 0 for the internal oscillator mode. Also, the DSPRPT bit should be set to 1 to repeat the PWM timing control and BLANK set to 0 to start the PWM control.
3. Write the 224-bit data packet for the (N – 1) TLC5971 without delay after step 2.
4. Repeat the data write sequence until all TLC5971s have data. The total shift clock count (SCKI) is now 224 × N. After all device data are written, stop the SCKI at a high or low level for 8× the period between the last SCKI rising edge and the second to last SCKI rising edge. Then the 218 LSBs in the 224-bit shift resister are copied to the 218-bit data latch in all devices and the PWM control is started or updated at the same time.

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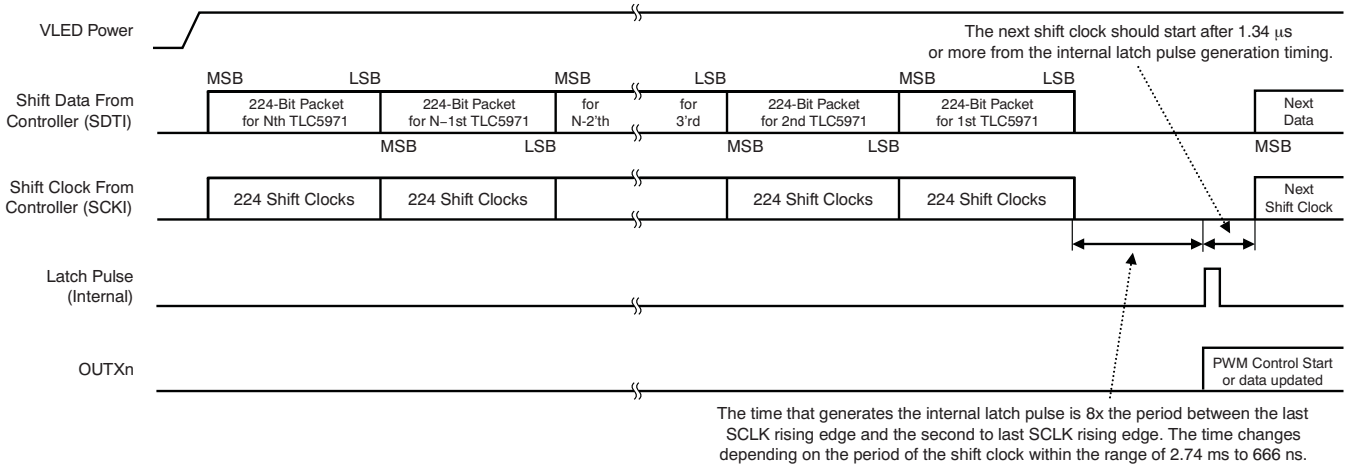

Figure 34. Data Packet and Display Start/Update Timing 1 (Internal Oscillator Mode)

9.2.2.3.2 Data Write and PWM Control with External Grayscale Clock Mode

When the EXTCLK bit is 1, the data shift clock (SCKI) is used for PWM control of OUTXn (X = R/G/B and n = 0-3) as the GS reference clock. This mode is ideal for video image applications that change the display image with high frequencies or for certain display applications that must synchronize all TLC5971s. The data and clock timing are shown in Figure 3 and Figure 35. A writing procedure for the display data and display timing control follows:

1. Power up VCC (VLED); all OUTXn are off because BLANK is set to 1.
2. Write the 224-bit data packet MSB-first for the Nth TLC5971 using the SDTI and SCKI signals. The first six bits of the 224-bit data packet are used as the write command. The write command must be 25h (100101b); otherwise, the 218-bit data in the 224-bit shift register are not copied to the 218-bit data latch. The EXTCLK bit must be set to 1 for the external oscillator mode. Also, the DSPRPT bit should be set to 0 so that the PWM control is not repeated, the TMGRST bit should be set to 1 to reset the PWM control timing at the internal latch pulse generation, and BLANK must be set to 0 to start the PWM control.
3. Write the 224-bit data for the (N – 1) TLC5971 without delay after step 2.
4. Repeat the data write sequence until all TLC5971s have data. The total shift clock count (SCKI) is 224 × N. After all device data are written, stop the SCKI at a high or low level for 8× the period between the last SCKI rising edge and the second to last SCKI rising edge. Then the 218 LSBs in the 224-bit shift resister are copied to the 218-bit data latch in all devices.
5. To start the PWM control, send one pulse of the SCKI clock with SDTI low after 1.34 µs or more from step 4. The OUTXn are turned on when the output GS data are not 0000h.
6. Send the remaining 65535 SCKI clocks with SDTI low. Then the PWM control for OUTXn is synchronized with the SCKI clock and one display period is finished with a total of 65536 SCKI clock periods.
7. Repeat step 2 to step 6 for the next display period.

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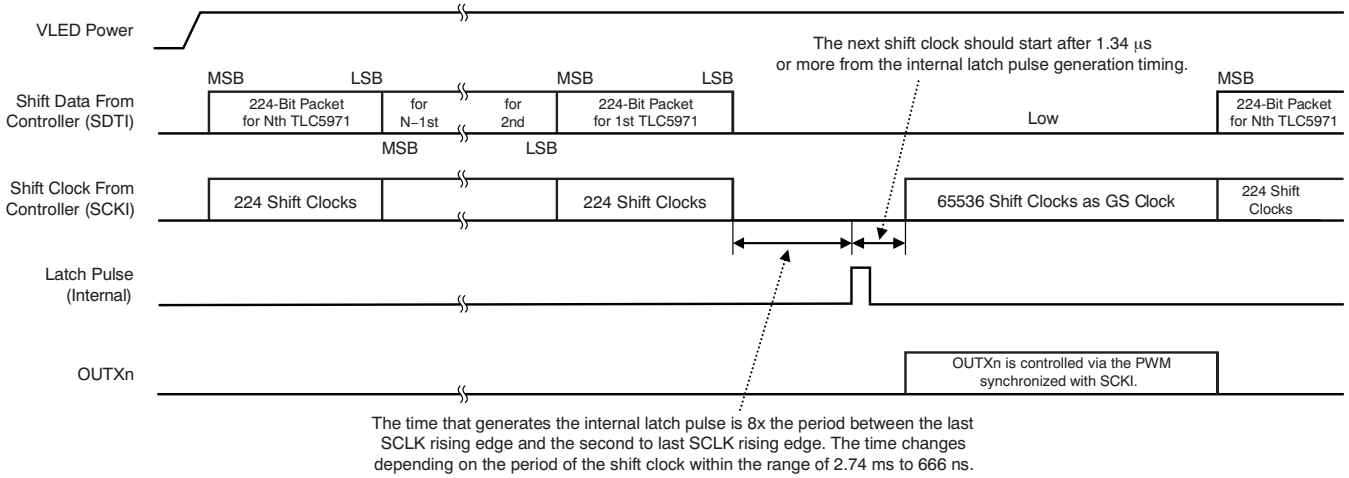

Figure 35. Data Packet and Display Start/Update Timing 2 (External Clock Mode)

There is another control procedure that is recommended for a long chain of cascaded devices. The data and clock timings are shown in Figure 3 and Figure 36. When 256 TLC5971 units are cascaded, use the following procedure:

1. Power up VCC (VLED); all OUTXn are off because BLANK is set to 1.
2. Write the 224-bit data packet MSB-first for the 256th TLC5971 using the SDTI and SCKI signals. The EXTCLK bit must be set to 1 for the external oscillator mode. Also, the DSPRPT bit should be set to 0 so that the PWM control does not repeat, the TMGRST bit should be set to 1 to reset the PWM control timing with the internal latch pulse, and BLANK must be set to 0 to start the PWM control.
3. Repeat the data write sequence for all TLC5971s. The total shift clock count (SCKI) is 57344 (224 × 256). After all device data are written, stop the SCKI signal at a high or low level for eight or more periods between the last SCKI rising edge and the second to last SCKI rising edge. Then the 218 LSBs in the 224-bit shift resister are copied to the 218-bit data latch in all devices.
4. To control the PWM, send 8192 SCKI clock periods with SDTI low after 1.34 µs or more from step 3 (or step 7). These 8192 clock periods are used for the OUTXn PWM control.
5. Write the new 224-bit data packets to the 256th to first TLC5971s for the next display with 256 × 224 SCKI clock for a total of 57344 clocks. The PWM control for OUTXn remains synchronized with the SCKI clock and one display period is finished with a total of 65536 SCKI clocks. The SCKI clock signal is therefore used for PWM control and, at the same time, to write data into the shift registers of all cascaded parts.
6. Stop the SCKI signal at a high or low level for eight or more periods between the last SCKI rising edge and the second to last SCKI rising edge. Then the 218-bit LSBs in the 224-bit shift resister are copied to the 218-bit data latch in all devices.
7. Repeat step 4 to step 6 for the next display periods.

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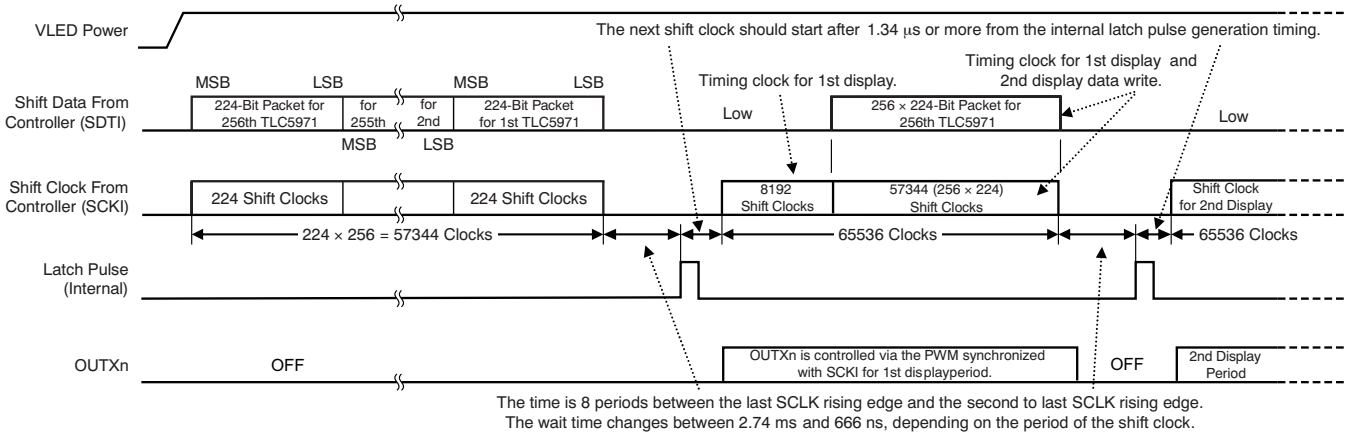

Figure 36. Data Packet and Display Start/Update Timing 3 (External Clock Mode With 256 Cascaded Devices)

9.2.3 Application Curve

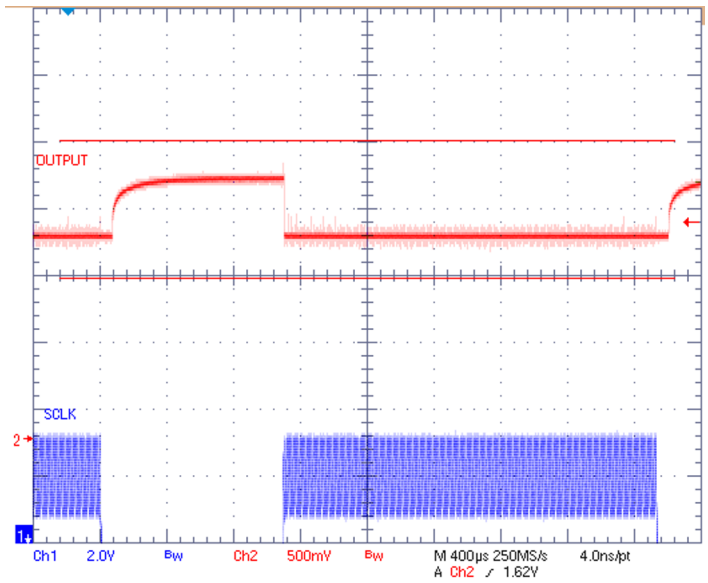

Figure 37. Output Waveform With GS Data Latch Input

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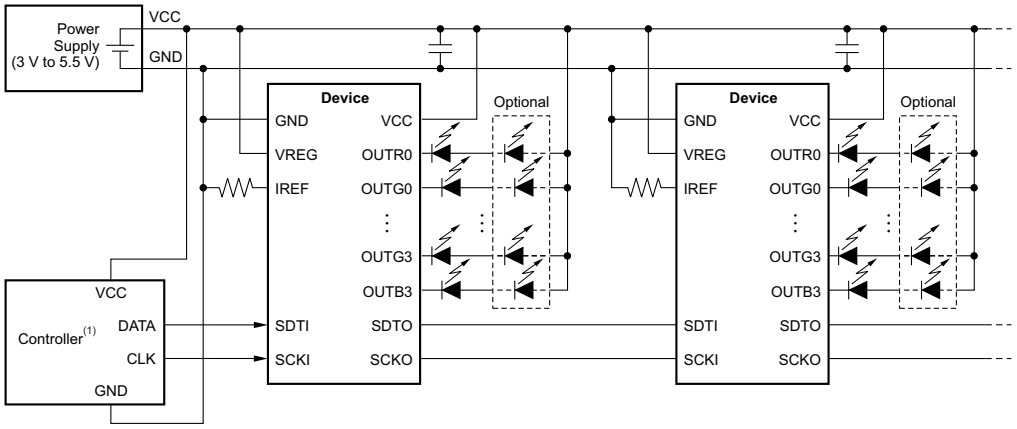
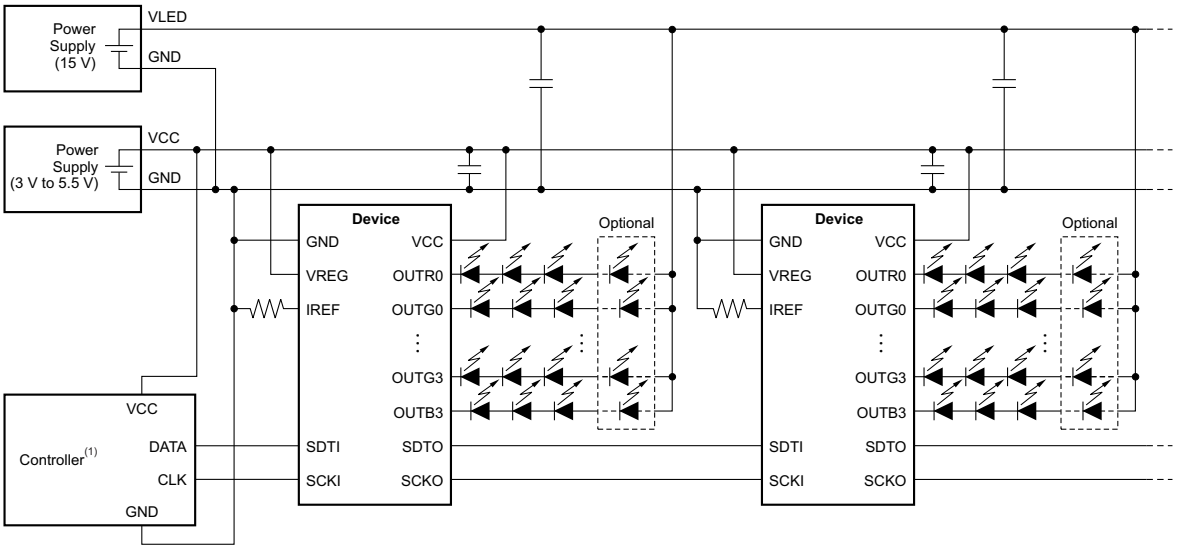
9.3 System Examples



(1) The output operating voltage range is from 0 V to VCC.

Figure 38. Typical Application Circuit Example (Direct Power Supplying V_{CC} = 3 V to 5.5 V)



(1) The output operating voltage range is from 0 V to VCC.

Figure 39. Typical Application Circuit Example (Direct Power Supplying V_{CC} = 3 V to 5.5 V, V_{LED} = 15 V)

10 Power Supply Recommendations

The V_{CC} power supply voltage should be decoupled by placing a 0.1-uF ceramic capacitor close to VCC pin and GND plane. Depending on panel size, several electrolytic capacitors must be placed on board equally distributed to get a well regulated LED supply voltage (V_{LED}). V_{LED} voltage ripple should be less than 5% of its nominal value.

11 Layout

11.1 Layout Guidelines

1. Place the decoupling capacitor near the VCC pin and GND plane.
2. Route the GND pattern as widely as possible for large GND currents.
3. Connecting wire between the chained ICs should be as short as possible to reduce wire inductance.

11.2 Layout Example

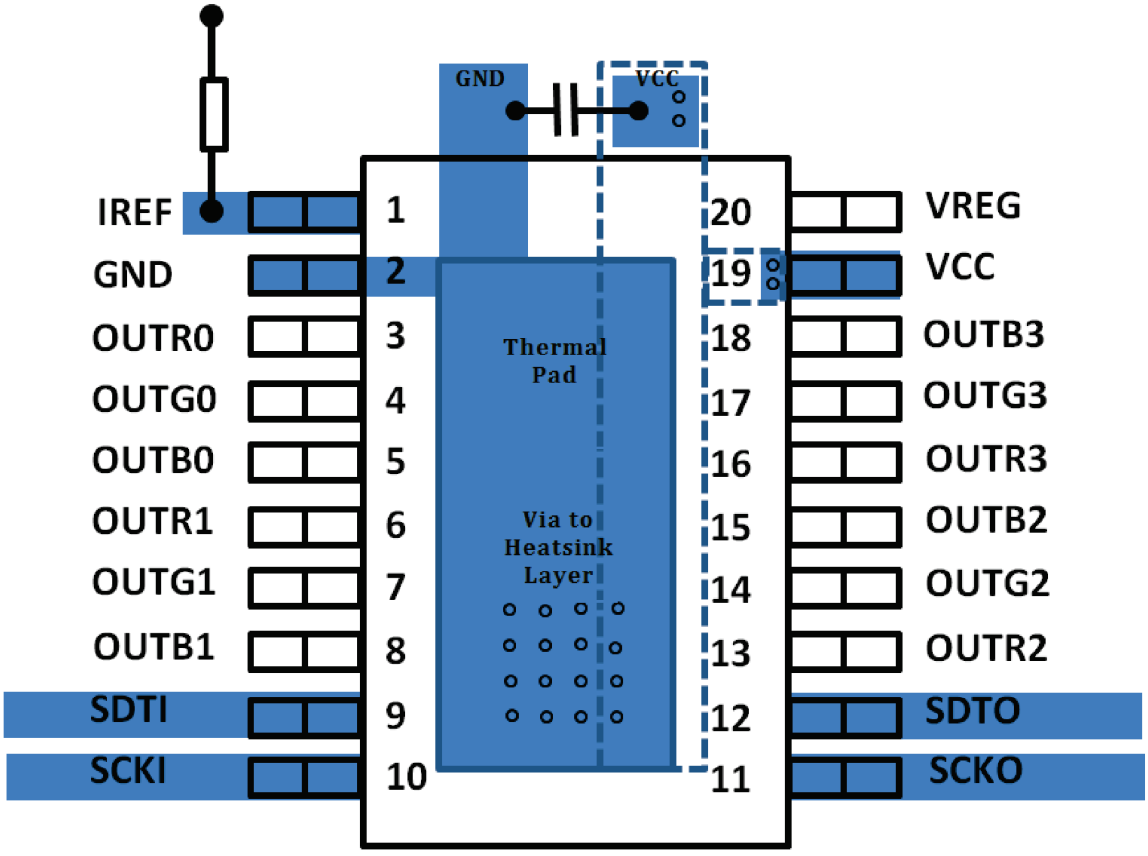


Figure 40. Layout Example

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12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC5971PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5971
TLC5971PWP.B	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5971
TLC5971PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5971
TLC5971PWPR.B	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5971
TLC5971RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5971
TLC5971RGER.B	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5971
TLC5971RGERG4	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5971
TLC5971RGERG4.B	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5971
TLC5971RGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5971
TLC5971RGET.B	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5971

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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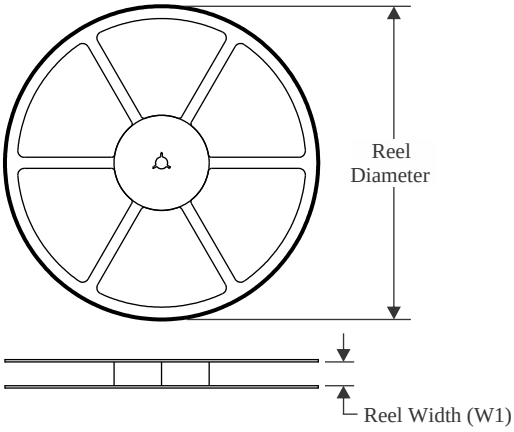
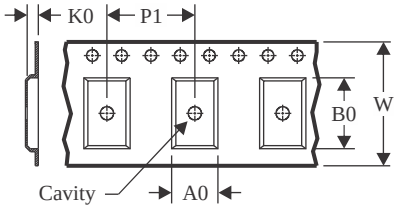
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

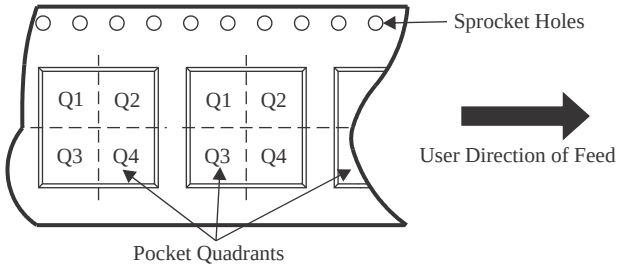


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

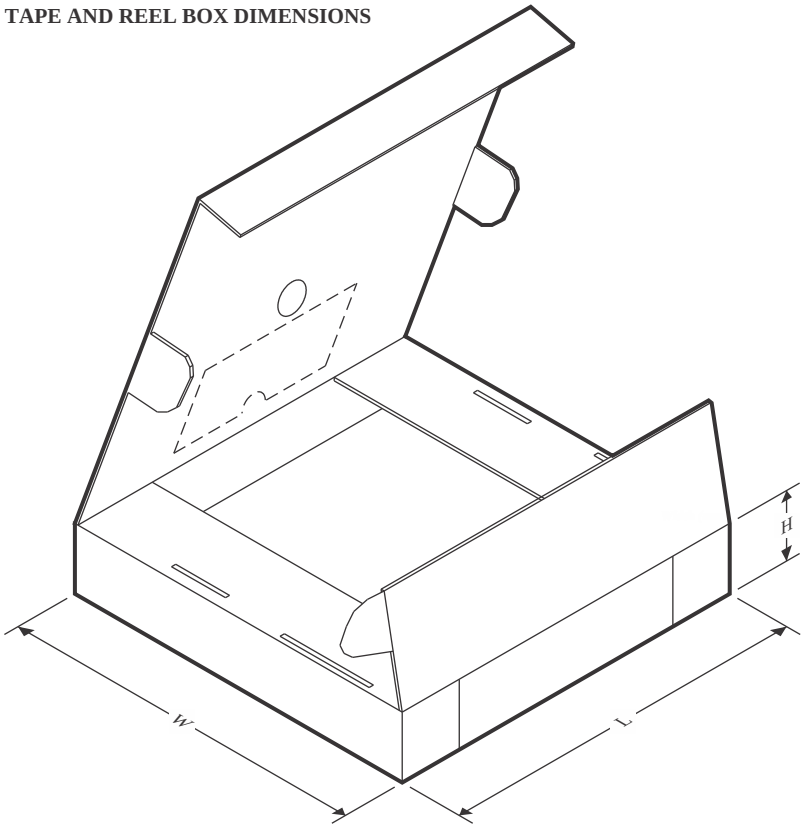
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5971PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLC5971RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC5971RGERG4	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC5971RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

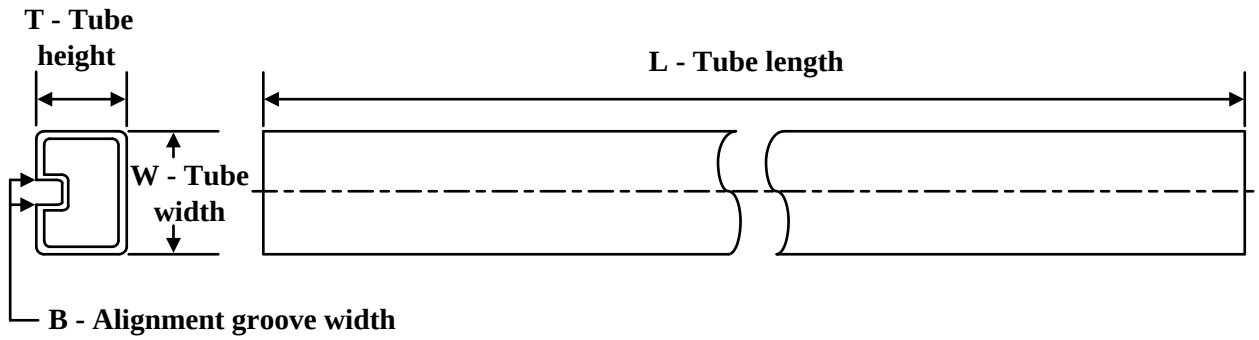
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5971PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TLC5971RGER	VQFN	RGE	24	3000	356.0	356.0	35.0
TLC5971RGERG4	VQFN	RGE	24	3000	356.0	356.0	35.0
TLC5971RGET	VQFN	RGE	24	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC5971PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TLC5971PWP.B	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

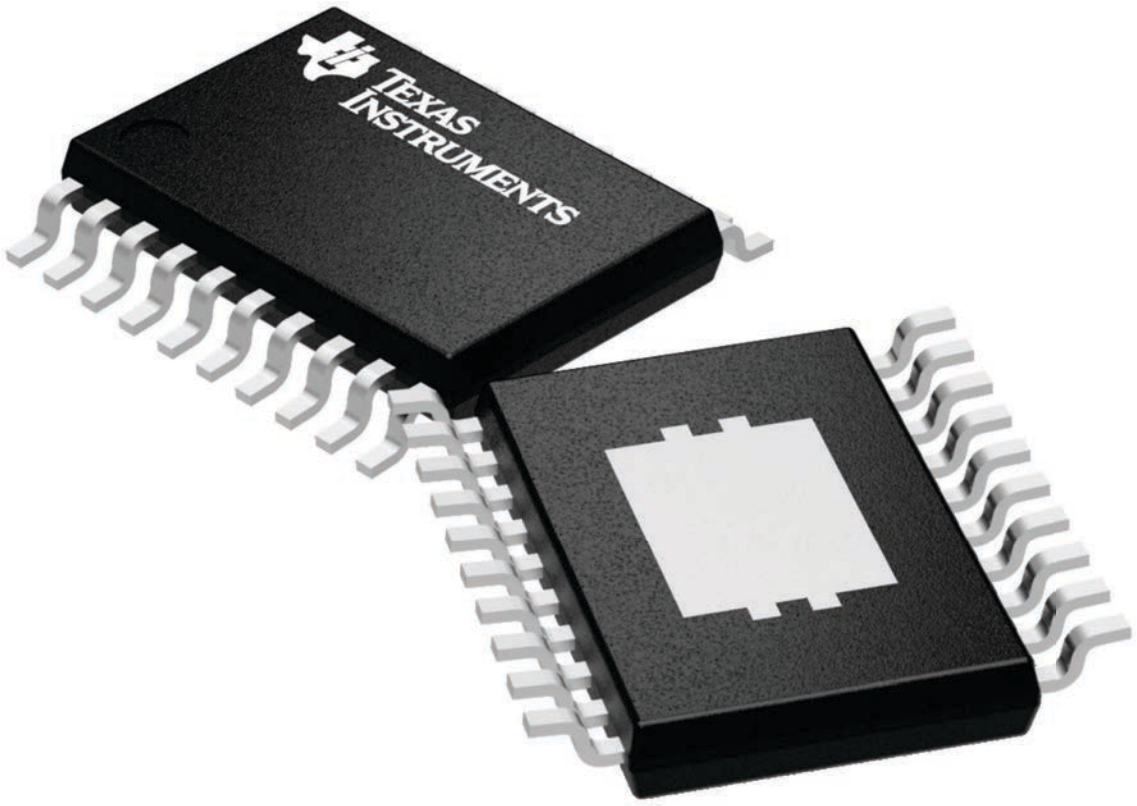
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

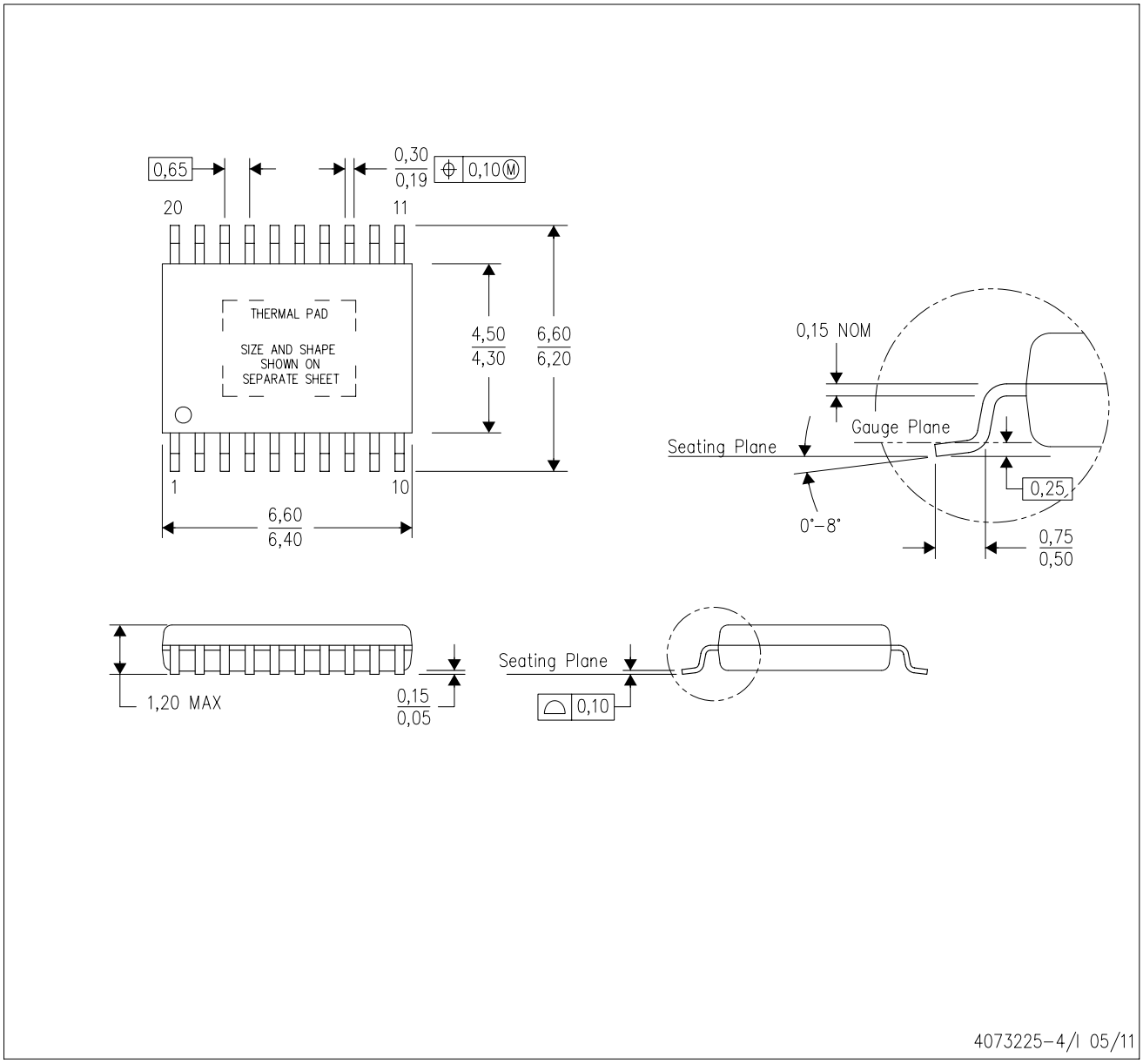
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

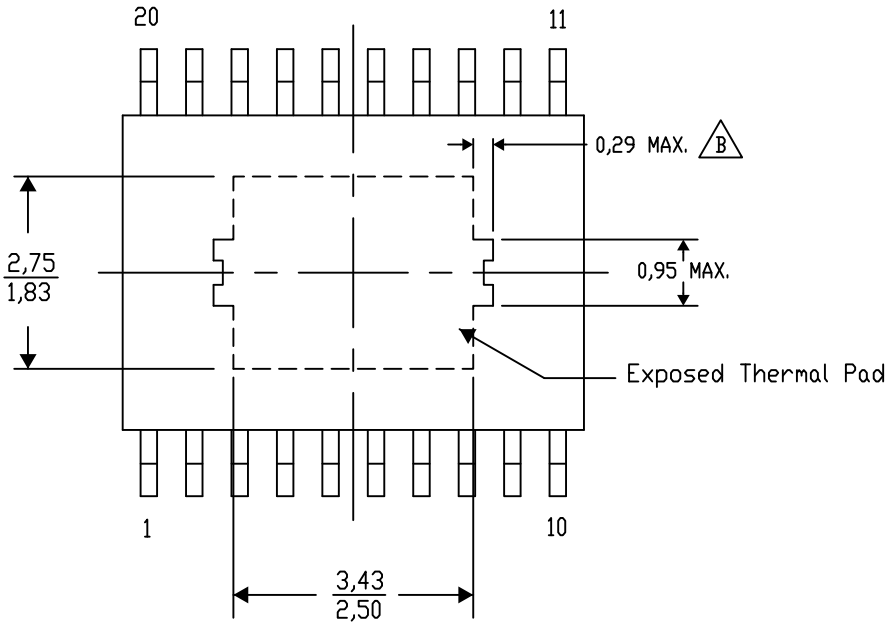
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

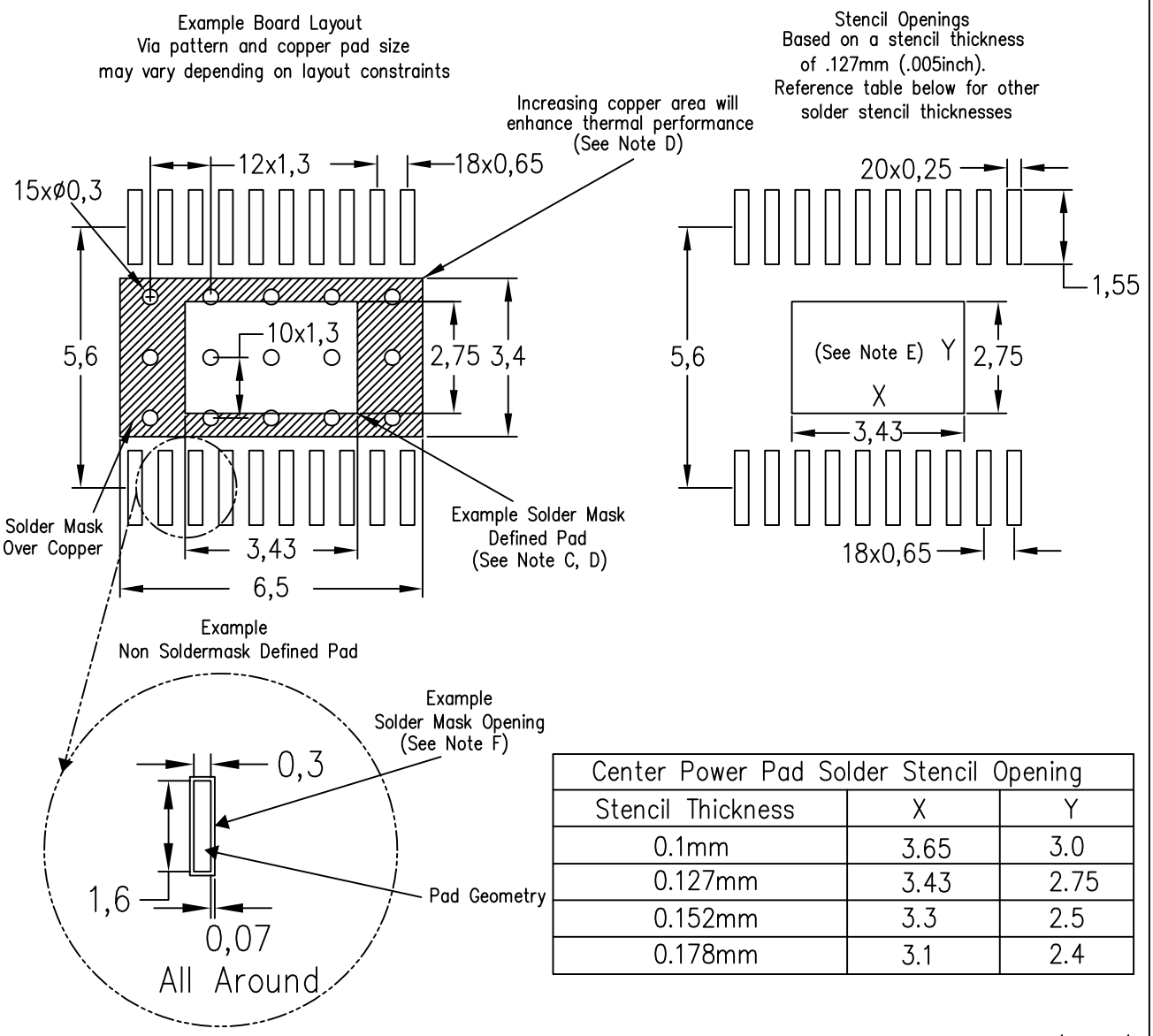
4206332–17/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.65	3.0
0.127mm	3.43	2.75
0.152mm	3.3	2.5
0.178mm	3.1	2.4

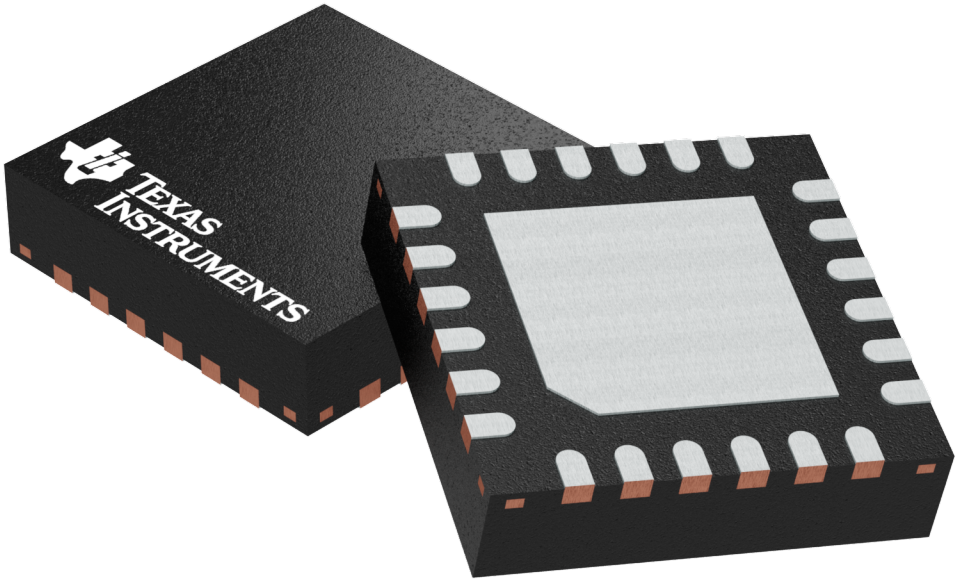
4207609–10/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



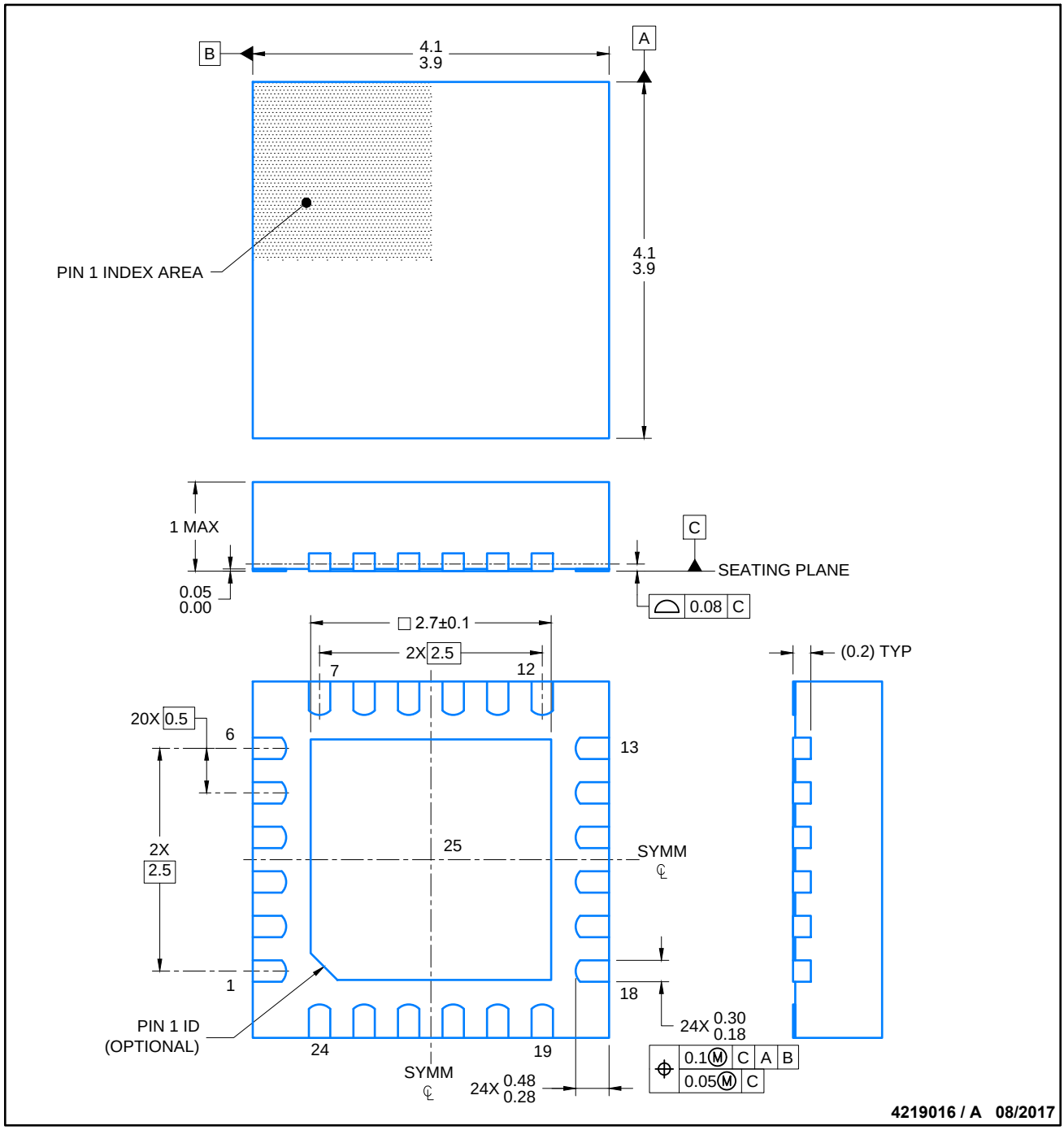
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGE0024H

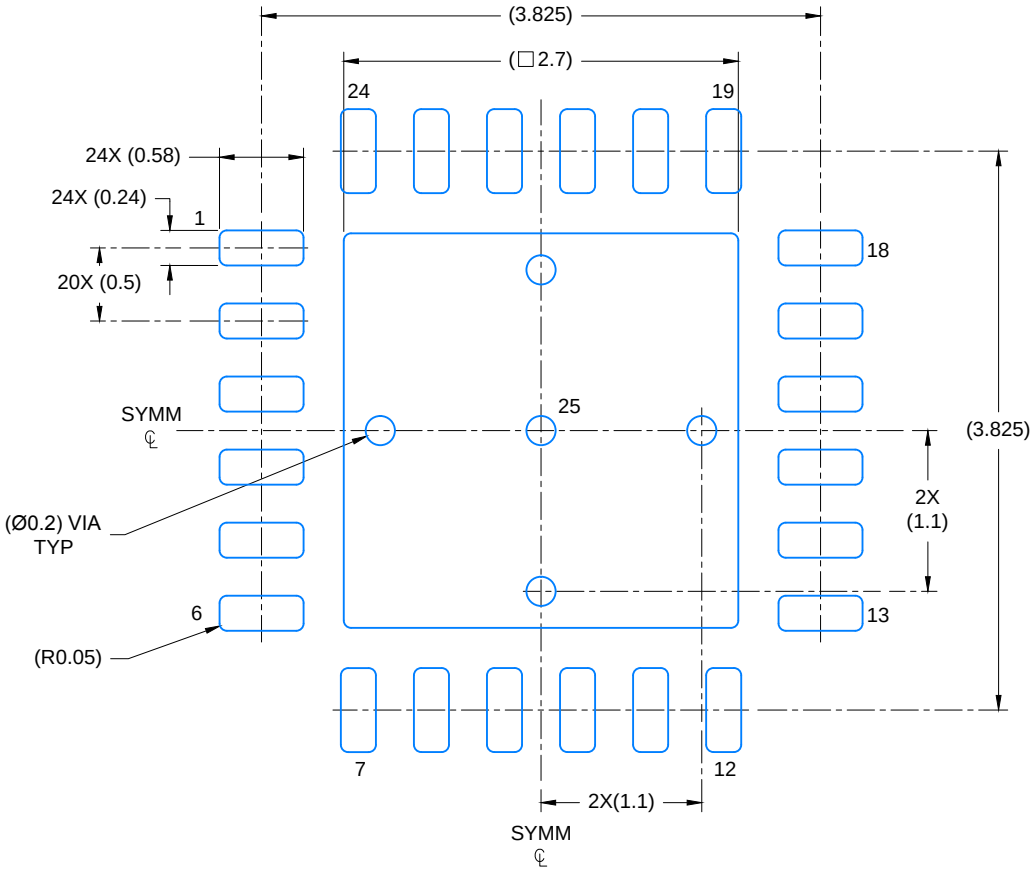
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



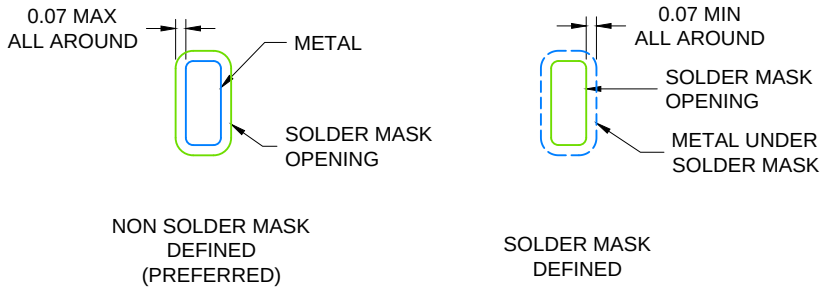
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

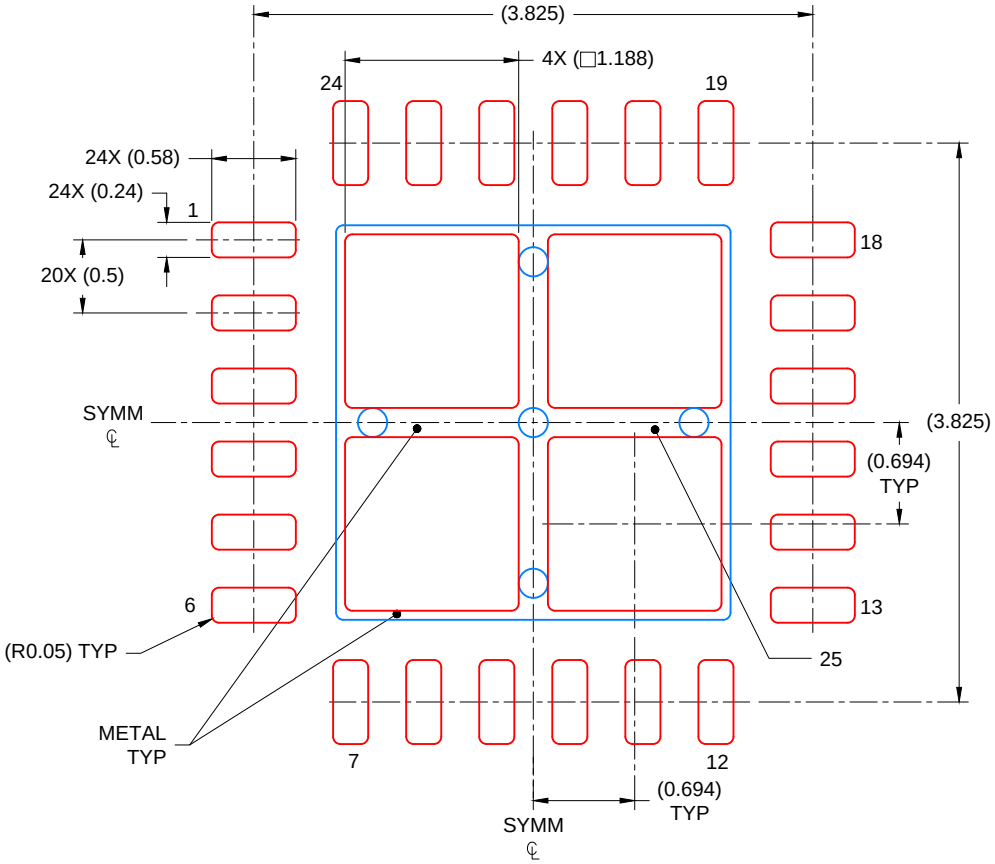


SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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