

LM4916 Boomer® Audio Power Amplifier Series 1.5V, Mono 85mW BTL Output, 14mW Stereo Headphone Audio Amplifier

Check for Samples: [LM4916](#)

FEATURES

- Single-Cell 0.9V to 2.5V Battery Operation
- BTL Mode for Mono Speaker
- Single-Ended Headphone Operation with Coupling Capacitors
- Unity-Gain Stable
- "Click and Pop" Suppression Circuitry
- Active-Low Micropower Shutdown
- Low Current, Active-Low Mute Mode
- Thermal Shutdown Protection Circuitry

APPLICATIONS

- Portable One-Cell Audio Products
- Portable One-Cell Electronic Devices

KEY SPECIFICATIONS

- Mono-BTL Output Power
- ($R_L=8\Omega$, $V_{DD}=1.5V$, THD+N=1%), 85mW (typ)
- Stereo Headphone Output Power
- ($R_L=16\Omega$, $V_{DD}=1.5V$, THD+N=1%), 14mW (typ)
- Micropower Shutdown Current, 0.02 μ A (typ)
- Supply Voltage Operating Range, 0.9V< V_{DD} <2.5V
- PSRR 1kHz, $V_{DD}=1.5V$, 66dB (typ)

Typical Application

DESCRIPTION

The unity gain stable LM4916 is both a mono differential output (for bridge-tied loads or BTL) audio power amplifier and a Single Ended (SE) stereo headphone amplifier. Operating on a single 1.5V supply, the mono BTL mode delivers 85mW into an 8 Ω load at 1% THD+N. In Single Ended stereo headphone mode, the amplifier delivers 14mW per channel into a 16 Ω load at 1% THD+N.

With the LM4916 packaged in the MM and WSON packages, the customer benefits include low profile and small size. These packages minimize PCB area and maximizes output power.

The LM4916 features circuitry that reduces output transients ("clicks" and "pops") during device turn-on and turn-off, an externally controlled, low-power consumption, active-low shutdown mode, and thermal shutdown. Boomer audio power amplifiers are designed specifically to use few external components and provide high quality output power in a surface mount package.

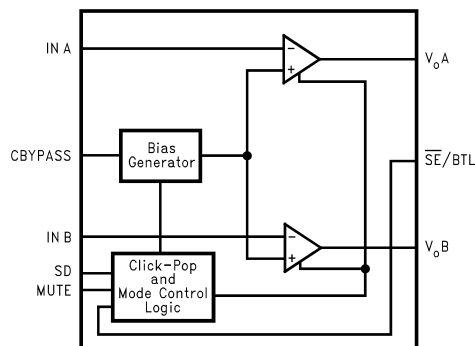


Figure 1. Block Diagram



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Connection Diagrams

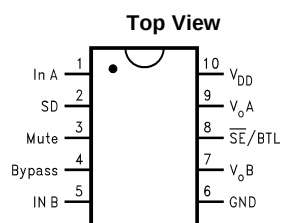


Figure 2. VSSOP Package
See Package Number DGS0010A

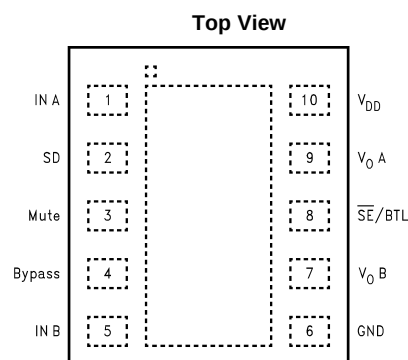


Figure 3. WSON Package
See Package Number NGY0010A

Typical Connections

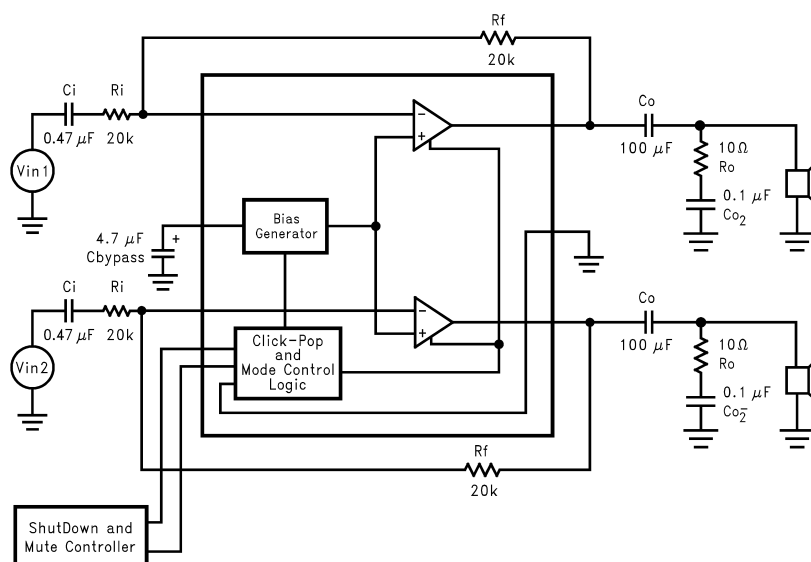


Figure 4. Typical Single Ended Output Configuration Circuit

ELECTRICAL CHARACTERISTICS FOR THE LM4916⁽¹⁾⁽²⁾

The following specifications apply for the circuit shown in [Figure 38](#) operating with $V_{DD} = 1.5V$, unless otherwise specified. Limits apply for $T_A = 25^\circ C$.

Parameter		Test Conditions	LM4916		Units (Limits)
			Typ ⁽³⁾	Limit ⁽⁴⁾	
V_{DD}	Supply Voltage ⁽⁵⁾⁽⁶⁾			0.9	V (min)
				2.5	V (max)
I_{DD}	Quiescent Power Supply Current	$V_{IN} = 0V$, $I_O = 0A$, $R_L = \infty$ See ⁽⁷⁾	1.0	1.4	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN} = GND$	0.02		μA (max)
V_{OS}	Output Offset Voltage	BTL	5	50	mV (max)
P_O	Output Power ⁽⁸⁾	$f = 1kHz$			
		$R_L = 8\Omega$ BTL, THD+N = 1%	85	70	mW (min)
		$R_L = 16\Omega$ SE, THD+N = 1%	14		mW
THD+N	Total Harmonic Distortion + Noise	$R_L = 8\Omega$, BTL, $P_O = 25mW$, $f = 1kHz$	0.1	0.5	%
		$R_L = 16\Omega$, SE, $P_O = 5mW$, $f = 1kHz$	0.2		
V_{NO}	Output Voltage Noise	20Hz to 20kHz, A-weighted	10		μV_{RMS}
I_{MUTE}	Mute Current	$V_{MUTE} = 0$, SE	15		μA
Crosstalk		$R_L = 16\Omega$, SE	55		dB (min)
PSRR	Power Supply Rejection Ratio	$V_{RIPPLE} = 200mV_{P-P}$ $C_{BYPASS} = 4.7\mu F$, $R_L = 8\Omega$ $f = 1kHz$, BTL	62		dB
		$V_{RIPPLE} = 200mV_{P-P}$ sine wave $C_{BYPASS} = 4.7\mu F$, $R_L = 16\Omega$ $f = 1kHz$, SE	66		dB (min)
V_{IH}	Control Logic High		0.7		V (min)
V_{IL}	Control Logic Low		0.3		V (max)

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (2) All voltages are measured with respect to the ground (GND) pins unless otherwise specified.
- (3) Typicals are measured at $25^\circ C$ and represent the parametric norm.
- (4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
- (5) When operating on a power supply voltage of 0.9V, the LM4916 will not function below $0^\circ C$. At a power supply voltage of 1V or greater, the LM4916 will operate down to $-40^\circ C$.
- (6) Ripple on power supply line should not exceed $400mV_{pp}$.
- (7) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.
- (8) Output power is measured at the device terminals.

TYPICAL PERFORMANCE CHARACTERISTICS

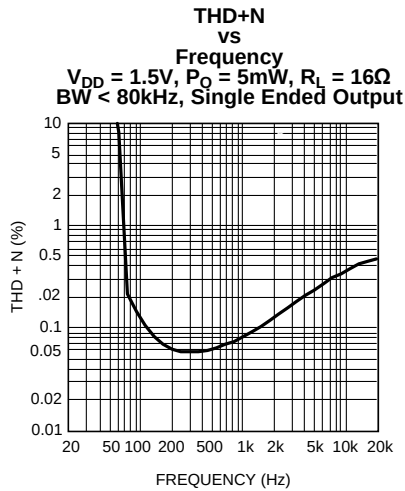


Figure 6.

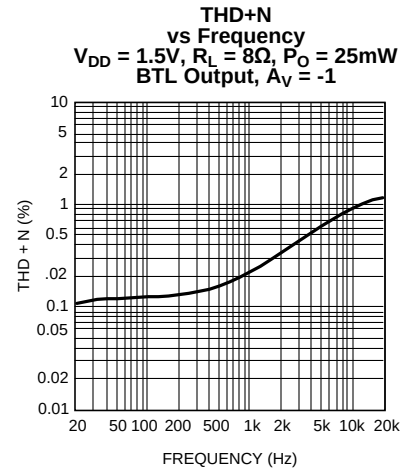


Figure 7.

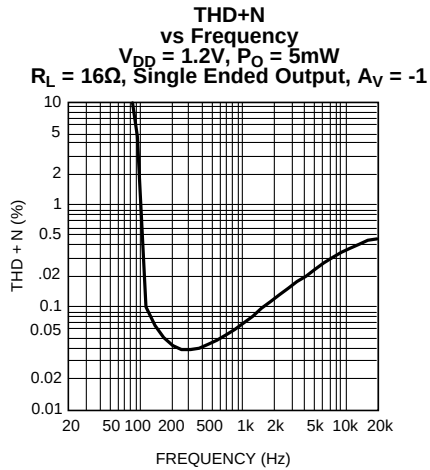


Figure 8.

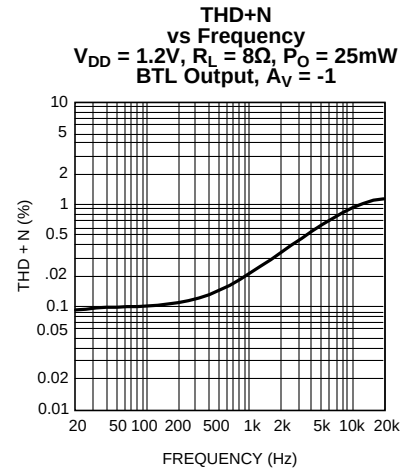


Figure 9.

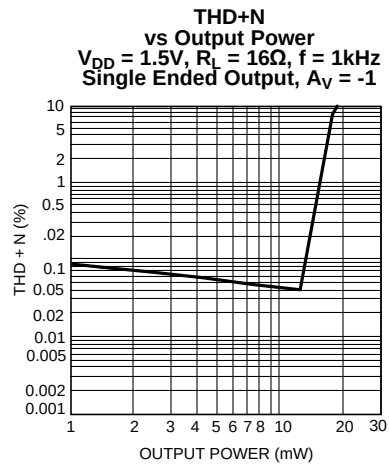


Figure 10.

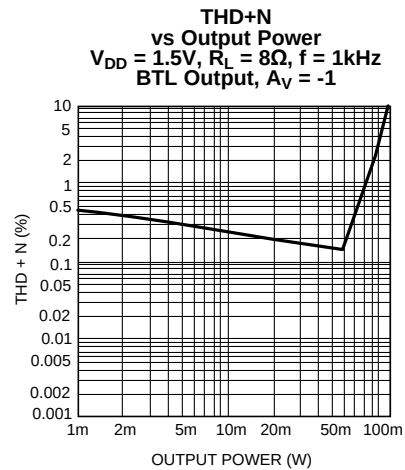
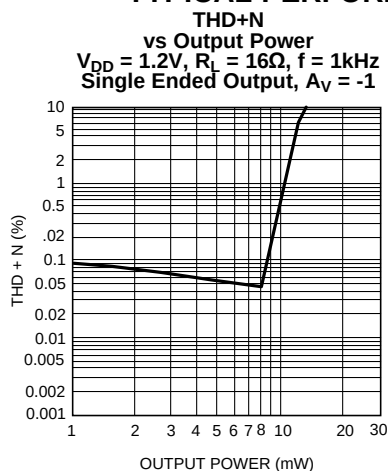
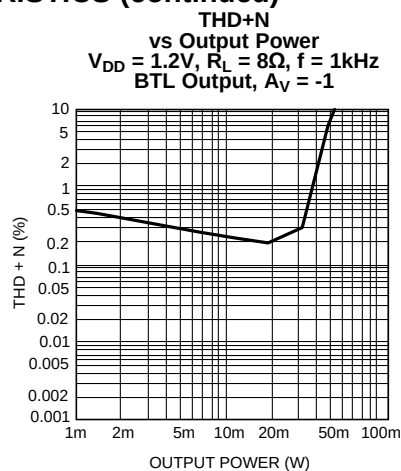
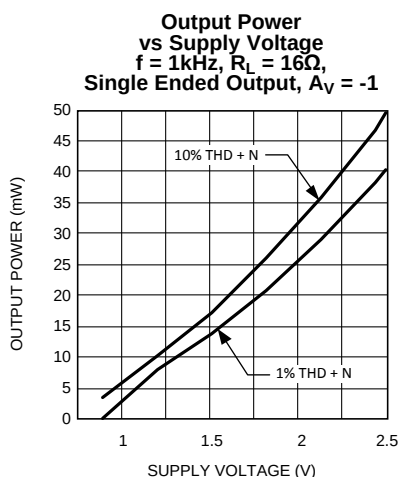
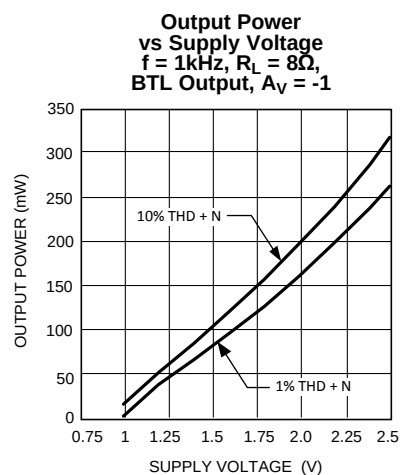
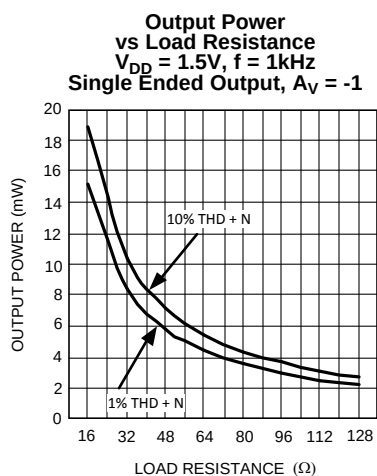
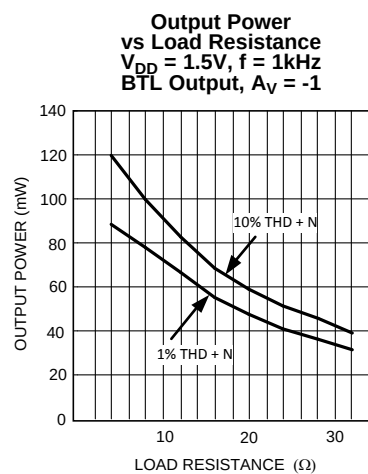


Figure 11.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)**Figure 12.****Figure 13.****Figure 14.****Figure 15.****Figure 16.****Figure 17.**

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

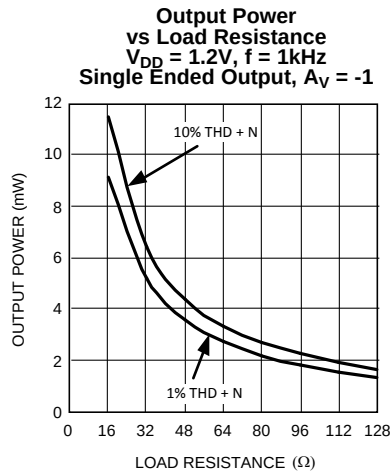


Figure 18.

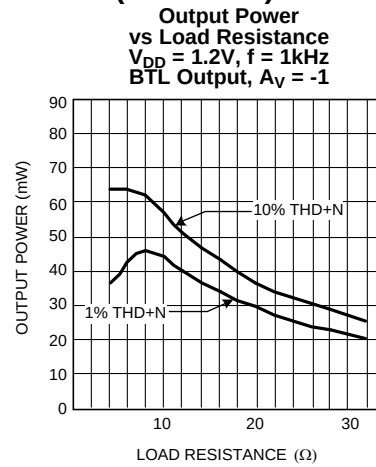


Figure 19.

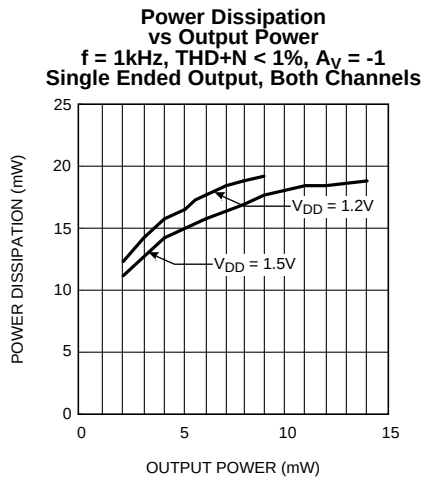


Figure 20.

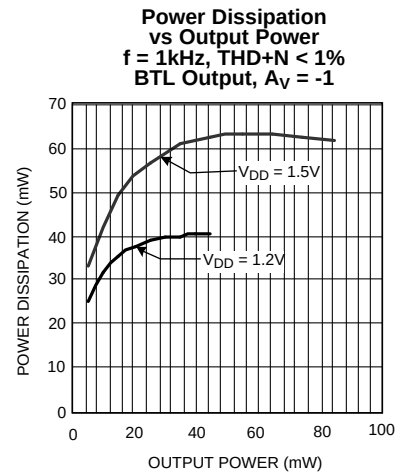


Figure 21.

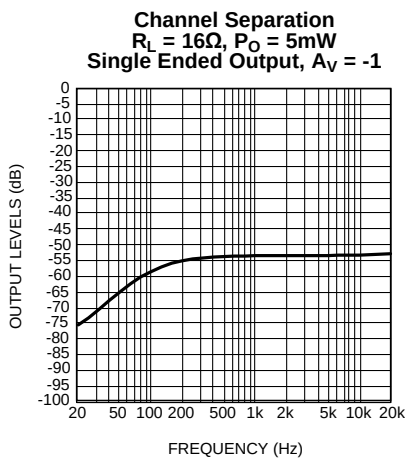


Figure 22.

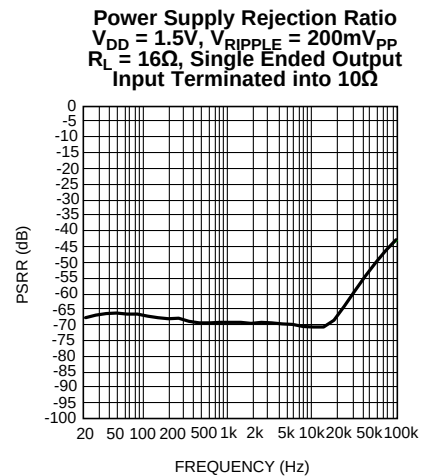


Figure 23.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power Supply Rejection Ratio
 $V_{DD} = 1.5V$, $V_{RIPPLE} = 200mV_{PP}$
 $R_L = 8\Omega$, BTL
 Input Terminated into 10Ω

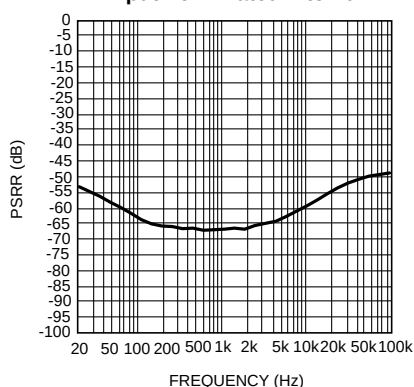


Figure 24.

Power Supply Rejection Ratio
 $V_{DD} = 1.2V$, $V_{RIPPLE} = 200mV_{PP}$
 $R_L = 16\Omega$, Single Ended Output
 Input Terminated into 10Ω

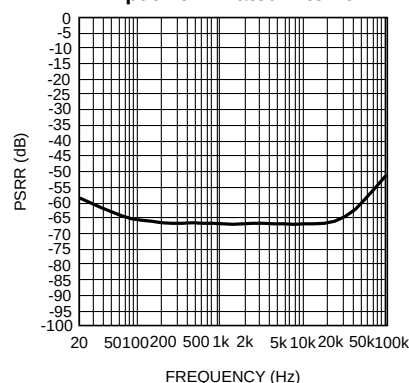


Figure 25.

Power Supply Rejection Ratio
 $V_{DD} = 1.2V$, $V_{RIPPLE} = 200mV_{PP}$
 $R_L = 8\Omega$, BTL
 Input Terminated into 10Ω

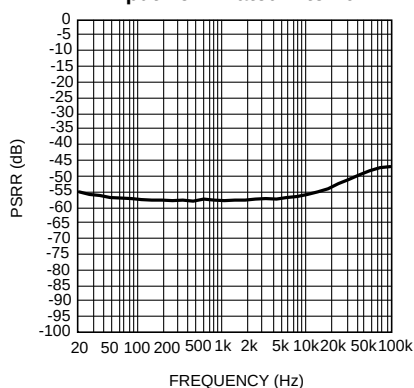


Figure 26.

Frequency Response vs Input Capacitor Size
 $V_{DD} = 1.5V$, $R_L = 16\Omega$
 $AV = -1$, $BW < 80kHz$, Single Ended Output

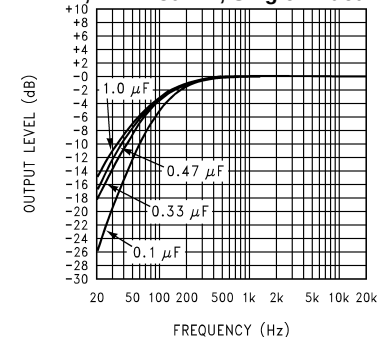


Figure 27.

Frequency Response vs Input Capacitor Size
 $V_{DD} = 1.5V$, $R_L = 8\Omega$
 $AV = -1$, $BW < 80kHz$, BTL Output

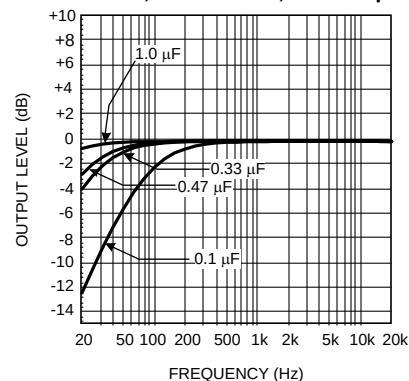


Figure 28.

Open Loop Frequency Response
 $V_{DD} = 1.5V$, No load

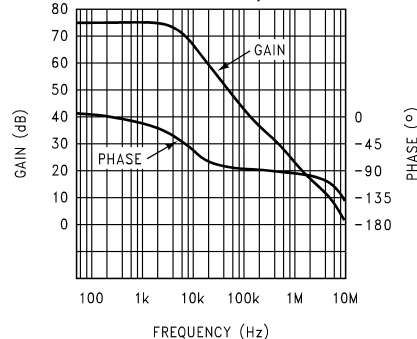


Figure 29.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

**Supply Voltage
vs Supply Current**

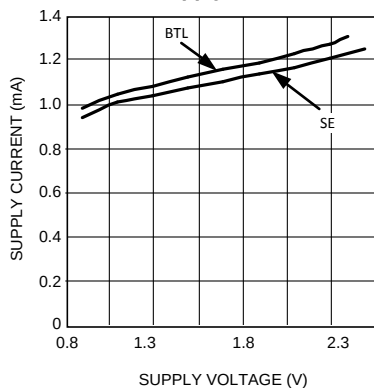


Figure 30.

**Clipping Voltage
vs Supply Voltage**

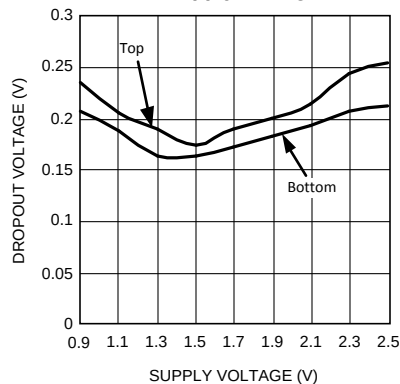


Figure 31.

**Noise Floor
V_{DD} = 1.5V, Single Ended Output
16Ω, 80kHz Bandwidth**

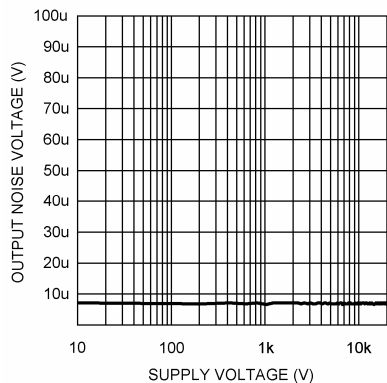


Figure 32.

**Noise Floor
V_{DD} = 1.5V, BTL Output
8Ω, 80kHz Bandwidth**

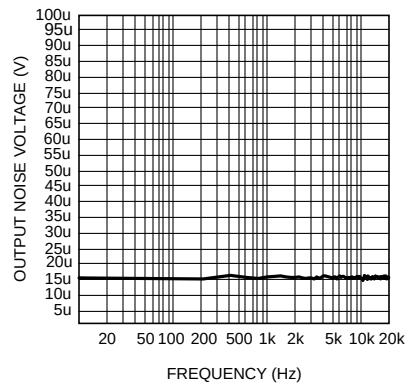


Figure 33.

**Shutdown Hysteresis Voltage
V_{DD} = 1.5V**

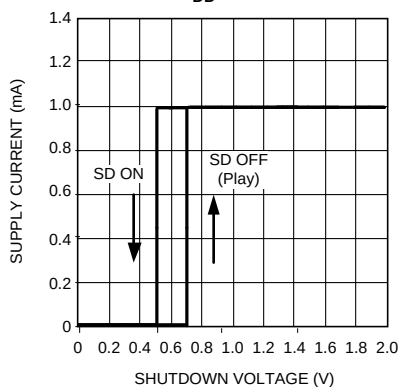


Figure 34.

**Power Derating Curve
V_{DD} = 1.5V**

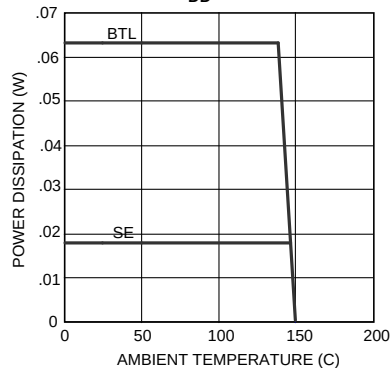
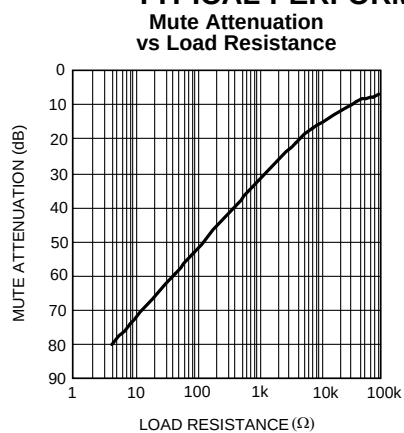
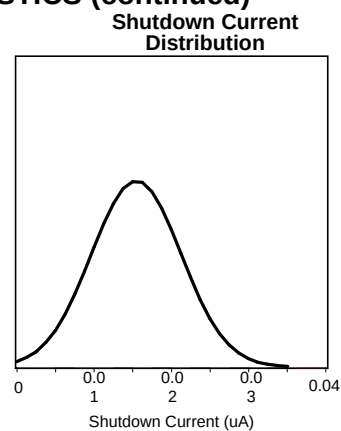


Figure 35.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)**Figure 36.****Figure 37.**

APPLICATION INFORMATION

SINGLE ENDED (SE) CONFIGURATION EXPLANATION

As shown in [Figure 4](#), the LM4916 has two operational amplifiers internally, which have externally configurable gain. The closed loop gain of the two configurable amplifiers is set by selecting the ratio of R_f to R_i . Consequently, the gain for each channel of the IC is

$$A_{VD} = -(R_f / R_i) \quad (1)$$

When the LM4916 operates in Single Ended mode, coupling capacitors are used on each output (VoA and VoB) and the SE/BTL pin (Pin 8) is connected to ground. These output coupling capacitors blocks the half supply voltage to which the output amplifiers are typically biased and couples the audio signal to the headphones or other single-ended (SE) loads. The signal return to circuit ground is through the headphone jack's sleeve.

BRIDGED (BTL) CONFIGURATION EXPLANATION

As shown in [Figure 5](#), the LM4916 has two internal operational amplifiers. The first amplifier's gain is externally configurable, while the second amplifier should be externally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain should be fixed by the two external 20kΩ resistors. [Figure 5](#) shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f / R_i). \quad (2)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground. A bridge amplifier design has a few distinct advantages over the single-ended configuration. It provides a differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the [AUDIO POWER AMPLIFIER DESIGN](#) section.

A bridge configuration, such as the one used in LM4916, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration.

MODE SELECT DETAIL

The LM4916 can be configured in either Single Ended or BTL mode (see [Figure 4](#) and [Figure 5](#)). The default state of the LM4916 at power up is single ended. During initial power up or return from shutdown, the LM4916 must detect the correct mode of operation by sensing the status of the SE/BTL pin. When the bias voltage of the part ramps up to 60mV (as seen on the Bypass pin), an internal comparator detects the status of SE/BTL; and at 10mV, latches that value in place. Ramp up of the bias voltage will proceed at a different rate from this point on depending upon operating mode. BTL mode will ramp up about 11 times faster than Single Ended mode. Shutdown is not a valid command during this time period (T_{WU}) and should not be enabled to ensure a proper power on reset (POR) signal. In addition, the slew rate of V_{DD} must be greater than 2.5V/ms to ensure reliable POR. Recommended power up timing is shown in [Figure 39](#) along with proper usage of Shutdown and Mute. The mode-select circuit is suspended during C_B discharge time. The circuit shown in [Figure 38](#) presents an applications solution to the problem of using different supply voltages with different turn-on times in a system with the LM4916. This circuit shows the LM4916 with a 25-50kΩ. Pull-up resistor connected from the shutdown pin to V_{DD} . The shutdown pin of the LM4916 is also being driven by an open drain output of an external microcontroller

on a separate supply. This circuit ensures that shutdown is disabled when powering up the LM4916 by either allowing shutdown to be high before the LM4916 powers on (the microcontroller powers up first) or allows shutdown to ramp up with V_{DD} (the LM4916 powers up first). This will ensure the LM4916 powers up properly and enters the correct mode of operation. Please note that the SE/BTL pin (Pin 8) should be tied to GND for Single Ended mode, and to V_{DD} for BTL mode.

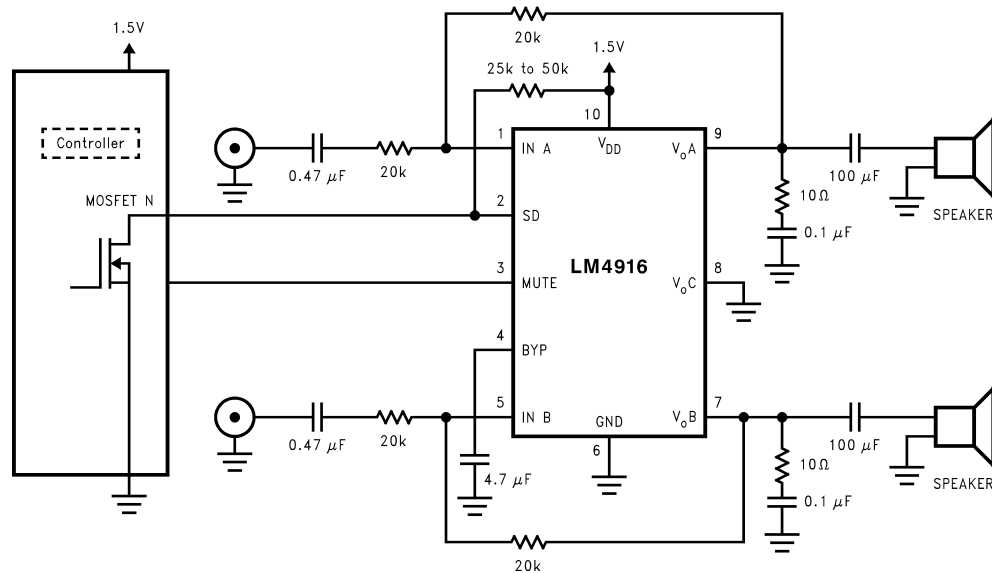


Figure 38. Recommended Circuit for Different Supply Turn-On Timing

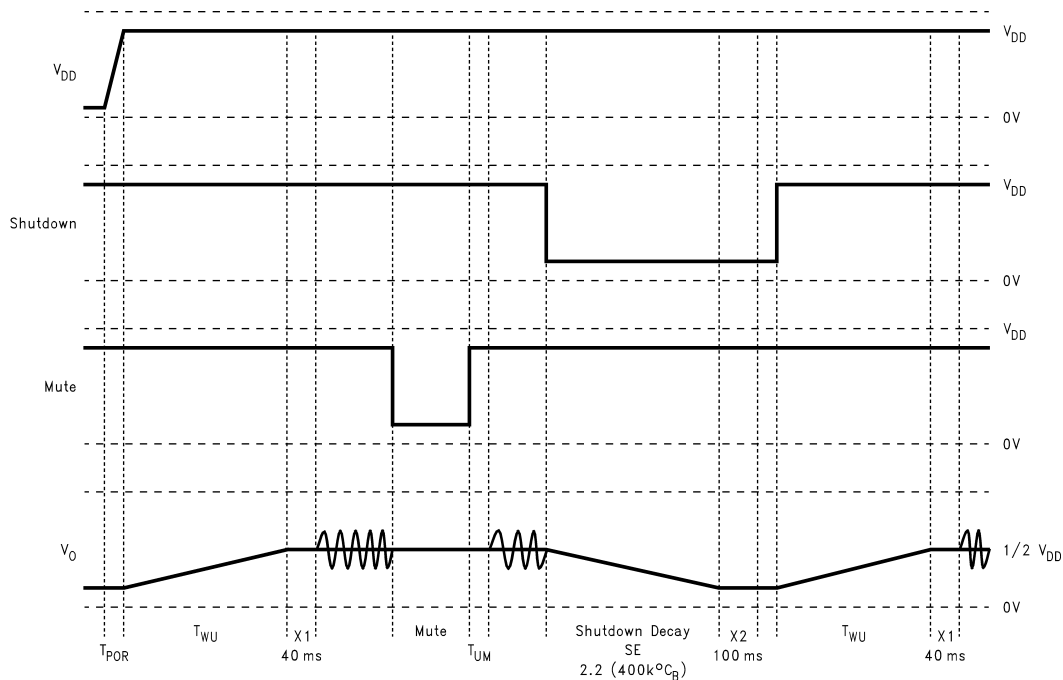


Figure 39. Turn-On, Shutdown, and Mute Timing for Cap-Coupled Mode

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4916 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given BTL application can be derived from the power dissipation graphs or from [Equation 3](#).

$$P_{\text{DMAX}} = 4 \cdot (V_{\text{DD}})^2 / (2\pi^2 R_L) \quad (3)$$

When operating in Single Ended mode, [Equation 4](#) states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{\text{DMAX}} = (V_{\text{DD}})^2 / (2\pi^2 R_L) \quad (4)$$

Since the LM4916 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number that results from [Equation 4](#). From [Equation 4](#), assuming a 1.5V power supply and a 16Ω load, the maximum power dissipation point is 7mW per amplifier. Thus the maximum package dissipation point is 14mW.

The maximum power dissipation point obtained from either [Equation 3](#) or [Equation 4](#) must not be greater than the power dissipation that results from [Equation 5](#):

$$P_{\text{DMAX}} = (T_{\text{JMAX}} - T_A) / \theta_{\text{JA}} \quad (5)$$

For package DGS0010A, $\theta_{\text{JA}} = 175^\circ\text{C/W}$. $T_{\text{JMAX}} = 150^\circ\text{C}$ for the LM4916. Depending on the ambient temperature, T_A , of the system surroundings, [Equation 5](#) can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of [Equation 3](#) or [Equation 4](#) is greater than that of [Equation 5](#), then either the supply voltage must be decreased, the load impedance increased or T_A reduced. For the typical application of a 1.5V power supply, with a 16Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 146°C provided that device operation is around the maximum power dissipation point. Thus, for typical applications, power dissipation is not an issue. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the Typical Performance Characteristics curves for power dissipation information for lower output powers.

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The LM4916's exposed-DAP (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air.

The LD package should have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad may be connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Further detailed and specific information concerning PCB layout, fabrication, and mounting an LD (WSON) package is available from Texas Instruments' Package Engineering Group under application note [AN-1187](#).

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is important for low noise performance and high power supply rejection. The capacitor location on the power supply pins should be as close to the device as possible. Typical applications employ a battery (or 1.5V regulator) with 10μF tantalum or electrolytic capacitor and a ceramic bypass capacitor that aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4916. A bypass capacitor value in the range of 0.1μF to 1μF is recommended.

MICRO POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4916's shutdown function. Activate micro-power shutdown by applying a logic-low voltage to the SHUTDOWN pin. When active, the LM4916's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The trigger point varies depending on supply voltage and is shown in the Shutdown Hysteresis Voltage graphs in the Typical Performance Characteristics section. The low 0.02μA (typ) shutdown current is achieved by applying a voltage that is as near as ground as possible to the SHUTDOWN pin. A voltage that is higher than ground may increase the shutdown current. There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100kΩ pull-up resistor between the SHUTDOWN pin and V_{DD} . Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by opening the switch. Closing the switch connects the SHUTDOWN pin to ground, activating micro-power shutdown. The switch and resistor ensure that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull-up resistor.

MUTE

When in single ended mode, the LM4916 also features a mute function that enables extremely fast turn-on/turn-off with a minimum of output pop and click with a low current consumption ($\leq 20\mu\text{A}$, typical). The mute function leaves the outputs at their bias level, thus resulting in higher power consumption than shutdown mode, but also provides much faster turn on/off times. Providing a logic low signal on the MUTE pin enables mute mode. Threshold voltages and activation techniques match those given for the shutdown function as well. Mute may not appear to function when the LM4916 is used to drive high impedance loads. This is because the LM4916 relies on a typical headphone load (16-32Ω) to reduce input signal feed-through through the input and feedback resistors. Mute attenuation can thus be calculated by the following formula:

$$\text{Mute Attenuation (dB)} = 20\text{Log}[R_L / (R_i + R_f)]$$

Parallel load resistance may be necessary to achieve satisfactory mute levels when the application load is known to be high impedance. The mute function, described above, is not necessary when the LM4916 is operating in BTL mode since the shutdown function operates quickly in BTL mode with less power consumption than mute. In these modes, the Mute signal is equivalent to the Shutdown signal. Mute may be enabled during shutdown transitions, but should not be toggled for a brief period immediately after exiting or entering shutdown. These brief time periods are labeled X1 (time after returning from shutdown) and X2 (time after entering shutdown) and are shown in the timing diagram given in [Figure 39](#). X1 occurs immediately following a return from shutdown (TWU) and lasts 40ms±25%. X2 occurs after the part is placed in shutdown and the decay of the bias voltage has occurred ($2.2 \times 250\text{k} \times \text{CB}$) and lasts for 100ms±25%. The timing of these transition periods relative to X1 and X2 is also shown in [Figure 39](#). While in single ended mode, mute should not be toggled during these time periods, but may be toggled during the shutdown transitions or any other time the part is in normal operation. Failure to operate mute correctly may result in much higher click and pop values or failure of the device to mute at all.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4916 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality. The LM4916 is unity-gain stable that gives the designer maximum system flexibility. The LM4916 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than $1V_{\text{rms}}$ are available from sources such as audio codecs. Very large values should not be used for the gain-setting resistors. Values for R_i and R_f should be less than 1MΩ. Please refer to the section, [AUDIO POWER AMPLIFIER DESIGN](#), for a more complete explanation of proper gain selection. Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in [Figure 4](#) and [Figure 5](#). The input coupling capacitor, C_i , forms a first order high pass filter that limits low frequency response. This value should be chosen based on needed frequency response and turn-on time.

SELECTION OF INPUT CAPACITOR SIZE

Amplifying the lowest audio frequencies requires a high value input coupling capacitor, C_i . A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the headphones used in portable systems have little ability to reproduce signals below 60Hz. Applications using headphones with this limited frequency response reap little improvement by using a high value input capacitor. In addition to system cost and size, turn on time is affected by the size of the input coupling capacitor C_i . A larger input coupling capacitor requires more charge to reach its quiescent DC voltage. This charge comes from the output via the feedback. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on time can be minimized. A small value of C_i (in the range of 0.1 μ F to 0.47 μ F), is recommended.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B , the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM4916 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4916's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 4.7 μ F along with a small value of C_i (in the range of 0.1 μ F to 0.47 μ F), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops. This ensures that output transients are eliminated when power is first applied or the LM4916 resumes operation after shutdown.

Minimizing External Components

Operating the LM4916 at higher gain settings can minimize the use of external components. For instance, a BTL configuration with a gain setting greater than 8V/V ($A_V > 8$) makes the output capacitor C_O unnecessary. For the Single Ended configuration, a gain setting greater than 4V/V ($A_V > 4$) eliminates the need for output capacitor C_{O2} and output resistor R_O , on each output channel.

If the LM4916 is operating with a lower gain setting ($A_V < 4$), external components can be further minimized only in Single Ended mode. For each channel, output capacitor (C_{O2}) and output resistor (R_O) can be eliminated. These components need to be compensated for by adding a 7.5k Ω resistor (R_C) between the input pin and ground pin on each channel (between Pin 1 and GND, and between Pin 5 and GND).

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4916 contains circuitry that eliminates turn-on and shutdown transients ("clicks and pops"). For this discussion, turn-on refers to either applying the power supply voltage or when the micro-power shutdown mode is deactivated.

As the $V_{DD}/2$ voltage present at the BYPASS pin ramps to its final value, the LM4916's internal amplifiers are configured as unity gain buffers. An internal current source charges the capacitor connected between the BYPASS pin and GND in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches $V_{DD}/2$. As soon as the voltage on the bypass pin is stable, the device becomes fully operational and the amplifier outputs are reconnected to their respective output pins. Although the BYPASS pin current cannot be modified, changing the size of C_B alters the device's turn-on time. There is a linear relationship between the size of C_B and the turn-on time. Here are some typical turn-on times for various values of C_B :

Table 1. Single-Ended

$C_B(\mu\text{F})$	T_{ON}
0.1	117ms
0.22	179ms
0.47	310ms
1.0	552ms
2.2	1.14s
4.7	2.4s

Table 2. BTL

$C_B(\mu F)$	$T_{ON}(ms)$
0.1	72
0.22	79
0.47	89
1.0	112
2.2	163
4.7	283

In order to eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause "clicks and pops".

AUDIO POWER AMPLIFIER DESIGN

A 25mW/32 Ω Audio Amplifier

Given:	
Power Output	10mWrms
Load Impedance	16 Ω
Input Level	0.4Vrms
Input Impedance	20k Ω

A designer must first choose a mode of operation (SE or BTL) and determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs. Supply Voltage graphs in the [Typical Performance Characteristics](#) section, the supply rail can be easily found. 1.5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4916 to reproduce peak in excess of 10mW without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the [Power Dissipation](#) section. Once the power dissipation equations have been addressed, the required gain can be determined from [Equation 6](#).

$$A_V \geq \sqrt{(P_O R_L)} / (V_{IN}) = V_{orms} / V_{inrms} \quad (6)$$

From [Equation 6](#), the minimum A_V is 1; use $A_V = 1$. Since the desired input impedance is 20k, and with a A_V gain of 1, a ratio of 1:1 results from [Equation 3](#) for R_i to R . The values are chosen with $R_i = 20k$ and $R_f = 20k$. The final design step is to address the bandwidth requirements which must be stated as a pair of -3dB frequency points. Five times away from a -3dB point is 0.17dB down from passband response which is better than the required $\pm 0.25dB$ specified.

$$f_L = 100Hz/5 = 20Hz$$

$$f_H = 20kHz * 5 = 100kHz$$

As stated in the [Proper Selection of External Components](#) section, R_i in conjunction with C_i creates a

$$C_i \geq 1 / (2\pi * 20k\Omega * 20Hz) = 0.397\mu F; \text{ use } 0.39\mu F.$$

The high frequency pole is determined by the product of the desired frequency pole, f_H , and the differential gain, A_V . With an $AV_V = 1$ and $f_H = 100\text{kHz}$, the resulting $GBWP = 100\text{kHz}$ which is much smaller than the LM4916 GBWP of 3MHz. This example displays that if a designer has a need to design an amplifier with higher differential gain, the LM4916 can still be used without running into bandwidth limitations.

Revision History

Rev	Date	Description
1.0	7/11/03	Re-released the D/S to the WEB.
1.1	7/25/06	Deleted the RL labels on curves E5, E6, E3, and E4, per Allan S., then re-released the D/S to the WEB.
E	5/03/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4916LD/NOPB	Active	Production	WSO N (NGY) 10	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L4916
LM4916LD/NOPB.A	Active	Production	WSO N (NGY) 10	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L4916
LM4916LDX/NOPB	Active	Production	WSO N (NGY) 10	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L4916
LM4916LDX/NOPB.A	Active	Production	WSO N (NGY) 10	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L4916
LM4916MM/NOPB	Active	Production	VSSOP (DGS) 10	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	GA9
LM4916MM/NOPB.A	Active	Production	VSSOP (DGS) 10	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	GA9

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

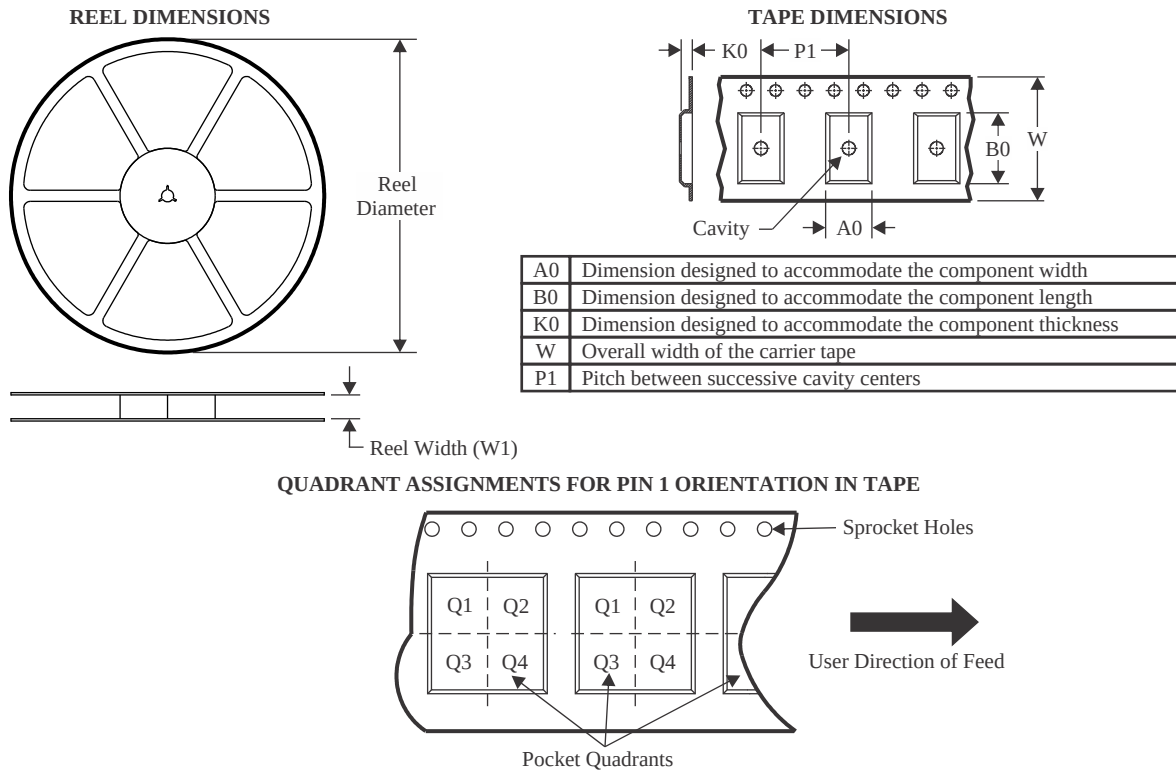
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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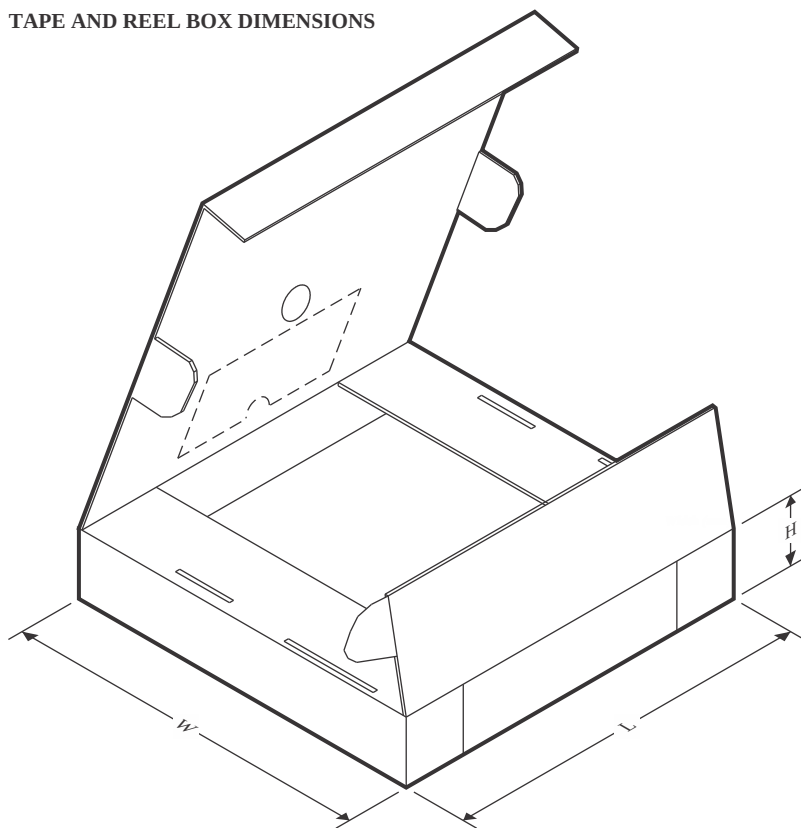
TAPE AND REEL INFORMATION



*All dimensions are nominal

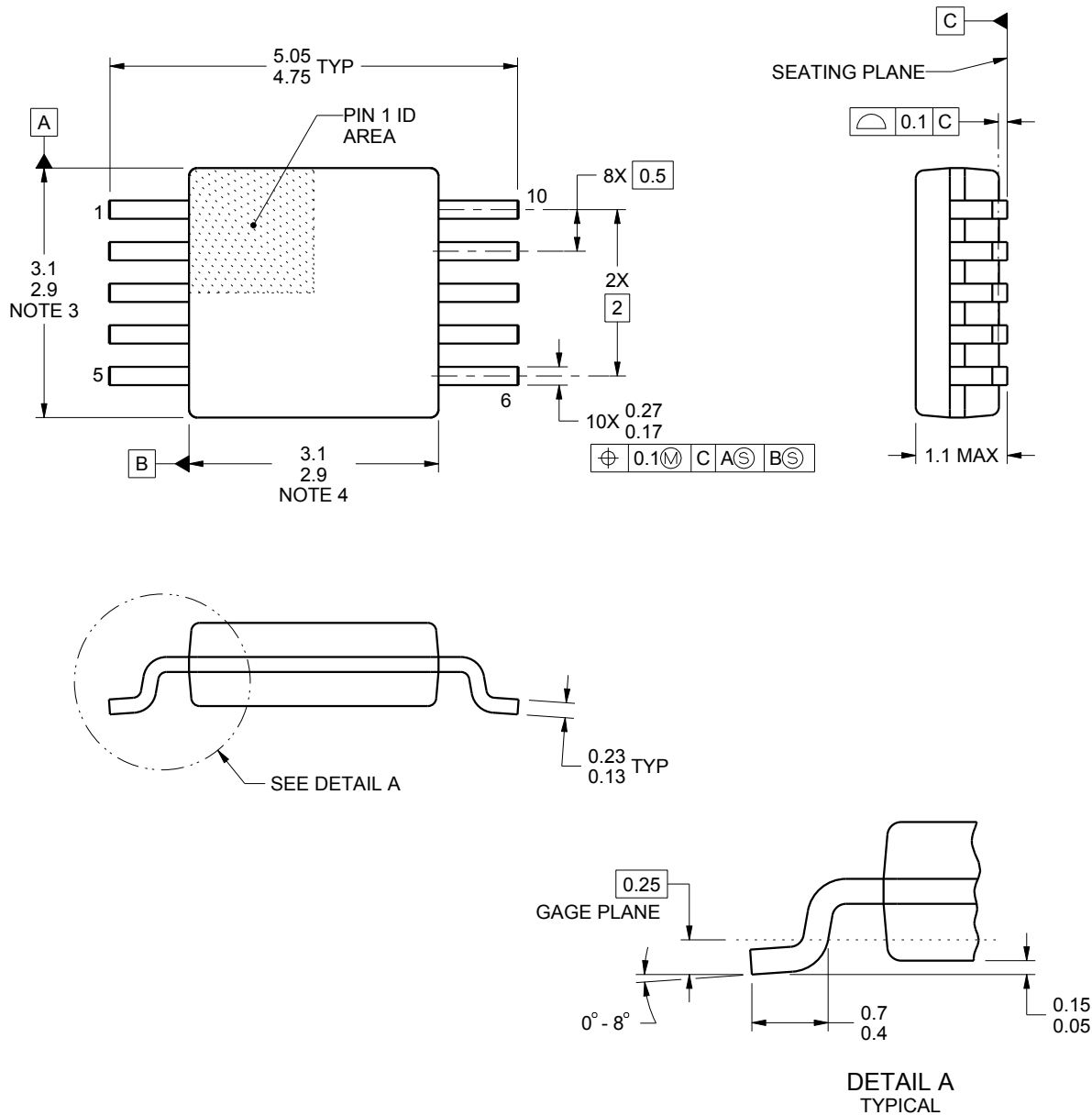
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4916LD/NOPB	WSOP	NGY	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM4916LDX/NOPB	WSOP	NGY	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM4916MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4916LD/NOPB	WSO	NGY	10	1000	208.0	191.0	35.0
LM4916LDX/NOPB	WSO	NGY	10	4500	356.0	356.0	36.0
LM4916MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0



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NOTES:

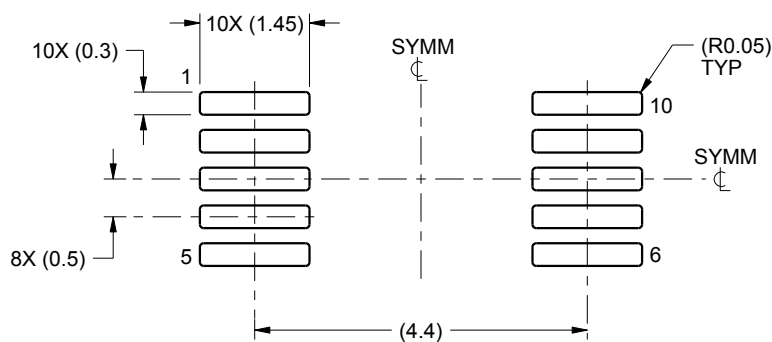
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

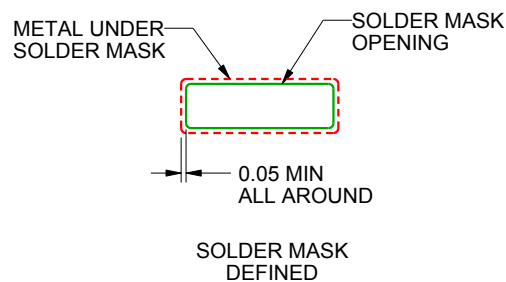
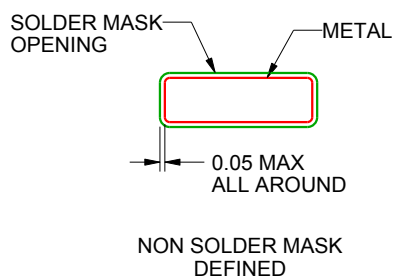
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

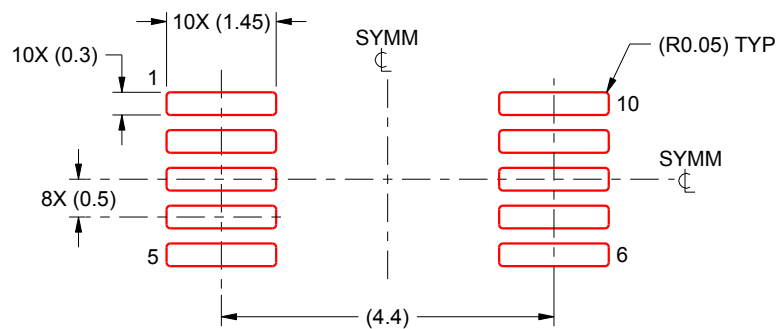
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



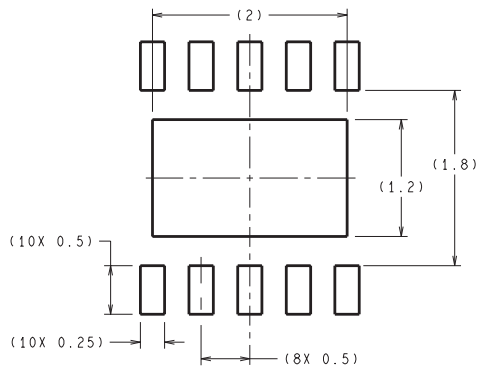
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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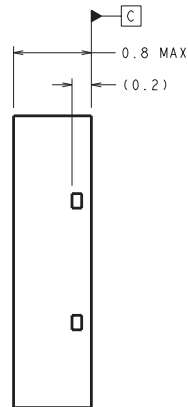
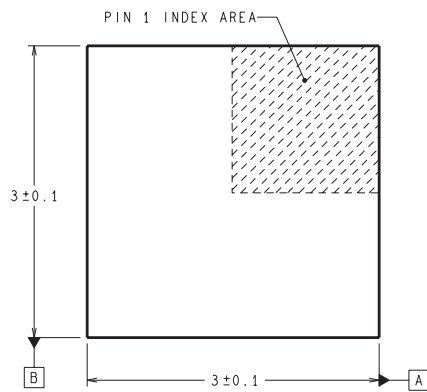
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

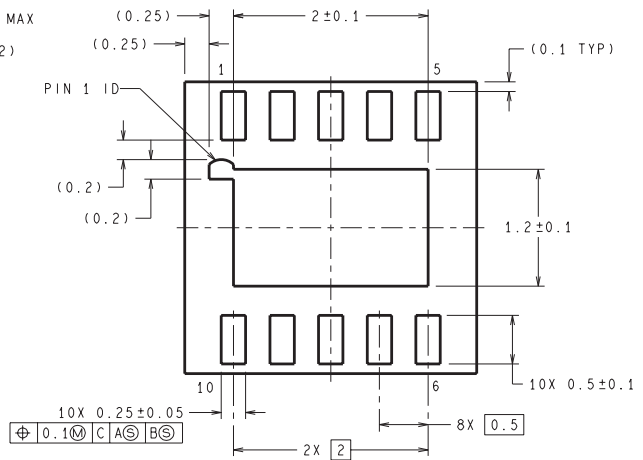
NGY0010A



RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS



DIMENSIONS ARE IN MILLIMETERS



LDA10A (Rev B)

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