

# CDCE(L)949: Flexible Low Power LVCMOS Clock Generator

## With SSC Support for EMI Reduction

### 1 Features

- Member of programmable clock generator family
  - CDCE913: 1 PLLs, 3 outputs
  - CDCE925: 2 PLLs, 5 outputs
  - CDCE937: 3 PLLs, 7 outputs
  - *CDCE949: 4 PLLs, 9 outputs*
- In-System programmability and EEPROM
  - Serial programmable volatile register
  - Nonvolatile EEPROM to store customer settings
- Flexible input clocking concept
  - External crystal: 8MHz to 32MHz
  - On-chip VCXO pull-range:  $\pm 150$ ppm
  - Single-ended LVCMOS up to 160MHz
- Free selectable output frequency up to 230MHz
- Low-noise PLL core
  - PLL loop filter components integrated
  - Low period jitter: 60ps (typical)
- Separate output supply pins
  - CDCE949: 3.3V and 2.5V
  - CDCEL949: 1.8V
- Flexible clock driver
  - Three user-definable control inputs [S0/S1/S2] (for example: SSC selection, frequency switching, output enable or power down)
  - Generates highly accurate clocks for video, audio, USB, IEEE1394, RFID, Bluetooth®, WLAN, Ethernet™, and GPS
  - Generates common clock frequencies used with TI-DaVinci™, OMAP™, DSPs
  - Programmable SSC modulation
  - Enables 0ppm clock generation
- 1.8V device core supply
- Wide temperature range:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Packaged in TSSOP
- Development and programming kit for easy PLL design and programming (TI Pro-Clock™)

### 2 Applications

- D-TVs
- STBs
- IP-STBs
- DVD players
- DVD recorders
- Printers

### 3 Description

The CDCE949 and CDCEL949 are modular PLL-based low cost, high-performance, programmable clock synthesizers, multipliers and dividers. These devices generate up to nine output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230MHz, using up to four independent configurable PLLs.

The CDCE949 has separate output supply pins ( $V_{DDOUT}$ ): 1.8V for the CDCEL949 and 2.5V to 3.3V for the CDCE949.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0pF to 20pF. Additionally, an on-chip VCXO is selectable, allowing synchronization of the output frequency to an external control signal, that is, a PWM signal.

The deep M/N divider ratio allows the generation of 0ppm audio or video, networking (WLAN, Bluetooth™, Ethernet, GPS) or Interface (USB, IEEE1394, Memory Stick) clocks from a reference input frequency, such as 27MHz.

All PLLs support SSC (Spread-Spectrum Clocking). SSC can be Center-Spread or Down-Spread clocking. This is a common technique to reduce electromagnetic interference (EMI).

Based on the PLL frequency and the divider settings, the internal loop-filter components are automatically adjusted to achieve high stability, and to optimize the jitter-transfer characteristics of each PLL.

#### Package Information

| PART NUMBER         | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|---------------------|------------------------|-----------------------------|
| CDCE949<br>CDCEL949 | PW (TSSOP, 24)         | 7.8mm × 6.4mm               |

(1) For all available packages, see [Section 12](#).

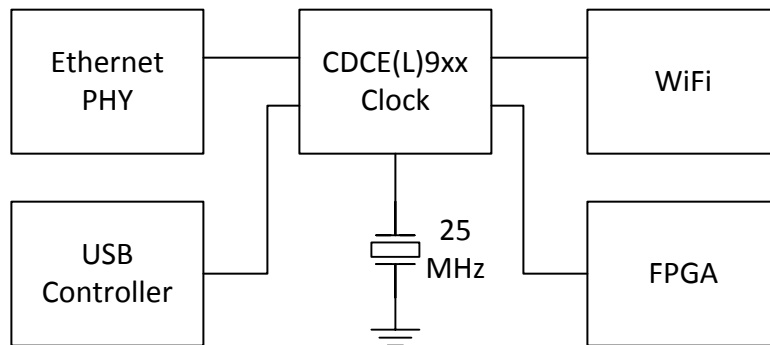
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



The device supports non-volatile EEPROM programming for easy customization of the device to the application. The CDCE949 is preset to a factory-default configuration. The device can be reprogrammed to a different application configuration before PCB assembly, or reprogrammed by in-system programming. All device settings are programmable through the SDA and SCL bus, a 2-wire serial interface.

Three programmable control inputs, S0, S1 and S2, can be used to control various aspects of operation including frequency selection, changing the SSC parameters to lower EMI, PLL bypass, power down, and choosing between low level or 3-state for the output-disable function.

The CDCE949 operates in a 1.8V environment within a temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



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**Typical Application Schematic**

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## 4 Pin Configuration and Functions

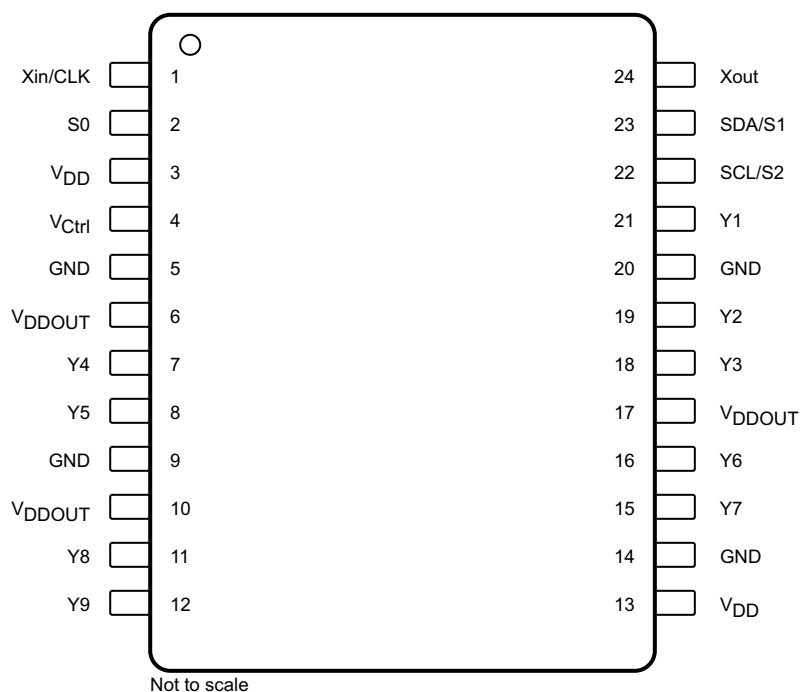


Figure 4-1. PW Package 24-Pin TSSOP (Top View)

Table 4-1. Pin Functions

| PIN                |              | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                        |
|--------------------|--------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME               | NO.          |                     |                                                                                                                                                                                                    |
| GND                | 5, 9, 14, 20 | G                   | Ground                                                                                                                                                                                             |
| SCL/S2             | 22           | I                   | <b>SCL</b> : Serial clock input (default configuration), LVCMOS; internal pullup 500 kΩ; or <b>S2</b> : User-programmable control input; LVCMOS inputs; internal pullup 500 kΩ                     |
| SDA/S1             | 23           | I/O                 | <b>SDA</b> : Bidirectional serial data input/output (default configuration), LVCMOS; internal pullup 500 kΩ; or <b>S1</b> : User-programmable control input; LVCMOS inputs; internal pullup 500 kΩ |
| S0                 | 2            | I                   | User-programmable control input S0; LVCMOS inputs; internal pullup 500 kΩ                                                                                                                          |
| V <sub>Ctrl</sub>  | 4            | I                   | VCXO control voltage (leave open or pull up when not used)                                                                                                                                         |
| V <sub>DD</sub>    | 3, 13        | P                   | 1.8-V power supply for the device                                                                                                                                                                  |
| V <sub>DDOUT</sub> | 6, 10, 17    | P                   | <b>CDCEL949</b> : 1.8-V supply for all outputs                                                                                                                                                     |
|                    |              |                     | <b>CDCE949</b> : 3.3-V or 2.5-V supply for all outputs                                                                                                                                             |
| Xin/CLK            | 1            | I                   | Crystal oscillator input or LVCMOS clock input (selectable through SDA/SCL bus)                                                                                                                    |
| Xout               | 24           | O                   | Crystal oscillator output (leave open or pull up when not used)                                                                                                                                    |
| Y1                 | 21           | O                   | LVCMOS output                                                                                                                                                                                      |
| Y2                 | 19           |                     |                                                                                                                                                                                                    |
| Y3                 | 18           |                     |                                                                                                                                                                                                    |
| Y4                 | 7            |                     |                                                                                                                                                                                                    |
| Y5                 | 8            |                     |                                                                                                                                                                                                    |
| Y6                 | 16           |                     |                                                                                                                                                                                                    |
| Y7                 | 15           |                     |                                                                                                                                                                                                    |
| Y8                 | 11           |                     |                                                                                                                                                                                                    |
| Y9                 | 12           |                     |                                                                                                                                                                                                    |

(1) G = Ground, I = Input, O = Output, P = Power

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                                       | MIN  | MAX                      | UNIT |
|------------------|-----------------------------------------------------------------------|------|--------------------------|------|
| V <sub>DD</sub>  | Supply voltage                                                        | −0.5 | 2.5                      | V    |
| V <sub>I</sub>   | Input voltage <sup>(2) (3)</sup>                                      | −0.5 | V <sub>DD</sub> + 0.5    | V    |
| V <sub>O</sub>   | Output voltage <sup>(2)</sup>                                         | −0.5 | V <sub>DDOUT</sub> + 0.5 | V    |
| I <sub>I</sub>   | Input current (V <sub>I</sub> < 0, V <sub>I</sub> > V <sub>DD</sub> ) |      | 20                       | mA   |
| I <sub>O</sub>   | Continuous output current                                             |      | 50                       | mA   |
| T <sub>J</sub>   | Junction temperature                                                  |      | 125                      | °C   |
| T <sub>stg</sub> | Storage temperature                                                   | −65  | 150                      | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) SDA and SCL can go up to 3.6 V as stated in the *Recommended Operating Conditions* table.

### 5.2 ESD Ratings

|                    |                         | VALUE                                                                          | UNIT  |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1500 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

|                                       |                                                          |                                                                   | MIN                   | NOM                   | MAX                   | UNIT |
|---------------------------------------|----------------------------------------------------------|-------------------------------------------------------------------|-----------------------|-----------------------|-----------------------|------|
| V <sub>DD</sub>                       | Device supply voltage                                    |                                                                   | 1.7                   | 1.8                   | 1.9                   | V    |
| V <sub>DD(OUT)</sub>                  | Output Yx supply voltage                                 | CDCE949                                                           | 2.3                   |                       | 3.6                   | V    |
|                                       |                                                          | CDCEL949                                                          | 1.7                   |                       | 1.9                   |      |
| V <sub>IL</sub>                       | Low level input voltage LVCMOS                           |                                                                   |                       |                       | 0.3 × V <sub>DD</sub> | V    |
| V <sub>IH</sub>                       | High level input voltage LVCMOS                          |                                                                   | 0.7 × V <sub>DD</sub> |                       |                       | V    |
| V <sub>I(thresh)</sub>                | Input voltage threshold LVCMOS                           |                                                                   |                       | 0.5 × V <sub>DD</sub> |                       | V    |
| V <sub>IS</sub>                       | Input voltage                                            | S0                                                                | 0                     |                       | 1.9                   | V    |
|                                       |                                                          | S1, S2, SDA, SCL,<br>V <sub>Ithresh</sub> = 0.5 × V <sub>DD</sub> | 0                     |                       | 3.6                   |      |
| V <sub>ICLK</sub>                     | Input voltage CLK                                        |                                                                   | 0                     |                       | 1.9                   | V    |
| I <sub>OH</sub> / I <sub>OL</sub>     | Output current                                           | V <sub>DDout</sub> = 3.3 V                                        |                       |                       | ±12                   | mA   |
|                                       |                                                          | V <sub>DDout</sub> = 2.5 V                                        |                       |                       | ±10                   | mA   |
|                                       |                                                          | V <sub>DDout</sub> = 1.8 V                                        |                       |                       | ±8                    | mA   |
| C <sub>L</sub>                        | Output load LVCMOS                                       |                                                                   |                       |                       | 10                    | pF   |
| T <sub>A</sub>                        | Operating free-air temperature                           |                                                                   | −40                   |                       | 85                    | °C   |
| <b>CRYSTAL AND VCXO<sup>(1)</sup></b> |                                                          |                                                                   |                       |                       |                       |      |
| f <sub>Xtal</sub>                     | Crystal Input frequency (fundamental mode)               |                                                                   | 8                     | 27                    | 32                    | MHz  |
| ESR                                   | Effective series resistance                              |                                                                   |                       |                       | 100                   | Ω    |
| f <sub>PR</sub>                       | Pulling (0 V ≤ V <sub>Ctrl</sub> ≤ 1.8 V) <sup>(2)</sup> |                                                                   | ±120                  | ±150                  |                       | ppm  |
| V <sub>(Ctrl)</sub>                   | Frequency control voltage                                |                                                                   | 0                     |                       | V <sub>DD</sub>       | V    |
| C <sub>0</sub> /C <sub>1</sub>        | Pullability ratio                                        |                                                                   |                       |                       | 220                   |      |

|                                                         | MIN | NOM | MAX | UNIT |
|---------------------------------------------------------|-----|-----|-----|------|
| C <sub>L</sub> On-chip load capacitance at Xin and Xout | 0   |     | 20  | pF   |

- (1) For more information about VCXO configuration and crystal recommendation, see [VCXO Application Guideline for CDCE\(L\)9xx Family](#) (SCAA085).
- (2) Pulling range depends on crystal type, on-chip crystal load capacitance and PCB stray capacitance; pulling range of min ±120 ppm applies for crystal listed in [VCXO Application Guideline for CDCE\(L\)9xx Family](#) (SCAA085).

## 5.4 Thermal Information

| THERMAL METRIC <sup>(2)</sup>                                       |                   | CDCEx949   | UNIT |
|---------------------------------------------------------------------|-------------------|------------|------|
|                                                                     |                   | PW (TSSOP) |      |
|                                                                     |                   | 24 PINS    |      |
| $\theta_{JA}$ Junction-to-ambient thermal resistance <sup>(1)</sup> | Airflow 0 (LFM)   | 91         | °C/W |
|                                                                     | Airflow 150 (LFM) | 75         |      |
|                                                                     | Airflow 200 (LFM) | 74         |      |
|                                                                     | Airflow 250 (LFM) | 73         |      |
|                                                                     | Airflow 500 (LFM) | 65         |      |
| $\theta_{JTop}$ Junction-to-case (top) thermal resistance           |                   | 0.5        | °C/W |
| $\theta_{JB}$ Junction-to-board thermal resistance                  |                   | 52         | °C/W |
| $\Psi_{JT}$ Junction-to-top characterization parameter              |                   | 0.5        | °C/W |
| $\Psi_{JB}$ Junction-to-board characterization parameter            |                   | 50.1       | °C/W |
| $\theta_{JBot}$ Junction-to-case (bottom) thermal resistance        |                   | 50         | °C/W |

- (1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
- (2) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                                                            | TEST CONDITIONS                                                                             | MIN                                    | TYP <sup>(1)</sup> | MAX  | UNIT |
|------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|----------------------------------------|--------------------|------|------|
| I <sub>DD</sub> Supply current (see <a href="#">Figure 5-1</a> )                                     | All outputs off, f <sub>CLK</sub> = 27 MHz, f <sub>VCO</sub> = 135 MHz                      | All PLLs on                            | 38                 |      | mA   |
|                                                                                                      |                                                                                             | Per PLL                                | 9                  |      |      |
| I <sub>DD(OUT)</sub> Supply current (see <a href="#">Figure 5-2</a> and <a href="#">Figure 5-3</a> ) | No load, all outputs on, f <sub>out</sub> = 27 MHz                                          | CDCE949<br>V <sub>DDOUT</sub> = 3.3 V  | 4                  |      | mA   |
|                                                                                                      |                                                                                             | CDCEL949<br>V <sub>DDOUT</sub> = 1.8 V | 2                  |      |      |
| I <sub>DD(PD)</sub> Power down current                                                               | Every circuit powered down except SDA/SCL, f <sub>IN</sub> = 0 MHz, V <sub>DD</sub> = 1.9 V |                                        | 50                 |      | μA   |
| V <sub>(PUC)</sub> Supply voltage V <sub>DD</sub> threshold for power up control circuit             |                                                                                             | 0.85                                   |                    | 1.45 | V    |
| f <sub>VCO</sub> VCO frequency range of PLL                                                          |                                                                                             | 80                                     |                    | 230  | MHz  |
| f <sub>OUT</sub> LVCMOS output frequency                                                             |                                                                                             | 230                                    |                    |      | MHz  |
| <b>LVCMOS</b>                                                                                        |                                                                                             |                                        |                    |      |      |
| V <sub>IK</sub> LVCMOS input voltage                                                                 | V <sub>DD</sub> = 1.7 V, I <sub>I</sub> = -18 mA                                            |                                        |                    | -1.2 | V    |
| I <sub>I</sub> LVCMOS input current                                                                  | V <sub>I</sub> = 0 V or V <sub>DD</sub> , V <sub>DD</sub> = 1.9 V                           |                                        |                    | ±5   | μA   |
| I <sub>IH</sub> LVCMOS input current for S0/S1/S2                                                    | V <sub>I</sub> = V <sub>DD</sub> , V <sub>DD</sub> = 1.9 V                                  |                                        |                    | 5    | μA   |
| I <sub>IL</sub> LVCMOS input current for S0/S1/S2                                                    | V <sub>I</sub> = 0 V, V <sub>DD</sub> = 1.9 V                                               |                                        |                    | -4   | μA   |

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                        |                                               | TEST CONDITIONS                                       | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|--------------------------------------------------|-----------------------------------------------|-------------------------------------------------------|-----|--------------------|-----|------|
| C <sub>I</sub>                                   | Input capacitance at Xin/Clk                  | V <sub>ICLK</sub> = 0 V or V <sub>DD</sub>            |     | 6                  |     | pF   |
|                                                  | Input capacitance at Xout                     | V <sub>IXout</sub> = 0 V or V <sub>DD</sub>           |     | 2                  |     |      |
|                                                  | Input capacitance at S0/S1/S2                 | V <sub>IS</sub> = 0 V or V <sub>DD</sub>              |     | 3                  |     |      |
| CDCE949 – LVCMOS FOR V <sub>DDOUT</sub> = 3.3 V  |                                               |                                                       |     |                    |     |      |
| V <sub>OH</sub>                                  | LVCMOS high-level output voltage              | V <sub>DDOUT</sub> = 3 V, I <sub>OH</sub> = –0.1 mA   | 2.9 |                    |     | V    |
|                                                  |                                               | V <sub>DDOUT</sub> = 3 V, I <sub>OH</sub> = –8 mA     | 2.4 |                    |     |      |
|                                                  |                                               | V <sub>DDOUT</sub> = 3 V, I <sub>OH</sub> = –12 mA    | 2.2 |                    |     |      |
| V <sub>OL</sub>                                  | LVCMOS low-level output voltage               | V <sub>DDOUT</sub> = 3 V, I <sub>OL</sub> = 0.1 mA    |     |                    | 0.1 | V    |
|                                                  |                                               | V <sub>DDOUT</sub> = 3 V, I <sub>OL</sub> = 8 mA      |     |                    | 0.5 |      |
|                                                  |                                               | V <sub>DDOUT</sub> = 3 V, I <sub>OL</sub> = 12 mA     |     |                    | 0.8 |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub>           | Propagation delay                             | PLL bypass                                            |     | 3.2                |     | ns   |
| t <sub>r</sub> /t <sub>f</sub>                   | Rise and fall time                            | V <sub>DDOUT</sub> = 3.3 V (20%–80%)                  |     | 0.6                |     | ns   |
| t <sub>jitter(cc)</sub>                          | Cycle-to-cycle jitter <sup>(2) (3)</sup>      | 1 PLL switching, Y2-to-Y3                             |     | 60                 | 90  | ps   |
|                                                  |                                               | 4 PLLs switching, Y2-to-Y9                            |     | 120                | 170 |      |
| t <sub>jitter(per)</sub>                         | Peak-to-peak period jitter <sup>(2) (3)</sup> | 1 PLL switching, Y2-to-Y3                             |     | 70                 | 100 | ps   |
|                                                  |                                               | 4 PLLs switching, Y2-to-Y9                            |     | 130                | 180 |      |
| t <sub>sk(o)</sub>                               | Output skew <sup>(4)</sup>                    | f <sub>OUT</sub> = 50 MHz, Y1-to-Y3                   |     |                    | 60  | ps   |
|                                                  |                                               | f <sub>OUT</sub> = 50 MHz, Y2-to-Y5 or Y6-to-Y9       |     |                    | 160 |      |
| odc                                              | Output duty cycle <sup>(5)</sup>              | f <sub>VCO</sub> = 100 MHz, Pdiv = 1                  | 45% |                    | 55% |      |
| CDCE949 – LVCMOS FOR V <sub>DDOUT</sub> = 2.5 V  |                                               |                                                       |     |                    |     |      |
| V <sub>OH</sub>                                  | LVCMOS high-level output voltage              | V <sub>DDOUT</sub> = 2.3 V, I <sub>OH</sub> = –0.1 mA | 2.2 |                    |     | V    |
|                                                  |                                               | V <sub>DDOUT</sub> = 2.3 V, I <sub>OH</sub> = –6 mA   | 1.7 |                    |     |      |
|                                                  |                                               | V <sub>DDOUT</sub> = 2.3 V, I <sub>OH</sub> = –10 mA  | 1.6 |                    |     |      |
| V <sub>OL</sub>                                  | LVCMOS low-level output voltage               | V <sub>DDOUT</sub> = 2.3 V, I <sub>OL</sub> = 0.1 mA  |     |                    | 0.1 | V    |
|                                                  |                                               | V <sub>DDOUT</sub> = 2.3 V, I <sub>OL</sub> = 6 mA    |     |                    | 0.5 |      |
|                                                  |                                               | V <sub>DDOUT</sub> = 2.3 V, I <sub>OL</sub> = 10 mA   |     |                    | 0.7 |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub>           | Propagation delay                             | PLL bypass                                            |     | 3.4                |     | ns   |
| t <sub>r</sub> /t <sub>f</sub>                   | Rise and fall time                            | V <sub>DDOUT</sub> = 2.5 V (20%–80%)                  |     | 0.8                |     | ns   |
| t <sub>jitter(cc)</sub>                          | Cycle-to-cycle jitter <sup>(2) (3)</sup>      | 1 PLL switching, Y2-to-Y3                             |     | 60                 | 90  | ps   |
|                                                  |                                               | 4 PLLs switching, Y2-to-Y9                            |     | 120                | 170 |      |
| t <sub>jitter(per)</sub>                         | Peak-to-peak period jitter <sup>(2) (3)</sup> | 1 PLL switching, Y2-to-Y3                             |     | 70                 | 100 | ps   |
|                                                  |                                               | 4 PLLs switching, Y2-to-Y9                            |     | 130                | 180 |      |
| t <sub>sk(o)</sub>                               | Output skew <sup>(4)</sup>                    | f <sub>OUT</sub> = 50 MHz, Y1-to-Y3                   |     |                    | 60  | ps   |
|                                                  |                                               | f <sub>OUT</sub> = 50 MHz, Y2-to-Y5 or Y6-to-Y9       |     |                    | 160 |      |
| odc                                              | Output duty cycle <sup>(5)</sup>              | f <sub>VCO</sub> = 100 MHz, Pdiv = 1                  | 45% |                    | 55% |      |
| CDCEL949 – LVCMOS FOR V <sub>DDOUT</sub> = 1.8 V |                                               |                                                       |     |                    |     |      |
| V <sub>OH</sub>                                  | LVCMOS high-level output voltage              | V <sub>DDOUT</sub> = 1.7 V, I <sub>OH</sub> = –0.1 mA | 1.6 |                    |     | V    |
|                                                  |                                               | V <sub>DDOUT</sub> = 1.7 V, I <sub>OH</sub> = –4 mA   | 1.4 |                    |     |      |
|                                                  |                                               | V <sub>DDOUT</sub> = 1.7 V, I <sub>OH</sub> = –8 mA   | 1.1 |                    |     |      |
| V <sub>OL</sub>                                  | LVCMOS low-level output voltage               | V <sub>DDOUT</sub> = 1.7 V, I <sub>OL</sub> = 0.1 mA  |     |                    | 0.1 | V    |
|                                                  |                                               | V <sub>DDOUT</sub> = 1.7 V, I <sub>OL</sub> = 4 mA    |     |                    | 0.3 |      |
|                                                  |                                               | V <sub>DDOUT</sub> = 1.7 V, I <sub>OL</sub> = 8 mA    |     |                    | 0.6 |      |

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                |                                               | TEST CONDITIONS                                  | MIN                 | TYP <sup>(1)</sup>  | MAX                 | UNIT |
|--------------------------|-----------------------------------------------|--------------------------------------------------|---------------------|---------------------|---------------------|------|
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation delay                             | PLL bypass                                       |                     | 2.6                 |                     | ns   |
| $t_r/t_f$                | Rise and fall time                            | $V_{DDOUT} = 1.8\text{ V}$ (20%–80%)             |                     | 0.7                 |                     | ns   |
| $t_{jit(cc)}$            | Cycle-to-cycle jitter <sup>(2) (3)</sup>      | 1 PLL switching, Y2-to-Y3                        |                     | 70                  | 120                 | ps   |
|                          |                                               | 4 PLLs switching, Y2-to-Y9                       |                     | 120                 | 170                 |      |
| $t_{jit(per)}$           | Peak-to-peak period jitter <sup>(2) (3)</sup> | 1 PLL switching, Y2-to-Y3                        |                     | 90                  | 140                 | ps   |
|                          |                                               | 4 PLLs switching, Y2-to-Y9                       |                     | 130                 | 190                 |      |
| $t_{sk(o)}$              | Output skew <sup>(4)</sup>                    | $f_{OUT} = 50\text{ MHz}$ , Y1-to-Y3             |                     |                     | 60                  | ps   |
|                          |                                               | $f_{OUT} = 50\text{ MHz}$ , Y2-to-Y5 or Y6-to-Y9 |                     |                     | 160                 |      |
| odc                      | Output duty cycle <sup>(5)</sup>              | $f_{VCO} = 100\text{ MHz}$ , Pdiv = 1            | 45%                 |                     | 55%                 |      |
| <b>SDA AND SCL</b>       |                                               |                                                  |                     |                     |                     |      |
| $V_{IK}$                 | SCL and SDA input clamp voltage               | $V_{DD} = 1.7\text{ V}$ , $I_I = -18\text{ mA}$  |                     |                     | -1.2                | V    |
| $I_{IH}$                 | SCL and SDA input current                     | $V_I = V_{DD}$ , $V_{DD} = 1.9\text{ V}$         |                     |                     | ±10                 | µA   |
| $V_{IH}$                 | SDA/SCL input high voltage <sup>(6)</sup>     |                                                  | $0.7 \times V_{DD}$ |                     |                     | V    |
| $V_{IL}$                 | SDA/SCL input low voltage <sup>(6)</sup>      |                                                  |                     | $0.3 \times V_{DD}$ |                     | V    |
| $V_{OL}$                 | SDA low-level output voltage                  | $I_{OL} = 3\text{ mA}$ , $V_{DD} = 1.7\text{ V}$ |                     |                     | $0.2 \times V_{DD}$ | V    |
| $C_I$                    | SCL/SDA input capacitance                     | $V_I = 0\text{ V}$ or $V_{DD}$                   |                     | 3                   | 10                  | pF   |

(1) All typical values are at respective nominal  $V_{DD}$ .

(2) 10000 cycles.

(3) Jitter depends on device configuration. Data is taken under the following conditions: 1-PLL:  $f_{IN} = 27\text{ MHz}$ , Y2/3 = 27 MHz, (measured at Y2), 4-PLL:  $f_{IN} = 27\text{ MHz}$ , Y2/3 = 27 MHz, (measured at Y2), Y4/5 = 16.384 MHz, Y6/7 = 74.25 MHz, Y8/9 = 48 MHz.

(4) The  $t_{sk(o)}$  specification is only valid for equal loading of each bank of outputs and outputs are generated from the same divider; data sampled on rising edge ( $t_r$ ).

(5) odc depends on output rise- and fall-time ( $t_r/t_f$ ).

(6) SDA and SCL pins are 3.3-V tolerant.

## 5.6 EEPROM Specification

|       |                              | MIN  | TYP | MAX | UNIT   |
|-------|------------------------------|------|-----|-----|--------|
| EEcyc | Programming cycles of EEPROM | 1000 |     |     | cycles |
| EEret | Data retention               | 10   |     |     | years  |

## 5.7 Timing Requirements: CLK\_IN

|                     |                                            | MIN             | NOM | MAX | UNIT |
|---------------------|--------------------------------------------|-----------------|-----|-----|------|
| $f_{CLK}$           | LVCMOS clock input frequency               | PLL bypass mode | 0   | 160 | MHz  |
|                     |                                            | PLL mode        | 8   | 160 |      |
| $t_r / t_f$         | Rise and fall time CLK signal (20% to 80%) |                 |     | 3   | ns   |
| duty <sub>CLK</sub> | Duty cycle CLK at $V_{DD} / 2$             | 40%             |     | 60% |      |

## 5.8 Timing Requirements: SDA/SCL

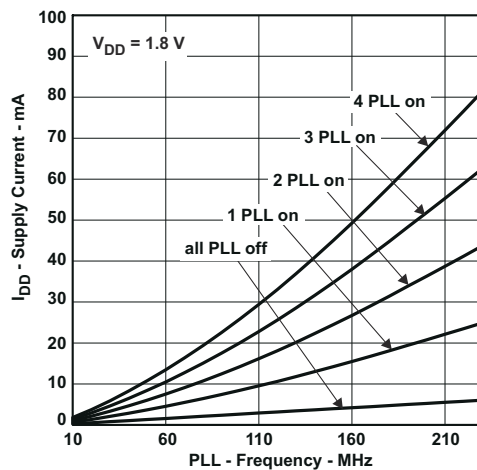
over operating free-air temperature range (unless otherwise noted; see Figure 7-9)

|                 |                                            | MIN           | NOM | MAX | UNIT |
|-----------------|--------------------------------------------|---------------|-----|-----|------|
| $f_{SCL}$       | SCL clock frequency                        | Standard mode | 0   | 100 | kHz  |
|                 |                                            | Fast mode     | 0   | 400 |      |
| $t_{su(START)}$ | START setup time (SCL high before SDA low) | Standard mode | 4.7 |     | µs   |
|                 |                                            | Fast mode     | 0.6 |     |      |

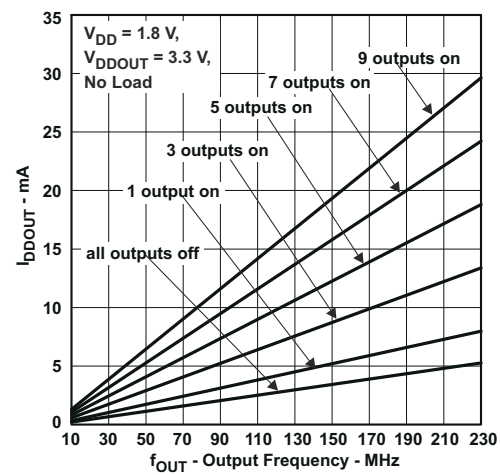
over operating free-air temperature range (unless otherwise noted; see [Figure 7-9](#))

|                |                                                  |               | MIN | NOM | MAX  | UNIT    |
|----------------|--------------------------------------------------|---------------|-----|-----|------|---------|
| $t_{h(START)}$ | START hold time (SCL low after SDA low)          | Standard mode | 4   |     |      | $\mu s$ |
|                |                                                  | Fast mode     | 0.6 |     |      |         |
| $t_{w(SCLL)}$  | SCL low-pulse duration                           | Standard mode | 4.7 |     |      | $\mu s$ |
|                |                                                  | Fast mode     | 1.3 |     |      |         |
| $t_{w(SCLH)}$  | SCL high-pulse duration                          | Standard mode | 4   |     |      | $\mu s$ |
|                |                                                  | Fast mode     | 0.6 |     |      |         |
| $t_{h(SDA)}$   | SDA hold time (SDA valid after SCL low)          | Standard mode | 0   |     | 3.45 | $\mu s$ |
|                |                                                  | Fast mode     | 0   |     | 0.9  |         |
| $t_{su(SDA)}$  | SDA setup time                                   | Standard mode | 250 |     |      | ns      |
|                |                                                  | Fast mode     | 100 |     |      |         |
| $t_r$          | SCL/SDA input rise time                          | Standard mode |     |     | 1000 | ns      |
|                |                                                  | Fast mode     |     |     | 300  |         |
| $t_f$          | SCL/SDA input fall time                          |               |     |     | 300  | ns      |
| $t_{su(STOP)}$ | STOP setup time                                  | Standard mode | 4   |     |      | $\mu s$ |
|                |                                                  | Fast mode     | 0.6 |     |      |         |
| $t_{BUF}$      | Bus free time between a STOP and START condition | Standard mode | 4.7 |     |      | $\mu s$ |
|                |                                                  | Fast mode     | 1.3 |     |      |         |

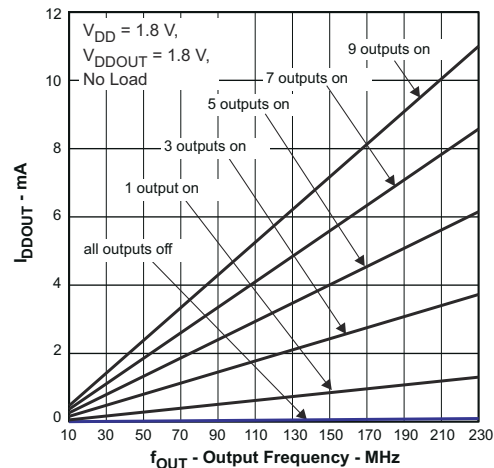
## 5.9 Typical Characteristics



**Figure 5-1. CDCE949 Supply Current vs PLL Frequency**

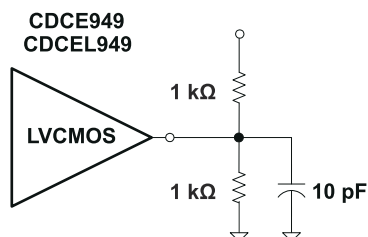


**Figure 5-2. CDCE949 Output Current vs Output Frequency**



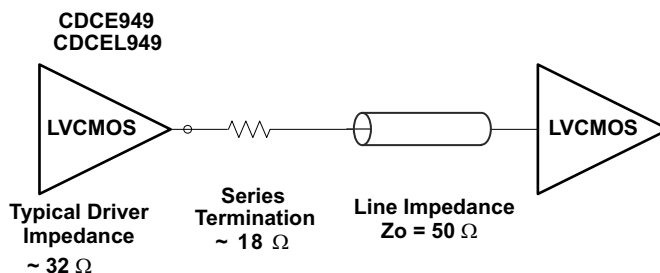
**Figure 5-3. CDCEL949 Output Current vs Output Frequency**

## 6 Parameter Measurement Information



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**Figure 6-1. Test Load**



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**Figure 6-2. Test Load for 50-Ω Board Environment**

## 7 Detailed Description

### 7.1 Overview

The CDCE949 and CDCEL949 devices are modular PLL-based, low-cost, high-performance, programmable clock synthesizers, multipliers, and dividers. They generate up to nine output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using one of the four integrated configurable PLLs.

The CDCE949 has separate output supply pins,  $V_{DDOUT}$ , which is 1.8 V for CDCEL949 and 2.5 V to 3.3 V for CDCE949.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 to 20 pF. Additionally, a selectable on-chip VCXO allows synchronization of the output frequency to an external control signal, that is, the PWM signal.

The deep M/N divider ratio allows the generation of 0-ppm audio and video, networking (WLAN, Bluetooth, Ethernet, GPS), or Interface (USB, IEEE1394, memory stick) clocks from a reference input frequency such as 27 MHz.

All PLLs support spread-spectrum clocking (SSC). SSC can be center-spread or down-spread clocking. This is a common technique to reduce electro-magnetic interference (EMI).

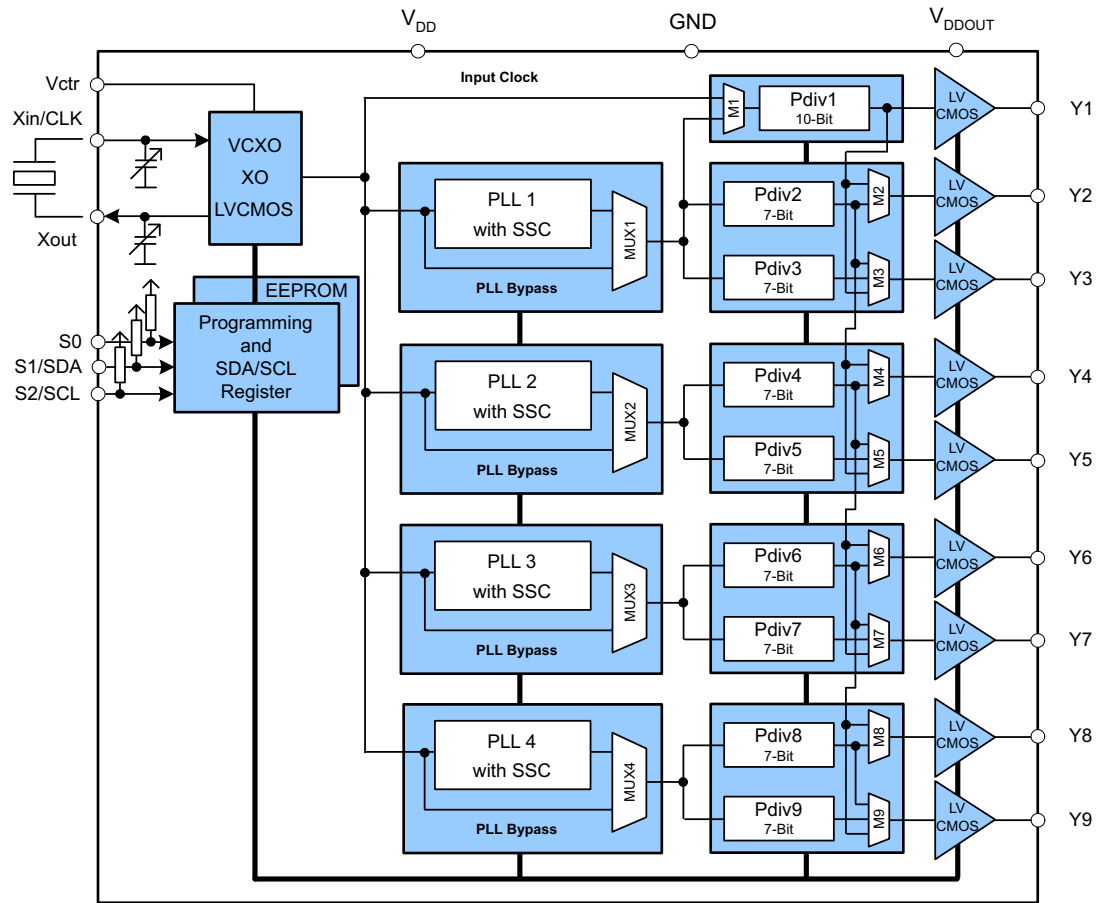
Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability, and to optimize the jitter-transfer characteristics of each PLL.

The device supports non-volatile EEPROM programming for easy customization of the device to the application. The internal EEPROM of the CDCE949 is preset to a factory-default configuration (see [Default Device Setting](#)). The EEPROM can be reprogrammed to a different application configuration before PCB assembly, or reprogrammed by in-system programming. All device settings are programmable through the SDA and SCL bus, a 2-wire serial interface.

Three programmable control inputs, S0, S1 and S2, can be used to control various aspects of operation including frequency selection, changing the SSC parameters to lower EMI, PLL bypass, power down, and choosing between low level or 3-state for the output-disable function.

The CDCE949 operates in a 1.8-V environment within a temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

## 7.2 Functional Block Diagram



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## 7.3 Feature Description

### 7.3.1 Control Terminal Setting

The CDCE949 has three user-definable control terminals (S0, S1, and S2) which allow external control of device settings. They can be programmed to any of the following setting:

- Spread spectrum clocking selection → spread type and spread amount selection
- Frequency selection → switching between any of two user-defined frequencies
- Output state selection → output configuration and power down control

The user can predefine up to eight different control settings. [Table 7-1](#) and [Table 7-2](#) explain these settings.

**Table 7-1. Control Terminal Definition**

| EXTERNAL CONTROL BITS | PLL1 SETTING            |               |                        | PLL2 SETTING            |               |                        | PLL3 SETTING            |               |                        | PLL4 SETTING            |               |                        | Y1 SETTING                         |
|-----------------------|-------------------------|---------------|------------------------|-------------------------|---------------|------------------------|-------------------------|---------------|------------------------|-------------------------|---------------|------------------------|------------------------------------|
| Control Function      | PLL Frequency Selection | SSC Selection | Output Y2/Y3 Selection | PLL Frequency Selection | SSC Selection | Output Y4/Y5 Selection | PLL Frequency Selection | SSC Selection | Output Y6/Y7 Selection | PLL Frequency Selection | SSC Selection | Output Y8/Y9 Selection | Output Y1 and Power Down Selection |

**Table 7-2. PLLx Setting (Can Be Selected for Each PLL Individual)**

| SSC SELECTION (CENTER/DOWN) <sup>(1)</sup> |   |   |          |          |
|--------------------------------------------|---|---|----------|----------|
| SSCx [3-bits]                              |   |   | CENTER   | DOWN     |
| 0                                          | 0 | 0 | 0% (off) | 0% (off) |
| 0                                          | 0 | 1 | ±0.25%   | –0.25%   |

**Table 7-2. PLLx Setting (Can Be Selected for Each PLL Individual) (continued)**

| SSC SELECTION (CENTER/DOWN) <sup>(1)</sup>  |   |            |        |        |
|---------------------------------------------|---|------------|--------|--------|
| SSCx [3-bits]                               |   |            | CENTER | DOWN   |
| 0                                           | 1 | 0          | ±0.5%  | −0.5%  |
| 0                                           | 1 | 1          | ±0.75% | −0.75% |
| 1                                           | 0 | 0          | ±1%    | −1%    |
| 1                                           | 0 | 1          | ±1.25% | −1.25% |
| 1                                           | 1 | 0          | ±1.5%  | −1.5%  |
| 1                                           | 1 | 1          | ±2%    | −2%    |
| FREQUENCY SELECTION <sup>(2)</sup>          |   |            |        |        |
| FSx                                         |   | FUNCTION   |        |        |
| 0                                           |   | Frequency0 |        |        |
| 1                                           |   | Frequency1 |        |        |
| OUTPUT SELECTION <sup>(3)</sup> (Y2 ... Y9) |   |            |        |        |
| YxYx                                        |   | FUNCTION   |        |        |
| 0                                           |   | State0     |        |        |
| 1                                           |   | State1     |        |        |

- (1) Center/Down-Spread, Frequency0/1 and State0/1 are user-definable in PLLx Configuration Register
- (2) Frequency0 and Frequency1 can be any frequency within the specified  $f_{VCO}$  range
- (3) State0/1 selection is valid for both outputs of the corresponding PLL module and can be power down, 3-state, low, or active

**Table 7-3. Y1 Setting<sup>(1)</sup>**

| Y1 SELECTION |          |
|--------------|----------|
| Y1           | FUNCTION |
| 0            | State 0  |
| 1            | State 1  |

- (1) State0 and State1 are user definable in Generic Configuration Register and can be power down, 3-state, low, or active.

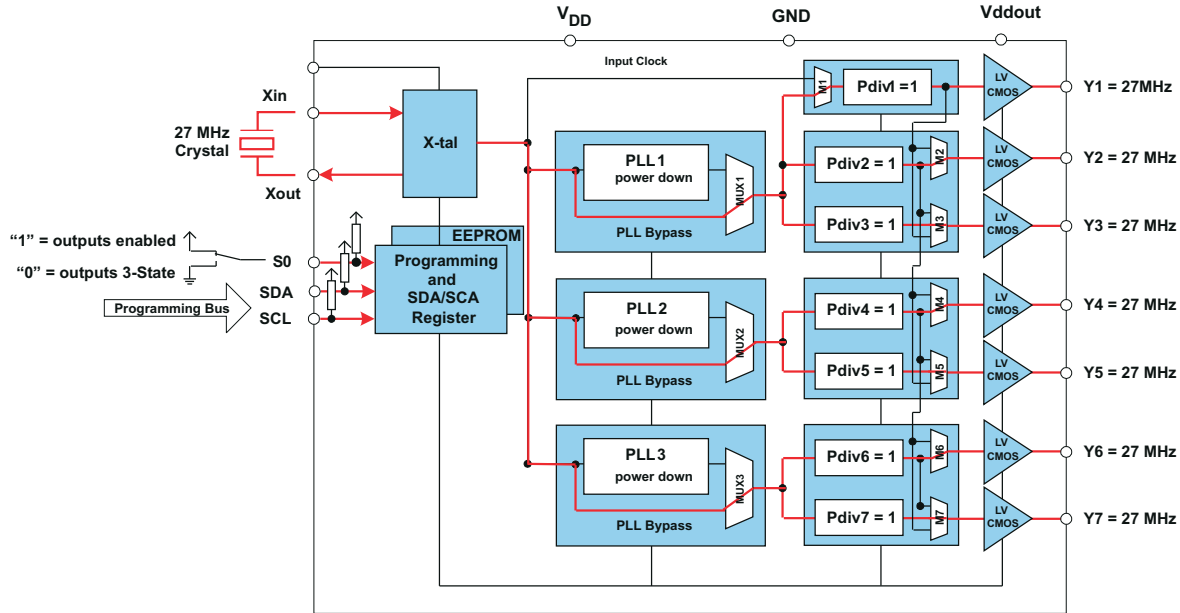
S1/SDA and S2/SCL pins of the CDCEx949 are dual function pins. In default configuration they are defined as SDA/SCL for the serial interface. They can be programmed as control-pins (S1/S2) by setting the relevant bits in the EEPROM. Note that the changes to the Control register (Bit [6] of Byte [02]) have no effect until they are written into the EEPROM.

Once they are set as control pins, the serial programming interface is no longer available. However, if  $V_{DDOUT}$  is forced to GND, the two control-pins, S1 and S2, temporally act as serial programming pins (SDA/SCL).

S0 is not a multi-use pin and is a control pin only.

### 7.3.2 Default Device Setting

The internal EEPROM of CDCEx949 is preconfigured as shown in [Figure 7-1](#) (the input frequency is passed through to the output as a default). This allows the device to operate in default mode without the extra production step of programming. The default setting appears after power is supplied or after power-down or power-up sequence until the setting is re-programmed by the user to a different application configuration. A new register setting is programmed through the serial SDA/SCL Interface.



**Figure 7-1. Default Device Setting**

Table 7-4 shows the factory default setting for the Control Terminal Register (external control pins). In normal operation, all 8 register settings are available, but in the default configuration only the first two settings (0 and 1) can be selected with S0, as S1 and S2 configured as programming pins in default mode.

**Table 7-4. Factory Default Setting for Control Terminal Register**

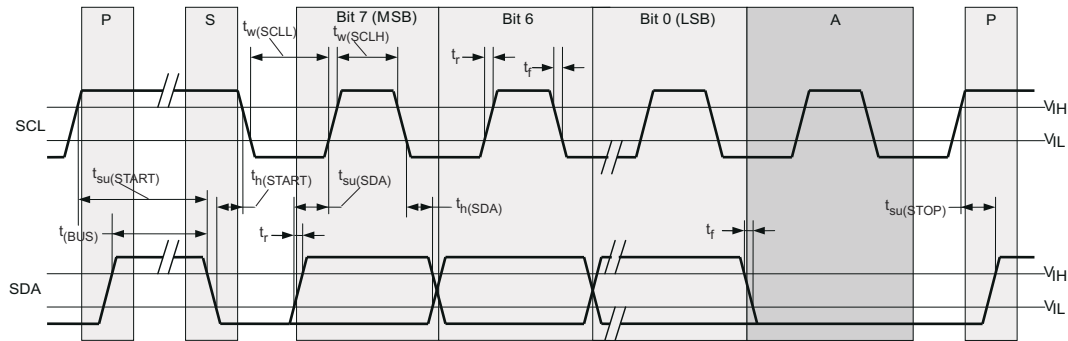
|                                      |                        |    | Y1            | PLL1 SETTING        |          |               | PLL2 SETTING        |          |               | PLL3 SETTING        |          |               | PLL3 SETTING        |          |               |
|--------------------------------------|------------------------|----|---------------|---------------------|----------|---------------|---------------------|----------|---------------|---------------------|----------|---------------|---------------------|----------|---------------|
| EXTERNAL CONTROL PINS <sup>(1)</sup> |                        |    | OUTPUT SELECT | FREQ. SELECT        | SSC SEL. | OUTPUT SELECT | FREQ. SELECT        | SSC SEL. | OUTPUT SELECT | FREQ. SELECT        | SSC SEL. | OUTPUT SELECT | FREQ. SELECT        | SSC SEL. | OUTPUT SELECT |
| S2                                   | S1                     | S0 | Y1            | FS1                 | SSC1     | Y2Y3          | FS2                 | SSC2     | Y4Y5          | FS3                 | SSC3     | Y6Y7          | FS4                 | SSC4     | Y8Y9          |
| SCL (I <sup>2</sup> C)               | SDA (I <sup>2</sup> C) | 0  | 3-state       | f <sub>VCO1_0</sub> | off      | 3-state       | f <sub>VCO2_0</sub> | off      | 3-state       | f <sub>VCO3_0</sub> | off      | 3-state       | f <sub>VCO4_0</sub> | off      | 3-state       |
| SCL (I <sup>2</sup> C)               | SDA (I <sup>2</sup> C) | 1  | enabled       | f <sub>VCO1_0</sub> | off      | enabled       | f <sub>VCO2_0</sub> | off      | enabled       | f <sub>VCO3_0</sub> | off      | enabled       | f <sub>VCO4_0</sub> | off      | enabled       |

(1) In default mode or when programmed respectively, S1 and S2 act as serial programming interface, SDA/SCL. They do not have any control-pin function but they are internally interpreted as if S1 = 0 and S2 = 0. However, S0 is a control-pin which in the default mode switches all outputs ON or OFF (as previously predefined).

### 7.3.3 SDA/SCL Serial Interface

The CDCE949 operates as a target device of the 2-wire serial SDA/SCL bus, compatible with the popular **SMBus** or **I<sup>2</sup>C Bus** specification. The device operates in the standard-mode transfer (up to 100 kbps) and fast-mode transfer (up to 400 kbps) and supports 7-bit addressing.

The S1/SDA and S2/SCL pins of the CDCE949 are dual function pins. In the default configuration they are used as SDA/SCL serial programming interface. They can be re-programmed as general-purpose control pins, S1 and S2, by changing the corresponding EEPROM setting, Byte 02, Bit [6].



**Figure 7-2. Timing Diagram for SDA/SCL Serial Control Interface**

### 7.3.4 Data Protocol

The device supports *Byte Write and Byte Read* and *Block Write and Block Read* operations.

For *Byte Write/Read* operations, the system controller can individually access addressed bytes.

For *Block Write/Read* operations, the bytes are accessed in sequential order from lowest to highest byte (with most significant bit first) with the ability to stop after any complete byte has been transferred. The numbers of Bytes read-out are defined by Byte Count in the Generic Configuration Register. At Block Read instruction all bytes defined in the Byte Count has to be readout to correctly finish the read cycle.

After a byte is sent, the byte is written into the internal register and is effective immediately. This applies to each transferred byte independent of whether this is a *Byte Write* or a *Block Write* sequence.

If the EEPROM Write Cycle is initiated, the internal SDA register contents are written into the EEPROM. During this write cycle, data is not accepted at the SDA/SCL bus until the write cycle is completed. However, data can be read during the programming sequence (Byte Read or Block Read). The programming status can be monitored by reading *EEPIP*, Byte 01–Bit [6].

The offset of the indexed byte is encoded in the command code, as described in [Table 7-5](#).

**Table 7-5. Target Receiver Address (7 Bits)**

| DEVICE   | A6 | A5 | A4 | A3 | A2 | A1 <sup>(1)</sup> | A0 <sup>(1)</sup> | R/ W |
|----------|----|----|----|----|----|-------------------|-------------------|------|
| CDCEx913 | 1  | 1  | 0  | 0  | 1  | 0                 | 1                 | 1/0  |
| CDCEx925 | 1  | 1  | 0  | 0  | 1  | 0                 | 0                 | 1/0  |
| CDCEx937 | 1  | 1  | 0  | 1  | 1  | 0                 | 1                 | 1/0  |
| CDCEx949 | 1  | 1  | 0  | 1  | 1  | 0                 | 0                 | 1/0  |

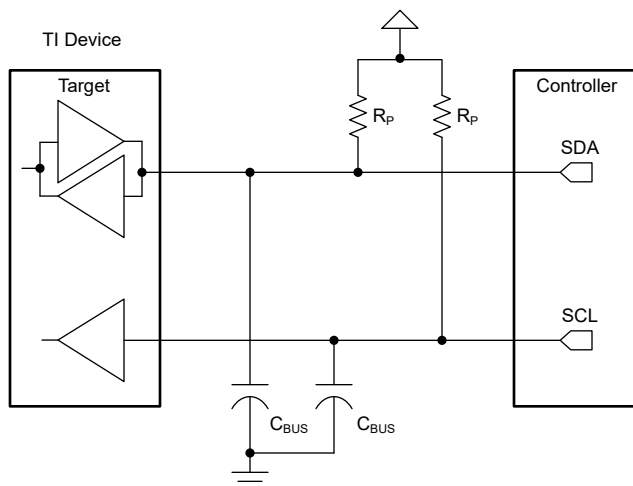
(1) Address bits A0 and A1 are programmable through the SDA/SCL bus (Byte 01, Bit [1:0]). This allows addressing up to 4 devices connected to the same SDA/SCL bus. The least-significant bit of the address byte designates a write or read operation.

## 7.4 Device Functional Modes

### 7.4.1 SDA/SCL Hardware Interface

[Figure 7-3](#) shows how the CDCEx949 clock synthesizer is connected to the SDA/SCL serial interface bus. Multiple devices can be connected to the bus but the speed may need to be reduced (400 kHz is the maximum) if many devices are connected.

Note that the pullup resistor value ( $R_P$ ) depends on the supply voltage, bus capacitance and number of connected devices. The recommended pullup value is 4.7 kΩ. The value must meet the minimum sink current of 3 mA at  $V_{OLmax} = 0.4$  V for the output stages (for more details, see [SMBus](#) or [I<sup>2</sup>C Bus](#) specification).



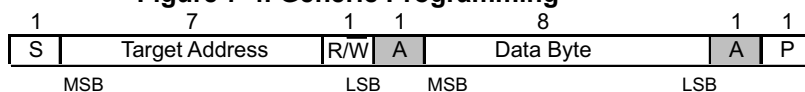
**Figure 7-3. SDA/SCL Hardware Interface**

## 7.5 Programming

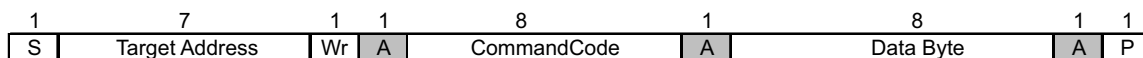
**Table 7-6. Command Code Definition**

| BIT   | DESCRIPTION                                                                      |
|-------|----------------------------------------------------------------------------------|
| 7     | 0 = Block Read or Block Write operation<br>1 = Byte Read or Byte Write operation |
| (6:0) | Byte Offset for Byte Read, Block Read, Byte Write and Block Write operation.     |

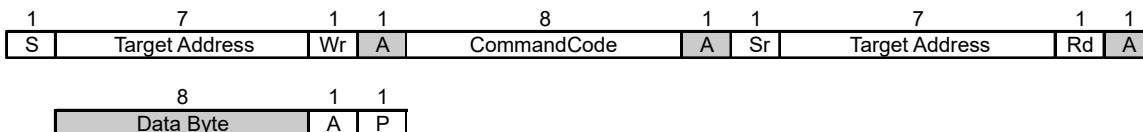
**Figure 7-4. Generic Programming**



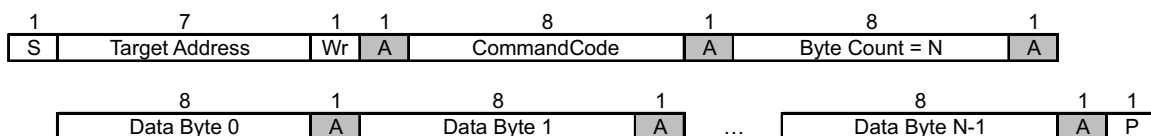
- S** Start Condition
- Sr** Repeated Start Condition
- R/W** 1 = Read (Rd) From CDCE9xx Device; 0 = Write (Wr) to CDCE9xxx
- A** Acknowledge (ACK = 0 and NACK =1)
- P** Stop Condition
- Controller-to-Target Transmission
- Sequence** Target-to-Controller Transmission



**Figure 7-5. Byte Write Protocol**

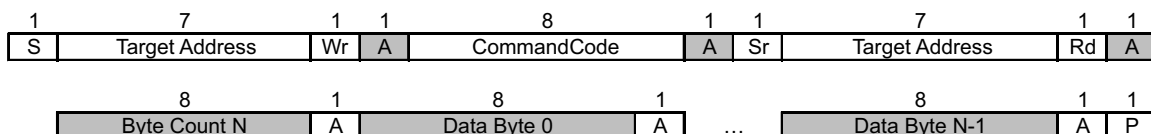


**Figure 7-6. Byte Read Protocol**

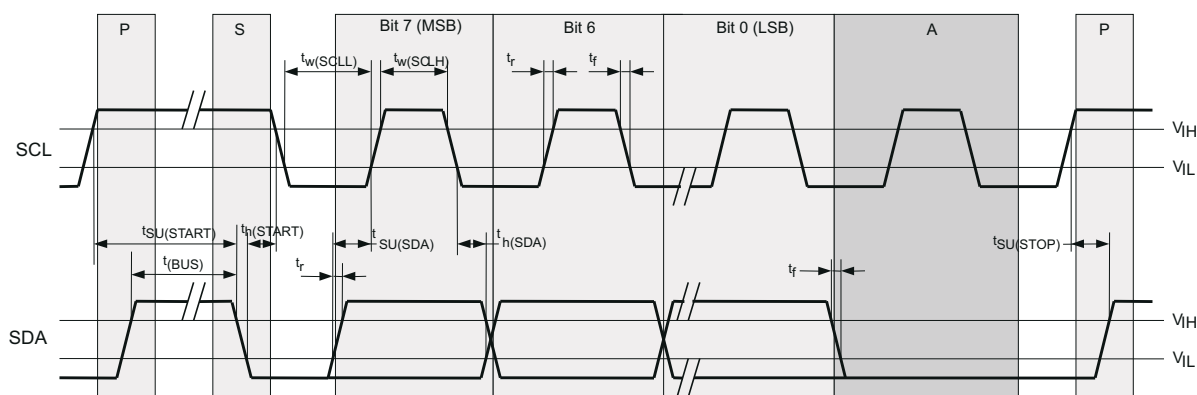


Data Byte 0 Bits [7:0] are reserved for Revision Code and Vendor Identification. The Data Byte 0 is used for internal test purpose and must not be overwritten.

**Figure 7-7. Block Write Programming**



**Figure 7-8. Block Read Protocol**



**Figure 7-9. Timing Diagram for the SDA/SCL Serial Control Interface**

## 8 Application and Implementation

### Note

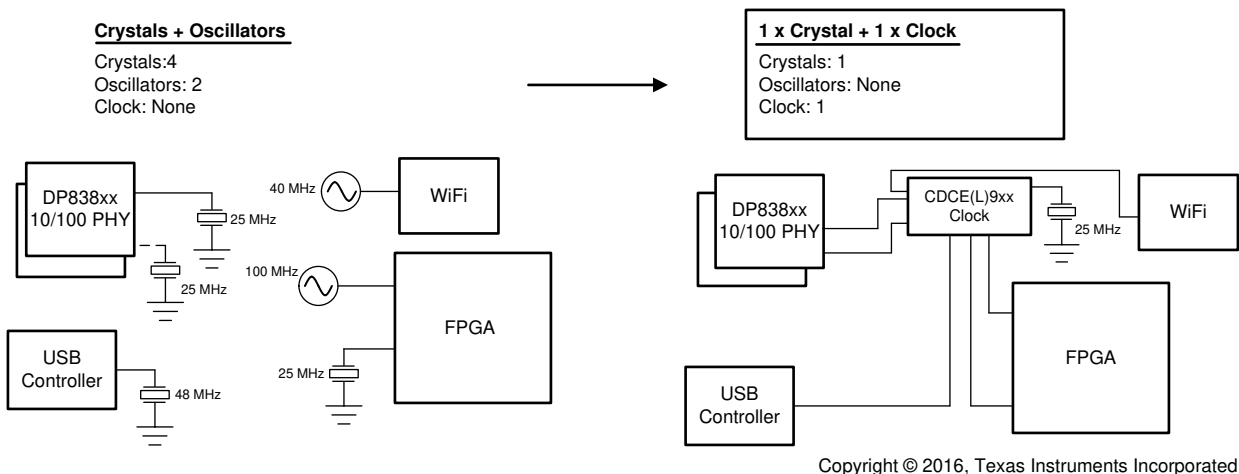
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The CDCE949 device is an easy-to-use high-performance, programmable CMOS clock synthesizer. The device can be used as a crystal buffer, clock synthesizer with separate output supply pin. The CDCE949 features an on-chip loop filter and Spread-spectrum modulation. Programming can be done through SPI, pin-mode, or using on-chip EEPROM. This section shows some examples of using CDCE949 in various applications.

### 8.2 Typical Application

Figure 8-1 shows the use of the CDCE949 devices for replacement of crystals and crystal oscillators on a Gigabit Ethernet Switch application.

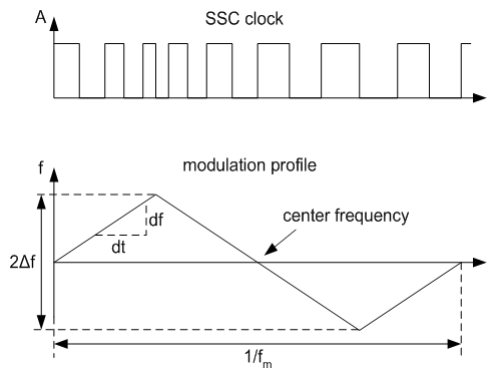


**Figure 8-1. Crystal and Oscillator Replacement Example**

#### 8.2.1 Design Requirements

CDCE949 supports spread spectrum clocking (SSC) with multiple control parameters:

- Modulation amount (%)
- Modulation frequency (>20 kHz)
- Modulation shape (triangular)
- Center spread / down spread ( $\pm$  or  $-$ )

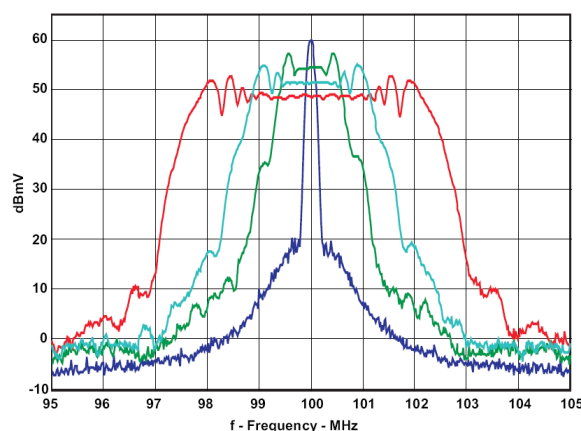


**Figure 8-2. Modulation Frequency ( $f_m$ ) and Modulation Amount**

## 8.2.2 Detailed Design Procedure

### 8.2.2.1 Spread Spectrum Clock (SSC)

Spread spectrum modulation is a method to spread emitted energy over a larger bandwidth. In clocking, spread spectrum can reduce Electromagnetic Interference (EMI) by reducing the level of emission from clock distribution network.



CDCS502 with a 25-MHz Crystal, FS = 1, Fout = 100 MHz, and 0%, ±0.5, ±1%, and ±2% SSC

**Figure 8-3. Comparison Between Typical Clock Power Spectrum and Spread-Spectrum Clock**

### 8.2.2.2 PLL Frequency Planning

At a given input frequency ( $f_{IN}$ ), use [Equation 1](#) to calculate the output frequency ( $f_{OUT}$ ) of the CDCEx949.

$$f_{OUT} = \frac{f_{IN}}{Pdiv} \times \frac{N}{M} \quad (1)$$

where

- M (1 to 511) and N (1 to 4095) are the multiplier/divide values of the PLL
- Pdiv (1 to 127) is the output divider

Use [Equation 2](#) to calculate the target VCO frequency ( $f_{VCO}$ ) of each PLL.

$$f_{VCO} = f_{IN} \times \frac{N}{M} \quad (2)$$

The PLL internally operates as fractional divider and requires the following multiplier/divider settings:

- N
- $P = 4 - \text{int}(\log_2 N/M)$ ; if  $P < 0$  then  $P = 0$
- $Q = \text{int}(N'/M)$
- $R = N' - M \times Q$

where

$$N' = N \times 2^P$$

$$N \geq M;$$

$$80 \text{ MHz} \leq f_{VCO} \leq 230 \text{ MHz}$$

$$16 \leq Q \leq 63$$

$$0 \leq P \leq 4$$

$$0 \leq R \leq 51$$

**Example:**

for  $f_{IN} = 27 \text{ MHz}$ ;  $M = 1$ ;  $N = 4$ ;  $P_{div} = 2$

- $f_{OUT} = 54 \text{ MHz}$
- $f_{VCO} = 108 \text{ MHz}$
- $P = 4 - \text{int}(\log_2 4) = 4 - 2 = 2$
- $N' = 4 \times 2^2 = 16$
- $Q = \text{int}(16) = 16$
- $R = 16 - 16 = 0$

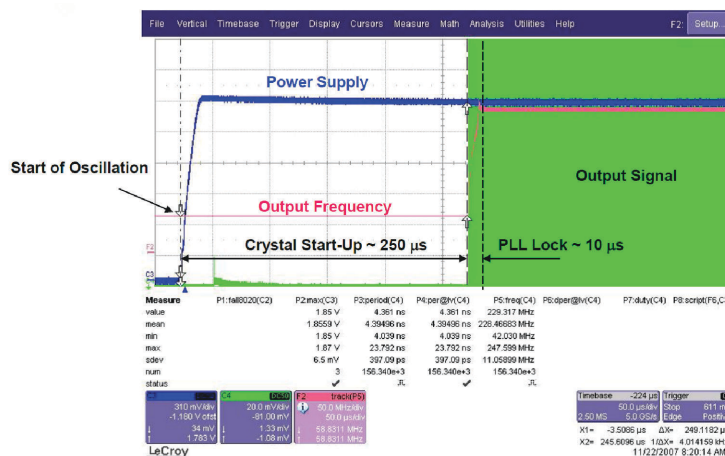
for  $f_{IN} = 27 \text{ MHz}$ ;  $M = 2$ ;  $N = 11$ ;  $P_{div} = 2$

- $f_{OUT} = 74.25 \text{ MHz}$
- $f_{VCO} = 148.50 \text{ MHz}$
- $P = 4 - \text{int}(\log_2 5.5) = 4 - 2 = 2$
- $N' = 11 \times 2^2 = 44$
- $Q = \text{int}(22) = 22$
- $R = 44 - 44 = 0$

The values for P, Q, R, and N' are automatically calculated when using TI Pro-Clock™ software.

### 8.2.2.3 Crystal Oscillator Start-Up

When the CDCE949 is used as a crystal buffer, crystal oscillator start-up dominates the start-up time compared to the internal PLL lock time. The following diagram shows the oscillator start-up sequence for a 27-MHz crystal input with an 8-pF load. The start-up time for the crystal is in the order of approximately 250  $\mu\text{s}$  compared to approximately 10  $\mu\text{s}$  of lock time. In general, lock time is an order of magnitude less compared to the crystal start-up time.



**Figure 8-4. Crystal Oscillator Start-Up vs PLL Lock Time**

### 8.2.2.4 Frequency Adjustment With Crystal Oscillator Pulling

The frequency for the CDCE949 is adjusted for media and other applications with the VCXO control input  $V_{Ctrl}$ . If a PWM modulated signal is used as a control signal for the VCXO, an external filter is needed.

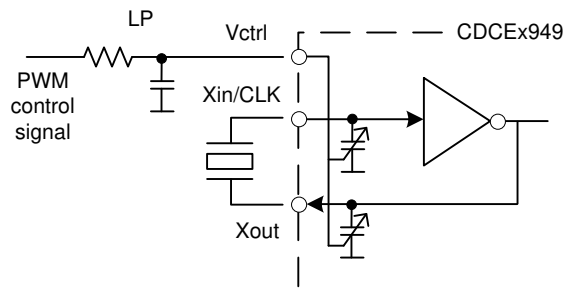


Figure 8-5. Frequency Adjustment Using PWM Input to the VCXO Control

### 8.2.2.5 Unused Inputs and Outputs

If VCXO pulling functionality is not required, leave  $V_{Ctrl}$  floating. Set all other unused inputs to GND. Leave unused outputs floating.

If one output block is not used, TI recommends disabling the that output block. However, TI always recommends providing the supply for the second output block even if the second output block is disabled.

### 8.2.2.6 Switching Between XO and VCXO Mode

When the CDCE949 is in crystal oscillator or in VCXO configuration, the internal capacitors require different internal capacitance. The following steps are recommended to switch to VCXO mode when the configuration for the on-chip capacitor is still set for XO mode. To center the output frequency to 0 ppm:

1. While in XO mode, put  $V_{Ctrl} = V_{dd}/2$
2. Switch from XO mode to VCXO mode
3. Program the internal capacitors to obtain 0 ppm at the output.

### 8.2.3 Application Curves

Figure 8-6, Figure 8-7, Figure 8-8, and Figure 8-9 show CDCE949 measurements with the SSC feature enabled. Device configuration: 27-MHz input, 27-MHz output.

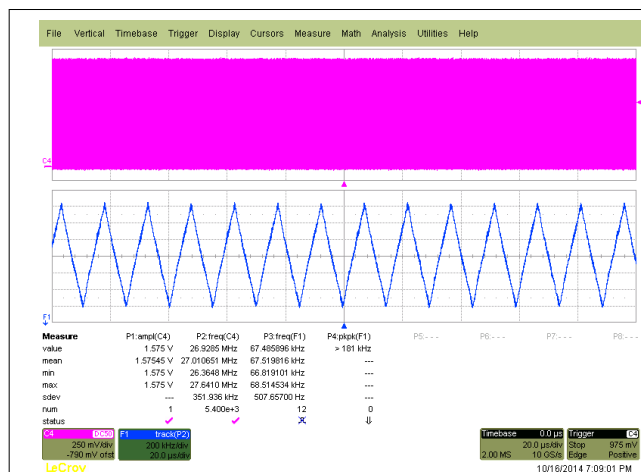


Figure 8-6.  $f_{OUT} = 27$  MHz, VCO Frequency < 125 MHz, SSC (2% Center)

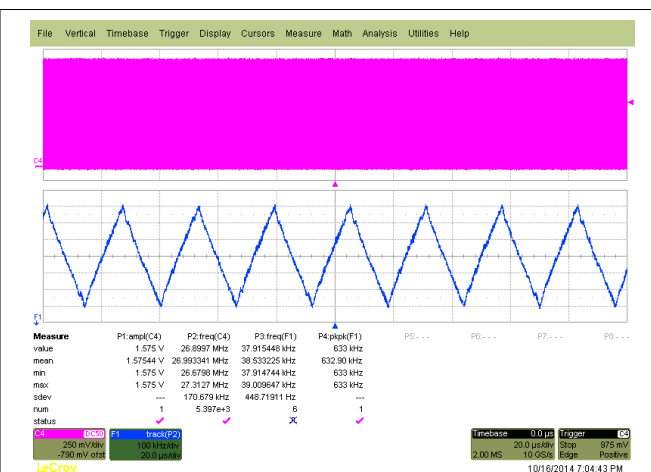
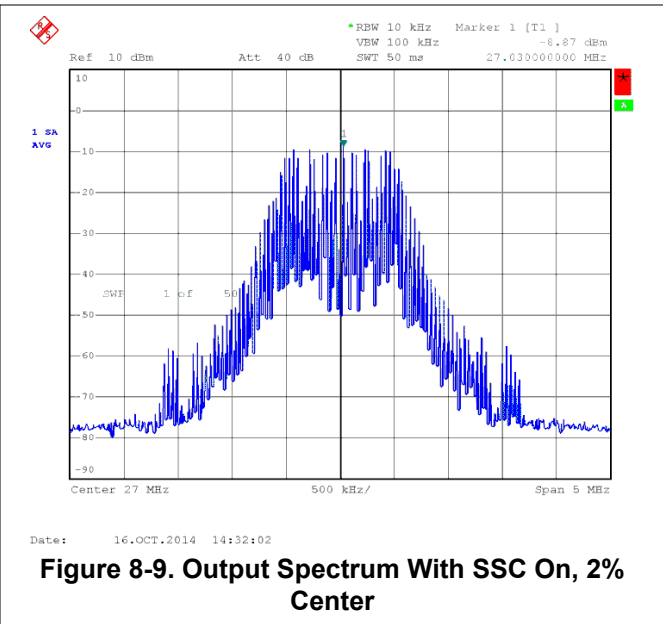
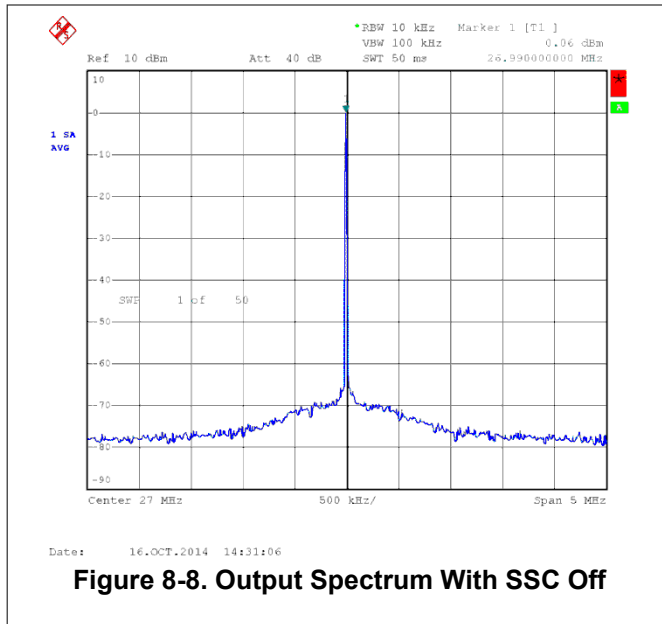


Figure 8-7.  $f_{OUT} = 27$  MHz, VCO Frequency > 175 MHz, SSC (1%, Center)



## 8.3 Power Supply Recommendations

There is no restriction on the power-up sequence. In case the  $V_{DDOUT}$  is applied first, TI recommends grounding the  $V_{DD}$ . In case the  $V_{DDOUT}$  is powered while  $V_{DD}$  is floating, there is a risk of high current flowing on the  $V_{DDOUT}$ .

The device has a power-up control that is connected to the 1.8-V supply. This keeps the whole device disabled until the 1.8-V supply reaches a sufficient voltage level. Then the device switches on all internal components, including the outputs. If there is a 3.3-V  $V_{DDOUT}$  available before the 1.8-V, the outputs stay disabled until the 1.8-V supply reaches a certain level.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When the CDCEx949 is used as a crystal buffer, any parasitics across the crystal affects the pulling range of the VCXO. Therefore, take care placing the crystal units on the board. Crystals must be placed as close to the device as possible so that the routing lines from the crystal terminals to XIN and XOUT have the same length.

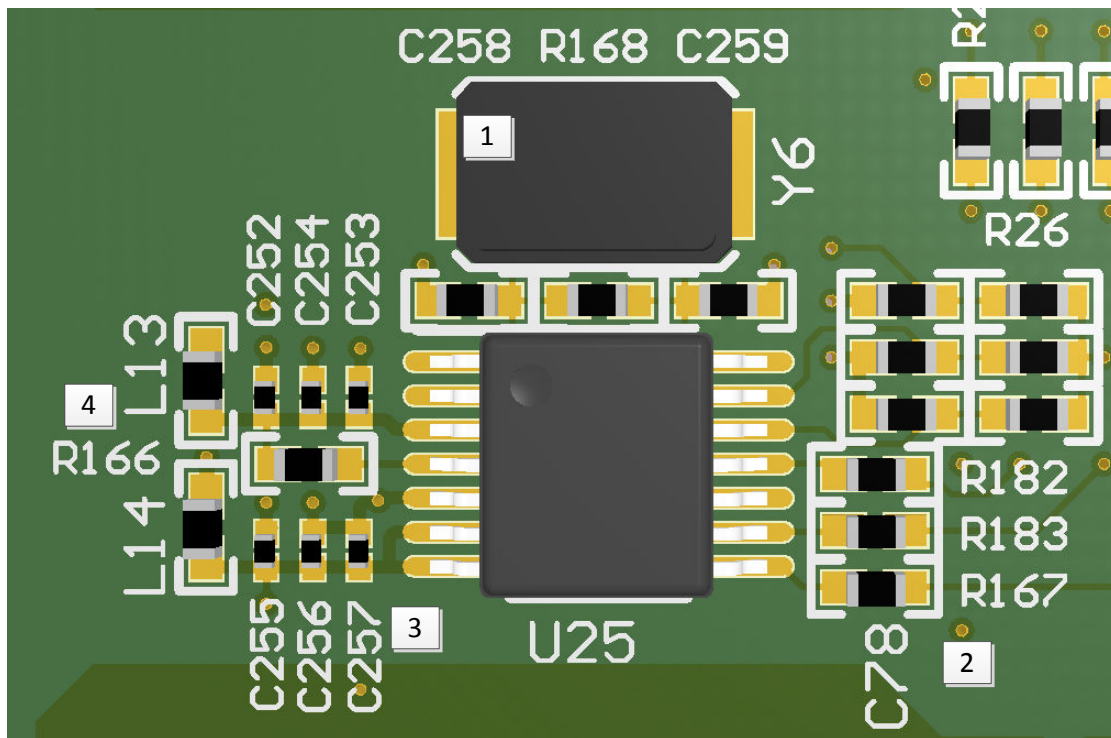
If possible, cut out both ground plane and power plane under the area where the crystal and the routing to the device are placed. In this area, always avoid routing any other signal line, as it can be a source of noise coupling.

Additional discrete capacitors can be required to meet the load capacitance specification of certain crystal. For example, a 10.7-pF load capacitor is not fully programmable on the chip, because the internal capacitor can range from 0 pF to 20 pF with steps of 1 pF. The 0.7-pF capacitor therefore can be discretely added on top of an internal 10-pF capacitor.

To minimize the inductive influence of the trace, TI recommends placing this small capacitor as close to the device as possible and symmetrically with respect to XIN and XOUT.

Figure 8-10 shows a conceptual layout detailing recommended placement of power supply bypass capacitors on the basis of CDCEx949. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

### 8.4.2 Layout Example



1 Place crystal with associated load caps as close to the chip

2 Place series termination resistors at Clock outputs to improve signal integrity

3 Place bypass caps close to the device pins, ensure wide freq. range

4 Use ferrite beads to isolate the device supply pins from board noise sources

**Figure 8-10. Annotated Layout**

## 9 Register Maps

### 9.1 SDA/SCL Configuration Registers

The clock input, control pins, PLLs, and output stages are user configurable. The following tables and explanations describe the programmable functions of the CDCE949. All settings can be manually written to the device through the SDA/SCL bus, or are easily programmable by using the TI Pro Clock software. TI Pro Clock software allows the user to quickly make all settings and automatically calculates the values for optimized performance at lowest jitter.

**Table 9-1. SDA/SCL Registers**

| ADDRESS OFFSET | REGISTER DESCRIPTION           | TABLE                     |
|----------------|--------------------------------|---------------------------|
| 00h            | Generic configuration register | <a href="#">Table 9-3</a> |
| 10h            | PLL1 configuration register    | <a href="#">Table 9-4</a> |
| 20h            | PLL2 configuration register    | <a href="#">Table 9-5</a> |
| 30h            | PLL3 configuration register    | <a href="#">Table 9-6</a> |
| 40h            | PLL4 configuration register    | <a href="#">Table 9-7</a> |

The grey-highlighted Bits described in the configuration registers tables on the following pages, belong to the Control Pin Register. The user can predefine up to eight different control settings. These settings can then be selected by the external control pins, S0, S1, and S2 (see [Control Terminal Setting](#)).

**Table 9-2. Configuration Register, External Control Pins**

| EXTERNAL<br>CONTROL<br>PINS    |    |    | Y1               | PLL1 SETTING   |               |                  | PLL2 SETTING   |               |                  | PLL3 SETTING   |               |                  | PLL4 SETTING   |               |                  |
|--------------------------------|----|----|------------------|----------------|---------------|------------------|----------------|---------------|------------------|----------------|---------------|------------------|----------------|---------------|------------------|
|                                |    |    | OUTPUT<br>SELECT | FREQ<br>SELECT | SSC<br>SELECT | OUTPUT<br>SELECT | FREQ<br>SELECT | SSC<br>SELECT | OUTPUT<br>SELECT | FREQ<br>SELECT | SSC<br>SELECT | OUTPUT<br>SELECT | FREQ<br>SELECT | SSC<br>SELECT | OUTPUT<br>SELECT |
| S2                             | S1 | S0 | Y1               | FS1            | SSC1          | Y2Y3             | FS2            | SSC2          | Y4Y5             | FS3            | SSC3          | Y6Y7             | FS4            | SSC4          | Y8Y9             |
| 0                              | 0  | 0  | Y1_0             | FS1_0          | SSC1_0        | Y2Y3_0           | FS2_0          | SSC2_0        | Y4Y5_0           | FS3_0          | SSC3_0        | Y6Y7_0           | FS4_0          | SSC4_0        | Y8Y9_0           |
| 0                              | 0  | 1  | Y1_1             | FS1_1          | SSC1_1        | Y2Y3_1           | FS2_1          | SSC2_1        | Y4Y5_1           | FS3_1          | SSC3_1        | Y6Y7_1           | FS4_1          | SSC4_1        | Y8Y9_1           |
| 0                              | 1  | 0  | Y1_2             | FS1_2          | SSC1_2        | Y2Y3_2           | FS2_2          | SSC2_2        | Y4Y5_2           | FS3_2          | SSC3_2        | Y6Y7_2           | FS4_2          | SSC4_2        | Y8Y9_2           |
| 0                              | 1  | 1  | Y1_3             | FS1_3          | SSC1_3        | Y2Y3_3           | FS2_3          | SSC2_3        | Y4Y5_3           | FS3_3          | SSC3_3        | Y6Y7_3           | FS4_3          | SSC4_3        | Y8Y9_3           |
| 1                              | 0  | 0  | Y1_4             | FS1_4          | SSC1_4        | Y2Y3_4           | FS2_4          | SSC2_4        | Y4Y5_4           | FS3_4          | SSC3_4        | Y6Y7_4           | FS4_4          | SSC4_4        | Y8Y9_4           |
| 1                              | 0  | 1  | Y1_5             | FS1_5          | SSC1_5        | Y2Y3_5           | FS2_5          | SSC2_5        | Y4Y5_5           | FS3_5          | SSC3_5        | Y6Y7_5           | FS4_5          | SSC4_5        | Y8Y9_5           |
| 1                              | 1  | 0  | Y1_6             | FS1_6          | SSC1_6        | Y2Y3_6           | FS2_6          | SSC2_6        | Y4Y5_6           | FS3_6          | SSC3_6        | Y6Y7_6           | FS4_6          | SSC4_6        | Y8Y9_6           |
| 1                              | 1  | 1  | Y1_7             | FS1_7          | SSC1_7        | Y2Y3_7           | FS2_7          | SSC2_7        | Y4Y5_7           | FS3_7          | SSC3_7        | Y6Y7_7           | FS4_7          | SSC4_7        | Y8Y9_7           |
| Addr.<br>Offset <sup>(1)</sup> |    |    | 04h              | 13h            | 10h-12h       | 15h              | 23h            | 20h-22h       | 25h              | 33h            | 30h-32h       | 35h              | 43h            | 40h-42h       | 45h              |

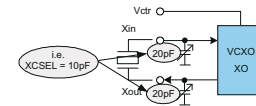
(1) Address Offset refers to the byte address in the Configuration Register on following pages.

**Table 9-3. Generic Configuration Register**

| OFFSET <sup>(1)</sup> | BIT <sup>(2)</sup> | ACRONYM    | DEFAULT <sup>(3)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                             |
|-----------------------|--------------------|------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00h                   | 7                  | E_EL       | xb                     | Device Identification (read only): '1' is CDCE949 (3.3V), '0' is CDCEL949 (1.8V)                                                                                                                                                                                                        |
|                       | 6:4                | RID        | Xb                     | Revision Identification Number (read only)                                                                                                                                                                                                                                              |
|                       | 3:0                | VID        | 1h                     | Vendor Identification Number (read only)                                                                                                                                                                                                                                                |
| 01h                   | 7                  | –          | 0b                     | Reserved - always write 0                                                                                                                                                                                                                                                               |
|                       | 6                  | EEPIP      | 0b                     | EEPROM Programming Status <sup>(4)</sup> : (read only)<br>0 – EEPROM programming is completed<br>1 – EEPROM is in programming mode                                                                                                                                                      |
|                       | 5                  | EELOCK     | 0b                     | Permanently Lock EEPROM Data <sup>(5)</sup> :<br>0 – EEPROM is not locked<br>1 – EEPROM is permanently locked                                                                                                                                                                           |
|                       | 4                  | PWDN       | 0b                     | Device power down (overwrites S0/S1/S2 setting; configuration register settings are unchanged)<br>Note: PWDN cannot be set to 1 in the EEPROM.<br>0 – device active (all PLLs and all outputs are enabled)<br>1 – device power down (all PLLs in power down and all outputs in 3-State) |
|                       | 3:2                | INCLK      | 00b                    | Input clock selection: 00 – X-tal 10 – LVCMOS<br>01 – VCXO 11 – reserved                                                                                                                                                                                                                |
|                       | 1:0                | TARGET_ADR | 00b                    | Programmable Address Bits A0 and A1 of the Target Receiver Address                                                                                                                                                                                                                      |

**Table 9-3. Generic Configuration Register (continued)**

| OFFSET <sup>(1)</sup> | BIT <sup>(2)</sup> | ACRONYM     | DEFAULT <sup>(3)</sup> | DESCRIPTION                                                                                                                                                                     |
|-----------------------|--------------------|-------------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 02h                   | 7                  | M1          | 1b                     | Clock source selection for output Y1:<br>0 – input clock<br>1 – PLL1 clock                                                                                                      |
|                       | 6                  | SPICON      | 0b                     | Operation mode selection for pin 22/23 <sup>(6)</sup><br>0 – serial programming interface SDA (pin 23) and SCL (pin 22)<br>1 – control pins S1 (pin 23) and S2 (pin 22)         |
|                       | 5:4                | Y1_ST1      | 11b                    | Y1-State0/1 Definition (applies to Y1_ST1 and Y1_ST0)                                                                                                                           |
|                       | 3:2                | Y1_ST0      | 01b                    | 00 – device power down (all PLLs in power down and all outputs in 3-state)<br>01 – Y1 disabled to 3-state<br>10 – Y1 disabled to low<br>11 – Y1 enabled (normal operation)      |
|                       | 1:0                | Pdiv1 [9:8] | 001h                   | 10-Bit Y1-Output-Divider<br>Pdiv1:<br>0 – divider reset and stand-by<br>1-to-1023 – divider value                                                                               |
| 03h                   | 7:0                | Pdiv1 [7:0] |                        |                                                                                                                                                                                 |
| 04h                   | 7                  | Y1_7        | 0b                     | Y1_x State Selection <sup>(7)</sup><br><br>0 – State0 (predefined by Y1-State0 Definition [Y1_ST0])<br>1 – State1 (predefined by Y1-State1 Definition [Y1_ST1])                 |
|                       | 6                  | Y1_6        | 0b                     |                                                                                                                                                                                 |
|                       | 5                  | Y1_5        | 0b                     |                                                                                                                                                                                 |
|                       | 4                  | Y1_4        | 0b                     |                                                                                                                                                                                 |
|                       | 3                  | Y1_3        | 0b                     |                                                                                                                                                                                 |
|                       | 2                  | Y1_2        | 0b                     |                                                                                                                                                                                 |
|                       | 1                  | Y1_1        | 1b                     |                                                                                                                                                                                 |
|                       | 0                  | Y1_0        | 0b                     |                                                                                                                                                                                 |
| 05h                   | 7:3                | XCSEL       | 0Ah                    | Crystal load capacitor selection <sup>(8)</sup> :<br>00h → 0 pF<br>01h → 1 pF<br>02h → 2 pF<br>14h-to-1Fh → 20 pF                                                               |
|                       | 2:0                | —           | 0b                     | Reserved - do not write others than 0                                                                                                                                           |
| 06h                   | 7:1                | BCOUNT      | 50h                    | 7-Bit Byte Count (Defines the number of Bytes which is sent from this device at the next Block Read transfer; all bytes must be read out to correctly finish the read cycle.)   |
|                       | 0                  | EEWRITE     | 0b                     | Initiate EEPROM Write Cycle <sup>(4)</sup> <sup>(9)</sup><br>0 – no EEPROM write cycle<br>1 – start EEPROM write cycle (internal configuration register is saved to the EEPROM) |
| 07h-0Fh               | —                  | —           | 0h                     | Reserved – do not write others than 0                                                                                                                                           |



- (1) Writing data beyond 50h may adversely affect device function.
- (2) All data is transferred MSB-first.
- (3) Unless custom setting is used.
- (4) During EEPROM programming, no data is allowed to be sent to the device through the SDA/SCL bus until the programming sequence is completed. Data, however, can be read during the programming sequence (Byte Read or Block Read).
- (5) If this bit is set high in the EEPROM, the actual data in the EEPROM is permanently locked, and no further programming is possible. Data, however can still be written through the SDA/SCL bus to the internal register to change device function on the fly. But new data can no longer be saved to the EEPROM. EELOCK is effective only if written into the EEPROM.
- (6) Selection of *control-pins* is effective only if written into the EEPROM. Once written into the EEPROM, the serial programming pins are no longer available. However, if  $V_{DDOUT}$  is forced to GND, the two control-pins, S1 and S2, temporally act as serial programming pins (SDA/SCL), and the two target receiver address bits are reset to A0 = 0 and A1 = 0.
- (7) These are the bits of the Control Pin Register. The user can predefine up to eight different control settings. These settings can then be selected by the external control pins, S0, S1, and S2.
- (8) The internal load capacitor ( $C_1$ ,  $C_2$ ) must be used to achieve the best clock performance. External capacitors must be used only to do a fine adjustment of  $C_L$  by few pF. The value of  $C_L$  can be programmed with a resolution of 1 pF for a total crystal load range of 0 pF to 20 pF. For  $C_L > 20$  pF use additional external capacitors. Also, the device input capacitance must be considered; this adds 1.5 pF (6 pF, 2 pF) to the selected  $C_L$ . For more information about VCXO configuration and crystal recommendations, see [VCXO Application Guideline for CDCE\(L\)9xx Family](#) (SCAA085).
- (9) NOTE: The EEPROM WRITE bit must be sent last to make sure the contents of all internal registers are written into the EEPROM. The EEWRITE cycle is initiated by the rising edge of the EEWRITE-Bit. A static level high does not trigger an EEPROM WRITE cycle. The EEWRITE-Bit must be reset low after the programming is completed. The programming status can be monitored by readout EEPIF. If EELOCK is set high, no EEPROM programming is possible.

**Table 9-4. PLL1 Configuration Register**

| OFFSET <sup>(1)</sup> | BIT <sup>(2)</sup> | ACRONYM      | DEFAULT <sup>(3)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                      |
|-----------------------|--------------------|--------------|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10h                   | 7:5                | SSC1_7 [2:0] | 000b                   | <b>SSC1: PLL1 SSC Selection (Modulation Amount)<sup>(4)</sup></b><br><br><div> <b>Down</b><br/> 000 (off)<br/> 001 – 0.25%<br/> 010 – 0.5%<br/> 011 – 0.75%<br/> 100 – 1.0%<br/> 101 – 1.25%<br/> 110 – 1.5%<br/> 111 – 2.0% </div> <div> <b>Center</b><br/> 000 (off)<br/> 001 ± 0.25%<br/> 010 ± 0.5%<br/> 011 ± 0.75%<br/> 100 ± 1.0%<br/> 101 ± 1.25%<br/> 110 ± 1.5%<br/> 111 ± 2.0% </div> |
|                       | 4:2                | SSC1_6 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 1:0                | SSC1_5 [2:1] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                                  |
| 11h                   | 7                  | SSC1_5 [0]   | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 6:4                | SSC1_4 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 3:1                | SSC1_3 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 0                  | SSC1_2 [2]   | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                                  |
| 12h                   | 7:6                | SSC1_2 [1:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 5:3                | SSC1_1 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 2:0                | SSC1_0 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                                  |
| 13h                   | 7                  | FS1_7        | 0b                     | <b>FS1_x: PLL1 Frequency Selection<sup>(4)</sup></b><br><br>0 – $f_{VCO1\_0}$ (predefined by PLL1_0 – Multiplier/Divider value)<br>1 – $f_{VCO1\_1}$ (predefined by PLL1_1 – Multiplier/Divider value)                                                                                                                                                                                           |
|                       | 6                  | FS1_6        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 5                  | FS1_5        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 4                  | FS1_4        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 3                  | FS1_3        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 2                  | FS1_2        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 1                  | FS1_1        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 0                  | FS1_0        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
| 14h                   | 7                  | MUX1         | 1b                     | PLL1 Multiplexer: 0 – PLL1<br>1 – PLL1 Bypass (PLL1 is in power down)                                                                                                                                                                                                                                                                                                                            |
|                       | 6                  | M2           | 1b                     | Output Y2 Multiplexer: 0 – Pdiv1<br>1 – Pdiv2                                                                                                                                                                                                                                                                                                                                                    |
|                       | 5:4                | M3           | 10b                    | Output Y3 Multiplexer: 00 – Pdiv1-Divider<br>01 – Pdiv2-Divider<br>10 – Pdiv3-Divider<br>11 – reserved                                                                                                                                                                                                                                                                                           |
|                       | 3:2                | Y2Y3_ST1     | 11b                    | Y2, Y3-State0/1definition: 00 – Y2/Y3 disabled to 3-State (PLL1 is in power down)<br>01 – Y2/Y3 disabled to 3-State (PLL1 on)<br>10 – Y2/Y3 disabled to low (PLL1 on)<br>11 – Y2/Y3 enabled (normal operation, PLL1 on)                                                                                                                                                                          |
|                       | 1:0                | Y2Y3_ST0     | 01b                    |                                                                                                                                                                                                                                                                                                                                                                                                  |
| 15h                   | 7                  | Y2Y3_7       | 0b                     | <b>Y2Y3_x Output State Selection<sup>(4)</sup></b><br><br>0 – state0 (predefined by Y2Y3_ST0)<br>1 – state1 (predefined by Y2Y3_ST1)                                                                                                                                                                                                                                                             |
|                       | 6                  | Y2Y3_6       | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 5                  | Y2Y3_5       | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 4                  | Y2Y3_4       | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 3                  | Y2Y3_3       | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 2                  | Y2Y3_2       | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 1                  | Y2Y3_1       | 1b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 0                  | Y2Y3_0       | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                                  |
| 16h                   | 7                  | SSC1DC       | 0b                     | PLL1 SSC down/center selection: 0 – down<br>1 – center                                                                                                                                                                                                                                                                                                                                           |
|                       | 6:0                | Pdiv2        | 01h                    | 7-Bit Y2-Output-Divider Pdiv2: 0 – reset and stand-by<br>1-to-127 – divider value                                                                                                                                                                                                                                                                                                                |
| 17h                   | 7                  | —            | 0b                     | Reserved – do not write others than 0                                                                                                                                                                                                                                                                                                                                                            |
|                       | 6:0                | Pdiv3        | 01h                    | 7-Bit Y3-Output-Divider Pdiv3: 0 – reset and stand-by<br>1-to-127 – divider value                                                                                                                                                                                                                                                                                                                |

**Table 9-4. PLL1 Configuration Register (continued)**

| OFFSET <sup>(1)</sup> | BIT <sup>(2)</sup> | ACRONYM        | DEFAULT <sup>(3)</sup> | DESCRIPTION                                                                                                                                                                                                      |
|-----------------------|--------------------|----------------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 18h                   | 7:0                | PLL1_0N [11:4] | 004h                   | PLL1_0 <sup>(5)</sup> : 30-Bit Multiplier/Divider value for frequency f <sub>VCO1_0</sub><br>(for more information, see <a href="#">PLL Frequency Planning</a> )                                                 |
| 19h                   | 7:4                | PLL1_0N [3:0]  | 000h                   |                                                                                                                                                                                                                  |
|                       | 3:0                | PLL1_0R [8:5]  |                        |                                                                                                                                                                                                                  |
| 1Ah                   | 7:3                | PLL1_0R[4:0]   | 10h                    |                                                                                                                                                                                                                  |
|                       | 2:0                | PLL1_0Q [5:3]  |                        |                                                                                                                                                                                                                  |
| 1Bh                   | 7:5                | PLL1_0Q [2:0]  | 010b                   |                                                                                                                                                                                                                  |
|                       | 4:2                | PLL1_0P [2:0]  |                        |                                                                                                                                                                                                                  |
|                       | 1:0                | VCO1_0_RANGE   | 00b                    | f <sub>VCO1_0</sub> range selection:<br>00 – f <sub>VCO1_0</sub> < 125 MHz<br>01 – 125 MHz ≤ f <sub>VCO1_0</sub> < 150 MHz<br>10 – 150 MHz ≤ f <sub>VCO1_0</sub> < 175 MHz<br>11 – f <sub>VCO1_0</sub> ≥ 175 MHz |
| 1Ch                   | 7:0                | PLL1_1N [11:4] | 004h                   | PLL1_1 <sup>(5)</sup> : 30-Bit Multiplier/Divider value for frequency f <sub>VCO1_1</sub><br>(for more information, see <a href="#">PLL Frequency Planning</a> ).                                                |
| 1Dh                   | 7:4                | PLL1_1N [3:0]  | 000h                   |                                                                                                                                                                                                                  |
|                       | 3:0                | PLL1_1R [8:5]  |                        |                                                                                                                                                                                                                  |
| 1Eh                   | 7:3                | PLL1_1R[4:0]   | 10h                    |                                                                                                                                                                                                                  |
|                       | 2:0                | PLL1_1Q [5:3]  |                        |                                                                                                                                                                                                                  |
| 1Fh                   | 7:5                | PLL1_1Q [2:0]  | 010b                   |                                                                                                                                                                                                                  |
|                       | 4:2                | PLL1_1P [2:0]  |                        |                                                                                                                                                                                                                  |
|                       | 1:0                | VCO1_1_RANGE   | 00b                    | f <sub>VCO1_1</sub> range selection:<br>00 – f <sub>VCO1_1</sub> < 125 MHz<br>01 – 125 MHz ≤ f <sub>VCO1_1</sub> < 150 MHz<br>10 – 150 MHz ≤ f <sub>VCO1_1</sub> < 175 MHz<br>11 – f <sub>VCO1_1</sub> ≥ 175 MHz |

(1) Writing data beyond 50h may adversely affect device function.

(2) All data is transferred MSB-first.

(3) Unless a custom setting is used

(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

(5) PLL settings limits:  $16 \leq p \leq 63$ ,  $0 \leq p \leq 7$ ,  $0 \leq r \leq 511$ ,  $0 < N < 4096$ **Table 9-5. PLL2 Configuration Register**

| OFFSET <sup>(1)</sup> | BIT <sup>(2)</sup> | ACRONYM      | DEFAULT <sup>(3)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                      |
|-----------------------|--------------------|--------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20h                   | 7:5                | SSC2_7 [2:0] | 000b                   | SSC2: PLL2 SSC Selection (Modulation Amount) <sup>(4)</sup><br><br><div><div><b>Down</b><br/>000 (off)<br/>001 – 0.25%<br/>010 – 0.5%<br/>011 – 0.75%<br/>100 – 1.0%<br/>101 – 1.25%<br/>110 – 1.5%<br/>111 – 2.0%</div><div><b>Center</b><br/>000 (off)<br/>001 ± 0.25%<br/>010 ± 0.5%<br/>011 ± 0.75%<br/>100 ± 1.0%<br/>101 ± 1.25%<br/>110 ± 1.5%<br/>111 ± 2.0%</div></div> |
|                       | 4:2                | SSC2_6 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 1:0                | SSC2_5 [2:1] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                  |
| 21h                   | 7                  | SSC2_5 [0]   |                        |                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 6:4                | SSC2_4 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 3:1                | SSC2_3 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 0                  | SSC2_2 [2]   | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                  |
| 22h                   | 7:6                | SSC2_2 [1:0] |                        |                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 5:3                | SSC2_1 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 2:0                | SSC2_0 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                  |
| 23h                   | 7                  | FS2_7        | 0b                     | FS2_x: PLL2 Frequency Selection <sup>(4)</sup><br><br><div>0 – f<sub>VCO2_0</sub> (predefined by PLL2_0 – Multiplier/Divider value)<br/>1 – f<sub>VCO2_1</sub> (predefined by PLL2_1 – Multiplier/Divider value)</div>                                                                                                                                                           |
|                       | 6                  | FS2_6        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 5                  | FS2_5        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 4                  | FS2_4        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 3                  | FS2_3        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 2                  | FS2_2        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 1                  | FS2_1        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                  |
|                       | 0                  | FS2_0        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 9-5. PLL2 Configuration Register (continued)**

| OFFSET <sup>(1)</sup> | BIT <sup>(2)</sup> | ACRONYM        | DEFAULT <sup>(3)</sup> | DESCRIPTION                                                                                                                                                                                                          |                                                                                                                                                                                            |
|-----------------------|--------------------|----------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24h                   | 7                  | MUX2           | 1b                     | PLL2 Multiplexer:                                                                                                                                                                                                    | 0 – PLL2<br>1 – PLL2 Bypass (PLL2 is in power down)                                                                                                                                        |
|                       | 6                  | M4             | 1b                     | Output Y4 Multiplexer:                                                                                                                                                                                               | 0 – Pdiv2<br>1 – Pdiv4                                                                                                                                                                     |
|                       | 5:4                | M5             | 10b                    | Output Y5 Multiplexer:                                                                                                                                                                                               | 00 – Pdiv2-Divider<br>01 – Pdiv4-Divider<br>10 – Pdiv5-Divider<br>11 – reserved                                                                                                            |
|                       | 3:2                | Y4Y5_ST1       | 11b                    | Y4, Y5-<br>State0/1definition:                                                                                                                                                                                       | 00 – Y4/Y5 disabled to 3-State (PLL2 is in power down)<br>01 – Y4/Y5 disabled to 3-State (PLL2 on)<br>10–Y4/Y5 disabled to low (PLL2 on)<br>11 – Y4/Y5 enabled (normal operation, PLL2 on) |
|                       | 1:0                | Y4Y5_ST0       | 01b                    |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
| 25h                   | 7                  | Y4Y5_7         | 0b                     | Y4Y5_x Output State Selection <sup>(4)</sup><br><br>0 – state0 (predefined by Y4Y5_ST0)<br>1 – state1 (predefined by Y4Y5_ST1)                                                                                       |                                                                                                                                                                                            |
|                       | 6                  | Y4Y5_6         | 0b                     |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
|                       | 5                  | Y4Y5_5         | 0b                     |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
|                       | 4                  | Y4Y5_4         | 0b                     |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
|                       | 3                  | Y4Y5_3         | 0b                     |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
|                       | 2                  | Y4Y5_2         | 0b                     |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
|                       | 1                  | Y4Y5_1         | 1b                     |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
|                       | 0                  | Y4Y5_0         | 0b                     |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
| 26h                   | 7                  | SSC2DC         | 0b                     | PLL2 SSC down/center selection:                                                                                                                                                                                      | 0 – down<br>1 – center                                                                                                                                                                     |
|                       | 6:0                | Pdiv4          | 01h                    | 7-Bit Y4-Output-Divider Pdiv4:                                                                                                                                                                                       | 0 – reset and stand-by<br>1-to-127 – divider value                                                                                                                                         |
| 27h                   | 7                  | —              | 0b                     | Reserved – do not write others than 0                                                                                                                                                                                |                                                                                                                                                                                            |
|                       | 6:0                | Pdiv5          | 01h                    | 7-Bit Y5-Output-Divider Pdiv5:                                                                                                                                                                                       | 0 – reset and stand-by<br>1-to-127 – divider value                                                                                                                                         |
| 28h                   | 7:0                | PLL2_0N [11:4] | 004h                   | PLL2_0 <sup>(5)</sup> : 30-Bit Multiplier/Divider value for frequency f <sub>VCO2_0</sub><br>(for more information, see <a href="#">PLL Frequency Planning</a> ).                                                    |                                                                                                                                                                                            |
| 29h                   | 7:4                | PLL2_0N [3:0]  |                        |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
|                       | 3:0                | PLL2_0R [8:5]  | 000h                   |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
| 2Ah                   | 7:3                | PLL2_0R[4:0]   | 10h                    |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
|                       | 2:0                | PLL2_0Q [5:3]  |                        |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
| 2Bh                   | 7:5                | PLL2_0Q [2:0]  | 010b                   | f <sub>VCO2_0</sub> range selection:<br><br>00 – f <sub>VCO2_0</sub> < 125 MHz<br>01 – 125 MHz ≤ f <sub>VCO2_0</sub> < 150 MHz<br>10 – 150 MHz ≤ f <sub>VCO2_0</sub> < 175 MHz<br>11 – f <sub>VCO2_0</sub> ≥ 175 MHz |                                                                                                                                                                                            |
|                       | 4:2                | PLL2_0P [2:0]  |                        |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
|                       | 1:0                | VCO2_0_RANGE   | 00b                    |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
| 2Ch                   | 7:0                | PLL2_1N [11:4] | 004h                   | PLL2_1 <sup>(5)</sup> : 30-Bit Multiplier/Divider value for frequency f <sub>VCO1_1</sub><br>(for more information, see <a href="#">PLL Frequency Planning</a> ).                                                    |                                                                                                                                                                                            |
| 2Dh                   | 7:4                | PLL2_1N [3:0]  |                        |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
|                       | 3:0                | PLL2_1R [8:5]  | 000h                   |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
| 2Eh                   | 7:3                | PLL2_1R[4:0]   | 10h                    |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
|                       | 2:0                | PLL2_1Q [5:3]  |                        |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
| 2Fh                   | 7:5                | PLL2_1Q [2:0]  | 010b                   | f <sub>VCO2_1</sub> range selection:<br><br>00 – f <sub>VCO2_1</sub> < 125 MHz<br>01 – 125 MHz ≤ f <sub>VCO2_1</sub> < 150 MHz<br>10 – 150 MHz ≤ f <sub>VCO2_1</sub> < 175 MHz<br>11 – f <sub>VCO2_1</sub> ≥ 175 MHz |                                                                                                                                                                                            |
|                       | 4:2                | PLL2_1P [2:0]  |                        |                                                                                                                                                                                                                      |                                                                                                                                                                                            |
|                       | 1:0                | VCO2_1_RANGE   | 00b                    |                                                                                                                                                                                                                      |                                                                                                                                                                                            |

- (1) Writing data beyond 50h may adversely affect device function.  
(2) All data is transferred MSB-first.  
(3) Unless a custom setting is used  
(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.  
(5) PLL settings limits:  $16 \leq q \leq 63$ ,  $0 \leq p \leq 7$ ,  $0 \leq r \leq 511$ ,  $0 < N < 4096$

**Table 9-6. PLL3 Configuration Register**

| OFFSET <sup>(1)</sup> | BIT <sup>(2)</sup> | ACRONYM      | DEFAULT <sup>(3)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                             |
|-----------------------|--------------------|--------------|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30h                   | 7:5                | SSC3_7 [2:0] | 000b                   | SSC3: PLL3 SSC Selection (Modulation Amount) <sup>(4)</sup><br><br><div><div>Down</div><div>000 (off)<br/>001 – 0.25%<br/>010 – 0.5%<br/>011 – 0.75%<br/>100 – 1.0%<br/>101 – 1.25%<br/>110 – 1.5%<br/>111 – 2.0%</div><div>Center</div><div>000 (off)<br/>001 ± 0.25%<br/>010 ± 0.5%<br/>011 ± 0.75%<br/>100 ± 1.0%<br/>101 ± 1.25%<br/>110 ± 1.5%<br/>111 ± 2.0%</div></div> |                                                                                                                                                                                             |
|                       | 4:2                | SSC3_6 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 1:0                | SSC3_5 [2:1] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
| 31h                   | 7                  | SSC3_5 [0]   |                        |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 6:4                | SSC3_4 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 3:1                | SSC3_3 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 0                  | SSC3_2 [2]   | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
| 32h                   | 7:6                | SSC3_2 [1:0] |                        |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 5:3                | SSC3_1 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 2:0                | SSC3_0 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
| 33h                   | 7                  | FS3_7        | 0b                     | FS3_x: PLL3 Frequency Selection <sup>(4)</sup><br><br>0 – f <sub>VCO3_0</sub> (predefined by PLL3_0 – Multiplier/Divider value)<br>1 – f <sub>VCO3_1</sub> (predefined by PLL3_1 – Multiplier/Divider value)                                                                                                                                                                   |                                                                                                                                                                                             |
|                       | 6                  | FS3_6        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 5                  | FS3_5        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 4                  | FS3_4        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 3                  | FS3_3        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 2                  | FS3_2        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 1                  | FS3_1        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 0                  | FS3_0        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
| 34h                   | 7                  | MUX3         | 1b                     | PLL3 Multiplexer:                                                                                                                                                                                                                                                                                                                                                              | 0 – PLL3<br>1 – PLL3 Bypass (PLL3 is in power down)                                                                                                                                         |
|                       | 6                  | M6           | 1b                     | Output Y6 Multiplexer:                                                                                                                                                                                                                                                                                                                                                         | 0 – Pdiv4<br>1 – Pdiv6                                                                                                                                                                      |
|                       | 5:4                | M7           | 10b                    | Output Y7 Multiplexer:                                                                                                                                                                                                                                                                                                                                                         | 00 – Pdiv4-Divider<br>01 – Pdiv6-Divider<br>10 – Pdiv7-Divider<br>11 – reserved                                                                                                             |
|                       | 3:2                | Y6Y7_ST1     | 11b                    | Y6, Y7-<br>State0/1definition:                                                                                                                                                                                                                                                                                                                                                 | 00 – Y6/Y7 disabled to 3-State (PLL3 is in power down)<br>01 – Y6/Y7 disabled to 3-State (PLL3 on)<br>10 –Y6/Y7 disabled to low (PLL3 on)<br>11 – Y6/Y7 enabled (normal operation, PLL3 on) |
|                       | 1:0                | Y6Y7_ST0     | 01b                    |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
| 35h                   | 7                  | Y6Y7_7       | 0b                     | Y6Y7_x Output State Selection <sup>(4)</sup><br><br>0 – state0 (predefined by Y6Y7_ST0)<br>1 – state1 (predefined by Y6Y7_ST1)                                                                                                                                                                                                                                                 |                                                                                                                                                                                             |
|                       | 6                  | Y6Y7_6       | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 5                  | Y6Y7_5       | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 4                  | Y6Y7_4       | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 3                  | Y6Y7_3       | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 2                  | Y6Y7_2       | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 1                  | Y6Y7_1       | 1b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
|                       | 0                  | Y6Y7_0       | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                             |
| 36h                   | 7                  | SSC3DC       | 0b                     | PLL3 SSC down/center selection:                                                                                                                                                                                                                                                                                                                                                | 0 – down<br>1 – center                                                                                                                                                                      |
|                       | 6:0                | Pdiv6        | 01h                    | 7-Bit Y6-Output-Divider Pdiv6:                                                                                                                                                                                                                                                                                                                                                 | 0 – reset and stand-by<br>1-to-127 – divider value                                                                                                                                          |
| 37h                   | 7                  | —            | 0b                     | Reserved – do not write others than 0                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                             |
|                       | 6:0                | Pdiv7        | 01h                    | 7-Bit Y7-Output-Divider Pdiv7:                                                                                                                                                                                                                                                                                                                                                 | 0 – reset and stand-by<br>1-to-127 – divider value                                                                                                                                          |

**Table 9-6. PLL3 Configuration Register (continued)**

| OFFSET <sup>(1)</sup> | BIT <sup>(2)</sup> | ACRONYM        | DEFAULT <sup>(3)</sup> | DESCRIPTION                                                                                                                                                    |
|-----------------------|--------------------|----------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 38h                   | 7:0                | PLL3_0N [11:4] | 004h                   | PLL3_0 <sup>(5)</sup> : 30-Bit Multiplier/Divider value for frequency f <sub>VCO3_0</sub> (for more information, see <a href="#">PLL Frequency Planning</a> ). |
| 39h                   | 7:4                | PLL3_0N [3:0]  | 000h                   |                                                                                                                                                                |
|                       | 3:0                | PLL3_0R [8:5]  |                        |                                                                                                                                                                |
| 3Ah                   | 7:3                | PLL3_0R[4:0]   | 10h                    |                                                                                                                                                                |
|                       | 2:0                | PLL3_0Q [5:3]  |                        |                                                                                                                                                                |
| 3Bh                   | 7:5                | PLL3_0Q [2:0]  | 010b                   |                                                                                                                                                                |
|                       | 4:2                | PLL3_0P [2:0]  |                        |                                                                                                                                                                |
|                       | 1:0                | VCO3_0_RANGE   |                        | 00b                                                                                                                                                            |
| 3Ch                   | 7:0                | PLL3_1N [11:4] | 004h                   | PLL3_1 <sup>(5)</sup> : 30-Bit Multiplier/Divider value for frequency f <sub>VCO3_1</sub> (for more information, see <a href="#">PLL Frequency Planning</a> ). |
| 3Dh                   | 7:4                | PLL3_1N [3:0]  | 000h                   |                                                                                                                                                                |
|                       | 3:0                | PLL3_1R [8:5]  |                        |                                                                                                                                                                |
| 3Eh                   | 7:3                | PLL3_1R[4:0]   | 10h                    |                                                                                                                                                                |
|                       | 2:0                | PLL3_1Q [5:3]  |                        |                                                                                                                                                                |
| 3Fh                   | 7:5                | PLL3_1Q [2:0]  | 010b                   |                                                                                                                                                                |
|                       | 4:2                | PLL3_1P [2:0]  |                        |                                                                                                                                                                |
|                       | 1:0                | VCO3_1_RANGE   |                        | 00b                                                                                                                                                            |

- (1) Writing data beyond 50h may adversely affect device function.
- (2) All data is transferred MSB-first.
- (3) Unless a custom setting is used
- (4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.
- (5) PLL settings limits:  $16 \leq q \leq 63$ ,  $0 \leq p \leq 7$ ,  $0 \leq r \leq 511$ ,  $0 < N < 4096$

**Table 9-7. PLL4 Configuration Register**

| OFFSET <sup>(1)</sup> | BIT <sup>(2)</sup> | ACRONYM      | DEFAULT <sup>(3)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                    |  |  |
|-----------------------|--------------------|--------------|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|
| 40h                   | 7:5                | SSC4_7 [2:0] | 000b                   | SSC4: PLL4 SSC Selection (Modulation Amount) <sup>(4)</sup><br><br><div><div>Down</div><div>000 (off)<br/>001 – 0.25%<br/>010 – 0.5%<br/>011 – 0.75%<br/>100 – 1.0%<br/>101 – 1.25%<br/>110 – 1.5%<br/>111 – 2.0%</div><div>Center</div><div>000 (off)<br/>001 ± 0.25%<br/>010 ± 0.5%<br/>011 ± 0.75%<br/>100 ± 1.0%<br/>101 ± 1.25%<br/>110 ± 1.5%<br/>111 ± 2.0%</div></div> |  |  |
|                       | 4:2                | SSC4_6 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
|                       | 1:0                | SSC4_5 [2:1] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
| 41h                   | 7                  | SSC4_5 [0]   |                        |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
|                       | 6:4                | SSC4_4 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
|                       | 3:1                | SSC4_3 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
| 42h                   | 0                  | SSC4_2 [2]   | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
|                       | 7:6                | SSC4_2 [1:0] |                        |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
|                       | 5:3                | SSC4_1 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
|                       | 2:0                | SSC4_0 [2:0] | 000b                   |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
| 43h                   | 7                  | FS4_7        | 0b                     | FS4_x: PLL4 Frequency Selection <sup>(4)</sup> sl<br><br>0 – f <sub>VCO4_0</sub> (predefined by PLL4_0 – Multiplier/Divider value)<br>1 – f <sub>VCO4_1</sub> (predefined by PLL4_1 – Multiplier/Divider value)                                                                                                                                                                |  |  |
|                       | 6                  | FS4_6        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
|                       | 5                  | FS4_5        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
|                       | 4                  | FS4_4        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
|                       | 3                  | FS4_3        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
|                       | 2                  | FS4_2        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
|                       | 1                  | FS4_1        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |  |  |
|                       | 0                  | FS4_0        | 0b                     |                                                                                                                                                                                                                                                                                                                                                                                |  |  |

**Table 9-7. PLL4 Configuration Register (continued)**

| OFFSET <sup>(1)</sup> | BIT <sup>(2)</sup> | ACRONYM        | DEFAULT <sup>(3)</sup> | DESCRIPTION                                                                                                                                                                                                      |                                                                                                                                                                                             |
|-----------------------|--------------------|----------------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 44h                   | 7                  | MUX4           | 1b                     | PLL4 Multiplexer:                                                                                                                                                                                                | 0 – PLL4<br>1 – PLL4 Bypass (PLL4 is in power down)                                                                                                                                         |
|                       | 6                  | M8             | 1b                     | Output Y8 Multiplexer:                                                                                                                                                                                           | 0 – Pdiv6<br>1 – Pdiv8                                                                                                                                                                      |
|                       | 5:4                | M9             | 10b                    | Output Y9 Multiplexer:                                                                                                                                                                                           | 00 – Pdiv6-Divider<br>01 – Pdiv8-Divider<br>10 – Pdiv9-Divider<br>11 – reserved                                                                                                             |
|                       | 3:2                | Y8Y9_ST1       | 11b                    | Y8, Y9-<br>State0/1definition:                                                                                                                                                                                   | 00 – Y8/Y9 disabled to 3-State (PLL4 is in power down)<br>01 – Y8/Y9 disabled to 3-State (PLL4 on)<br>10 –Y8/Y9 disabled to low (PLL4 on)<br>11 – Y8/Y9 enabled (normal operation, PLL4 on) |
|                       | 1:0                | Y8Y9_ST0       | 01b                    |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
| 45h                   | 7                  | Y8Y9_7         | 0b                     | Y8Y9_x Output State Selection <sup>(4)</sup><br><br>0 – state0 (predefined by Y8Y9_ST0)<br>1 – state1 (predefined by Y8Y9_ST1)                                                                                   |                                                                                                                                                                                             |
|                       | 6                  | Y8Y9_6         | 0b                     |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
|                       | 5                  | Y8Y9_5         | 0b                     |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
|                       | 4                  | Y8Y9_4         | 0b                     |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
|                       | 3                  | Y8Y9_3         | 0b                     |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
|                       | 2                  | Y8Y9_2         | 0b                     |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
|                       | 1                  | Y8Y9_1         | 1b                     |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
|                       | 0                  | Y8Y9_0         | 0b                     |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
| 46h                   | 7                  | SSC4DC         | 0b                     | PLL4 SSC down/center selection:                                                                                                                                                                                  | 0 – down<br>1 – center                                                                                                                                                                      |
|                       | 6:0                | Pdiv8          | 01h                    | 7-Bit Y8-Output-Divider Pdiv8:                                                                                                                                                                                   | 0 – reset and stand-by<br>1-to-127 – divider value                                                                                                                                          |
| 47h                   | 7                  | —              | 0b                     | Reserved – do not write others than 0                                                                                                                                                                            |                                                                                                                                                                                             |
|                       | 6:0                | Pdiv9          | 01h                    | 7-Bit Y9-Output-Divider Pdiv9:                                                                                                                                                                                   | 0 – reset and stand-by<br>1-to-127 – divider value                                                                                                                                          |
| 48h                   | 7:0                | PLL4_ON [11:4] | 004h                   | PLL4_0 <sup>(5)</sup> : 30-Bit Multiplier/Divider value for frequency f <sub>VCO4_0</sub><br>(for more information, see <a href="#">PLL Frequency Planning</a> ).                                                |                                                                                                                                                                                             |
| 49h                   | 7:4                | PLL4_ON [3:0]  |                        |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
|                       | 3:0                | PLL4_OR [8:5]  | 000h                   |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
| 4Ah                   | 7:3                | PLL4_OR[4:0]   |                        |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
|                       | 2:0                | PLL4_OQ [5:3]  | 10h                    |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
| 4Bh                   | 7:5                | PLL4_OQ [2:0]  | 010b                   | f <sub>VCO4_0</sub> range selection:<br>00 – f <sub>VCO4_0</sub> < 125 MHz<br>01 – 125 MHz ≤ f <sub>VCO4_0</sub> < 150 MHz<br>10 – 150 MHz ≤ f <sub>VCO4_0</sub> < 175 MHz<br>11 – f <sub>VCO4_0</sub> ≥ 175 MHz |                                                                                                                                                                                             |
|                       | 4:2                | PLL4_OP [2:0]  |                        |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
|                       | 1:0                | VCO4_0_RANGE   | 00b                    |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
| 4Ch                   | 7:0                | PLL4_1N [11:4] | 004h                   | PLL4_1 <sup>(5)</sup> : 30-Bit Multiplier/Divider value for frequency f <sub>VCO4_1</sub><br>(for more information, see <a href="#">PLL Frequency Planning</a> ).                                                |                                                                                                                                                                                             |
| 4Dh                   | 7:4                | PLL4_1N [3:0]  |                        |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
|                       | 3:0                | PLL4_1R [8:5]  | 000h                   |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
| 4Eh                   | 7:3                | PLL4_1R[4:0]   |                        |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
|                       | 2:0                | PLL4_1Q [5:3]  | 10h                    |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
| 4Fh                   | 7:5                | PLL4_1Q [2:0]  | 010b                   | f <sub>VCO4_1</sub> range selection:<br>00 – f <sub>VCO4_1</sub> < 125 MHz<br>01 – 125 MHz ≤ f <sub>VCO4_1</sub> < 150 MHz<br>10 – 150 MHz ≤ f <sub>VCO4_1</sub> < 175 MHz<br>11 – f <sub>VCO4_1</sub> ≥ 175 MHz |                                                                                                                                                                                             |
|                       | 4:2                | PLL4_1P [2:0]  |                        |                                                                                                                                                                                                                  |                                                                                                                                                                                             |
|                       | 1:0                | VCO4_1_RANGE   | 00b                    |                                                                                                                                                                                                                  |                                                                                                                                                                                             |

(1) Writing data beyond 50h may adversely affect device function.

(2) All data is transferred MSB-first.

(3) Unless a custom setting is used

(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

(5) PLL settings limits:  $16 \leq q \leq 63$ ,  $0 \leq p \leq 7$ ,  $0 \leq r \leq 511$ ,  $0 < N < 4096$

## 10 Device and Documentation Support

### 10.1 Device Support

#### 10.1.1 Development Support

For development support see the following:

- [SMBus](#)
- [I<sup>2</sup>C Bus](#)

### 10.2 Related Documentation

For related documentation see the following:

[VCXO Application Guideline for CDCE\(L\)9xx Family](#) (SCAA085)

### 10.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 10-1. Related Links**

| PARTS    | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| CDCE949  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CDCEL949 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 10.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.5 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.6 Trademarks

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### 10.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.8 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

---

**Changes from Revision F (October 2016) to Revision G (January 2024)**
**Page**


---

- Changed data sheet title from: *CDCE(L)913: Flexible Low Power LVCMOS Clock Generator With SSC Support for EMI Reduction* to *CDCE(L)949: Flexible Low Power LVCMOS Clock Generator With SSC Support for EMI Reduction* ..... [1](#)
  - Updated the numbering format for tables, figures, and cross-references throughout the document..... [1](#)
  - Changed all instances of legacy terminology to controller and target where I<sup>2</sup>C is mentioned..... [1](#)
  - Changed the *Device Information* table to *Package Information* ..... [1](#)
- 

**Changes from Revision E (August 2016) to Revision F (October 2016)**
**Page**


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- Changed data sheet title from: *CDCEx949 Programmable 4-PLL VCXO Clock Synthesizer With 1.8-V, 2.5-V, and 3.3-V LVCMOS Outputs* to: *CDCE(L)913: Flexible Low Power LVCMOS Clock Generator With SSC Support for EMI Reduction* ..... [1](#)
- 

**Changes from Revision D (March 2010) to Revision E (August 2016)**
**Page**


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- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... [1](#)
  - Condensed down bullets in *Features* ..... [1](#)
  - Deleted 'General Purpose Frequency Synthesizing' from *Applications* ..... [1](#)
  - Updated values in the *Thermal Information* table to align with JEDEC standards ..... [6](#)
  - Changed Byte Read Protocol image, second S to Sr..... [17](#)
  - Changed 100 MHz <  $f_{VCO}$  > 200 MHz; TO 80 MHz ≤  $f_{VCO}$  ≤ 230 MHz; and changed 0 ≤ p ≤ 7 TO 0 ≤ p ≤ 4 [20](#)
  - Changed under Example, fifth row, N", 2 places TO N'..... [20](#)
- 

**Changes from Revision C (October 2009) to Revision D ( )**
**Page**


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- Added PLL settings limits: 16 ≤ q ≤ 63, 0 ≤ p ≤ 7, 0 ≤ r ≤ 511, 0 < N < 4096 foot to PLL1, PLL2, PLL3, & PLL4 Configure Register Table..... [25](#)
- 

**Changes from Revision B (September 2009) to Revision C ( )**
**Page**


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- Deleted sentence - A different default setting can be programmed on customer request. Contact Texas Instruments sales or marketing representative for more information..... [14](#)
- 

**Changes from Revision A (December 2007) to Revision B ( )**
**Page**


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- Added Note 3: SDA and SCL can go up to 3.6 V as stated in the *Recommended Operating Conditions* table. [5](#)
- 

**Changes from Revision \* (August 2007) to Revision A ( )**
**Page**


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- Changed the THERMAL RESISTANCE FOR TSSOP table..... [6](#)
  - Changed *Generic Configuration Register* table RID From: 0h To: Xb..... [25](#)
  - Added note to the PWDN description, *Generic Configuration Register* table..... [25](#)
-

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CDCE949PW</a>   | Active        | Production           | TSSOP (PW)   24 | 60   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDCE949             |
| CDCE949PW.B                 | Active        | Production           | TSSOP (PW)   24 | 60   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDCE949             |
| CDCE949PWG4                 | Active        | Production           | TSSOP (PW)   24 | 60   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDCE949             |
| <a href="#">CDCE949PWR</a>  | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDCE949             |
| CDCE949PWR.B                | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDCE949             |
| CDCE949PWRG4                | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDCE949             |
| CDCE949PWRG4.B              | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDCE949             |
| <a href="#">CDCEL949PW</a>  | Active        | Production           | TSSOP (PW)   24 | 60   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDCEL949            |
| CDCEL949PW.B                | Active        | Production           | TSSOP (PW)   24 | 60   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDCEL949            |
| <a href="#">CDCEL949PWR</a> | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDCEL949            |
| CDCEL949PWR.B               | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDCEL949            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF CDCE949 :**

- Automotive : [CDCE949-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDCE949PWR   | TSSOP        | PW              | 24   | 2000 | 330.0              | 16.4               | 6.95    | 8.3     | 1.6     | 8.0     | 16.0   | Q1            |
| CDCE949PWRG4 | TSSOP        | PW              | 24   | 2000 | 330.0              | 16.4               | 6.95    | 8.3     | 1.6     | 8.0     | 16.0   | Q1            |
| CDCEL949PWR  | TSSOP        | PW              | 24   | 2000 | 330.0              | 16.4               | 6.95    | 8.3     | 1.6     | 8.0     | 16.0   | Q1            |

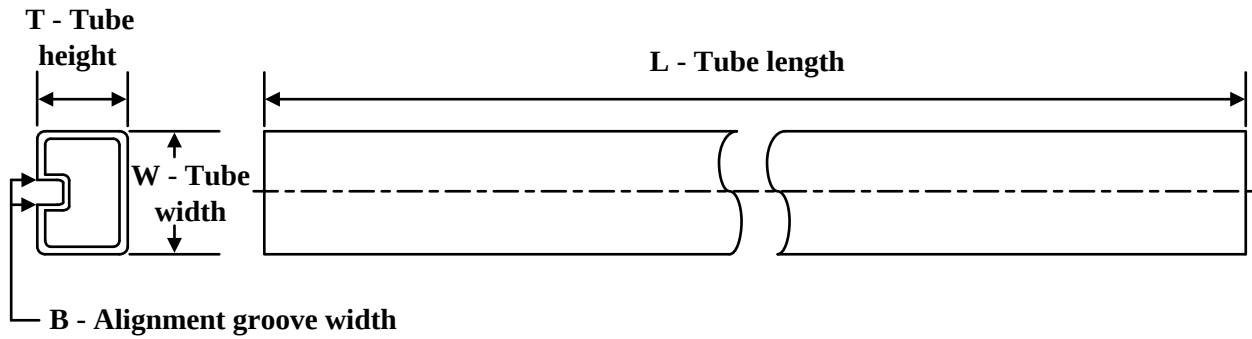
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

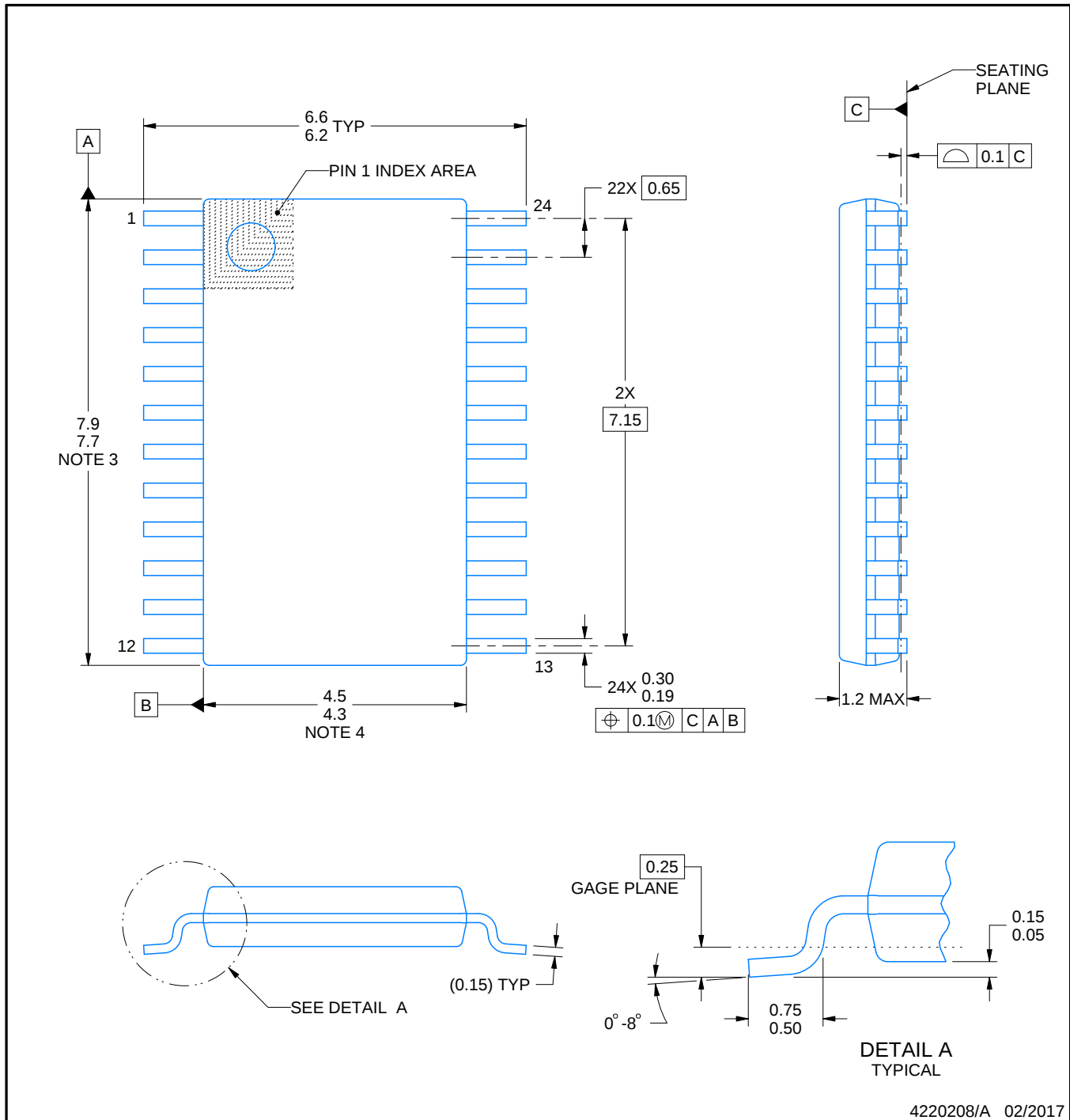
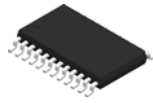
| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDCE949PWR   | TSSOP        | PW              | 24   | 2000 | 356.0       | 356.0      | 35.0        |
| CDCE949PWRG4 | TSSOP        | PW              | 24   | 2000 | 356.0       | 356.0      | 35.0        |
| CDCEL949PWR  | TSSOP        | PW              | 24   | 2000 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CDCE949PW    | PW           | TSSOP        | 24   | 60  | 530    | 10.2   | 3600   | 3.5    |
| CDCE949PW.B  | PW           | TSSOP        | 24   | 60  | 530    | 10.2   | 3600   | 3.5    |
| CDCE949PWG4  | PW           | TSSOP        | 24   | 60  | 530    | 10.2   | 3600   | 3.5    |
| CDCEL949PW   | PW           | TSSOP        | 24   | 60  | 530    | 10.2   | 3600   | 3.5    |
| CDCEL949PW.B | PW           | TSSOP        | 24   | 60  | 530    | 10.2   | 3600   | 3.5    |



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## NOTES:

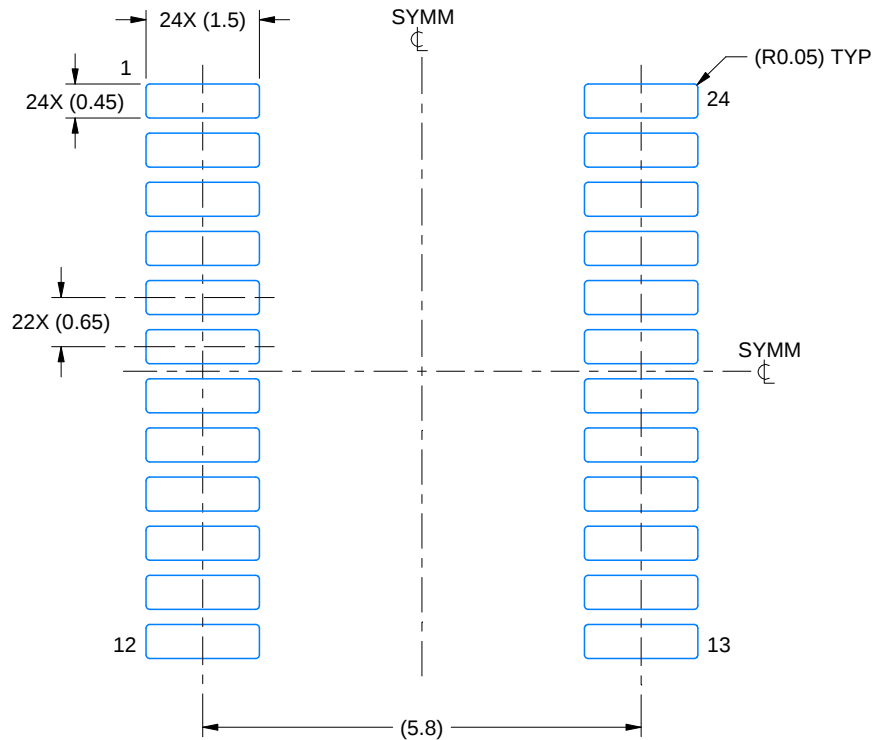
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

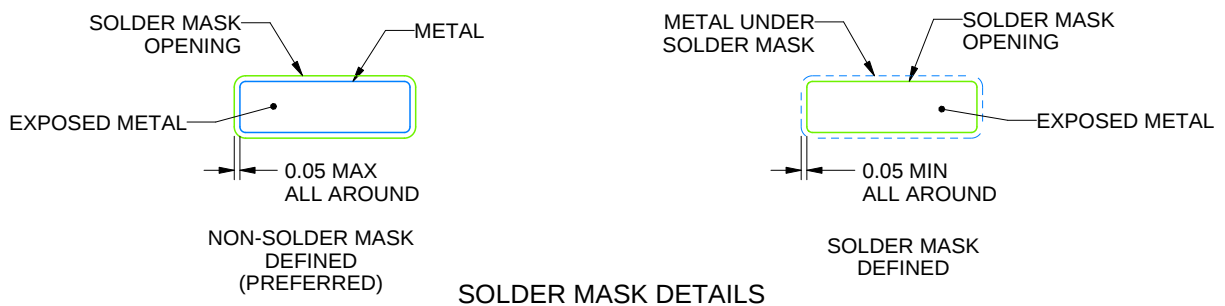
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

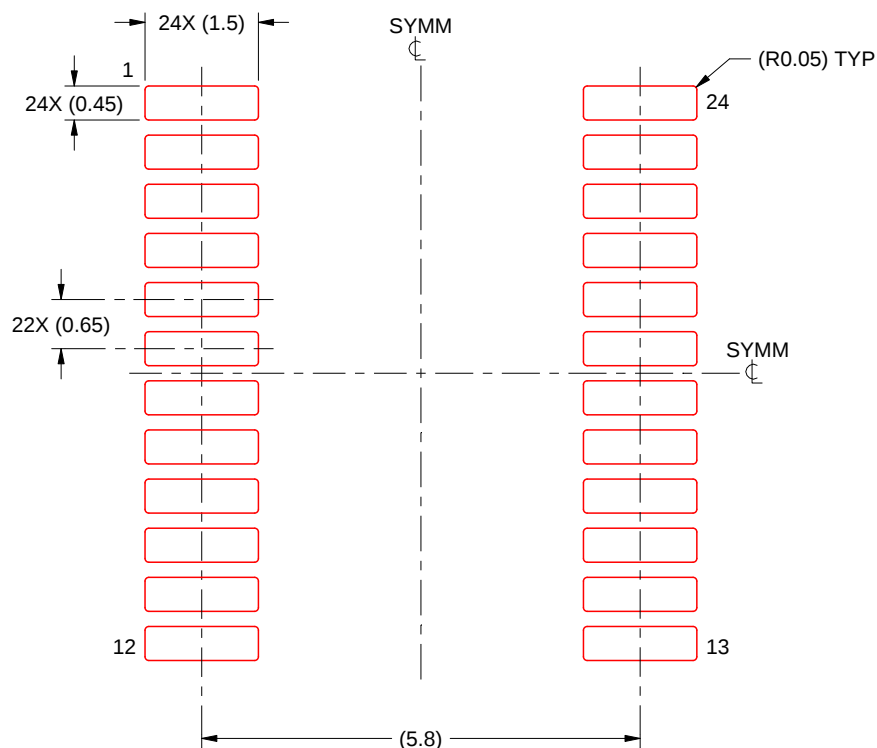
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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