DS90UB662-Q1 Quad 3-Gbps FPD-Link III Deserializer Hub With Single CSI-2 Output Port

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 2: –40°C to +105°C ambient operating temperature range
  - Device HBM ESD classification Level ±3 kV
  - Device CDM ESD classification Level C5
- Quad deserializer hub aggregates data from up to 4 sensors simultaneously supports
- Supports 1-Megapixel sensors up to 60-Hz frame rate and 2-Megapixel sensors up to 30-Hz frame rate
- Precise multi-camera synchronization
- MIPI DPHY version 1.2 / CSI-2 version 1.3 compliant
  - 1 × CSI-2 MIPI Output Port
  - Supports 1, 2, 3, 4 data lanes
  - CSI-2 data rate scalable for 400 Mbps / 800 Mbps / 1.2 Gbps / 1.5 Gbps / 1.6 Gbps per lane
- Ultra-low data and control path latency
- Supports single-ended coaxial including Power-over-Coax (PoC) or Shielded Twisted-Pair (STP) cable
- Adaptive receive equalization
- Dual I2C ports with fast-mode plus up to 1 Mbps
- Flexible GPIOs for sensor synchronization and diagnostics
- Compatible with DS90UB633A-Q1 serializer and DS90UB63x CSI-2 Serializers
- Internal programmable precision frame sync generator
- Line fault detection and advanced diagnostics
- *Functional Safety-Capable*
  - Documentation available to aid ISO 26262 system design

2 Applications

- Automotive ADAS
  - Rear View Cameras (RVC)
  - Surround View Systems (SVS)
  - Camera Monitoring Systems (CMS)
  - Forward Vision Cameras (FC)
  - Driver Monitoring Systems (DMS)
  - Satellite RADAR, Time-of-Flight (ToF), and LIDAR sensors modules
  - Sensor fusion
- Security and Surveillance

3 Description

The DS90UB662-Q1 is a versatile sensor hub capable of connecting serialized sensor data received from four independent video data streams through a FPD-Link III interface. When paired with a DS90UB633A-Q1 or DS90UB63x CSI-2 serializer, the DS90UB662-Q1 receives data from 1-Megapixel image sensors supporting 720p/800p/960p/1MP resolution at 30-Hz or 60-Hz frame rates. Data is received and aggregated into a MIPI CSI-2 compliant output for interconnect to a downstream processor.

The DS90UB662-Q1 includes four FPD-Link III deserializers, each enabling a connection through cost-effective 50-Ω single-ended coaxial or 100-Ω differential STP cables. The receive equalizers automatically adapt to compensate for cable loss characteristics, including degradation over time.

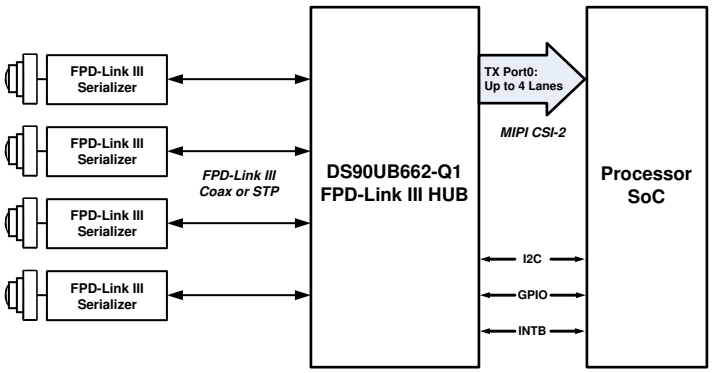
Each of the FPD-Link III interfaces also includes a separate low latency bidirectional control channel that continuously conveys I2C, GPIOs, and other control information. General-purpose I/O signals such as those required for camera synchronization and diagnostics features also make use of this bidirectional control channel.

The DS90UB662-Q1 is AEC-Q100 qualified for automotive applications and is offered in a cost-effective and space-saving 64-pin VQFN package.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
DS90UB662-Q1	VQFN (64)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2016) to Revision A (September 2018)	Page
• Updated marketing status from Advance Information to production data.	1

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5 Pin Configuration and Functions

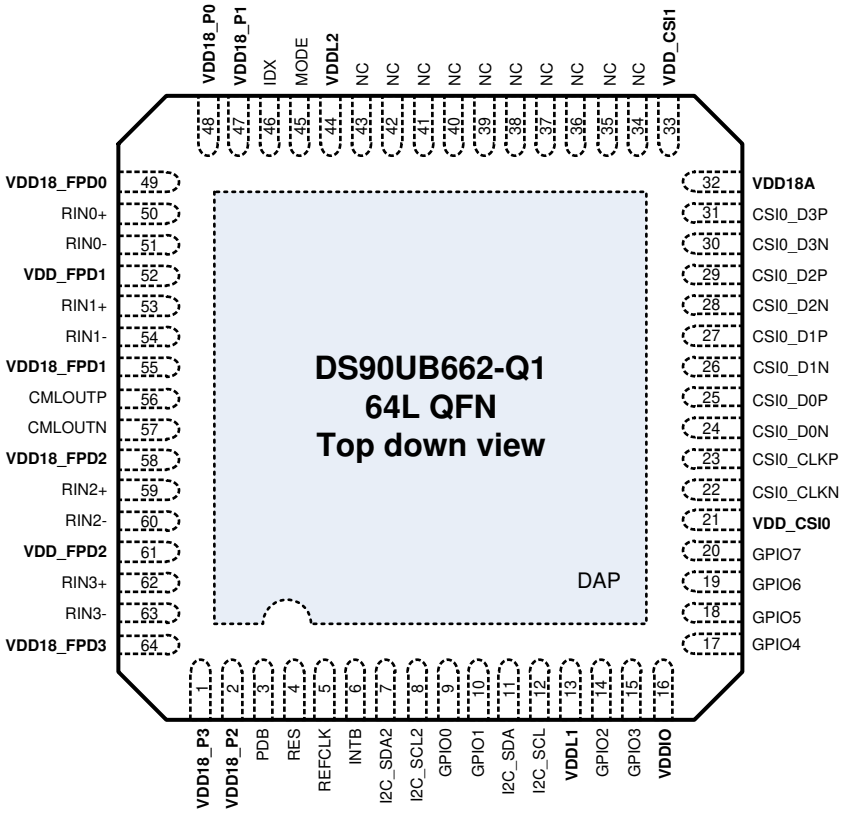

Figure 5-1. RTD Package 64-Pin VQFN (Top View)

Pin Functions

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
MIPI CSI-2 TX INTERFACE			
CSI_CLKN	22	O	CSI-2 differential clock output pins. Leave unused pins as No Connect.
CSI_CLKP	23		
CSI_D0N	24		CSI-2 differential data output pins. Use CSI_PORT_SEL (see Table 7-68), CSI_CTL (see Table 7-69), and CSI_CTL2 (see Table 7-70) registers for the CSI-2 TX control. Leave unused pins as No Connect.
CSI_D0P	25		
CSI_D1N	26		
CSI_D1P	27		
CSI_D2N	28		
CSI_D2P	29		
CSI_D3N	30		
CSI_D3P	31		
FPD-LINK III RX INTERFACE			
RIN0+	50	I/O	FPD-Link III RX Port 0 pins. The port receives FPD-Link III high-speed forward channel video and control data and transmits back channel control data. It can interface with a compatible FPD-Link III serializer TX through a STP or coaxial cable (see Figure 8-6 and Figure 8-7). It must be AC-coupled per Table 8-4. If port is unused, set RX_PORT_CTL register bit 0 to 0 to disable RX Port 0 (see Table 7-30) and leave the pins as No Connect.
RIN0-	51		
RIN1+	53		FPD-Link III RX Port 1 pins. The port receives FPD-Link III high-speed forward channel video and control data and transmits back channel control data. It can interface with a compatible FPD-Link III serializer TX through a STP or coaxial cable (see Figure 8-6 and Figure 8-7). It must be AC-coupled per Table 8-4. If port is unused, set RX_PORT_CTL register bit 1 to 0 to disable RX Port 1 (see Table 7-30) and leave the pins as No Connect.
RIN1-	54		
RIN2+	59		FPD-Link III RX Port 2 pins. The port receives FPD-Link III high-speed forward channel video and control data and transmits back channel control data. It can interface with a compatible FPD-Link III serializer TX through a STP or coaxial cable (see Figure 8-6 and Figure 8-7). It must be AC-coupled per Table 8-4. If port is unused, set RX_PORT_CTL register bit 2 to 0 to disable RX Port 2 (See Table 7-30) and leave the pins as No Connect.
RIN2-	60		
RIN3+	62		FPD-Link III RX Port 3 pins. The port receives FPD-Link III high-speed forward channel video and control data and transmits back channel control data. It can interface with a compatible FPD-Link III serializer TX through a STP or coaxial cable (see Figure 8-6 and Figure 8-7). It must be AC-coupled per Table 8-4. If port is unused, set RX_PORT_CTL register bit 3 to 0 to disable RX Port 3 (see Table 7-30) and leave the pins as No Connect.
RIN3-	63		
SYNCHRONIZATION AND GENERAL-PURPOSE I/O			
GPIO0	9	I/O, PD	General-Purpose Input/Output pins. The pins can be used to control and respond to various commands. They may be configured to be input signals for the corresponding GPIOs on the serializer or they may be configured to be outputs to follow local register settings. At power up, the GPIO pins are disabled and by default include a pulldown resistor (25-kΩ typ). See *Section 7.4.11.* for programmability. If unused, leave the pin as No Connect.
GPIO1	10		
GPIO2	14		
GPIO3	15		
GPIO4	17		
GPIO5	18		
GPIO6	19		
GPIO7	20		
INTB	6	O, OD	Interrupt Output pin. INTB is an active-low open drain and controlled by the status registers. See *Section 7.5.9*. Recommend a 4.7-kΩ Pullup to to 1.8 V or 3.3 V. If unused, leave the pin as No Connect.
SERIAL CONTROL BUS (I2C)			

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PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
I2C_SCL	12	I/O, OD	Primary I2C Clock Input / Output interface pin. See *Section 7.5.1*. Recommend a 2.2-kΩ to 4.7-kΩ Pullup(1) to 1.8 V or 3.3 V.
I2C_SDA	11	I/O, OD	Primary I2C Data Input / Output interface pin. See *Section 7.5.1*. Recommend a 2.2-kΩ to 4.7-kΩ Pullup(1) to 1.8 V or 3.3 V.
I2C_SCL2	8	I/O, OD	Secondary I2C Clock Input / Output interface pin. See *Section 7.5.2*. Recommend a 2.2-kΩ to 4.7-kΩ Pullup(1) to 1.8 V or 3.3 V.
I2C_SDA2	7	I/O, OD	Secondary I2C Data Input / Output interface pin. See *Section 7.5.2*. Recommend a 2.2-kΩ to 4.7-kΩ Pullup(1) to 1.8 V or 3.3 V.
CONFIGURATION AND CONTROL			
IDX	46	S	I2C Serial Control Bus Device ID Address Select configuration pin. Connect to an external pullup to VDD18 and a pulldown to GND to create a voltage divider. See Table 7-15.
MODE	45	S	Mode Select configuration pin. Connect to external pullup to VDD18 and a pulldown to GND to create a voltage divider. See Table 7-1.
PDB	3	I, PD	Inverted Power-Down input pin. Typically connected to a processor GPIO with a pulldown. When PDB input is brought HIGH, the device is enabled and internal registers and state machines are reset to default values. Asserting PDB signal low will power down the device and consume minimum power. The default function of this pin is PDB = LOW; POWER DOWN with an internal 50-kΩ internal pulldown enabled. PDB should remain low until after power supplies are applied and reach minimum required levels. See *Section 9.1*. **INPUT IS 3.3-V TOLERANT** PDB = 1.8 V, device is enabled (normal operation) PDB = 0 V, device is powered down.
POWER AND GROUND			
VDDIO	16	P	1.8-V (±5%) OR 3.3-V (±10%) LVCMOS I/O Power Requires 1-µF and 0.1-µF or 0.01-µF capacitors to GND.
VDD_CSI VDD_CSI	21 33	P	1.1-V (±5%) Power Supplies Requires 0.1-µF or 0.01-µF capacitors to GND at each VDD pin. Additional 1-µF and 10-µF decoupling is recommended for the pin group.
VDDL1 VDDL2	13 44	P	1.1-V (±5%) Power Supplies Requires 0.1-µF or 0.01-µF capacitors to GND at each VDD pin. Additional 1-µF and 10-µF decoupling is recommended for the pin group.
VDD_FPD1 VDD_FPD2	52 61	P	1.1-V (±5%) Power Supplies Requires 0.1-µF or 0.01-µF capacitors to GND at each VDD pin. Additional 1-µF and 10-µF decoupling is recommended for the pin group.
VDD18_P2 VDD18_P3 VDD18_P1 VDD18_P0	2 1 47 48	P	1.8-V (±5%) Power Supplies Requires 0.1-µF or 0.01-µF capacitors to GND at each VDD pin. Additional 1-µF, and 10-µF decoupling is recommended for the pin group.
VDD18A	32	P	1.8-V (±5%) Power Supplies Requires 0.1-µF or 0.01-µF capacitors to GND at each VDD pin. Additional 1-µF, and 10-µF decoupling is recommended for the pin group.
VDD18_FPD0 VDD18_FPD1 VDD18_FPD2 VDD18_FPD3	49 55 58 64	P	1.8-V (±5%) Power Supplies Requires 0.1-µF or 0.01-µF capacitors to GND at each VDD pin. Additional 1-µF, and 10-µF decoupling is recommended for the pin group.
GND	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the VQFN package. Connect to the ground plane (GND).
OTHERS			
REFCLK	5	I	Reference clock oscillator input. Typically connected to a 23-MHz to 26-MHz LVCMOS-level oscillator (100 ppm). For 400-Mbps, 800-Mbps or 1.6-Gbps CSI-2 data rates, use 25-MHz frequency. For the oscillator requirements, see *Section 7.4.4*. For other common CSI-2 data rates, see *Section 7.4.19*.
RES	4	-	This pin must be tied to GND for normal operation.

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PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
CMLOUTP	56	O	Channel Monitor Loop-through Driver differential output. Route to a test point or a pad with 100-Ω termination resistor between pins for channel monitoring (recommended). See *Section 7.4.8*.
CMLOUTN	57		
NC	34 - 43	-	NO CONNECT pins. Leave these pins unconnected.

(1) Optimum Pullup Resistor (RPU) value depends on the I2C mode of operation, refer to *I2C Bus Pullup Resistor Calculation* (SLVA689)

The definitions below define the functionality of the I/O cells for each pin. TYPE:

- I = Input
- O = Output
- I/O = Input/Output
- S = Configuration/Strap Input (All strap pins have internal pulldowns determined by IOZ specification. If the default strap value needs to be changed then an external resistor should be used.
- PD = Internal Pulldown
- OD = Open Drain
- P = Power Supply
- G = Ground

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
Supply voltage	VDD11 (VDD_CSI, VDDL1, VDDL2, VDD_FPD1, VDD_FPD2)		–0.3	1.32 and <V (VDD18)	V
	VDD18 (VDD18_P0, VDD18_P1, VDD18_P2, VDD18_P3, VDD18A, VDD18_FPD0, VDD18_FPD1, VDD18_FPD2, VDD18_FPD3)		–0.3	2.16	V
	VDDIO		–0.3	3.96	V
FPD-Link III input voltage	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	Device powered up (All supplies within recommended operating conditions)	–0.3	2.75	V
		Device powered down, Transient voltage	–0.3	1.45	V
		Device powered down, DC voltage	–0.3	1.35	V
CSI-2 voltage	CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_D2P, CSI_D2N, CSI_D3P, CSI_D3N, CSI_CLKP, CSI_CLKN		–0.3	1.32	V
LVCMOS IO voltage	PDB		–0.3	3.96	V
	GPIO[7:0], REFCLK, RES, CMLOUTP, CMLOUTN		–0.3	$V_{(VDDIO)}$ + 0.3	V
Configuration input voltage	MODE, IDX		–0.3	$V_{(VDD18)}$ + 0.3	V
Open-Drain voltage	I2C_SDA, I2C_SCL, I2C_SDA2, I2C_SCL2, INTB		–0.3	3.96	V
NC voltage	No Connect pins, 34 - 43		–0.3	1.32	V
Junction temperature				150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office or Distributors for availability and specifications.

(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 3A	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	±6000	V
			Other pins	±3000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6		±1000	V
		ESD Rating (IEC 61000-4-2) R_D= 330 Ω, C_S = 150 pF	Contact Discharge (RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-)	±10 000	V
			Air Discharge (RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-)	±21 000	V
		ESD Rating (ISO 10605) R_D= 330 Ω, C_S = 150 pF and 330 pF R_D= 2 kΩ, C_S = 150 pF and 330 pF	Contact Discharge (RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-)	±10 000	V
			Air Discharge (RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-)	±21 000	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	$V_{(VDD11)}$	1.045	1.1	1.155	V
	$V_{(VDD18)}$	1.71	1.8	1.89	V
LVCMOS I/O supply voltage	$V_{(VDDIO)}$ = 1.8 V	1.71	1.8	1.89	V
	OR $V_{(VDDIO)}$ = 3.3 V	3.0	3.3	3.6	V
Open-drain voltage	INTB = $V_{(INTB)}$, I2C pins = $V_{(I2C)}$	1.71		3.6	V
Operating free-air temperature, T_A		–40	25	105	°C

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Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
MIPI data rate (per CSI-2 lane)		368	800	1664	Mbps
MIPI CSI-2 HS clock frequency		184	400	832	MHz
Reference clock frequency		23	25	26	MHz
Spread-spectrum reference clock modulation percentage	REFCLK, Center spread	-0.5		0.5	%
	REFCLK, Down spread	-1		0	%
Local I^2C frequency, f_{I2C}				1	MHz
Supply noise, See Note 1	$V_{(VDD11)}$			25	mV_{P-P}
	$V_{(VDD18)}$			50	mV_{P-P}
	$V_{(VDDIO)}$ = 1.8 V			50	mV_{P-P}
	$V_{(VDDIO)}$ = 3.3 V			100	mV_{P-P}
	RIN0+, RIN1+, RIN2+, RIN3+		10		mV_{P-P}

6.4 Thermal Information

THERMAL METRIC(1)		DS90UB662-Q1 RTD (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.8	°C/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	10.4	°C/W
$R_{\theta JC(BOT)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
POWER CONSUMPTION							
P_T	Total power consumption in operation mode(1) (2)	CSI-2 TX = 4 data lanes + 1 CLK lane CSI-2 TX line rate = 1.664 Gbps 4 × FPD-Link III RX inputs FPD-Link III line rate = 4.16 Gbps CSI-2 mode, Default registers	VDD18, VDD11, VDDIO		800	999	mW

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Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{DDT1}	Deserializer supply current (includes load current)(1) (2)	CSI-2 TX = 4 data lanes + 1 CLK lane CSI-2 TX line rate = 1.664 Gbps 4 × FPD-Link III RX inputs FPD-Link III line rate = 4.16 Gbps CSI-2 mode, Default registers	VDD11		165	310	mA
			VDD18		295	340	
			VDDIO		2	3	
		CSI-2 TX = 4 data lanes + 1 CLK lane CSI-2 TX line rate = 832 Mbps 4 × FPD-Link III RX inputs FPD-Link III line rate = 4.16 Gbps CSI-2 mode, Default registers	VDD11		150	290	mA
			VDD18		295	340	
			VDDIO		2	3	
I_{DDT2}	Deserializer supply current (includes load current)(1) (2)	CSI-2 TX = 4 data lanes + 1 CLK lane CSI-2 TX line rate = 1.664 Gbps 4 × FPD-Link III RX inputs FPD-Link III line rate = 1.867 Gbps RAW12 HF mode, Default registers	VDD11		122	300	mA
			VDD18		263	305	
			VDDIO		2	3	
I_{DDZ}	Deserializer shutdown current(1) (2)	PDB = LOW	VDD11			160	mA
			VDD18			4	
			VDDIO			3	
1.8-V LVCMOS I/O							
V_{OH}	High level output voltage	I_{OH} = –2 mA, $V_{(VDDIO)}$ = 1.71 to 1.89 V	GPIO[7:0]	$V_{(VDDIO)}$ – 0.45		$V_{(VDDIO)}$	V
V_{OL}	Low level output voltage	I_{OL} = 2 mA, $V_{(VDDIO)}$ = 1.71 to 1.89 V	GPIO[7:0], INTB	GND		0.45	V
V_{IH}	High level input voltage	$V_{(VDDIO)}$ = 1.71 to 1.89 V	GPIO[7:0], PDB, REFCLK	0.65 × $V_{(VDDIO)}$		$V_{(VDDIO)}$	V
V_{IL}	Low level input voltage			GND		0.35 × $V_{(VDDIO)}$	
I_{IH}	Input high current	V_{IN} = $V_{(VDDIO)}$ = 1.71 to 1.89 V, internal pulldown enabled	GPIO[7:0], PDB	45		115	µA
		V_{IN} = $V_{(VDDIO)}$ = 1.71 to 1.89 V, internal pulldown disabled	GPIO[7:0], REFCLK			20	µA
I_{IL}	Input low current	V_{IN} = 0 V	GPIO[7:0], PDB, REFCLK	–20		3.5	µA
$I_{IN-STRAP}$	Strap pin input current	V_{IN} = 0 V to $V_{(VDD18)}$	MODE, IDX	–1		1	µA
I_{OS}	Output short circuit current	V_{OUT} = 0 V	GPIO[7:0]		–40		mA
I_{OZ}	TRI-STATE output current	V_{OUT} = 0 V or $V_{(VDDIO)}$, PDB = LOW	GPIO[7:0]	–20		20	µA
3.3-V LVCMOS I/O							
V_{OH}	High level output voltage	I_{OH} = –4 mA, $V_{(VDDIO)}$ = 3.0 to 3.6 V	GPIO[7:0]	2.4		$V_{(VDDIO)}$	V
V_{OL}	Low level output voltage	I_{OL} = 4 mA, $V_{(VDDIO)}$ = 3.0 to 3.6 V	GPIO[7:0], INTB	GND		0.4	V
V_{IH}	Highlevel input voltage	$V_{(VDDIO)}$ = 3.0 to 3.6 V	GPIO[7:0], REFCLK	2		$V_{(VDDIO)}$	V
			PDB	1.17		$V_{(VDDIO)}$	V
V_{IL}	Low level input voltage	$V_{(VDDIO)}$ = 3.0 to 3.6 V	GPIO[7:0], REFCLK	GND		0.8	V
			PDB	GND		0.63	V
I_{IH}	Input high current	V_{IN} = $V_{(VDDIO)}$ = 3.0 to 3.6 V, internal pulldown enabled	GPIO[7:0], PDB	85		215	µA
		V_{IN} = $V_{(VDDIO)}$ = 3.0 to 3.6 V, internal pulldown disabled	GPIO[7:0], REFCLK			30	µA
I_{IL}	Input low current	V_{IN} = $V_{(VDDIO)}$ = 0 V	GPIO[7:0], PDB, REFCLK	–20		3.5	µA

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Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
I_{OS}	Output short circuit current	V_{OUT} = 0 V		GPIO[7:0]		–65		mA
I_{OZ}	TRI-STATE output current	V_{OUT} = 0 V or $V_{(VDDIO)}$, PDB = LOW		GPIO[7:0]	–20		30	µA
I²C SERIAL CONTROL BUS								
V_{IH}	Input high level			I2C_SDA, I2C_SCL I2C_SDA2, I2C_SCL2	0.7 × $V_{(I2C)}$		$V_{(I2C)}$	V
V_{IL}	Input low level				GND		0.3 × $V_{(I2C)}$	V
V_{HYS}	Input hysteresis					50		mV
V_{OL1}	Output low level	$V_{(I2C)}$ = 3.0 to 3.6 V, I_{OL} = 3 mA	Standard-mode Fast-mode		0		0.4	V
		$V_{(I2C)}$ = 3.0 to 3.6 V, I_{OL} = 20 mA	Fast-mode Plus					
V_{OL2}	Output low level	$V_{(I2C)}$ = 1.71 to 1.89 V, I_{OL} = 2 mA	Fast-mode Fast-mode Plus		0		0.2 × $V_{(I2C)}$	V
I_{IN}	Input current	V_{IN} = 0 V or $V_{(I2C)}$			–10		10	µA
C_{IN}	Input capacitance					5		pF
FPD-LINK III RECEIVER INPUT								
V_{CM}	Common mode voltage			RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		1.2		V
R_T	Internal termination resistance	Single-ended RIN+ or RIN-			40	50	60	Ω
		Differential across RIN+ and RIN-			80	100	120	Ω
FPD-LINK III BACK CHANNEL DRIVER OUTPUT								
V_{OUT-BC}	Back channel single-ended output voltage	R_L = 50 Ω Coaxial configuration Forward channel disabled		RIN0+, RIN1+ RIN2+, RIN3+	190	220	260	mV
V_{OD-BC}	Back channel differential output voltage $V_{(RIN+)}$ - $V_{(RIN-)}$	R_L = 100 Ω STP configuration Forward channel disabled		RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	380	440	520	mV
HSTX DRIVER								
V_{CMTX}	HS transmit static common-mode voltage			CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_D2P, CSI_D2N, CSI_D3P, CSI_D3N, CSI_CLKP, CSI_CLKN	150	200	250	mV
$\lvert\Delta V_{CMTX(1,0)}\rvert$	V_{CMTX} mismatch when output is 1 or 0						5	mV_{P-P}
$\lvert V_{OD}\rvert$	HS transmit differential voltage				140	200	270	mV
$\lvert\Delta V_{OD}\rvert$	V_{OD} mismatch when output is 1 or 0						14	mV
V_{OHHS}	HS output high voltage						360	mV
Z_{OS}	Single-ended output impedance				40	50	62.5	Ω
ΔZ_{OS}	Mismatch in single-ended output impedance						10	%
LPTX DRIVER								

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PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	CSI-2 TX line rate ≤ 1.5 Gbps	CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_D2P, CSI_D2N, CSI_D3P, CSI_D3N, CSI_CLKP, CSI_CLKN	1.1	1.2	1.3	V
		CSI-2 TX line rate > 1.5 Gbps		0.95		1.3	V
V_{OL}	Low level output voltage			–50		50	mV
Z_{OLP}	Output impedance			110			Ω

(1) For typ: Data comes from initial bench validation and does not take into account activity of all IO pins.
(2) For max (estimated): Data comes from initial bench validation and does not take into account activity of all IO pins. Maximum values are estimated based on initial bench validation and are not ensured.

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6.6 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
LVCMOS I/O							
t_{CLH}	LVCMOS low-to-high transition time	$V_{(VDDIO)}$ = 1.71 V to 1.89 V OR $V_{(VDDIO)}$ = 3.0 V to 3.6 V C_L = 8 pF (lumped load) Default Registers (Figure 6-1)	GPIO[7:0]		2.5		ns
t_{CHL}	LVCMOS high-to-low transition time		GPIO[7:0]		2.5		ns
t_{PDB}	PDB reset pulse width	Power supplies applied and stable (Figure 9-1)	PDB	2			ms
FPD-LINK III RECEIVER INPUT							
V_{IN}	Single ended input voltage	Coaxial cable attenuation = -19.2 dB @ 2.1 GHz	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	60			mV
V_{ID}	Differential input voltage	STP cable attenuation = -19.6 dB @ 2.1 GHz		115			mV
t_{DDLT}	Deserializer data lock time	Raw Mode, paired with DS90UB633A-Q1, coaxial cable attenuation = -14 dB @ 1.0 GHz, AEQ range +/-3			15	30	ms
		Raw Mode, paired with DS90UB633A-Q1, coaxial cable attenuation = -14 dB @ 1.0 GHz, AEQ default range			400		ms
t_{IJIT}	Input Jitter	CSI-2 Mode, paired with DS90UB63x CSI-2 Serializer, coaxial cable attenuation = -19.2 dB @ 2.1 GHz, Jitter frequency > FPD3_PCLK(1) / 15 See Section 7.4.6			0.4		UI
		CSI-2 Mode, paired with DS90UB63x CSI-2 Serializer, STP cable attenuation = -19.6 dB @ 2.1 GHz, Jitter frequency > FPD3_PCLK(1) / 15 See Section 7.4.6					
FPD-LINK III BACK CHANNEL DRIVER							
E_{W-BC}	Back channel output eye width	Coaxial or STP configuration, f_{BC} = 2.5 Mbps	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	0.7	0.8		UI_{BC}
E_{H-BC}	Back channel output eye height	Coaxial configuration, f_{BC} = 52 Mbps		130	160		mV
		STP configuration, f_{BC} = 52 Mbps		260	320		mV
f_{BC}	Back channel data	CSI-2 synchronous mode	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		2x REFCLK		Mbps
		CSI-2 synchronous mode, no REFCLK		46		56	Mbps
		CSI-2 non-synchronous mode			2x REFCLK /5		Mbps
		Raw Mode			REFCLK /10		Mbps

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6.7 CSI-2 Timing Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
HSTX DRIVER							
$HSTX_{DBR}$	Data rate	REFCLK = 23 MHz	CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_D2P, CSI_D2N, CSI_D3P, CSI_D3N	368	736	1472	Mbps
		REFCLK = 25 MHz		400	800	1600	Mbps
		REFCLK = 26 MHz		416	832	1664	Mbps
f_{CLK}	DDR clock frequency	REFCLK = 23 MHz	CSI_CLKP, CSI_CLKN	184	368	736	MHz
		REFCLK = 25 MHz		200	400	800	MHz
		REFCLK = 26 MHz		208	416	832	MHz
$\Delta V_{CMTX(HF)}$	Common mode voltage variations HF	Above 450 MHz	CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_D2P, CSI_D2N, CSI_D3P, CSI_D3N, CSI_CLKP, CSI_CLKN			15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common mode voltage variations LF	Between 50 and 450 MHz				25	mV_{RMS}
t_{RHS} t_{FHS}	20% to 80% rise and fall HS	HS data rates ≤ 1 Gbps (UI ≥ 1 ns)				0.3	UI
		HS data rates > 1 Gbps (UI ≤ 1 ns) but less than 1.5 Gbps (UI ≥ 0.667 ns)				0.35	UI
		Applicable when supporting maximum HS data rates ≤ 1.5 Gbps.		100			ps
		Applicable for all HS data rates when supporting > 1.5 Gbps.				0.4	UI
		Applicable for all HS data rates when supporting > 1.5 Gbps.		50			ps
SDD_{TX}	TX differential return loss	f_{LPMAX}	HS data rates <1.5 Gbps		-18		dB
		f_H			-9		dB
		f_{MAX}			-3		dB
		f_{LPMAX}	HS data rates >1.5 Gbps		-18		dB
		f_H			-4.5		dB
		f_{MAX}			-2.5		dB
SCC_{TX}	TX common mode return loss	DC to f_{LPMAX}	All HS data rates		-20		dB
		f_H			-15		dB
		f_{MAX}			-9		dB
LPTX DRIVER							

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PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
t_{RLP}	Rise time LP(1)	15% to 85% rise time	CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_D2P, CSI_D2N, CSI_D3P, CSI_D3N, CSI_CLKP, CSI_CLKN			25	ns
t_{FLP}	Fall time LP(1)	15% to 85% fall time				25	ns
t_{REOT}	Rise time post-EoT(1)	30%-85% rise time				35	ns
$t_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock(1)	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state		40			ns
		All other pulses		20			ns
$t_{LP-PER-TX}$	Period of the LP exclusive-OR clock			90			ns
DV/DtSR	Slew rate(1)	C_{LOAD} = 0 pF				500	mV/ns
		C_{LOAD} = 5 pF				300	mV/ns
		C_{LOAD} = 20 pF				250	mV/ns
		C_{LOAD} = 70 pF				150	mV/ns
		C_{LOAD} = 0 to 70 pF (falling edge only), data rate ≤ 1.5 Gbps		30			mV/ns
		C_{LOAD} = 0 to 70 pF (falling edge only), data rate ≤ 1.5 Gbps		30			mV/ns
		C_{LOAD} = 0 to 70 pF (falling edge only), data rate > 1.5 Gbps		25			mV/ns
		C_{LOAD} = 0 to 70 pF (falling edge only), data rate > 1.5 Gbps		25			mV/ns
		C_{LOAD} = 0 to 70 pF (falling edge only)(2) (3)		30 - 0.075× (VO,INST - 700)			mV/ns
		C_{LOAD} = 0 to 70 pF (falling edge only)(4) (5)		25 - 0.0625× (VO,INST - 550)			mV/ns
C_{LOAD}	Load capacitance(1)			0		70	pF

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Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
DATA-CLOCK TIMING (Figure 6-6, Figure 6-7)							
UI_{INST}	UI instantaneous	In 1, 2, 3, or 4 lane configuration Data rate = 368 Mbps to 1.664 Gbps	CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_D2P, CSI_D2N, CSI_D3P, CSI_D3N, CSI_CLKP, CSI_CLKN	0.6		2.7	ns
ΔUI	UI variation	UI ≥ 1 ns Figure 6-5		-10%		10%	UI
		UI < 1 ns Figure 6-5		-5%		5%	UI
$t_{SKEW(TX)}$	Data to clock skew (measured at transmitter) Skew between clock and data from ideal center	Data rate ≤ 1 Gbps Figure 6-5		-0.15		0.15	UI_{INST}
		1 Gbps ≤ Data rate ≤ 1.5 Gbps Figure 6-5		-0.2		0.2	UI_{INST}
$t_{SKEW(TX)}$ static	Static data to clock skew	Data rate > 1.5 Gbps		-0.2		0.2	UI_{INST}
$t_{SKEW(TX)}$ dynamic	Dynamic data to clock skew			-0.15		0.15	UI_{INST}
ISI	Channel ISI					0.2	UI_{INST}
GLOBAL TIMING (Figure 6-6, Figure 6-7)							
$t_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX		CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_D2P, CSI_D2N, CSI_D3P, CSI_D3N, CSI_CLKP, CSI_CLKN	60			ns
$t_{CLK-POST}$	HS exit			60 + 52×UI_{INST}			ns
$t_{CLK-PRE}$	Time HS clock shall be driver prior to any associated Data Lane beginning the transition from LP to HS mode			8			UI_{INST}
$t_{CLK-PREPARE}$	Clock Lane HS Entry			38		95	ns
$t_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions			95		300	ns
$t_{CLK-TERM-EN}$	Time-out at Clock Lane Display Module to enable HS Termination			Time for Dn to reach VTERM-EN		38	ns
$t_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst			60			ns
$t_{CLK-PREPARE}$ + $t_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock			300			ns

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Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$t_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination		CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_D2P, CSI_D2N, CSI_D3P, CSI_D3N, CSI_CLKP, CSI_CLKN	Time for Dn to reach V-TERM-EN		35 + 4×UI INST	ns
t_{EOT}	Transmitted time interval from the start of $t_{HS-TRAIL}$ to the start of the LP-11 state following a HS burst					105 + 12×UI INST	ns
$t_{HS-EXIT}$	Time that the transmitter drives LP=11 following a HS burst			100			ns
$t_{HS-PREPARE}$	Data Lane HS Entry			40 + 4×UI INST		85 + 6×UI INST	ns
$t_{HS-PREPARE}$ + $t_{HS-ZERO}$	$t_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence			145 + 10×UI INST			ns
$t_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $t_{HS-SETTLE}$			85 + 6×UI INST		145 + 10×UI INST	ns
$t_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.			40		55 + 4×UI INST	ns
$t_{HS-TRAIL}$	Data Lane HS Exit		CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_D2P, CSI_D2N, CSI_D3P, CSI_D3N, CSI_CLKP, CSI_CLKN	60 + 4×UI INST			ns
t_{LPX}	Transmitted length of LP state			50			ns
t_{WAKEUP}	Recovery Time from Ultra Low Power State (ULPS)			1			ms
t_{INIT}	Initialization period		CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_D2P, CSI_D2N, CSI_D3P, CSI_D3N, CSI_CLKP, CSI_CLKN	100			µs

(1) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2 ns delay.
(2) When the output voltage is between 700 mV and 930 mV
(3) Applicable when the supported data rate ≤ 1.5 Gbps
(4) When the output voltage is between 550 mV and 790 mV
(5) Applicable when the supported data rate > 1.5 Gbps.

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6.8 Recommended Timing for the Serial Control Bus

Over I^2C supply and temperature ranges unless otherwise specified.

			MIN	TYP	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard-mode	>0		100	kHz
		Fast-mode	>0		400	kHz
		Fast-mode Plus	>0		1	MHz
t_{LOW}	SCL Low Period	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
t_{HIGH}	SCL High Period	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{SU;STA}$	Set up time for a start or a repeated start condition	Standard-mode	4.7			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{HD;DAT}$	Data hold time	Standard-mode	0			µs
		Fast-mode	0			µs
		Fast-mode Plus	0			µs
$t_{SU;DAT}$	Data set up time	Standard-mode	250			ns
		Fast -mode	100			ns
		Fast-mode Plus	50			ns
$t_{SU;STO}$	Set up time for STOP condition	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
t_{BUF}	Bus free time between STOP and START	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
t_r	SCL & SDA rise time	Standard-mode			1000	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
t_f	SCL & SDA fall time	Standard-mode			300	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
C_b	Capacitive load for each bus line	Standard-mode			400	pF
		Fast-mode			400	pF
		Fast-mode Plus			550	pF
$t_{VD:DAT}$	Data valid time	Standard-mode			3.45	µs
		Fast-mode			0.9	µs
		Fast-mode Plus			0.45	µs
$t_{VD;ACK}$	Data vallid acknowledge time	Standard-mode			3.45	µs
		Fast-mode			0.9	µs
		Fast-mode Plus			0.45	µs

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Over I^2C supply and temperature ranges unless otherwise specified.

			MIN	TYP	MAX	UNIT
t_{SP}	Input filter	Fast-mode			50	ns
		Fast-mode Plus			50	ns

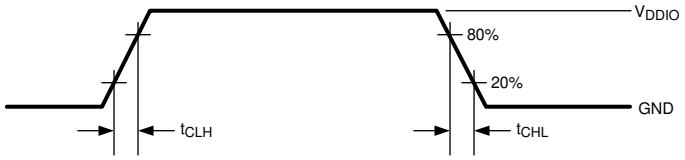

Figure 6-1. LVCMOS Transition Times

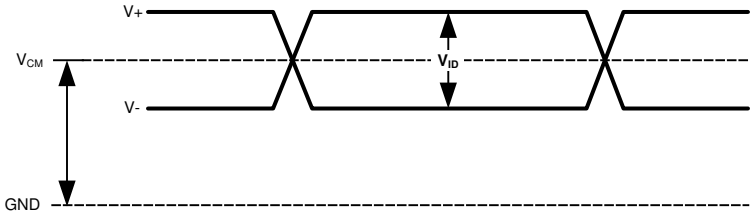

Figure 6-2. FPD-Link Receiver VID

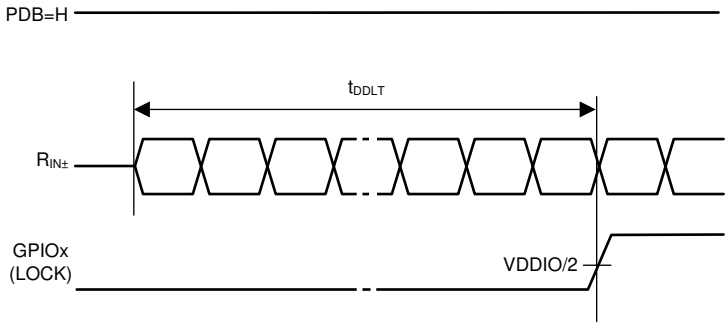

Figure 6-3. Deserializer Data Lock Time

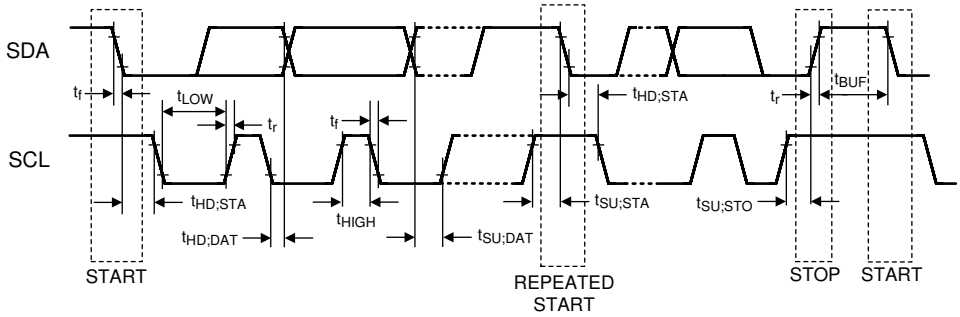

Figure 6-4. I2C Serial Control Bus Timing

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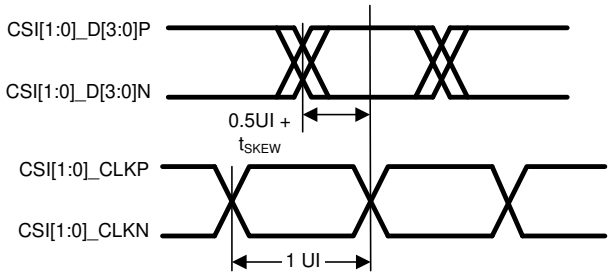

Figure 6-5. Clock and Data Timing in HS Transmission

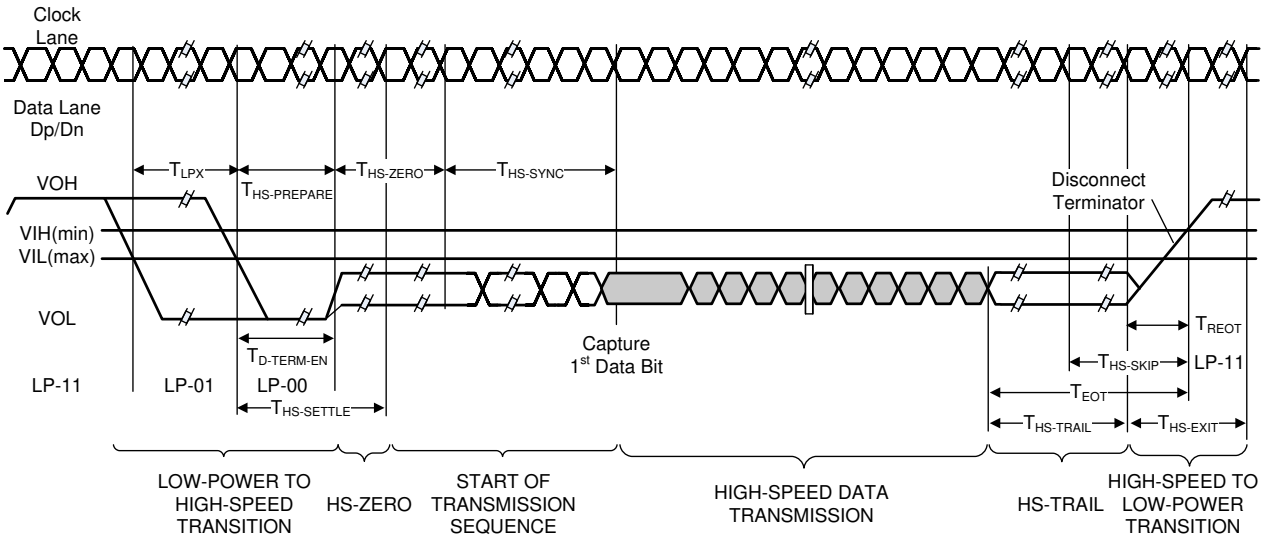

Figure 6-6. High Speed Data Transmission Burst

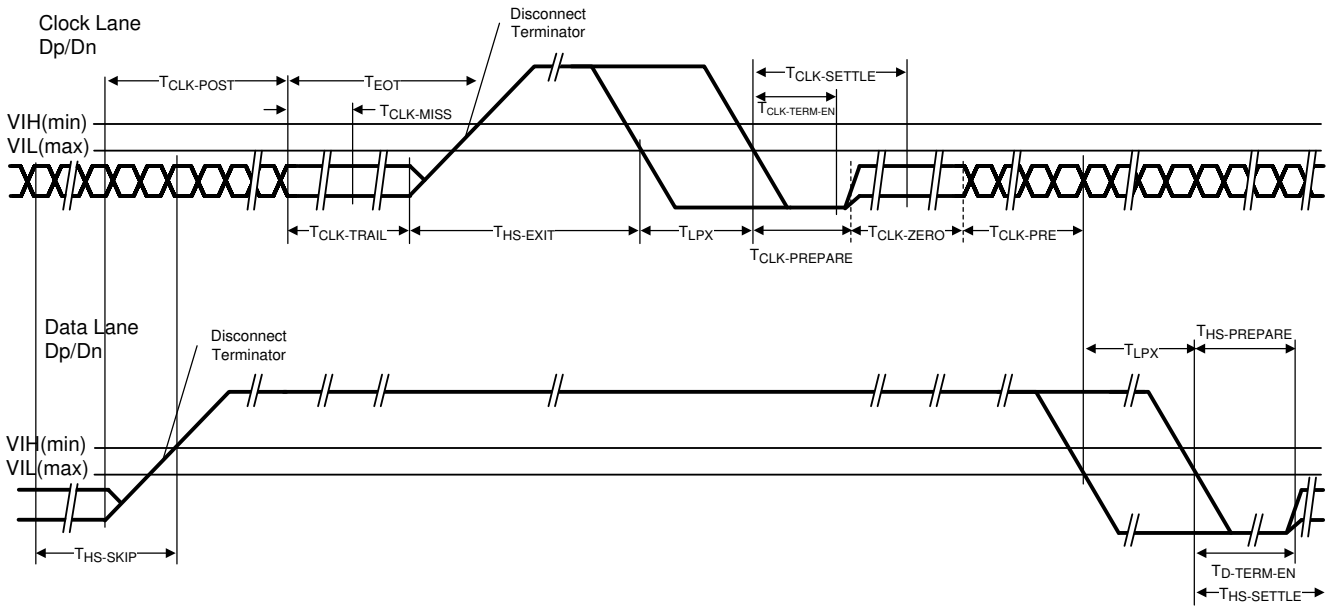

Figure 6-7. Switching the Clock Lane between Clock Transmission and Low-Power Mode

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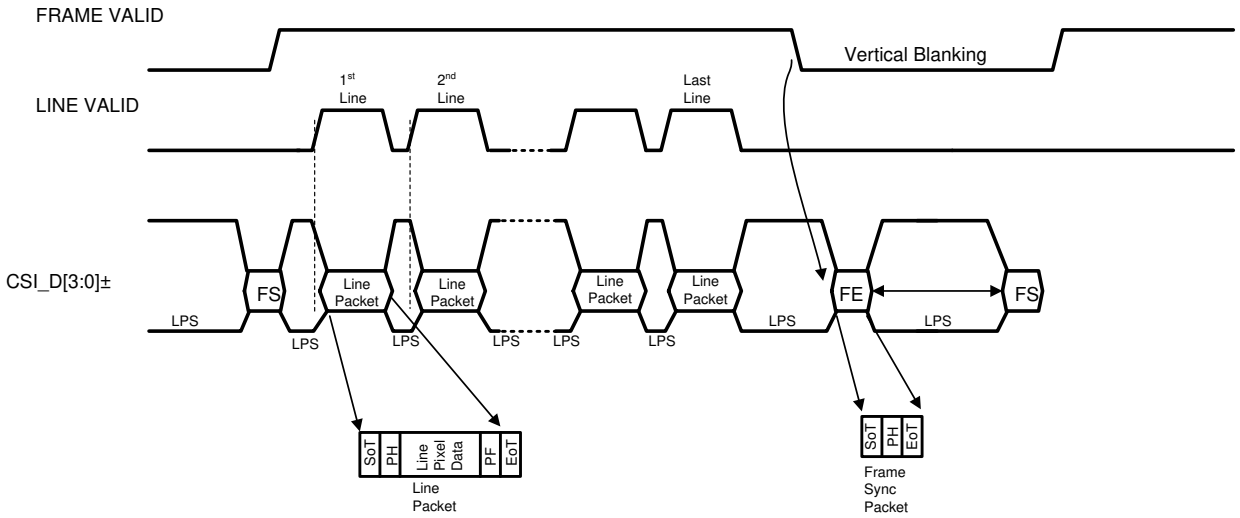

Figure 6-8. Long Line Packets and Short Frame Sync Packets

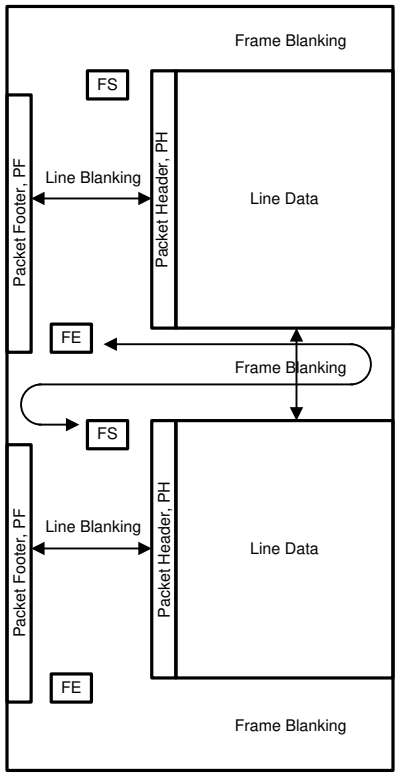

Figure 6-9. CSI-2 General Frame Format (Single Rx / VC)

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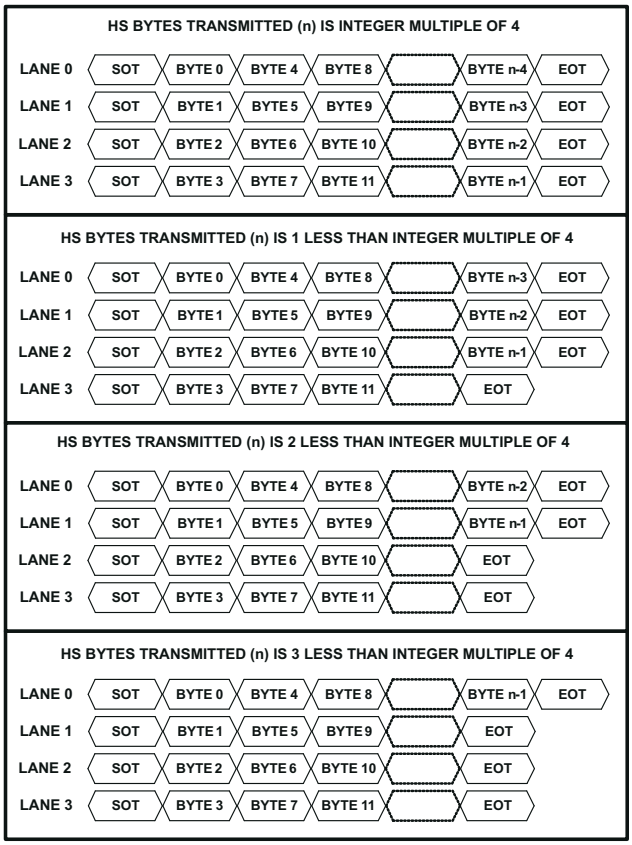
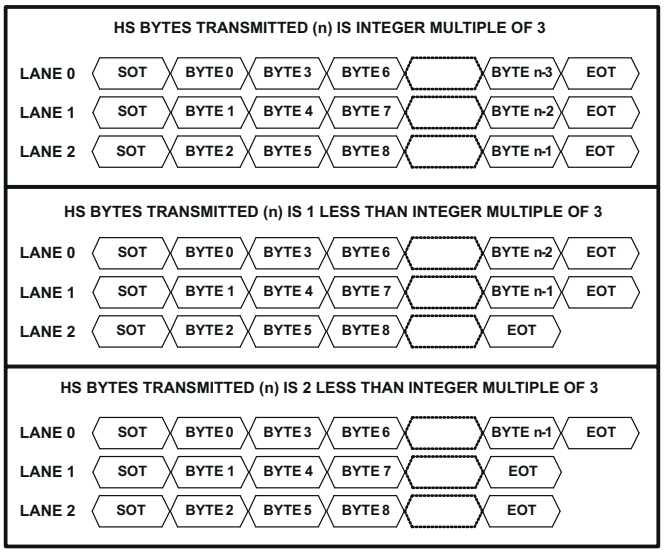
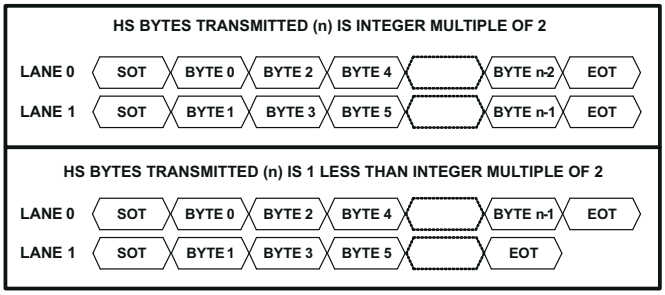


4 CSI-2 Data Lane Configuration (default)



3 CSI-2 Data Lane Configuration



2 CSI-2 Data Lane Configuration

Figure 6-10. 4 MIPI Data Lane Configuration

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6.9 Typical Characteristics

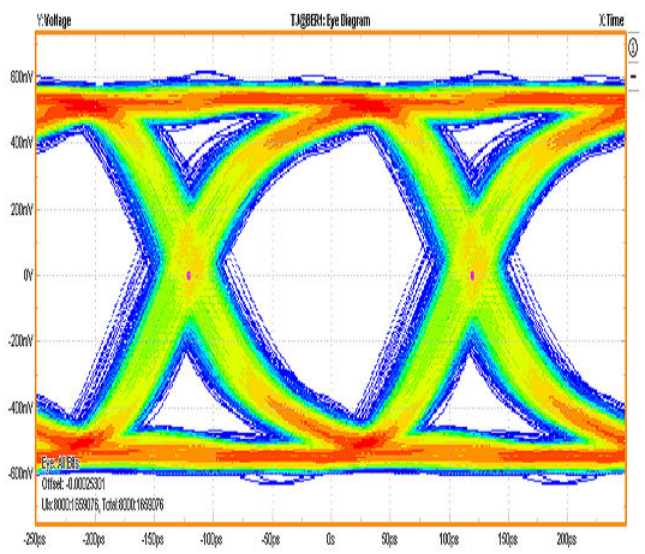

Figure 6-11. Typical 4 Gbps Forward Channel Monitor Loop Through Waveform (CMLOUT)

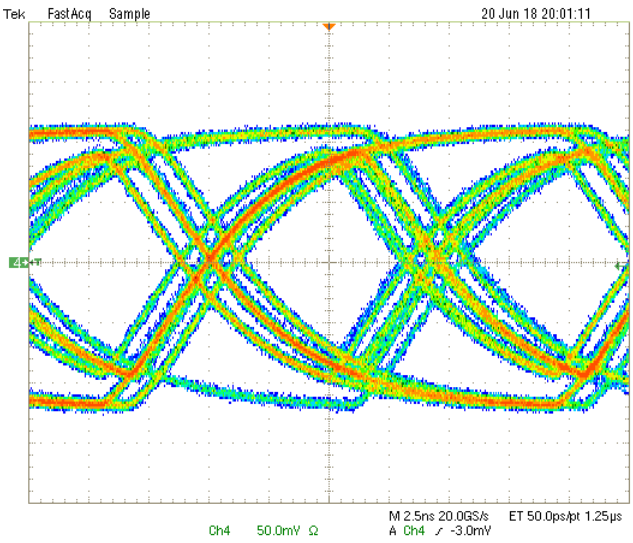

Figure 6-12. Typical 50 Mbps Back Channel Output Waveform

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7 Detailed Description

7.1 Overview

The DS90UB662-Q1 is a sensor hub that accepts four sensor inputs from a FPD-Link III interface. When coupled with ADAS FPD-Link III serializers (DS90UB633A-Q1 and DS90UB63x CSI-2 Serializers), the device combines data streams from multiple sensor sources onto one CSI-2 port with up to four data lanes .

7.1.1 Functional Description

The DS90UB662-Q1 is a sensor hub that aggregates up to four inputs acquired from a FPD-Link III stream and transmitted over a MIPI sensor serial interface (CSI-2). When coupled with the DS90UB633A-Q1 or DS90UB63x CSI-2 FPD-Link III serializer, the DS90UB662-Q1 receives data streams from multiple imagers that can be multiplexed on the same CSI-2 link. The DS90UB662-Q1 supplies a single MIPI CSI-2 port, configured with four lanes with up to 1.6 Gbps per lane. The DS90UB662-Q1 can support multiple data formats (programmable as RAW, YUV, RGB) and different sensor resolutions. The CSI-2 Tx module accommodates both image data and non-image data (including synchronization or embedded data packets).

The DS90UB662-Q1 CSI-2 interface combines each of the sensor data streams into packets designated for each virtual channel. The output generated is composed of virtual channels to separate different streams to be interleaved. Each virtual channel is identified by a unique channel identification number in the packet header.

When the DS90UB662-Q1 is paired with a DS90UB63x CSI-2 Serializer serializer, the received FPD-Link III forward channel is constructed in 40-bit long frames. Each encoded frame contains video payload data, I2C forward channel data, and additional information on framing, data integrity and link diagnostics. The high-speed, serial bit stream from the DS90UB633A-Q1 contains an embedded clock and DC-balancing to allow sufficient data line transitions for enhanced signal quality. When paired with ADAS serializers in RAW input mode, the received FPD-Link III forward channel is similarly constructed at a lower line rate in 28-bit long frames.The DS90UB662-Q1 device recovers a high-speed, FPD-Link III forward channel signal and generates a bidirectional control channel control signal in the reverse channel direction. The DS90UB662-Q1 converts the FPD-Link III stream into a MIPI CSI-2 output interface designed to support automotive sensors, including 1MP/60fps image sensors.

The DS90UB662-Q1 device has four receive input ports to accept up to four sensor streams simultaneously. The control channel function of the DS90UB633A-Q1 / DS90UB662-Q1 pair supplies bidirectional communication between the image sensors and ECU. The integrated bidirectional control channel transfers data bidirectionally over the same differential pair used for video data interface. This interface has advantages over other chipsets because the interface eliminates the need for additional wires for programming and control. The bidirectional control channel bus is controlled through an I2C port. The bidirectional control channel supplies continuous low latency communication and is not dependent on video blanking intervals.

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7.2 Functional Block Diagram

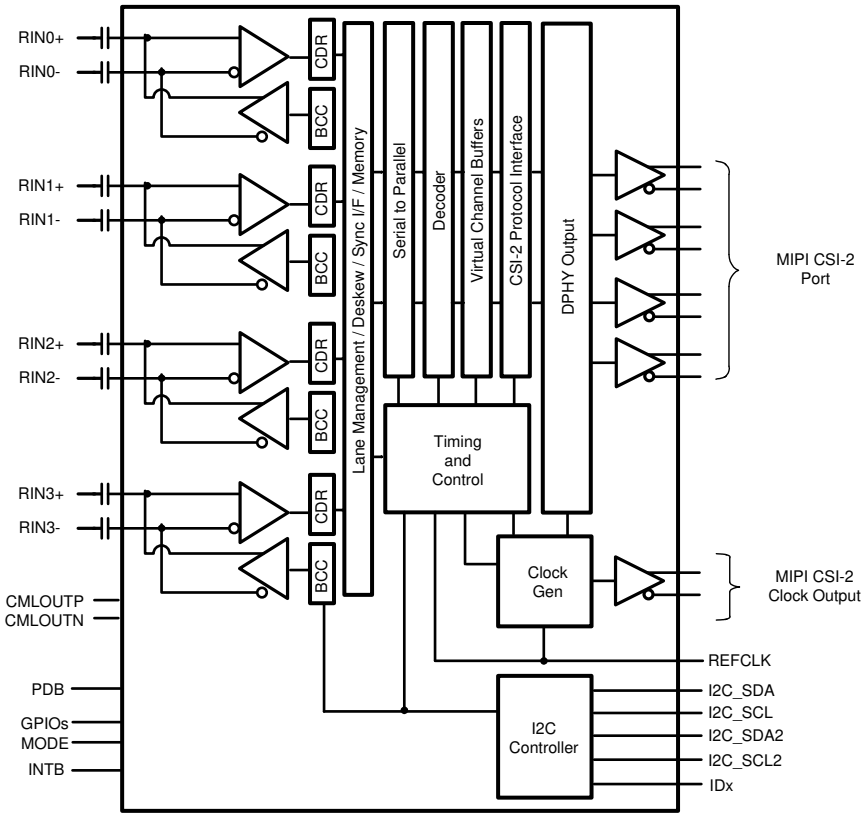

Figure 7-1. Functional Block Diagram

7.3 Feature Description

The DS90UB662-Q1 provides a 4:1 hub for sensor applications. The device includes four FPD-Link III inputs for sensor data streams from up to four DS90UB63x CSI-2 Serializer. The interfaces are also backward-compatible to DS90UB633A-Q1 serializer. Data received from the four input ports is aggregated onto one 4-lane CSI-2 interface.

7.4 Device Functional Modes

The DS90UB662-Q1 supports one main operating mode:

- CSI-2 Mode (DS90UB63x CSI-2 Serializers compatible)
- RAW Mode (DS90UB633A-Q1 compatible)

The mode controls the FPD-Link III receiver operation, in this case, the output format for the device is CSI-2 through one CSI-2 transmit port.

The DS90UB662-Q1 includes forwarding control to allow multiple video streams from any of the received ports to be mapped to the CSI-2 port.

7.4.1 CSI-2 Mode

When operating in CSI-2 Mode, the DS90UB662-Q1 receives CSI-2 formatted data on up to four FPD-Link III input ports and forwards the data to one or two CSI-2 transmit ports. The deserializer can operate in CSI-2 mode with synchronous back channel reference or non-synchronous mode. The forward channel line rate is independent of the CSI-2 rate in synchronous or non-synchronous with external clock mode. The mode supports the remapping of Virtual Channel IDs at the input of each receive port. This remapping allows the receivers to handle conflicting VC-IDs for input streams from multiple sensors and to send those streams to the same CSI-2 transmit port.

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In CSI-2 mode each deserializer Rx Port can support an FPD-Link III line rate up to 4.16 Gbps, where the line (or forward channel) and back channel rates are based on the reference frequency used for the serializer:

- In Synchronous mode based on REFCLK input frequency reference, the FPD-Link III forward channel rate is a fixed value of 160 × REFCLK. FPD3_PCLK = 4 × REFCLK and back channel rate = 2 × REFCLK. For example with REFCLK = 25 MHz, forward channel data rate = 4.0 Gbps, FPD3_PCLK = 100 MHz, back channel data rate = 50 Mbps.
- In Non-synchronous clocking mode when the DS90UB63x CSI-2 Serializers uses external reference clock (CLK_IN) the FPD-Link line rate is typically CLK_IN × 80, FPD3_PCLK = 2 × CLK_IN or 1 x CLK_IN. The back channel data rate must be set to 10 Mbps in this mode. For example, with CLK_IN = 50 MHz, forward channel rate = 4 Gbps, FPD3_PCLK = 100 MHz, and the back channel rate is 10 Mbps. The sensor CSI-2 rate is independent of the CLK_IN.

7.4.2 RAW Mode

In RAW mode, the DS90UB662-Q1 receives RAW8, RAW10, or RAW12 data from a DS90UB633A-Q1 serializer. The data is translated into a RAW8, RAW10, or RAW12 CSI-2 video stream for forwarding on one of the CSI-2 transmit ports. For each input port, the CSI-2 packet header VC-ID and Data Type are programmable.

In RAW mode, each Rx Port can support up to:

- 12 bits of DATA + 2 SYNC bits for an input PCLK range of 37.5 MHz to 100 MHz (75 MHz for DS90UB633A-Q1) in the 12-bit, high-frequency mode. Line rate = PCLK × (2/3) × 28. For example, PCLK = 100 MHz, line rate = (100 MHz) × (2/3) × 28 = 1.87 Gbps. Note: No HS/VS restrictions (raw). NOTE: The back channel rate must be set to 2.5 Mbps in this mode.
- 12 bits of DATA + 2 bits SYNC for an input PCLK range of 25 MHz to 50 MHz in the 12-bit, low-frequency mode. Line rate = PCLK × 28. For example, PCLK = 50 MHz, line rate = 50 MHz × 28 = 1.40 Gbps. Note: No HS/VS restrictions (raw). The back channel rate must be set to 2.5 Mbps in this mode.
- 10 bits of DATA + 2 SYNC bits for an input PCLK range of 50 MHz to 100 MHz in the 10-bit mode. Line rate = (PCLK / 2) × 28. For example, PCLK = 100 MHz, line rate = (100 MHz / 2) × 28 = 1.40 Gbps. Note: HS/HV is restricted to no more than one transition per 10 PCLK cycles. The back channel rate must be set to 2.5 Mbps in this mode.

7.4.3 MODE Pin

Configuration of the device may be done through the MODE input strap pin, or through the configuration register bits. A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the MODE input (V_{MODE}) and V_{DD18} to select one of the four six possible modes. Possible configurations are:

- CSI-2 Mode (DS90UB63x CSI-2 Serializer compatible)
  - 40-bit forward channel frame
  - 50-Mbps back channel rate for serializer operation in Synchronous mode (default)
  - 10-Mbps back channel rate for serializer operation in Non-synchronous mode (must be programmed by setting BC_FREQ_SELECT register 0x58[2:0] = 010))
- 12-bit LF / 12-bit HF / 10-bit RAW modes (DS90UB633A-Q1 compatible)
  - 28-bit forward channel frame
  - 2.5-Mbps back channel rate (default)

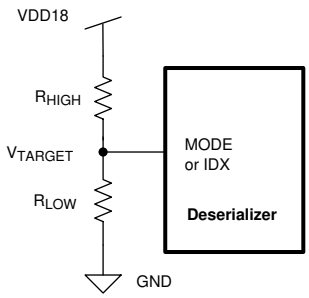

Figure 7-2. Strap Pin Connection Diagram

Table 7-1. Strap Configuration Mode Select

NO.	V_{MODE} VOLTAGE RANGE			V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		RX MODE
	V_{MIN}	V_{TYP}	V_{MAX}	VDD18 = 1.80 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	
0	0	0	0.131 × $V_{(VDD18)}$	0	OPEN	10.0	CSI-2 Mode
1	0.179 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.374	88.7	23.2	RAW12 LF
2	0.296 × $V_{(VDD18)}$	0.330 × $V_{(VDD18)}$	0.362 × $V_{(VDD18)}$	0.582	75.0	35.7	RAW12 HF
3	0.412 × $V_{(VDD18)}$	0.443 × $V_{(VDD18)}$	0.474 × $V_{(VDD18)}$	0.792	71.5	56.2	RAW10
4	0.525 × $V_{(VDD18)}$	0.559 × $V_{(VDD18)}$	0.592 × $V_{(VDD18)}$	0.995	78.7	97.6	CSI-2 Mode
5	0.642 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.704 × $V_{(VDD18)}$	1.202	39.2	78.7	RAW12 LF
6	0.761 × $V_{(VDD18)}$	0.792 × $V_{(VDD18)}$	0.823 × $V_{(VDD18)}$	1.420	25.5	95.3	RAW12 HF
7	0.876 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	RAW10

The strapped values can be viewed and/or modified in the following locations:

- RX Mode – Port Configuration FPD3_MODE Register 0x6D[1:0] bits (see Table 7-123)

7.4.4 REFCLK

A valid 23-MHz to 26-MHz reference clock is required on the REFCLK pin 5 for precise frequency operation. The REFCLK frequency defines all internal clock timers, including the back channel rate, I2C timers, CSI-2 datarate, FrameSync signal parameters, and other timing critical internal circuitry. REFCLK input must be continuous. If the REFCLK input does not detect a transition more than 20 µs, this may cause a disruption in the CSI-2 output. REFCLK should be applied to the DS90UB662-Q1 only when the supply rails are above minimum levels (see Figure 9-1). At start-up, the DS90UB662-Q1 defaults to an internal oscillator to generate an backup internal reference clock at nominal frequency of 25 MHz ±10%.

As an option for mitigating EMI / EMC, the DS90UB662-Q1 is capable of tolerating a REFCLK with spread-spectrum clocking (SSC) profile with up to ±0.5% amplitude deviations (center spread) or up to 1% amplitude deviations (down spread) and up to 33-kHz frequency modulation from a clock source.

The REFCLK LVCMOS input oscillator specifications are listed in Table 7-2.

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Table 7-2. REFCLK Oscillator Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE CLOCK					
Frequency tolerance with aging	–40°C ≤ T_A ≤ 105°C, aging, no spread-spectrum			±100	ppm
Amplitude		800	1200	$V_{(VDDIO)}$	mVp-p
Symmetry	Duty Cycle	40%	50%	60%	
Rise and fall time	10% – 90%			6	ns
Jitter	200 kHz – 10 MHz		50	200	ps p-p
Frequency		23	25	26	MHz
Spread-spectrum clock modulation percentage (Optional)	Center spread	-0.5%		+0.5%	
	Down spread	-1%		0%	
Spread-spectrum clock modulation frequency (Optional)				33	kHz

7.4.5 Receiver Port Control

The DS90UB662-Q1 can support up to four simultaneous inputs to Rx ports 0 - 4. The Receiver port control register RX_PORT_CTL 0x0C (see Table 7-30) allows for disabling any Rx inputs when not in use. These bits can only be written by a local I2C master at the deserializer side of the FPD-Link.

Each FPD-Link III Receive port has a unique set of registers that provides control and status corresponding to Rx ports 0 - 4. Control of the FPD-Link III port registers is assigned by the FPD3_PORT_SEL register, which sets the page controls for reading or writing individual ports unique registers. For each of the FPD-Link III Receive Ports, the FPD3_PORT_SEL 0x4C register defaults to selecting that port's registers as detailed in register description (see Table 7-90).

As an alternative to paging to access FPD-Link III Receive unique port registers, separate I2C addresses may be enabled to allow direct access to the port-specific registers. The Port I2C address registers 0xF8 - 0xFB allow programming a separate 7-bit I2C address to allow access to unique, port-specific registers without paging (see Section 7.6.17. I2C commands to these assigned I2C addresses are also allowed access to all shared registers.

7.4.5.1 Video Stream Forwarding

Video stream forwarding is handled by the Rx Port forwarding control in register 0x20 (see Table 7-50). Forwarding from input ports are disabled by default and must be enabled using per-port controls. Different options for forwarding CSI-2 packets can also be selected as described starting in *Section 7.4.25*.

7.4.6 Input Jitter Tolerance

Input jitter tolerance is the ability of the clock and data recovery (CDR) and phase-locked loop (PLL) of the receiver to track and recover the incoming serial data stream. Jitter tolerance at a specific frequency is the maximum jitter permissible before data errors occur. Figure 7-3 shows the allowable total jitter of the receiver inputs and must be less than the values in Table 7-3.

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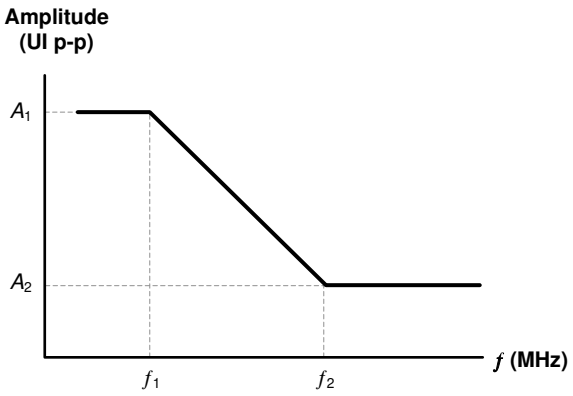

Figure 7-3. Input Jitter Tolerance Plot

Table 7-3. Input Jitter Tolerance Limit

INTERFACE	JITTER AMPLITUDE (UI p-p)		FREQUENCY (MHz) (1)	
FPD3	A1	A2	*f*1	*f*2
	1	0.4	FPD3_PCLK / 80	FPD3_PCLK / 15

(1) FPD3_PCLK frequency is a function of the PCLK, CLK_IN, or REFCLK frequency and dependent on the serializer operating MODE:CSI-2 synchronous mode: FPD3_PCLK = 4 x REFCLKCSI-2 non-synchronous mode: FPD3_PCLK = 2 x CLK_IN
RAW 10-bit mode: FPD3_PCLK = PCLK / 2
RAW 12-bit HF mode: FPD3_PCLK = 2 x PCLK / 3
RAW 12-bit LF mode: FPD3_PCLK = PCLK

7.4.7 Adaptive Equalizer

The receiver inputs provide an adaptive equalization filter to compensate for signal degradation from the interconnect components. To determine the maximum cable reach, factors that affect signal integrity such as jitter, skew, ISI, crosstalk, and so forth, must be considered. The equalization status and configuration are selected through AEQ registers 0xD2–0xD5 (see Table 7-181 through Table 7-184).

Each RX receiver incorporates an adaptive equalizer (AEQ), which continuously monitors cable characteristics for long-term cable aging and temperature changes. The AEQ attempts to optimize the equalization setting of the RX receiver.

If the deserializer loses LOCK, the adaptive equalizer will reset and perform the LOCK algorithm again to reacquire the serial data stream being sent by the serializer.

7.4.7.1 Transmission Distance

The DS90UB662-Q1 AEQ can compensate for the transmission channel insertion loss of up to –19.2 dB at 2.1 GHz. When designing the transmission channel, consider the total insertion loss of all components in the signal path between a serializer and a deserializer. Typically, the transmission channel would consist of a serializer PCB, two or more connectors, one or more cables, and a deserializer PCB as shown in Figure 7-4.

Figure 7-4. Typical Transmission Channel Components With Coaxial Cables

Assuming –1.2 dB at 2.1-GHz insertion loss (IL) budget for each serializer and deserializer PCB and 0.1 dB for each connector, it is easy to determine maximum cable reach given the insertion loss characteristic of the cable. For example, Dacar 462 has typical insertion loss of about –1.31 dB/m at 2.1 GHz. With the –19.2-dB total IL budget, the remaining IL budget for the cable is –16.6 dB (–19.2 dB – 2 × (–1.2 dB) – 2 × (–0.1 dB)) after

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insertion loss of the two PCBs and two connectors are deducted from the total channel IL budget. Given this IL cable budget, the maximum cable reach with a single Dacar 462 is greater than 12 m (–16.6 dB / –1.31 dB/m).

Lower loss cables such as Dacar 302 (typical insertion loss of –0.78 dB/m at 2.1 GHz) may be used alone or in combination with Dacar 462 to achieve even longer transmission distances as exemplified in Figure 7-4. Table 7-4 shows typical Dacar 462 and Dacar 302 cable combinations that achieve a 15-m transmission distance and stay within the maximum insertion loss budget.

Table 7-4. Typical 15-m Cable Combinations with Dacar 462 and Dacar 302 Cables

EXAMPLE	PCB INSERTION LOSS AT 2.1 GHz	CONNECTOR INSERTION LOSS AT 2.1 GHz	DACAR 462 INSERTION LOSS AT 2.1 GHz	DACAR 302 INSERTION LOSS AT 2.1 GHz	TOTAL CHANNEL INSERTION LOSS AT 2.1 GHz
A	2 × (–1.2) dB	4 × (–0.1) dB	2 × 2.5 m × (–1.31) dB/m	10 m × (–0.78) dB/m	–14.75 dB
B	2 × (–1.2) dB	4 × (–0.1) dB	2 × 3 m × (–1.31) dB/m	9 m × (–0.78) dB/m	–15.28 dB
C	2 × (–1.2) dB	4 × (–0.1) dB	2 × 4 m × (–1.31) dB/m	7 m × (–0.78) dB/m	–16.87 dB

7.4.7.2 Adaptive Equalizer Algorithm

The AEQ process steps through the allowed equalizer control values to find a value that allows the Clock Data Recovery (CDR) circuit to keep a valid lock condition. The circuit waits for a programmed re-lock time period for each EQ setting, then the circuit checks the results for a valid lock. If a valid lock is detected, the circuit will stop at the current EQ setting and maintain a constant value as long as the lock state persists. If the deserializer loses the lock, the adaptive equalizer will resume the LOCK algorithm and the EQ setting is incremented to the next valid state. When the lock is lost, the circuit will search the EQ settings to find another valid setting to reacquire the serial data stream sent by the serializer that remains locked.

7.4.7.3 AEQ Settings

7.4.7.3.1 AEQ Start-Up and Initialization

The AEQ circuit can be restarted at any time by setting the AEQ_RESTART bit in the AEQ_CTL2 register 0xD2 (see Table 7-181). When the deserializer is powered on, the AEQ is continually searching through the EQ settings and could be at any setting when the serializer supplies a signal. If the Rx Port CDR locks to the signal, it may be acceptable for low bit errors, but it may not optimized or overequalized. When connected to a compatible serializer (DS90UB633A-Q1 or DS90UB63x CSI-2 Serializer), the DS90UB662-Q1 will restart the AEQ adaption by default after the device achieves the first positive lock indication to supply a more consistent start-up from known conditions.

With this feature disabled, the AEQ may lock at a relatively random EQ setting based on when the FPD-Link III input signal is initially present. Alternatively, AEQ_RESTART or DIGITAL_RESET0 can be applied once the compatible serializer input signal frequency is stable to restart adaption from the minimum EQ gain value. These techniques allow for a more consistent initial EQ setting following adaption.

7.4.7.3.2 AEQ Range

The AEQ circuit can be programmed with minimum and maximum settings used during the EQ adaption. Using the full AEQ range provides the most flexible solution, if the channel conditions are known however, an improved deserializer lock time can be achieved by narrowing the search window for allowable EQ gain settings. For example, in a system use case with a longer cable and multiple interconnects creating higher channel attenuation, the AEQ would not adapt to the minimum EQ gain settings. Likewise, in a system use case with a short cable and low channel attenuation, the AEQ would not generally adapt to the highest EQ gain settings. The AEQ range is determined by the AEQ_MIN_MAX register 0xD5 (see Table 7-184) where AEQ_MAX sets the maximum value of EQ gain. The ADAPTIVE_EQ_FLOOR_VALUE determines the starting value for EQ gain adaption. To enable the minimum AEQ limit, the SET_AEQ_FLOOR bit in the AEQ_CTL2 register 0xD2[2] must also be set (see Table 7-181). An AEQ range (AEQ_MAX - AEQ_FLOOR) to allow a variation around the nominal setting of –2/+4 or ±3 around the nominal AEQ value specific to Rx port channel characteristics gives a

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good trade-off in lock time and adaptability. The setting for the AEQ after adaption can be read back from the AEQ_STATUS register 0xD3 (see Table 7-182). The suggested AEQ_FLOOR settings are given in Table 7-5.

Table 7-5. Suggested ADAPTIVE_EQ_FLOOR_VALUE as a Function of Channel Insertion Loss

CHANNEL INSERTION LOSS AT 2.1 GHz (dB)	ADAPTIVE_EQ_FLOOR_VALUE
Up to –9.4	0
–9.4 to –13.2	2
–13.2 to –15.4	4
–15.4 to –17.8	5
–17.8 to –19.2	6

7.4.7.3.3 AEQ Timing

The dwell time for AEQ to wait for lock or error-free status is also programmable. When checking each EQ setting the AEQ will wait for a time interval, controlled by the ADAPTIVE_EQ_RELOCK_TIME field in the AEQ_CTL2 register (see Table 7-181) before incrementing to the next allowable EQ gain setting. The default wait time is set to 2.62 ms based on REFCLK = 25 MHz. When the maximum setting is reached and there is no lock acquired during the programmed relock time, the AEQ will restart adaption at minimum setting or AEQ_FLOOR value.

7.4.7.3.4 AEQ Threshold

The DS90UB662-Q1 receiver will adapt by default based on the FPD-Link error checking during the Adaptive Equalization process. The specific errors linked to equalizer adaption, FPD-Link III clock recovery error, packet encoding error, and parity error can be individually selected in AEQ_CTL register 0x42 (see Table 7-80). Errors are accumulated over 1/2 of the period of the timer set by the ADAPTIVE_EQ_RELOCK_TIME. If the number of errors is greater than the programmed threshold (AEQ_ERR_THOLD), the AEQ will attempt to increase the EQ setting.

7.4.8 Channel Monitor Loop-Through Output Driver

The DS90UB662-Q1 includes an internal **C**hannel **M**onitor **L**oop-through output on the CMLOUTP/N pins. The CMLOUTP/N supplies a buffered loop-through output driver to observe the jitter after equalization for each of the four RX receiver channels. The CMLOUT monitors the post EQ stage, thus providing the recovered input of the deserializer signal. The measured serial data width on the CMLOUT loop-through is the total jitter including the internal driver, AEQ, back channel echo, and so forth. Each channel also has its own CMLOUT monitor and can be used for debug purposes. This CMLOUT is useful in identifying gross signal conditioning issues.

Table 7-6 shows the minimum CMLOUT differential eye opening as a measure of acceptable forward channel signal integrity. A CMLOUT eye opening of at least 0.35 UI suggests that the forward channel signal integrity is likely acceptable. However, further testing such as BIST is recommended to verify error-free operation. An eye opening of less than 0.35 UI indicates possible issues with the forward channel signal integrity.

Table 7-6. CML Monitor Output Driver

PARAMETER		TEST CONDITIONS	PIN	MIN	TYP	MAX	UNIT
E_W	Differential Output Eye Opening	R_L = 100 Ω (Figure 7-5)	CMLOUTP, CMLOUTN	0.35			UI(1)

(1) Unit Interval (UI) is equivalent to one ideal serialized data bit width. The UI scales with serializer input PCLK frequency (RAW Modes), serializer CLK_IN frequency (CSI-2 Mode, Serializer Non-synchronous Mode) or REFCLK (CSI-2 Mode, Serializer Synchronous Mode).CSI-2 Mode, Serializer Synchronous Mode: 1 UI = 1 / (160 x REFCLK) (typ) CSI-2 Mode, Serializer Non-synchronous Mode: 1 UI = 1 / (80 x CLK_IN) (typ)
RAW 10-bit mode: 1 UI = 1 / (28 x PCLK / 2)
RAW 12-bit HF mode: 1 UI = 1 / (28 x 2/3 x PCLK)
RAW 12-bit LF mode: 1 UI = 1 / (28 x PCLK)

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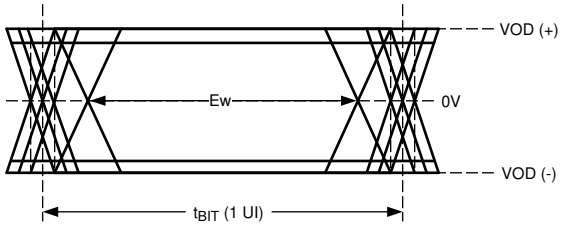

Figure 7-5. CMLOUT Output Driver

Table 7-7 includes details on selecting the corresponding RX receiver of CMLOUTP/N configuration.

Table 7-7. Channel Monitor Loop-Through Output Configuration

	FPD3 RX Port 0	FPD3 RX Port 1	FPD3 RX Port 2	FPD3 RX Port 3
ENABLE MAIN LOOPTHRU DRIVER	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80
SELECT CHANNEL MUX	0xB1 = 0x01 0xB2 = 0x01	0xB1 = 0x01 0xB2 = 0x02	0xB1 = 0x01 0xB2 = 0x04	0xB1 = 0x01 0xB2 = 0x08
SELECT RX PORT	0xB0 = 0x04 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02	0xB0 = 0x08 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02	0xB0 = 0x0C 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02	0xB0 = 0x10 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02

7.4.8.1 Code Example for CMLOUT FPD3 RX Port 0:

```
WriteI2C(0xB0,0x14)    # FPD3 RX Shared, page 0
WriteI2C(0xB1,0x00)    # Offset 0 (reg_0_sh)
WriteI2C(0xB2,0x80)    # Enable loop throu driver
WriteI2C(0xB1,0x01)    # Select Drive Mux
WriteI2C(0xB2,0x01)    #
WriteI2C(0xB0,0x04)    # FPD3 RX Port 0, page 0
WriteI2C(0xB1,0x0F)    #
WriteI2C(0xB2,0x01)    # Loop through select
WriteI2C(0xB1,0x10)    #
WriteI2C(0xB2,0x02)    # Enable CML data output
```

7.4.9 RX Port Status

The DS90UB662-Q1 is able to monitor and detect several other RX port specific conditions and interrupt states. This information is latched into the RX port status registers RX_PORT_STS1 0x4D (see Table 7-91) and RX_PORT_STS2 0x4E (see Table 7-92). There are bits to flag any change in LOCK status (LOCK_STS_CHG) or detect any errors in the control channel over the forward link (BCC_CRC_ERROR, BCC_SEQ_ERROR) which are cleared upon read. The Rx Port status registers also allow monitoring of the presence stable input signal along with monitoring parity and CRC errors, line length, and lines per video frame.

7.4.9.1 RX Parity Status

The FPD-Link III receiver checks the decoded data parity to detect any errors in the received FPD-Link III frame. Parity errors are counted up and accessible through the RX_PAR_ERR_HI and RX_PAR_ERR_LO registers 0x55 and 0x56 (see Table 7-99 and Table 7-100) to provide combined 16-bit error counter. In addition, a parity error flag can be set once a programmed number of parity errors have been detected. This condition is indicated by the PARITY_ERROR flag in the RX_PORT_STS1 register. Reading the counter value will clear the counter value and PARITY_ERROR flag. An interrupt may also be generated based on assertion of the parity error flag. By default, the parity error counter will be cleared and flag will be cleared on loss of Receiver lock. To ensure an exact read of the parity error counter, parity checking should be disabled in the GENERAL_CFG register 0x02 (see Table 7-20) before reading the counter.

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7.4.9.2 FPD-Link Decoder Status

The FPD-Link III receiver also checks the decoded data for encoding or sequence errors in the received FPD-Link III frame. If either of these error conditions are detected the FPD3_ENC_ERROR bit will be latched in the RX_PORT_STS2 register 0x4E[5] (see Table 7-92). An interrupt may also be generated based on assertion of the encoded error flag. To detect FPD-Link III Encoder errors, the LINK_ERROR_COUNT must be enabled with a LINK_ERR_THRESH value greater than 1. Otherwise, the loss of Receiver Lock will prevent detection of the Encoder error. The FPD3_ENC_ERROR flag is cleared on read.

When partnered with a DS90UB633A-Q1 the FPD3 Encoder may be configured to include a CRC check of the FPD3 encoder sequence. The CRC check provides an extra layer of error checking on the encoder sequence. This CRC checking adds protection to the encoder sequence used to send link information comprised of Datapath Control registers 0x59 (Table 7-103) and 0x5A (Table 7-104), Sensor Status registers 0x51 - 0x54 (Table 7-95 through Table 7-98), and Serializer ID register 0x5B (Table 7-106). TI recommends that designers enable CRC error checking on the FPD3 Encoder sequence to prevent any updates of link information values from encoded packets that do not pass CRC check. The FPD3 Encoder CRC is enabled by setting the FPD3_ENC_CRC_DIS register 0xBA[7] to 0 (see Table 7-172). In addition, the FPD3_ENC_CRC_CAP flag should be set in register 0x4A[4] (see Table 7-88).

7.4.9.3 RX Port Input Signal Detection

The DS90UB662-Q1 can detect and measure the approximate input frequency and frequency stability of each RX input port and indicate status in bits [2:1] of RX_PORT_STS2 (see Table 7-92). Frequency measurement stable FREQ_STABLE indicates the FPD-Link III input clock frequency is stable. When no FPD-Link III input clock is detected at the RX input port, the NO_FPD3_CLK bit indicates that condition has occurred. The setting of these error flags is dependent on the stability control settings in the FREQ_DET_CTL register 0x77 (see Table 7-133). The NO_FPD3_CLK bit will be set if the input frequency is below the setting programmed in the FREQ_LO_THR setting in the FREQ_DET_CTL register. A change in frequency FREQ_STABLE = 0, is defined as any change in MHz greater than the value programmed in the FREQ_HYST value. The frequency is continually monitored and provided for readback through the I2C interface less than every 1 ms. A 16-bit value is used to provide the frequency in registers 0x4F and 0x50 (see Table 7-93 and Table 7-94). An interrupt can also be generated for any of the ports to indicate if a change in frequency is detected on any port.

7.4.9.4 Line Counter

For each video frame received, the deserializer will count the number of video lines in the frame. In CSI-2 input mode, any long packet will be counted as a video line. In RAW mode, any assertion of the Line Valid (LV) signal will be interpreted as a video line. The LINE_COUNT_1 and LINE_COUNT_0 registers (Table 7-129 and Table 7-130) can be used to read the line count for the most recent video frame. Line Length may not be consistent when receiving multiple CSI-2 video streams differentiated by VC-ID. An interrupt may be enabled based on a change in the LINE_COUNT value. If interrupts are enabled, the LINE_COUNT registers will be latched at the interrupt and held until read back by the processor through the I2C.

7.4.9.5 Line Length

For each video line, the length (in bytes) will be determined. The LINE_LEN_1 and LINE_LEN_0 registers (Table 7-131 and Table 7-132) can be used to read the line count for the most recent video frame. If the line length is not stable throughout the frame, the length of the last line of the frame will be reported. Line Count may not be consistent when receiving multiple CSI-2 video streams differentiated by VC-ID. An interrupt may be enabled based on a change in the LINE_LEN value. If interrupts are enabled, the LINE_LEN registers will be latched at the interrupt and held until read by the processor through the I2C.

7.4.10 Sensor Status

When paired with the DS90UB633A-Q1 serializer, the DS90UB662-Q1 is capable of receiving diagnostic indicators from the serializer. The sensor alarm and status diagnostic information are reported in the SENSOR_STS_X registers (Table 7-95 through Table 7-98). The interrupt capability from detected status changes in sensor are described in *Section 7.5.9.4*. This interrupt condition will be cleared by reading the SEN_INT_RISE_STS and SEN_INT_FALL_STS registers (Table 7-193 and Table 7-194).

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7.4.11 GPIO Support

The DS90UB662-Q1 supports 8 pins which are programmable for use in multiple options through the GPIOx_PIN_CTL registers.

7.4.11.1 GPIO Input Control and Status

Upon initialization GPIO0 through GPIO7 are enabled as inputs by default. Each GPIO pin has an input disable and a pulldown disable control bit with exception of the open-drain GPIO3 pin. By default, the GPIO pin input paths are enabled and the internal pulldown circuit for the GPIO is enabled. The GPIO_INPUT_CTL (Table 7-33) and GPIO_PD_CTL (Table 7-176) registers allow control of the input enable and the pulldown, respectively. For example to disable GPIO1 and GPIO2 as inputs you would program in register 0x0F[2:1] = 11. For most applications, there is no need to modify the default register settings for the pull down resistors. The status HIGH or LOW of each GPIO pin 0 through 7 may be read through the GPIO_PIN_STS register 0x0E (Table 7-32). This register read operation provides the status of the GPIO pin independent of whether the GPIO pin is configured as an input or output.

7.4.11.2 GPIO Output Pin Control

Individual GPIO output pin control is programmable through the GPIOx_PIN_CTL registers 0x10 to 0x17 (Table 7-34 through Table 7-41). To enable any of the GPIO as output, set bit 0 = 1 in the respective register 0x10 to 0x17 after clearing the corresponding input enable bit in register 0x0F.

7.4.11.3 Forward Channel GPIO

The DS90UB662-Q1 8 GPIO pins can output data received from the forward channel when paired with a DS90UB63x CSI-2 Serializer . The remote Serializer GPIO are mapped to GPIO. Each GPIO pin can be programmed for output mode and mapped. Up to four GPIOs are supported in the forward direction on each FPD-Link III Receive port. Each forward channel GPIO (from any port) can be mapped to any GPIO output pin. The DS90UB633A-Q1 GPIO's cannot be configured as inputs for remote communication over the forward channel to the DS90UB662-Q1.

The timing for the forward channel GPIO is dependant on the number of GPIOs assigned at the serializer. When a single GPIO input from the DS90UB63x CSI-2 Serializer is linked to a DS90UB662-Q1 deserializer GPIO output the value is sampled every forward channel transmit frame. Two linked GPIO are sampled every two forward channel frames and 3-linked or 4-linked GPIOs are sampled every 5 frames. The minimum latency for the GPIO remains consistent (approximately 225 ns), but as the information spreads over multiple frames, the jitter typically increases on the order of the sampling period (number of forward channel frames). TI recommends maintaining a 4x oversampling ratio for linked GPIO throughput. For example, when operating in 4-Gbps synchronous mode with REFCLK = 25 MHz, the maximum recommended GPIO input frequency based on the number of GPIO linked over the forward channel is shown in Table 7-8. When operating in 2.0 Gbps forward channel frequency, the maximum forward channel GPIO frequency will be half of the rate as compared to 4.0 Gbps operation.

Table 7-8. Forward Channel GPIO Typical Timing

NUMBER OF LINKED FORWARD CHANNEL GPIOs (FC_GPIO_EN)	SAMPLING FREQUENCY (MHz) AT FPD-Link III LINE RATE = 4 Gbps	MAXIMUM RECOMMENDED FORWARD CHANNEL GPIO FREQUENCY (MHz)	TYPICAL JITTER (ns)
1	100	25	12
2	50	12.5	24
4	20	5	60

In addition to mapping remote serializer GPI, an internally generated FrameSync (see *Section 7.4.24*) or other control signals may be output from any of the deserializer GPIOs for synchronization with a local processor or another deserializer.

7.4.11.4 Back Channel GPIO

Each DS90UB662-Q1 GPIO pin defaults to input mode at start-up. The deserializer can link GPIO pin input data on up to four available slots to send on the back channel per each remote serializer connection. Any of the 8

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GPIO pin data can be mapped to send over the available back channel slots for each FPD-Link III Rx port. The same GPIO on the deserializer pin can be mapped to multiple back channel GPIO signals. For 50-Mbps back channel operation, the frame period is 600 ns (30 bits × 20 ns/bit). For 2.5-Mbps back channel operation, the frame period is 12 µs (30 bits × 400 ns/bit). As the back channel GPIOs are sampled and sent back by the DS90UB662-Q1 deserializer, the latency and jitter timing are on the order of one back channel frame. The back channel GPIO is effectively sampled at a rate of 1/30 of the back channel rate or 1.67 MHz at f_{BC} = 50 Mbps. TI recommends that the input switching frequency for the back channel GPIO is < 1/4 of the sampling rate or 416 kHz at f_{BC} = 50 Mbps. For example, when operating in 4-Gbps synchronous mode with REFCLK = 25 MHz, the maximum recommended GPIO input frequency based on the data rate when linked over the back channel is shown in Table 7-9.

Table 7-9. Back Channel GPIO Typical Timing

BACK CHANNEL RATE (Mbps)	SAMPLING FREQUENCY (kHz)	MAXIMUM RECOMMENDED BACK CHANNEL GPIO FREQUENCY (kHz)	TYPICAL LATENCY (µs)	TYPICAL JITTER (µs)
50	1670	416	1.5	0.7
10	334	83.5	3.2	3
2.5	83.5	20	12.2	12

In addition to sending GPIO from pins, an internally generated FrameSync or external FrameSync input signal may be mapped to any of the back channel GPIOs for synchronization of multiple sensors with extremely low skew (see *Section 7.4.24*).

In addition to sending GPIO from pins, an internally generated FrameSync signal may be sent on any of the back channel GPIOs.

For each port, the following GPIO control is available through the BC_GPIO_CTL0 register 0x6E and BC_GPIO_CTL1 register 0x6F.

7.4.11.5 GPIO Pin Status

GPIO pin status may be read through the GPIO_PIN_STS register 0x0E. This register provides the status of the GPIO pin independent of whether the GPIO pin is configured as an input or output.

7.4.11.6 Other GPIO Pin Controls

Each GPIO pin can has a input disable and a pulldown disable. By default, the GPIO pin input paths are enabled and the internal pulldown circuit in the GPIO is enabled. The GPIO_INPUT_CTL register 0x0F (Table 7-33) and GPIO_PD_CTL register 0xBE (Table 7-176) allow control of the input enable and the pulldown, respectively. For most applications, there is no need to modify the default register settings.

7.4.12 RAW Mode LV / FV Controls

The Raw modes provide FrameValid (FV) and LineValid (LV) controls for the video framing. The FV is equivalent to a Vertical Sync (VSYNC) while the LineValid is equivalent to a Horizontal Sync (HSYNC) input to the DS90UB633A-Q1 device.

The DS90UB662-Q1 allows setting the polarity of these signals by register programming. The FV and LV polarity are controlled on a per-port basis and can be independently set in the PORT_CONFIG2 register 0x7C (Table 7-138).

To prevent false detection of FrameValid, FV must be asserted for a minimum number of clocks prior to first video line to be considered valid. The minimum FrameValid time is programmable in the FV_MIN_TIME register 0xBC. Because the measurement is in FPD3 clocks, the minimum FrameValid setup to LineValid timing at the Serializer will vary based on operating mode.

A minimum FV to LV timing is required when processing video frames at the serializer input. If the FV to LV minimum setup is not met (by default), the first video line is discarded. Optionally, a register control (PORT_CONFIG:DISCARD_1ST_ON_ERR) forwards the first video line missing some number of pixels at the start of the line. There is no timing restrictions at the end of the frame.

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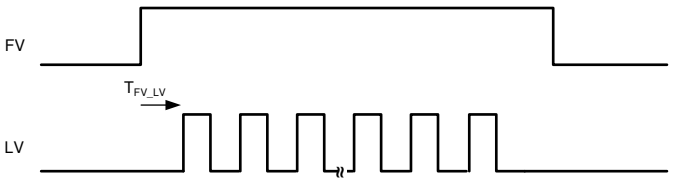

Figure 7-6. Minimum FV to LV

Table 7-10. Minimum FV to LV Setup Requirement (in Serializer PCLKs)

MODE	FV_MIN_TIME Conversion Factor	Absolute Min (FV_MIN_TIME = 0)	Default (FV_MIN_TIME = 128)
RAW12 LF	1	2	130
RAW12 HF	1.5	3	195
RAW10	2	5	261

For other settings of FV_MIN_TIME, use Equation 1 to determine the required FV to LV setup in Serializer PCLKs.

$$\text{Absolute Min} + (\text{FV_MIN_TIME} \times \text{Conversion factor}) \quad (1)$$

7.4.13 CSI-2 Protocol Layer

The DS90UB662-Q1 implements High-Speed mode to forward CSI-2 Low Level Protocol data. This includes features as described in the Low Level Protocol section of the MIPI CSI-2 Specification. It supports short and long packet formats.

The feature set of the protocol layer implemented by the CSI-2 TX is:

- Transport of arbitrary data (payload-independent)
- 8-bit word size
- Support for up to four interleaved virtual channels on the same link
- Special packets for frame start, frame end, line start, and line end information
- Descriptor for the type, pixel depth, and format of the Application Specific Payload data
- 16-bit Checksum Code for error detection

Figure 7-7 shows the CSI-2 protocol layer with short and long packets.

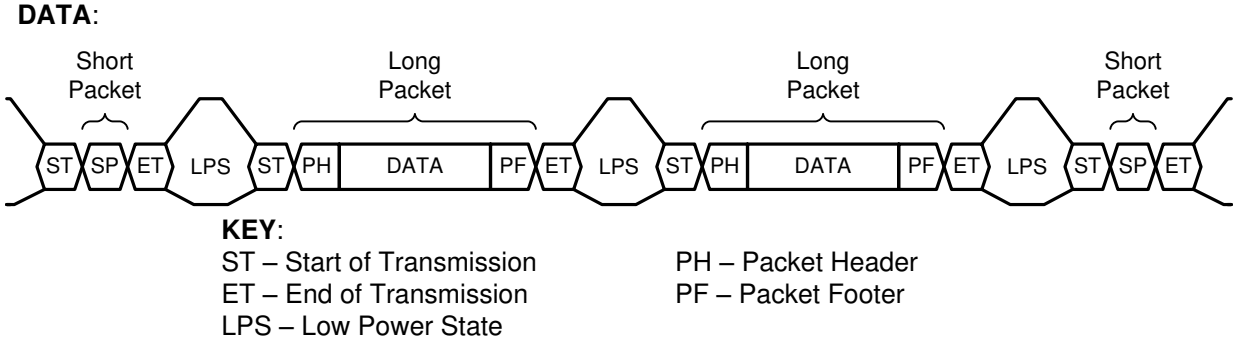

Figure 7-7. CSI-2 Protocol Layer With Short and Long Packets

7.4.14 CSI-2 Short Packet

The short packet provides frame or line synchronization. Figure 7-8 shows the structure of a short packet. A short packet is identified by data types 0x00 to 0x0F.

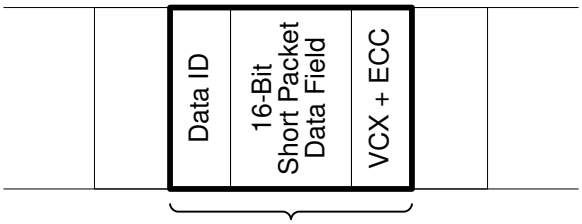

Figure 7-8. CSI-2 Short Packet Structure

7.4.15 CSI-2 Long Packet

A long packet consists of three elements: a 32-bit packet header (PH), an application-specific data payload with a variable number of 8-bit data words, and a 16-bit packet footer (PF). The packet header is further composed of three elements: an 8-bit data identifier, a 16-bit word count field, and an 8-bit ECC. The packet footer has one element, a 16-bit checksum. Figure 7-9 shows the structure of a long packet.

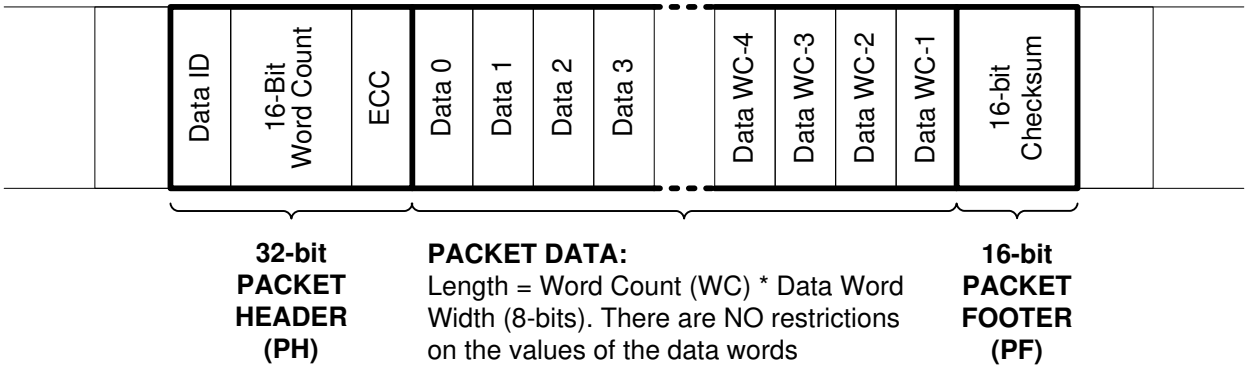

Figure 7-9. CSI-2 Long Packet Structure

Table 7-11. CSI-2 Long Packet Structure Description

PACKET PART	FIELD NAME	SIZE (BIT)	DESCRIPTION
Header	VC / Data ID	8	Contains the virtual channel identifier and the data-type information.
	Word Count	16	Number of data words in the packet data. A word is 8 bits.
	ECC	8	ECC for data ID and WC field. Allows 1-bit error recovery and 2-bit error detection.
Data	Data	WC * 8	Application-specific payload (WC words of 8 bits).
Footer	Checksum	16	16-bit cyclic redundancy check (CRC) for packet data.

7.4.16 CSI-2 Data Identifier

The DS90UB662-Q1 MIPI CSI-2 protocol interface transmits the data identifier byte containing the values for the virtual channel ID (VC) and data type (DT) for the application specific payload data, as shown in Figure 7-10. The virtual channel ID is contained in the 2 MSbs of the data identifier byte and identify the data as directed to one of four virtual channels. The value of the data type is contained in the 6 LSbs of the data identifier byte. When partnered with a DS90UB633A-Q1 serializer, the Data Type is passed through from the received CSI-2 packets. When partnered with a DS90UB633A-Q1 the received RAW mode data is converted to CSI-2 Tx packets with assigned data type and virtual channel ID.

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For each RX Port, register defines with which channel and data type the context is associated:

- For FPD Receiver port operating in RAW input mode connected to a DS90UB633A-Q1 serializer, register 0x70 describes RAW10 Mode and 0x71 RAW12 Mode.
- RAW1x_VC[7:6] field defines the associated virtual ID transported by the CSI-2 protocol from the camera sensor.
- RAW1x_ID[5:0] field defines the associated data type. The data type is a combination of the data type transported by the CSI-2 protocol.

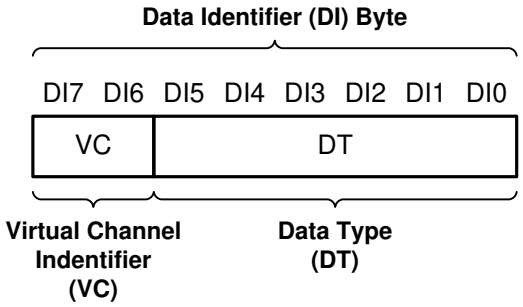

Figure 7-10. CSI-2 Data Identifier Structure

7.4.17 Virtual Channel and Context

The CSI-2 protocol layer transports virtual channels. The purpose of virtual channels is to separate different data flows interleaved in the same data stream. Each virtual channel is identified by a unique channel identification number in the packet header. Therefore, a CSI-2 TX context can be associated with a virtual channel and a data type. Virtual channels are defined by a 2-bit field. This channel identification number is encoded in the 2-bit code.

The CSI-2 TX transmits the channel identifier number and multiplexes the interleaved data streams. The CSI-2 TX supports up to four concurrent virtual channels.

7.4.18 CSI-2 Mode Virtual Channel Mapping

The CSI-2 Mode provides per-port Virtual Channel ID mapping. For each FPD-Link III input port, separate mapping may be done for each input VC-ID to any of the four VC-ID values. The mapping is controlled by the VC_ID_MAP register. This function sends the output as a time-multiplexed CSI-2 stream, where the video sources are differentiated by the virtual channel.

7.4.18.1 Example 1

The DS90UB662-Q1 is receiving data from sensors attached to each port. Each port is sending a video stream using VC-ID of 0. The DS90UB662-Q1 can be configured to re-map the incoming VC-IDs to ensure each video stream has a unique ID. The direct implementation would map incoming VC-ID of 0 for RX Port 0, VC-ID of 1 for RX Port 1, VC-ID of 2 for RX Port 2, and VC-ID of 3 for RX Port 3.

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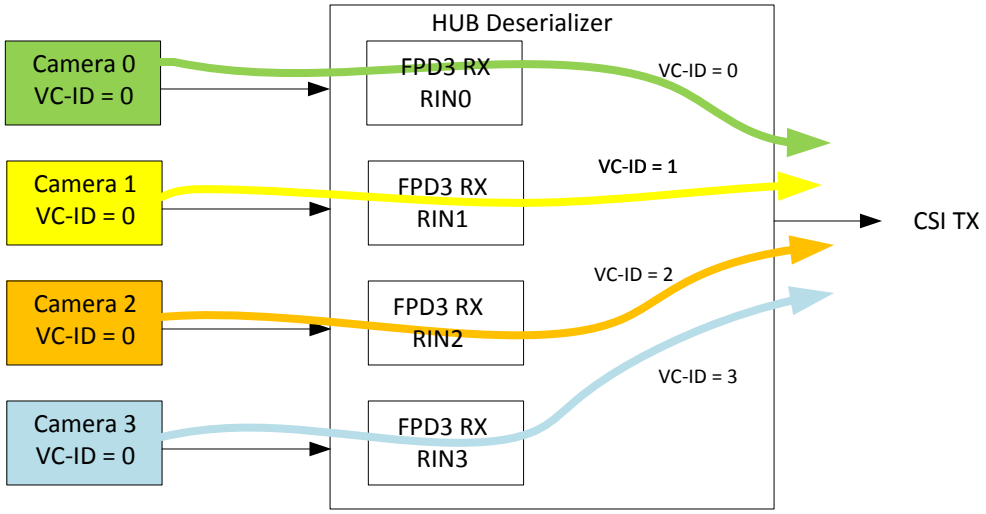

Figure 7-11. VC-ID Mapping Example 1

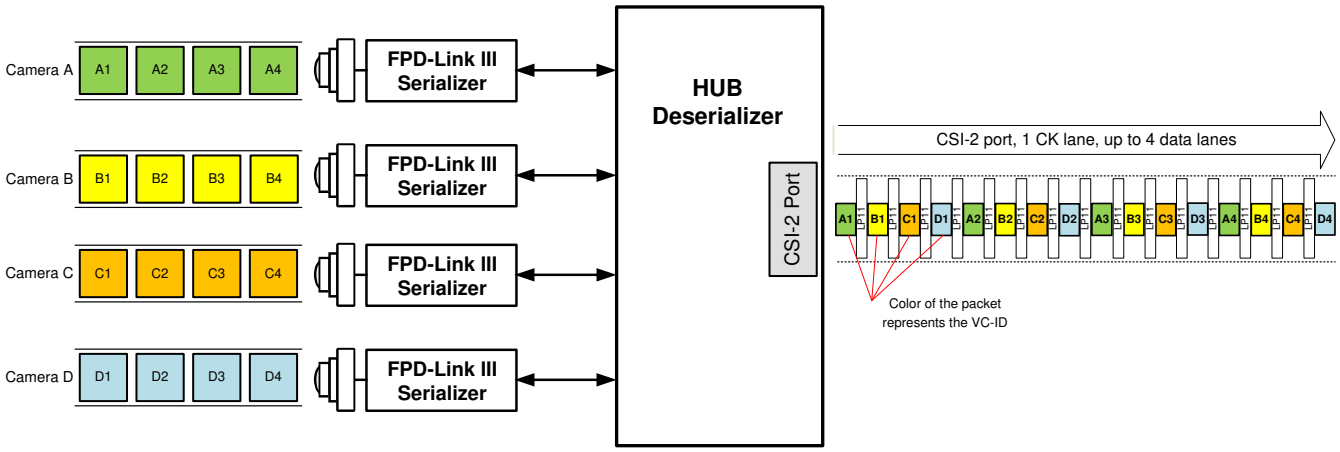

Figure 7-12. Four Sensor Data onto CSI-2 With Virtual Channels (VC-ID)

7.4.19 CSI-2 Transmitter Frequency

The CSI-2 Transmitters may operate at 400 Mbps, 800 Mbps, 1.2 Gbps (not available on prototype devices, PDS90UB662 A0 or A1) or 1.6 Gbps per data lane. This operation is controlled through the CSI_PLL_CTL 0x1F register (Table 7-49).

Table 7-12. CSI-2 Transmitter Data Rate vs CSI_PLL_CTL

CSI_PLL_CTL[1:0]	CSI-2 TX Data Rate	REFCLK Frequency
00	1.664 Gbps	26 MHz
	1.6 Gbps	25 MHz
	1.472 Gbps	23 MHz
01	1.2 Gbps	25 MHz
10	800 Mbps	25 MHz
11	400 Mbps	25 MHz

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When configuring to 800 Mbps or 1.6 Gbps, the CSI-2 timing parameters are automatically set based on the CSI_PLL_CTL 0x1F register. In the case of 400 Mbps, the respective CSI-2 timing parameters registers must be programmed, and the appropriate override bit must be set. To enable CSI-2 400 Mbps mode, set the following registers:

```
# Set CSI-2 Timing parameters
WriteI2C(0xB0,0x2)    # set auto-increment, page 0
WriteI2C(0xB1,0x40)   # CSI-2 Port 0
WriteI2C(0xB2,0x83)   # TCK Prep
WriteI2C(0xB2,0x8D)   # TCK Zero
WriteI2C(0xB2,0x87)   # TCK Trail
WriteI2C(0xB2,0x87)   # TCK Post
WriteI2C(0xB2,0x83)   # THS Prep
WriteI2C(0xB2,0x86)   # THS Zero
WriteI2C(0xB2,0x84)   # THS Trail
WriteI2C(0xB2,0x86)   # THS Exit
WriteI2C(0xB2,0x84)   # TLPX
```

```
# Set CSI-2 Timing parameters
WriteI2C(0xB0,0x2)    # set auto-increment, page 0
WriteI2C(0xB1,0x60)   # CSI-2 Port 1
WriteI2C(0xB2,0x83)   # TCK Prep
WriteI2C(0xB2,0x8D)   # TCK Zero
WriteI2C(0xB2,0x87)   # TCK Trail
WriteI2C(0xB2,0x87)   # TCK Post
WriteI2C(0xB2,0x83)   # THS Prep
WriteI2C(0xB2,0x86)   # THS Zero
WriteI2C(0xB2,0x84)   # THS Trail
WriteI2C(0xB2,0x86)   # THS Exit
WriteI2C(0xB2,0x84)   # TLPX
```

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7.4.20 CSI-2 Output Bandwidth

During normal operation, CSI-2 transmitter output bandwidth is reduced as it needs to transition between Low-Power and High-Speed modes. The minimum CSI-2 High-Speed data transmission overhead consists of T_{LPX}, $T_{HS-PREPARE}$, $T_{HS-ZERO}$, $T_{HS-SYNC}$, $T_{HS-TRAIL}$, and $T_{HS-EXIT}$ as shown in Figure 6-6. The bandwidth is further reduced when operating in Discontinuous CSI-2 Clock mode as the CSI-2 clock requires additional overhead time to transition between Low-Power and Clock Transmission modes. The minimum CSI-2 Discontinuous Clock timing overhead consists of $T_{CLK-POST}$, $T_{CLK-TRAIL}$, $T_{CLK-PREPARE}$, $T_{CLK-ZERO}$, and $T_{CLK-PRE}$ as shown in Figure 6-7. The typical CSI-2 timing overhead is given in Table 7-13.

Table 7-13. CSI-2 Transmitter Overhead vs Data Rate

CSI-2 TX Data Rate	CSI-2 TX Overhead, $t_{CSI_Overhead}$ [µs]	
	Continuos CSI-2 Clock (0x33[1]=1)	Discontinuous CSI-2 Clock (0x33[1]=0)
1.664 Gbps	0.73	1.68
1.6 Gbps	0.76	1.74
1.472 Gbps	0.83	1.89
1.2 Gbps	0.91	1.92
800 Mbps	0.93	2.06
400 Mbps	1.30	2.65

For Best-Effort Round Robin, Basic Synchronized or Line-Interleaved CSI-2 Forwarding, the maximum CSI-2 bandwidth for each CSI-2 port is defined in Equation 2.

$$BW = \frac{H_{active} \cdot N_{bits/pxl}}{\frac{H_{active} \cdot N_{bits/pxl}}{N_{CSI_Lanes} \cdot f_{CSI}} + t_{CSI_Overhead}} \quad (2)$$

For Line-Concatenated CSI-2 Forwarding, the maximum CSI-2 output bandwidth for each CSI-2 port is defined in Equation 3.

$$BW_{LC} = \frac{N_{sensor} \cdot H_{active} \cdot N_{bits/pxl}}{\frac{N_{sensor} \cdot H_{active} \cdot N_{bits/pxl}}{N_{CSI_Lanes} \cdot f_{CSI}} + t_{CSI_Overhead}} \quad (3)$$

where

- N_{sensor} is the number of sensors attached to the DS90UB662-Q1
- H_{active} is the horizontal line length of the active video frame in pixels
- $N_{bits/pxl}$ is the number of bits per pixel
- N_{CSI_Lanes} is the number of CSI-2 Lanes
- f_{CSI} is the CSI-2 TX data rate per lane in Hz
- $t_{CSI_Overhead}$ is the CSI-2 High-speed data and clock timing overhead as given in Table 7-13

NOTE: Calculations only hold if all 4 sensors have identical resolution and frame rate. Contact TI for bandwidth tools to calculate BW given a mix of inputs with different video parameters

7.4.20.1 CSI-2 Output Bandwidth Calculation Example

Assuming the following:

- Four identical sensors are attached to the DS90UB662-Q1 (N_{sensor} = 4)
- Each sensor outputs active video frame with the horizontal line length of 1080 pixels (H_{active} = 1080 pixels)
- Video format is RAW12 ($N_{bits/pxl}$ = 12 bits/pixel)
- DS90UB662-Q1 is configured to use a single CSI-2 port with all four CSI-2 lanes enabled (N_{CSI_Lanes} = 4)
- DS90UB662-Q1 CSI-2 TX is configured to operate at 800 Mbps / lane (f_{CSI} = 800 MHz)

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For Best-Effort Round Robin, Basic Synchronized or Line-Interleaved CSI-2 Forwarding, Equation 2 gives the maximum bandwidth of about 2.60 Gbps (out of 3.2 Gbps for 4 lanes) with continuous CSI-2 clock and about 2.12 Gbps without continuous CSI-2 clock.

For Line-Concatenated CSI-2 Forwarding, Equation 3 gives us the maximum bandwidth of about 3.03 Gbps (out of 3.2 Gbps for 4 lanes) with continuous CSI-2 clock and about 2.84 Gbps without continuous CSI-2 clock.

7.4.21 CSI-2 Transmitter Status

The status of the CSI-2 Transmitter may be monitored by readback of the CSI_STS register 0x35 (Table 7-71), or brought to one of the configurable GPIO pins as an output. The TX_PORT_PASS 0x35[0] indicates valid CSI-2 data being presented on CSI-2 port. If no data is being forwarded or if error conditions have been detected on the video data, the CSI-2 Pass signal will be cleared. The TX_PORT_SYNC 0x35[0] indicates the CSI-2 Tx port is able to properly synchronize input data streams from multiple sources. TX_PORT_SYNC will always return 0 if Synchronized Forwarding is disabled. Interrupts may also be generated based on changes in the CSI-2 port status.

7.4.22 Video Buffers

The DS90UB662-Q1 implements four video line buffer/FIFO, one for each RX channel. The video buffers provide storage of data payload and forward requirements for sending multiple video streams on the CSI-2 transmit ports. The total line buffer memory size is a 16-kB block for each RX port.

The CSI-2 transmitter waits for an entire packet to be available before pulling data from the video buffers.

7.4.23 CSI-2 Line Count and Line Length

The DS90UB662-Q1 counts the number of lines (long packets) to determine line count on LINE_COUNT_1/0 registers 0x73–74. For line length, DS90UB662-Q1 generates the word count field in the CSI-2 header on LINE_LEN_1/0 registers 0x75 – 0x76 (Table 7-131 and Table 7-132).

7.4.24 FrameSync Operation

A frame synchronization signal (FrameSync) can be sent through the back channel using any of the back channel GPIOs. The signal can be generated in two different methods. The first option offers sending the external FrameSync using one of the available GPIO pins on the DS90UB662-Q1 and mapping that GPIO to a back channel GPIO on one or more of the FPD-Link III ports.

The second option is to have the DS90UB662-Q1 internally generate a FrameSync signal to send through GPIO to one or more of the attached Serializers.

FrameSync signaling on the four back channels is synchronous. Thus, the FrameSync signal arrives at each of the four serializers with limited skew.

7.4.24.1 External FrameSync Control

In External FrameSync mode, an external signal is input to the DS90UB662-Q1 through one of the GPIO pins on the device. The external FrameSync signal may be propagated to one or more of the attached FPD3 Serializers through a GPIO signal in the back channel.

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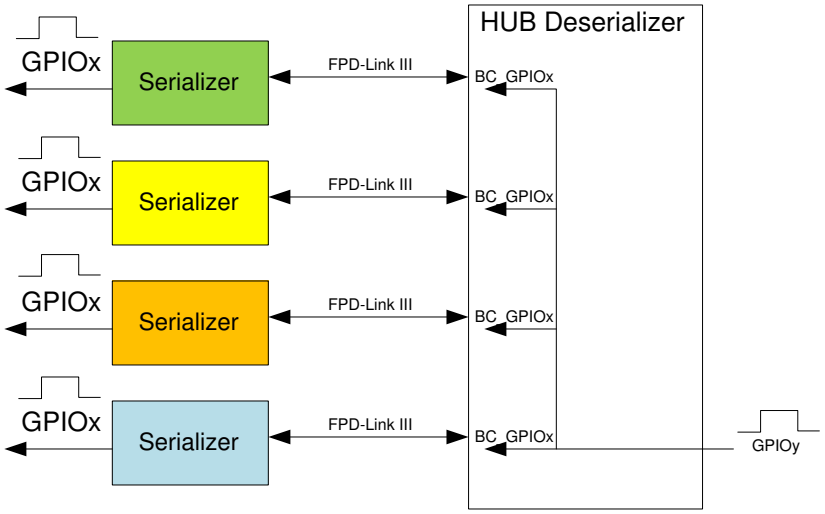

Figure 7-13. External FrameSync

Enabling the external FrameSync mode is done by setting the FS_MODE control in the FS_CTL register to a value between 0x8 (GPIO0 pin) to 0xF (GPIO7 pin). Set FS_GEN_ENABLE to 0 for this mode.

To send the FrameSync signal on the BC_GPIOx port signal, the BC_GPIO_CTL0 or BC_GPIO_CTL1 register should be programmed for that port to select the FrameSync signal.

7.4.24.2 Internally Generated FrameSync

In Internal FrameSync mode, an internally generated FrameSync signal is sent to one or more of the attached FPD3 Serializers through a GPIO signal in the back channel.

FrameSync operation is controlled by the FS_CTL, FS_HIGH_TIME_x, and FS_LOW_TIME_x 0x18 – 0x1C registers (Table 7-42 through Table 7-46). The resolution of the FrameSync generator clock (FS_CLK_PD) is derived from the back channel frame period (BC_FREQ_SELECT register). For 50-Mbps back-channel operation, the frame period is 600 ns (30 bits × 20 ns/bit). For each 2.5-Mbps back channel operation, the frame period is 12 µs (30 bits × 400 ns/bit).

Once enabled, the FrameSync signal is sent continuously based on the programmed conditions.

Enabling the internal FrameSync mode is done by setting the FS_GEN_ENABLE control in the FS_CTL register to a value of 1. The FS_MODE field controls the clock source used for the FrameSync generation. The FS_GEN_MODE field configures whether the duty cycle of the FrameSync is 50/50 or whether the high and low periods are controlled separately. The FrameSync high and low periods are controlled by the FS_HIGH_TIME and FS_LOW_TIME registers.

The accuracy of the internally generated FrameSync is directly dependent on the accuracy of the 25-MHz oscillator used as the reference clock.

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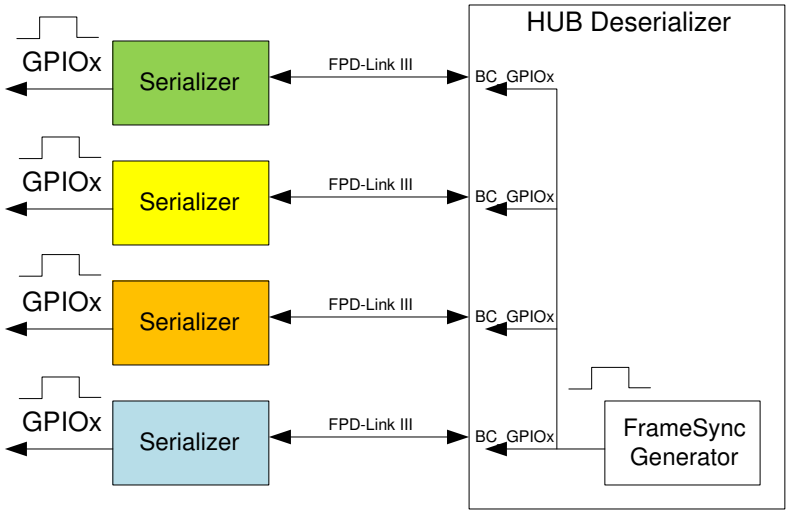
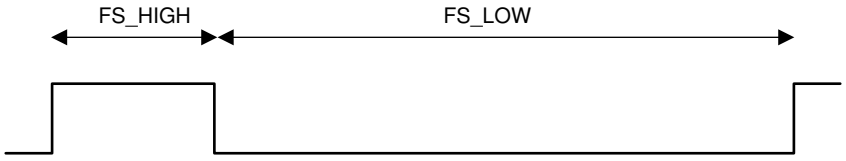


Figure 7-14. Internal FrameSync



FS_LOW = FS_LOW_TIME * FS_CLK_PD
FS_HIGH = FS_HIGH_TIME * FS_CLK_PD
where FS_CLK_PD is the resolution of the FrameSync generator clock

Figure 7-15. Internal FrameSync Signal

The following example shows generation of a FrameSync signal at 60 pulses per second. Mode settings:

- Programmable High/Low periods: FS_GEN_MODE 0x18[1]=0
- Use port 0 back channel frame period: FS_MODE 0x18[7:4]=0x0
- Back channel rate of 50 Mbps: BC_FREQ_SELECT for port 0 0x58[2:0]=110b
- Initial FS state of 0: FS_INIT_STATE 0x18[2]=0

Based on mode settings, the FrameSync is generated based upon FS_CLK_PD of 12 us.

The total period of the FrameSync is (1 sec / 60 hz) / 600 ns or approximately 27,778 counts.

For a 10% duty cycle, set the high time to 2,776 (0x0AD7) cycles, and the low time to 24,992 (0x61A0) cycles:

- FS_HIGH_TIME_1: 0x19=0x0A
- FS_HIGH_TIME_0: 0x1A=0xD7
- FS_LOW_TIME_1: 0x1B=0x61
- FS_LOW_TIME_0: 0x1C=0xA0

7.4.24.2.1 Code Example for Internally Generated FrameSync

```
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x10,0x91) # FrameSync signal; Device Status; Enabled
WriteI2C(0x58,0x5E) # BC FREQ SELECT: 50 Mbps
WriteI2C(0x19,0x0A) # FS_HIGH_TIME_1
WriteI2C(0x1A,0xD7) # FS_HIGH_TIME_0
WriteI2C(0x1B,0x61) # FS_LOW_TIME_1
```

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```
WriteI2C(0x1C,0xA0) # FS_LOW_TIME_0
WriteI2C(0x18,0x01) # Enable FrameSync
```

7.4.25 CSI-2 Forwarding

Video stream forwarding is handled by the forwarding control in the DS90UB662-Q1 on FWD_CTL1 register 0x20 (Table 7-50). The forwarding control pulls data from the video buffers for each FPD3 RX port and forwards the data to one of the CSI-2 output interfaces. It also handles generation of transitions between LP and HS modes as well as sending of Synchronization frames. The forwarding control monitors each of the video buffers for packet and data availability.

Forwarding from input ports may be disabled using per-port controls. Each of the forwarding engines may be configured to pull data from any of the four video buffers, although a buffer may only be assigned to one CSI-2 Transmitter at a time. The two forwarding engines operate independently. Video buffers are assigned to the CSI-2 Transmitters using the mapping bits in the FWD_CTL1 register 0x20[7:4].

7.4.25.1 Best-Effort Round Robin CSI-2 Forwarding

By default, the round-robin (RR) forwarding of packets use standard CSI-2 method of video stream determination. No special ordering of CSI-2 packets are specified, effectively relying on the Virtual Channel Identifier (VC) and Data Type (DT) fields to distinguish video streams. Each image sensor is assigned a VC-ID to identify the source. Different data types within a virtual channel is also supported in this mode.

The forwarding engine forwards packets as they become available to the forwarding engine. In the case where multiple packets may be available to transmit, the forwarding engine typically operates in an RR fashion based on the input port from which the packets are received.

Best-effort CSI-2 RR forwarding has the following characteristics and capabilities:

- Uses Virtual Channel ID to differentiate each video stream
- Separate Frame Synchronization packets for each VC
- No synchronization requirements

This mode of operation allows input RX ports to have different video characteristics and there is no requirement that the video be synchronized between ports. The attached video processor would be required to properly decode the various video streams based on the VC and DT fields.

Best-effort forwarding is enabled by setting the CSIx_RR_FWD bits in the FWD_CTL2 register 0x21 (Table 7-51).

7.4.25.2 Synchronized CSI-2 Forwarding

In cases with multiple input sources, synchronized forwarding offers synchronization of all incoming data stored within the buffer. If packets arrive within a certain window, the forwarding control may be programmed to attempt to synchronize the video buffer data. In this mode, it attempts to send each channel synchronization packets in order (VC0, VC1, VC2, VC3) as well as sending packet data in the same order. In the following sections, Sensor 0 (S0), Sensor 1 (S1), Sensor 2 (S2), and Sensor 3 (S3) refers to the sensors connected at FPD3 RX port 0, RX port 1, RX port 2, and RX port 3, respectively. The following describe only the 4-port operation, but other possible port combinations can be applied.

The forwarding engine for each CSI-2 Transmitter can be configured independently and synchronize up to all four video sources.

Requirements:

- Video arriving at input ports should be synchronized within approximately 1 video line period
- All enabled ports should have valid, synchronized video
- Each port must have identical video parameters, including number and size of video lines, presence of synchronization packets, and so forth.

The forwarding engine attempts to send the video synchronized. If synchronization fails, the CSI-2 transmitter stops forwarding packets and attempt to restart sending synchronized video at the next FrameStart indication. Packets are discarded as long as the forwarding engine is unable to send the synchronized video.

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Status is provided to indicate when the forwarding engine is synchronized. In addition, a flag is used to indicate that synchronization has been lost (status is cleared on a read).

Three options are available for Synchronized forwarding:

- Basic Synchronized forwarding
- Line-Interleave forwarding
- Line-Concatenated forwarding

Synchronized forwarding modes are selected by setting the CSIx_SYNC_FWD controls in the FWD_CTL2 register. To enable synchronized forwarding the following order of operations is recommended:

1. Disable Best-effort forwarding by clearing the CSIx_RR_FWD bits in the FWD_CTL2 register
2. Enable forwarding per Receive port by clearing the FWD_PORTx_DIS bits in the FWD_CTL1 register
3. Enable Synchronized forwarding in the FWD_CTL2 register

7.4.25.3 Basic Synchronized CSI-2 Forwarding

During Basic Synchronized Forwarding each forwarded frame is an independent CSI-2 video frame including FrameStart (FS), video lines, and FrameEnd (FE) packets. Each forwarded stream may have a unique VC ID. If the forwarded streams do not have a unique VC-ID, the receiving process may use the frame order to differentiate the video stream packets.

The forwarding engine attempts to send the video synchronized. If synchronization fails, the CSI-2 transmitter stops forwarding packets and attempts to restart sending synchronized video at the next FS indication. Packets are discarded as long as the forwarding engine is unable to send the synchronized video.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS0 – FS1 – FS2 – FS3 – S0L1 – S1L1 – S2L1 – S3L1 – S0L2 – S1L2 – S2L2 – S3L2 – S0L3 …

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... S0LN – S1LN – S2LN – S3LN – FE0 – FE1 – FE2 – FE3

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Notes:

FSx	FrameStart for Sensor X
FEx	FrameEnd for Sensor X
SxLy	Line Y for Sensor X video frame
SxLN	Last line for Sensor X video frame

Each packet includes the virtual channel ID assigned to receive port for each sensor.

7.4.25.3.1 Code Example for Basic Synchronized CSI-2 Forwarding

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x70,0x1F) # RAW10_datatype_yuv422b10_VC0
# "*** RX1 VC=1 ***"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x70,0x5F) # RAW10_datatype_yuv422b10_VC1
# "*** RX2 VC=2 ***"
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0x70,0x9F) # RAW10_datatype_yuv422b10_VC2
# "*** RX3 VC=3 ***"
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0x70,0xDF) # RAW10_datatype_yuv422b10_VC3
#  "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI0 select
#  "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI0 4L
#  "***Basic_FWD"
WriteI2C(0x21,0x14) # Synchronized Basic_FWD
#  "***FWD_PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0
```

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x70,0x1F) # RAW10_datatype_yuv422b10_VC0
# "*** RX1 VC=1 ***"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x70,0x5F) # RAW10_datatype_yuv422b10_VC1
# "*** RX2 VC=2 ***"
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0x70,0x9F) # RAW10_datatype_yuv422b10_VC2
# "*** RX3 VC=3 ***"
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0x70,0xDF) # RAW10_datatype_yuv422b10_VC3
#  "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI-2 select
#  "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI-2 4L
#  "***Basic_FWD"
WriteI2C(0x21,0x14) # Synchronized Basic_FWD
#  "***FWD_PORT all RX to CSI"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI-2
```


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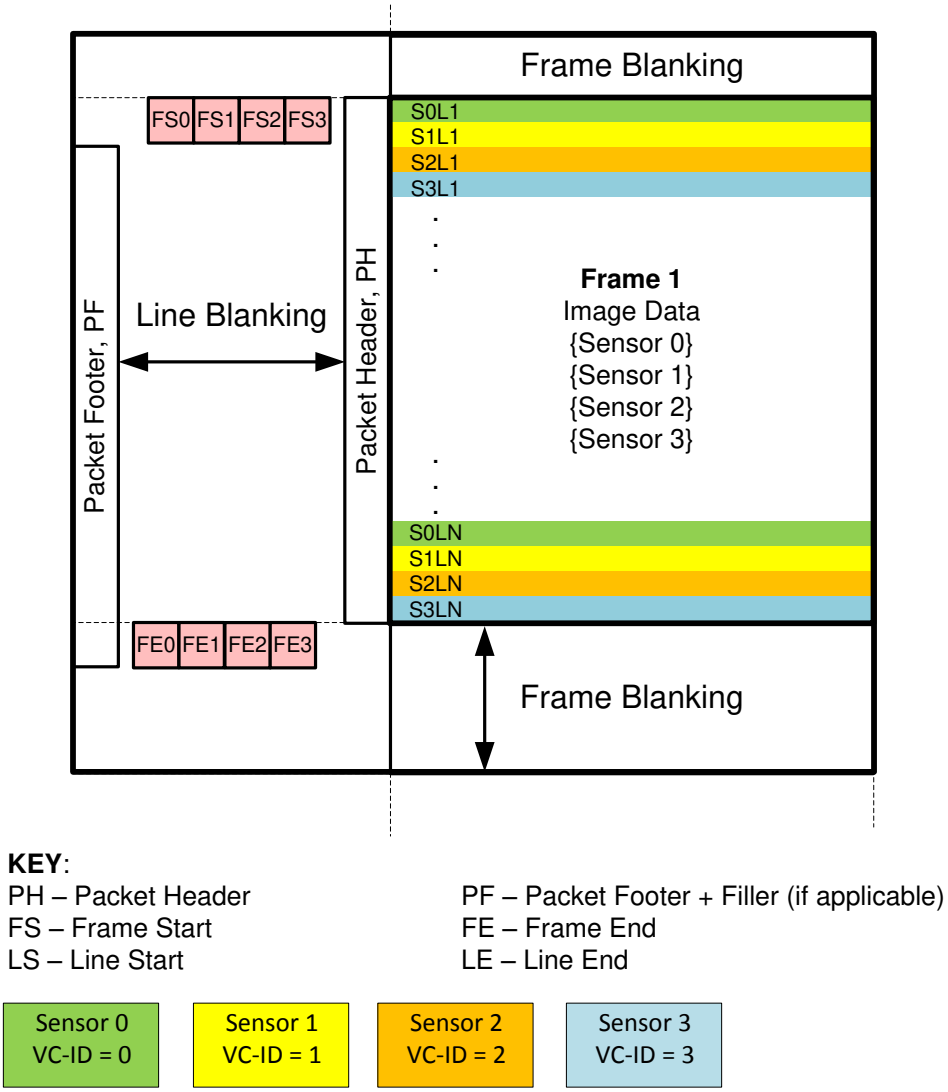

Figure 7-16. Basic Synchronized Format

7.4.25.4 Line-Interleaved CSI-2 Forwarding

In synchronized forwarding, the forwarding engine may be programmed to send only one of each synchronization packet. For example, if forwarding from all four input ports, only one FS, FE packet is sent for each video frame. The synchronization packets for the other 3 ports are dropped. The video line packets for each video stream are sent as individual packets. This effectively merges the frames from N video sources into a single frame that has N times the number of video lines.

In this mode, all video streams must also have the same VC, although this is not checked by the forwarding engine. This is useful when connected to a controller that does not support multiple VCs. The receiving processor must process the image based on order of video line reception.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS0 – S0L1 – S1L1 – S2L1 – S3L1 – S0L2 – S1L2 – S2L2 – S3L2 – S0L3 …

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... S0LN – S1LN – S2LN – S3LN – FE0

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Notes:

FSx	FrameStart for Sensor X
FEx	FrameEnd for Sensor X
SxLy	Line Y for Sensor X video frame
SxLN	Last line for Sensor X video frame

All packets would have the same VC ID.

7.4.25.4.1 Code Example for Line-Interleaved CSI-2 Forwarding

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4c,0x01) # RX0
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX1 VC=0 ***"
WriteI2C(0x4c,0x12) # RX1
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX2 VC=0 ***"
WriteI2C(0x4c,0x24) # RX2
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX3 VC=0 ***"
WriteI2C(0x4c,0x38) # RX3
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
#  "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI0 select
#  "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI0 4L
# "*** CSI0_SYNC_FWD synchronous forwarding with line interleaving ***"
WriteI2C(0x21,0x28) # synchronous forwarding with line interleaving
#  "*** FWD_PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0
```

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4c,0x01) # RX0
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX1 VC=0 ***"
WriteI2C(0x4c,0x12) # RX1
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX2 VC=0 ***"
WriteI2C(0x4c,0x24) # RX2
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX3 VC=0 ***"
WriteI2C(0x4c,0x38) # RX3
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
#  "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI-2 select
#  "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI-2 4L
# "*** CSI_SYNC_FWD synchronous forwarding with line interleaving ***"
WriteI2C(0x21,0x28) # synchronous forwarding with line interleaving
#  "*** FWD_PORT all RX to CSI"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI-2
```


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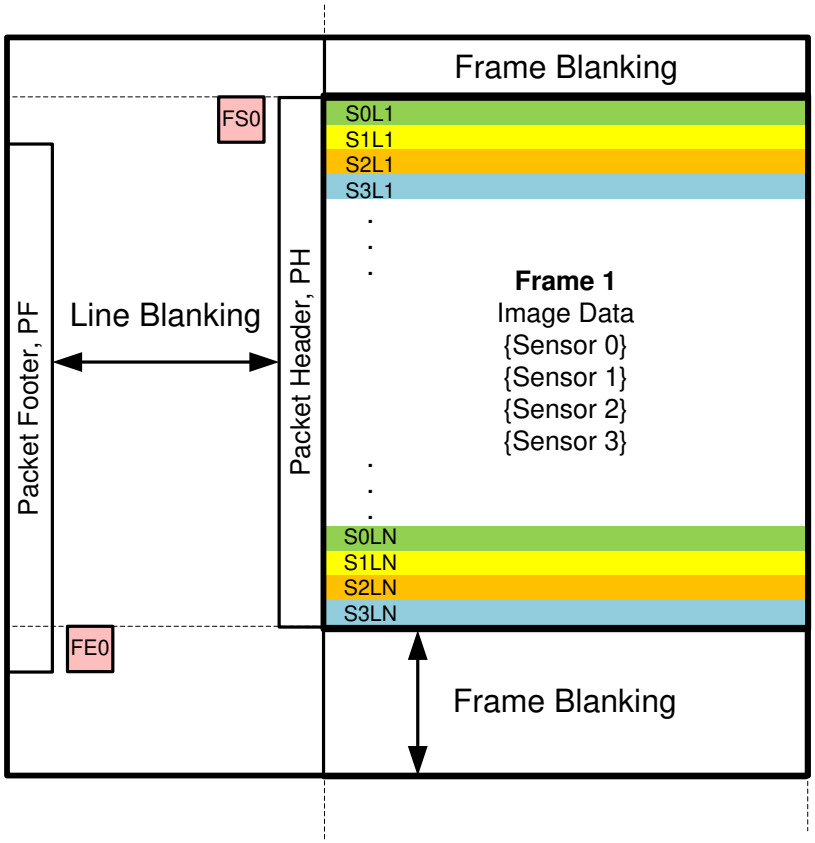

KEY:
PH – Packet Header
FS – Frame Start
LS – Line Start
PF – Packet Footer + Filler (if applicable)
FE – Frame End
LE – Line End

Sensor 0 VC-ID = 0	Sensor 1 VC-ID = 0	Sensor 2 VC-ID = 0	Sensor 3 VC-ID = 0

**Blanking intervals do not provide accurate synchronization timing*

Figure 7-17. Line-Interleave Format

7.4.25.5 Line-Concatenated CSI-2 Forwarding

In synchronized forwarding, the forwarding engine may be programmed to merge video frames from multiple sources into a single video frame by concatenating video lines. Each of the sensors for each RX carry different data streams that get concatenated into one CSI-2 stream. For example, if forwarding from all four input ports, only one FS, an FE packet is sent for each video frame. The synchronization packets for the other 3 ports are dropped. In addition, the video lines from each sensor are combined into a single line. The controller must separate the single video line into the separate components based on position within the concatenated video line.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS0 – S0L1,S1L1,S2L1,S3L1 – S0L2,S1L2,S2L2,S3L2 – S0L3,S1L3,S2L3,S3L3 …

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... S0LN,S1LN,S2LN,S3LN – FE0

Notes:

FSx FrameStart for Sensor X

FEx	FrameEnd for Sensor X
SxLy	Line Y for Sensor X video frame
SxLN	Last line for Sensor X video frame

S0L1,S1L1,S2L1,S3L1 indicates concatenation of the first video line from each sensor into a single video line. This packet has a modified header and footer that matches the concatenated line data.

Packets would have the same VC ID, based on the VC ID for the lowest number sensor port being forwarded.

Lines are concatenated on a byte basis without padding between video line data.

7.4.25.5.1 Code Example for Line-Concatenated CSI-2 Forwarding

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4c,0x01) # RX0
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX1 VC=0 ***"
WriteI2C(0x4c,0x12) # RX1
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX2 VC=0 ***"
WriteI2C(0x4c,0x24) # RX2
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX3 VC=0 ***"
WriteI2C(0x4c,0x38) # RX3
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
#  "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI0 select
#  "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI0 4L
# "*** CSI0_SYNC_FWD synchronous forwarding with line concatenation ***"
WriteI2C(0x21,0x3c) # synchronous forwarding with line concatenation
#  "***FWD_PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0
```

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4c,0x01) # RX0
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX1 VC=0 ***"
WriteI2C(0x4c,0x12) # RX1
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX2 VC=0 ***"
WriteI2C(0x4c,0x24) # RX2
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
# "*** RX3 VC=0 ***"
WriteI2C(0x4c,0x38) # RX3
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
#  "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI-2 select
#  "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI-2 4L
# "*** CSI_SYNC_FWD synchronous forwarding with line interleaving ***"
WriteI2C(0x21,0x28) # synchronous forwarding with line interleaving
#  "*** FWD_PORT all RX to CSI"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI-2
```


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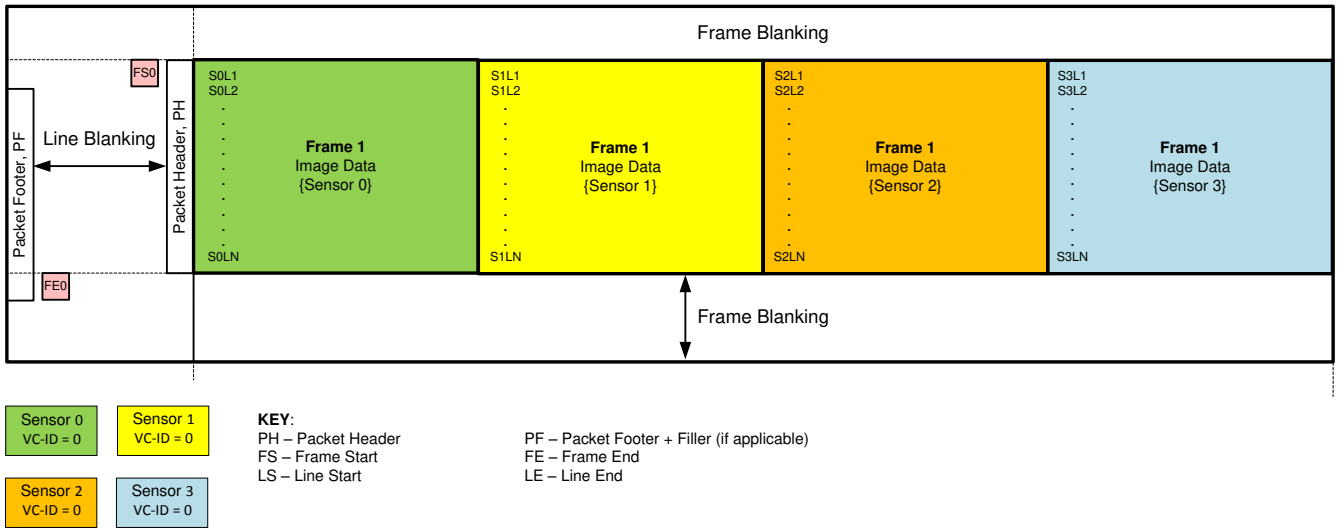

Blanking intervals do not provide accurate synchronization timing

Figure 7-18. Line-Concatenated Format

7.4.25.6 CSI-2 Transmitter Output Control

Two register controls allow control of CSI-2 Transmitter outputs to disable the CSI-2 Transmitter outputs. If the OUTPUT_SLEEP_STATE_SELECT (OSS_SEL) control is set to 0 in the GENERAL_CFG 0x02 register (Table 7-20), the CSI-2 Transmitter outputs are forced to the HS-0 state. If the OUTPUT_ENABLE (OEN) register bit is set to 0 in the GENERAL_CFG register, the CSI-2 pins are set to the high-impedance state.

For normal operation (OSS_SEL and OEN both set to 1), the detection of activity on FPD3 inputs determines the state of the CSI-2 outputs. The FPD3 inputs are considered active if the Receiver indicates valid lock to the incoming signal. For a CSI-2 TX port, lock is considered valid if any Received port mapped to the TX port is indicating Lock.

Table 7-14. CSI-2 Output Control Options

PDB pin	OSS_SEL	OEN	FPD3 INPUT	CSI-2 PIN STATE
0	X	X	X	Hi-Z
1	0	X	X	HS-0
1	1	0	X	Hi-Z
1	1	1	Inactive	Hi-Z
1	1	1	Active	Valid

7.4.25.7 Enabling and Disabling CSI-2 Transmitters

Once enabled, it is typically best to leave the CSI-2 Transmitter enabled, and only change the forwarding controls if changes are required to the system. When enabling and disabling the CSI-2 Transmitter, forwarding should be disabled to ensure proper start and stop of the CSI-2 Transmitter.

When enabling and disabling the CSI-2 Transmitter, use the following sequence:

To Disable:
1. Disable Forwarding for assigned ports in the FWD_CTL1 register
2. Disable CSI-2 Periodic Calibration (if enabled) in the CSI_ CTL2 register
3. Disable Continuous Clock operation (if enabled) in the CSI_ CTL register
4. Clear CSI-2 Transmit enable in CSI_ CTL register

To Enable:
1. Set CSI-2 Transmit enable (and Continuous clock if desired) in CSI_ CTL register
2. Enable CSI-2 Periodic Calibration (if desired) in the CSI_CTL2 register

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3. Enable Forwarding for assigned ports in the FWD_CTL1 register

7.5 Programming

7.5.1 Serial Control Bus

The DS90UB662-Q1 implements two I2C-compatible serial control buses. Both I2C ports support local device configuration and incorporate a bidirectional control channel (BCC) that allows communication with a remote serializers as well as remote I2C slave devices.

The device address is set through a resistor divider connected to the IDx pin (R1 and R2 – see Figure 7-19).

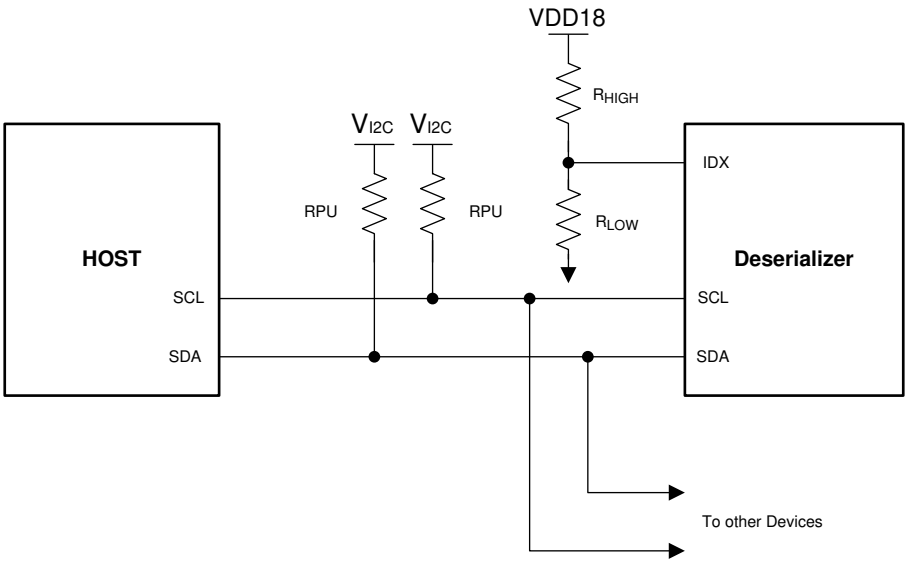

Figure 7-19. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pullup resistor to VDDIO. For most applications, TI recommends a 4.7-kΩ pullup resistor to VDDIO. However, the pullup resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

The IDX pin configures the control interface to one of eight possible device addresses. A pullup resistor and a pulldown resistor may be used to set the appropriate voltage ratio between the IDX input pin (V_{IDX}) and $V_{(VDD18)}$, each ratio corresponding to a specific device address. See Table 7-15, Serial Control Bus Addresses for IDX.

Table 7-15. Serial Control Bus Addresses for IDX

NO.	V_{IDX} VOLTAGE RANGE			V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		PRIMARY ASSIGNED I2C ADDRESS	
	V_{MIN}	V_{TYP}	V_{MAX}	VDD18 = 1.80 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	7-BIT	8-BIT
0	0	0	0.131 × $V_{(VDD18)}$	0	OPEN	10.0	0x30	0x60
1	0.179 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.374	88.7	23.2	0x32	0x64
2	0.296 × $V_{(VDD18)}$	0.330 × $V_{(VDD18)}$	0.362 × $V_{(VDD18)}$	0.582	75.0	35.7	0x34	0x68
3	0.412 × $V_{(VDD18)}$	0.443 × $V_{(VDD18)}$	0.474 × $V_{(VDD18)}$	0.792	71.5	56.2	0x36	0x6C
4	0.525 × $V_{(VDD18)}$	0.559 × $V_{(VDD18)}$	0.592 × $V_{(VDD18)}$	0.995	78.7	97.6	0x38	0x70
5	0.642 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.704 × $V_{(VDD18)}$	1.202	39.2	78.7	0x3A	0x74
6	0.761 × $V_{(VDD18)}$	0.792 × $V_{(VDD18)}$	0.823 × $V_{(VDD18)}$	1.420	25.5	95.3	0x3C	0x78
7	0.876 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	0x3D	0x7A

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SDA transitions Low while SCL is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See Figure 7-20.

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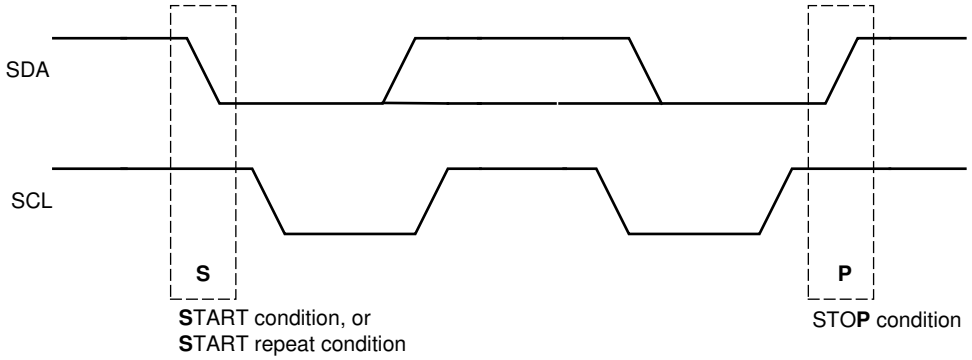

Figure 7-20. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it acknowledges (ACKs) the master by driving the SDA bus low. If the address does not match one of the slave addresses of the device, it not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs can also occur on the bus when data transmissions are in process. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 7-21 and a WRITE is shown in Figure 7-22.

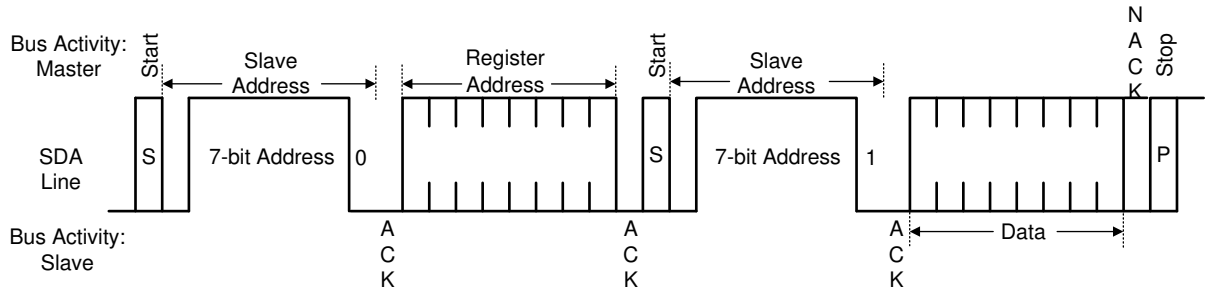

Figure 7-21. Serial Control Bus — READ

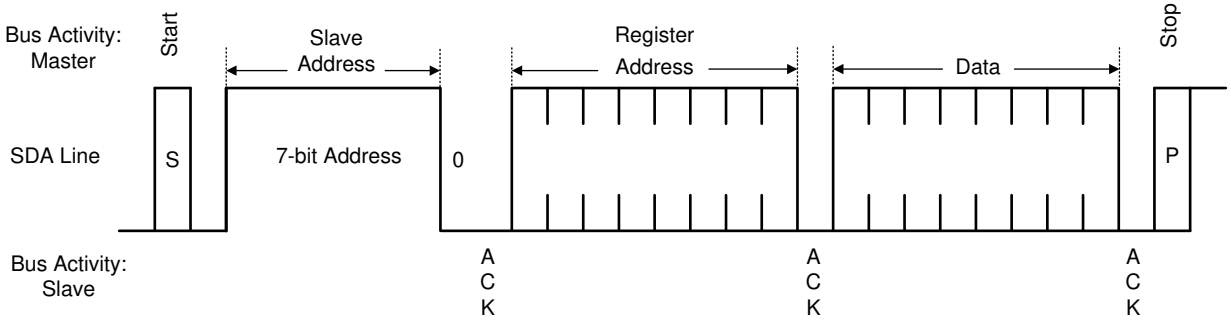

Figure 7-22. Serial Control Bus — WRITE

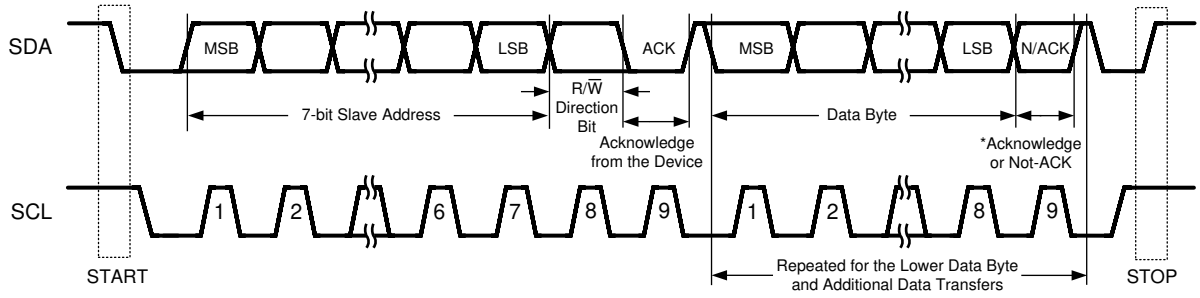

Figure 7-23. Basic Operation

The I2C Master located at the Deserializer must support I2C clock stretching. For more information on I2C interface requirements and throughput considerations, refer to *I2C Communication Over FPD-Link III With Bidirectional Control Channel* (SNLA131) and *I2C over DS90UB913/4 FPD-Link III With Bidirectional Control Channel* (SNLA222).

7.5.2 Second I2C Port

The DS90UB662-Q1 includes a second I2C port that allows bidirectional control channel access to both local registers and remote devices. Remote device access is configured on BCCx_MAP register 0x0C[7:4] (Table 7-30).

The second I2C port uses the same I2C address as the primary I2C port. In addition, RX Port I2C IDs are also available for the second I2C port.

In general, TI recommends that the second I2C port be used in cases where the CSI-2 TX ports are connected to separate processors. The second I2C port allows independent control of the DS90UB662-Q1 as well as remote devices by the second processor. However, Register 0x01 (RESET_CTL) can only be written by the primary I2C port.

7.5.3 I2C Slave Operation

The DS90UB662-Q1 implements an I2C-compatible slave capable of operation compliant to the Standard, Fast, and Fast-plus modes of operation allowing I2C operation at up to 1-MHz clock frequencies. Local I2C transactions to access DS90UB662-Q1 registers can be conducted 2 ms after power supplies are stable and PDB is brought high. For accesses to local registers, the I2C Slave operates without stretching the clock. The primary I2C slave address is set through the IDx pin. The primary I2C slave address is stored in the I2C Device ID register at address 0x0. In addition to the primary I2C slave address, the DS90UB662-Q1 may be programmed to respond to up to four other I2C addresses. The four RX Port ID addresses provide direct access to the Receive Port registers without the need to set the paging controls normally required to access the port registers.

7.5.4 Remote Slave Operation

The Bidirectional control channel provides a mechanism to read or write I2C registers in remote devices over the FPD-Link III interface. The I2C Master located at the Deserializer must support I2C clock stretching. Accesses to serializer or remote slave devices over the Bidirectional Control Channel will result in clock stretching to allow for response time across the link. The DS90UB662-Q1 acts as an I2C slave on the local bus, forwards read and write requests to the remote device, and returns the response from the remote device to the local I2C bus. To allow for the propagation and regeneration of the I2C transaction at the remote device, the DS90UB662-Q1 will stretch the I2C clock while waiting for the remote response. To communicate with a remote slave device, the Rx Port which is intended for messaging also must be selected in register 0x4C (Table 7-90). The I2C address of the currently selected RX Port serializer will be populated in register 0x5B of the DS90UB662-Q1. The BCC_CONFIG register 0x58 (Table 7-102) also must have bit 6, I2C_PASS_THROUGH set to one. If enabled, local I2C transactions with valid address decode will then be forwarded through the Bidirectional Control Channel to the remote I2C bus. When I2C PASS THROUGH is set, the deserializer will only propagate messages that it recognizes, such as the registered serializer alias address (SER ALIAS), or any registered remote slave alias attached to the serializer I2C bus (SLAVE ALIAS) assigned to the specific Rx Port. Setting

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PASS THROUGH ALL and AUTO ACK are less common use cases and primarily used for debugging I2C messaging as they will respectively pass all addresses regardless of valid I2C address (PASS_THROUGH_ALL) and acknowledge all I2C commands without waiting for a response from serializer (AUTO_ACK).

7.5.5 Remote Slave Addressing

Various system use cases require multiple sensor devices with the same fixed I2C slave address to be remotely accessible from the same I2C bus at the deserialilzer. The DS90UB662-Q1 provides slave ID virtual addressing to differentiate target slave addresses when connecting two or more remote devices. Eight pairs of SlaveAlias and SlaveID registers are allocated for each FPD-Link III Receive port in registers 0x5D through 0x6C (Table 7-107 through Table 7-122). The SlaveAlias register allows programming a virtual address which the host controller uses to access the remote device. The SlaveID register provides the actual slave address for the device on the remote I2C bus. Eight pairs of registers are available for each port (total of 16 pairs), so multiple devices may be directly accessible remotely without the need for reprogramming. Multiple SlaveAlias can be assigned to the same SlaveID as well.

7.5.6 Broadcast Write to Remote Devices

The DS90UB662-Q1 provides a mechanism to broadcast I2C writes to remote devices (either remote slaves or serializers). For each Receive port, the SlaveID/Alias register pairs would be programmed with the same SlaveAlias value so they would each respond to the local I2C access. The SlaveID value would match the intended remote device address, either remote slave or serializers. For each receive port, on of the SlaveAlias registers is set with an Alias value. For each port, the SlaveID value is set to the address of the remote device. These values may be the same. To access the remote serializer registers rather than a remote slave, the serializer ID (SER_IDx or SER_IDy) would be used as the SlaveID value.

7.5.6.1 Code Example for Broadcast Write

```
#  "FPD3_PORT_SEL Boardcast RX0/1/2/3"
WriteI2C(0x4c,0x0f) # RX_PORT0 read; RX0/1/2/3 write
#  "enable pass throu"
WriteI2C(0x58,0x58) # enable pass throu
WriteI2C(0x5c,0x18) # "SER_ALIAS_ID"
WriteI2C(0x5d,0x60) # "SlaveID[0]"
WriteI2C(0x65,0x60) # "SlaveAlias[0]"
WriteI2C(0x7c,0x01) # "FV_POLARITY"
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
```

7.5.7 I2C Master Proxy

The DS90UB662-Q1 implements an I2C master that acts as a proxy master to regenerate I2C accesses originating from a remote serializer (DS90UB633A-Q1). By default, the I2C Master Enable bit (I2C_MASTER_EN) is set = 0 in register 0x02[5] to block Master access to local deserialilzer I2C from remote serializers. Set I2C_MASTER_EN] = 1 if the system requires the deserializer to act as proxy master for remote serializers on the local deserializer I2C bus. The proxy master is an I2C-compatible master capable of operating with Standard-mode, Fast-mode, or Fast-mode Plus I2C timing. It is also capable of arbitration with other masters, allowing multiple masters and slaves to exist on the I2C bus. A separate I2C proxy master is implemented for each Receive port. This allows independent operation for all sources to the I2C interface. Arbitration between multiple sources is handled automatically using I2C multi-master arbitration.

7.5.8 I2C Master Proxy Timing

The proxy master timing parameters are based on the REFCLK timing. Timing accuracy for the I2C proxy master based on the REFCLK clock source attached to the DS90UB662-Q1 deserializer. Before REFCLK is applied the deserializer will default to internal reference clock with accuracy of 25 MHz ±10%. The I2C Master regenerates the I2C read or write access using timing controls in the registers 0x0A and 0x0B (Table 7-28 and Table 7-29) to regenerate the clock and data signals to meet the desired I2C timing in standard, fast, or fast-plus modes of operation.

I2C Master SCL High Time is set in register 0x0A[7:0]. This field configures the high pulse width of the SCL output when the Serializer is the Master on the local deserializer I2C bus. The default value is set to provide a minimum 5-µs SCL high time with the reference clock at 25 MHz + 100 ppm including four additional oscillator

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clock periods or synchronization and response time. Units are 40 ns for the nominal oscillator clock frequency, giving Min_delay = 40 ns × (SCL_HIGH_TIME + 4).

I2C Master SCL Low Time is set in register 0x0B[7:0]. This field configures the low pulse width of the SCL output when the Serializer is the Master on the local deserializer I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. The default value is set to provide a minimum 5-µs SCL high time with the reference clock at 25 MHz + 100ppm including four additional oscillator clock periods or synchronization and response time. Units are 40 ns for the nominal oscillator clock frequency, giving Min_delay = 40 ns × (SCL_HIGH_TIME + 4). See Table 7-16 example settings for Standard mode, Fast mode and Fast-mode Plus timing.

Table 7-16. Typical I2C Timing Register Settings

I2C MODE	SCL HIGH TIME		SCL LOW TIME	
	0x7A[7:0]	NOMINAL DELAY AT REFCLK = 25 MHz	0x7B[7:0]	NOMINAL DELAY AT REFCLK = 25 MHz
Standard	0x7A	5.04 µs	0x7A	5.04 µs
Fast	0x13	0.920 µs	0x25	1.64 µs
Fast - Plus	0x06	0.400 µs	0x0C	0.640 µs

7.5.8.1 Code Example for Configuring Fast-Mode Plus I2C Operation

```
#  "RX0 I2C Master Fast Plus Configuration"
WriteI2C(0x02,0x3E) # Enable Proxy
WriteI2C(0x4c,0x01) # Select RX_PORT0
# Set SCL High and Low Time delays
WriteI2C(0x0a,0x06) # SCL High
WriteI2C(0x0b,0x0C) # SCL Low
```

7.5.9 Interrupt Support

Interrupts can be brought out on the INTB pin as controlled by the INTERRUPT_CTL 0x23 (Table 7-53) and INTERRUPT_STS 0x24 (Table 7-54) registers. The main interrupt control registers provide control and status for interrupts from the individual sources. Sources include each of the four FPD3 Receive ports as well as each of the two CSI-2 Transmit ports. Clearing interrupt conditions requires reading the associated status register for the source. The setting of the individual interrupt status bits is not dependent on the related interrupt enable controls. The interrupt enable controls whether an interrupt is generated based on the condition, but does not prevent the interrupt status assertion.

For an interrupt to be generated based on one of the interrupt status assertions, both the individual interrupt enable and the INT_EN control must be set in the INTERRUPT_CTL 0x23 register. For example, to generate an interrupt if IS_RX0 is set, both the IE_RX0 and INT_EN bits must be set. If IE_RX0 is set but INT_EN is not, the INT status is indicated in the INTERRUPT_STS register, and the INTB pin does not indicate the interrupt condition.

See the INTERRUPT_CTL (Table 7-53) and INTERRUPT_STS (Table 7-54) register for details.

7.5.9.1 Code Example to Enable Interrupts

```
#  "RX01/2/3/4 INTERRUPT_CTL enable"
WriteI2C(0x23,0xBF) # RX all & INTB PIN EN
# Individual RX01/2/3/4 INTERRUPT_CTL enable
# "RX0 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x23,0x81) # RX0 & INTB PIN EN
# "RX1 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x23,0x82) # RX1 & INTB PIN EN
# "RX2 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0x23,0x84) # RX2 & INTB PIN EN
# "RX3 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0x23,0x88) # RX3 & INTB PIN EN
```


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7.5.9.2 FPD-Link III Receive Port Interrupts

For each FPD-Link III Receive port, multiple options are available for generating interrupts. Interrupt generation is controlled through the PORT_ICR_HI 0xD8 (Table 7-187) and PORT_ICR_LO 0xD9 (Table 7-188) registers. In addition, the PORT_ISR_HI 0xDA (Table 7-189) and PORT_ISR_LO 0xDB (Table 7-190) registers provide read-only status for the interrupts. Clearing of interrupt conditions is handled by reading the RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS registers. The status bits in the PORT_ISR_HI/LO registers are copies of the associated bits in the main status registers.

To enable interrupts from one of the Receive port interrupt sources:

1. Enable the interrupt source by setting the appropriate interrupt enable bit in the PORT_ICR_HI or PORT_ICR_LO register
2. Set the RX Port X Interrupt control bit (IE_RXx) in the INTERRUPT_CTL register
3. Set the INT_EN bit in the INTERRUPT_CTL register to allow the interrupt to assert the INTB pin low

To clear interrupts from one of the Receive port interrupt sources:

1. (optional) Read the INTERRUPT_STS register to determine which RX Port caused the interrupt
2. (optional) Read the PORT_ISR_HI and PORT_ISR_LO registers to determine source of interrupt
3. Read the appropriate RX_PORT_STS1, RX_PORT_STS2, or CSI_RX_STS register to clear the interrupt.

The first two steps are optional. The interrupt could be determined and cleared by just reading the status registers.

7.5.9.3 Interrupts on Forward Channel GPIO

When connected to the DS90UB633A-Q1 serializer, interrupts can be generated on changes in any of the four forward channel GPIOs per port. Interrupts are enabled by setting bits in the FC_GPIO_ICR register. Interrupts may be generated on rising and/or falling transitions on the GPIO signal. The GPIO interrupt status is cleared by reading the FC_GPIO_STS register.

Interrupts should only be used for GPIO signals operating at less than 10 MHz. High or low pulses that are less than 100 ns might not be detected at the DS90UB662-Q1. To avoid false interrupt indications, the interrupts should not be enabled until after the Forward Channel GPIOs are enabled at the serializer.

7.5.9.4 Interrupts on Change in Sensor Status

The FPD-Link III Receiver recovers 32-bits of Sensor status from the attached DS90UB633A-Q1 serializer. Interrupts may be generated based on changes in the Sensor Status values received from the forward channel. The Sensor Status consists of 4 bytes of data, which may be read from the SENSOR_STS_x registers for each Receive port. Interrupts may be generated based on a change in any of the bits in the first byte (SENSOR_STS_0). Each bit can be individually masked for Rising and/or Falling interrupts.

Two registers control the interrupt masks for the SENSOR_STS bits: SEN_INT_RISE_CTL and SEN_INT_FALL_CTL.

Two registers provide interrupt status: SEN_INT_RISE_STS, SEN_INT_FALL_STS.

If a mask bit is set, a change in the associated SENSOR_STS_0 bit will be detected and latched in the SEN_INT_RISE_STS or SEN_INT_FALL_STS registers. If the mask bit is not set, the associated interrupt status bit will always be 0. If any of the SEN_INT_RISE_STS or SEN_INT_FALL_STS bits is set, the IS_FC_SEN_STS bit will be set in the PORT_ISR_HI register.

7.5.9.5 Code Example to Readback Interrupts

```
INTERRUPT_STS = ReadI2C(0x24) # 0x24 INTERRUPT_STS
if ((INTERRUPT_STS & 0x80) >> 7):
    print "# GLOBAL INTERRUPT DETECTED "
if ((INTERRUPT_STS & 0x40) >> 6):
    print "# RESERVED "
if ((INTERRUPT_STS & 0x20) >> 5):
    print "# IS_CSI_TX1 DETECTED "
if ((INTERRUPT_STS & 0x10) >> 4):
    print "# IS_CSI_TX0 DETECTED "
```

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```
if ((INTERRUPT_STS & 0x08) >> 3):
    print "# IS_RX3 DETECTED "
if ((INTERRUPT_STS & 0x04) >> 2):
    print "# IS_RX2 DETECTED "
if ((INTERRUPT_STS & 0x02) >> 1):
    print "# IS_RX1 DETECTED "
if ((INTERRUPT_STS & 0x01) ):
    print "# IS_RX0 DETECTED "
# "################################################"
#  "RX0 status"
# "################################################"
WriteReg(0x4C,0x01) # RX0
PORT_ISR_LO = ReadI2C(0xDB)
print "0xDB PORT_ISR_LO : ", hex(PORT_ISR_LO) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "
################################################
PORT_ISR_HI = ReadI2C(0xDA)
print "0xDA PORT_ISR_HI : ", hex(PORT_ISR_HI) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "
################################################
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR
if (  (RX_PORT_STS1 & 0xc0) >> 6) == 3:
    print "# RX_PORT_NUM = RX3"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 2:
    print "# RX_PORT_NUM = RX2"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "
################################################
RX_PORT_STS2 = ReadI2C(0x4E)
if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "
```


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```
################################################
# "################################################"
#  "RX1 status"
# "################################################"
WriteReg(0x4C,0x12) # RX1
PORT_ISR_LO = ReadI2C(0xDB) # PORT_ISR_LO readout; cleared by RX_PORT_STS2
if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "
################################################
PORT_ISR_HI = ReadI2C(0xDA) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "
################################################
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR
if (  (RX_PORT_STS1 & 0xc0) >> 6) == 3:
    print "# RX_PORT_NUM = RX3"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 2:
    print "# RX_PORT_NUM = RX2"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "
################################################
RX_PORT_STS2 = ReadI2C(0x4E)
if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "
################################################
# "################################################"
#  "RX2 status"
# "################################################"
WriteReg(0x4C,0x24) # RX2
PORT_ISR_LO = ReadI2C(0xDB) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
```

```
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "
################################################
PORT_ISR_HI = ReadI2C(0xDA) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "
################################################
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR
if (  (RX_PORT_STS1 & 0xc0) >> 6) == 3:
    print "# RX_PORT_NUM = RX3"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 2:
    print "# RX_PORT_NUM = RX2"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "
################################################
RX_PORT_STS2 = ReadI2C(0x4E)
if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "

################################################
# "################################################"
#  "RX3 status"
# "################################################"
WriteReg(0x4C,0x38) # RX3
PORT_ISR_LO = ReadI2C(0xDB) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
```


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```
    print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "
################################################
PORT_ISR_HI = ReadI2C(0xDA) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "
################################################
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR
if (  (RX_PORT_STS1 & 0xc0) >> 6) == 3:
    print "# RX_PORT_NUM = RX3"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 2:
    print "# RX_PORT_NUM = RX2"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "
################################################
RX_PORT_STS2 = ReadI2C(0x4E)
if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "

################################################
```

7.5.9.6 CSI-2 Transmit Port Interrupts

The following interrupts are available for each CSI-2 Transmit Port:

- Pass indication
- Synchronized status
- Deassertion of Pass indication for an input port assigned to the CSI-2 TX Port
- Loss of Synchronization between input video streams
- RX Port Interrupt – interrupts from RX Ports mapped to this CSI-2 Transmit port

See the CSI_TX_ICR address 0x36 (Table 7-72) and CSI_TX_ISR address 0x37 (Table 7-73) registers for details.

The setting of the individual interrupt status bits is not dependent on the related interrupt enable controls. The interrupt enable controls whether an interrupt is generated based on the condition, but the enable does not prevent the interrupt status assertion.

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7.5.10 Error Handling

In the DS90UB662-Q1, the FPD-Link III receiver transfers incoming video frames to internal video buffers for forwarding to the CSI-2 Transmit ports. When the DS90UB662-Q1 detects an error condition the standard operation would be to flag this error condition, and stop sending the CSI-2 frame to avoid sending corrupted data downstream. When the DS90UB662-Q1 recovers from an error condition, it will provide a Start of Frame and resume sending valid data. Consequently, when the downstream CSI-2 input receives a repeated Start of Frame condition, this will indicate that the data received in between the prior start of frame is suspect and the signal processor can then discard the suspected data. The settings in registers PORT_CONFIG2 (Table 7-138) and PORT_PASS_CTL (Table 7-139) can be used to change how the DS90UB662-Q1 handles errors when passing video frames. The receive ports may be configured to qualify the incoming video and provide a status indication and prevent the forwarding of video frames until certain error-free conditions are met. The Pass indication may be used to prevent forwarding packets to the internal video buffers by setting the PASS_DISCARD_EN bit in the PORT_PASS_CTL register. When this bit is set, video input will be discarded until the Pass signal indicates valid receive data. The Receive port will indicate Pass status once specific conditions are met, including a number of valid frames received. Valid frames may include requiring no FPD-Link III Parity errors and consistent frame size, including video line length and/or number of video lines.

In addition, the Receive port may be programmed to cut off video frames containing errors and/or prevent forwarding of video until the Pass conditions are met. Register settings in PORT_CONFIG2 register (Table 7-138) can be used to cut off frames on different line/frame sizes or a CSI-2 parity error is detected. When the deserializer cuts off frames in cases of different line/frame sizes different line/frame sizes, the video frame will stop immediately with no frame end packet. Often the condition will not be cleared until the next valid frame is received.

The Rx Port PASS indication may be used to prevent forwarding packets to the internal video buffers by setting the PASS_DISCARD_EN bit in the PORT_PASS_CTL register (Table 7-139). When this bit is set, video input will be discarded until the Pass signal indicates valid receive data. The incoming video frames may be cut off based on error conditions or change in video line size or number of lines. These functions are controlled by bits in the PORT_CONFIG2 register. When cutting off video frames, the video frame may be cut off after sending any number of video lines. A cut off frame will not send a Frame End packet to the CSI-2 Transmit port.

7.5.10.1 Receive Frame Threshold

The FPD-Link III Receiver may be programmed to require a specified number of valid video frames prior to indicating a Pass condition and forwarding video frames. The number of required valid video frames is programmable through the PASS_THRESH field in the PORT_PASS_CTL register (Table 7-139). The threshold can be programmed from 0 to 3 video frames. If set to 0, Pass will typically be indicated as soon as the FPD-Link III Receiver reports Lock to the incoming signal. If set greater than 0, the Receiver will require that number of valid frames before indicating Pass. Determination of valid frames will be dependent on the control bits in the PORT_PASS_CTL register. In the case of a Parity Error, when PASS_PARITY_ERR is set to 1 forwarding will be enabled one frame early. To ensure at least one good frame occurs following a parity error the counter should be set to 2 or higher when PASS_PARITY_ERR = 1.

7.5.10.2 Port PASS Control

When the PASS_LINE_SIZE control is set in the PORT_PASS_CTL register, the Receiver will qualify received frames based on having a consistent video line size. For PASS_LINE_SIZE to be clear, the deserializer checks that the received line length remains consistent during the frame and between frames. For each video line, the length (in bytes) will be determined. If it varies then we will flag this condition. Each video line in the packet must be the same size, and the line size must be consistent across video frames. A change in video line size will restart the valid frame counter.

When the PASS_LINE_CNT control is set in the PORT_PASS_CTL register, the Receiver will qualify received frames based on having a consistent frame size in number of lines. A change in number of video lines will restart the valid frame counter.

When the PASS_PARITY_ERR control is set in the PORT_PASS_CTL register, the Receiver will clear the Pass indication on receipt of a parity error on the FPD-Link III interface. The valid frame counter will also be cleared on

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the parity error event. When PASS_PARITY_ERR is set to 1, TI also recommends that the designer set the PASS_THRESHOLD to 2 or higher to ensure at least one good frame occurs following a parity error.

7.5.11 Timestamp – Video Skew Detection

The DS90UB662-Q1 implements logic to detect skew between video signaling from attached sensors. For each input port, the DS90UB662-Q1 provides the ability to capture a time-stamp for both a start-of-frame and start-of-line event. Comparison of timestamps can provide information on the relative skew between the ports. Start-of-frame timestamps are generated at the active edge of the Vertical Sync signal in Raw mode. Start-of-line timestamps are generated at the start of reception of the Nth line of video data after the Start of Frame for either mode of operation. The function does not use the Line Start (LS) packet or Horizontal Sync controls to determine the start of lines.

The skew detection can run in either a FrameSync mode or free-run mode.

Skew detection can be individually enabled for each RX port.

For start-of-line timestamps, a line number must be programmed. The same line number is used for all 4 channels. Prior to reading timestamps, the TS_FREEZE bit for each port that will be read should be set. This will prevent overwrite of the timestamps by the detection circuit until all timestamps have been read. The freeze condition will be released automatically once all frozen timestamps have been read. The freeze bits can also be cleared if it does not read all the timestamp values.

The TS_STATUS register includes the following:

- Flags to indicate multiple start-of-frame per FrameSync period
- Flag to indicate Timestamps Ready
- Flags to indicate Timestamps valid (per port) – if ports are not synchronized, all ports may not indicate valid timestamps

The Timestamp Ready flag will be cleared when the TS_FREEZE bit is cleared.

7.5.12 Pattern Generation

The DS90UB662-Q1 supports an internal pattern generation feature to provide a simple way to generate video test patterns for the CSI-2 transmitter outputs. Two types of patterns are supported: Reference Color Bar pattern and Fixed Color patterns and accessed by the Pattern Generator page 0 in the indirect register set.

Prior to enabling the Packet Generator, the following should be done:

1. Disable video forwarding by setting bits [5:4] of the FWD_CTL1 register (that is, set register 0x20 to 0x30).
2. Configure CSI-2 Transmitter operating speed using the CSI_PLL_CTL register.
3. Enable the CSI-2 Transmitter for port 0 using the CSI_CTL register.

7.5.12.1 Reference Color Bar Pattern

The Reference Color Bar Patterns are based on the pattern defined in Appendix D of the mipi_CTS_for_D-PHY_v1-1_r03 specification. The pattern is an eight color bar pattern designed to provide high, low, and medium frequency outputs on the CSI-2 transmit data lanes.

The CSI-2 Reference pattern provides eight color bars by default with the following byte data for the color bars: X bytes of 0xAA (high-frequency pattern, inverted) X bytes of 0x33 (mid-frequency pattern) X bytes of 0xF0 (low-frequency pattern, inverted) X bytes of 0x7F (lone 0 pattern) X bytes of 0x55 (high-frequency pattern) X bytes of 0xCC (mid-frequency pattern, inverted) X bytes of 0x0F (low-frequency pattern) Y bytes of 0x80 (lone 1 pattern) In most cases, Y will be the same as X. For certain data types, the last color bar may need to be larger than the others to properly fill the video line dimensions.

The Pattern Generator is programmable with the following options:

- Number of color bars (1, 2, 4, or 8)
- Number of bytes per line
- Number of bytes per color bar
- CSI-2 DataType field and VC-ID

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- Number of active video lines per frame
- Number of total lines per frame (active plus blanking)
- Line period (possibly program in units of 10 ns)
- Vertical front porch – number of blank lines prior to FrameEnd packet
- Vertical back porch – number of blank lines following FrameStart packet

The pattern generator relies on proper programming by software to ensure the color bar widths are set to multiples of the block (or word) size required for the specified DataType. For example, for RGB888, the block size is 3 bytes which also matches the pixel size. In this case, the number of bytes per color bar must be a multiple of 3. The Pattern Generator is implemented in the CSI-2 Transmit clock domain, providing the pattern directly to the CSI-2 Transmitter. The circuit generates the CSI-2 formatted data.

7.5.12.2 Fixed Color Patterns

When programmed for Fixed Color Pattern mode, Pattern Generator can generate a video image with a programmable fixed data pattern. The basic programming fields for image dimensions are the same as used with the Color Bar Patterns. When sending Fixed Color Patterns, the color bar controls allow alternating between the fixed pattern data and the bit-wise inverse of the fixed pattern data.

The Fixed Color patterns assume a fixed block size for the byte pattern to be sent. The block size is programmable through the register and is designed to support most 8-bit, 10-bit, and 12-bit pixel formats. The block size should be set based on the pixel size converted to blocks that are an integer multiple of bytes. For example, an RGB888 pattern would consist of 3-byte pixels and therefore require a 3-byte block size. A 2x12-bit pixel image would also require 3-byte block size, while a 3x12-bit pixel image would require nine bytes (two pixels) to send an integer number of bytes. Sending a RAW10 pattern typically requires a 5-byte block size for four pixels, so 1x10-bit and 2x10-bit could both be sent with a 5-byte block size. For 3x10-bit, a 15-byte block size would be required.

The Fixed Color patterns support block sizes up to 16 bytes in length, allowing additional options for patterns in some conditions. For example, an RGB888 image could alternate between four different pixels by using a 12-byte block size. An alternating black and white RGB888 image could be sent with a block size of 6-bytes and setting first three bytes to 0xFF and next three bytes to 0x00.

To support up to 16-byte block sizes, a set of sixteen registers are implemented to allow programming the value for each data byte. The line period is calculated in units of 10 ns, unless the CSI-2 mode is set to 400-Mb operation in which case the unit time dependancy is 20 ns.

7.5.12.3 Packet Generator Programming

The information in this section provides details on how to program the Pattern Generator to provide a specific color bar pattern, based on data type, frame size, and line size.

Most basic configuration information is determined directly from the expected video frame parameters. The requirements should include the data type, frame rate (frames per second), number of active lines per frame, number of total lines per frame (active plus blanking), and number of pixels per line.

- PGEN_ACT_LPF – Number of active lines per frame
- PGEN_TOT_LPF – Number of total lines per frame
- PGEN_LSIZE – Video line length size in bytes. Compute based on pixels per line multiplied by pixel size in bytes
- CSI-2 DataType field and VC-ID
- Optional: PGEN_VBP – Vertical back porch. This is the number of lines of vertical blanking following Frame Valid
- Optional: PGEN_VFP – Vertical front porch. This is the number of lines of vertical blanking preceding Frame Valid
- PGEN_LINE_PD – Line period in 10-ns units. Compute based on Frame Rate and total lines per frame
- PGEN_BAR_SIZE – Color bar size in bytes. Compute based on datatype and line length in bytes (see details below)

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7.5.12.3.1 Determining Color Bar Size

The color bar pattern should be programmed in units of a block or word size dependent on the datatype of the video being sent. The sizes are defined in the Mipi CSI-2 specification. For example, RGB888 requires a 3-byte block size which is the same as the pixel size. RAW10 requires a 5-byte block size which is equal to 4 pixels. RAW12 requires a 3-byte block size which is equal to 2 pixels.

When programming the Pattern Generator, software should compute the required bar size in bytes based on the line size and the number of bars. For the standard eight color bar pattern, that would require the following algorithm:

- Select the desired data type, and a valid length for that data type (in pixels).
- Convert pixels/line to blocks/line (by dividing by the number of pixels/block, as defined in the data type specification).
- Divide the blocks/line result by the number of color bars (8), giving blocks/bar
- Round result down to the nearest integer
- Convert blocks/bar to bytes/bar and program that value into the PGEN_BAR_SIZE register

As an alternative, the blocks/line can be computed by converting pixels/line to bytes/line and divide by bytes/block.

7.5.12.4 Code Example for Pattern Generator

```
#Patgen Fixed Colorbar 1280x720p30
WriteI2C(0x33,0x01) # CSI0 enable
WriteI2C(0xB0,0x00) # Indirect Pattern Gen Registers
WriteI2C(0xB1,0x01) # PGEN_CTL
WriteI2C(0xB2,0x01)
WriteI2C(0xB1,0x02) # PGEN_CFG
WriteI2C(0xB2,0x33)
WriteI2C(0xB1,0x03) # PGEN_CSI_DI
WriteI2C(0xB2,0x24)
WriteI2C(0xB1,0x04) # PGEN_LINE_SIZE1
WriteI2C(0xB2,0x0F)
WriteI2C(0xB1,0x05) # PGEN_LINE_SIZE0
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x06) # PGEN_BAR_SIZE1
WriteI2C(0xB2,0x01)
WriteI2C(0xB1,0x07) # PGEN_BAR_SIZE0
WriteI2C(0xB2,0xE0)
WriteI2C(0xB1,0x08) # PGEN_ACT_LPF1
WriteI2C(0xB2,0x02)
WriteI2C(0xB1,0x09) # PGEN_ACT_LPF0
WriteI2C(0xB2,0xD0)
WriteI2C(0xB1,0x0A) # PGEN_TOT_LPF1
WriteI2C(0xB2,0x04)
WriteI2C(0xB1,0x0B) # PGEN_TOT_LPF0
WriteI2C(0xB2,0x1A)
WriteI2C(0xB1,0x0C) # PGEN_LINE_PD1
WriteI2C(0xB2,0x0C)
WriteI2C(0xB1,0x0D) # PGEN_LINE_PD0
WriteI2C(0xB2,0x67)
WriteI2C(0xB1,0x0E) # PGEN_VBP
WriteI2C(0xB2,0x21)
WriteI2C(0xB1,0x0F) # PGEN_VFP
WriteI2C(0xB2,0x0A)
```

7.5.13 FPD-Link BIST Mode

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high-speed serial link and the back channel without external data connections. The BIST mode is enabled by programming the BIST configuration register (Table 7-165). This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

When BIST is activated, the DS90UB662-Q1 sends register writes to the Serializer through the Back Channel. The control channel register writes configure the Serializer for BIST mode operation. The serializer outputs a continuous stream of a pseudo-random sequence and drives the link at speed. The deserializer detects the test

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pattern and monitors the pattern for errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The CMLOUT output function is also available during BIST mode. While the lock indications are required to identify the beginning of proper data reception, for any link failures or data corruption, the best indication is the contents of the error counter in the BIST_ERR_COUNT register 0x57 (Table 7-101) for each RX port. The test may select whether the Serializer uses an external or internal clock as reference for the BIST pattern frequency.

7.5.13.1 BIST Operation

The FPD-Link III BIST is configured and enabled by programming the BIST Control register (Table 7-165). Set 0xB3 = 0x01 to enable BIST and set 0xB3 = 00 to disable BIST. BIST pass or fail status may be brought to GPIO pins by selecting the Pass indication for each receive port using the GPIOx_PIN_CTL registers. The Pass/Fail status will be de-asserted low for each data error detected on the selected port input data. In addition, it is advisable to bring the Receiver Lock status for selected ports to the GPIO pins as well. After completion of BIST, the BIST Error Counter may be read to determine if errors occurred during the test. If the DS90UB662-Q1 failed to lock to the input signal or lost lock to the input signal, the BIST Error Counter will indicate 0xFF. The maximum normal count value will be 0xFE. The SER_BIST_ACT register bit 0xD0[5] can be monitored during testing to ensure BIST is activated in the serializer.

During BIST, DS90UB662-Q1 output activity are gated by BIST_Control[7:6] (BIST_OUT_MODE[1:0]) as follows:

00 : Outputs disabled during BIST

10 : Outputs enabled during BIST

When enabling the outputs by setting BIST_OUT_MODE = 10, the CSI-2 will be inactive by default (LP11 state). To exercise the CSI-2 interface during BIST mode, it is possible to Enable Pattern Generator to send a video data pattern on the CSI-2 outputs.

The BIST clock frequency is controlled by the BIST_CLOCK_SOURCE field in the BIST Control register. This 2-bit value will be written to the Serializer register 0x14[2:1]. A value of 00 will select an external clock. A non-zero value will enable an internal clock of the frequency defined in the Serializer register 0x14. Note that when the DS90UB662-Q1 is paired with DS90UB633A-Q1, a setting of 11 may result in a frequency that is too slow for the DS90UB662-Q1 to recover. The BIST_CLOCK_SOURCE field is sampled at the start of BIST. Changing this value after BIST is enabled will not change operation.

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7.6 Register Maps

The DS90UB662-Q1 implements the following register blocks, accessible through I2C as well as the bidirectional control channel:

- Main Registers
- FPD3 RX Port Registers (separate register block for each of the four RX ports)
- CSI-2 Port Registers (separate register block for each of the CSI-2 ports)

Table 7-17. Main Register Map Descriptions

ADDRESS RANGE	DESCRIPTION	ADDRESS MAP			
0x00-0x32	Digital Registers	Shared			
0x33-0x3A	Digital CSI-2 Registers (paged, broadcast write allowed)	CSI-2 TX Port 0 *R: 0x32[4]=0* *W: 0x32[0]=1*		Reserved	
0x3B-0x3F	Reserved Registers	Reserved			
0x40-0x45	AEQ Registers	Shared			
0x46-0x7F	Digital RX Port Registers (paged, broadcast write allowed)	FPD3 RX Port 0 *R: 0x4C[5:4]=00* *W: 0x4C[0]=1*	FPD3 RX Port 1 *R: 0x4C[5:4]=01* *W: 0x4C[1]=1*	FPD3 RX Port 2 *R: 0x4C[5:4]=10* *W: 0x4C[2]=1*	FPD3 RX Port 3 *R: 0x4C[5:4]=11* *W: 0x4C[3]=1*
0x80-0x8F	Reserved Registers	Reserved			
0x90-0x9F	Digital CSI-2 Debug Registers	Shared			
0xA0-0xAF	Reserved Registers	Reserved			
0xB0-0xB2	Indirect Access Registers	Shared			
0xB3-0xBF	Digital Registers	Shared			
0xC0-0xCF	Reserved Registers	Reserved			
0xD0-0xDF	Digital RX Port Debug Registers	FPD3 RX Port 0 *R: 0x4C[5:4]=00* *W: 0x4C[0]=1*	FPD3 RX Port 1 *R: 0x4C[5:4]=01* *W: 0x4C[1]=1*	FPD3 RX Port 2 *R: 0x4C[5:4]=10* *W: 0x4C[2]=1*	FPD3 RX Port 3 *R: 0x4C[5:4]=11* *W: 0x4C[3]=1*
0xE0-0xEF	Reserved Registers	Reserved			
0xF0-0xF5	FPD3 RX ID Registers	Shared			
0xF6-0xF7	Reserved Registers	Reserved			
0xF8-0xFB	Port I2C Addressing	Shared			
0xFC-0xFF	Reserved Registers	Reserved			

7.6.1 Digital Registers (Shared)

7.6.1.1 I2C Device ID Register

The I2C Device ID Register field always indicates the current value of the I2C ID. When bit 0 of this register is 0, this field is read-only and shows the strapped ID from device initialization after power on. When bit 0 of this register is 1, this field is read/write and can be used to assign any valid I2C ID address to the deserializer.

Table 7-18. I2C_DEVICE_ID Register (Address 0x00)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	DEVICE_ID	R/W/S	Strap	7-bit I2C ID of Deserializer. This field always indicates the current value of the I2C ID. When bit 0 of this register is 0, this field is read-only and show the strapped ID. When bit 0 of this register is 1, this field is read/write and can be used to assign any valid I2C ID.
0	DES_ID	R/W	0	0: Device ID is from strap 1: Register I2C Device ID overrides strapped value

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7.6.1.2 Reset Control Register

The Reset Control register allows for soft digital reset of the DS90UB662-Q1 device internal circuitry without using PDB hardware analog reset. Digital Reset 0 is recommended if desired to reset without overwriting configuration registers to default values.

Table 7-19. RESET_CTL Register (Address 0x01)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	-	0x0	Reserved
5	RESERVED	-	0	Reserved
4:3	RESERVED	-	0x0	Reserved
2	RESTART_AUTOLOAD	R/W/SC	0	Restart ROM Auto-load Setting this bit to 1 causes a re-load of the ROM. This bit is self-clearing. Software may check for Auto-load complete by checking the CFG_INIT_DONE bit in the DEVICE_STS register.
1	DIGITAL_RESET1	R/W/SC	0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation
0	DIGITAL_RESET0	R/W/SC	0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation

7.6.1.3 General Configuration Register

The general configuration register enables and disables high level block functionality.

Table 7-20. GENERAL_CFG Register (Address 0x02)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	-	0x0	Reserved
5	I2C_MASTER_EN	R/W	0	I2C Master Enable When this bit is 0, the local I2C master is disabled, when it is 1, the master is enabled.
4	OUTPUT_EN_MODE	R/W	1	Output Enable Mode If set to 0, the CSI-2 TX output port is forced to the high-impedance state if no assigned RX ports have an active Receiver lock. If set to 1, the CSI-2 TX output port will continue in normal operation if no assigned RX ports have an active Receiver lock. CSI-2 TX operation will remain under register control via the CSI_CTL register for each port. If no assigned RX ports have an active Receiver lock, this will result in the CSI-2 Transmitter entering the LP-11 state.
3	OUTPUT_ENABLE	R/W	1	Output Enable Control (in conjunction with Output Sleep State Select) If OUTPUT_SLEEP_STATE_SEL is set to 1 and this bit is set to 0, the CSI-2 TX outputs is forced into a high impedance state.
2	OUTPUT_SLEEP_STATE_SEL	R/W	1	OSS Select to control output state when LOCK is low (used in conjunction with Output Enable) When this bit is set to 0, the CSI-2 TX outputs is forced into a HS-0 state.
1	RX_PARITY_CHECKER_EN	R/W	1	FPD3 Receiver Parity Checker Enable When enabled, the parity check function is enabled for the FPD3 receiver. This allows detection of errors on the FPD3 receiver data bits. 0: Disable 1: Enable
0	FORCE_REFCLK_DET	R/W	0	Force indication of external reference clock 0: Normal operation, reference clock detect circuit indicates the presence of an external reference clock 1: Force reference clock to be indicated present

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7.6.1.4 Revision / Mask ID Register

Revision ID field for production silicon version can be read back from this register.

Table 7-21. REV_MASK_ID Register (Address 0x03)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	REVISION_ID	R	0x4	Revision ID 0010: PDS90UB662-Q1 A0
3:0	MASK_ID	R	0x0	Mask ID

7.6.1.5 Device Status Register

Device status register provides read back access to high level link diagnostics.

Table 7-22. DEVICE_STS Register (Address 0x04)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	CFG_CKSUM_STS	R	1	Config Checksum Passed This bit is set following initialization if the Configuration data in the eFuse ROM had a valid checksum
6	CFG_INIT_DONE	R	1	Power-up initialization complete This bit is set after Initialization is complete. Configuration from eFuse ROM has completed.
5	RESERVED	R	0	Reserved
4	REFCLK_VALID	R	0	REFCLK valid frequency This bit indicates when a valid frequency has been detected on the REFCLK pin. 0 : invalid frequency detected 1 : REFCLK frequency between 12 MHz and 64 MHz
3:0	RESERVED	-	0x0	Reserved

7.6.1.6 PAR_ERR_THOLD_HI Register

For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to total value in PAR_ERR_THOLD[15:0], the PARITY_ERROR flag is set in the RX_PORT_STS1 register. PAR_ERR_THOLD_HI contains bits [15:8] of the 16 bit parity error threshold PAR_ERR_THOLD[15:0].

Table 7-23. PAR_ERR_THOLD_HI Register (Address 0x05)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PAR_ERR_THOLD_HI	R/W	0x1	FPD3 Parity Error Threshold High byte This register provides the 8 most significant bits of the Parity Error Threshold value. For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to this value, the PARITY_ERROR flag is set in the RX_PORT_STS1 register.

7.6.1.7 PAR_ERR_THOLD_LO Register

For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to total value in PAR_ERR_THOLD[15:0], the PARITY_ERROR flag is set in the RX_PORT_STS1 register. PAR_ERR_THOLD_LO contains bits [7:0] of the 16-bit parity error threshold PAR_ERR_THOLD[15:0].

Table 7-24. PAR_ERR_THOLD_LO Register (Address 0x06)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PAR_ERR_THOLD_LO	R/W	0x0	FPD3 Parity Error Threshold Low byte This register provides the 8 least significant bits of the Parity Error Threshold value. For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to this value, the PARITY_ERROR flag is set in the RX_PORT_STS1 register.

7.6.1.8 BCC_WATCHDOG_CONTROL Register

The BCC watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time.

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Table 7-25. BCC_WATCHDOG_CONTROL Register (Address 0x07)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	BCC_WATCHDOG_TIMER	R/W	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bi-directional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
0	BCC_WATCHDOG_TIMER_DISABLE	R/W	0	Disable Bi-directional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation

7.6.1.9 I2C_CONTROL_1 Register

Table 7-26. I2C_CONTROL_1 Register (Address 0x08)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	LOCAL_WRITE_DISABLE	R/W	0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I2C master attached to the Serializer. Setting this bit does not affect remote access to I2C slaves at the Deserializer.
6:4	I2C_SDA_HOLD	R/W	0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds.
3:0	I2C_FILTER_DEPTH	R/W	0xC	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that is rejected. Units are 5 nanoseconds.

7.6.1.10 I2C_CONTROL_2 Register

Table 7-27. I2C_CONTROL_2 Register (Address 0x09)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	SDA_OUTPUT_SETUP	R/W	0x1	Remote Ack SDA Output Setup When a Control Channel (remote) access is active, this field configures setup time from the SDA output relative to the rising edge of SCL during ACK cycles. Setting this value will increase setup time in units of 640ns. The nominal output setup time value for SDA to SCL when this field is 0 is 80ns.
3:2	SDA_OUTPUT_DELAY	R/W	0x0	SDA Output Delay This field configures additional delay on the SDA output relative to the falling edge of SCL. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00: 240ns 01: 280ns 10: 320ns 11: 360ns
1	I2C_BUS_TIMER_SPEEDUP	R/W	0	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
0	I2C_BUS_TIMER_DISABLE	R/W	0	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 second, the I2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL

7.6.1.11 SCL High Time Register

The SCL High Time register field configures the high pulse width of the I2C SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to approximately 100 kHz with the internal oscillator clock running at nominal 25 MHz. Delay includes 4 additional

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oscillator clock periods. The internal oscillator has ±10% variation when REFCLK is not applied, which must be taken into account when setting the SCL High and Low Time registers.

Table 7-28. SCL High Time Register (Address 0x0A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SCL_HIGH_TIME	R/W	0x7A	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the reference clock at 25 MHz + 100ppm. The delay includes 5 additional oscillator clock periods. Min_delay = 39.996ns * (SCL_HIGH_TIME + 5)

7.6.1.12 SCL Low Time Register

The SCL Low Time register field configures the low pulse width of the SCL output when the serializer is the master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional control channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to approximately 100 kHz with the internal oscillator clock running at nominal 25 MHz. Delay includes 4 additional oscillator clock periods. The internal oscillator has ±10% variation when REFCLK is not applied, which must be taken into account when setting the SCL High and Low Time registers.

Table 7-29. SCL Low Time Register (Address 0x0B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SCL_LOW_TIME	R/W	0x7A	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bi-directional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the reference clock at 25 MHz + 100ppm. The delay includes 5 additional clock periods. Min_delay = 39.996ns * (SCL_LOW_TIME+ 5)

7.6.1.13 RX_PORT_CTL Register

Receiver port control register assigns rules for lock and pass in the general status register and allows for enabling and disabling each Rx port.

Table 7-30. RX_PORT_CTL Register (Address 0x0C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	BCC3_MAP	R/W	0	Map Control Channel 3 to I2C Slave Port 0: I2C Slave Port 0 1: I2C Slave Port 1
6	BCC2_MAP	R/W	0	Map Control Channel 2 to I2C Slave Port 0: I2C Slave Port 0 1: I2C Slave Port 1
5	BCC1_MAP	R/W	0	Map Control Channel 1 to I2C Slave Port 0: I2C Slave Port 0 1: I2C Slave Port 1
4	BCC0_MAP	R/W	0	Map Control Channel 0 to I2C Slave Port 0: I2C Slave Port 0 1: I2C Slave Port 1
3	PORT3_EN	R/W	1	Port 3 Receiver Enable 0: Disable Port 3 Receiver 1: Enable Port 3 Receiver
2	PORT2_EN	R/W	1	Port 2 Receiver Enable 0: Disable Port 2 Receiver 1: Enable Port 2 Receiver

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Table 7-30. RX_PORT_CTL Register (Address 0x0C) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
1	PORT1_EN	R/W	1	Port 1 Receiver Enable 0: Disable Port 1 Receiver 1: Enable Port 1 Receiver
0	PORT0_EN	R/W	1	Port 0 Receiver Enable 0: Disable Port 0 Receiver 1: Enable Port 0 Receiver

7.6.1.14 IO_CTL Register

Table 7-31. IO_CTL Register (Address 0x0D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	SEL3P3V	R/W	0	3.3V I/O Select on pins INTB, I2C, GPIO 0: 1.8V I/O Supply 1: 3.3V I/O Supply If IO_SUPPLY_MODE_OV is 0, a read of this register will return the detected I/O voltage level.
6	IO_SUPPLY_MODE_OV	R/W	0	Override I/O Supply Mode bit If set to 0, the detected voltage level is used for both SEL3P3V and IO_SUPPLY_MODE controls. If set to 1, the values written to the SEL3P3V and IO_SUPPLY_MODE fields is used.
5:4	IO_SUPPLY_MODE	R/W	0x0	I/O Supply Mode 00: 1.8V 11: 3.3V If IO_SUPPLY_MODE_OV is 0, a read of this register will return the detected I/O voltage level.
3:0	RESERVED	-	0x9	Reserved

7.6.1.15 GPIO_PIN_STS Register

This register reads the current values on each of the 8 GPIO pins.

Table 7-32. GPIO_PIN_STS Register (Address 0x0E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	GPIO_STS	R	0x0	GPIO Pin Status This register reads the current values on each of the 8 GPIO pins. Bit 7 reads GPIO7 and bit 0 reads GPIO0.

7.6.1.16 GPIO_INPUT_CTL Register

Table 7-33. GPIO_INPUT_CTL Register (Address 0x0F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	GPIO7_INPUT_EN	R/W	1	GPIO7 Input Enable 0: Disabled 1: Enabled
6	GPIO6_INPUT_EN	R/W	1	GPIO6 Input Enable 0: Disabled 1: Enabled
5	GPIO5_INPUT_EN	R/W	1	GPIO5 Input Enable 0: Disabled 1: Enabled
4	GPIO4_INPUT_EN	R/W	1	GPIO4 Input Enable 0: Disabled 1: Enabled
3	GPIO3_INPUT_EN	R/W	1	GPIO3 Input Enable 0: Disabled 1: Enabled

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Table 7-33. GPIO_INPUT_CTL Register (Address 0x0F) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
2	GPIO2_INPUT_EN	R/W	1	GPIO2 Input Enable 0: Disabled 1: Enabled
1	GPIO1_INPUT_EN	R/W	1	GPIO1 Input Enable 0: Disabled 1: Enabled
0	GPIO0_INPUT_EN	R/W	1	GPIO0 Input Enable 0: Disabled 1: Enabled

7.6.1.17 GPIO0_PIN_CTL Register

Table 7-34. GPIO0_PIN_CTL Register (Address 0x10)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO0_OUT_SEL	R/W	0x0	GPIO0 Output Select Determines the output data for the selected source. If GPIO0_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO0_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO0_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO0_OUT_SRC is set to 11x (one of the CSI-2 Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI-2 TX Port Interrupt 11 : Reserved
4:2	GPIO0_OUT_SRC	R/W	0x0	GPIO0 Output Source Select Selects output source for GPIO0 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI-2 TX Port 0 111 : Reserved
1	GPIO0_OUT_VAL	R/W	0	GPIO0 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO0_OUT_EN	R/W	0	GPIO0 Output Enable 0: Disabled 1: Enabled

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7.6.1.18 GPIO1_PIN_CTL Register

Table 7-35. GPIO1_PIN_CTL Register (Address 0x11)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO1_OUT_SEL	R/W	0x0	GPIO1 Output Select Determines the output data for the selected source. If GPIO1_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO1_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO1_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO1_OUT_SRC is set to 11x (one of the CSI-2 Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI-2 TX Port Interrupt 111 : Reserved
4:2	GPIO1_OUT_SRC	R/W	0x0	GPIO1 Output Source Select Selects output source for GPIO1 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI-2 TX Port 0 111 : Reserved
1	GPIO1_OUT_VAL	R/W	0	GPIO1 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO1_OUT_EN	R/W	0	GPIO1 Output Enable 0: Disabled 1: Enabled

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7.6.1.19 GPIO2_PIN_CTL Register

Table 7-36. GPIO2_PIN_CTL Register (Address 0x12)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO2_OUT_SEL	R/W	0x0	GPIO2 Output Select Determines the output data for the selected source. If GPIO2_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO2_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO2_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO2_OUT_SRC is set to 11x (one of the CSI-2 Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI-2 TX Port Interrupt 111 : Reserved
4:2	GPIO2_OUT_SRC	R/W	0x0	GPIO2 Output Source Select Selects output source for GPIO2 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI-2 TX Port 0 111 : Reserved
1	GPIO2_OUT_VAL	R/W	0	GPIO2 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO2_OUT_EN	R/W	0	GPIO2 Output Enable 0: Disabled 1: Enabled

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7.6.1.20 GPIO3_PIN_CTL Register

Table 7-37. GPIO3_PIN_CTL Register (Address 0x13)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO3_OUT_SEL	R/W	0x0	GPIO3 Output Select Determines the output data for the selected source. If GPIO3_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO3_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO3_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO3_OUT_SRC is set to 11x (one of the CSI-2 Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI-2 TX Port Interrupt 111 : Reserved
4:2	GPIO3_OUT_SRC	R/W	0x0	GPIO3 Output Source Select Selects output source for GPIO3 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI-2 TX Port 0 111 : Reserved
1	GPIO3_OUT_VAL	R/W	0	GPIO3 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO3_OUT_EN	R/W	0	GPIO3 Output Enable 0: Disabled 1: Enabled

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7.6.1.21 GPIO4_PIN_CTL Register

Table 7-38. GPIO4_PIN_CTL Register (Address 0x14)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO4_OUT_SEL	R/W	0x0	GPIO4 Output Select Determines the output data for the selected source. If GPIO4_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO4_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO4_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO4_OUT_SRC is set to 11x (one of the CSI-2 Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI-2 TX Port Interrupt 111 : Reserved
4:2	GPIO4_OUT_SRC	R/W	0x0	GPIO4 Output Source Select Selects output source for GPIO4 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI-2 TX Port 0 111 : Reserved
1	GPIO4_OUT_VAL	R/W	0	GPIO4 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO4_OUT_EN	R/W	0	GPIO4 Output Enable 0: Disabled 1: Enabled

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7.6.1.22 GPIO5_PIN_CTL Register

Table 7-39. GPIO5_PIN_CTL Register (Address 0x15)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO5_OUT_SEL	R/W	0x0	GPIO5 Output Select Determines the output data for the selected source. If GPIO5_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO5_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO5_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO5_OUT_SRC is set to 11x (one of the CSI-2 Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI-2 TX Port Interrupt 111 : Reserved
4:2	GPIO5_OUT_SRC	R/W	0x0	GPIO5 Output Source Select Selects output source for GPIO5 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI-2 TX Port 0 111 : Reserved
1	GPIO5_OUT_VAL	R/W	0	GPIO5 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO5_OUT_EN	R/W	0	GPIO5 Output Enable 0: Disabled 1: Enabled

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7.6.1.23 GPIO6_PIN_CTL Register

Table 7-40. GPIO6_PIN_CTL Register (Address 0x16)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO6_OUT_SEL	R/W	0x0	GPIO6 Output Select Determines the output data for the selected source. If GPIO6_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO6_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO6_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO6_OUT_SRC is set to 11x (one of the CSI-2 Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI-2 TX Port Interrupt 111 : Reserved
4:2	GPIO6_OUT_SRC	R/W	0x0	GPIO6 Output Source Select Selects output source for GPIO6 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI-2 TX Port 0 111 : Reserved
1	GPIO6_OUT_VAL	R/W	0	GPIO6 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO6_OUT_EN	R/W	0	GPIO6 Output Enable 0: Disabled 1: Enabled

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7.6.1.24 GPIO7_PIN_CTL Register

Table 7-41. GPIO7_PIN_CTL Register (Address 0x17)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO7_OUT_SEL	R/W	0x0	GPIO7 Output Select Determines the output data for the selected source. If GPIO7_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110 : Frame Valid signal 111 : Line Valid signal If GPIO7_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO7_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved If GPIO7_OUT_SRC is set to 11x (one of the CSI-2 Transmit ports), the following selections apply: 000 : Pass (AND of selected RX port status) 001 : Pass (OR of selected RX port status) 010 : Frame Valid (sending video frame) 011 : Line Valid (sending video line) 100 : Synchronized - multi-port data is synchronized 101 : CSI-2 TX Port Interrupt 111 : Reserved
4:2	GPIO7_OUT_SRC	R/W	0x0	GPIO7 Output Source Select Selects output source for GPIO7 data: 000 : RX Port 0 001 : RX Port 1 010 : RX Port 2 011 : RX Port 3 100 : Device Status 101 : Reserved 110 : CSI-2 TX Port 0 111 : Reserved
1	GPIO7_OUT_VAL	R/W	0	GPIO7 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO7_OUT_EN	R/W	0	GPIO7 Output Enable 0: Disabled 1: Enabled

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7.6.1.25 FS_CTL Register

Table 7-42. FS_CTL Register (Address 0x18)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	FS_MODE	R/W	0x0	FrameSync Mode 0000: Internal Generated FrameSync, use Back-channel frame clock from port 0 0001: Internal Generated FrameSync, use Back-channel frame clock from port 1 0010: Internal Generated FrameSync, use Back-channel frame clock from port 2 0011: Internal Generated FrameSync, use Back-channel frame clock from port 3 01xx: Internal Generated FrameSync, use 25MHz clock 1000: External FrameSync from GPIO0 1001: External FrameSync from GPIO1 1010: External FrameSync from GPIO2 1011: External FrameSync from GPIO3 1100: External FrameSync from GPIO4 1101: External FrameSync from GPIO5 1110: External FrameSync from GPIO6 1111: External FrameSync from GPIO7
3	FS_SINGLE	R/W/SC	0	Generate Single FrameSync pulse When this bit is set, a single FrameSync pulse is generated. The system should wait for the full duration of the desired pulse before generating another pulse. When using this feature, the FS_GEN_ENABLE bit should remain set to 0. This bit is self-clearing and will always return 0.
2	FS_INIT_STATE	R/W	0	Initial State This register controls the initial state of the FrameSync signal. 0: FrameSync initial state is 0 1: FrameSync initial state is 1
1	FS_GEN_MODE	R/W	0	FrameSync Generation Mode This control selects between Hi/Lo and 50/50 modes. In Hi/Lo mode, the FrameSync generator will use the FS_HIGH_TIME[15:0] and FS_LOW_TIME[15:0] register values to separately control the High and Low periods for the generated FrameSync signal. In 50/50 mode, the FrameSync generator will use the values in the FS_HIGH_TIME_0, FS_LOW_TIME_1 and FS_LOW_TIME_0 registers as a 24-bit value for both the High and Low periods of the generated FrameSync signal. 0: Hi/Lo 1: 50/50
0	FS_GEN_ENABLE	R/W	0	FrameSync Generation Enable 0: Disabled 1: Enabled

7.6.1.26 FS_HIGH_TIME_1 Register

Table 7-43. FS_HIGH_TIME_1 Register (Address 0x19)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FRAMESYNC_HIGH_TIME_1	R/W	0x0	FrameSync High Time bits 15:8 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

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7.6.1.27 FS_HIGH_TIME_0 Register

Table 7-44. FS_HIGH_TIME_0 Register (Address 0x1A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FRAMESYNC_HIGH_TIME_0	R/W	0x0	FrameSync High Time bits 7:0 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

7.6.1.28 FS_LOW_TIME_1 Register

Table 7-45. FS_LOW_TIME_1 Register (Address 0x1B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FRAMESYNC_LOW_TIME_1	R/W	0x0	FrameSync Low Time bits 15:8 The value programmed to the FS_LOW_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_LOW_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

7.6.1.29 FS_LOW_TIME_0 Register

Table 7-46. FS_LOW_TIME_0 Register (Address 0x1C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FRAMESYNC_LOW_TIME_0	R/W	0x0	FrameSync Low Time bits 7:0 The value programmed to the FS_LOW_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_LOW_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

7.6.1.30 MAX_FRM_HI Register

Table 7-47. MAX_FRM_HI Register (Address 0x1D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	MAX_FRAME_HI	R/W	0x0	CSI-2 Maximum Frame Count bits 15:8 In RAW mode operation, the FPD3 Receiver will create CSI-2 video frames. For the Frame Start and Frame End packets of each video frame, a 16-bit frame number field is generated. If the Maximum Frame Count value is set to 0, the frame number is disabled and will always be 0. If Maximum Frame Count value is non-zero, the frame number will increment for each from 1 up to the Maximum Frame Count value before resetting to 1.

7.6.1.31 MAX_FRM_LO Register

Table 7-48. MAX_FRM_LO Register (Address 0x1E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	MAX_FRAME_LO	R/W	0x04	CSI-2 Maximum Frame Count bits 7:0 In RAW mode operation, the FPD3 Receiver will create CSI-2 video frames. For the Frame Start and Frame End packets of each video frame, a 16-bit frame number field is generated. If the Maximum Frame Count value is set to 0, the frame number is disabled and will always be 0. If Maximum Frame Count value is non-zero, the frame number will increment for each from 1 up to the Maximum Frame Count value before resetting to 1.

7.6.1.32 CSI_PLL_CTL Register

Table 7-49. CSI_PLL_CTL Register (Address 0x1F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	RESERVED	-	0x0	Reserved

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Table 7-49. CSI_PLL_CTL Register (Address 0x1F) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
3	SEL_OSC_200M	R/W	0	Select 200MHz Oscillator Clock The external reference clock is normally used to generate the digital and CSI-2 PLL reference clocks. This bit allows the use of the internal 200 MHz always-on oscillator clock instead. 0: Select external reference clock 1: Select internal always-on clock
2	REF_CLK_MODE	R/W	0	Reference Clock mode The digital logic requires a 200 MHz reference clock generated from the CSI-2 PLL. If this bit is set to 1, the reference clock will be 100 MHz. 0 : clock is 200 MHz 1 : clock is 100 MHz This bit should not be set to 1 if CSI_TX_SPEED is set for 400Mbps operation.
1:0	CSI_TX_SPEED	R/W	10	CSI-2 Transmitter Speed select: (See *Section 7.4.19*) Controls the CSI-2 Transmitter frequency. 00 : 1.472 - 1.664 1.5 / 1.6 Gbps serial rate 01 : 1.2 Gbps serial rate Reserved 10 : 800 Mbps serial rate 11 : 400 Mbps serial rate

7.6.1.33 FWD_CTL1 Register

Table 7-50. FWD_CTL1 Register (Address 0x20)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	FWD_PORT3_DIS	R/W	1	Disable forwarding of RX Port 3 0: Forwarding enabled 1: Forwarding disabled
6	FWD_PORT2_DIS	R/W	1	Disable forwarding of RX Port 2 0: Forwarding enabled 1: Forwarding disabled
5	FWD_PORT1_DIS	R/W	1	Disable forwarding of RX Port 1 0: Forwarding enabled 1: Forwarding disabled
4	FWD_PORT0_DIS	R/W	1	Disable forwarding of RX Port 0 0: Forwarding enabled 1: Forwarding disabled
3	Reserved	R/W	0	Reserved
2	Reserved	R/W	0	Reserved
1	Reserved	R/W	0	Reserved
0	Reserved	R/W	0	Reserved

7.6.1.34 FWD_CTL2 Register

Table 7-51. FWD_CTL2 Register (Address 0x21)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	Reserved	R/W	0	Reserved

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Table 7-51. FWD_CTL2 Register (Address 0x21) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
6	FWD_SYNC_AS_AVAIL	R/W	0	Synchronized Forwarding As Available During Synchronized Forwarding, each forwarding engine will wait for video data to be available from each enabled port, prior to sending the video line. Setting this bit to a 1 will allow sending the next video line as it becomes available. For example if RX Ports 0 and 1 are being forwarded, port 0 video line is forwarded when it becomes available, rather than waiting until both ports 0 and ports 1 have video data available. This operation may reduce the likelihood of buffer overflow errors in some conditions. This bit will have no affect in video line concatenation mode and only affects video lines (long packets) rather than synchronization packets. This bit applies to both CSI-2 output ports
5:4	Reserved	R/W	0x0	Reserved
3:2	CSI0_SYNC_FWD	R/W	0x0	Enable synchronized forwarding for CSI-2 output port 0 (see *Section 7.4.25.2*) 00: Synchronized forwarding disabled 01: Basic Synchronized forwarding enabled 10: Synchronous forwarding with line interleaving 11: Synchronous forwarding with line concatenation Only one of CSI0_RR_FWD and CSI0_SYNC_FWD must be enabled at a time.
1	Reserved	R/W	1	Reserved
0	CSI0_RR_FWD	R/W	1	Enable best-effort forwarding for CSI-2 output port 0. When this mode is enabled, no attempt is made to synchronize the video traffic. When multiple sources have data available to forward, the data will tend to be forwarded in a round-robin fashion. 0: Round robin forwarding disabled 1: Round robin forwarding enabled Only one of CSI0_RR_FWD and CSI0_SYNC_FWD must be enabled at a time.

7.6.1.35 FWD_STS Register

Table 7-52. FWD_STS Register (Address 0x22)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	RESERVED	-	0x0	Reserved
3	Reserved	R/RC	0	Reserved
2	FWD_SYNC_FAIL0	R/RC	0	Forwarding synchronization failed for CSI-2 output port 0 During Synchronized forwarding, this flag indicates a failure of synchronized video has been detected. For this bit to be set, the forwarding process must have previously been successful at sending at least one synchronized video frame. 0: No failure 1: Synchronization failure This bit is cleared on read.
1	Reserved	R	0	Reserved
0	FWD_SYNC0	R	0	Forwarding synchronized for CSI-2 output port 0 During Synchronized forwarding, this bit indicates that the forwarding engine is currently able to provide synchronized video from enabled Receive ports. This bit will always be 0 if Synchronized forwarding is disabled. 0: Video is not synchronized 1: Video is synchronized

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7.6.1.36 INTERRUPT_CTL Register

Table 7-53. INTERRUPT_CTL Register (Address 0x23)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	INT_EN	R/W	0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.
6	RESERVED	-	0	Reserved
5	Reserved	R/W	0	Reserved
4	IE_CSI_TX	R/W	0	CSI-2 Transmit Port Interrupt: Enable interrupt from CSI-2 Transmitter Port.
3	IE_RX3	R/W	0	RX Port 3 Interrupt: Enable interrupt from Receiver Port 3.
2	IE_RX2	R/W	0	RX Port 2 Interrupt: Enable interrupt from Receiver Port 2.
1	IE_RX1	R/W	0	RX Port 1 Interrupt: Enable interrupt from Receiver Port 1.
0	IE_RX0	R/W	0	RX Port 0 Interrupt: Enable interrupt from Receiver Port 0.

7.6.1.37 INTERRUPT_STS Register

Table 7-54. INTERRUPT_STS Register (Address 0x24)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	INT	R	0	Global Interrupt: Set if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INT_EN bit in the INTERRUPT_CTL register but does depend on the IE_xxx bits. For example, if IE_RX0 and IS_RX0 are both asserted, the INT bit is set to 1.
6	RESERVED	-	0	Reserved
5	Reserved	R	0	Reserved
4	IS_CSI_TX	R	0	CSI-2 Transmit Port Interrupt: An interrupt has occurred for CSI-2 Transmitter Port. This interrupt is cleared upon reading the CSI_TX_ISR register for CSI-2 Transmit Port.
3	IS_RX3	R	0	RX Port 3 Interrupt: This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
2	IS_RX2	R	0	RX Port 2 Interrupt: An interrupt has occurred for Receive Port 2. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
1	IS_RX1	R	0	RX Port 1 Interrupt: 0x An interrupt has occurred for Receive Port 1. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
0	IS_RX0	R	0	RX Port 0 Interrupt: An interrupt has occurred for Receive Port 0. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.

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7.6.1.38 TS_CONFIG Register

Table 7-55. TS_CONFIG Register (Address 0x25)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	-	0	Reserved
6	FS_POLARITY	R/W	0	Framesync Polarity Indicates active edge of FrameSync signal 0: Rising edge 1: Falling edge
5:4	TS_RES_CTL	R/W	0x0	Timestamp Resolution Control 00: 40 ns 01: 80 ns 10: 160 ns 11: 1.0 us
3	TS_AS_AVAIL	R/W	0	Timestamp Ready Control 0: Normal operation 1: Indicate timestamps ready as soon as all port timestamps are available
2	RESERVED	-	0	Reserved
1	TS_FREERUN	R/W	0	FreeRun Mode 0: FrameSync mode 1: FreeRun mode
0	TS_MODE	R/W	0	Timestamp Mode 0: Line start 1: Frame start

7.6.1.39 TS_CONTROL Register

Table 7-56. TS_CONTROL Register (Address 0x26)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	-	0x0	Reserved
4	TS_FREEZE	R/W	0	Freeze Timestamps 0: Normal operation 1: Freeze timestamps Setting this bit will freeze timestamps and clear the TS_READY flag. The TS_FREEZE bit should be cleared after reading timestamps to resume operation.
3	TS_ENABLE3	R/W	0	Timestamp Enable RX Port 3 0: Disabled 1: Enabled
2	TS_ENABLE2	R/W	0	Timestamp Enable RX Port 2 0: Disabled 1: Enabled
1	TS_ENABLE1	R/W	0	Timestamp Enable RX Port 1 0: Disabled 1: Enabled
0	TS_ENABLE0	R/W	0	Timestamp Enable RX Port 0 0: Disabled 1: Enabled

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7.6.1.40 TS_LINE_HI Register

Table 7-57. TS_LINE_HI Register (Address 0x27)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TS_LINE_HI	R/W	0x0	Timestamp Line, upper 8 bits This field is the line number at which to capture the timestamp when Line Start mode is enabled. For proper operation, the line number should be set to a value greater than 1. During Frame Start mode, if TS_FREERUN is set, the TS_LINE value is used to determine when to begin checking for Frame Start

7.6.1.41 TS_LINE_LO Register

Table 7-58. TS_LINE_LO Register (Address 0x28)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TS_LINE_LO	R/W	0x0	Timestamp Line, lower 8 bits This field is the line number at which to capture the timestamp when Line Start mode is enabled. For proper operation, the line number should be set to a value greater than 1. During Frame Start mode, if TS_FREERUN is set, the TS_LINE value is used to determine when to begin checking for Frame Start

7.6.1.42 TS_STATUS Register

Table 7-59. TS_STATUS Register (Address 0x29)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	-	0x0	Reserved
4	TS_READY	R	0	Timestamp Ready This flag indicates when timestamps are ready to be read. This flag is cleared when the TS_FREEZE bit is set.
3	TS_VALID3	R	0	Timestamp Valid, RX Port 3
2	TS_VALID2	R	0	Timestamp Valid, RX Port 2
1	TS_VALID1	R	0	Timestamp Valid, RX Port 1
0	TS_VALID0	R	0	Timestamp Valid, RX Port 0

7.6.1.43 TIMESTAMP_P0_HI Register

Table 7-60. TIMESTAMP_P0_HI Register (Address 0x2A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TIMESTAMP_P0_HI	R	0x0	Timestamp, upper 8 bits, RX Port 0

7.6.1.44 TIMESTAMP_P0_LO Register

Table 7-61. TIMESTAMP_P0_LO Register (Address 0x2B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TIMESTAMP_P0_LO	R	0x0	Timestamp, lower 8 bits, RX Port 0

7.6.1.45 TIMESTAMP_P1_HI Register

Table 7-62. TIMESTAMP_P1_HI Register (Address 0x2C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TIMESTAMP_P1_HI	R	0x0	Timestamp, upper 8 bits, RX Port 1

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7.6.1.46 TIMESTAMP_P1_LO Register

Table 7-63. TIMESTAMP_P1_LO Register (Address 0x2D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TIMESTAMP_P1_LO	R	0x0	Timestamp, lower 8 bits, RX Port 1

7.6.1.47 TIMESTAMP_P2_HI Register

Table 7-64. TIMESTAMP_P2_HI Register (Address 0x2E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TIMESTAMP_P2_HI	R	0x0	Timestamp, upper 8 bits, RX Port 2

7.6.1.48 TIMESTAMP_P2_LO Register

Table 7-65. TIMESTAMP_P2_LO Register (Address 0x2F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TIMESTAMP_P2_LO	R	0x0	Timestamp, lower 8 bits, RX Port 2

7.6.1.49 TIMESTAMP_P3_HI Register

Table 7-66. TIMESTAMP_P3_HI Register (Address 0x30)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TIMESTAMP_P3_HI	R	0x0	Timestamp, upper 8 bits, RX Port 3

7.6.1.50 TIMESTAMP_P3_LO Register

Table 7-67. TIMESTAMP_P3_LO Register (Address 0x31)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TIMESTAMP_P3_LO	R	0x0	Timestamp, lower 8 bits, RX Port 3

7.6.2 CSI-2 Port Select Register

This register selects access to Digital CSI-2 registers.

Table 7-68. CSI_PORT_SEL Register (Address 0x32)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	-	0x0	Reserved
4	RESERVED	R/W	0	Reserved
3:2	RESERVED	-	0x0	Reserved
1	RESERVED	R/W	0	Reserved
0	RESERVED	R/W	0	Reserved

7.6.3 Digital CSI-2 Registers (Paged)

Use CSI_PORT_SEL (0x32) register to select CSI-2 TX Port 0 or CSI-2 TX Port1 registers.

- CSI-2 TX Port 0:
  - Read: 0x32[4] = 0
  - Write: 0x32[0] = 1
- CSI-2 TX Port 1:
  - Read: 0x32[4] = 1
  - Write: 0x32[1] = 1

7.6.3.1 CSI_CTL Register

CSI-2 TX port-specific register. The CSI-2 Port Select register 0x32 configures which unique CSI-2 TX port registers can be accessed by I2C read and write commands.

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Table 7-69. CSI_CTL Register (Address 0x33)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	-	0	Reserved
6	CSI_CAL_EN	R/W	0	Enable initial CSI-2 Skew-Calibration sequence When the initial skew-calibration sequence is enabled, the CSI-2 Transmitter will send the sequence at initialization, prior to sending any HS data. This bit should be set when operating at 1.6 Gbps CSI-2 speed (as configured in the CSI_PLL register). 0: Disabled 1: Enabled
5:4	CSI_LANE_COUNT	R/W	0x0	CSI-2 lane count 00: 4 lanes 01: 3 lanes 10: 2 lanes 11: 1 lane
3:2	CSI_ULP	R/W	0	Force LP00 state on data/clock lanes 00: Normal operation 01: LP00 state forced only on data lanes 10: Reserved 11: LP00 state forced on data and clock lanes
1	CSI_CONTS_CLOCK	R/W	0	Enable CSI-2 continuous clock mode 0: Disabled 1: Enabled NOTE: When enabled, the CSI-2 Transmitter will enter continuous clock mode upon transmission of the first packet
0	CSI_ENABLE	R/W	0	Enable CSI-2 output 0: Disabled 1: Enabled NOTE: Forwarding should be disabled (via the FWD_CTL1 register) prior to enabling or disabling the CSI-2 output.

7.6.3.2 CSI_CTL2 Register

CSI-2 TX port-specific register. The CSI-2 Port Select register 0x32 configures which unique CSI-2 TX port registers can be accessed by I2C read and write commands.

Table 7-70. CSI_CTL2 Register (Address 0x34)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	RESERVED	-	0x0	Reserved
3	CSI_PASS_MODE	R/W	0	CSI-2PASS indication mode Determines whether the CSI-2 Pass indication is for a single port or all enabled ports. 0 : Assert PASS if at least one enabled Receive port is providing valid video data 1 : Assert PASS only if ALL enabled Receive ports are providing valid video data
2	CSI_CAL_INV	R/W	0	CSI-2 Calibration Inverted Data pattern During the CSI-2 skew-calibration pattern, the CSI-2 Transmitter will send a sequence of 01010101 data (first bit 0). Setting this bit to a 1 will invert the sequence to 10101010 data.
1	CSI_CAL_SINGLE	R/W/SC	0	Enable single periodic CSI-2 Skew-Calibration sequence Setting this bit will send a single skew-calibration sequence from the CSI-2 Transmitter. The skew-calibration sequence is the 2^{10} bit sequence required for periodic calibration. The calibration sequence is sent at the next idle period on the CSI-2 interface. This bit is self-clearing and will reset to 0 after the calibration sequence is sent.

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Table 7-70. CSI_CTL2 Register (Address 0x34) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	CSI_CAL_PERIODIC	R/W	0	Enable periodic CSI-2 Skew-Calibration sequence When the periodic skew-calibration sequence is enabled, the CSI-2 Transmitter will send the periodic skew-calibration sequence following the sending of Frame End packets. 0: Disabled 1: Enabled

7.6.3.3 CSI_STS Register

CSI-2 TX port-specific register. The CSI-2 Port Select register 0x32 configures which unique CSI-2 TX port registers can be accessed by I2C read and write commands.

Table 7-71. CSI_STS Register (Address 0x35)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	-	0x0	Reserved
4	TX_PORT_NUM	R	0	TX Port Number This read-only field indicates the number of the currently selected TX read port.
3:2	RESERVED	-	0x0	Reserved
1	TX_PORT_SYNC	R	0	TX Port Synchronized This bit indicates the CSI-2 Transmit Port is able to properly synchronize input data streams from multiple sources. This bit is 0 if synchronization is disabled via the FWD_CTL2 register. 0 : Input streams are not synchronized 1 : Input streams are synchronized
0	TX_PORT_PASS	R	0	TX Port Pass Indicates valid data is available on at least one port, or on all ports if configured for all port status via the CSI_PASS_MODE bit in the CSI_CTL2 register. The function differs based on mode of operation. In asynchronous operation, the TX_PORT_PASS indicates the CSI-2 port is actively delivering valid video data. The status is cleared based on detection of an error condition that interrupts transmission. During Synchronized forwarding, the TX_PORT_PASS indicates valid data is available for delivery on the CSI-2 TX output. Data may not be delivered if ports are not synchronized. The TX_PORT_SYNC status is a better indicator that valid data is being delivered to the CSI-2 transmit port.

7.6.3.4 CSI_TX_ICR Register

CSI-2 TX port-specific register. The CSI-2 Port Select register 0x32 configures which unique CSI-2 TX port registers can be accessed by I2C read and write commands.

Table 7-72. CSI_TX_ICR Register (Address 0x36)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	-	0x0	Reserved
4	IE_RX_PORT_INT	R/W	0	RX Port Interrupt Enable Enable interrupt based on receiver port interrupt for the RX Ports being forwarded to the CSI-2 Transmit Port.
3	IE_CSI_SYNC_ERROR	R/W	0	CSI-2 Sync Error interrupt Enable Enable interrupt on CSI-2 Synchronization enable.
2	IE_CSI_SYNC	R/W	0	CSI-2 Synchronized interrupt Enable Enable interrupts on CSI-2 Transmit Port assertion of CSI-2 Synchronized Status.
1	IE_CSI_PASS_ERROR	R/W	0	CSI-2 RX Pass Error interrupt Enable Enable interrupt on CSI-2 Pass Error
0	IE_CSI_PASS	R/W	0	CSI-2 Pass interrupt Enable Enable interrupt on CSI-2 Transmit Port assertion of CSI-2 Pass.

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7.6.3.5 CSI_TX_ISR Register

CSI-2 TX port-specific register. The CSI-2 Port Select register 0x32 configures which unique CSI-2 TX port registers can be accessed by I2C read and write commands.

Table 7-73. CSI_TX_ISR Register (Address 0x37)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	-	0x0	Reserved
4	IS_RX_PORT_INT	R/RC	0	RX Port Interrupt A Receiver port interrupt has been generated for one of the RX Ports being forwarded to the CSI-2 Transmit Port. A read of the associated port receive status registers will clear this interrupt. See the PORT_ISR_HI and PORT_ISR_LO registers for details.
3	IS_CSI_SYNC_ERROR	R/RC	0	CSI-2 Sync Error interrupt A synchronization error has been detected for multiple video stream inputs to the CSI-2 Transmitter.
2	IS_CSI_SYNC	R/RC	0	CSI-2 Synchronized interrupt CSI-2 Transmit Port assertion of CSI-2 Synchronized Status. Current status for CSI-2 Sync can be read from the TX_PORT_SYNC flag in the CSI_STS register.
1	IS_CSI_PASS_ERROR	R/RC	0	CSI-2 RX Pass Error interrupt A deassertion of CSI-2 Pass has been detected on one of the RX Ports being forwarded to the CSI-2 Transmit Port
0	IS_CSI_PASS	R/RC	0	CSI-2 Pass interrupt CSI-2 Transmit Port assertion of CSI-2 Pass detected. Current status for the CSI-2 Pass indication can be read from the TX_PORT_PASS flag in the CSI_STS register

7.6.3.6 RESERVED Register

Table 7-74. RESERVED Register (Address 0x38)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x0	Reserved

7.6.3.7 RESERVED Register

Table 7-75. RESERVED Register (Address 0x39)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x0	Reserved

7.6.3.8 RESERVED Register

Table 7-76. RESERVED Register (Address 0x3A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x0	Reserved

7.6.4 RESERVED Registers

Table 7-77. RESERVED Registers (Address 0x3B - 0x3F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x0	Reserved

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7.6.5 AEQ Registers (Shared)

7.6.5.1 RESERVED Register

Table 7-78. RESERVED Register (Address 0x40)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x0	Reserved

7.6.5.2 SFILTER_CFG Register

Table 7-79. SFILTER_CFG Register (Address 0x41)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	SFILTER_MAX	R/W	0xA	SFILTER Maximum Setting This field controls the maximum SFILTER setting. Allowed values are 0-14 with 7 being the mid point. These values are used for both AEQ adaption and dynamic SFILTER control. The maximum setting must be greater than of equal to the SFILTER_MIN.
3:0	SFILTER_MIN	R/W	0x9	SFILTER Minimum Setting This field controls the minimum SFILTER setting. Allowed values are 0-14, where 7 is the mid point. These values are used for both AEQ adaption and dynamic SFILTER control. The minimum setting must be less than or equal to the SFILTER_MAX

7.6.5.3 AEQ_CTL Register

Table 7-80. AEQ_CTL Register (Address 0x42)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	-	0	Reserved
6:4	AEQ_ERR_CTL	R/W	0x7	AEQ Error Control Setting any of these bits will enable FPD3 error checking during the Adaptive Equalization process. Errors are accumulated over 1/2 of the period of the timer set by the ADAPTIVE_EQ_RELOCK_TIME filed in the AEQ_TEST register. If the number of errors is greater than the programmed threshold (AEQ_ERR_THOLD), the AEQ will attempt to increase the EQ setting. The errors may also be checked as part of EQ setting validation if AEQ_2STEP_EN is set. The following errors are checked based on this three bit field: [2] FPD3 clk1/clk0 errors [1] DCA sequence errors [0] Parity errors
3	AEQ_SFIL_ORDER	R/W	0	AEQ SFILTER Adapt order This bit controls the order of adaption for SFILTER values during Adaptive Equalization. 0 : Default order, start at largest clock delay 1 : Start at midpoint, no additional clock or data delay
2	AEQ_2STEP_EN	R/W	0	AEQ 2-step enable This bit enables a two-step operation as part of the Adaptive EQ algorithm. If disabled, the state machine will wait for a programmed period of time, then check status to determine if setting is valid. If enabled, the state machine will wait for 1/2 the programmed period, then check for errors over an additional 1/2 the programmed period. If errors occur during the 2nd step, the state machine will immediately move to the next setting. 0 : Wait for full programmed delay, then check instantaneous lock value 1 : Wait for 1/2 programmed time, then check for errors over 1/2 programmed time. The programmed time is controlled by the ADAPTIVE_EQ_RELOCK_TIME field in the AEQ_TEST register
1	AEQ_OUTER_LOOP	R/W	0	AEQ outer loop control This bit controls whether the Equalizer or SFILTER adaption is the outer loop when the AEQ adaption includes SFILTER adaption. 0 : AEQ is inner loop, SFILTER is outer loop 1 : AEQ is outer loop, SFILTER is inner loop

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Table 7-80. AEQ_CTL Register (Address 0x42) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	AEQ_SFILTER_EN	R/W	1	Enable SFILTER Adaption with AEQ Setting this bit allows SFILTER adaption as part of the Adaptive Equalizer algorithm.

7.6.5.4 AEQ_ERR_THOLD Register

Table 7-81. AEQ_ERR_THOLD Register (Address 0x43)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	AEQ_ERR _THRESHOLD	R/W	0x1	AEQ Error Threshold This register controls the error threshold to determine when to re-adapt the EQ settings. This register should not be programmed to a value of 0.

7.6.5.5 RESERVED Register

Table 7-82. RESERVED Register (Address 0x44)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0	Reserved

7.6.5.6 RESERVED Register

Table 7-83. RESERVED Register (Address 0x45)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x0	Reserved

7.6.6 Digital RX Port Registers

Use FPD3_PORT_SEL (0x4C) register to select digital RX Port 0, RX Port1, RX Port 2, or RX Port 3 registers.

- FPD3 RX Port 0:
  - Read: 0x4C[5:4] = 00
  - Write: 0x4C[0] = 1
- FPD3 RX Port 1:
  - Read: 0x4C[5:4] = 01
  - Write: 0x4C[1] = 1
- FPD3 RX Port 2:
  - Read: 0x4C[5:4] = 10
  - Write: 0x4C[2] = 1
- FPD3 RX Port 3:
  - Read: 0x4C[5:4] = 11
  - Write: 0x4C[3] = 1

7.6.6.1 BCC_ERR_CTL Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-84. BCC_ERR_CTL Register (Address 0x46)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	BCC_ACK_REMOTE_READ	R/W	0	Enable Control Channel to acknowledge start of remote read. When operating with a link partner that supports Enhanced Error Checking for the Bidirectional Control Channel, setting this bit allows the Deserializer to generate an internal acknowledge to the beginning of a remote I2C slave read. This allows additional error detection at the Serializer. This bit should not be set when operating with Serializers that do not support Enhanced Error Checking. 0: Disable 1: Enable
6	BCC_EN_DATA_CHK	R/W	0	Enable checking of returned data Enhanced Error checking can check for errors on returned data during an acknowledge cycle for data sent to remote devices over the Bidirectional Control Channel. In addition, If an error is detected, this register control will allow changing a remote Ack to a Nack to indicate the data error on the local I2C interface. This bit should not be set when operating with Serializers that do not support Enhanced Error checking as they will not always return the correct data during an Ack. 0: Disable returned data error detection 1: Enable returned data error detection
5	BCC_EN_ENH_ERROR	R/W	1	Enable Enhanced Error checking in Bidirectional Control Channel The Bidirectional Control Channel can detect certain error conditions and terminate transactions if an error is detected. This capability can be disabled by setting this bit to 0. 0: Disable Enhanced Error checking 1: Enable Enhanced Error checking
4:3	FORCE_BCC_ERROR	R/W	0x0	BCC Force Error The BCC Force Error control causes an error to be forced on the BCC over the back channel. 00 : No error 01 : Force CRC Error on BCC frame = BCC_FRAME_SEL 10 : Force CRC Error on normal frame following BCC frame = BCC_FRAME_SEL 11 : FORCE Data Error on BCC frame = BCC_FRAME_SEL Setting this control generates a single error on the back channel signaling.
2:0	BCC_FRAME_SEL	R/W	0x0	BCC Frame Select The BCC Frame Select allows selection of the forward channel BCC frame which will include the error condition selected in the force control bits of this register. BCC transfers are sent in bytes for each block transferred. This value may be set in range of 0 to 7 to force an error on any of the first 8 bytes sent on the BCC forward channel.

7.6.6.2 BCC_STATUS Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-85. BCC_STATUS Register (Address 0x47)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	-	0x0	Reserved
5	BCC_SEQ_ERROR	R/RC	0	Bidirectional Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. If BCC_EN_ENH_ERR is 0 (disabled), this register is read-only copy of the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register. If BCC_EN_ENH_ERR is 1 (enabled), this register is cleared on read of this register.
4	BCC_MASTER_ERR	R/RC	0	BCC Master Error This flag indicates a Forward Channel BCC Sequence, BCC CRC, or Lock error occurred while waiting for a response from the Serializer while the BCC I2C Master is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.

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Table 7-85. BCC_STATUS Register (Address 0x47) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
3	BCC_MASTER_TO	R/RC	0	BCC Master Timeout Error This bit will be set if the BCC Watchdog Timer expires while waiting for a response from the Serializer while the BCC I2C Master is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.
2	BCC_SLAVE_ERR	R/RC	0	BCC Slave Error This flag indicates a Forward Channel BCC Sequence, BCC CRC, or Lock error occurred while waiting for a response from the Serializer while the BCC I2C Slave is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.
1	BCC_SLAVE_TO	R/RC	0	BCC Slave Timeout Error This bit will be set if the BCC Watchdog Timer expires will waiting for a response from the Serializer while the BCC I2C Slave is active. This flag is cleared on read of this register.
0	BCC_RESP_ERR	R/RC	0	BCC Response Error This flag indicates an error has been detected in response to a command on the Bidirectional Control Channel. When the I2C Slave is active, the Serializer should return data written (I2C address, offset, or data). When the I2C Slave is active, the Serializer should return data read. The BCC function checks the returned data for errors, and will set this flag if an error is detected. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.

7.6.6.3 RESERVED Register

Table 7-86. RESERVED (Address 0x48)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x00	Reserved

7.6.6.4 RESERVED Register

Table 7-87. RESERVED (Address 0x49)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x00	Reserved

7.6.6.5 FPD3_CAP Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Recommend to set bit four in the FPD-Link III capabilities register to one in order to flag errors detected from enhanced CRC on encoded link control information. The FPD-Link III Encoder CRC must also be enabled by setting the FPD3_ENC_CRC_DIS (register 0xBA[7]) to 0.

Table 7-88. FPD3_CAP (Address 0x4A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	-	0x0	Reserved
4	FPD3_ENC_CRC_CAP	R/W	0	0: Disable CRC error flag from FPD-Link III encoder 1: Disable CRC error flag from FPD-Link III encoder (recommended)
3:0	RESERVED	-	0x0	Reserved

7.6.6.6 RAW_EMBED_DTYPE Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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When the receiver is programmed for Raw mode data, this register field allows setting the Data Type field for the first N lines to indicated embedded non-image data. RAW_EMBED_DTYPE has no effect on CSI-2 receiver modes.

Table 7-89. RAW_EMBED_DTYPE (Address 0x4B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	EMBED_DTYPE _EN	R/W	00	Embedded Data Type Enable. 00 : All long packets will be forwarded as RAW10 or RAW12 video data 01, 10, or 11 : Send first N long packets (1, 2, or 3) as Embedded data using the data type in the EMBED_DTYPE_ID field of this register. This control has no effect if the Receiver is programmed to receive CSI-2 formatted data.
5:0	EMBED_DTYPE _ID	R/W	0x12	Embedded Data Type. If sending embedded data is enabled via the EMBED_DTYPE_EN control in this register, the Data Type field for the first N lines of each frame will use this value rather than the value programmed in the RAW12_ID or RAW10_ID registers. The default setting matches the CSI-2 specification for Embedded 8-bit non Image Data

7.6.6.7 FPD3_PORT_SEL Register

The FPD-Link III Port Select register configures which port is accessed in I2C commands to unique Rx Port registers 0x4D - 0x7F and 0xD0 - 0xDF. A 2-bit RX_READ_PORT field provides for reading values from a single port. The RX_WRITE_PORT fields provide individual enables for each port, allowing simultaneous writes broadcast to all of the FPD-Link III Receive port register blocks in unison. The DS90UB662-Q1 maintains separate page control, preventing conflict between sources.

Table 7-90. FPD3_PORT_SEL Register (Address 0x4C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	PHYS_PORT_NUM	R	0x0 Port#	Physical port number This field provides the physical port connection when reading from a remote device via the Bi-directional Control Channel. When accessed via local I2C interfaces, the value returned is always 0. When accessed via Bi-directional Control Channel, the value returned is the port number of the Receive port connection.
5:4	RX_READ_PORT	R/W	0x0 Port#	Select RX port for register read This field selects one of the four RX port register blocks for readback. This applies to all paged FPD3 Receiver port registers. 00: Port 0 registers 01: Port 1 registers 10: Port 2 registers 11: Port 3 registers When accessed via local I2C interfaces, the default setting is 0. When accessed via Bi-directional Control Channel, the default value is the port number of the Receive port connection.
3	RX_WRITE_PORT_3	R/W	0 1 for RX Port 3	Write Enable for RX port 3 registers This bit enables writes to RX port 3 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bi-directional Control Channel, the default value is 1 if accessed over RX port 3.
2	RX_WRITE_PORT_2	R/W	0 1 for RX Port 2	Write Enable for RX port 2 registers This bit enables writes to RX port 2 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bi-directional Control Channel, the default value is 1 if accessed over RX port 2.

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Table 7-90. FPD3_PORT_SEL Register (Address 0x4C) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
1	RX_WRITE_PORT_1	R/W	0 1 for RX Port 1	Write Enable for RX port 1 registers This bit enables writes to RX port 1 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bi-directional Control Channel, the default value is 1 if accessed over RX port 1.
0	RX_WRITE_PORT_0	R/W	0 1 for RX Port 0	Write Enable for RX port 0 registers This bit enables writes to RX port 0 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bi-directional Control Channel, the default value is 1 if accessed over RX port 0.

7.6.6.8 RX_PORT_STS1 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-91. RX_PORT_STS1 Register (Address 0x4D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RX_PORT_NUM	R	0x0	RX Port Number This read-only field indicates the number of the currently selected RX read port.
5	BCC_CRC_ERROR	R/RC	0	Bi-directional Control Channel CRC Error Detected This bit indicates a CRC error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read.
4	LOCK_STS_CHG	R/RC	0	Lock Status Changed This bit is set if a change in receiver lock status has been detected since the last read of this register. Current lock status is available in the LOCK_STS bit of this register This bit is cleared on read.
3	BCC_SEQ_ERROR / BCC_ERROR	R/RC // R	0	The function of this bit depends on the setting of the BCC_EN_ENH_ERR control in the BCC_ERR_CTL register. If BCC_EN_ENH_ERR is 0 (disabled), this register is defined as follows: Bidirectional Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read. If BCC_EN_ENH_ERR is 1 (enabled), this register is defined as follows: Bidirectional Control Channel Error Flag This flag indicates one or more errors have been detected during Bidirectional Control Channel communication with the Deserializer. The BCC_STATUS register contains further information on the type of error detected. This bit will be cleared upon read of the BCC_STATUS register.
2	PARITY_ERROR	R	0	FPD3 parity errors detected This flag is set when the number of parity errors detected is greater than the threshold programmed in the PAR_ERR_THOLD registers. 1: Number of FPD3 parity errors detected is greater than the threshold 0: Number of FPD3 parity errors is below the threshold This bit is cleared when the RX_PAR_ERR_HI/LO registers are cleared.
1	PORT_PASS	R	0	Receiver PASS indication This bit indicates the current status of the Receiver PASS indication. The requirements for setting the Receiver PASS indication are controlled by the PORT_PASS_CTL register. 1: Receive input has met PASS criteria 0: Receive input does not meet PASS criteria

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Table 7-91. RX_PORT_STS1 Register (Address 0x4D) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	LOCK_STS	R	0	FPD-Link III receiver is locked to incoming data 1: Receiver is locked to incoming data 0: Receiver is not locked

7.6.6.9 RX_PORT_STS2 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-92. RX_PORT_STS2 Register (Address 0x4E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	LINE_LEN_UNSTABLE	R/RC	0	Line Length Unstable If set, this bit indicates the line length was detected as unstable during a previous video frame. The line length is considered to be stable if all the lines in the video frame have the same length. This flag will remain set until read.
6	LINE_LEN_CHG	R/RC	0	Line Length Changed 1: Change of line length detected 0: Change of line length not detected This bit is cleared on read.
5	FPD3_ENCODE _ERROR	R/RC	0	FPD3 Encoder error detected If set, this flag indicates an error in the FPD-Link III encoding has been detected by the FPD-Link III receiver. This bit is cleared on read. Note, to detect FP3 Encoder errors, the LINK_ERROR_COUNT must be enabled with a LINK_ERR_THRESH value greater than 1. Otherwise, the loss of Receiver Lock will prevent detection of the Encoder error.
4	BUFFER_ERROR	R/RC	0	Packet buffer error detected. If this bit is set, an overflow condition has occurred on the packet buffer FIFO. 1: Packet Buffer error detected 0: No Packet Buffer errors detected This bit is cleared on read.
3	CSI_ERROR	R	0	CSI-2 Receive error detected See the CSI_RX_STS register for details.
2	FREQ_STABLE	R	0	Frequency measurement stable
1	NO_FPD3_CLK	R	0	No FPD-Link III input clock detected
0	LINE_CNT_CHG	R/RC	0	Line Count Changed 1: Change of line count detected 0: Change of line count not detected This bit is cleared on read.

7.6.6.10 RX_FREQ_HIGH Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-93. RX_FREQ_HIGH Register (Address 0x4F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FREQ_CNT_HIGH	R	0x0	Frequency Counter High Byte (MHz) The Frequency counter reports the measured frequency for the FPD3 Receiver. This portion of the field is the integer value in MHz.

7.6.6.11 RX_FREQ_LOW Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-94. RX_FREQ_LOW Register (Address 0x50)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FREQ_CNT_LOW	R	0x0	Frequency Counter Low Byte (1/256 MHz) The Frequency counter reports the measured frequency for the FPD3 Receiver. This portion of the field is the fractional value in 1/256 MHz.

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7.6.6.12 SENSOR_STS_0 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Sensor Status Register 0 field provides additional status information when paired with a DS90UB633A-Q1 Serializer. This field is automatically loaded from the forward channel.

Table 7-95. SENSOR_STS_0 (Address 0x51)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	-	00	Reserved
5	CSI_ALARM	R	0	Alarm flag for CSI-2 error from serializer
4	BCC_ALARM	R	0	Alarm flag for back channel error from serializer
3	LINK_DETECT _ALARM	R	0	Alarm flag for link detect from serializer
2	TEMP_SENSE _ALARM	R	0	Alarm flag for temp sensor from serializer
1	VOLT1_SENSE _ALARM	R	0	Alarm flag for voltage sensor 1 from serializer
0	VOLT0_SENSE _ALARM	R	0	Alarm flag for voltage sensor 0 from serializer

7.6.6.13 SENSOR_STS_1 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Sensor Status Register 1 field provides additional status information when paired with a DS90UB633A-Q1 Serializer. This field is automatically loaded from the forward channel.

Table 7-96. SENSOR_STS_1 (Address 0x52)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	-	0	Reserved
6:4	VOLT1_SENSE _LEVEL	R	0x0	Voltage sensor sampled value from serializer
3	RESERVED	-	0	Reserved
2:0	VOLT0_SENSE _LEVEL	R	0x0	Voltage sensor sampled value from serializer

7.6.6.14 SENSOR_STS_2 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Sensor Status Register 2 field provides additional status information when paired with a DS90UB633A-Q1 Serializer. This field is automatically loaded from the forward channel.

Table 7-97. SENSOR_STS_2 (Address 0x53)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	RESERVED	-	0	
2:0	TEMP_SENSE _LEVEL	R	0x0	Temperature sensor sampled value from serializer

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7.6.6.15 SENSOR_STS_3 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Sensor Status Register 3 field provides additional status information on the CSI-2 input when paired with a DS90UB633A-Q1 Serializer. This field is automatically loaded from the forward channel.

Table 7-98. SENSOR_STS_3 (Address 0x54)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	-	0	Reserved
4	CSI_ECC_2BIT_ERR	R	0	CSI-2 -2 ECC error flag from serializer
3	CSI_CHKSUM_ERR	R	0	CSI-2 checksum error from serializer
2	CSI_SOT_ERR	R	0	CSI-2 start of transmission error from serializer
1	CSI_SYNC_ERR	R	0	CSI-2 synchronization error from serializer
0	CSI_CNTRL_ERR	R	0	CSI-2 control error from serializer

7.6.6.16 RX_PAR_ERR_HI Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-99. RX_PAR_ERR_HI Register (Address 0x55)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PAR_ERROR_BYTE_1	R	0x0	Number of FPD3 parity errors – 8 most significant bits The parity error counter registers return the number of data parity errors that have been detected on the FPD3 Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX PARITY CHECKER ENABLE bit in register 0x2 prior to reading the parity error count registers. This register is cleared upon reading the RX_PAR_ERR_LO register.

7.6.6.17 RX_PAR_ERR_LO Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-100. RX_PAR_ERR_LO Register (Address 0x56)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PAR_ERROR_BYTE_0	R	0x0	Number of FPD3 parity errors – 8 least significant bits The parity error counter registers return the number of data parity errors that have been detected on the FPD3 Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX PARITY CHECKER ENABLE bit in register 0x2 prior to reading the parity error count registers. This register is cleared on read.

7.6.6.18 BIST_ERR_COUNT Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-101. BIST_ERR_COUNT Register (Address 0x57)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	BIST_ERROR_COUNT	R	0x0	Bist Error Count Returns BIST error count

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7.6.6.19 BCC_CONFIG Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-102. BCC_CONFIG Register (Address 0x58)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	I2C_PASS_THROUGH _ALL	R/W	0	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
6	I2C_PASS_THROUGH	R/W	0	I2C Pass-Through to Serializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled
5	AUTO_ACK_ALL	R/W	0	Automatically Acknowledge all I2C writes independent of the forward channel lock state or status of the remote Acknowledge 1: Enable 0: Disable
4	BC_ALWAYS_ON	R/W	1	Back channel enable 1: Back channel is always enabled independent of I2C_PASS_THROUGH and I2C_PASS_THROUGH_ALL 0: Back channel enable requires setting of either I2C_PASS_THROUGH and I2C_PASS_THROUGH_ALL This bit may only be written via a local I2C master.
3	BC_CRC_GENERATOR _ENABLE	R/W	1	Back Channel CRC Generator Enable 0: Disable 1: Enable
2:0	BC_FREQ_SELECT	R/W/S	Strap	Back Channel Frequency Select 000: 2.5 Mbps (default for DS90UB633A-Q1 compatibility) 001: Reserved 010 - 111 : Reserved 010: 10 Mbps 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Deserializer should first be programmed to Auto-Ack operation to avoid a control channel timeout due to lack of response from the Serializer. The 20 Mbps and 100 Mbps modes should not be used when the internal reference clock is running at 100 MHz. This includes operation with either CSI_PLL_CTL:REF_CLK_MODE set to 1 or CSI_PLL_CTL:CSI_TX_SPEED set for 400 Mbps operation.

7.6.6.20 DATAPATH_CTL1 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-103. DATAPATH_CTL1 Register (Address 0x59)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	OVERRIDE_FC _CONFIG	R/W	0	1: Disable loading of the DATAPATH_CTL registers from the forward channel, keeping locally written values intact. 0: Allow forward channel loading of DATAPATH_CTL registers
6:2	RESERVED	-	0x0	Reserved

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Table 7-103. DATAPATH_CTL1 Register (Address 0x59) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
1:0	FC_GPIO_EN	R/W	0x0	Forward Channel GPIO Enable Configures the number of enabled forward channel GPIOs 00: GPIOs disabled 01: One GPIO 10: Two GPIOs 11: Four GPIOs This field is normally loaded from the remote serializer. It can be overwritten if the OVERRIDE_FC_CONFIG bit in this register is 1.

7.6.6.21 DATAPATH_CTL2 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-104. DATAPATH_CTL2 Register (Address 0x5A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x0	Reserved

7.6.6.22 SER_ID Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-105. SER_ID Register (Address 0x5B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SER_ID	R/W	0x0	Remote Serializer ID This field is normally loaded automatically from the remote Serializer.
0	FREEZE_DEVICE_ID	R/W	0	Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID is frozen at the value written.

7.6.6.23 SER_ALIAS_ID Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-106. SER_ALIAS_ID Register (Address 0x5C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SER_ALIAS_ID	R/W	0x0	7-bit Remote Serializer Alias ID Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction is remapped to the address specified in the Slave ID register. A value of 0 in this field disables access to the remote I2C Slave.
0	SER_AUTO_ACK	R/W	0	Automatically Acknowledge all I2C writes to the remote Serializer independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.6.24 SlaveID[0] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-107. SlaveID[0] Register (Address 0x5D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ID0	R/W	0x0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
0	RESERVED	-	0	Reserved.

7.6.6.25 SlaveID[1] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-108. SlaveID[1] Register (Address 0x5E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ID1	R/W	0x0	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
0	RESERVED	-	0	Reserved.

7.6.6.26 SlaveID[2] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-109. SlaveID[2] Register (Address 0x5F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ID2	R/W	0x0	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
0	RESERVED	-	0	Reserved.

7.6.6.27 SlaveID[3] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-110. SlaveID[3] Register (Address 0x60)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ID3	R/W	0x0	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
0	RESERVED	-	0	Reserved.

7.6.6.28 SlaveID[4] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-111. SlaveID[4] Register (Address 0x061)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ID4	R/W	0x0	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
0	RESERVED	-	0	Reserved.

7.6.6.29 SlaveID[5] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-112. SlaveID[5] Register (Address 0x62)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ID5	R/W	0x0	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID5, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
0	RESERVED	-	0	Reserved.

7.6.6.30 SlaveID[6] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-113. SlaveID[6] Register (Address 0x63)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ID6	R/W	0x0	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
0	RESERVED	-	0	Reserved.

7.6.6.31 SlaveID[7] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-114. SlaveID[7] Register (Address 0x64)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ID7	R/W	0x0	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction is remapped to this address before passing the transaction across the Bi-directional Control Channel to the Serializer.
0	RESERVED	-	0	Reserved.

7.6.6.32 SlaveAlias[0] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-115. SlaveAlias[0] Register (Address 0x65)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ALIAS_ID0	R/W	0x0	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_0	R/W	0	Automatically Acknowledge all I2C writes to the remote Slave 0 independent of the forward channel lock state or status of the remote Serializer Acknowledge1: Enable0: Disable

7.6.6.33 SlaveAlias[1] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-116. SlaveAlias[1] Register (Address 0x66)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ALIAS_ID1	R/W	0x0	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_1	R/W	0	Automatically Acknowledge all I2C writes to the remote Slave 1 independent of the forward channel lock state or status of the remote Serializer Acknowledge1: Enable0: Disable

7.6.6.34 SlaveAlias[2] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-117. SlaveAlias[2] Register (Address 0x67)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ALIAS_ID2	R/W	0x0	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_2	R/W	0	Automatically Acknowledge all I2C writes to the remote Slave 2 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.6.35 SlaveAlias[3] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-118. SlaveAlias[3] Register (Address 0x68)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ALIAS_ID3	R/W	0x0	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.

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Table 7-118. SlaveAlias[3] Register (Address 0x68) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	SLAVE_AUTO_ACK_3	R/W	0	Automatically Acknowledge all I2C writes to the remote Slave 3 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.6.36 SlaveAlias[4] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-119. SlaveAlias[4] Register (Address 0x69)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ALIAS_ID4	R/W	0x0	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_4	R/W	0	Automatically Acknowledge all I2C writes to the remote Slave 4 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.6.37 SlaveAlias[5] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-120. SlaveAlias[5] Register (Address 0x6A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ALIAS_ID5	R/W	0x0	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_5	R/W	0	Automatically Acknowledge all I2C writes to the remote Slave 5 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.6.38 SlaveAlias[6] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-121. SlaveAlias[6] Register (Address 0x6B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ALIAS_ID6	R/W	0x0	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_6	R/W	0	Automatically Acknowledge all I2C writes to the remote Slave 6 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

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7.6.6.39 SlaveAlias[7] Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-122. SlaveAlias[7] Register (Address 0x6C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SLAVE_ALIAS_ID7	R/W	0x0	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction is remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_7	R/W	0	Automatically Acknowledge all I2C writes to the remote Slave 7 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.6.40 PORT_CONFIG Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-123. PORT_CONFIG Register (Address 0x6D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	CSI_WAIT_FS1	R/W	0	CSI-2 Wait for FrameStart packet with count 1 The CSI-2 Receiver will wait for a Frame Start packet with count of 1 before accepting other packets This bit has no effect in RAW FPD3 input modes.
6	CSI_WAIT_FS	R/W	1	CSI-2 Wait for FrameStart packet CSI2 Receiver will wait for a Frame Start packet before accepting other packets This bit has no effect in RAW FPD3 input modes.
5	CSI_FWD_CKSUM	R/W	1	Forward CSI-2 packets with checksum errors 0: Do not forward errored packets 1: Forward errored packets This bit has no effect in RAW FPD3 input modes.
4	CSI_FWD_ECC	R/W	1	Forward CSI-2 packets with ECC errors 0: Do not forward errored packets 1: Forward errored packets
3	DISCARD_1ST_LINE _ON_ERR / CSI_FWD_LEN	R/W	1	In RAW Mode, Discard first video line if FV to LV setup time is not met. 0 : Forward truncated 1st video line 1 : Discard truncated 1st video line In FPD3 CSI-2 Mode, Forward CSI-2 packets with length errors 0: Do not forward errored packets 1: Forward errored packets
2	RESERVED	R/W/S	Strap	Reserved.
1:0	FPD3_MODE	R/W/S	Strap	FPD3 Input Mode 00: Reserved 00: Reserved 01: RAW12 Low Frequency Mode (DS90UB633A-Q1 compatible) 10: RAW12 High Frequency Mode(DS90UB633A-Q1 compatible) 11: RAW10 Mode (DS90UB633A-Q1 compatible)

7.6.6.41 BC_GPIO_CTL0 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-124. BC_GPIO_CTL0 Register (Address 0x6E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	BC_GPIO1_SEL	R/W	0x8	Back channel GPIO1 Select: Determines the data sent on GPIO1 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO1_SEL[2:0] 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved
3:0	BC_GPIO0_SEL	R/W	0x8	Back channel GPIO0 Select: Determines the data sent on GPIO0 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO0_SEL[2:0] 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved

7.6.6.42 BC_GPIO_CTL1 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-125. BC_GPIO_CTL1 Register (Address 0x6F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	BC_GPIO3_SEL	R/W	0x8	Back channel GPIO3 Select: Determines the data sent on GPIO3 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO3_SEL[2:0] 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved
3:0	BC_GPIO2_SEL	R/W	0x8	Back channel GPIO2 Select: Determines the data sent on GPIO2 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO2_SEL[2:0] 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved

7.6.6.43 RAW10_ID Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

RAW10 virtual channel mapping only applies when FPD-Link III is operating in RAW10 input mode. See register 0x71 for RAW12 and register 0x72 for CSI-2 mode operation.

Table 7-126. RAW10_ID Register (Address 0x70)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RAW10_VC	R/W	<RX Port #>	RAW10 Mode Virtual Channel This field configures the CSI-2 Virtual Channel assigned to the port when receiving RAW10 data. The field value defaults to the FPD-Link III receive port number (0, 1, 2, or 3)
5:0	RAW10_DT	R/W	0x2B	RAW10 DT This field configures the CSI-2 data type used in RAW10 mode. The default of 0x2B matches the CSI-2 specification.

7.6.6.44 RAW12_ID Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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RAW12 virtual channel mapping only applies when FPD-Link III is operating in RAW12 input mode. See register 0x70 for RAW10 and register 0x72 for CSI-2 mode operation.

Table 7-127. RAW12_ID Register (Address 0x71)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RAW12_VC	R/W	<RX Port #>	RAW12 Mode Virtual Channel This field configures the CSI-2 Virtual Channel assigned to the port when receiving RAW12 data. The field value defaults to the FPD-Link III receive port number (0, 1, 2, or 3)
5:0	RAW12_DT	R/W	0x2C	RAW12 DT This field configures the CSI-2 data type used in RAW12 mode. The default of 0x2C matches the CSI-2 specification.

7.6.6.45 CSI_VC_MAP Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

CSI-2 virtual channel mapping only applies when FPD-Link III operating in CSI-2 input mode. See registers 0x70 and 0x71 for RAW mode operation.

Table 7-128. CSI_VC_MAP Register (Address 0x72)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_VC_MAP	R/W	0xE4	CSI-2 Virtual Channel Mapping Register This register provides a method for replacing the Virtual Channel Identifier (VC-ID) of incoming CSI-2 packets. [7:6] : Map value for VC-ID of 3 [5:4] : Map value for VC-ID of 2 [3:2] : Map value for VC-ID of 1 [1:0] : Map value for VC-ID of 0

7.6.6.46 LINE_COUNT_1 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-129. LINE_COUNT_1 Register (Address 0x73)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LINE_COUNT_HI	R	0x0	High byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value is frozen until read.

7.6.6.47 LINE_COUNT_0 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-130. LINE_COUNT_0 Register (Address 0x74)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LINE_COUNT_LO	R	0x0	Low byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value is frozen until read. In addition, when reading the LINE_COUNT registers, the LINE_COUNT_LO is latched upon reading LINE_COUNT_HI to ensure consistency between the two portions of the Line Count.

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7.6.6.48 LINE_LEN_1 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-131. LINE_LEN_1 Register (Address 0x75)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LINE_LEN_HI	R	0	High byte of Line Length The Line Length reports the line length recorded during the most recent video frame. If line length is not stable during the frame, this register will report the length of the last line in the video frame. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value is frozen until read.

7.6.6.49 LINE_LEN_0 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-132. LINE_LEN_0 Register (Address 0x76)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LINE_LEN_LO	R	0	Low byte of Line Length The Line Length reports the length of the most recent video line. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value is frozen until read. In addition, when reading the LINE_LEN registers, the LINE_LEN_LO is latched upon reading LINE_LEN_HI to ensure consistency between the two portions of the Line Length.

7.6.6.50 FREQ_DET_CTL Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-133. FREQ_DET_CTL Register (Address 0x77)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	FREQ_HYST	R/W	0x3	Frequency Detect Hysteresis The Frequency detect hysteresis setting allows ignoring minor fluctuations in frequency. A new frequency measurement will be captured only if the measured frequency differs from the current measured frequency by more than the FREQ_HYST setting. The FREQ_HYST setting is in MHz.
5:4	FREQ_STABLE_THR	R/W	0x0	Frequency Stable Threshold The Frequency detect circuit can be used to detect a stable clock frequency. The Stability Threshold determines the amount of time required for the clock frequency to stay within the FREQ_HYST range to be considered stable: 00 : 40us 01 : 80us 10 : 320us 11 : 1.28ms
3:0	FREQ_LO_THR	R/W	0x5	Frequency Low Threshold Sets the low threshold for the Clock frequency detect circuit in MHz. If the input clock is below this threshold, the NO_FPD3_CLK status will be set to 1.

7.6.6.51 MAILBOX_0 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-134. MAILBOX_0 Register (Address 0x78)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	MAILBOX_0	R/W	0x0	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link.

7.6.6.52 MAILBOX_1 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-135. MAILBOX_1 Register (Address 0x79)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	MAILBOX_1	R/W	0x01	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link.

7.6.6.53 CSI_RX_STS Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-136. CSI_RX_STS Register (Address 0x7A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	RESERVED	-	0x0	Reserved
3	LENGTH_ERR	R/RC	0	Packet Length Error detected for received CSI-2 packet If set, this bit indicates a packet length error was detected on at least one CSI-2 packet received from the sensor. Packet length errors occur if the data length field in the packet header does not match the actual data length for the packet. 1: One or more Packet Length errors have been detected 0: No Packet Length errors have been detected This bit is cleared on read.
2	CKSUM_ERR	R/RC	0	Data Checksum Error detected for received CSI-2 packet If set, this bit indicates a data checksum error was detected on at least one CSI-2 packet received from the sensor. Data checksum errors indicate an error was detected in the packet data portion of the CSI-2 packet. 1: One or more Data Checksum errors have been detected 0: No Data Checksum errors have been detected This bit is cleared on read.
1	ECC2_ERR	R/RC	0	2-bit ECC Error detected for received CSI-2 packet If set, this bit indicates a multi-bit ECC error was detected on at least one CSI-2 packet received from the sensor. Multi-bit errors are not corrected by the device. 1: One or more multi-bit ECC errors have been detected 0: No multi-bit ECC errors have been detected This bit is cleared on read.
0	ECC1_ERR	R/RC	0	1-bit ECC Error detected for received CSI-2 packet If set, this bit indicates a single-bit ECC error was detected on at least one CSI-2 packet received from the sensor. Single-bit errors are corrected by the device. 1: One or more 1-bit ECC errors have been detected 0: No 1-bit ECC errors have been detected This bit is cleared on read.

7.6.6.54 CSI_ERR_COUNTER Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-137. CSI_ERR_COUNTER Register (Address 0x7B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_ERR_CNT	R/RC	0x0	CSI-2 Error Counter Register This register counts the number of CSI-2 packets received with errors since the last read of the counter.

7.6.6.55 PORT_CONFIG2 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-138. PORT_CONFIG2 Register (Address 0x7C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RAW10_8BIT_CTL	R/W	0x0	Raw10 8-bit mode When Raw10 Mode is enabled for the port, the input data is processed as 8-bit data and packed accordingly for transmission over CSI. 00 : Normal Raw10 Mode 01 : Reserved 10 : 8-bit processing using upper 8 bits 11 : 8-bit processing using lower 8 bits
5	DISCARD_ON _PAR_ERR	R/W	1	Discard frames on Parity Error 0 : Forward packets with parity errors 1 : Truncate Frames if a parity error is detected
4	DISCARD_ON _LINE_SIZE	R/W	0	Discard frames on Line Size 0 : Allow changes in Line Size within packets 1 : Truncate Frames if a change in line size is detected
3	DISCARD_ON _FRAME_SIZE	R/W	0	Discard frames on change in Frame Size When enabled, a change in the number of lines in a frame will result in truncation of the packet. The device will resume forwarding video frames based on the PASS_THRESHOLD setting in the PORT_PASS_CTL register. 0 : Allow changes in Frame Size 1 : Truncate Frames if a change in frame size is detected
2	AUTO_POLARITY	R/W	0	Automatic Polarity Detection This register enables automatic polarity detection. When this bit is set, polarity of LineValid and FrameValid will be automatically detected from the incoming data. In this mode, at least one initial frame will be discarded to allow for proper detection of the incoming video. 1 : Automatically detect LV and FV polarity 0 : Use LV_POLARITY and FV_POLARITY register settings to determine polarity
1	LV_POLARITY	R/W	0	LineValid Polarity This register indicates the expected polarity for the LineValid indication received in Raw mode. 1 : LineValid is low for the duration of the video frame 0 : LineValid is high for the duration of the video frame
0	FV_POLARITY	R/W	0	FrameValid Polarity This register indicates the expected polarity for the FrameValid indication received in Raw mode. 1 : FrameValid is low for the duration of the video frame 0 : FrameValid is high for the duration of the video frame

7.6.6.56 PORT_PASS_CTL Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-139. PORT_PASS_CTL Register (Address 0x7D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	PASS_DISCARD_EN	R/W	0	Pass Discard Enable Discard packets if PASS is not indicated. 0 : Ignore PASS for forwarding packets 1 : Discard packets when PASS is not true
6	PASS_CLEAR_CNT	R/W	0	Pass Clear Count Control This bit controls the values read back from the LINE_COUNT_1, LINE_COUNT_0, LINE_LEN_1, and LINE_LEN_0 registers. 0: Registers read back the counter values regardless of the state of the PASS flag 1: Registers read back zero when the PASS flag is de-asserted and the counter values when PASS is asserted
5	PASS_LINE_CNT	R/W	0	Pass Line Count Control This register controls whether the device will include line count in qualification of the Pass indication: 0 : Don't check line count 1 : Check line count When checking line count, Pass is deasserted upon detection of a change in the number of video lines per frame. Pass will not be reasserted until the PASS_THRESHOLD setting is met.
4	PASS_LINE_SIZE	R/W	0	Pass Line Size Control This register controls whether the device will include line size in qualification of the Pass indication: 0 : Don't check line size 1 : Check line size When checking line size, Pass is deasserted upon detection of a change in video line size. Pass will not be reasserted until the PASS_THRESHOLD setting is met.
3	PASS_PARITY_ERR	R/W	0	Parity Error Mode If this bit is set to 0, the port Pass indication is deasserted for every parity error detected on the FPD3 Receive interface. If this bit is set to a 1, the port Pass indication is cleared on a parity error and remain clear until the PASS_THRESHOLD is met.
2	PASS_WDOG_DIS	R/W	0	RX Port Pass Watchdog disable When enabled, if the FPD Receiver does not detect a valid frame end condition within two video frame periods, the Pass indication is deasserted. The watchdog timer will not have any effect if the PASS_THRESHOLD is set to 0. 0 : Enable watchdog timer for RX Pass 1 : Disable watchdog timer for RX Pass
1:0	PASS_THRESHOLD	R/W	0x0	Pass Threshold Register This register controls the number of valid frames before asserting the port Pass indication. If set to 0, PASS is asserted after Receiver Lock detect. If non-zero, PASS is asserted following reception of the programmed number of valid frames.

7.6.6.57 SEN_INT_RISE_CTL Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-140. SEN_INT_RISE_CTL Register (Address 0x7E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SEN_INT_RISE_MASK	R/W	0x0	Sensor Interrupt Rise Mask This register provides the interrupt mask for detecting rising edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in this register, a rising edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in the SEN_INT_RISE_STS register.

7.6.6.58 SEN_INT_FALL_CTL Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-141. SEN_INT_FALL_CTL Register (Address 0x7F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SEN_INT_FALL_MASK	R/W	0x0	Sensor Interrupt Fall Mask This register provides the interrupt mask for detecting falling edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in this register, a falling edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in the SEN_INT_FALL_STS register.

7.6.7 RESERVED Registers

Table 7-142. RESERVED (Address 0x80 - 0x8F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x00	Reserved

7.6.8 Digital CSI-2 Debug Registers (Shared)

7.6.8.1 CSI_FRAME_COUNT_HI Register

Table 7-143. CSI_FRAME_COUNT_HI Register (Address 0x90)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_FRAME_COUNT_HI	R/RC	0x0	CSI-2 Port, Frame Counter MSBs When read, this register returns the value of bits [15:8] of the 16-bit counter csi_frame_count. The LSBs of the counter are sampled into the CSI_FRAME_COUNT_LO register and the counter is cleared.

7.6.8.2 CSI_FRAME_COUNT_LO Register

Table 7-144. CSI_FRAME_COUNT_LO Register (Address 0x91)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_FRAME_COUNT_LO	R	0x0	CSI-2 Port, Frame Counter LSBs When read, this register returns the value of bits [7:0] of the 16-bit counter csi_frame_count. The CSI_FRAME_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

7.6.8.3 CSI_FRAME_ERR_COUNT_HI Register

Table 7-145. CSI_FRAME_ERR_COUNT_HI Register (Address 0x92)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_FRAME_ERR_COUNT_HI	R/RC	0x0	CSI-2 Port, Frame Counter with Errors MSBs When read, this register returns the value of bits [15:8] of the 16-bit counter csi_frame_err_count. The LSBs of the counter are sampled into the CSI_FRAME_ERR_COUNT_LO register and the counter is cleared.

7.6.8.4 CSI_FRAME_ERR_COUNT_LO Register

Table 7-146. CSI_FRAME_ERR_COUNT_LO Register (Address 0x93)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_FRAME_ERR_COUNT_LO	R	0x0	CSI-2 Port, Frame Counter with Errors LSBs When read, this register returns the value of bits [7:0] of the 16-bit counter csi_frame_err_count. The CSI_FRAME_ERR_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

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7.6.8.5 CSI_LINE_COUNT_HI Register

Table 7-147. CSI_LINE_COUNT_HI Register (Address 0x94)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_LINE_COUNT_HI	R/RC	0x0	CSI-2 Port, Line Counter MSBs When read, this register returns the value of bits [15:8] of the 16-bit counter csi_line_count. The LSBs of the counter are sampled into the CSI_LINE_COUNT_LO register and the counter is cleared.

7.6.8.6 CSI_LINE_COUNT_LO Register

Table 7-148. CSI_LINE_COUNT_LO Register (Address 0x95)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_LINE_COUNT_LO	R	0x0	CSI-2 Port, Line Counter LSBs When read, this register returns the value of bits [7:0] of the 16-bit counter csi_line_count. The CSI_LINE_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

7.6.8.7 CSI_LINE_ERR_COUNT_HI Register

Table 7-149. CSI_LINE_ERR_COUNT_HI Register (Address 0x96)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_LINE_ERR _COUNT_HI	R/RC	0x0	CSI-2 Port, Line Counter with Errors MSBs When read, this register returns the value of bits [15:8] of the 16-bit counter csi_line_err_count. The LSBs of the counter are sampled into the CSI_LINE_ERR_COUNT_LO register and the counter is cleared.

7.6.8.8 CSI_LINE_ERR_COUNT_LO Register

Table 7-150. CSI_LINE_ERR_COUNT_LO Register (Address 0x97)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_LINE_ERR _COUNT_LO	R	0x0	CSI-2 Port, Line Counter with Errors LSBs When read, this register returns the value of bits [7:0] of the 16-bit counter csi_line_err_count. The CSI_LINE_ERR_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

7.6.8.9 RESERVED Register

Table 7-151. RESERVED Register (Address 0x98)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/RC	0x0	Reserved

7.6.8.10 RESERVED Register

Table 7-152. RESERVED Register (Address 0x99)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R	0x0	Reserved

7.6.8.11 RESERVED Register

Table 7-153. RESERVED Register (Address 0x9A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/RC	0x0	Reserved

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7.6.8.12 RESERVED Register

Table 7-154. RESERVED Register (Address 0x9B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R	0x0	Reserved

7.6.8.13 RESERVED Register

Table 7-155. RESERVED Register (Address 0x9C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/RC	0x0	Reserved

7.6.8.14 RESERVED Register

Table 7-156. RESERVED Register (Address 0x9D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R	0x0	Reserved

7.6.8.15 RESERVED Register

Table 7-157. RESERVED Register (Address 0x9E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/RC	0x0	Reserved

7.6.8.16 RESERVED Register

Table 7-158. RESERVED Register (Address 0x9F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R	0x0	Reserved

7.6.9 RESERVED (Shared)

7.6.9.1 RESERVED Registers

Table 7-159. RESERVED Registers (Address 0xA0 - 0xA4)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x0	Reserved

7.6.9.2 REFCLK_FREQ Register

Table 7-160. REFCLK_FREQ Register (Address 0xA5)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	REFCLK_FREQ	R	0x0	REFCLK frequency measurement in MHz.

7.6.9.3 RESERVED Registers

Table 7-161. RESERVED Registers (Address 0xA6 - 0xAF)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x0	Reserved

7.6.10 Indirect Access Registers (Shared)

7.6.10.1 IND_ACC_CTL Register

Table 7-162. IND_ACC_CTL Register (Address 0xB0)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	-	0x0	Reserved

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Table 7-162. IND_ACC_CTL Register (Address 0xB0) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
5:2	IA_SEL	R/W	0x7	Indirect Access Register Select: Selects target for register access 0000 : CSI-2 Pattern Generator & Timing Registers 0001 : FPD3 RX Port 0 Reserved Registers 0010 : FPD3 RX Port 1 Reserved Registers 0011 : FPD3 RX Port 2 Reserved Registers 0100 : FPD3 RX Port 3 Reserved Registers 0101 : FPD3 RX Shared Reserved Registers 0110 : Simultaneous write to FPD3 RX Reserved Registers 0111 : CSI-2 Reserved Registers
1	IA_AUTO_INC	R/W	0	Indirect Access Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1
0	IA_READ	R/W	0	Indirect Access Read: Setting this allows generation of a read strobe to the selected register block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes will also be asserted following a read of the IND_ACC_DATA register. This function is only required for blocks that need to pre-fetch register data.

7.6.10.2 IND_ACC_ADDR Register

Table 7-163. IND_ACC_ADDR Register (Address 0xB1)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	IA_ADDR	R/W	0x3A	Indirect Access Register Offset: This register contains the 8-bit register offset for the indirect access.

7.6.10.3 IND_ACC_DATA Register

Table 7-164. IND_ACC_DATA Register (Address 0xB2)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	IA_DATA	R/W	0x14	Indirect Access Data: Writing this register will cause an indirect write of the IND_ACC_DATA value to the selected analog block register. Reading this register will return the value of the selected block register. The default value may be different from a device to a device.

7.6.11 Digital Registers (Shared)

7.6.11.1 BIST Control Register

Table 7-165. BIST Control Register (Address 0xB3)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	BIST_OUT_MODE	R/W	0x0	BIST Output Mode 00 : No toggling 01 : Alternating 1/0 toggling 1x : Toggle based on BIST data
5:4	RESERVED	-	0x0	Reserved
3	RESERVED	R/W	1	Bist Configuration 1: Reserved 0: Bist configured through bits 2:0 in this register
2:1	BIST_CLOCK_SOURCE	R/W	0	BIST Clock Source This register field selects the BIST Clock Source at the Serializer. These register bits are automatically written to the CLOCK SOURCE bits (register offset 0x14) in the Serializer after BIST is enabled. See the appropriate Serializer register descriptions for details.
0	BIST_EN	R/W	0	BIST Control 1: Enabled 0: Disabled

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7.6.11.2 RESERVED Register

Table 7-166. RESERVED Register (Address 0xB4)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x25	Reserved

7.6.11.3 RESERVED Register

Table 7-167. RESERVED Register (Address 0xB5)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x00	Reserved

7.6.11.4 RESERVED Register

Table 7-168. RESERVED Register (Address 0xB6)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x18	Reserved

7.6.11.5 RESERVED Register

Table 7-169. RESERVED Register (Address 0xB7)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x00	Reserved

7.6.11.6 MODE_IDX_STS Register

Table 7-170. MODE_IDX_STS Register (Address 0xB8)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	IDX_DONE	R	1	IDX Done If set, indicates the IDX decode has completed and latched into the IDX status bits.
6:4	IDX	R/S	Strap	IDX Decode 3-bit decode from IDX pin
3	MODE_DONE	R	1	MODE Done If set, indicates the MODE decode has completed and latched into the MODE status bits.
2:0	MODE	R/S	Strap	MODE Decode 3-bit decode from MODE pin

7.6.11.7 LINK_ERROR_COUNT Register

Table 7-171. LINK_ERROR_COUNT Register (Address 0xB9)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	-	0x0	Reserved
5	LINK_SFIL_WAIT	R/W	1	During SFILTER adaption, setting this bit will cause the Lock detect circuit to ignore errors during the SFILTER wait period after the SFILTER control is updated. 1: Errors during SFILTER Wait period will be ignored 0: Errors during SFILTER Wait period will not be ignored and may cause loss of Lock
4	LINK_ERR_COUNT_EN	R/W	1	Enable serial link data integrity error count 1: Enable error count 0: DISABLE

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Table 7-171. LINK_ERROR_COUNT Register (Address 0xB9) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
3:0	LINK_ERR_THRESH	R/W	0x3	Link error count threshold. The Link Error Counter monitors the forward channel link and determines when link will be dropped. The link error counter is pixel clock based. clk0, clk1, parity, and DCA are monitored for link errors. If the error counter is enabled, the deserializer will lose lock once the error counter reaches the LINK_ERR_THRESH value. If the link error counter is disabled, the deserilizer will lose lock after one error.

7.6.11.8 FPD3_ENC_CTL Register

Recommended to set bit seven in the FPD-Link III encoder control register to 0 in order to prevent any updates of link information values from encoded packets that do not pass CRC check. The FPD-Link III Encoder CRC flag must also be in place by setting FPD3_ENC_CRC_DIS (register 0x4A[4]) to 1.

Table 7-172. FPD3_ENC_CTL (Address 0xBA)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	1	0: Enable FPD-Link III encoder CRC (recommended) 1: Disable FPD-Link III encoder CRC
6:0	RESERVED	-	0x03	Reserved

7.6.11.9 RESERVED Register

Table 7-173. RESERVED Register (Address 0xBB)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x74	Reserved

7.6.11.10 FV_MIN_TIME Register

Table 7-174. FV_MIN_TIME Register (Address 0xBC)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FRAME_VALID_MIN	R/W	0x80	Frame Valid Minimum Time This register controls the minimum time the FrameValid (FV) should be active before the Raw mode FPD3 receiver generates a FrameStart packet. Duration is in FPD3 clock periods.

7.6.11.11 RESERVED Register

Table 7-175. RESERVED Register (Address 0xBD)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x00	Reserved

7.6.11.12 GPIO_PD_CTL Register

Table 7-176. GPIO_PD_CTL Register (Address 0xBE)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	GPIO7_PD_DIS	R/W	0	GPIO7 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor (25-kΩ typ) that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor

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Table 7-176. GPIO_PD_CTL Register (Address 0xBE) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
6	GPIO6_PD_DIS	R/W	0	GPIO6 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor (25-kΩ typ) that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
5	GPIO5_PD_DIS	R/W	0	GPIO5 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor (25-kΩ typ) that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
4	GPIO4_PD_DIS	R/W	0	GPIO4 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor (25-kΩ typ) that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
3	GPIO3_PD_DIS	R/W	0	GPIO3 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor (25-kΩ typ) that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
2	GPIO2_PD_DIS	R/W	0	GPIO2 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor (25-kΩ typ) that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
1	GPIO1_PD_DIS	R/W	0	GPIO1 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor (25-kΩ typ) that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor
0	GPIO0_PD_DIS	R/W	0	GPIO0 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor (25-kΩ typ) that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pull-down resistor 0 : Enable GPIO pull-down resistor

7.6.11.13 RESERVED Register

Table 7-177. RESERVED (Address 0xBF)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x00	Reserved

7.6.12 RESERVED Registers

Table 7-178. RESERVED (Address 0xC0 - 0xCF)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x00	Reserved

7.6.13 Digital RX Port Debug Registers (Paged)

Use FPD3_PORT_SEL (0x4C) register to select digital RX Port 0, RX Port1, RX Port 2, or RX Port 3 debug registers.

- FPD3 RX Port 0:
  - Read: 0x4C[5:4] = 00
  - Write: 0x4C[0] = 1
- FPD3 RX Port 1:
  - Read: 0x4C[5:4] = 01
  - Write: 0x4C[1] = 1
- FPD3 RX Port 2:
  - Read: 0x4C[5:4] = 10
  - Write: 0x4C[2] = 1
- FPD3 RX Port 3:
  - Read: 0x4C[5:4] = 11
  - Write: 0x4C[3] = 1

7.6.13.1 PORT_DEBUG Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-179. PORT_DEBUG Register (Address 0xD0)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	-	0	Reserved
6	RESERVED	-	0	Reserved
5	SER_BIST_ACT	R	0	Serializer BIST active This register indicates the Serializer is in BIST mode. If the Deserializer is not in BIST mode, this could indicate an error condition.
4:2	RESERVED	-	0x0	Reserved
1	FORCE_BC_ERRORS	R/W	0	This bit introduces continuous errors into Back channel frame.
0	FORCE_1_BC_ERROR	R/W/SC	0	This bit introduces one error into Back channel frame. Self clearing bit.

7.6.13.2 RESERVED Register

Table 7-180. RESERVED Register (Address 0xD1)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x43	Reserved

7.6.13.3 AEQ_CTL2 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-181. AEQ_CTL2 Register (Address 0xD2)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	ADAPTIVE_EQ _RELOCK_TIME	R/W	0x4	Time to wait for lock before incrementing the EQ to next setting 000 : 164 us 001 : 328 us 010 : 655 us 011 : 1.31 ms 100 : 2.62 ms 101 : 5.24 ms 110 : 10.5ms 111 : 21.0 ms
4	AEQ_1ST_LOCK _MODE	R/W	1	AEQ First Lock Mode This register bit controls the Adaptive Equalizer algorithm operation at initial Receiver Lock. 0 : Initial AEQ lock may occur at any value 1 : Initial Receiver lock will restart AEQ at 0, providing a more deterministic initial AEQ value
3	AEQ_RESTART	R/W/SC	0	Set high to restart AEQ adaptation from initial value. This bit is self clearing. Adaption is restarted.
2	SET_AEQ_FLOOR	R/W	1	AEQ adaptation starts from a pre-set floor value rather than from zero - good in long cable situations
1:0	RESERVED	-	0x0	Reserved

7.6.13.4 AEQ_STATUS Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-182. AEQ_STATUS Register (Address 0xD3)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	-	0x0	Reserved
5:3	EQ_STATUS_2	R	0x0	Adaptive EQ Status 2
2:0	EQ_STATUS_1	R	0x0	Adaptive EQ Status 1

7.6.13.5 ADAPTIVE_EQ_BYPASS Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-183. ADAPTIVE EQ BYPASS Register (Address 0xD4)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	EQ_STAGE_1 _SELECT_VALUE	R/W	0x3	EQ select value [5:3] - Used if adaptive EQ is bypassed.
4	AEQ_LOCK_MODE	R/W	0	Adaptive Equalizer lock mode When set to a 1, Receiver Lock status requires the Adaptive Equalizer to complete adaption. When set to a 0, Receiver Lock is based only on the Lock circuit itself. AEQ may not have stabilized.
3:1	EQ_STAGE_2 _SELECT_VALUE	R/W	0x0	EQ select value [2:0] - Used if adaptive EQ is bypassed.
0	ADAPTIVE_EQ _BYPASS	R/W	0	1: Disable adaptive EQ 0: Enable adaptive EQ

7.6.13.6 AEQ_MIN_MAX Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-184. AEQ_MIN_MAX Register (Address 0xD5)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	AEQ_MAX	R/W	0xF	Adaptive Equalizer Maximum value This register sets the maximum value for the Adaptive EQ algorithm.
3:0	ADAPTIVE_EQ _FLOOR_VALUE	R/W	0x2	When AEQ floor is enabled by register 0xD2[2] the starting setting is given by this register.

7.6.13.7 SFILTER_STS_0 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-185. SFILTER_STS_0 Register (Address 0xD6)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	SFILTER_MAXED	R/RC	0	SFILTER has reached limit When set, the adaptive control of the SFILTER has reached the maximum limit and the algorithm is unable to further adapt. This register is cleared on read.
6	SFILTER_STABLE	R/LL	0	Indicates SFILTER setting is stable This register bit value is latched low. Read to clear for current status.
5:0	SFILTER_CDLY	R	0x0	SFITLER Clock Delay Current value of clock delay control to SFILTER circuit

7.6.13.8 SFILTER_STS_1 Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-186. SFILTER_STS_1 Register (Address 0xD7)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	-	0	Reserved
6	SFILTER_ERROR	R/RC	0	SFILTER measurement error detect If this bit is set, one or more measurements since the last read reported invalid results. This register is cleared on read.
5:0	SFILTER_DDLY	R	0x0	SFITLER Data Delay Current value of data delay control to SFILTER circuit (The readout may vary depending on device status).

7.6.13.9 PORT_ICR_HI Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-187. PORT_ICR_HI Register (Address 0xD8)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	RESERVED	-	0x0	Reserved
2	IE_FPD3_ENC_ERR	R/W	0	Interrupt on FPD-Link III Receiver Encoding Error When enabled, an interrupt is generated on detection of an encoding error on the FPD-Link III interface for the receive port as reported in the FPD3_ENC_ERROR bit in the RX_PORT_STS2 register
1	IE_BCC_SEQ_ERR	R/W	0	Interrupt on BCC SEQ Sequence Error When enabled, an interrupt is generated if a Sequence Error is detected for the Bi-directional Control Channel forward channel receiver as reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register.
0	IE_BCC_CRC_ERR	R/W	0	Interrupt on BCC CRC error detect When enabled, an interrupt is generated if a CRC error is detected on a Bi-directional Control Channel frame received over the FPD-Link III forward channel as reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register.

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7.6.13.10 PORT_ICR_LO Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-188. PORT_ICR_LO Register (Address 0xD9)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	-	0	Reserved
6	IE_LINE_LEN_CHG	R/W	0	Interrupt on Video Line length When enabled, an interrupt is generated if the length of the video line changes. Status is reported in the LINE_LEN_CHG bit in the RX_PORT_STS2 register.
5	IE_LINE_CNT_CHG	R/W	0	Interrupt on Video Line count When enabled, an interrupt is generated if the number of video lines per frame changes. Status is reported in the LINE_CNT_CHG bit in the RX_PORT_STS2 register.
4	IE_BUFFER_ERR	R/W	0	Interrupt on Receiver Buffer Error When enabled, an interrupt is generated if the Receive Buffer overflow is detected as reported in the BUFFER_ERROR bit in the RX_PORT_STS2 register.
3	RESERVED	-	0	Reserved
2	IE_FPD3_PAR_ERR	R/W	0	Interrupt on FPD-Link III Receiver Parity Error When enabled, an interrupt is generated on detection of parity errors on the FPD-Link III interface for the receive port. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register.
1	IE_PORT_PASS	R/W	0	Interrupt on change in Port PASS status When enabled, an interrupt is generated on a change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register.
0	IE_LOCK_STS	R/W	0	Interrupt on change in Lock Status When enabled, an interrupt is generated on a change in lock status. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register.

7.6.13.11 PORT_ISR_HI Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-189. PORT_ISR_HI Register (Address 0xDA)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	RESERVED	-	0x0	Reserved
2	IS_FPD3_ENC_ERR	R	0	FPD-Link III Receiver Encode Error Interrupt Status An encoding error on the FPD-Link III interface for the receive port has been detected. Status is reported in the FPD3_ENC_ERROR bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
1	IS_BCC_SEQ_ERR	R	0	BCC CRC Sequence Error Interrupt Status A Sequence Error has been detected for the Bi-directional Control Channel forward channel receiver. Status is reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
0	IS_BCC_CRC_ERR	R	0	BCC CRC error detect Interrupt Status A CRC error has been detected on a Bi-directional Control Channel frame received over the FPD-Link III forward channel. Status is reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.

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7.6.13.12 PORT_ISR_LO Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-190. PORT_ISR_LO Register (Address 0xDB)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	-	0	Reserved
6	IS_LINE_LEN_CHG	R	0	Video Line Length Interrupt Status A change in video line length has been detected. Status is reported in the LINE_LEN_CHG bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
5	IS_LINE_CNT_CHG	R	0	Video Line Count Interrupt Status A change in number of video lines per frame has been detected. Status is reported in the LINE_CNT_CHG bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
4	IS_BUFFER_ERR	R	0	Receiver Buffer Error Interrupt Status A Receive Buffer overflow has been detected as reported in the BUFFER_ERROR bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
3	RESERVED	-	0	Reserved
2	IS_FPD3_PAR_ERR	R	0	FPD-Link III Receiver Parity Error Interrupt Status A parity error on the FPD-Link III interface for the receive port has been detected. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
1	IS_PORT_PASS	R	0	Port Valid Interrupt Status A change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
0	IS_LOCK_STS	R	0	Lock Interrupt Status A change in lock status has been detected. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.

7.6.13.13 FC_GPIO_STS Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-191. FC_GPIO_STS Register (Address 0xDC)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	GPIO3_INT_STS	R/RC	0	GPIO3 Interrupt Status This bit indicates an interrupt condition has been met for GPIO3. This bit is cleared on read.
6	GPIO2_INT_STS	R/RC	0	GPIO2 Interrupt Status This bit indicates an interrupt condition has been met for GPIO2. This bit is cleared on read.
5	GPIO1_INT_STS	R/RC	0	GPIO1 Interrupt Status This bit indicates an interrupt condition has been met for GPIO1. This bit is cleared on read.
4	GPIO0_INT_STS	R/RC	0	GPIO0 Interrupt Status This bit indicates an interrupt condition has been met for GPIO0. This bit is cleared on read.
3	FC_GPIO3_STS	R	0	Forward Channel GPIO3 Status This bit indicates the current value for forward channel GPIO3.

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Table 7-191. FC_GPIO_STS Register (Address 0xDC) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
2	FC_GPIO2_STS	R	0	Forward Channel GPIO2 Status This bit indicates the current value for forward channel GPIO3.
1	FC_GPIO1_STS	R	0	Forward Channel GPIO1 Status This bit indicates the current value for forward channel GPIO3.
0	FC_GPIO0_STS	R	0	Forward Channel GPIO0 Status This bit indicates the current value for forward channel GPIO3.

7.6.13.14 FC_GPIO_ICR Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-192. FC_GPIO_ICR Register (Address 0xDD)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	GPIO3_FALL_IE	W	0	GPIO3 Fall Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO3.
6	GPIO3_RISE_IE	W	0	GPIO3 Rise Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO3.
5	GPIO2_FALL_IE	W	0	GPIO2 Fall Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO2.
4	GPIO2_RISE_IE	W	0	GPIO2 Rise Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO2.
3	GPIO1_FALL_IE	W	0	GPIO1 Fall Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO1.
2	GPIO1_RISE_IE	W	0	GPIO1 Rise Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO1.
1	GPIO0_FALL_IE	W	0	GPIO0 Fall Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO0.
0	GPIO1_RISE_IE	W	0	GPIO3 Rise Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO0.

7.6.13.15 SEN_INT_RISE_STS Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

Table 7-193. SEN_INT_RISE_STS Register (Address 0xDE)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SEN_INT_RISE	R/RC	0x00	Sensor Interrupt Rise Status This register provides the interrupt status for rising edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in the SEN_INT_RISE_MASK register, a rising edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in this register.

7.6.13.16 SEN_INT_FALL_STS Register

RX port-specific register. The FPD-Link III Port Select register 0x4C configures which unique Rx port registers can be accessed by I2C read and write commands.

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Table 7-194. SEN_INT_FALL_STS Register (Address 0xDF)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SEN_INT_FALL	R/RC	0x00	Sensor Interrupt Fall Status This register provides the interrupt status for falling edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in the SEN_INT_FALL_MASK register, a falling edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in this register.

7.6.14 RESERVED Registers

Table 7-195. RESERVED (Address 0xE0 - 0xEF)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x00	Reserved

7.6.15 FPD3 RX ID Registers (Shared)

7.6.15.1 FPD3_RX_ID0 Register

Table 7-196. FPD3_RX_ID0 Register (Address 0xF0)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_RX_ID0	R	0x5F	FPD3_RX_ID0: First byte ID code: '_'

7.6.15.2 FPD3_RX_ID1 Register

Table 7-197. FPD3_RX_ID1 Register (Address 0xF1)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_RX_ID1	R	0x55	FPD3_RX_ID1: 2nd byte of ID code: 'U'

7.6.15.3 FPD3_RX_ID2 Register

Table 7-198. FPD3_RX_ID2 Register (Address 0xF2)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_RX_ID2	R	0x42	FPD3_RX_ID2: 3rd byte of ID code: 'B'

7.6.15.4 FPD3_RX_ID3 Register

Table 7-199. FPD3_RX_ID3 Register (Address 0xF3)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_RX_ID3	R	0x36	FPD3_RX_ID3: 4th byte of ID code: '6'

7.6.15.5 FPD3_RX_ID4 Register

Table 7-200. FPD3_RX_ID4 Register (Address 0xF4)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_RX_ID4	R	0x36	FPD3_RX_ID4: 5th byte of ID code: '6'

7.6.15.6 FPD3_RX_ID5 Register

Table 7-201. FPD3_RX_ID5 Register (Address 0xF5)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_RX_ID5	R	0x32	FPD3_RX_ID5: 6th byte of ID code: '2'

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7.6.16 RESERVED Registers

Table 7-202. RESERVED (Address 0xF6 - 0xF7)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x00	Reserved

7.6.17 RX Port I2C Addressing Registers (Shared)

7.6.17.1 I2C_RX0_ID Register

As an alternative to paging to access FPD-Link III receive port 0 registers, a separate I2C address may be enabled to allow direct access to the port 0 specific registers. The I2C_RX_0_ID register provides a simpler method of accessing device registers specifically for port 0 without having to use the paging function to select the register page. Using this address also allows access to all shared registers.

Table 7-203. I2C_RX0_ID Register (Address 0xF8)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	RX_PORT0_ID	R/W	0x0	7-bit Receive Port 0 I2C ID Configures the decoder for detecting transactions designated for Receiver port 0 registers. This provides a simpler method of accessing device registers specifically for port 0 without having to use the paging function to select the register page. A value of 0 in this field disables the Port0 decoder.
0	RESERVED	-	0	Reserved

7.6.17.2 I2C_RX1_ID Register

As an alternative to paging to access FPD-Link III receive port 1 registers, a separate I2C address may be enabled to allow direct access to the port 1 specific registers. The I2C_RX_1_ID register provides a simpler method of accessing device registers specifically for port 1 without having to use the paging function to select the register page. Using this address also allows access to all shared registers.

Table 7-204. I2C_RX1_ID Register (Address 0xF9)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	RX_PORT1_ID	R/W	0x0	7-bit Receive Port 1 I2C ID Configures the decoder for detecting transactions designated for Receiver port 1 registers. This provides a simpler method of accessing device registers specifically for port 1 without having to use the paging function to select the register page. A value of 0 in this field disables the Port1 decoder.
0	RESERVED	-	0	Reserved

7.6.17.3 I2C_RX2_ID Register

As an alternative to paging to access FPD-Link III receive port 2 registers, a separate I2C address may be enabled to allow direct access to the port 2 specific registers. The I2C_RX_2_ID register provides a simpler method of accessing device registers specifically for port 2 without having to use the paging function to select the register page. Using this address also allows access to all shared registers.

Table 7-205. I2C_RX2_ID Register (Address 0xFA)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	RX_PORT2_ID	R/W	0x0	7-bit Receive Port 2 I2C ID Configures the decoder for detecting transactions designated for Receiver port 2 registers. This provides a simpler method of accessing device registers specifically for port 2 without having to use the paging function to select the register page. A value of 0 in this field disables the Port2 decoder.
0	RESERVED	-	0	Reserved

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7.6.17.4 I2C_RX3_ID Register

As an alternative to paging to access FPD-Link III receive port 3 registers, a separate I2C address may be enabled to allow direct access to the port 3 specific registers. The I2C_RX_3_ID register provides a simpler method of accessing device registers specifically for port 3 without having to use the paging function to select the register page. Using this address also allows access to all shared registers.

Table 7-206. I2C_RX3_ID Register (Address 0xFB)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	RX_PORT3_ID	R/W	0x0	7-bit Receive Port 3 I2C ID Configures the decoder for detecting transactions designated for Receiver port 3 registers. This provides a simpler method of accessing device registers specifically for port 3 without having to use the paging function to select the register page. A value of 0 in this field disables the Port3 decoder.
0	RESERVED	-	0	Reserved

7.6.18 RESERVED Registers

Table 7-207. RESERVED (Address 0xFC - 0xFF)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x00	Reserved

7.6.19 Indirect Access Registers

Several functional blocks include register sets contained in the Indirect Access map; i.e. Pattern Generator, CSI-2 timing, and Analog controls. Register access is provided via an indirect access mechanism through the Indirect Access registers (IND_ACC_CTL, IND_ACC_ADDR, and IND_ACC_DATA). These registers are located at offsets 0xB0-0xB2 in the main register space.

The indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:

1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Write the data value to the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 will write additional data bytes to subsequent register offset locations

For reads, the process is as follows:

1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Read from the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 will read additional data bytes from subsequent register offset locations.

Table 7-208. Indirect Register Map Description

IA Select 0xB0[5:2]	Page/Block	Indirect Registers	Address Range	Description
0000	0	Digital Page 0 Indirect Registers	0x01-0x1F	Pattern Gen Registers
			0x40-0x51	CSI-2 TX Port Timing Registers
0001	1	FPD3 Channel 0 Reserved Registers	0x00-0x14	Reserved
0010	2	FPD3 Channel 1 Reserved Registers	0x00-0x14	Reserved

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Table 7-208. Indirect Register Map Description (continued)

IA Select 0xB0[5:2]	Page/Block	Indirect Registers	Address Range	Description
0011	3	FPD3 Channel 2 Reserved Registers	0x00-0x14	Reserved
0100	4	FPD3 Channel 3 Reserved Registers	0x00-0x14	Reserved
0101	5	FPD3 Share Reserved Registers	0x00-0x04	Reserved
0110	6	Write All FPD3 Reserved Registers	0x00-0x14	Reserved
0111	7	CSI-2 TX Reserved Registers	0x00-0x1D	Reserved

7.6.20 Digital Page 0 Indirect Registers

7.6.20.1 RESERVED

Table 7-209. RESERVED Register (Address 0x00)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x0	Reserved

7.6.20.2 PGEN_CTL

Table 7-210. PGEN_CTL Register (Address 0x01)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	RESERVED	-	0x0	Reserved
0	PGEN_ENABLE	R/W	0	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

7.6.20.3 PGEN_CFG

Table 7-211. PGEN_CFG Register (Address 0x02)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	PGEN_FIXED_EN	R/W	0	Fixed Pattern Enable Setting this bit enables Fixed Color Patterns. 0 : Send Color Bar Pattern 1 : Send Fixed Color Pattern
6	RESERVED	-	0	Reserved
5:4	NUM_CBARS	R/W	0x3	Number of Color Bars 00 : 1 Color Bar 01 : 2 Color Bars 10 : 4 Color Bars 11 : 8 Color Bars
3:0	BLOCK_SIZE	R/W	0x3	Block Size For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 15.

7.6.20.4 PGEN_CSI_DI

Table 7-212. PGEN_CSI_DI Register (Address 0x03)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	PGEN_CSI_VC	R/W	0x0	CSI-2 Virtual Channel Identifier This field controls the value sent in the CSI-2 packet for the Virtual Channel Identifier
5:0	PGEN_CSI_DT	R/W	0x24	CSI-2 Data Type This field controls the value sent in the CSI-2 packet for the Data Type. The default value (0x24) indicates RGB888.

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7.6.20.5 PGEN_LINE_SIZE1

Table 7-213. PGEN_LINE_SIZE1 Register (Address 0x04)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_LINE_SIZE[15:8]	R/W	0x07	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

7.6.20.6 PGEN_LINE_SIZE0

Table 7-214. PGEN_LINE_SIZE0 Register (Address 0x05)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_LINE_SIZE[7:0]	R/W	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

7.6.20.7 PGEN_BAR_SIZE1

Table 7-215. PGEN_BAR_SIZE1 Register (Address 0x06)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_BAR_SIZE[15:8]	R/W	0x0	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

7.6.20.8 PGEN_BAR_SIZE0

Table 7-216. PGEN_BAR_SIZE0 Register (Address 0x07)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_BAR_SIZE[7:0]	R/W	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

7.6.20.9 PGEN_ACT_LPF1

Table 7-217. PGEN_ACT_LPF1 Register (Address 0x08)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ACT_LPF[15:8]	R/W	0x01	Active Lines Per Frame Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

7.6.20.10 PGEN_ACT_LPF0

Table 7-218. PGEN_ACT_LPF0 Register (Address 0x09)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ACT_LPF[7:0]	R/W	0xE0	Active Lines Per Frame Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

7.6.20.11 PGEN_TOT_LPF1

Table 7-219. PGEN_TOT_LPF1 Register (Address 0x0A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_TOT_LPF[15:8]	R/W	0x02	Total Lines Per Frame Most significant byte of the number of total lines per frame including vertical blanking

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7.6.20.12 PGEN_TOT_LPF0

Table 7-220. PGEN_TOT_LPF0 Register (Address 0x0B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_TOT_LPF[7:0]	R/W	0x0D	Total Lines Per Frame Least significant byte of the number of total lines per frame including vertical blanking

7.6.20.13 PGEN_LINE_PD1

Table 7-221. PGEN_LINE_PD1 Register (Address 0x0C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_LINE_PD[15:8]	R/W	0x0C	Line Period Most significant byte of the line period. In 800 Mbps and 1.6 Gbps CSI-2 modes, units are 10 ns and the default setting for the line period registers sets a line period of 31.75 microseconds. In 1.2 Gbps CSI-2 mode, units are 13.33 ns and the default setting for the line period registers sets a line period of 42.33 microseconds. In 400 Mbps CSI-2 mode, units are 20ns and the default setting for the line period registers sets a line period of 63.5 microseconds.

7.6.20.14 PGEN_LINE_PD0

Table 7-222. PGEN_LINE_PD0 Register (Address 0x0D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_LINE_PD[7:0]	R/W	0x67	Line Period Least significant byte of the line period. In 800 Mbps and 1.6 Gbps CSI-2 modes, units are 10 ns and the default setting for the line period registers sets a line period of 31.75 microseconds. In 1.2 Gbps CSI-2 mode, units are 13.33 ns and the default setting for the line period registers sets a line period of 42.33 microseconds. In 400 Mbps CSI-2 mode, units are 20ns and the default setting for the line period registers sets a line period of 63.5 microseconds.

7.6.20.15 PGEN_VBP

Table 7-223. PGEN_VBP Register (Address 0x0E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_VBP	R/W	0x21	Vertical Back Porch This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.

7.6.20.16 PGEN_VFP

Table 7-224. PGEN_VFP Register (Address 0x0F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_VFP	R/W	0x0A	Vertical Front Porch This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.

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7.6.20.17 PGEN_COLOR0

Table 7-225. PGEN_COLOR0 Register (Address 0x10)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR0	R/W	0xAA	Pattern Generator Color 0 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0.For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.

7.6.20.18 PGEN_COLOR1

Table 7-226. PGEN_COLOR1 Register (Address 0x11)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR1	R/W	0x33	Pattern Generator Color 1 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1.For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.

7.6.20.19 PGEN_COLOR2

Table 7-227. PGEN_COLOR2 Register (Address 0x12)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR2	R/W	0xF0	Pattern Generator Color 2 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2.For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.

7.6.20.20 PGEN_COLOR3

Table 7-228. PGEN_COLOR3 Register (Address 0x13)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR3	R/W	0x7F	Pattern Generator Color 3 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3.For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.

7.6.20.21 PGEN_COLOR4

Table 7-229. PGEN_COLOR4 Register (Address 0x14)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR4	R/W	0x55	Pattern Generator Color 4 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4.For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.

7.6.20.22 PGEN_COLOR5

Table 7-230. PGEN_COLOR5 Register (Address 0x15)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR5	R/W	0xCC	Pattern Generator Color 5 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5.For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

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7.6.20.23 PGEN_COLOR6

Table 7-231. PGEN_COLOR6 Register (Address 0x16)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR6	R/W	0x0F	Pattern Generator Color 6 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6.For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.

7.6.20.24 PGEN_COLOR7

Table 7-232. PGEN_COLOR7 Register (Address 0x17)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR7	R/W	0x80	Pattern Generator Color 7 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7.For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.

7.6.20.25 PGEN_COLOR8

Table 7-233. PGEN_COLOR8 Register (Address 0x18)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR8	R/W	0x0	Pattern Generator Color 8 For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.

7.6.20.26 PGEN_COLOR9

Table 7-234. PGEN_COLOR9 Register (Address 0x19)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR9	R/W	0x0	Pattern Generator Color 9 For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.

7.6.20.27 PGEN_COLOR10

Table 7-235. PGEN_COLOR10 Register (Address 0x1A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR10	R/W	0x0	Pattern Generator Color 10 For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.

7.6.20.28 PGEN_COLOR11

Table 7-236. PGEN_COLOR11 Register (Address 0x1B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR11	R/W	0x0	Pattern Generator Color 11 For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.

7.6.20.29 PGEN_COLOR12

Table 7-237. PGEN_COLOR12 Register (Address 0x1C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR12	R/W	0x0	Pattern Generator Color 12 For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.

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7.6.20.30 PGEN_COLOR13

Table 7-238. PGEN_COLOR13 Register (Address 0x1D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR13	R/W	0x0	Pattern Generator Color 13 For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.

7.6.20.31 PGEN_COLOR14

Table 7-239. PGEN_COLOR14 Register (Address 0x1E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR14	R/W	0x0	Pattern Generator Color 14 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

7.6.20.32 PGEN_COLOR15

Table 7-240. PGEN_COLOR15 Register (Address 0x1F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x0	Reserved

7.6.20.33 CSI_TCK_PREP

Table 7-241. CSI_TCK_PREP Register (Address 0x40)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_TCK_PREP_OV	R/W	0	Override CSI-2 Tck-prep parameter 0: Tck-prep is automatically determined 1: Override Tck-prep with value in bits 6:0 of this register
6:0	MR_TCK_PREP	R R/W	0x5	Tck-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. The default value is based on the 800 Mbps CSI-2 rate and may change if different rate is selected. If bit 7 of this register is 1, this field is read/write.

7.6.20.34 CSI_TCK_ZERO

Table 7-242. CSI_TCK_ZERO Register (Address 0x41)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_TCK_ZERO_OV	R/W	0	Override CSI-2 Tck-zero parameter 0: Tck-zero is automatically determined 1: Override Tck-zero with value in bits 6:0 of this register
6:0	MR_TCK_ZERO	R R/W	0x1B	Tck-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. The default value is based on the 800 Mbps CSI-2 rate and may change if different rate is selected. If bit 7 of this register is 1, this field is read/write.

7.6.20.35 CSI_TCK_TRAIL

Table 7-243. CSI_TCK_TRAIL Register (Address 0x42)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_TCK_TRAIL_OV	R/W	0	Override CSI-2 Tck-trail parameter 0: Tck-trail is automatically determined 1: Override Tck-trail with value in bits 6:0 of this register

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Table 7-243. CSI_TCK_TRAIL Register (Address 0x42) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
6:0	MR_TCK_TRAIL	R R/W	0x0B	Tck-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. The default value is based on the 800 Mbps CSI-2 rate and may change if different rate is selected. If bit 7 of this register is 1, this field is read/write.

7.6.20.36 CSI_TCK_POST

Table 7-244. CSI_TCK_POST Register (Address 0x43)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_TCK_POST_OV	R/W	0	Override CSI-2 Tck-post parameter 0: Tck-post is automatically determined 1: Override Tck-post with value in bits 6:0 of this register
6:0	MR_TCK_POST	R R/W	0x0A	Tck-post value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. The default value is based on the 800 Mbps CSI-2 rate and may change if different rate is selected. If bit 7 of this register is 1, this field is read/write.

7.6.20.37 CSI_THS_PREP

Table 7-245. CSI_THS_PREP Register (Address 0x44)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_THS_PREP_OV	R/W	0	Override CSI-2 Ths-prep parameter 0: Ths-prep is automatically determined 1: Override Ths-prep with value in bits 6:0 of this register
6:0	MR_THS_PREP	R R/W	0x6	Ths-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. The default value is based on the 800 Mbps CSI-2 rate and may change if different rate is selected. If bit 7 of this register is 1, this field is read/write.

7.6.20.38 CSI_THS_ZERO

Table 7-246. CSI_THS_ZERO Register (Address 0x45)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_THS_ZERO_OV	R/W	0	Override CSI-2 Ths-zero parameter 0: Ths-zero is automatically determined 1: Override Ths-zero with value in bits 6:0 of this register
6:0	MR_THS_ZERO	R R/W	0x0C	Ths-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. The default value is based on the 800 Mbps CSI-2 rate and may change if different rate is selected. If bit 7 of this register is 1, this field is read/write.

7.6.20.39 CSI_THS_TRAIL

Table 7-247. CSI_THS_TRAIL Register (Address 0x46)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_THS_TRAIL_OV	R/W	0	Override CSI-2 Ths-trail parameter 0: Ths-trail is automatically determined 1: Override Ths-trail with value in bits 6:0 of this register
6:0	MR_THS_TRAIL	R R/W	0x8	Ths-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. The default value is based on the 800 Mbps CSI-2 rate and may change if different rate is selected. If bit 7 of this register is 1, this field is read/write.

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7.6.20.40 CSI_THS_EXIT

Table 7-248. CSI_THS_EXIT Register (Address 0x47)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_THS_EXIT_OV	R/W	0	Override CSI-2 Ths-exit parameter 0: Ths-exit is automatically determined 1: Override Ths-exit with value in bits 6:0 of this register
6:0	MR_THS_EXIT	R R/W	0x0B	Ths-exit value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. The default value is based on the 800 Mbps CSI-2 rate and may change if different rate is selected. If bit 7 of this register is 1, this field is read/write.

7.6.20.41 CSI1_TPLX

Table 7-249. CSI1_TPLX Register (Address 0x68)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_TPLX_OV	R/W	0	Override CSI-2 Tplx parameter 0: Tplx is automatically determined 1: Override Tplx with value in bits 6:0 of this register
6:0	MR_TPLX	R R/W	0x6	Tplx value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. The default value is based on the 800 Mbps CSI-2 rate and may change if different rate is selected. If bit 7 of this register is 1, this field is read/write.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS90UB662-Q1 is a highly integrated sensor hub deserializer which includes four FPD-Link III inputs targeted at ADAS applications, such as front/rear/surround-view camera sensors, driver monitoring systems, and sensor fusion.

8.1.1 Power Over Coax

The DS90UB662-Q1 is designed to support the Power-over-Coax (PoC) method of powering remote sensor systems. With this method, the power is delivered over the same medium (a coaxial cable) used for high-speed digital video data and bidirectional control and diagnostics data transmission. The method uses passive networks or filters that isolate the transmission line from the loading of the DC-DC regulator circuits and their connecting power traces on both sides of the link as shown in Figure 8-1.

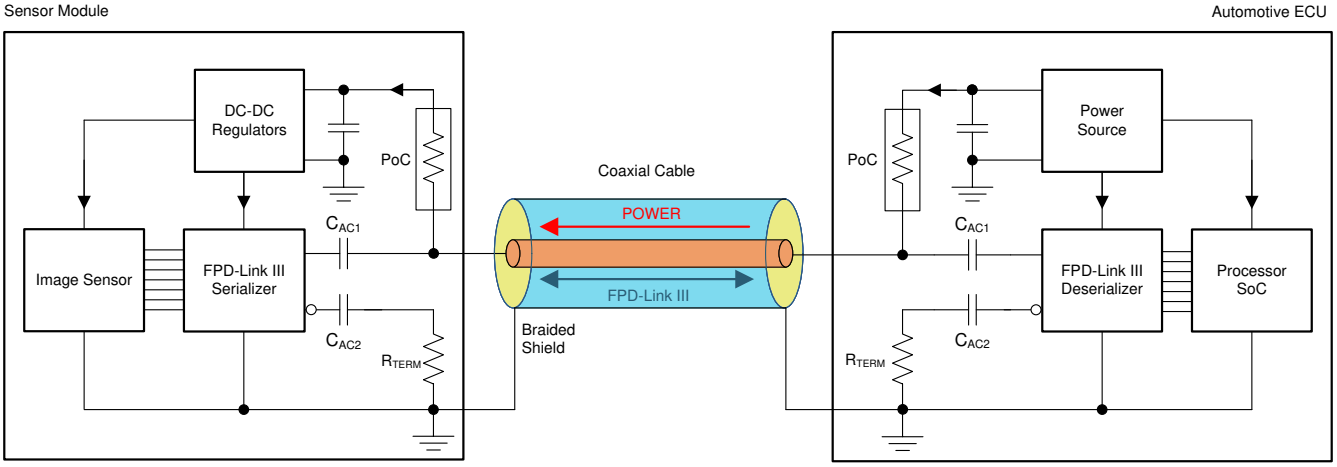

Figure 8-1. Power-over-Coax (PoC) System Diagram

The PoC networks' impedance of ≥ 1 kΩ over a specific frequency band is typically sufficient to isolate the transmission line from the loading of the regulator circuits provided good layout practices are followed and the PCB return loss requirements given in Table 8-3 are met. The lower limit of the frequency band is defined as ½ of the bidirectional control channel's frequency, f_{BC}. The upper limit of the frequency band is the frequency of the forward high-speed channel, f_{FC}.

Figure 8-2 shows a PoC network recommended for a 4G FPD-Link III consisting of DS90UB63x CSI-2 Serializer and DS90UB662-Q1 pair with the bidirectional channel operating at 50 Mbps (½ fBCC = 25 MHz) and the forward channel operating at 4.16 Gbps (fFC ≈ 2.1 GHz).

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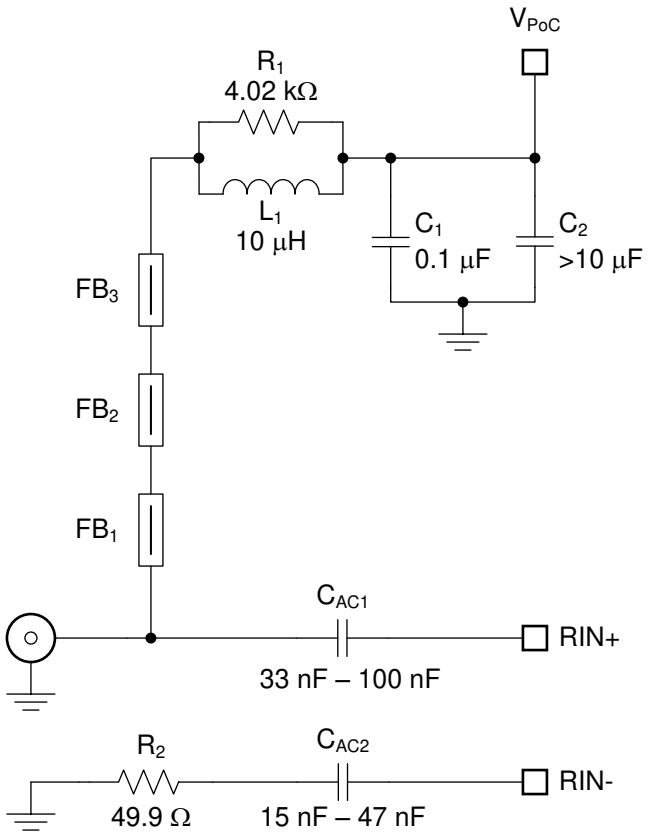

Figure 8-2. Typical PoC Network for a *4G* FPD-Link III

Table 8-1 lists essential components for this particular PoC network.

Table 8-1. Suggested Components for a *4G* FPD-Link PoC Network

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
1	L1	Inductor, 10 µH, 0.288 Ω maximum, 530 mA minimum (Isat, Itemp) 30-MHz SRF min, 3 mm × 3 mm, General-Purpose	LQH3NPN100MJR	Murata
		Inductor, 10 µH, 0.288 Ω maximum, 530 mA minimum (Isat, Itemp) 30-MHz SRF min, 3 mm × 3 mm, AEC-Q200	LQH3NPZ100MJR	Murata
		Inductor, 10 µH, 0.360 Ω maximum, 450 mA minimum (Isat, Itemp) 30-MHz SRF min, 3.2 mm x 2.5 mm, AEC-Q200	NLCV32T-100K-EFD	TDK
		Inductor, 10 µH, 0.400 Ω typical, 550 mA minimum (Isat, Itemp) 39-MHz SRF typ, 3 mm × 3 mm, AEC-Q200	TYS3010100M-10	Laird
		Inductor, 10 µH, 0.325 Ω maximum, 725 mA minimum (Isat, Itemp) 41-MHz SRF typ, 3 mm × 3 mm, AEC-Q200	TYS3015100M-10	Laird
3	FB1-FB3	Ferrite Bead, 1500 kΩ at 1 GHz, 0.5 Ω maximum at DC 500 mA at 85°C, SM0603, General Purpose	BLM18HE152SN1	Murata
		Ferrite Bead, 1500 kΩ at 1 GHz, 0.5 Ω maximum at DC 500 mA at 85°C, SM0603, AEC-Q200	BLM18HE152SZ1	Murata

Application report *Sending Power over Coax in DS90UB913A Designs* (SNLA224) discusses and defines the PoC networks in more detail.

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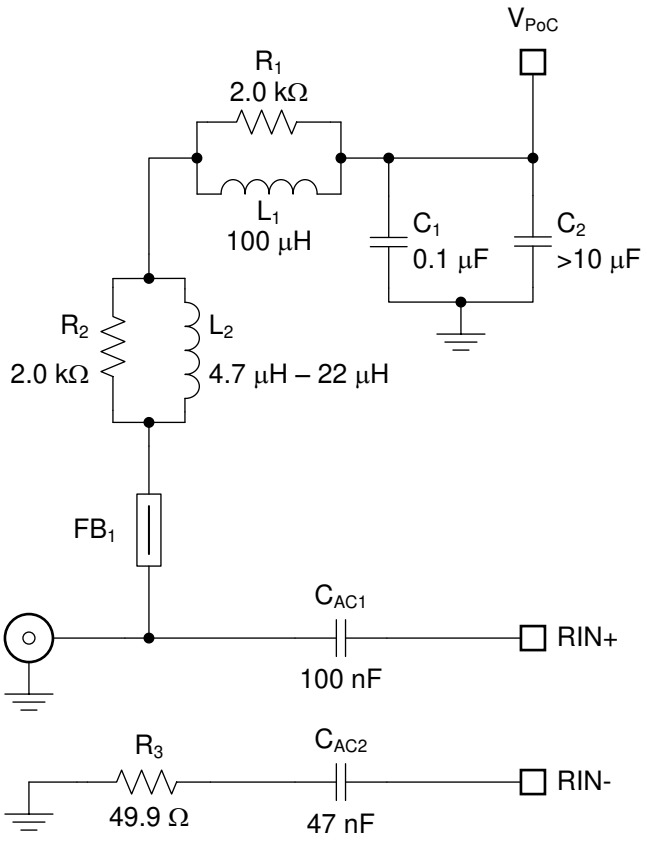

Figure 8-3. Typical PoC Network for a *2G* FPD-Link III

lists essential components for this particular PoC network.

Table 8-2. Suggested Components for a *2G* FPD-Link III PoC Network

Count	Ref Des	Description	Part Number	MFR
1	L1	Inductor, 100 µH, 0.310 Ω max, 710 mA MIN (Isat, Itemp) 7.2 MHz SRF typ, 6.6 mm × 6.6 mm, AEC-Q200	MSS7341-104ML	Coilcraft
		Inductor, 100 µH, 0.606 Ω max, 750 mA MIN (Isat, Itemp) 7.2 MHz SRF typ, 6.0 mm × 6.0 mm, AEC-Q200	NRS6045T101MMGKV	Taiyo Yuden
1	L2	Inductor, 4.7 µH, 0.350 Ω max, 700 mA MIN (Isat, Itemp) 160 MHz SRF typ, 3.8 mm × 3.8 mm, AEC-Q200	1008PS-472KL	Coilcraft
		Inductor, 4.7 µH, 0.130 Ω max, 830 mA MIN (Isat, Itemp), 70 MHz SRF typ, 3.2 mm × 2.5 mm, General Purpose	CBC3225T4R7MRV	Taiyo Yuden
		Inductor, 10 µH, 0.288 Ω max, 530 mA MIN (Isat, Itemp) 30 MHz SRF min, 3 mm × 3 mm, AEC-Q200	LQH3NPZ100MJR	Murata
1	FB1	Ferrite Bead, 1500 kΩ at 1 GHz, 0.5 Ω max at DC 500 mA at 85°C, SM0603, General Purpose	BLM18HE152SN1	Murata
		Ferrite Bead, 1500 kΩ at 1 GHz, 0.5 Ω max at DC 500 mA at 85°C, SM0603, AEC-Q200	BLM18HE152SZ1	Murata

Application report https://www.ti.com/lit/an/snla224/snla224.pdf?ts=1602885821293 (SNLA224) discusses and defines the PoC networks in more detail.

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In addition to the PoC network components selection, their placement and layout play a critical role as well.

- Place the smallest component, typically a ferrite bead or a chip inductor, as close to the connector as possible. Route the high-speed trace through one of its pads to avoid stubs.
- Use the smallest component pads as allowed by manufacturer's design rules. Add anti-pads in the inner planes below the component pads to minimize impedance drop.
- Consult with connector manufacturer for optimized connector footprint.
- Use coupled 100-Ω differential signal traces from the device pins to the AC-coupling caps. Use 50-Ω single-ended traces from the AC-coupling capacitors to the connector.
- Terminate the inverting signal traces close to the connectors with standard 49.9-Ω resistors.

The suggested characteristics for single-ended PCB traces (microstrips or striplines) for serializer or deserializer boards are detailed in Table 8-3. The effects of the PoC networks need to be accounted for when testing the traces for compliance to the suggested limits.

Table 8-3. Suggested Characteristics for Single-Ended PCB Traces With Attached PoC Networks

PARAMETER			MIN	TYP	MAX	UNIT
L_{trace}	Single-ended PCB trace length from the device pin to the connector pin				5	cm
Z_{trace}	Single-ended PCB trace characteristic impedance		45	50	55	Ω
Z_{con}	Connector (mounted) characteristic impedance		40	50	62.5	Ω
RL	Return Loss, S11	½ f_{BC} < f < 0.1 GHz			–20	dB
		0.1 GHz < f < 1 GHz (f in GHz)			–12 + 8 × log(f)	dB
		1 GHz < f < f_{FC}			–12	dB
IL	Insertion Loss, S12	f < 0.5 GHz	–0.35			dB
		f = 1 GHz	–0.6			dB
		f = 2.1 GHz	–1.2			dB

The V_{POC} noise must be kept to 10 mVp-p or lower on the source / deserializer side of the system. The V_{POC} fluctuations on the serializer side, caused by the sensor's transient current draw and the DC resistance of cables and PoC components, must be kept at minimum as well. Increasing the V_{POC} voltage and adding extra decoupling capacitance (> 10 µF) help reduce the amplitude and slew rate of the V_{POC} fluctuations.

Figure 8-3 shows a PoC network recommended for a "2G" FPD-Link III consisting of a DS90UB633A-Q1 serializer and DS90UB662-Q1 with the bidirectional channel operating at the data rate of 2.5 Mbps (½ fBC = 1.25 MHz) and the forward channel operating at the data rate as high as 1.87 Gbps (fFC ≈ 1 GHz).

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8.2 Typical Application

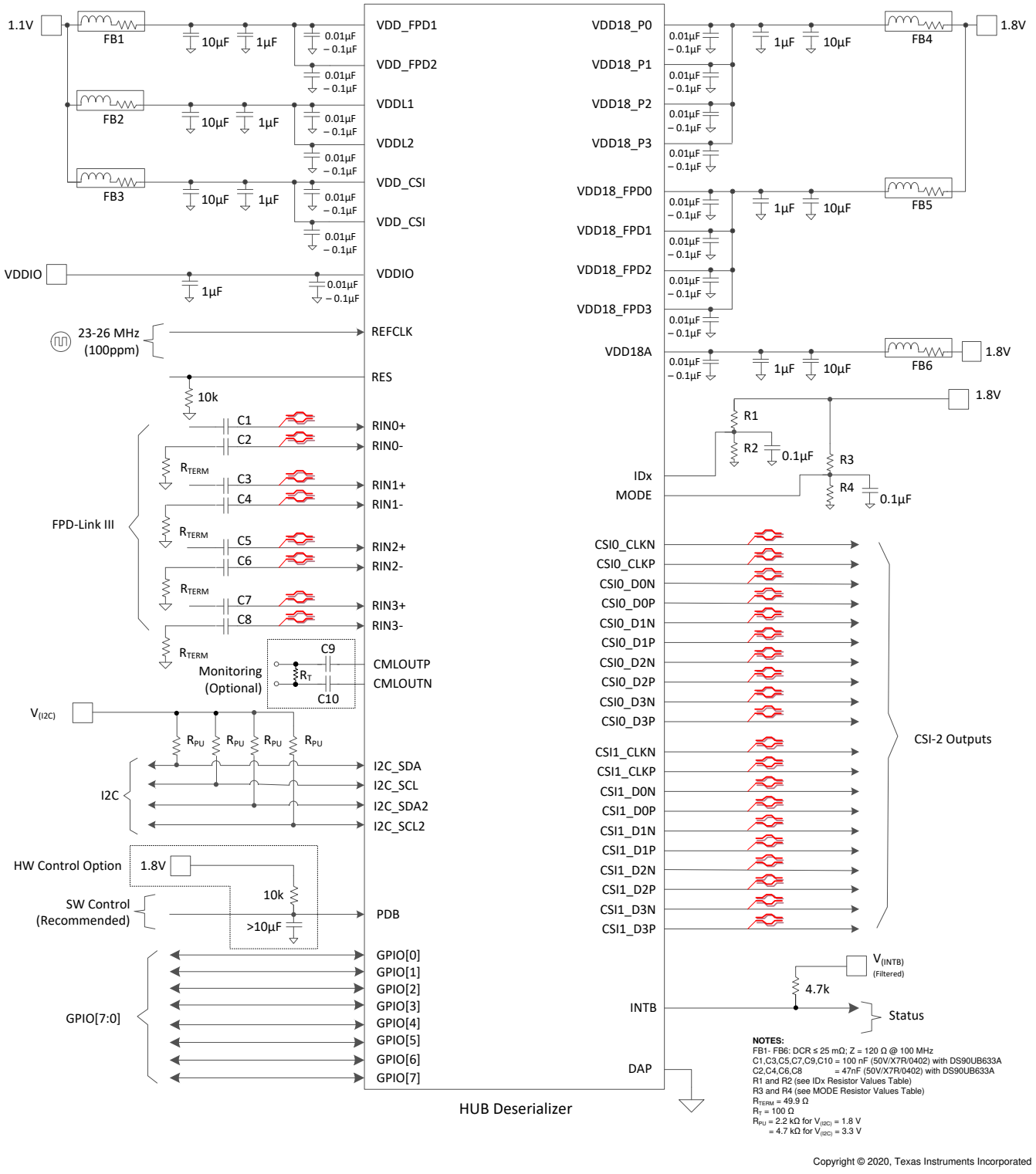

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Figure 8-4. Typical Connection Diagram (Coaxial)

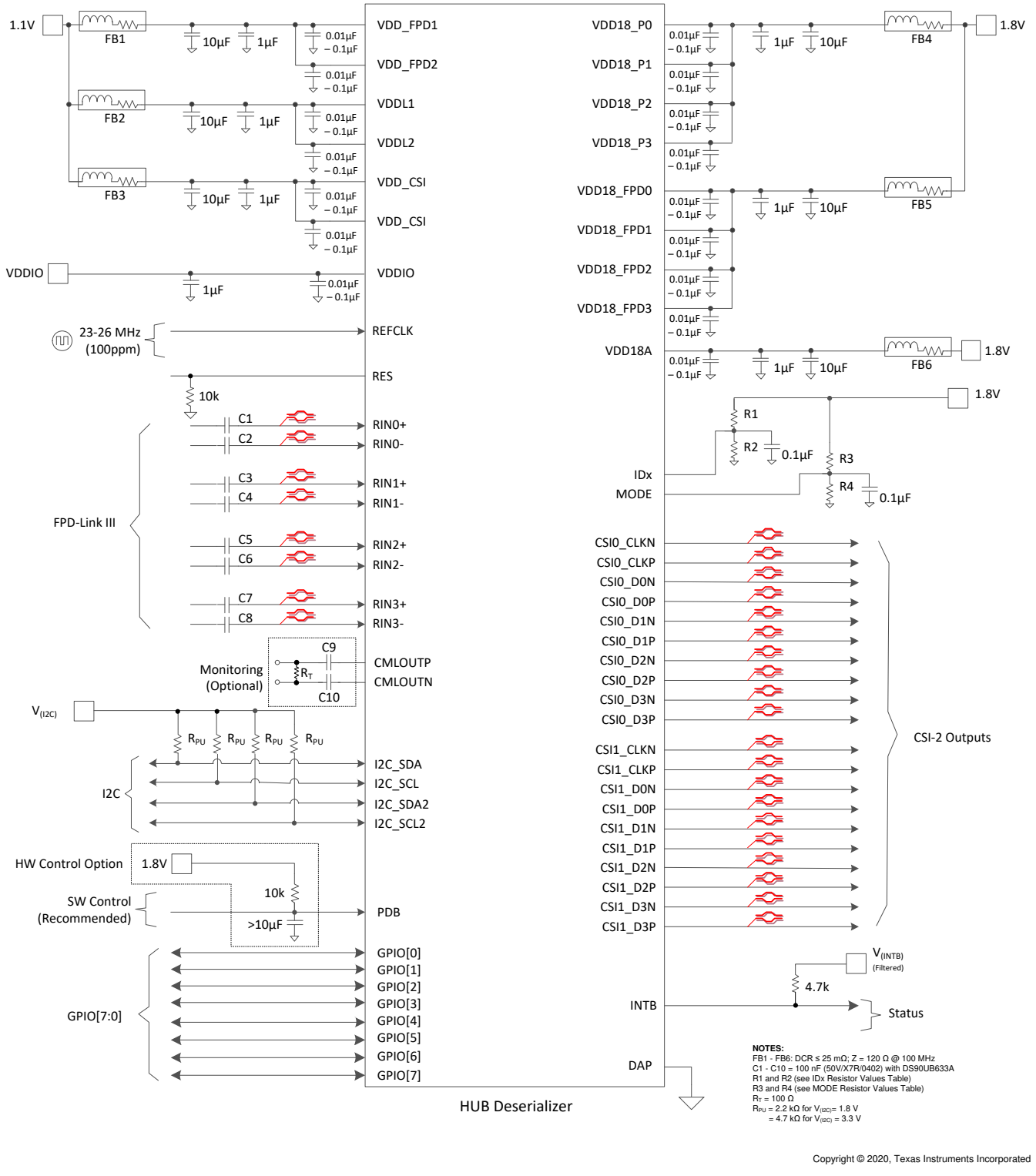

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Figure 8-5. Typical Connection Diagram (STP)

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8.2.1 Design Requirements

For the typical design application, use the parameters listed in Table 8-4.

Table 8-4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V or 3.3 V
VDD11	1.1 V
VDD18	1.8 V
AC Coupling Capacitor for STP with DS90UB63x CSI-2 Serializer: RIN[3:0]±	33 nF - 100 nF (50V/X7R/0402)
AC Coupling Capacitor for Coaxial with DS90UB63x CSI-2 Serializer: RIN[3:0]+	33 nF - 100 nF (50V/X7R/0402)
AC Coupling Capacitor for Coaxial with DS90UB63x CSI-2 Serializer: RIN[3:0]-	15 nF - 47 nF (50V/X7R/0402)
AC-Coupling Capacitor for STP with DS90UB633A-Q1: RIN[3:0]±	100 nF (50V/X7R/0402)
AC-Coupling Capacitor for Coaxial with DS90UB633A-Q1: RIN[3:0]+	100 nF (50V/X7R/0402)
AC-Coupling Capacitor for Coaxial with DS90UB633A-Q1: RIN[3:0]-	47 nF (50V/X7R/0402)

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as shown in Figure 8-6. For applications using single-ended 50-Ω coaxial cable, terminate the unused data pins (RIN0–, RIN1–, RIN2–, RIN3–) with an AC-coupling capacitor and a 50-Ω resistor.

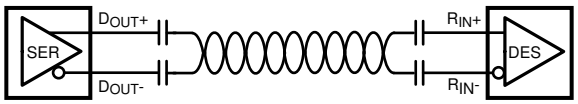

Figure 8-6. AC-Coupled Connection (STP)

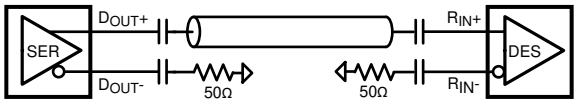

Figure 8-7. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link III transmissions, use the smallest available package for the AC-coupling capacitor to help minimize degradation of signal quality due to package parasitics.

8.2.2 Detailed Design Procedure

Figure 8-12 Figure 8-13 show typical applications of the DS90UB662-Q1 for a multi-camera surround view system. The FPD-Link III must have an external 33 to 100-nF or 15 to 47-nF, AC-coupling capacitors for coaxial interconnects. The same AC-coupling capacitor values should be matched on the paired serializer boards. The deserializer has an internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, 0.1-µF or 0.01-µF capacitors should be used for each of the core supply pins for local device bypassing. Ferrite beads are placed on the VDD18 and VDD11 supplies for effective noise suppression.

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8.2.3 Application Curves

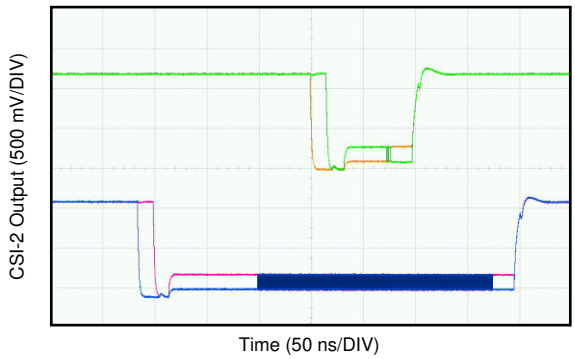

Figure 8-8. CSI-2 DATA and CLK Output

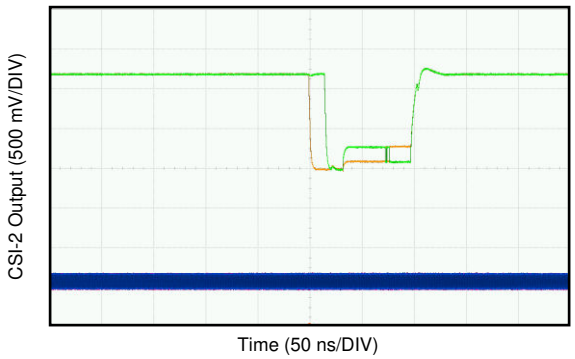

Figure 8-9. CSI-2 DATA and Continuous CLK Output

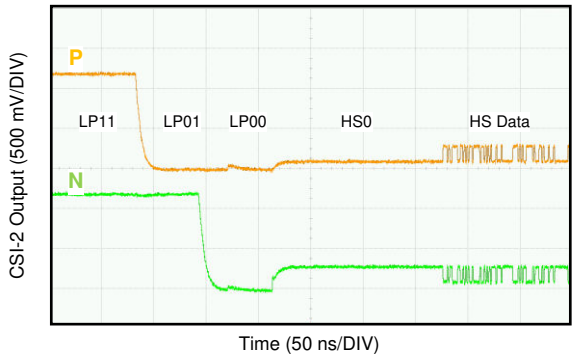

Figure 8-10. CSI-2 Start of Transmission (SoT)

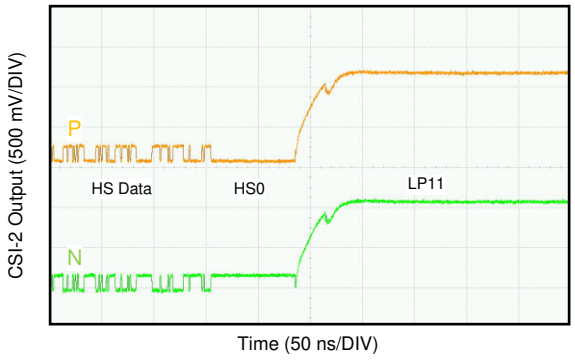

Figure 8-11. CSI-2 End of Transmission (EoT)

8.3 System Example

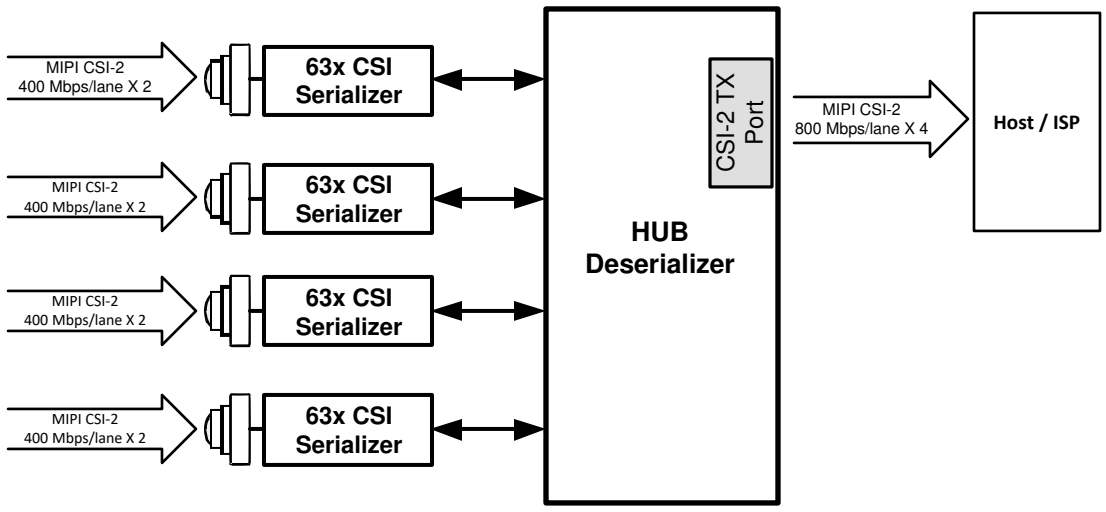

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Figure 8-12. Four DS90UB63x CSI-2 Serialzier Sensor Data Onto CSI-2

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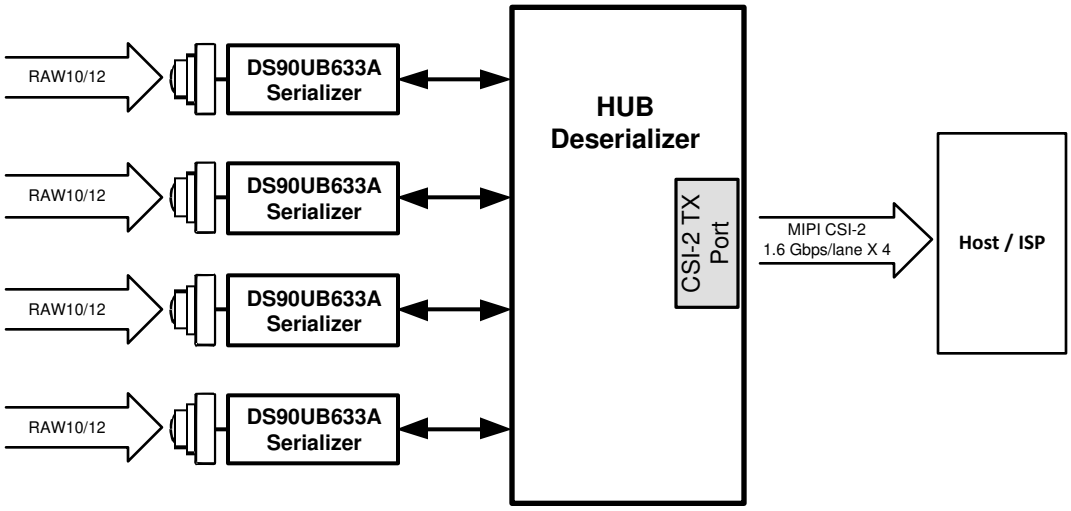

Figure 8-13. Four DS90UB633A-Q1 Sensor Data Onto CSI-2

9 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. The *Section 5* section provides guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

9.1 VDD Power Supply

Each VDD power supply pin must have a 10-nF (or 100-nF) capacitor to ground connected as close as possible to DS90UB662-Q1 device. TI recommends having additional decoupling capacitors (1 µF and 10 µF) and the pins connected to a solid power plane.

9.2 Power-Up Sequencing

The power-up sequence for the DS90UB662-Q1 is as follows:

Table 9-1. Timing Diagram for the Power-Up Sequence

PARAMETER		MIN	TYP	MAX	UNIT	NOTES
t_{r0}	VDD18 / VDDIO rise time	0.2			ms	@10/90%
t_{r1}	VDD11 rise time	0.05			ms	@10/90%
t_0	VDD18 / VDDIO to VDD11 delay	0			ms	
t_1	VDDx to REFCLK delay	0			ms	Keep REFCLK low until all supplies are up and stable.
t_2	VDDx to PDB delay	0			ms	Release PDB after all supplies are up and stable.
t_3	PDB to I2C ready (IDX and MODE valid) delay	2			ms	
t_4	PDB pulse width	2			ms	Hard reset
t_5	PDB to GPIO delay	0			ms	Keep GPIOs low or high until PDB is high.

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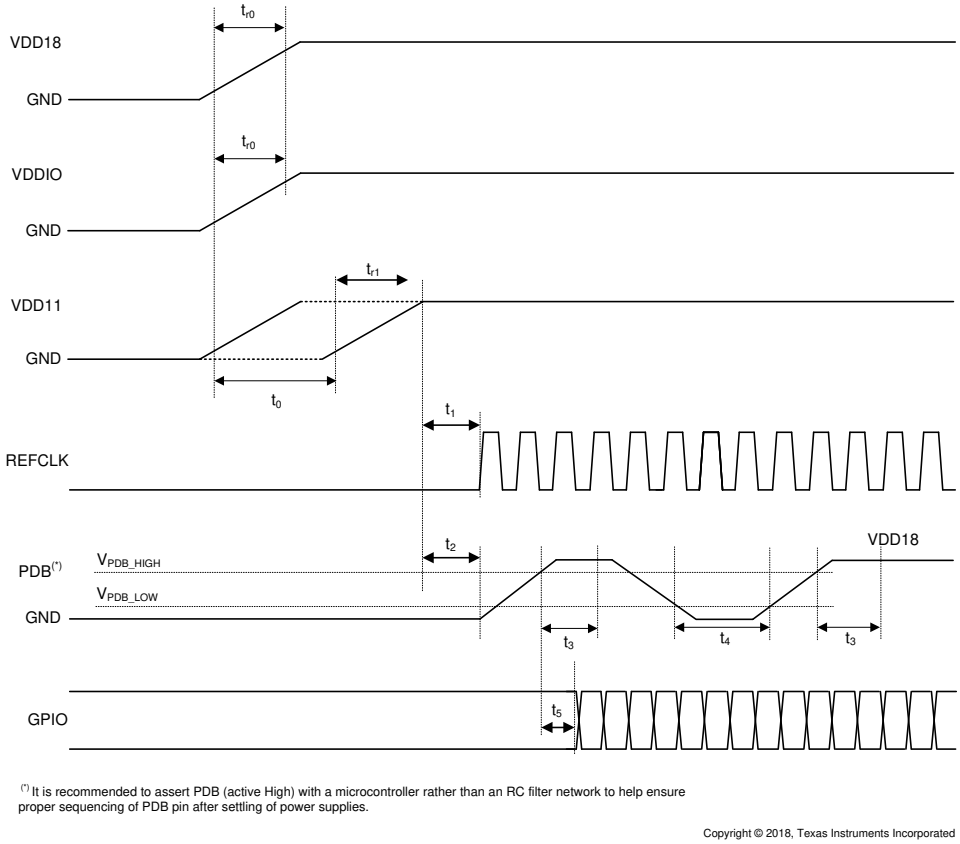

Figure 9-1. Power-Up Sequencing

9.2.1 PDB Pin

The PDB pin is active HIGH and must remain LOW while the VDD pin power supplies are in transition. An external RC network on the PDB pin may be connected to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to VDD18, a 10-kΩ pullup and a > 10-µF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until both power supplies have reached steady state.

Table 9-2. PDB Reset Signal Pulse Width

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PDB						
t_{LRST}	PDB Reset Low Pulse		2			ms

9.2.2 System Initialization

When initializing the communications link between the DS90UB662-Q1 deserializer hub and a DS90UB633A-Q1 serializer, the system timing will depend on the mode selected for generating the serializer reference clock. When synchronous clocking mode is selected, the serializer will re-lock onto the extracted back channel reference clock once available, so there is no need for local crystal oscillator at the sensor module (Figure 9-2). When the DS90UB633A-Q1 is operating in non-synchronous mode, or is connecting to DS90UB633A-Q1 serializer, the sensor module requires a local reference clock and the timing would follow Figure 9-3.

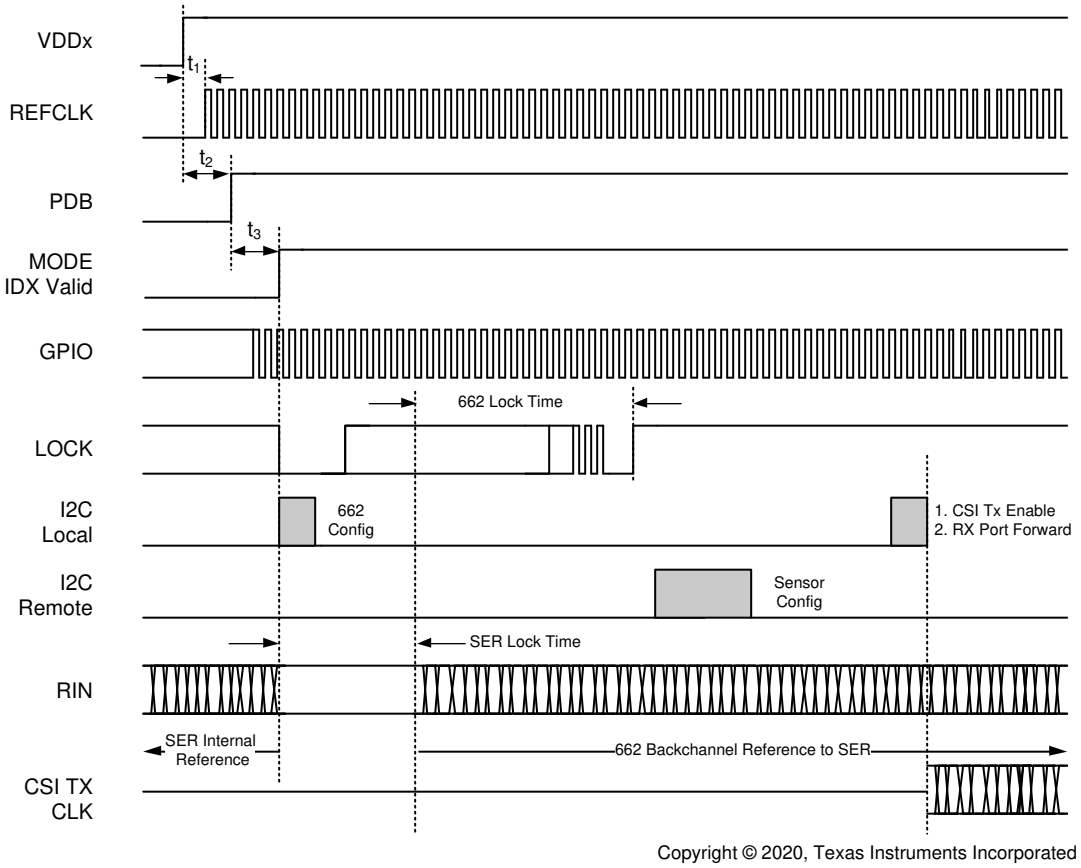

Figure 9-2. Power-Up Sequencing With Synchronous Clocking Mode

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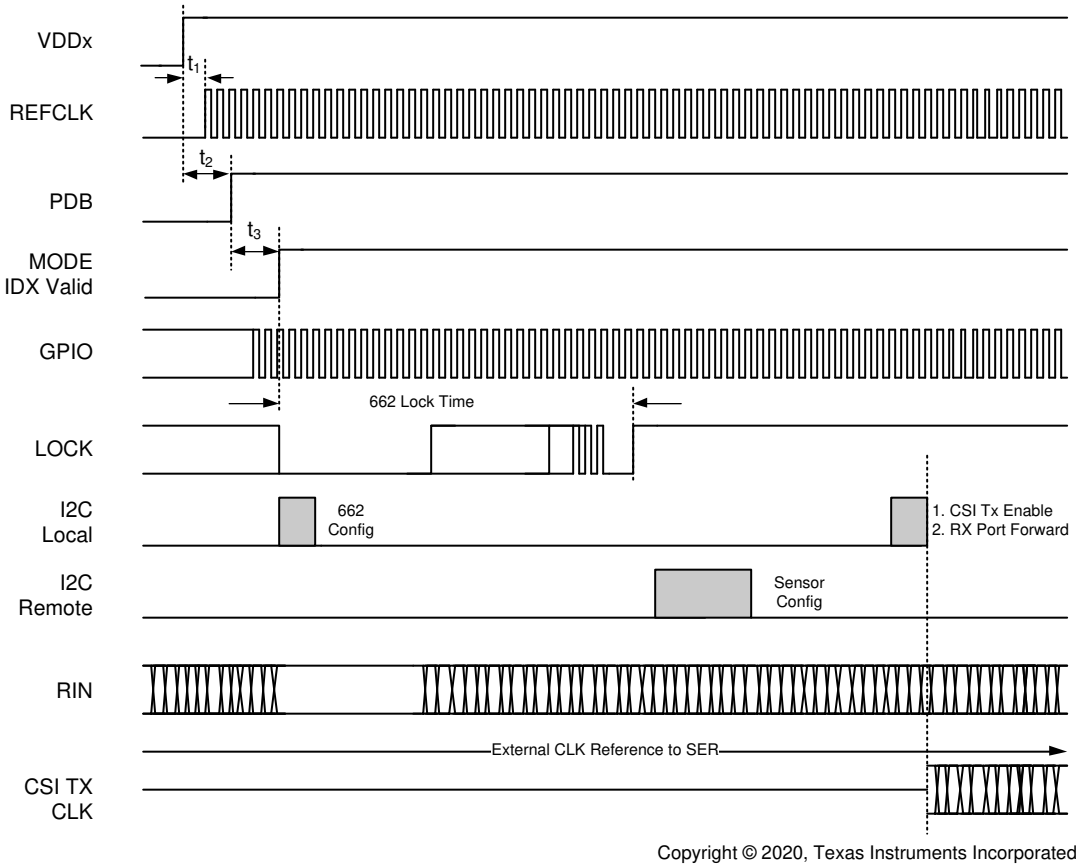

Figure 9-3. Power-Up Sequencing With Non-Synchronous Clocking Mode

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the FPD-Link III devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise pick-up, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power/ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Ceramic capacitors may be in the 2.2-µF to 10-µF range. The voltage rating of the ceramic capacitors must be at least 5× the power supply voltage being used

TI recommends surface-mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, place the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50-µF to 100-µF range, which smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. The small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also common practice to use two vias from power and ground pins to the planes to reduce the impedance at high frequency.

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Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Differential impedance of 100 Ω are typically recommended for STP interconnect and single-ended impedance of 50 Ω for coaxial interconnect. The closely coupled lines help to ensure that coupled noise appears as common-mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

10.1.1 Ground

TI recommends that a consistent ground plane reference for the high-speed signals in the PCB design to provide the best image plane for signal traces running parallel to the plane. Connect the thermal pad of the DS90UB662-Q1 to this plane with vias.

10.1.2 Routing FPD-Link III Signal Traces and PoC Filter

Routing the FPD-Link III signal traces between the R_{IN} pins and the connector as well as connecting the PoC filter to these traces are the most critical pieces of a successful DS90UB662-Q1 PCB layout. Figure 10-1 shows an example PCB layout of the DS90UB662-Q1 configured for interface to remote sensor modules over coaxial cables. The layout example also uses a footprint of an edge-mount Quad Mini-FAKRA connector provided by Rosenberger. For additional PCB layout details of the example, refer to the *DS90UB960-Q1EVM User's Guide* (SNLU226).

The following list provides essential recommendations for routing the FPD-Link III signal traces between the DS90UB662-Q1 receiver input pins (R_{IN}) and the FAKRA connector, and connecting the PoC filter.

- The routing of the FPD-Link III traces may be all on the top layer (as shown in the example) or partially embedded in middle layers if EMI is a concern.
- The AC-coupling capacitors should be on the top layer and very close to the DS90UB662-Q1 receiver input pins to minimize the length of coupled differential trace pair between the pins and the capacitors.
- Route the RIN+ trace between the AC-coupling capacitor and the FAKRA connector as a 50-Ω single-ended micro-strip with tight impedance control (±10%). Calculate the proper width of the trace for a 50-Ω impedance based on the PCB stack-up. Ensure that the trace can carry the PoC current for the maximum load presented by the remote sensor module.
- The PoC filter should be connected to the RIN+ trace through the first ferrite bead (FB_1). The FB_1 should be touching the high-speed trace to minimize the stub length seen by the transmission line. Create an anti-pad or a moat under the FB_1 pad that touches the trace. The anti-pad should be a plane cutout of the ground plane directly underneath the top layer without cutting out the ground reference under the trace. The purpose of the anti-pad is to maintain the impedance as close to 50 Ω as possible.
- Route the RIN– trace with minimum coupling to the RIN+ trace (S > 3W).
- Consult with connector manufacturer for optimized connector footprint. If the connector is mounted on the same side as the IC, minimize the impact of the thru-hole connector stubs by routing the high-speed signal traces on the opposite side of the connector mounting side.

When configured for STP and routing differential signals to the DS90UB662-Q1 receiver inputs, the traces should maintain a 100-Ω differential impedance routed to the connector. When choosing to implement a common mode choke for common mode noise reduction, take care to minimize the effect of any mismatch.

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10.1.3 CSI-2 Guidelines

1. Route CSI0_D*P/N and CSI1_D*P/N pairs with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).
2. Keep away from other high-speed signals.
3. Keep intra-pair length mismatch to < 5 mils.
4. Keep inter-pair length mismatch to < 50 mils within a single CSI-2 TX port. CSI-2 TX Port 0 differential traces do not need to match CSI-2 Port 1 differential traces.
5. Length matching should be near the location of mismatch.
6. Each pair should be separated at least by 3 times the signal trace width.
7. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bend should be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
8. Route all differential pairs on the same layer.
9. Keep the number of VIAS to a minimum — TI recommends keeping the VIA count to 2 or fewer.
10. Keep traces on layers adjacent to ground plane.
11. Do NOT route differential pairs over any plane split.
12. Adding Test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Test points must not be placed in a manner that causes a stub on the differential pair.

10.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the VQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP.

Example PCB layout is used to demonstrate both proper routing and proper solder techniques when designing in the Deserializer.

Figure 10-1 shows a PCB layout example are derived from the layout design of the DS90UB662-Q1EVM Evaluation Board. The graphic and layout description are used to determine proper routing when designing the board. The high-speed FPD-Link III traces routed differentially up to the connector. A 100-Ω differential characteristic impedance and 50-Ω single-ended characteristic impedance traces are maintained as much as possible for both STP and coaxial applications. For the layout of a coaxial interconnects, coupled traces should be used with the RINx- termination near to the connector.

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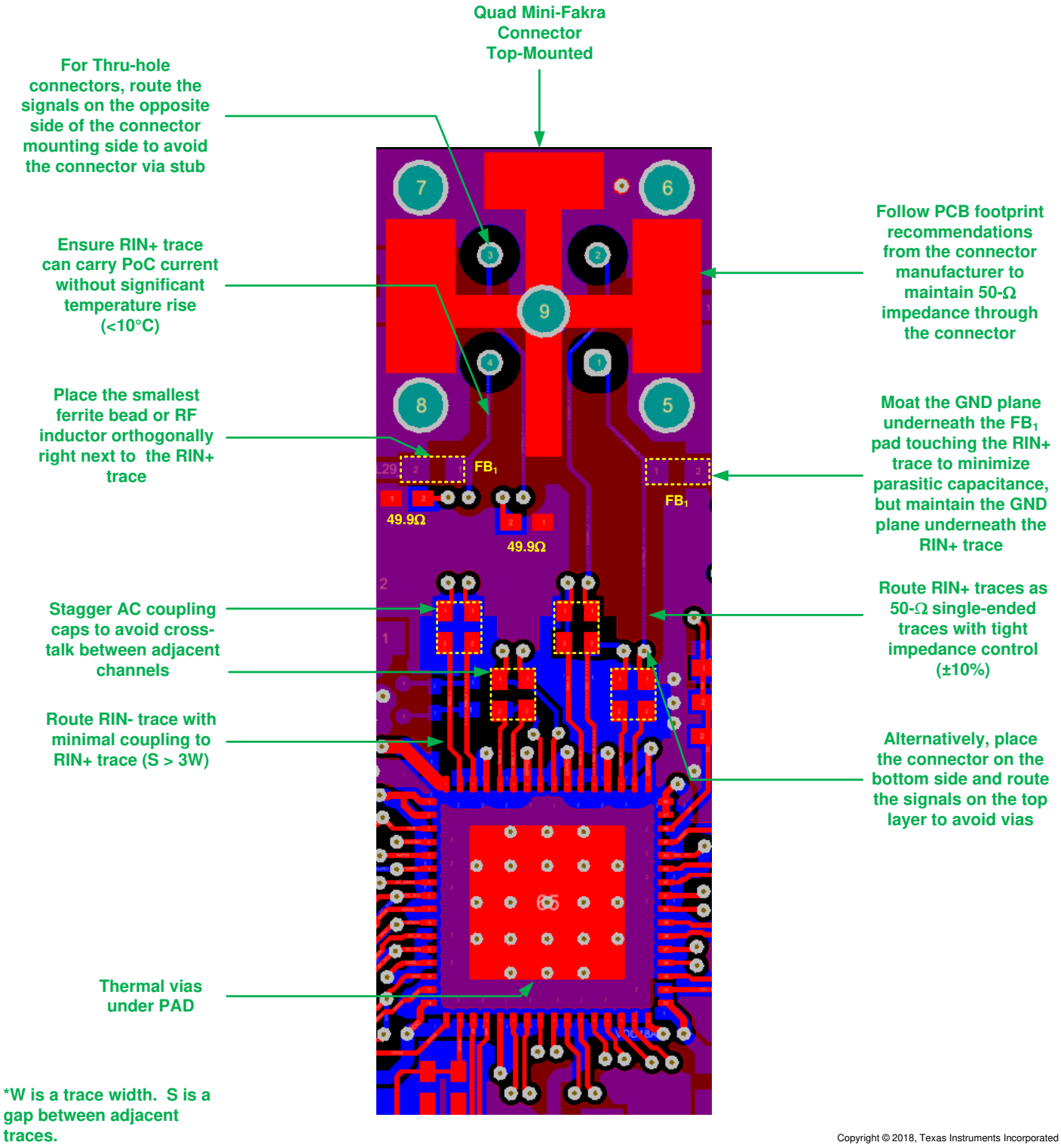

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Figure 10-1. DS90UB662-Q1 Example PCB Layout With Quad Mini-Fakra Connector

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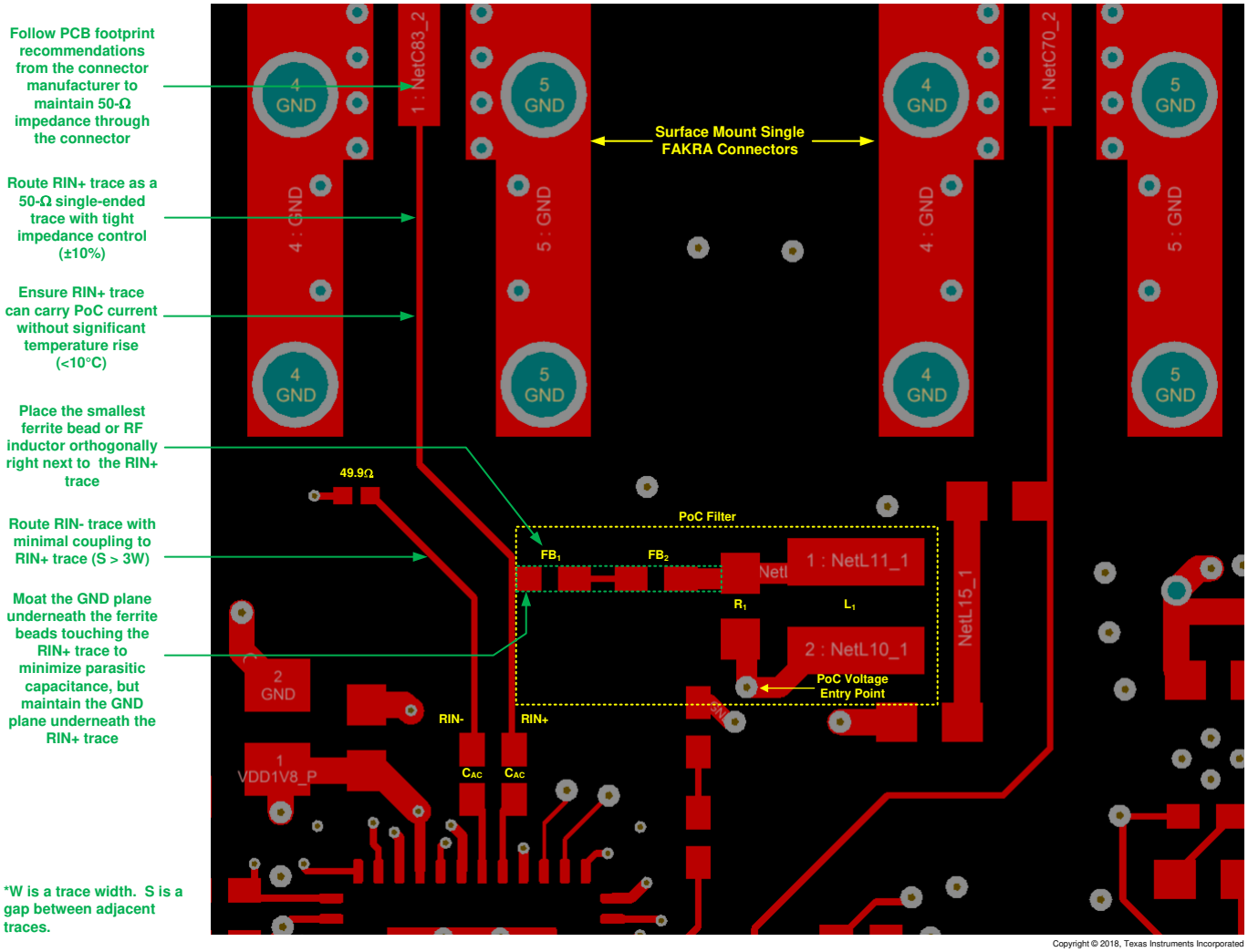

Figure 10-2. Example Routing of FPD-Link III Traces to a Single Mini-Fakra Connector and PoC Components

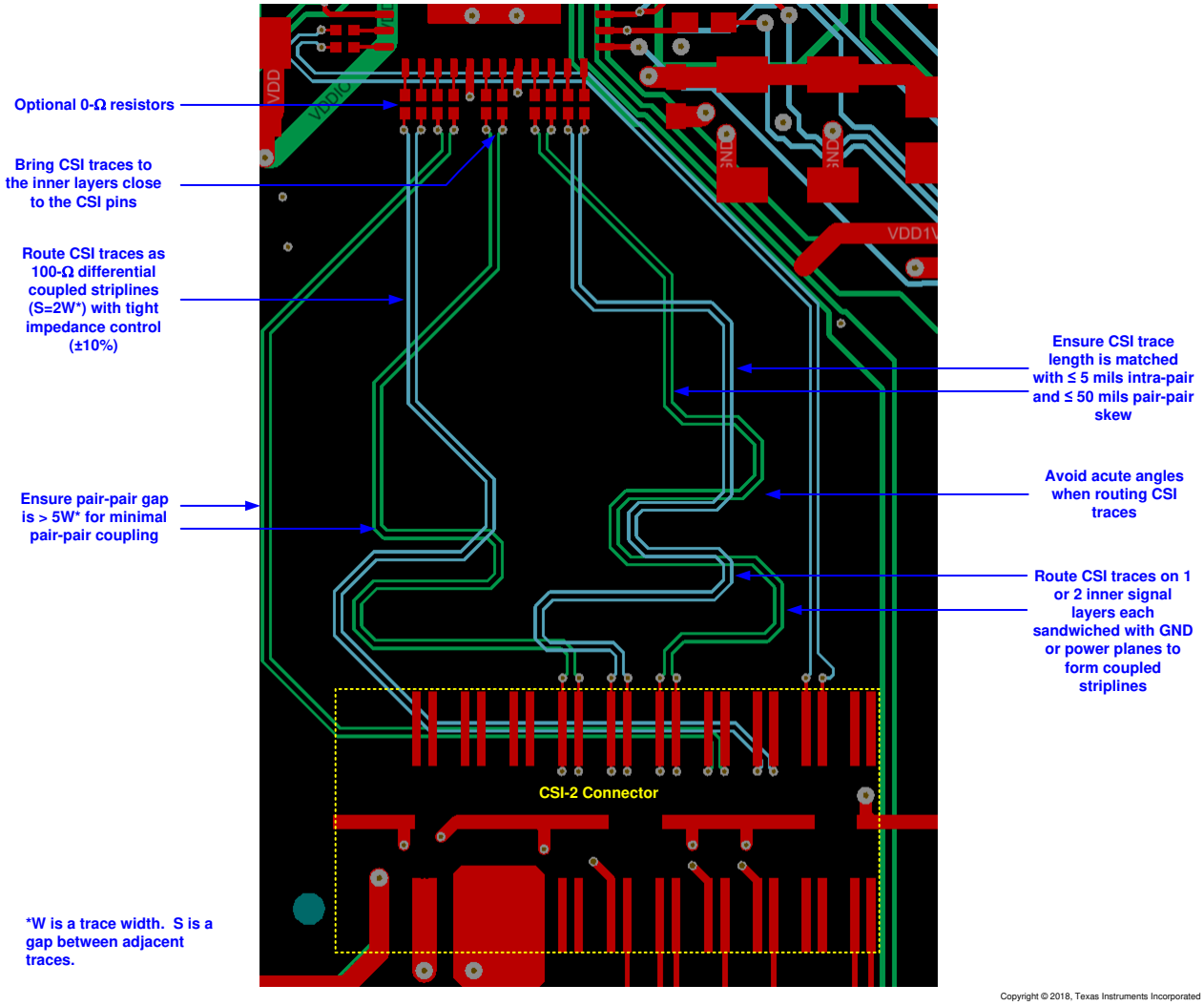

Figure 10-3. Example Routing of CSI-2 Traces

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

-
- *Sending Power over Coax in DS90UB913A Designs* (SNLA224)
- *I2C Over DS90UB913/4 FPD-Link III With Bidirectional Control Channel* (SNLA222)
- *DS90UB960-Q1EVM User's Guide* (SNLU226)
- *I2C Communication Over FPD-Link III With Bidirectional Control Channel* (SNLA131)
- *I2C Bus Pullup Resistor Calculation* (SLVA689)
- FPD-Link University Training Material
- *An EMC/EMI System-Design and Testing Methodology for FPD-Link III SerDes* (SLYT719)
- *Ten Tips for Successfully Designing With Automotive EMC/EMI Requirements* (SLYT636) (SLYT636)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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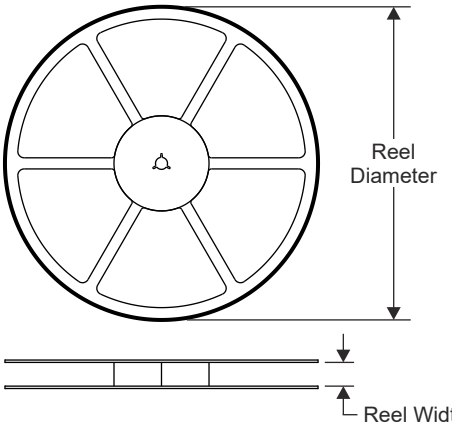
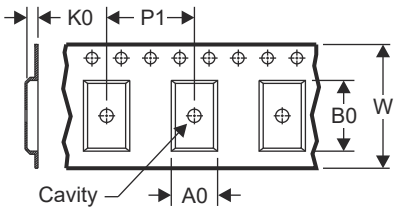
Tape and Reel Information

REEL DIMENSIONS

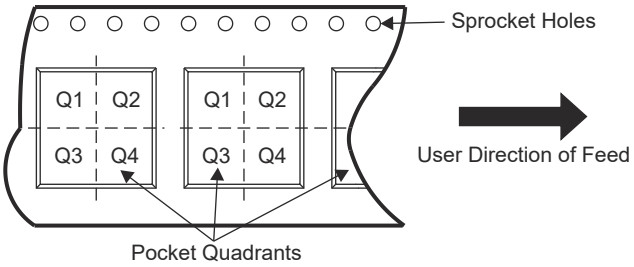


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB662WRTDRQ1	VQFN	RTD	64	2000	330	16.4	9.3	9.3	1.1	12	16	Q2
DS90UB662WRTDRQ1	VQFN	RTD	64	250	180	16.4	9.3	9.3	1.1	12	16	Q2

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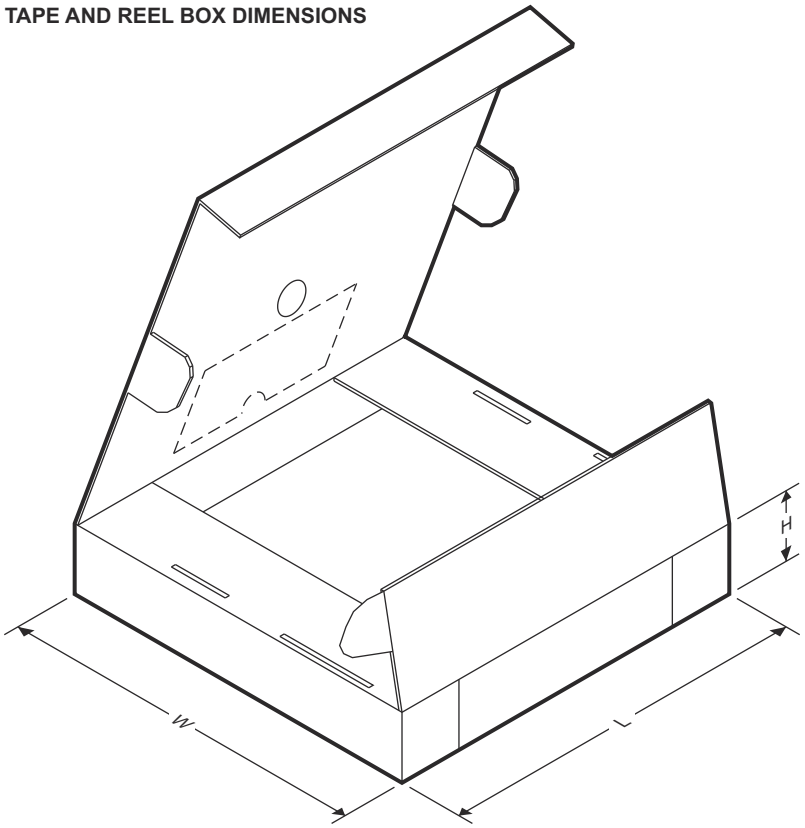
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB662WRTDRQ1	VQFN	RTD	64	2000	367	367	38
DS90UB662WRTDRQ1	VQFN	RTD	64	250	210	185	35

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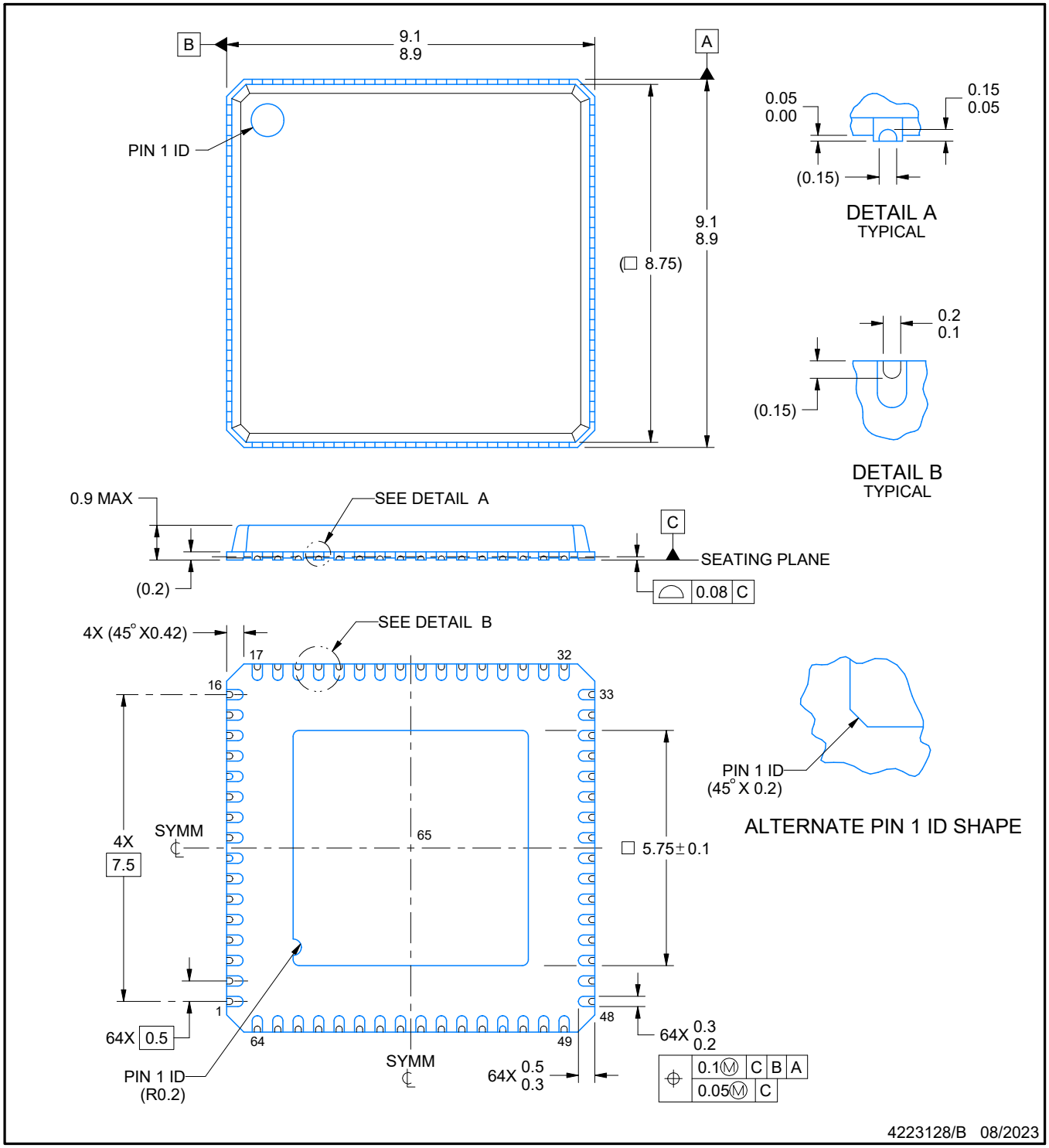
PACKAGE OUTLINE

RTD0064F

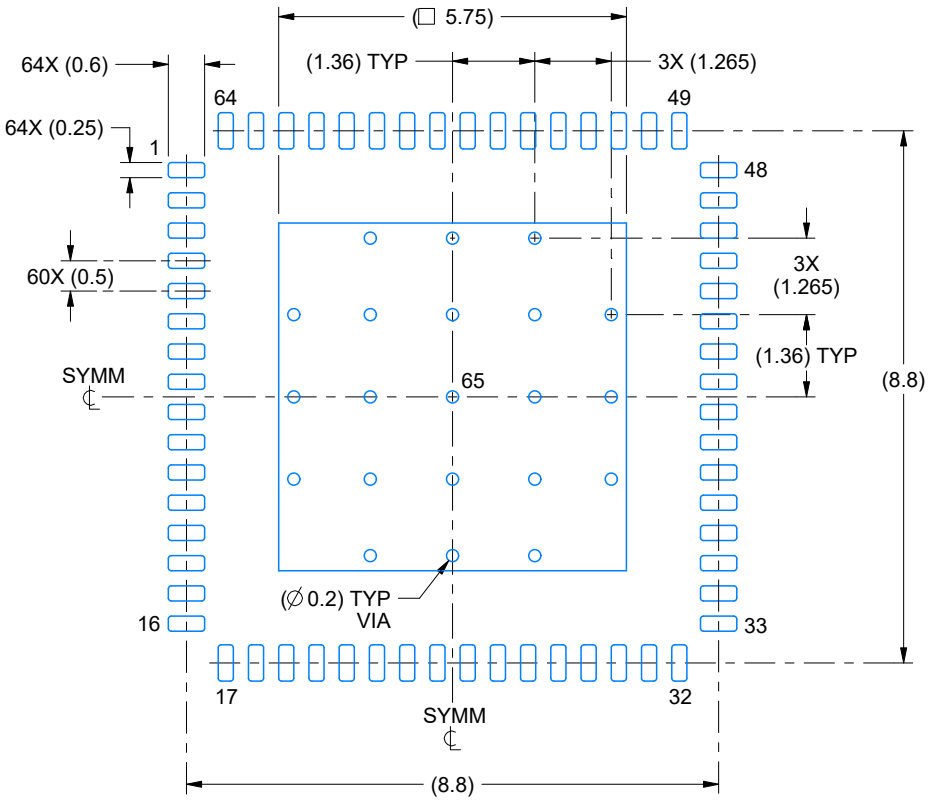
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

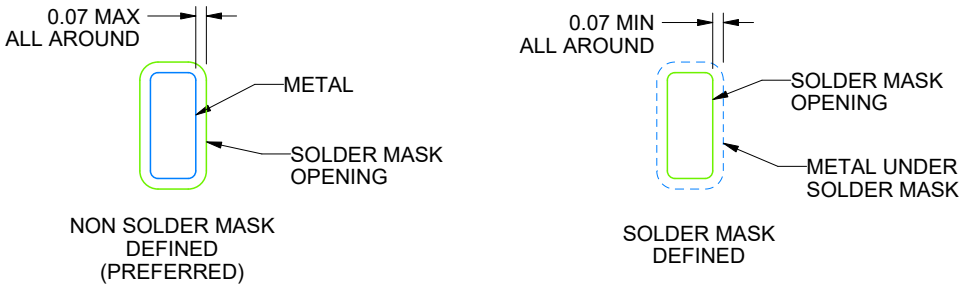


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X

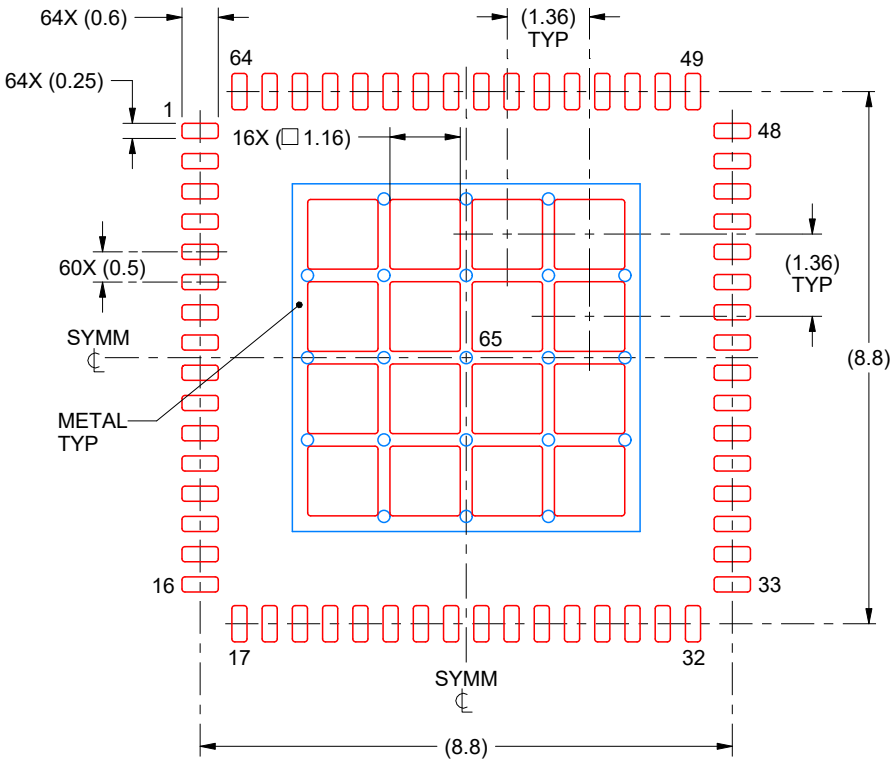


SOLDER MASK DETAILS

4223128/B 08/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 65:
65% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:8X

4223128/B 08/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90UB662WRTDRQ1	Active	Production	VQFN (RTD) | 64	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	UB662Q
DS90UB662WRTDRQ1.A	Active	Production	VQFN (RTD) | 64	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	UB662Q
DS90UB662WRTDTQ1	Active	Production	VQFN (RTD) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	UB662Q
DS90UB662WRTDTQ1.A	Active	Production	VQFN (RTD) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	UB662Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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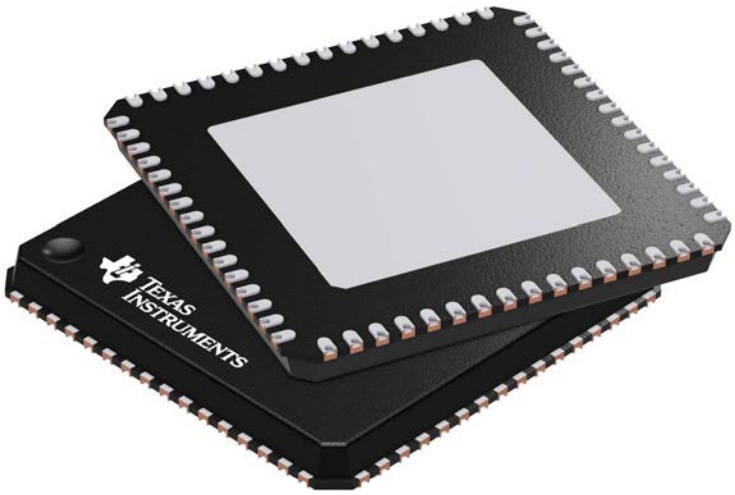
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

RTD 64

VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



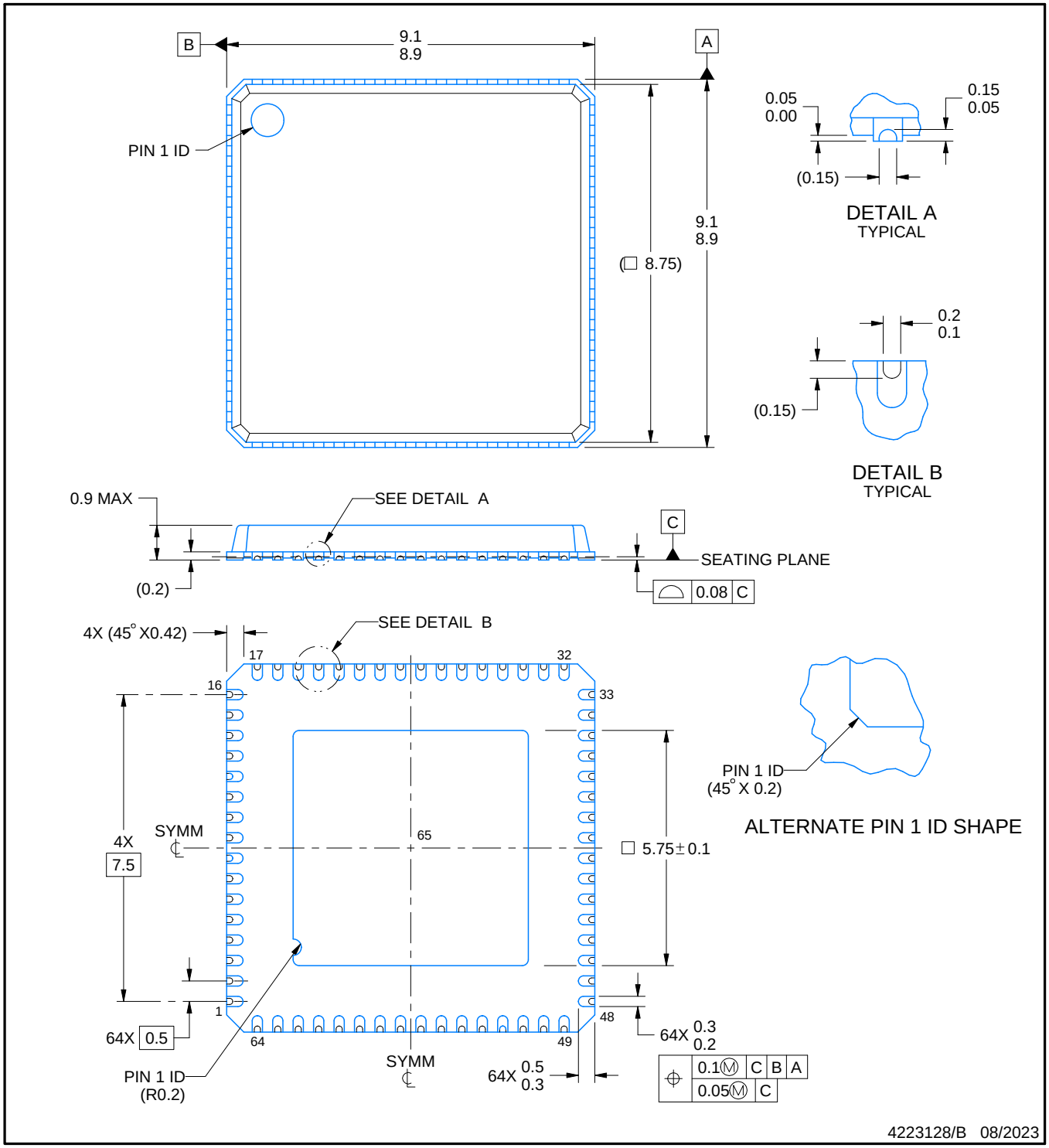
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RTD0064F

PACKAGE OUTLINE

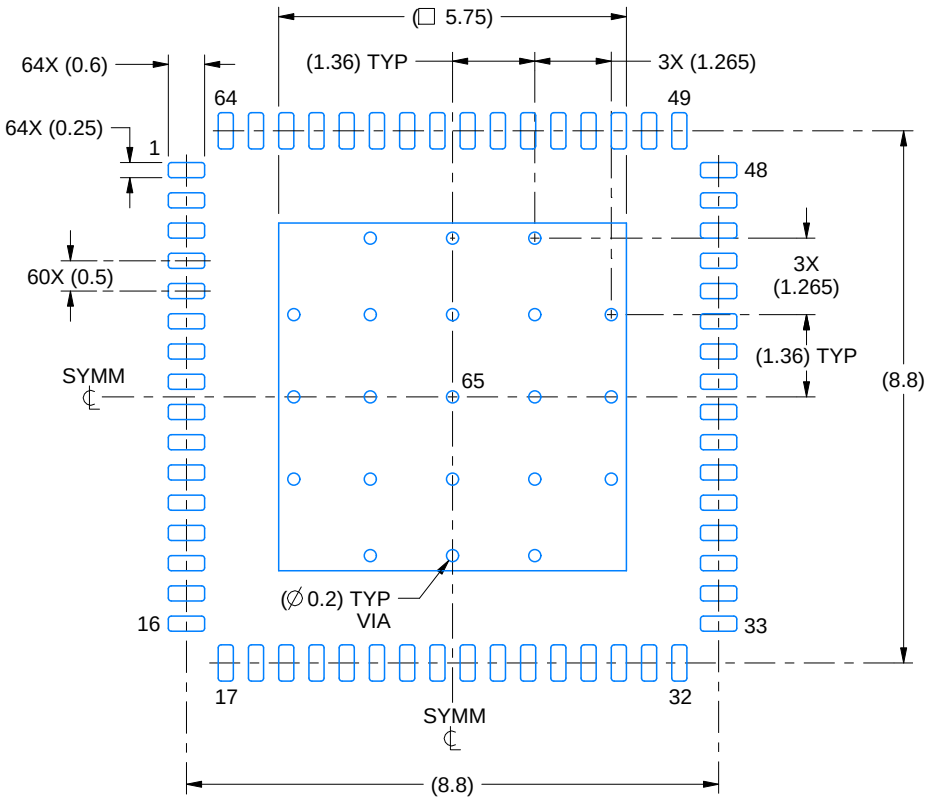
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

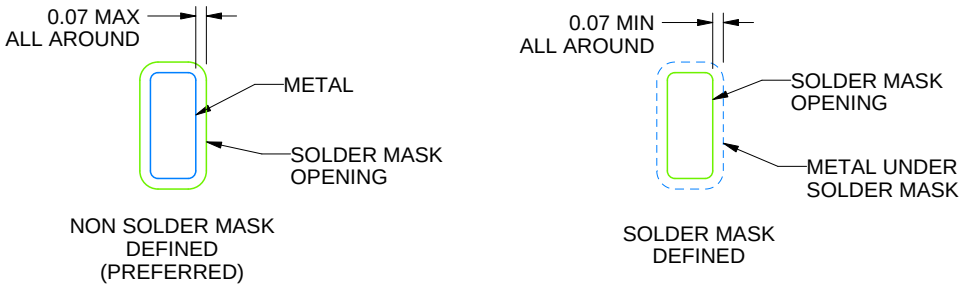


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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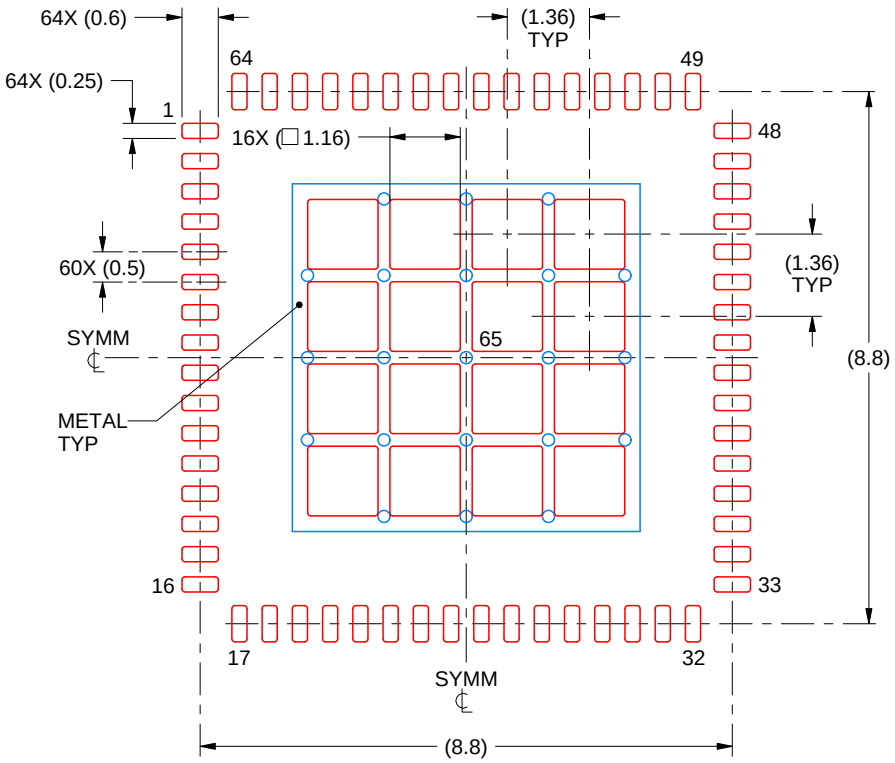
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 65:
65% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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