



INA217 Low-Noise, Low-Distortion Instrumentation Amplifier Replacement for SSM2017

1 Features

- Low Noise: $1.3 \text{ nV/M} \sqrt{\text{Hz}}$ at 1 kHz
- Low THD+N: 0.004% at 1 kHz, $G = 100$
- Wide Bandwidth: 800 kHz at $G = 100$
- Wide Supply Range: $\pm 4.5 \text{ V}$ to $\pm 18 \text{ V}$
- High CMR: $> 100 \text{ dB}$
- Gain Set With External Resistor
- DIP-8 and SOL-16 Widebody Packages

2 Applications

- Professional Microphone Preamps
- Moving-coil Transducer Amplifiers
- Differential Receivers
- Bridge Transducer Amplifiers

3 Description

The INA217 device is a low-noise, low-distortion, monolithic instrumentation amplifier. Current-feedback circuitry allows the INA217 device to achieve wide bandwidth and excellent dynamic response over a wide range of gain. The INA217 device is ideal for low-level audio signals such as balanced low-impedance microphones. Many industrial, instrumentation, and medical applications also benefit from its low noise and wide bandwidth.

Unique distortion cancellation circuitry reduces distortion to extremely low levels, even in high gain. The INA217 device provides near-theoretical noise performance for 200- Ω source impedance. The INA217 device features differential input, low noise, and low distortion that provides superior performance in professional microphone amplifier applications.

The INA217 device features wide supply voltage, excellent output voltage swing, and high output current drive, making it an optimal candidate for use in high-level audio stages.

The INA217 device is available in the same DIP-8 and SOL-16 wide body packages and pinouts as the SSM2017. For a smaller package, see the INA163 device in SO-14 narrow. The INA217 device is specified over the temperature range of -40°C to 85°C .

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA217	SOIC (16)	10.30 mm $\times$ 7.50 mm
	PDIP (8)	9.81 mm $\times$ 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



INA217

SBOS247C – JUNE 2002 – REVISED NOVEMBER 2015

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Simplified Schematic

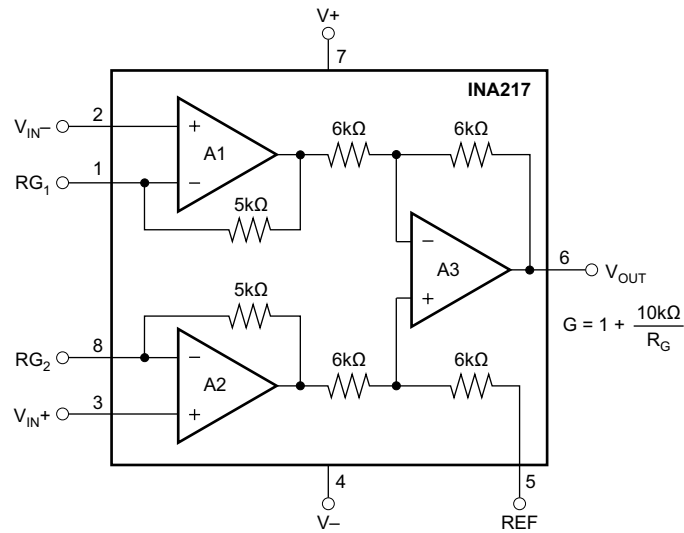


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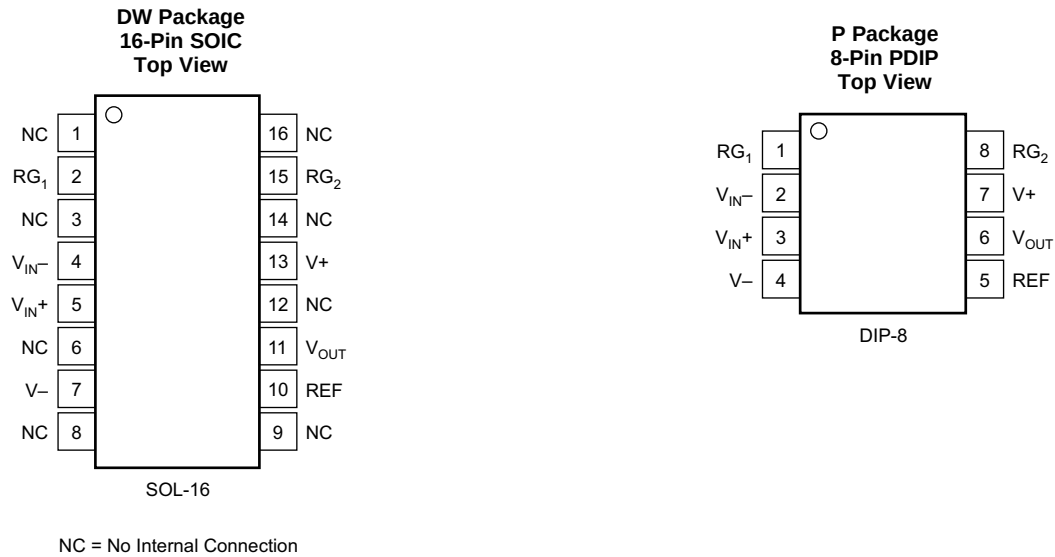
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2005) to Revision C	Page
Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
PDIP			
NC	1	—	No internal connection
RG1	2	I	Gain setting pin, for gains greater than one, connect an external resistor between pins 2 and 15
NC	3	—	No internal connection
VIN–	4	I	Inverting input
VIN+	5	I	Non-inverting input
NC	6	—	No internal connection
V–	7	I	negative power supply
NC	8	—	No internal connection
NC	9	—	No internal connection
REF	10	I	Reference input
VOUT	11	O	Output
NC	12	—	No internal connection
V+	13	I	Positive power supply
NC	14	—	No internal connection
RG2	15	I	Gain setting pin, for gains greater than one, connect an external resistor between pins 2 and 15
NC	16	—	No internal connection
SOIC			
RG1	1	I	Gain setting pin, for gains greater than one, connect an external resistor between pins 1 and 8
VIN–	2	I	Inverting input
VIN+	3	I	Non-inverting input
V–	4	I	negative power supply
REF	5	I	Reference input
VOUT	6	O	Output
V+	7	I	Positive power supply
RG2	8	I	Gain setting pin, for gains greater than one, connect an external resistor between pins 2 and 15

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V+ to V–	Supply voltage		±18	V
Signal input terminals	Voltage ⁽²⁾	(V–) – 0.5	(V+) + 0.5	V
	Current ⁽²⁾		10	mA
Output short circuit ⁽³⁾		Continuous		
Operating temperature		–55	125	°C
Junction temperature			300	°C
T _{stg}	Storage temperature	–55	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
- Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge		
	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+ to V–	Supply voltage	±4.5	±15	±18	V
T _A	Ambient Temperature	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA217		UNIT
		DW (SOIC)	P (PDIP)	
		16 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	64.3	46.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	24.9	34.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	29.4	23.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	3.3	11.7	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	28.8	23.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics: $V_S = \pm 15\text{ V}$

$T_A = 25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$, $V_S = \pm 15\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	$T_A = 25^\circ\text{C}$			UNIT
			MIN	TYP	MAX	
GAIN EQUATION⁽¹⁾			$G = 1 + 10\text{k}/R_G$			
Range			1 to 10000			V/V
Gain Error	$G = 1$			$\pm 0.1\%$	$\pm 0.25\%$	
	$G = 10$			$\pm 0.2\%$	$\pm 0.7\%$	
	$G = 100$			$\pm 0.2\%$		
	$G = 1000$			$\pm 0.5\%$		
GAIN TEMPERATURE DRIFT COEFFICIENT						
$G = 1$		$T_A = -40^\circ\text{C}$ to 85°C		± 3	± 10	ppm/ $^\circ\text{C}$
$G > 10$		$T_A = -40^\circ\text{C}$ to 85°C		± 40	± 100	ppm/ $^\circ\text{C}$
Nonlinearity	$G = 1$			± 0.0003		% of FS
	$G = 100$			± 0.0006		% of FS
INPUT STAGE NOISE						
Voltage Noise	$f_O = 1\text{ kHz}$	$R_{\text{SOURCE}} = 0\ \Omega$		1.3		nV/ $\sqrt{\text{Hz}}$
	$f_O = 100\text{ Hz}$			1.5		nV/ $\sqrt{\text{Hz}}$
	$f_O = 10\text{ Hz}$			3.5		nV/ $\sqrt{\text{Hz}}$
Current Noise, $f_O = 1\text{ kHz}$				0.8		pA/ $\sqrt{\text{Hz}}$
OUTPUT STAGE NOISE						
Voltage Noise, $f_O = 1\text{ kHz}$				90		nV/ $\sqrt{\text{Hz}}$
INPUT OFFSET VOLTAGE						
Input Offset Voltage		$V_{\text{CM}} = V_{\text{OUT}} = 0\text{ V}$		$50 + 2000/G$	$250 + 5000/G$	μV
vs Temperature		$T_A = -40^\circ\text{C}$ to 85°C		$1 + 20/G$		$\mu\text{V}/^\circ\text{C}$
vs Power Supply		$V_S = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$		$1 + 50/G$	$3 + 200/G$	$\mu\text{V/V}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range		$V_{\text{IN}+} - V_{\text{IN}-} = 0\text{ V}$	$(V+) - 4$	$(V+) - 3$		V
		$V_{\text{IN}+} - V_{\text{IN}-} = 0\text{ V}$	$(V-) + 4$	$(V-) + 3$		V
Common-Mode Rejection	$G = 1$	$V_{\text{CM}} = \pm 11\text{ V}$, $R_{\text{SRC}} = 0\ \Omega$	70	80		dB
	$G = 100$		100	116		dB
INPUT BIAS CURRENT						
Initial Bias Current				2	12	μA
vs Temperature		$T_A = -40^\circ\text{C}$ to 85°C		10		nA/ $^\circ\text{C}$
Initial Offset Current				0.1	1	μA
vs Temperature		$T_A = -40^\circ\text{C}$ to 85°C		0.5		nA/ $^\circ\text{C}$
INPUT IMPEDANCE						
		Differential		$60 \parallel 2$		M $\Omega \parallel$ pF
		Common-Mode		$60 \parallel 2$		M $\Omega \parallel$ pF
DYNAMIC RESPONSE						
Bandwidth, Small Signal, -3d B						
$G = 1$				3.4		MHz
$G = 100$				800		kHz
Slew Rate				15		V/ μs
THD+Noise, $f = 1\text{ kHz}$		$G = 100$		0.004%		
Settling Time	0.1%	$G = 100$, 10V Step		2		μs
	0.01%	$G = 100$, 10V Step		3.5		μs
Overload Recovery		50% Overdrive		1		μs

(1) Gain accuracy is a function of external R_G .

Electrical Characteristics: $V_S = \pm 15\text{ V}$ (continued)
 $T_A = 25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$, $V_S = \pm 15\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	T _A = 25°C			UNIT
		MIN	TYP	MAX	
OUTPUT					
Voltage	R _L to GND	(V+) – 2 (V–) + 2	(V+) – 1.8 (V–) + 1.8		V V
Load Capacitance Stability			1000		pF
Short Circuit Current	Continuous-to-Common		±60		mA
POWER SUPPLY					
Rated Voltage			±15		V
Voltage Range		±4.5		±18	V
Current, Quiescent	I _O = 0 mA		±10	±12	mA
TEMPERATURE RANGE					
Specification		–40		85	°C
Operating		–40		125	°C

6.6 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 2\text{ k}\Omega$, unless otherwise noted.

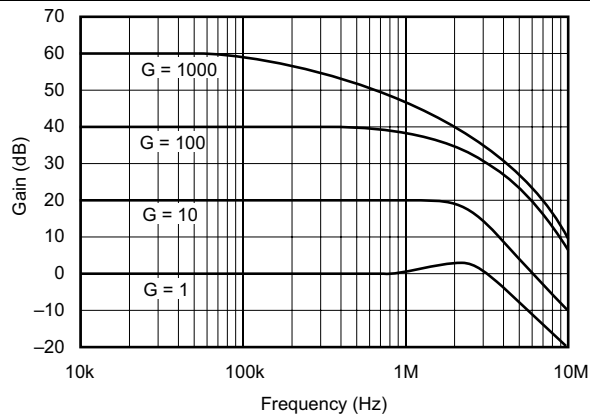


Figure 1. Gain vs Frequency

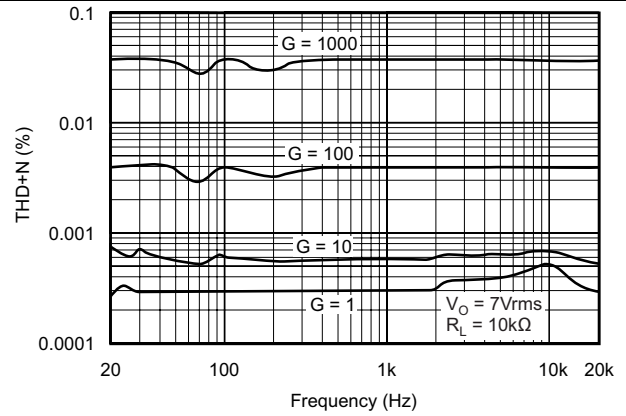


Figure 2. THD+N vs Frequency

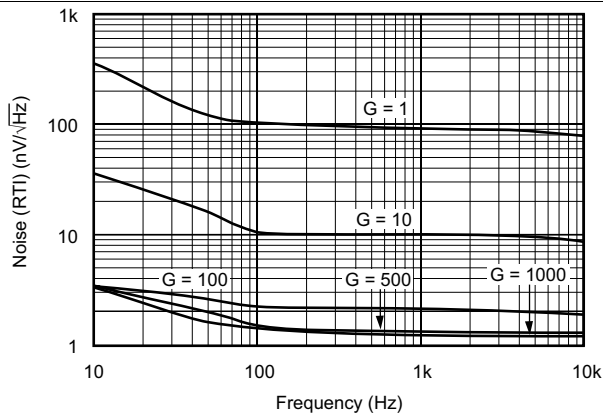


Figure 3. Noise Voltage (RTI) vs Frequency

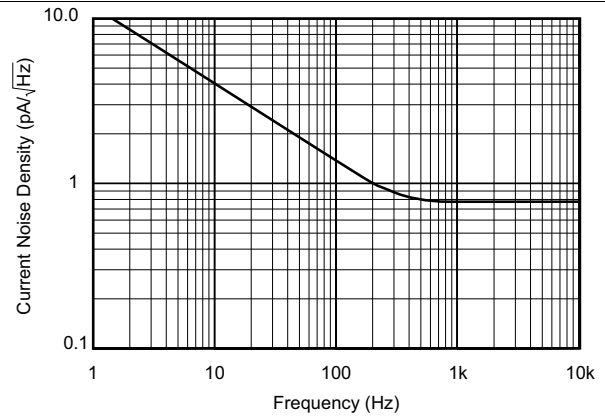


Figure 4. Current Noise Spectral Density

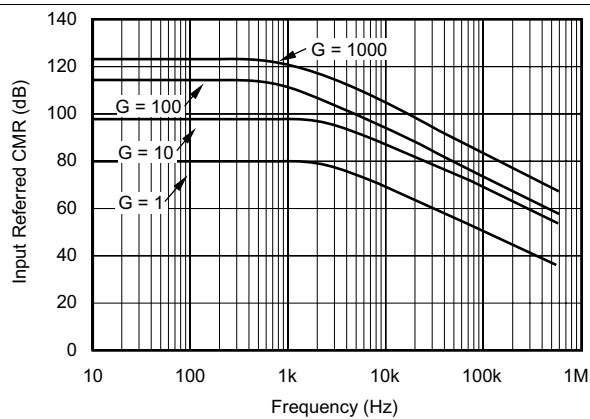


Figure 5. CMR vs Frequency

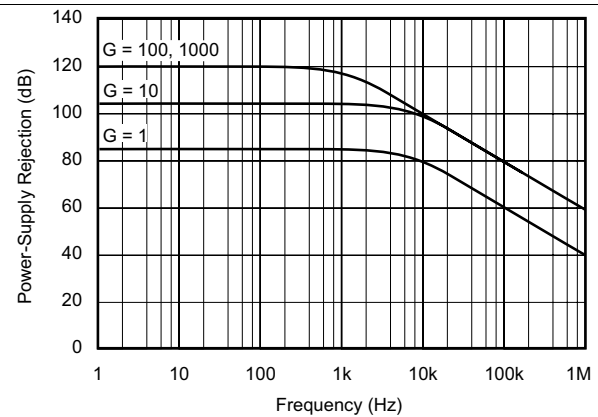


Figure 6. Power-Supply Rejection vs Frequency

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 2\text{ k}\Omega$, unless otherwise noted.

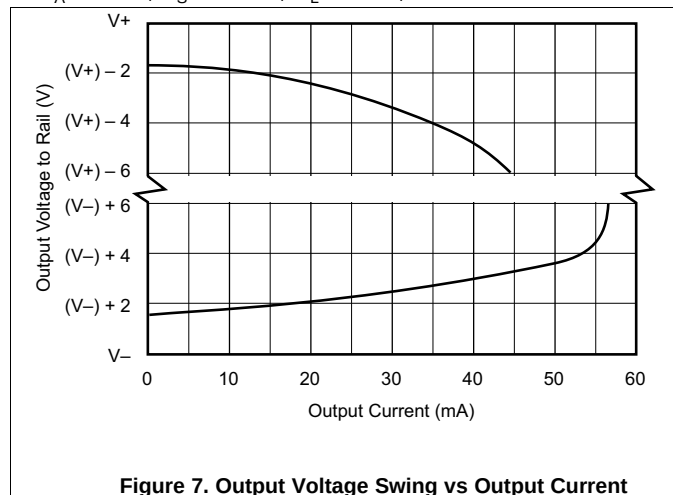


Figure 7. Output Voltage Swing vs Output Current

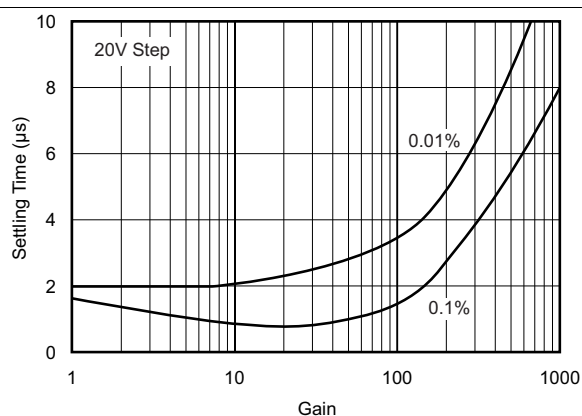


Figure 8. Settling Time vs Gain

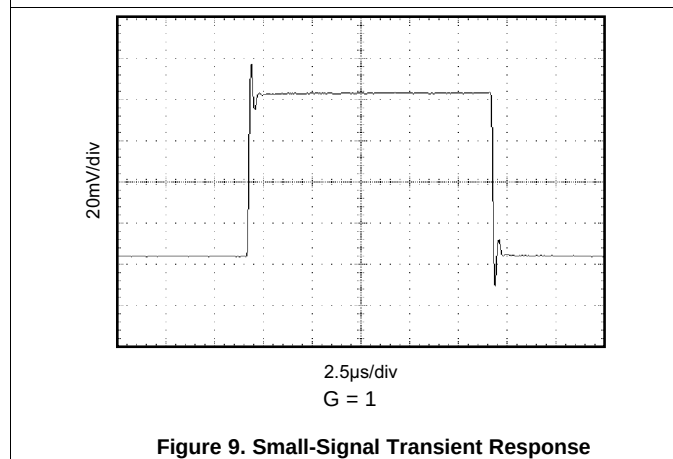


Figure 9. Small-Signal Transient Response

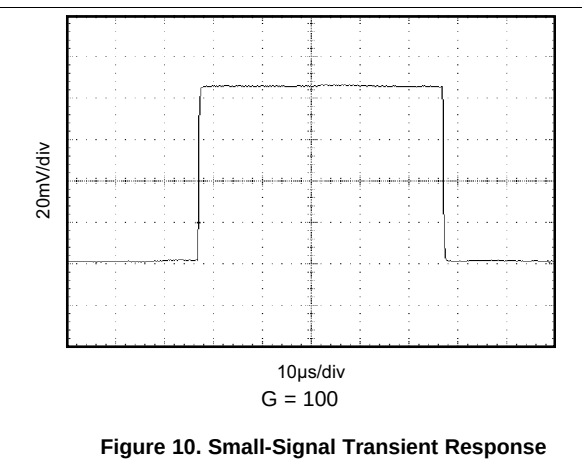


Figure 10. Small-Signal Transient Response

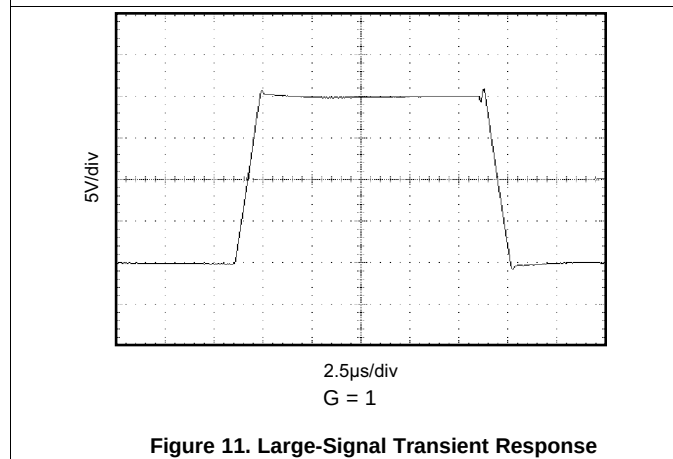


Figure 11. Large-Signal Transient Response

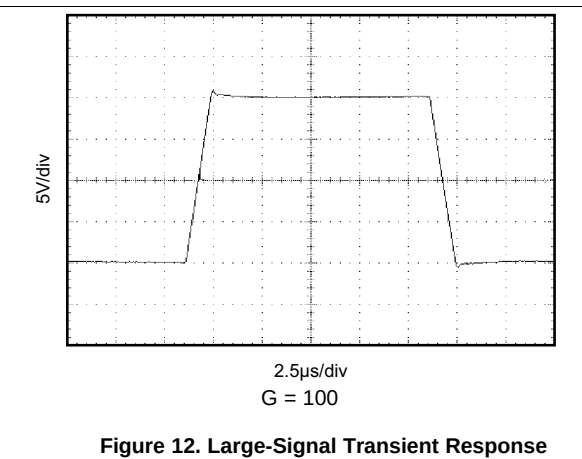


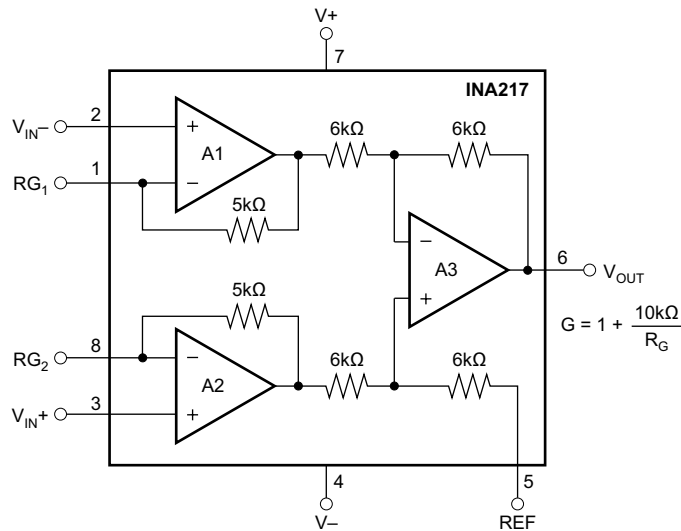
Figure 12. Large-Signal Transient Response

7 Detailed Description

7.1 Overview

The INA217 is a classical three-amp instrumentation amplifier designed for audio applications. Featuring low noise and low distortion the INA217 is ideally suited for amplifying low level audio signals. With a wide supply voltage, wide output voltage swing, and high output current drive the INA217 is also ideally suited for processing high level audio signals. Specified from -40°C to 85°C the INA217 is well suited for industrial applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Basic Connections

Figure 13 shows the basic connections required for operation. Power supplies should be bypassed with 0.1-μF tantalum capacitors near the device pins. The output Reference (pin 5) should be a low-impedance connection. Resistance of a few Ωs in series with this connection will degrade the common-mode rejection of the INA217.

Feature Description (continued)

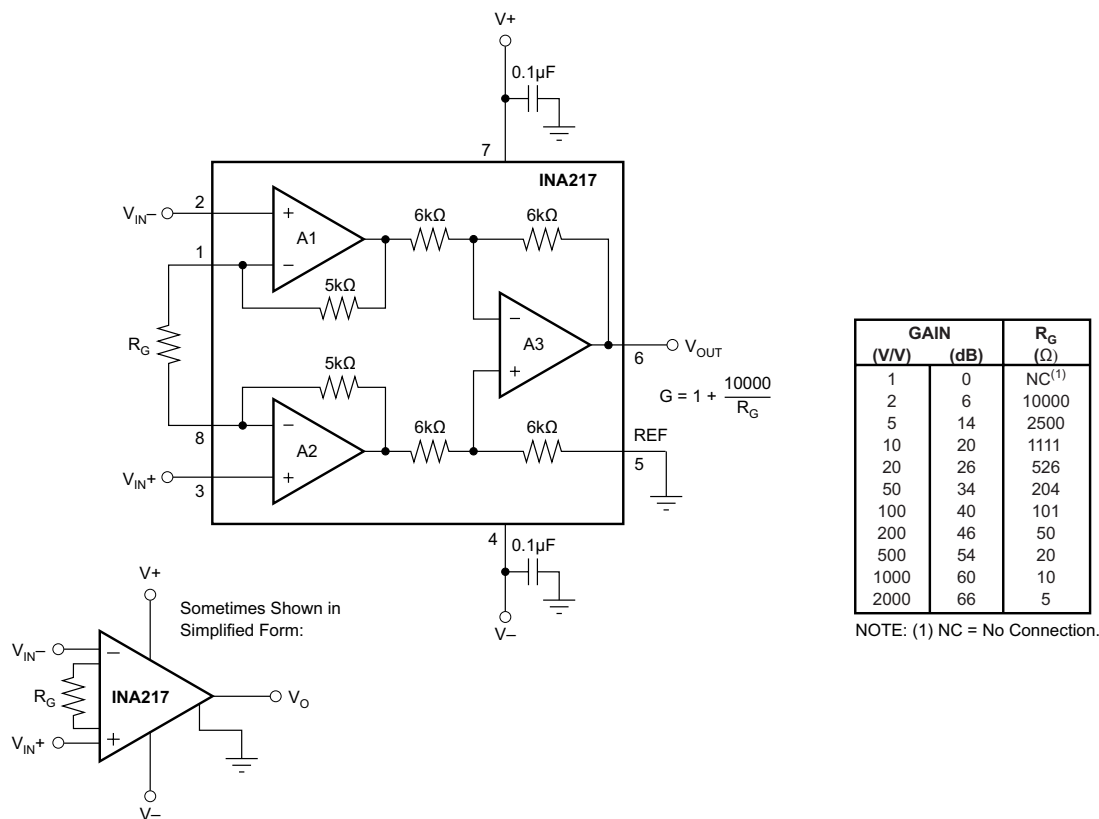


Figure 13. Basic Circuit Connections

7.3.2 Gain-Set Resistor

Gain is set with an external resistor, R_G , as shown in Figure 13. The two internal 5-kΩ feedback resistors are laser-trimmed to 5-kΩ within approximately $\pm 0.2\%$. Equation 1 shows the gain equation for the INA217.

$$G = 1 + \frac{10\,000}{R_G} \quad (1)$$

The temperature coefficient of the internal 5-kΩ resistors is approximately ± 25 ppm/°C. Accuracy and TCR of the external R_G will also contribute to gain error and temperature drift. These effects can be inferred from the gain equation. Make a short, direct connection to the gain set resistor, R_G . Avoid running output signals near these sensitive input nodes.

7.3.3 Noise Performance

The INA217 provides very low noise with low-source impedance. Its 1.3-nV/M $\sqrt{\text{Hz}}$ voltage noise delivers near-theoretical noise performance with a source impedance of 200 Ω. The input stage design used to achieve this low noise results in relatively high input bias current and input bias current noise. As a result, the INA217 may not provide the best noise performance with a source impedance greater than 10 kΩ. For source impedance greater than 10 kΩ, other instrumentation amplifiers may provide improved noise performance.

7.3.4 Input Considerations

Very low source impedance (less than 10 Ω) can cause the INA217 to oscillate. This depends on circuit layout, signal source, and input cable characteristics. An input network consisting of a small inductor and resistor, as shown in Figure 14, can greatly reduce any tendency to oscillate. This is especially useful if a variety of input sources are to be connected to the INA217. Although not shown in other figures, this network can be used as needed with all applications shown.

Feature Description (continued)

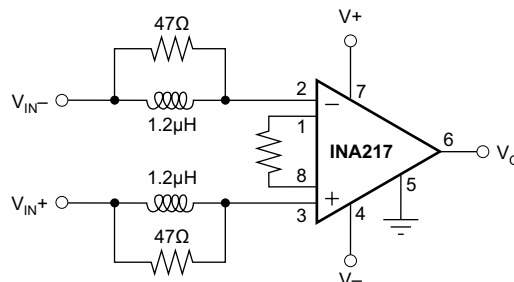


Figure 14. Input Stabilization Network

7.3.5 Offset Voltage Trim

A variable voltage applied to pin 5, as shown in [Figure 15](#), can be used to adjust the output offset voltage. A voltage applied to pin 5 is summed with the output signal. An operational amplifier connected as a buffer is used to provide a low impedance at pin 5 to assure good common-mode rejection.

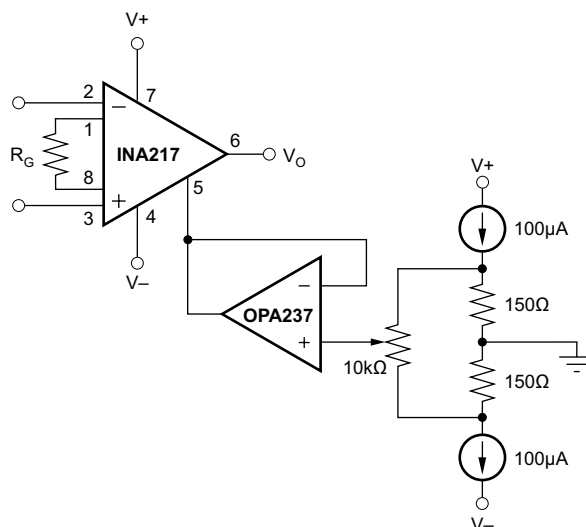


Figure 15. Offset Voltage Adjustment Circuit

7.4 Device Functional Modes

The INA217 has a single functional mode of operation. The mode is operational when the power supply voltage exceeds ± 4.5 V. The maximum power supply voltage is ± 18 V. The INA217 is specified over the temperature range from -40°C to 85°C and is operational to 125°C .

Typical Application (continued)

R_4 and R_5 provide a path for input bias current of the INA217. Input offset current (typically 100 nA) creates a DC differential input voltage that will produce an output offset voltage. This is generally the dominant source of output offset voltage in this application. With a maximum gain of 1000 (60 dB), the output offset voltage can be several volts. This may be entirely acceptable if the output is AC-coupled into the subsequent stage. An alternate technique is shown in [Figure 16](#). An inexpensive FET-input operational amplifier in a feedback loop drives the DC output voltage to 0 V. A2 is not in the audio signal path and does not affect signal quality.

Gain is set with a variable resistor, R_7 , in series with R_6 . R_6 determines the maximum gain. The total resistance, $R_6 + R_7$, determines the lowest gain. A special reverse-log taper potentiometer for R_7 can be used to create a linear change (in dB) with rotation.

8.2.3 Application Curve

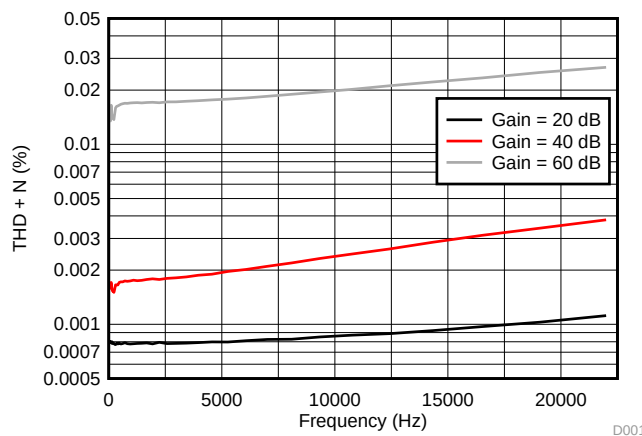


Figure 17. THD + Noise for the Phantom Powered Microphone Circuit

9 Power Supply Recommendations

The INA217 is specified for operation from ± 4.5 V to ± 18 V; many specifications apply from -40°C to 85°C . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*, [SLOA089](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- TI recommends cleaning the PCB following board assembly for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

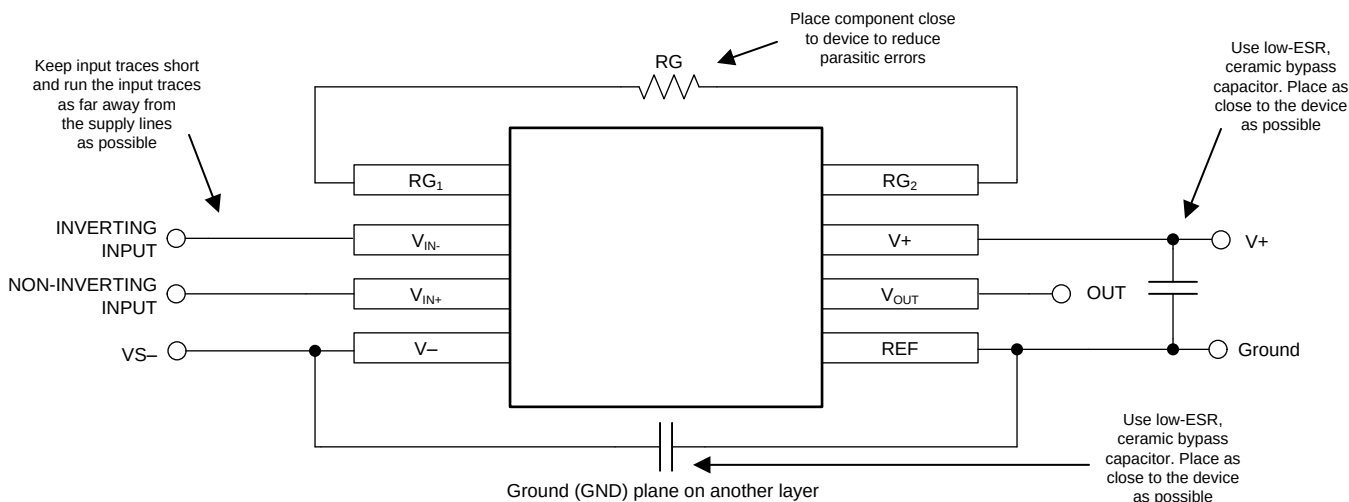


Figure 18. INA217 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

11.1.1.2 TI Precision Designs

TI Precision Designs are available online at <http://www.ti.com/ww/en/analog/precision-designs/>. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.1.1.3 WEBENCH® Filter Designer

[WEBENCH® Filter Designer](#) is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH® Design Center, [WEBENCH® Filter Designer](#) allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Circuit Board Layout Techniques*, [SLOA089](#).
- *Shelf-Life Evaluation of Lead-Free Component Finishes*, [SZZA046](#).

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA217AIDWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA217
INA217AIDWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA217
INA217AIDWT	Active	Production	SOIC (DW) 16	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA217
INA217AIDWT.A	Active	Production	SOIC (DW) 16	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA217

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

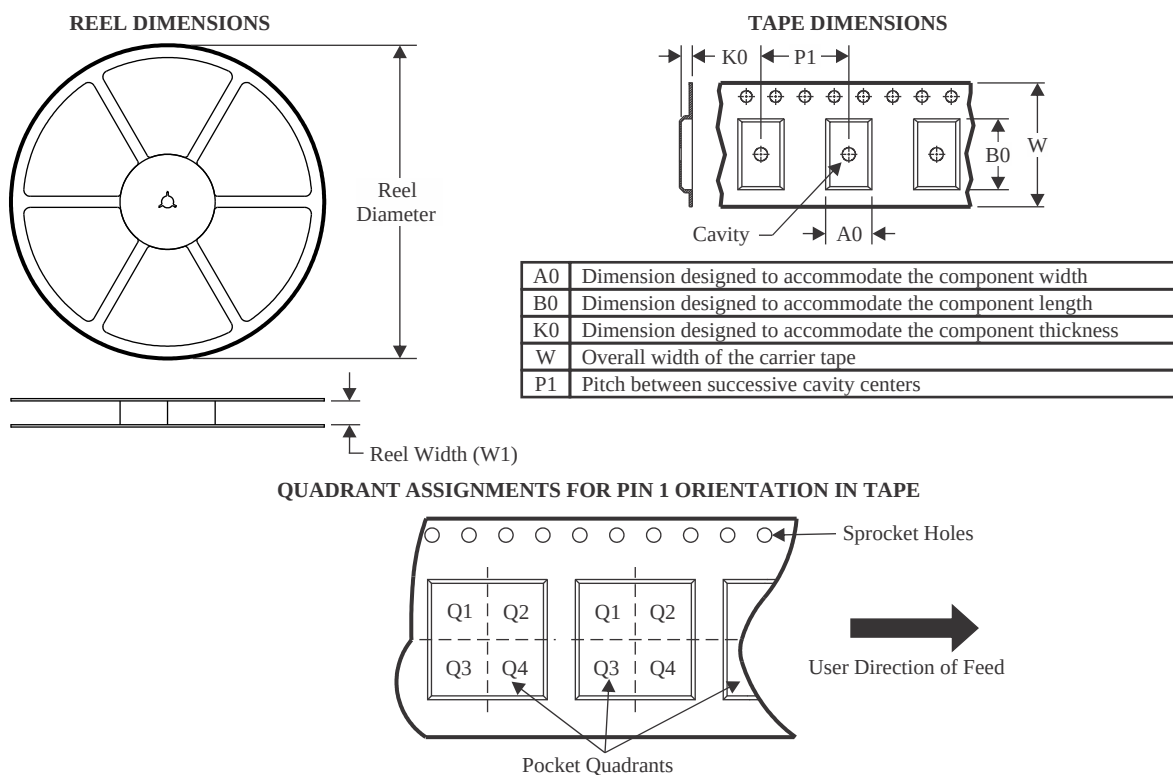
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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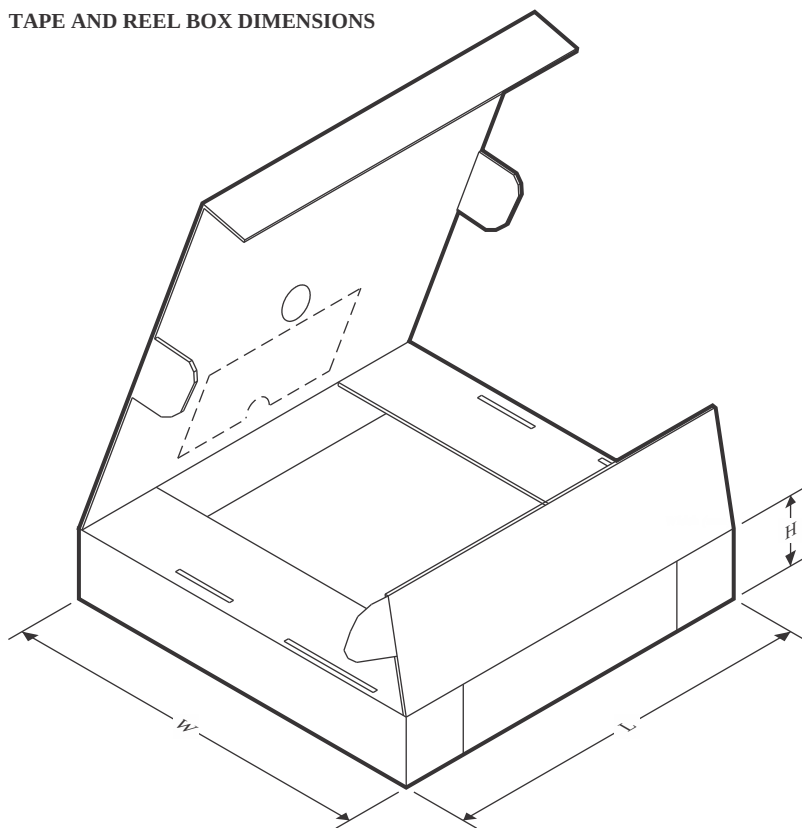
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA217AIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
INA217AIDWT	SOIC	DW	16	250	180.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA217AIDWR	SOIC	DW	16	2000	356.0	356.0	35.0
INA217AIDWT	SOIC	DW	16	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

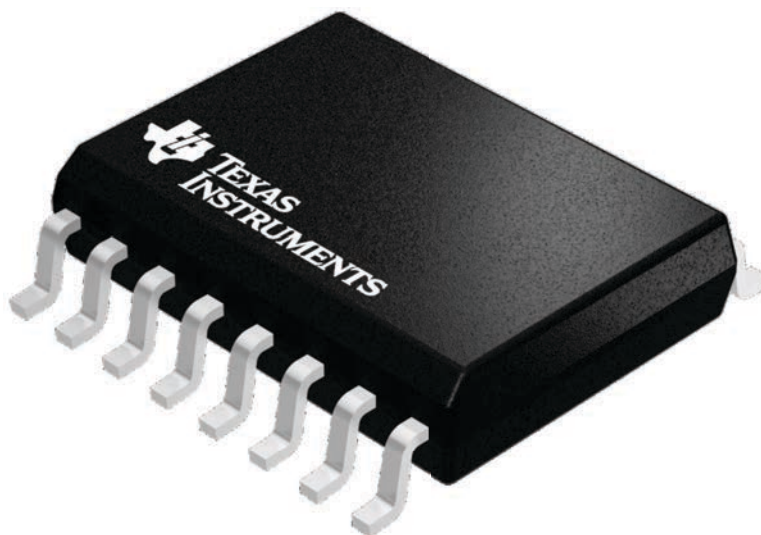
DW 16

SOIC - 2.65 mm max height

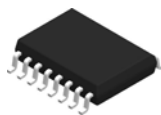
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

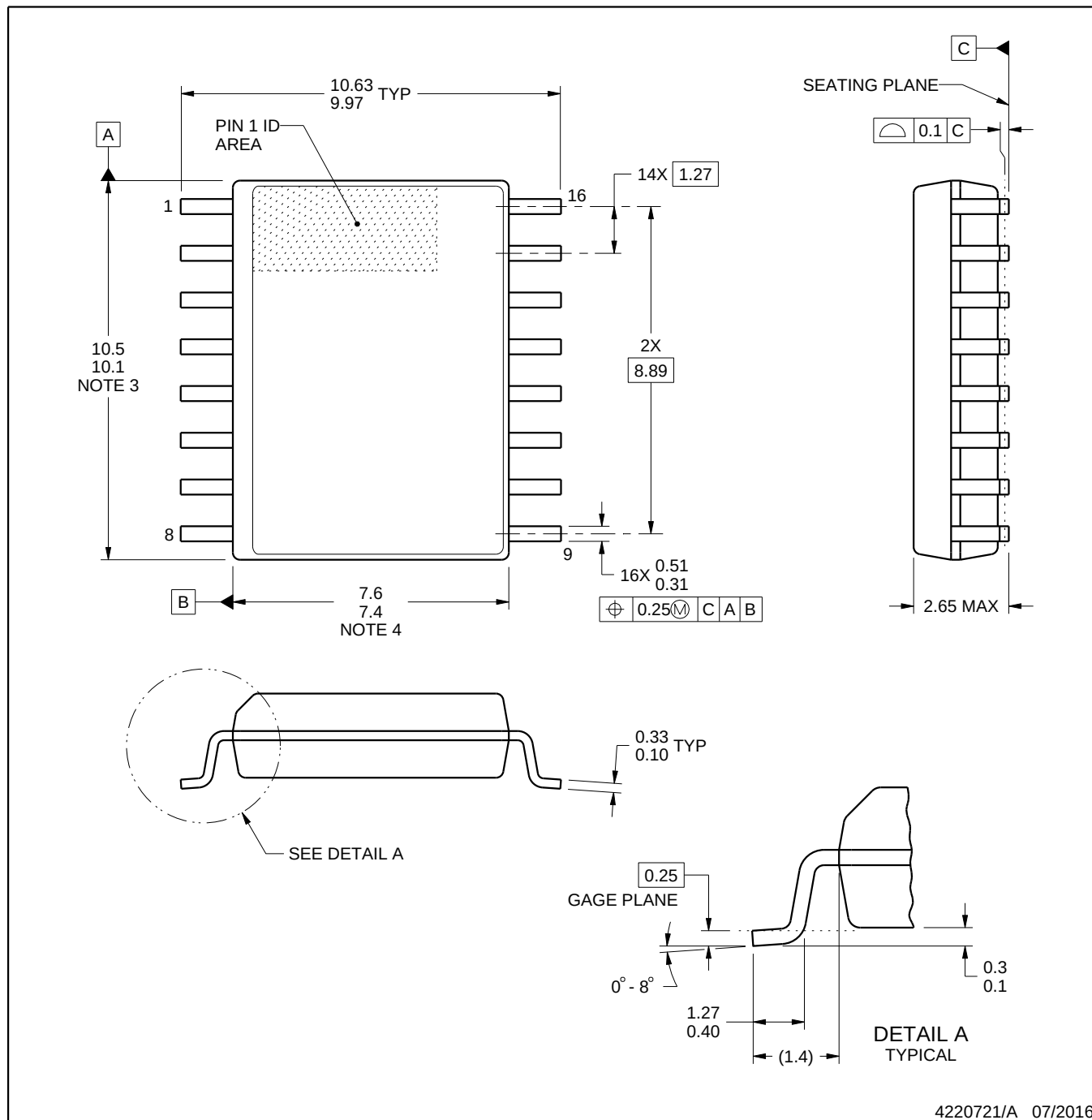


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

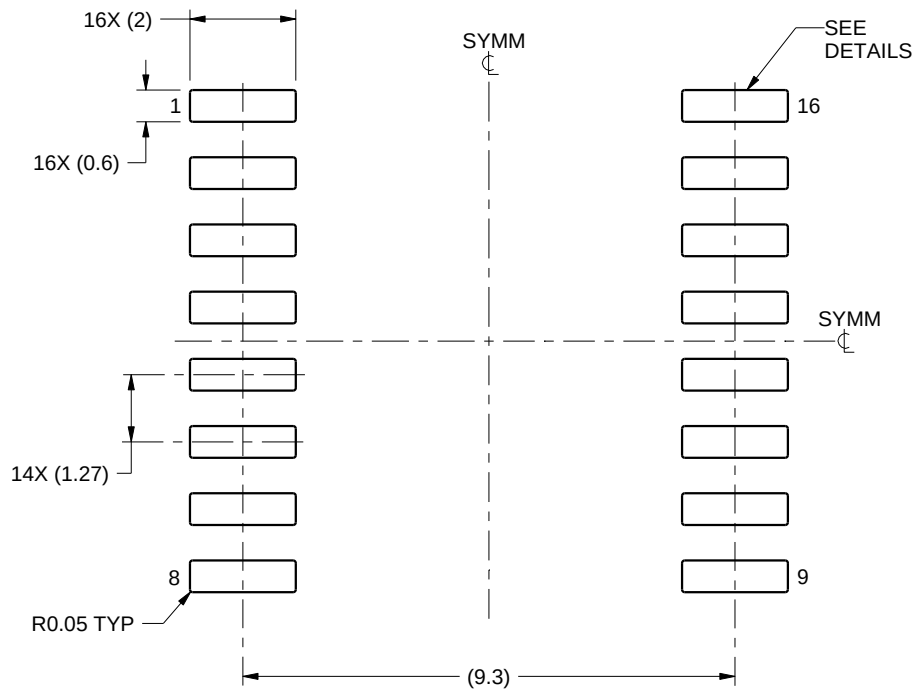
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

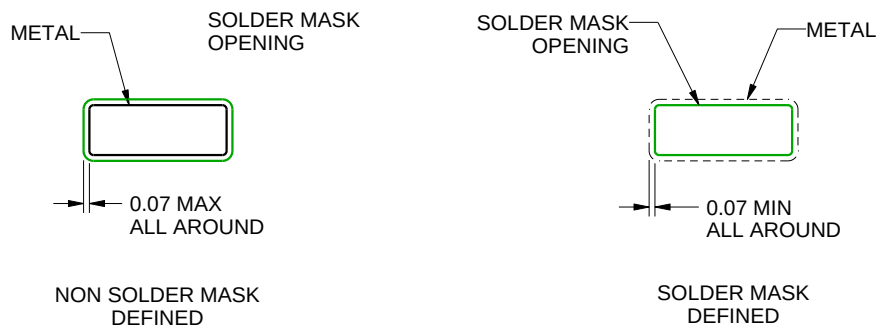
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

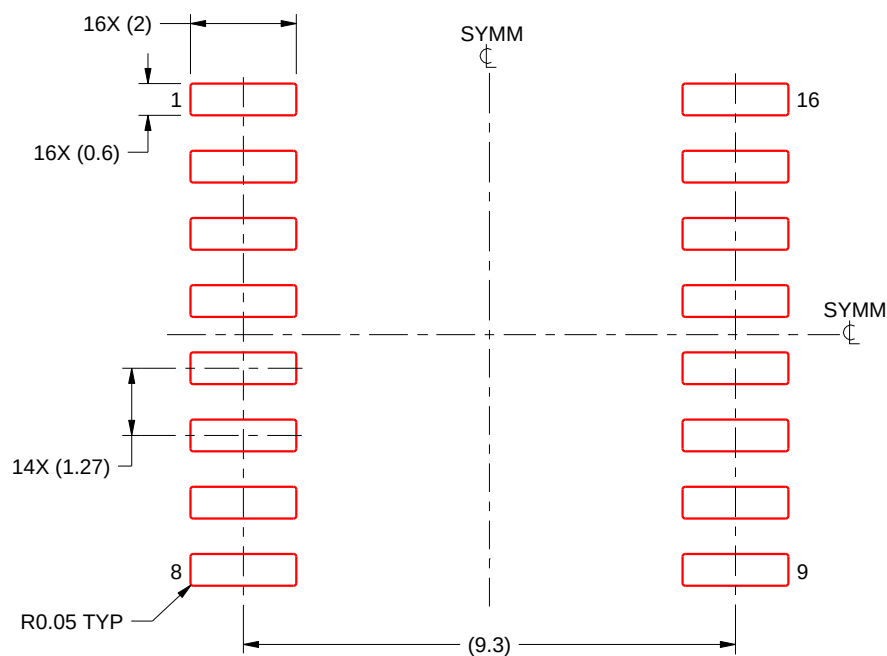
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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