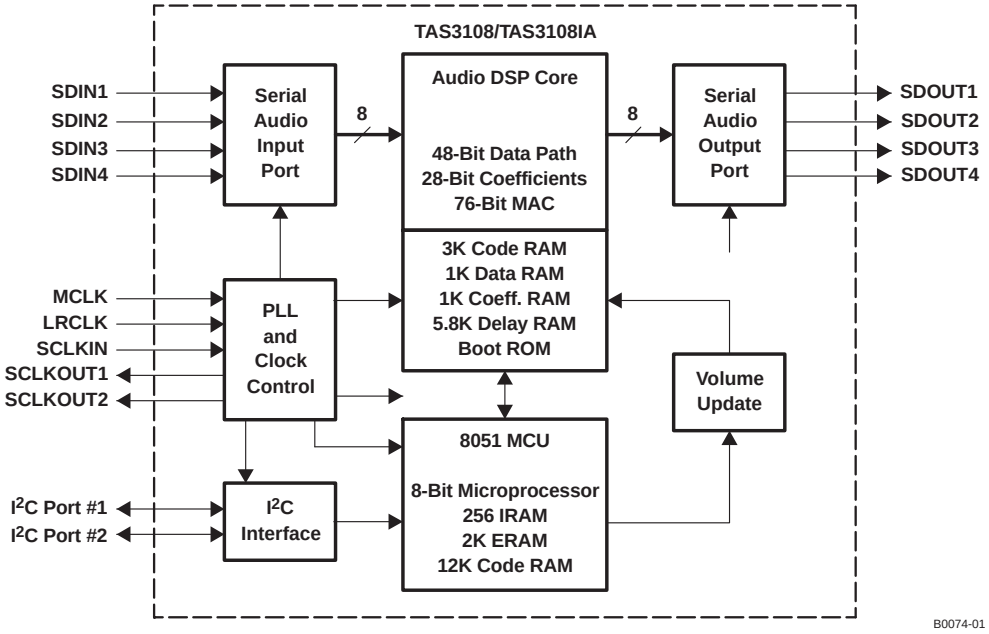
1 Introduction

1.1 Features

- 8 channel Programmable Audio Digital Signal Processor (DSP)
- 135-MHz Maximum Speed, >2800 Processing Cycles Per Sample at 48 kHz
- Sample Rates of 32 kHz to 192 kHz
- 48-Bit Data Path and 28-Bit Coefficients
- Single-Cycle, 76-Bit Multiply Accumulate
- Five Simultaneous Operations Per Clock Cycle
- 1022 Words of 48-Bit Data Memory
- 1022 Words of 28-Bit Coefficient Memory
- 3K Words of 54-Bit Program RAM
- 5.88K Words of 24-Bit Delay Memory (122.5 ms at 48 kHz)
- 15 Stereo/TDM Data Formats
- Independent Input/Output Data Formats
- 16-, 20-, 24-, and 32-Bit Word Sizes
- 64-f_S, 128-f_S, 192-f_S, and 256-f_S SCLK to Support Discrete 4 channel TDM, 6 channel TDM, and 8 channel TDM Data-Transfer Formats
- Two I^2C Ports for Slave or Master Download
- Soft Volume Controller
- Dither Generator
- Efficient $\log^2/2^x$ Estimator
- Single 3.3-V Power Supply
- 38-Pin Thin Shrink Small-Outline Package (TSSOP) (DCP)
- AEC-Q100 (Grade 2: –40°C to 105°C) Compliant for Automotive Applications (TAS3108IA)

1.2 Applications

- Automotive Sound Systems
- Digital Televisions
- Home Theater Systems
- Mini-Component Audio



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2 Functional Description

2.1 Device Description

The TAS3108 and TAS3108IA are fully programmable high-performance audio processors. The devices use an efficient, custom, multi-instruction programming environment optimized for digital audio processing algorithms. The TAS3108/TAS3108IA architecture provides high-quality audio processing by using a 48-bit data path, 28-bit filter coefficients, and a single-cycle 28 × 48-bit multiplier with a 76-bit accumulator. An embedded 8051 microprocessor provides algorithm and data control for the TAS3108/TAS3108IA. The TAS3108 is the commercial version intended for home audio and other commercial applications. The TAS3108IA is the automotive version that is qualified for use in automotive applications.

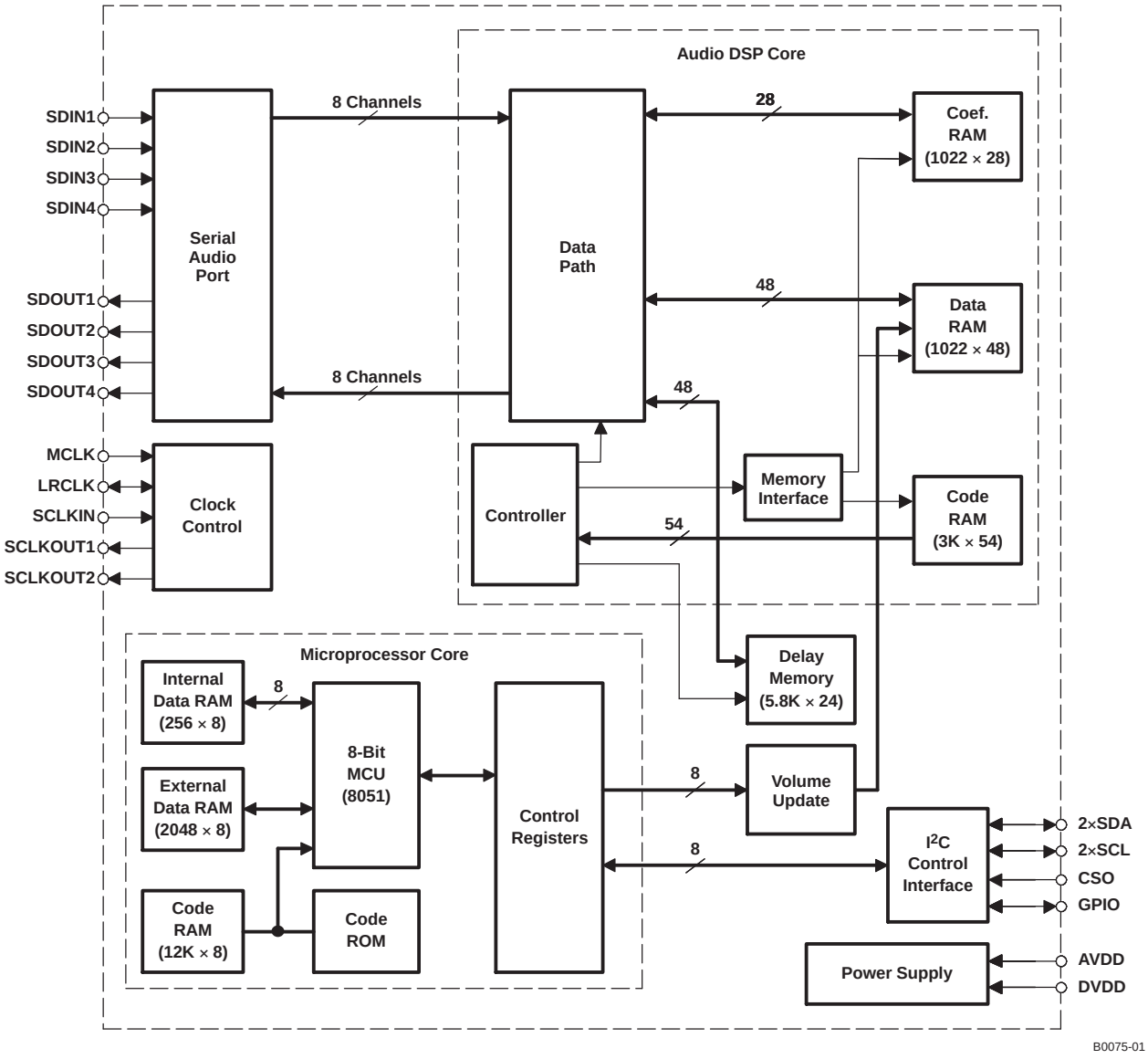


Figure 2-1. Expanded TAS3108/TAS3108IA Functional Block Diagram

2.2 Power Supply

The power supply contains supply regulators that provide analog and digital regulated power for various sections of the TAS3108/TAS3108IA. Only one external 3.3-V supply is required. All other voltages are generated on-chip from the external 3.3-V supply.

2.3 Clock Control

The TAS3108/TAS3108IA can be an audio data clock-master or clock-slave device. In clock-master mode, it generates MCLK, SCLK, and LRCLK. In clock-slave mode, it accepts MCLK, SCLK, and LRCLK. It can generate or accept master clocks from 6 MHz to 24.576 MHz. Master or slave operation is set via I^2C register 0x00. The TAS3108/TAS3108IA can use a 6-MHz to 20-MHz crystal or a 6-MHz to 24.576-MHz, 3.3-V MCLKI digital input as the master clock in either clock-master or clock-slave mode. In clock-slave mode, the master clock frequency does not need to be an integer multiple of the sample rate.

The TAS3108/TAS3108IA does not support clock error detection. If a clock error occurs, the TAS3108/TAS3108IA does not prevent invalid data or clocks from being output. This means that the application system must be designed to handle clock errors.

2.4 Serial Audio Ports (SAPs)

Serial audio data is input via pins SDIN1, SDIN2, SDIN3, and SDIN4. Serial audio data is output on pins SDOUT1, SDOUT2, SDOUT3, and SDOUT4. The TAS3108/TAS3108IA accepts 32-, 44.1-, 48-, 88.2-, 96-, 176.4-, or 192-kHz serial data as 16-, 20-, 24-, or 32-bit data in left justified, right justified, or I^2S serial data formats. All four ports accommodate these three 2 channel data formats.

In addition to supporting the 2 channel formats, SDIN1 and SDOUT1 also provide support for time-division multiplex (TDM) data formats of 4, 6, or 8 channels. The data formats are selectable via I^2C register 0x00. All input channels must use the same data format. All output channels must use the same data format. However, the input and output formats can be different.

2.5 M8051Warp Microprocessor

The M8051Warp (8051) microprocessor controls I^2C reads and writes and participates in some audio processing tasks requiring multiframe (f_S period) processing cycles. The 8051 processor performs some control calculations and exchanges data between the audio DSP core and the I^2C interface. It also provides mode control for the SAP interface and clock control. The microcode can program the GPIO pin for post-boot-up operation to be an input or an output. For more information, see the *TAS3108/TAS3108IA Firmware Programmer's Guide* (SLEU067).

2.6 I^2C Control Interface

The TAS3108/TAS3108IA has an I^2C slave-only interface (SDA1 and SCL1) for receiving commands and providing status to the system controller, and a separate master I^2C interface (SDA2 and SCL2) to download programs and data from external memory such as an EEPROM. See Section 6 for more information.

2.7 Audio DSP Core

The audio DSP core arithmetic unit is a fixed-point computational engine consisting of an arithmetic unit and data and coefficient memory blocks. The primary features of the audio DSP core are:

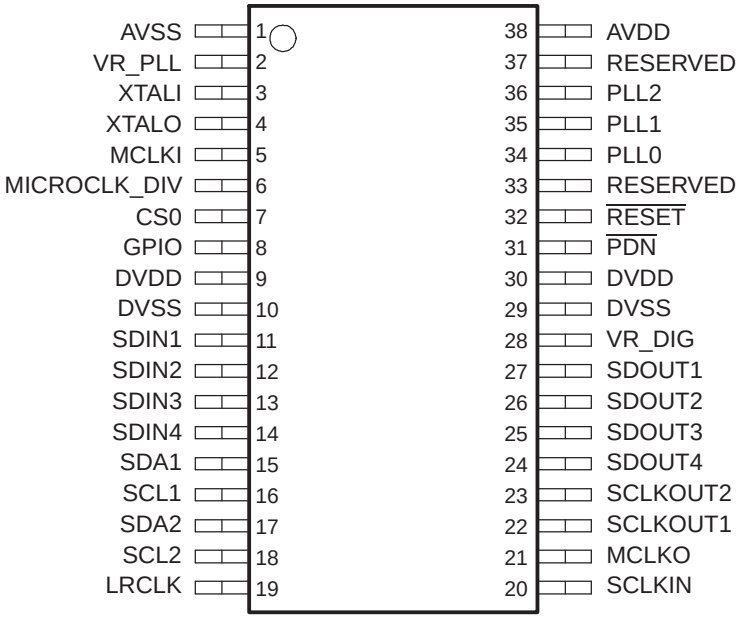
- 48-bit data path with 76-bit accumulator
- Hardware multiplier (28 bit × 48bit)
- Read/write single-cycle memory access
- Input is 48-bit 2s-complement data multiplexed in from the SAP immediately following an LRCLK pulse.
- Output is 32-bit 2s-complement data on four buses.
- Separate control for writing to delay memory
- Separate coefficient memory (28 bit) and data memory (48 bit)
- Linear feedback shift register (LFSR) is a random-number generator that can be used to dither the audio.
- Coefficient RAM, data RAM, LFSR seed, program counter, and memory pointers are all mapped into the same 5.88K memory space for convenient addressing by the microprocessor.
- Memory interface block contains four pointers – two for data memory and two for coefficient memory.

The audio DSP core is used to implement all audio processing functions.

3 Physical Characteristics

3.1 Terminal Assignments

DCP PACKAGE
(TOP VIEW)



3.2 Terminal Descriptions

TERMINAL		INPUT/ OUTPUT(1)	PULLUP/ PULLDOWN(2)	DESCRIPTION
NAME	NO.			
AVDD	38	I		Analog power supply (3.3 V)
AVSS	1			Analog ground
CS0	7	I	Pulldown	Chip select
DVDD	9, 30	I		Digital power supply input (3.3 V)
DVSS	10, 29			Digital ground
GPIO	8	I/O	Pullup	GPIO control (user programmable)
LRCLK	19	I/O	Pulldown	Sample rate clock (f_S)
MCLKIN	5	I		Master clock input (connect to ground when not in use)
MCLKO	21	O		Master clock output
MICROCLK_DIV	6	I	Pulldown	Internal microprocessor clock divide control
$\overline{PDN}$	31	I	Pullup	Power down. Powers down all logic and stops all clocks, active low. Coefficient memory remains stable through the power-down cycle.
PLL0	34	I	Pullup	PLL control 0
PLL1	35	I	Pulldown	PLL control 1
PLL2	36	I	Pullup	PLL control 2
RESERVED	33, 37			Reserved. Connect to ground
$\overline{RESET}$	32	I	Pullup	Reset, active low
SCL1	16	I/O		I^2C port 1 clock (always a slave)
SCL2	18	I/O		I^2C port 2 clock (always a master)
SCLKIN	20	I	Pulldown	Bit clock input
SCLKOUT1	22	O		Bit clock 1 out. Used to receive input serial data.
SCLKOUT2	23	O		Bit clock 2 out. Used to clock output serial data.
SDA1	15	I/O		I^2C port 1 data (always a slave)
SDA2	17	I/O		I^2C port 2 data (always a master)
SDIN1	11	I	Pulldown	Serial data input 1
SDIN2	12	I	Pulldown	Serial data input 2
SDIN3	13	I	Pulldown	Serial data input 3
SDIN4	14	I	Pulldown	Serial data input 4
SDOUT1	27	O		Serial data output 1
SDOUT2	26	O		Serial data output 2
SDOUT3	25	O		Serial data output 3
SDOUT4	24	O		Serial data output 4
VR_PLL	2			Internal regulator. This pin must not be used to power external devices.
XTALI	3	O		Oscillator input (connect to ground when not in use)
XTALO	4	O		Oscillator output
VR_DIG	28			Internal regulator. This pin must not be used to power external devices.

(1) I = input, O = output
(2) All pullups are 20-µA weak pullups, and all pulldowns are 20-µA weak pulldowns. The pullups and pulldowns are included to ensure proper input logic levels if the terminals are left unconnected (pullups → logic 1 input; pulldowns → logic 0 input). Devices that drive inputs with pullups must be able to sink 20 µA while maintaining a logic-0 drive level. Devices that drive inputs with pulldowns must be able to source 20 µA while maintaining a logic-1 drive level.

3.3 Reset ($\overline{RESET}$)

The $\overline{RESET}$ pin is an asynchronous control signal that restores all TAS3108/TAS3108IA components to the default configuration. When a reset occurs, the audio DSP core is put into an idle state and the 8051 starts initialization. A valid MCLKI or XTLI must be present when clearing the $\overline{RESET}$ pin to initiate a device reset. A reset can be initiated by applying a logic 0 on $\overline{RESET}$. A reset can also be issued at power turnon by the three internal power supplies.

As long as $\overline{\text{RESET}}$ is held LOW, the device is in the reset state. During reset, all I^2C and serial data bus operations are ignored. The I^2C interface SCL and SDA lines go into a high-impedance state and remain in that state until device initialization has completed.

The rising edge of the reset pulse begins the initialization housekeeping functions of clearing memory and setting the default register values. Once these are complete, the TAS3108/TAS3108IA enables its master I^2C interface and disables its slave I^2C interface.

Then the TAS3108/TAS3108IA looks for an EEPROM as described in Section 2.6, *I^2C Control Interface*.

3.4 Power-On Reset ($\overline{\text{RESET}}$)

On power up, it is recommended that the TAS3108/TAS3108IA $\overline{\text{RESET}}$ be held LOW until DVDD has reached 3.3 V. This can be done by programming the system controller or by using an external RC delay circuit. The 1-kΩ and 1-µF values provide a delay of approximately 200 µs. The values of R and C can be adjusted to provide other delay values as necessary.

3.5 Power Down ($\overline{\text{PDN}}$)

$\overline{\text{PDN}}$ is a user-firmware-definable pin that is programmed in the default TAS3108 and TAS3108IA configuration to stop all clocks in the TAS3108/TAS3108IA, while preserving the state of the device. For more information, see *TAS3108/TAS3108IA Firmware Programmer's Guide* (SLEU067).

3.6 I^2C Bus Control (CS0)

The TAS3108/TAS3108IA has a control to specify the slave and master I^2C address. This control permits up to two TAS3108/TAS3108IA devices to be placed in a system without external logic.

See Section 6.2 for a complete description of this pin.

3.7 Programmable General Purpose I/O (GPIO)

The TAS3108/TAS3108IA has one GPIO pin that is 8051 firmware programmable.

On power up or following a reset, the GPIO pin becomes an input. Afterwards, the microprocessor can program the GPIO as an input or an output.

For more information, see *TAS3108/TAS3108IA Firmware Programmer's Guide* (SLEU067).

3.7.1 No EEPROM is Present or a Memory Error Occurs

Following reset or power-up initialization with the EEPROM not present or if a memory error occurs, the TAS3108/TAS3108IA is in one of two modes, depending on the setting of the GPIO pin.

- GPIO pin is logic HIGH (through a 20-kΩ resistor)

  With the GPIO pin held HIGH during initialization, the TAS3108/TAS3108IA comes up in the default configuration with the serial data outputs not active. Once the TAS3108/TAS3108IA has completed the default initialization procedure and after the status register is updated and the I^2C slave interface is enabled, the GPIO pin is an output and is driven LOW. Following the HIGH-to-LOW transition of the GPIO pin, the system controller can access the TAS3108/TAS3108IA through the I^2C interface and read the status register to determine the load status.

  If a memory-read error occurs, the TAS3108/TAS3108IA reports the error in the status register (I^2C subaddress 0x02).

- GPIO pin is logic LOW (through a 20-kΩ resistor)

  With GPIO pin held LOW during initialization, the TAS3108/TAS3108IA comes up in an I/O test configuration. In this case, once the TAS3108/TAS3108IA completes its default test initialization procedure, the status register is updated, the I^2C slave interface is enabled, and the TAS3108/TAS3108IA streams audio unaltered from input to output as SDIN1 to SDOUT1, SDIN2 to SDOUT2, etc.

  In this configuration, the GPIO pin is an output signal that is driven LOW. If the external logic is no

longer driving the GPIO pin low after the load has completed (~100 ms following a reset if no EEPROM is present), the state of the GPIO pin can be observed.

Then the system controller can access the TAS3108/TAS3108IA through the I^2C interface and read the status register to determine the load status.

If the GPIO pin state is not observed, the only indication that the device has completed its initialization procedure is that the TAS3108/TAS3108IA streams audio and the I^2C slave interface has been enabled.

3.7.2 GPIO Pin Function After Device Is Programmed

Once the TAS3108/TAS3108IA has been programmed, either through a successful boot load or via slave I^2C download, the operation of GPIO can be programmed to be an input and/or output.

3.8 Input and Output Serial Audio Ports

The TAS3108/TAS3108IA supports system architectures that require data format conversions between TDM and non-TDM of the same format type without the need for additional glue logic. In addition, the TAS3108/TAS3108IA supports data format conversions between right justified and I^2S and between left justified and I^2S. All the supported conversions are listed in Table 3-1. If the input port is configured for a TDM format, only SDIN1 is active. If a TDM format is selected for the output port, only SDOUT1 is active.

Table 3-1. Supported Conversions

INPUT SAP (SDIN1, SDIN2, SDIN3, SDIN4)	OUTPUT SAP (SDOUT1, SDOUT2, SDOUT3, SDOUT4)
2 channel left justified	TDM left justified
2 channel left justified	2 channel I^2S
TDM left justified	2 channel left justified
2 channel I^2S	TDM I^2S
TDM I^2S	2 channel I^2S
2 channel I^2S	2 channel leftjustified
2 channel I^2S	2 channel right justified
2 channel right justified	2 channel I^2S

Table 3-2. Serial Data Input and Output Formats

MODE	INPUT CONTROL IM[3:0]	OUTPUT CONTROL OM[3:0]	SERIAL FORMAT	WORD LENGTHS	DATA RATES (kHz)	MAX SCLK
2 channel	0000	0000	Left justified	16, 20, 24, 32	32–192	12.288
	0001	0001	Right justified	16, 20, 24, 32		
	0010	0010	I^2S	16, 20, 24		
Time-division multiplexed (4, 6, or 8 channel)	0011	0011	8 channel left justified	16, 20, 24, 32	32–96 MCLK 32–48 crystal	24.576 MCLK 12.288 crystal
	0110	0110	8 channel I^2S	16, 20, 24		
	0100	0100	6 channel left justified	16, 20, 24, 32	32–96	18.432
	0111	0111	6 channel I^2S	16, 20, 24		
	0101	0101	4 channel left justified	16, 20, 24, 32	32–192 MCLK 32–96 crystal	24.576 MCLK 12.288 crystal
	1000	1000	4 channel I^2S	16, 20, 24		

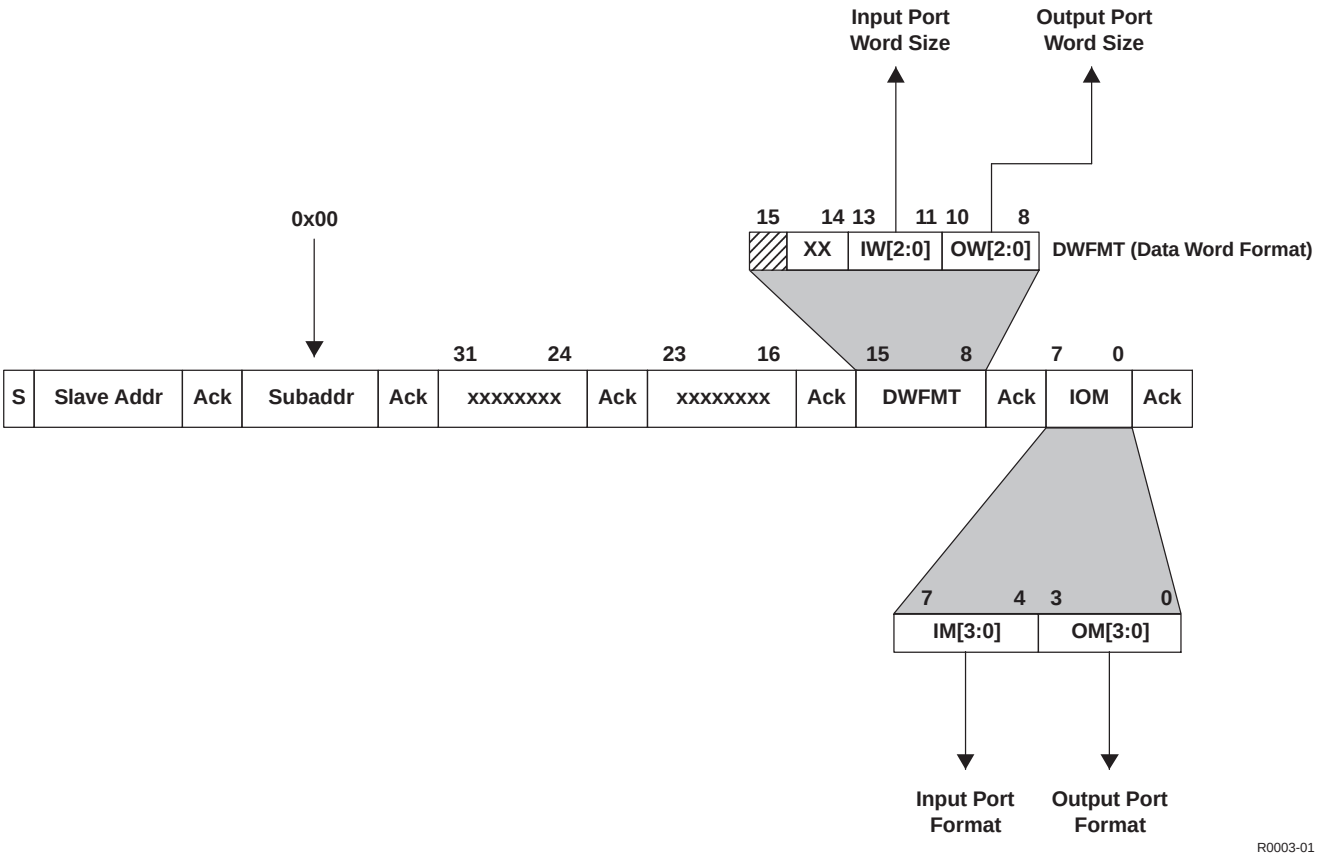


Figure 3-1. Serial Data Controls

Table 3-3. Serial Data Input and Output Data Word Sizes

IW1, OW1	IW0, OW0	FORMAT
0	0	32-bit data
0	1	16-bit data
1	0	20-bit data
1	1	24-bit data

Following a reset, ensure that the clock register (0x00) is written before performing volume, treble, or bass updates.

Commands to reconfigure the SAP can be accompanied by mute and unmute commands for quiet operation. However, care must be taken to ensure that the mute command has completed before the SAP is commanded to reconfigure. Similarly, the TAS3108/TAS3108IA should not be commanded to unmute until after the SAP has completed a reconfiguration. The reason for this is that an SAP configuration change while a volume or bass or treble update is taking place can cause the update not to be completed properly.

When the TAS3108/TAS3108IA is transmitting serial data, it uses the negative edge of SCLK to output a new data bit. The TAS3108/TAS3108IA samples incoming serial data on the rising edge of SCLK. The TAS3108/TAS3108IA only supports TDM, left justified, right justified, and I^2S formats.

3.8.1 2 channel I^2S Timing

In 2 channel I^2S timing, LRCLK is LOW when left channel data is transmitted and HIGH when right channel data is transmitted. SCLK is a bit clock running at $64 \times f_S$, which clocks in each bit of the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of the bit clock. The TAS3108/TAS3108IA masks unused trailing data-bit positions.

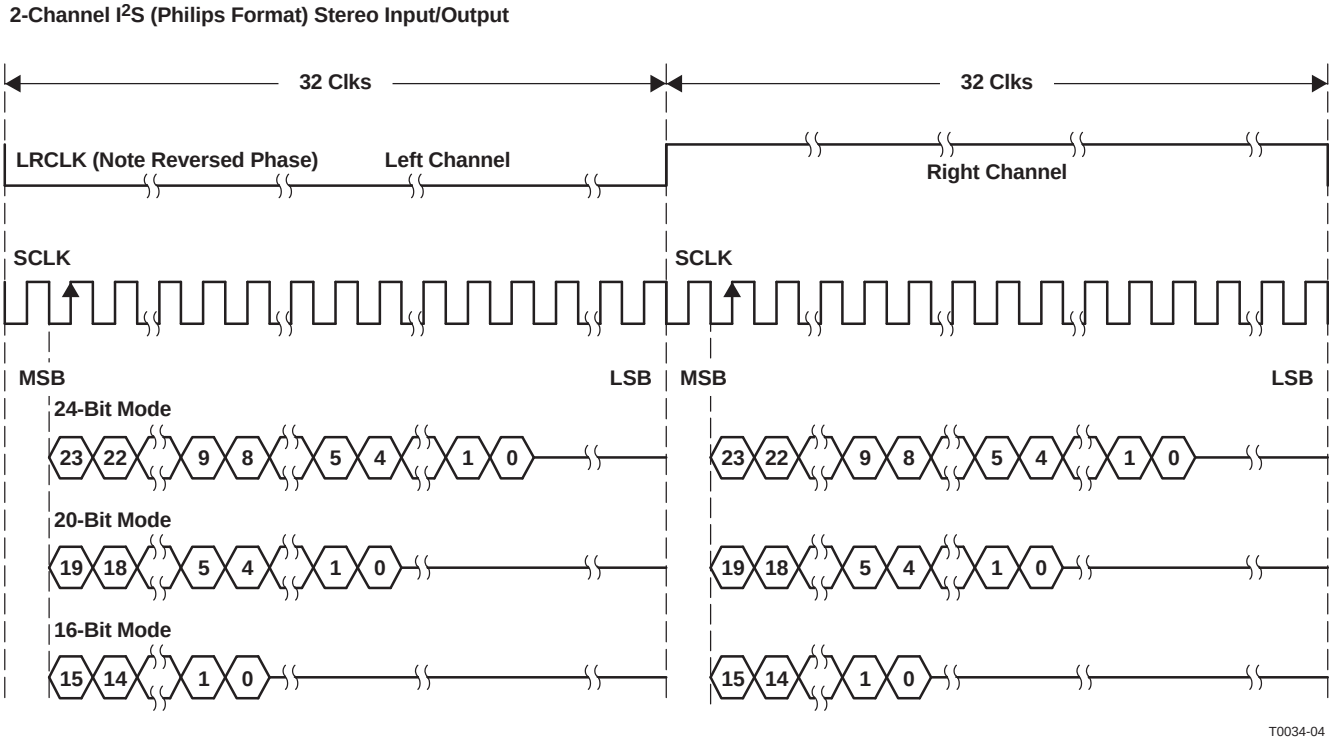


Figure 3-2. I^2S 64-f_S Format

3.8.2 2 Channel Left Justified Timing

In 2 channel left justified timing, LRCLK is HIGH when left channel data is transmitted and LOW when right channel data is transmitted. SCLK is a bit clock running at 64 × f_S which clocks in each bit of the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The TAS3108/TAS3108IA masks unused trailing data-bit positions.

2-Channel Left-Justified Stereo Input

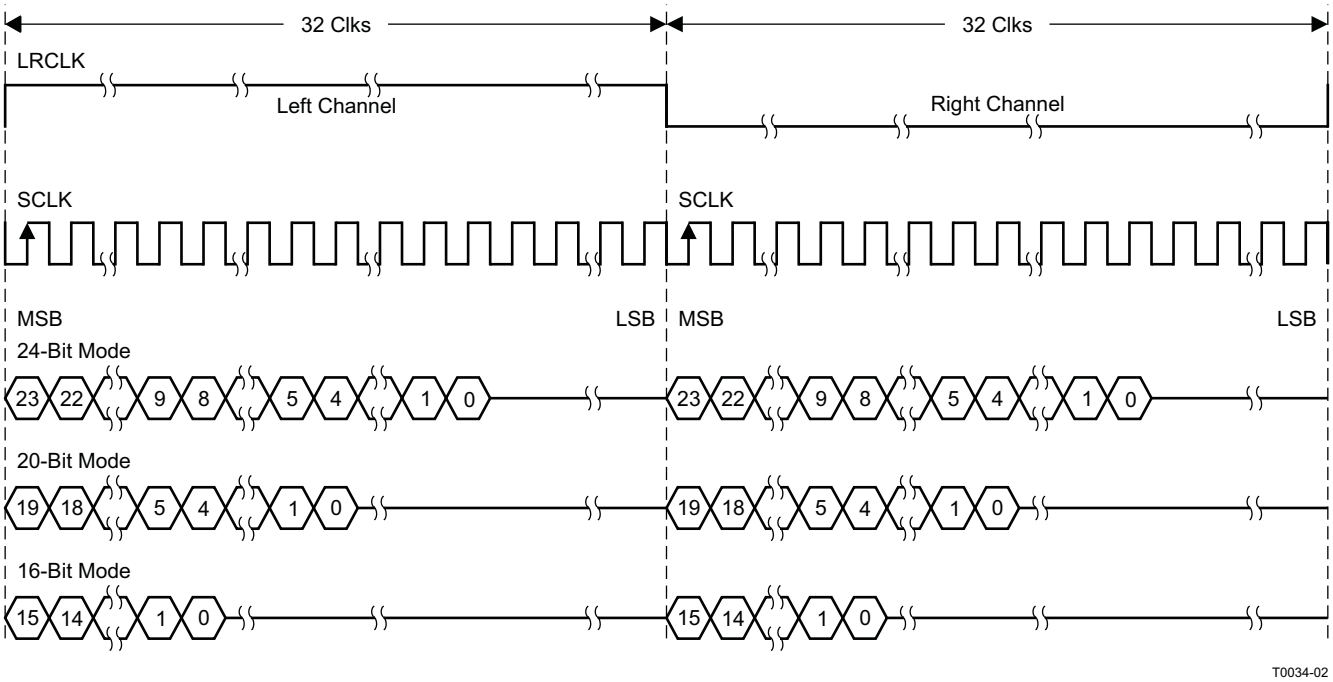


Figure 3-3. Left justified 64-f_S Format

3.8.3 2 Channel Right Justified Timing

In 2-channel right-justified timing, LRCLK is HIGH when left channel data is transmitted and LOW when right channel data is transmitted. SCLK is a bit clock running at 64 × f_S, which clocks in each bit of the data. The first bit of data appears on the data lines 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In the right-justified mode, the last bit clock before LRCLK transitions always clocks the LSB of data. The data is written MSB first and is valid on the rising edge of the bit clock. The TAS3108/TAS3108IA masks unused leading data-bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input

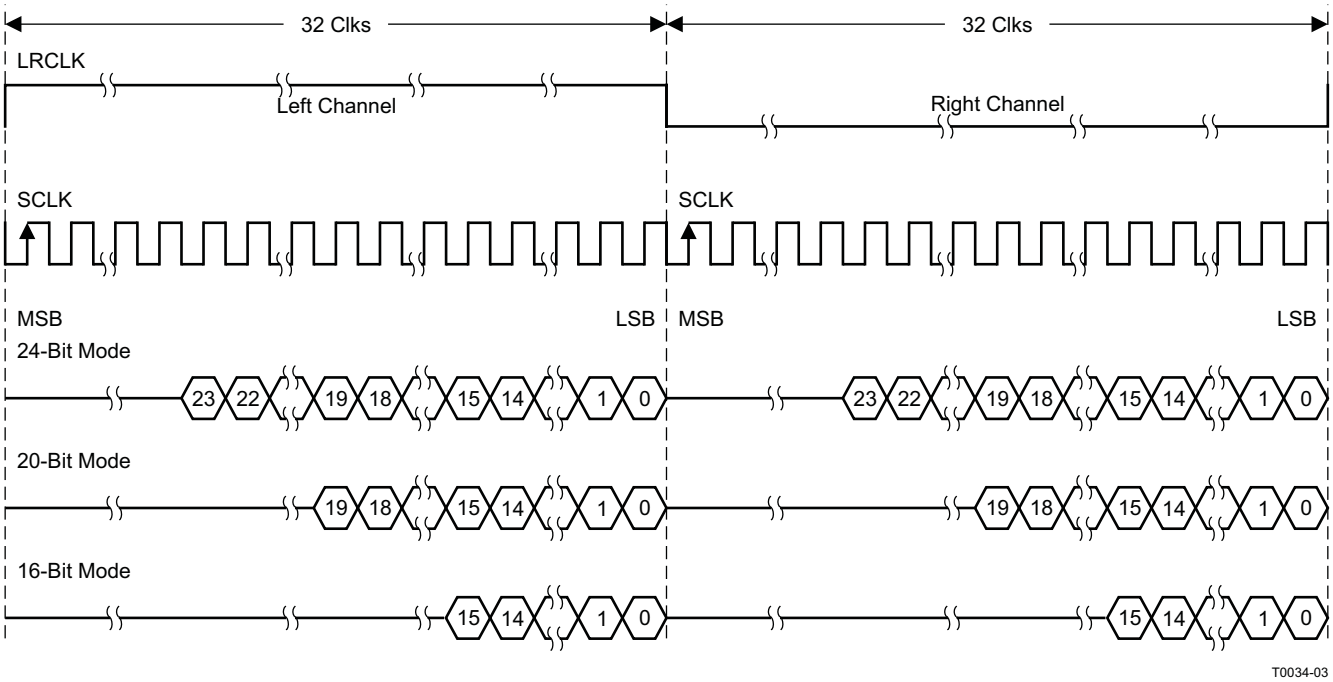


Figure 3-4. Right justified 64-f_S Format

3.8.4 TDM Modes

The TDM modes on the TAS3108/TAS3108IA provide left justified and I^2S formats. Each word in the TDM data stream adheres to the bit placement shown in Figure 3-5 and Figure 3-6. Two cases are illustrated—an I^2S data format and a left-justified data format.

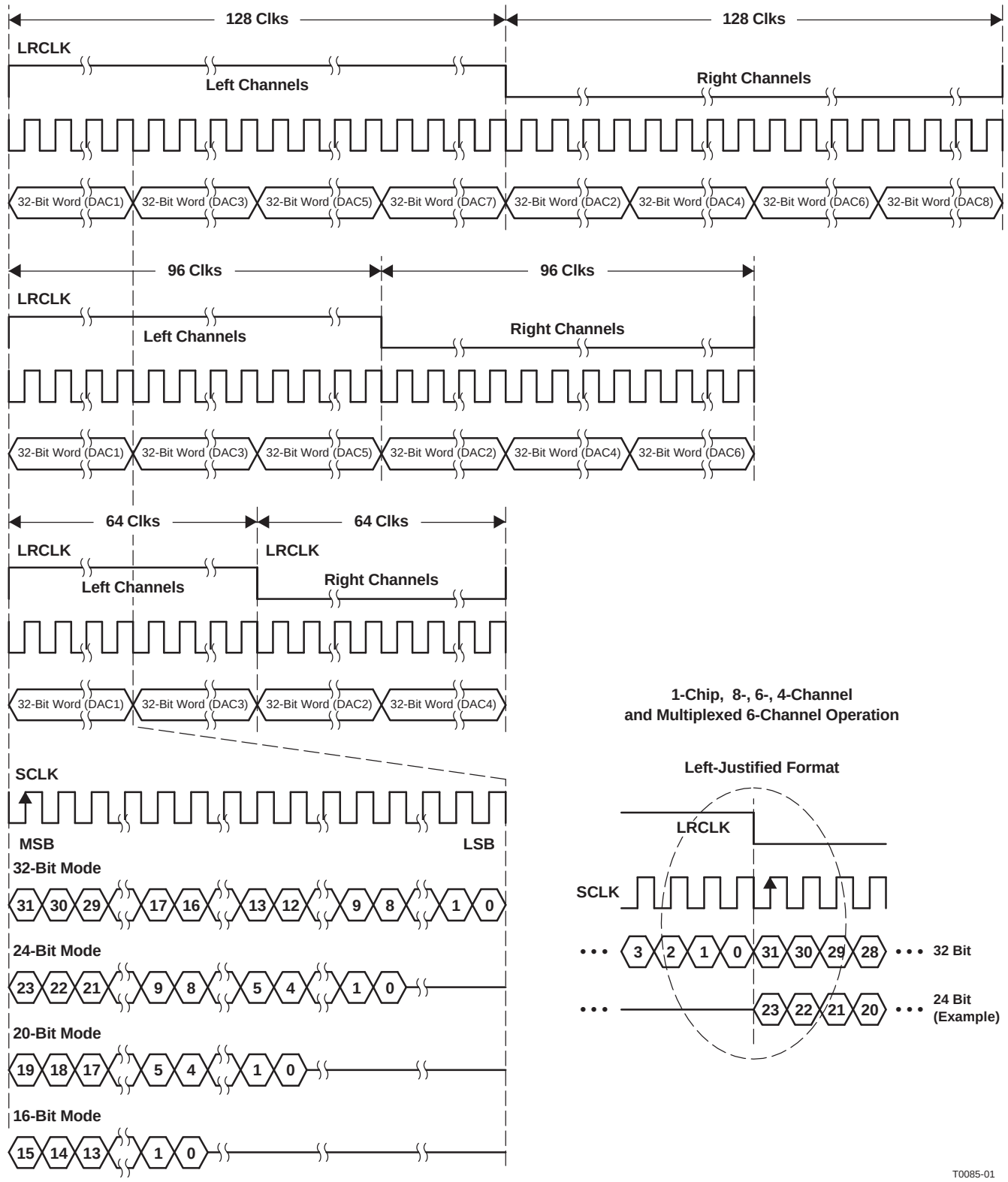


Figure 3-5. Left-Justified TDM Formats

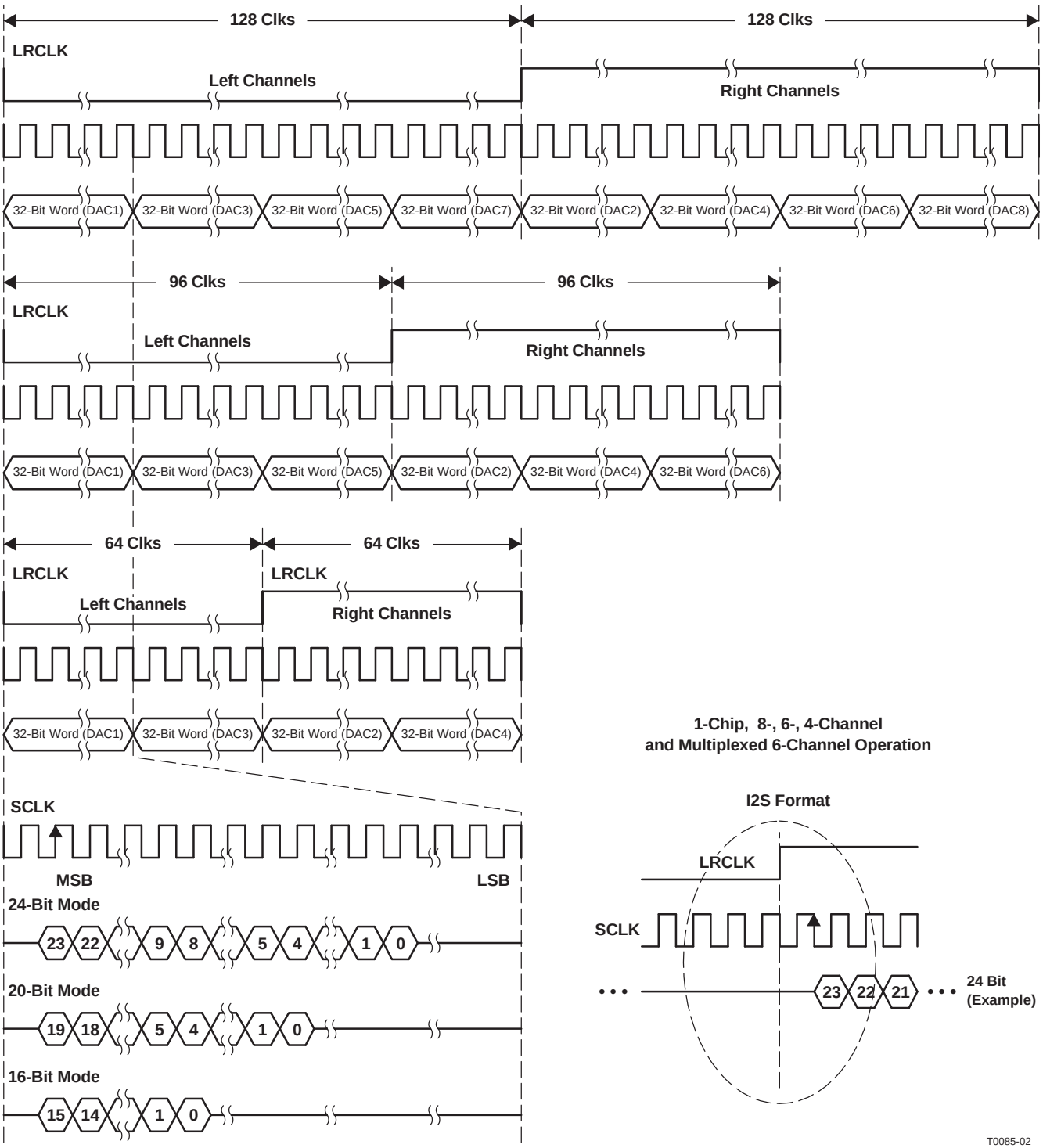


Figure 3-6. I²S TDM Formats

3.8.5 SAP Input to SAP Output—Processing Flow

All SAP data format options other than I^2S result in a two-sample delay from input to output, as shown in Figure 3-7. If I^2S formatting is used for both the input SAP and the output SAP, the polarity of LRCLK in Figure 3-7 must be inverted. However, if I^2S format conversions are performed between input and output, the delay becomes either 1.5 samples or 2.5 samples, depending on the processing clock frequency selected for the audio DSP core relative to the sample rate of the incoming data.

The I^2S format uses the falling edge of LRCLK to begin a sample period, whereas all other formats use the rising edge of LRCLK to begin a sample period. This means that the input SAP and audio DSP core operate on sample windows that are 180° out of phase, with respect to the sample window used by the output SAP. This phase difference results in the output SAP outputting a new data sample at the midpoint of the sample period used by the audio DSP core to process the data. If the processing cycle completes all processing tasks before the midpoint of the processing sample period, the output SAP outputs this processed data. However, if the processing time extends past the midpoint of the processing sample period, the output SAP outputs the data processed during the previous processing sample period. In the former case, the delay from input to output is 1.5 samples. In the latter case, the delay from input to output is 2.5 samples.

Therefore, delay from input to output can be either 1.5 or 2.5 sample times when data format conversions are performed that involve the I^2S format. However, which delay time is obtained for a particular application is determinable and fixed for that application, providing care is taken in the selection of MCLKI/XTALI with respect to the incoming sample clock, LRCLK.

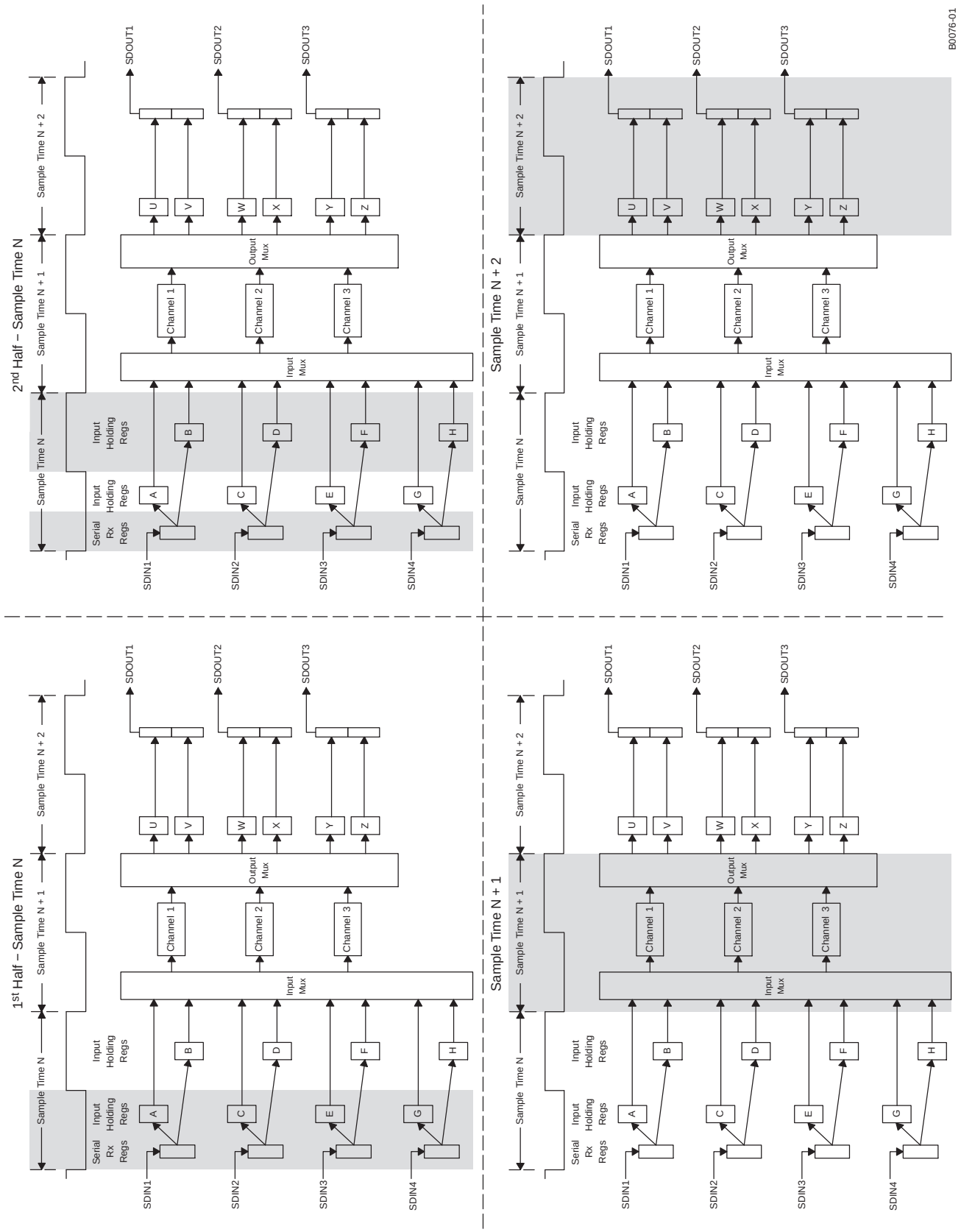


Figure 3-7. SAP Input-to-Output Latency

4 Algorithm and Software Development Tools for TAS3108/TAS3108IA

The TAS3108/TAS3108IA algorithm and software development tool set is a combination of classical development tools and graphical development tools. The tool set is used to build, debug, and execute programs in both the audio DSP and 8051 sections of the TAS3108/TAS3108IA.

Classical development tooling includes text editors, compilers, assemblers, simulators, and source-level debuggers. The 8051 can be programmed exclusively in ANSI C.

The 8051 tool set is an off-the-shelf tool set, with modifications as specified in this document. The 8051 tool set is a complete environment with an IDE, editor, compiler, debugger, and simulator.

The audio DSP core is programmed exclusively in assembly. The audio DSP tool set is a complete environment with an IDE, context-sensitive editor, assembler, and simulator/debugger.

Graphical development tooling provides a means of programming the audio DSP core and 8051 through a graphical drag-and-drop interface using modular audio software components from a component library. The graphical tooling produces audio DSP assembly and 8051 ANSI C code, as well as coefficients and data. The classical tools can also be used to produce the executable code.

In addition to building applications, the tool set supports the debug and execution of audio DSP and 8051 code on both simulators and EVM hardware.

5 Clock Controls

Clock management for the TAS3108/TAS3108IA consists of two control structures:

- Master clock management
  - Oversees the selection of the clock frequencies for the 8051 microprocessor, the I^2C controller, and the audio DSP core
  - The master clock (MCLKI or XTALI) is the source for these clocks.
  - In most applications, the master clock drives an on-chip digital phase-locked loop (DPLL), and the DPLL output drives the microprocessor and audio DSP clocks.
  - Also available is the DPLL bypass mode, in which the high-speed master clock directly drives the microprocessor and audio DSP clocks.
- Serial audio port (SAP) clock management
  - Oversees SAP master/slave mode
  - Controls output of SCLKOUT1, SCLKOUT2, and LRCLK in the SAP master mode

Figure 5-2 shows the clock circuitry in the TAS3108/TAS3108IA. Input pin MCLKI or XTALI provides the master clock for the TAS3108/TAS3108IA. Within the TAS3108/TAS3108IA, these two inputs are combined by an OR gate and, thus, only one of these two sources can be active at any one time. The source that is not active must be logic 0.

In normal operation, 1, 2, or 4 (as determined by the logic levels set at input pins PLL0 and PLL1) divides the master clock. The DPLL then multiplies this signal by 11 in frequency (PLL2 = LOW). The multiplier ratio is always 11 (pin PLL2 = LOW). The DPLL output is the processing clock used by the audio DSP core.

Table 5-1. PLL2, PLL1, and PLL0 Pin Configuration Controls

PLL2	PLL1	PLL0	AUDIO DSP CLOCK
0	0	0	11 × MCLK/1
0	0	1	11 × MCLK/2
0	1	0	11 × MCLK/4
0	1	1	Reserved
1	X	X	Reserved

Audio DSP clock or audio DSP clock/4 is used to clock the on-chip microprocessor. The input pin MICROCLK_DIV makes this clock choice. A logic-1 input level on this pin selects the audio DSP clock for the microprocessor clock; a logic-0 input level on this pin selects the audio DSP clock/4 for the microprocessor clock. The microprocessor clock must be ≤ 34 MHz.

Table 5-2. MICROCLK_DIV Pin Configuration Control

MICROCLK_DIV	MICROPROCESSOR CLOCK
0	Audio DSP clock/4
1	Audio DSP clock

NOTE

The state of PLL0, PLL1, PLL2, and MICROCLK_DIV can only be changed while the TAS3108 or TAS3108IA $\overline{\text{RESET}}$ pin is held low.

The TAS3108/TAS3108IA only supports dynamic sample-rate changes between any of the supported sample frequencies when a fixed-frequency master clock is provided. During dynamic sample-rate changes, the TAS3108/TAS3108IA remains in normal operation and the register contents are preserved. To avoid producing audio artifacts during the sample-rate changes, a volume or mute control can be included in the application firmware that mutes the output signal during the sample-rate change. The fixed-frequency clock can be provided by a crystal, attached to XTLI and XTLO, or an external 3.3-V fixed-frequency TTL source attached to MCLKI.

When the TAS3108/TAS3108IA is used in a system in which the master clock frequency (f_{MCLK}) can change, the TAS3108/TAS3108IA must be reset during the frequency change. In these cases, the procedure shown in Figure 5-1 should be used.

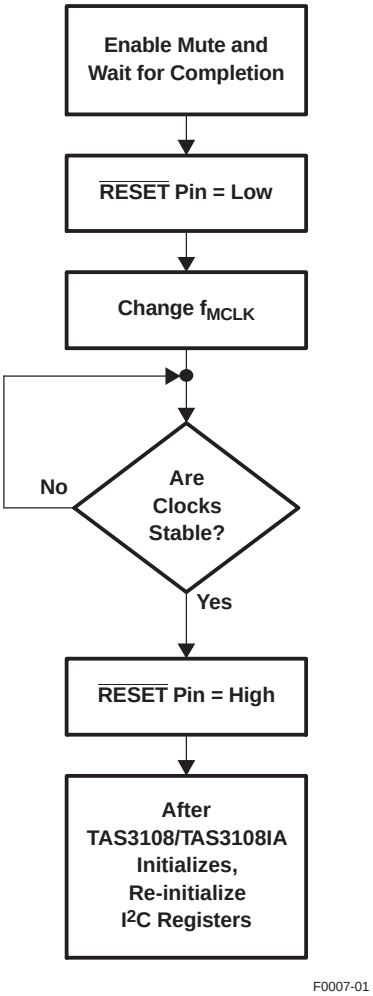


Figure 5-1. Master Clock Frequency (f_{MCLK}) Change Procedure

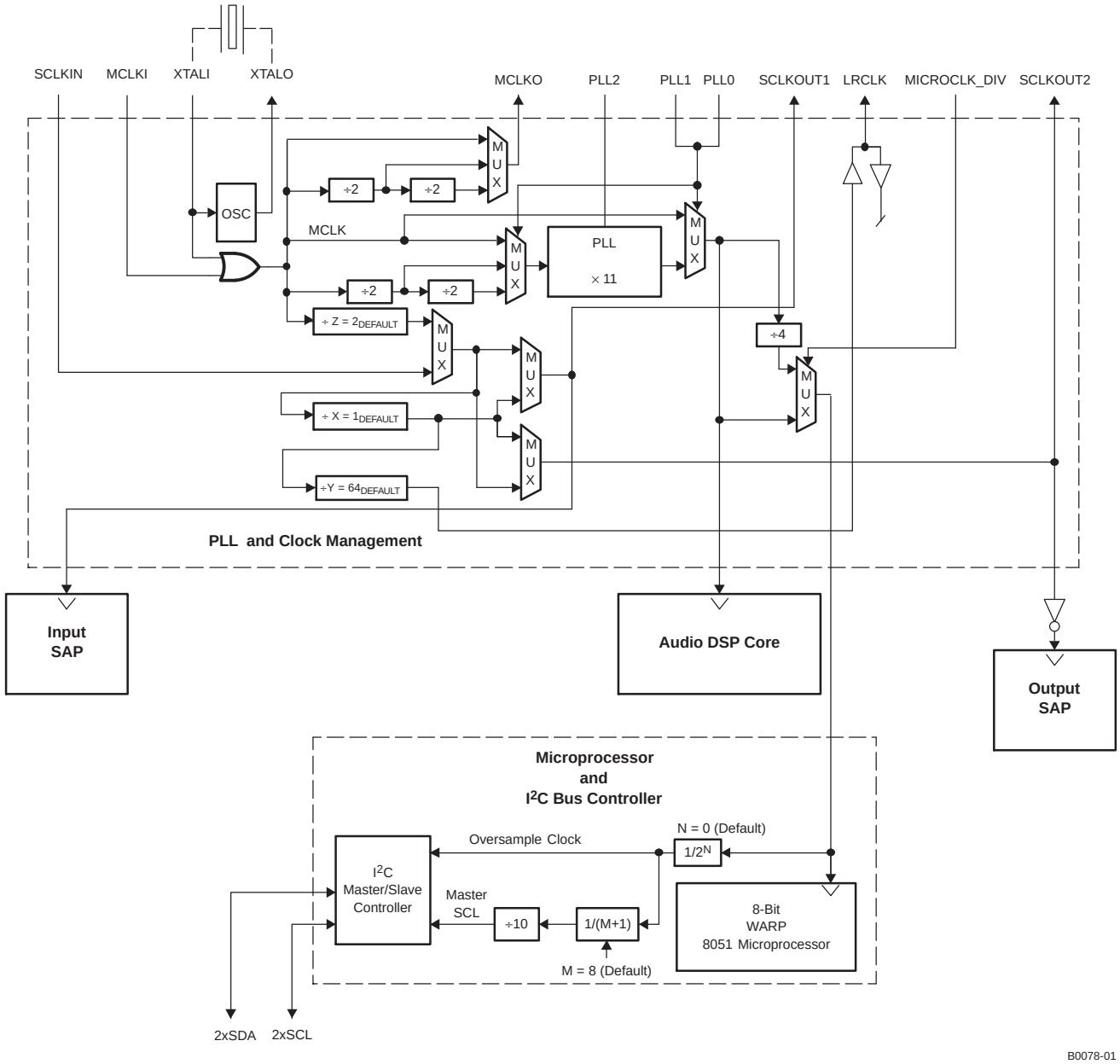
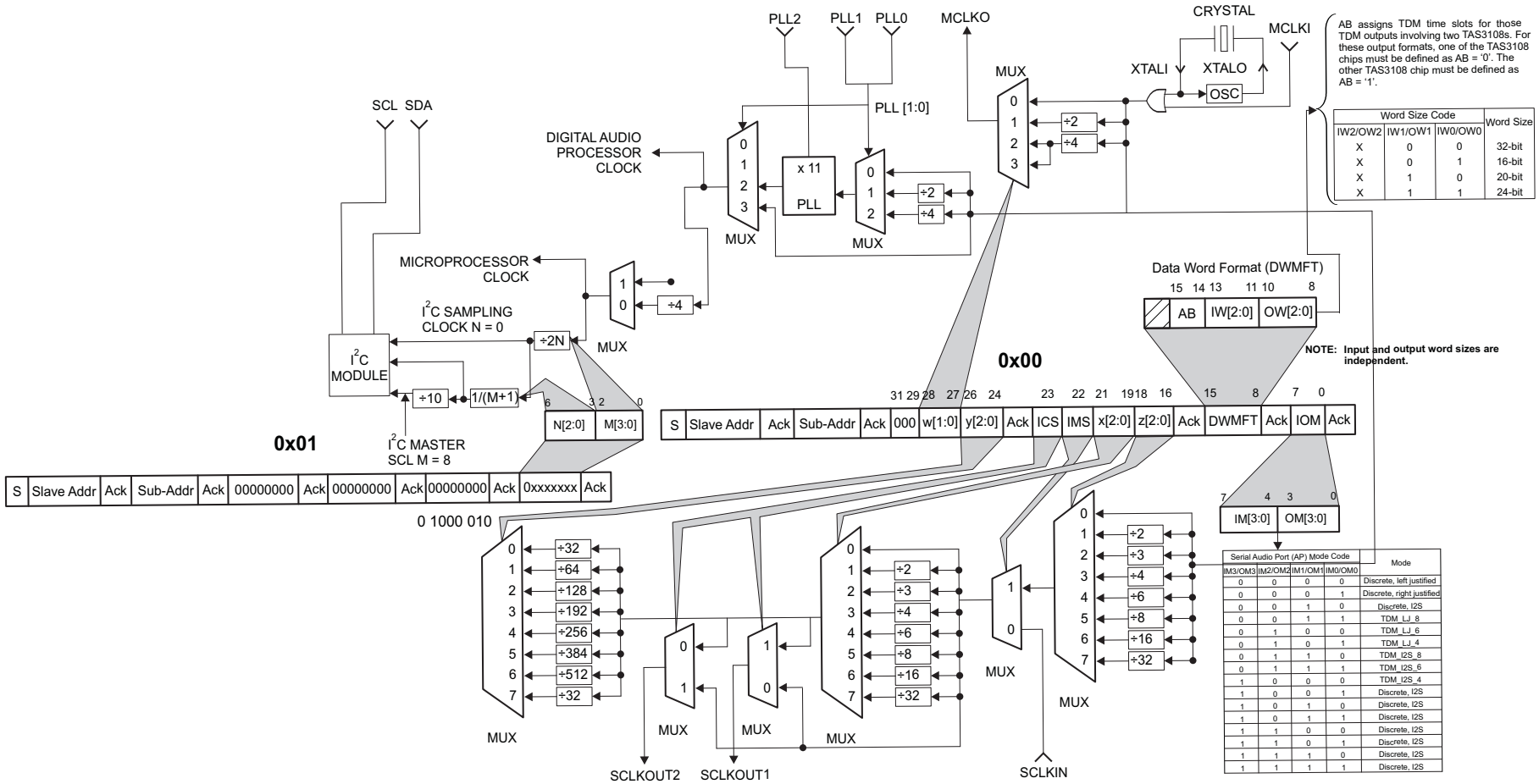


Figure 5-2. DPLL and Clock Management Block Diagram



Word Size Code			Word Size
IW2/OW2	IW1/OW1	IW0/OW0	
X	0	0	32-bit
X	0	1	16-bit
X	1	0	20-bit
X	1	1	24-bit

Serial Audio Port (AP) Mode Code				Mode
IM3/OM3	IM2/OM2	IM1/OM1	IM0/OM0	
0	0	0	0	Discrete, left justified
0	0	0	1	Discrete, right justified
0	0	1	0	Discrete, I2S
0	0	1	1	TDM_LJ_8
0	1	0	0	TDM_LJ_6
0	1	0	1	TDM_LJ_4
0	1	1	0	TDM_I2S_8
0	1	1	1	TDM_I2S_6
1	0	0	0	TDM_I2S_4
1	0	0	1	Discrete, I2S
1	0	1	0	Discrete, I2S
1	0	1	1	Discrete, I2S
1	1	0	0	Discrete, I2S
1	1	0	1	Discrete, I2S
1	1	1	0	Discrete, I2S
1	1	1	1	Discrete, I2S

Figure 5-3. Serial Data Format, Clock Management, and I²C M&N Assignments

When the serial audio port (SAP) is in the master mode, the SAP uses the MCLKI or XTALI master clock to drive the serial port clocks SCLKOUT1, SLCKOUT2, and LRCLK. When the SAP is in the slave mode, LRCLK is an input and SCLKOUT2 and SCLKOUT1 are derived from SCLKIN. As shown in Figure 5-2, SCLKOUT1 clocks data into the input SAP and SCLKOUT2 clocks data from the output SAP. Two distinct clocks are required to support TDM-to-discrete and discrete-to-TDM data-format conversions. Such format conversions also require that SCLKIN be the higher-valued bit-clock frequency. For TDM-in/discrete-out format conversions, SCLKIN must be equal to the input bit clock. For discrete-in/TDM-out format conversions, SCLKIN must be equal to the output bit clock. The frequency settings for SCLKOUT1, SCLKOUT2, and LRCLK in the SAP master mode, as well as the SAP master/slave mode selection, are all controlled by I^2C commands. Table 5-3 lists the default settings at power turnon or after a received reset.

Table 5-3. TAS3108/TAS3108IA Clock Default Settings

CLOCK	DEFAULT SETTING
SCLKOUT1	SCLKIN
SCLKOUT2	SCLKIN
MCLKO	MCLKI or XTALI
LRCLK	Input
Audio DSP clock	Set by pins PLL0 and PLL1
Microprocessor clock	Set by pin MICROCLK_DIV
PLL multiply ratio	11
I^2C sampling clock	N = 0
I^2C master SCL	M = 8

The selections provided by the dedicated TAS3108/TAS3108IA input pins and the programmable settings provided by I^2C subaddress commands give the TAS3108/TAS3108IA a variety of clocking options. However, the following clocking restrictions must be adhered to:

- MCLKI or XTALI ≥128 f_S

NOTE
For some TDM modes, MCLKI or XTALI must be ≥256 f_S

- Audio DSP clock <136 MHz
- Microprocessor clock/20 ≥ I^2C SCL clock
- Microprocessor clock ≤34 MHz
- I^2C oversample clock/20 ≥ I^2C SCL clock
- XTALI ≤20 MHz
- MCLKI ≤25 MHz

As long as these restrictions are met, all other clocking options are allowed.

See Section 7.1 for information on programming the clock register.

Table 5-4. TAS3108/TAS3108IA MCLK and LRCLK Common Values (MCLK = 12.288 MHz or MCLK = 11.2896 MHz)

f_S Sample Rate (kHz)	Ch per SDIN	MCLK/ LRCLK Ratio ($\times f_S$)	MCLK Freq (MHz)	SCLKIN Rate ($\times f_S$)	SCLKIN Freq (MHz)	MCLK/ SCLK 1, 2, 3, 4, 6, 8, 16, 32	X Mux 1, 2, 3, 4, 6, 8, 16, 32	SCLK OUT1 Rate ($\times f_S$)	Ch per SDOUT	SCLK OUT2 Rate ($\times f_S$)	LRCLK f_S Rate 32, 64, 128, 192, 256, 384, 512	Input Divider 1, 2, 4 (pins PLL0, PLL1)	PLL Multi-plier 11 (pin PLL2)	f_{DSPCLK} (MHz) Max 135.2 MHz	f_{DSPCLK}/f_S
Slave Mode, 2 Channels In, 2 Channels Out															
32	2	384	12.288	64	2.048	N/A	1	64	2	64	64	1	11	135.2	4224
44.1	2	256	11.2896	64	2.822	N/A	1	64	2	64	64	1	11	124.2	2816
48	2	256	12.288	64	3.072	N/A	1	64	2	64	64	1	11	135.2	2816
88.2	2	128	11.2896	64	5.645	N/A	1	64	2	64	64	1	11	124.2	1408
96	2	128	12.288	64	6.144	N/A	1	64	2	64	64	1	11	135.2	1408
176.4	2	64	11.2896	64	11.290	N/A	1	64	2	64	64	1	11	124.2	704
192	2	64	12.288	64	12.288	N/A	1	64	2	64	64	1	11	135.2	704
Slave Mode, 2 Channels In, TDM Out															
44.1	2	256	11.2896	256	11.290	N/A	4	64	8	256	64	1	11	124.2	2816
48	2	256	12.288	256	12.288	N/A	4	64	8	256	64	1	11	135.2	2816
88.2	2	128	11.2896	128	11.290	N/A	2	64	4	128	64	1	11	124.2	1408
96	2	128	12.288	128	6.144	N/A	2	64	4	128	64	1	11	135.2	1408
Slave Mode, TDM In, 2 Channels Out															
44.1	8	256	11.2896	256	11.290	N/A	4	256	2	64	64	1	11	124.2	2816
48	8	256	12.288	256	12.288	N/A	4	256	2	64	64	1	11	135.2	2816
88.2	4	128	11.2896	128	11.290	N/A	2	128	2	64	64	1	11	124.2	1408
96	4	128	12.288	128	12.288	N/A	2	128	2	64	64	1	11	135.2	1408
Slave Mode, TDM In, TDM Out															
44.1	8	256	11.2896	256	11.290	N/A	1	256	8	256	256	1	11	124.2	2816
48	8	256	12.288	256	12.288	N/A	1	256	8	256	256	1	11	135.2	2816
88.2	4	128	11.2896	128	11.290	N/A	1	128	4	128	128	1	11	124.2	1408
96	4	128	12.288	128	12.288	N/A	1	128	4	128	128	1	11	135.2	1408
Master Mode, 2 Channels In, 2 Channels Out															
32	2	384	12.288	N/A	N/A	6	1	64	2	64	64	1	11	135.2	4224
44.1	2	256	11.2896	N/A	N/A	4	1	64	2	64	64	1	11	124.2	2816
48	2	256	12.288	N/A	N/A	4	1	64	2	64	64	1	11	135.2	2816
88.2	2	128	11.2896	N/A	N/A	2	1	64	2	64	64	1	11	124.2	1408
96	2	128	12.288	N/A	N/A	2	1	64	2	64	64	1	11	135.2	1408
176.4	2	64	11.2896	N/A	N/A	1	1	64	2	64	64	1	11	124.2	704

Table 5-4. TAS3108/TAS3108IA MCLK and LRCLK Common Values (MCLK = 12.288 MHz or MCLK = 11.2896 MHz) (continued)

f_S Sample Rate (kHz)	Ch per SDIN	MCLK/ LRCLK Ratio ($\times f_S$)	MCLK Freq (MHz)	SCLKIN Rate ($\times f_S$)	SCLKIN Freq (MHz)	MCLK/ SCLK 1, 2, 3, 4, 6, 8, 16, 32	X Mux 1, 2, 3, 4, 6, 8, 16, 32	SCLK OUT1 Rate ($\times f_S$)	Ch per SDOUT	SCLK OUT2 Rate ($\times f_S$)	LRCLK f_S Rate 32, 64, 128, 192, 256, 384, 512	Input Divider 1, 2, 4 (pins PLL0, PLL1)	PLL Multi-plier 11 (pin PLL2)	f_{DSPCLK} (MHz) Max 135.2 MHz	f_{DSPCLK}/f_S
192	2	64	12.288	N/A	N/A	1	1	64	2	64	64	1	11	135.2	704
Master Mode, 2 Channels In, TDM Out															
44.1	2	256	11.2896	N/A	N/A	1	4	64	8	256	64	1	11	124.2	2816
48	2	256	12.288	N/A	N/A	1	4	64	8	256	64	1	11	135.2	2816
88.2	2	128	11.2896	N/A	N/A	1	2	64	4	128	64	1	11	124.2	1408
96	2	128	12.288	N/A	N/A	1	2	64	4	128	64	1	11	135.2	1408
32	2	384	12.288	N/A	N/A	2	3	64	6	192	64	1	11	135.2	4224
44.1	2	256	11.2896	N/A	N/A	2	2	64	4	128	64	1	11	124.2	2816
48	2	256	12.288	N/A	N/A	2	2	64	4	128	64	1	11	135.2	2816
32	2	384	12.288	N/A	N/A	3	2	64	4	384	64	1	11	135.2	4224
Master Mode, TDM In, 2 Channels Out															
44.1	8	256	11.2896	N/A	N/A	1	4	256	2	64	64	1	11	124.2	2816
48	8	256	12.288	N/A	N/A	1	4	256	2	64	64	1	11	135.2	2816
88.2	4	128	11.2896	N/A	N/A	1	2	128	2	64	64	1	11	124.2	1408
96	4	128	12.288	N/A	N/A	1	2	128	2	64	64	1	11	135.2	1408
32	6	384	12.288	N/A	N/A	2	3	192	2	64	64	1	11	135.2	4224
44.1	4	256	11.2896	N/A	N/A	2	2	128	2	64	64	1	11	124.2	2816
48	4	256	12.288	N/A	N/A	2	2	128	2	64	64	1	11	135.2	2816
32	4	384	12.288	N/A	N/A	3	6	384	2	64	64	1	11	135.2	4224
Master Mode, TDM In, TDM Out															
44.1	8	256	11.2896	N/A	N/A	1	1	256	8	256	256	1	11	124.2	2816
48	8	256	12.288	N/A	N/A	1	1	256	8	256	256	1	11	135.2	2816
88.2	4	128	11.2896	N/A	N/A	1	1	128	4	128	128	1	11	124.2	1408
96	4	128	12.288	N/A	N/A	1	1	128	4	128	128	1	11	135.2	1408
32	6	384	12.288	N/A	N/A	2	1	192	6	192	192	1	11	135.2	4224
44.1	4	256	11.2896	N/A	N/A	2	1	128	4	128	128	1	11	124.2	2816
48	4	256	12.288	N/A	N/A	2	1	128	4	128	128	1	11	135.2	2816
32	4	384	12.288	N/A	N/A	3	1	384	4	384	384	1	11	135.2	4224

6 Microprocessor Controller

The 8051 microprocessor receives and distributes I^{2}C write data, retrieves and outputs to the I^{2}C bus controllers the required I^{2}C read data, and participates in most processing tasks requiring multiframe processing cycles. The microprocessor has its own data RAM for storing intermediate values and queuing I^{2}C commands, a fixed boot-program ROM, and a program RAM. The microprocessor boot program cannot be altered. The microprocessor controller has specialized hardware for master and slave interface operation, volume updates, and a programmable interval timer interrupt. For more information, see the *TAS3108/TAS3108IA Firmware Programmer's Guide* (SLEU067).

The TAS3108/TAS3108IA has a slave-only I^{2}C interface that is compatible with the inter-IC (I^{2}C) bus protocol and supports both 100-kbps and 400-kbps data-transfer rates for multiple 4-byte write and read operations (maximum is 20 bytes). The slave I^{2}C control interface is used to program the registers of the device and to read device status.

The TAS3108/TAS3108IA also has a master-only I^{2}C interface that is compatible with the I^{2}C bus protocol and supports 375-kbps data transfer rates for multiple 4-byte write and read operations (maximum is 20 bytes). The master I^{2}C interface is used to load program and data from an external I^{2}C EEPROM.

On power up of the TAS3108/TAS3108IA, the slave interface is disabled and the master interface is enabled. Following a reset, the TAS3108/TAS3108IA disables the slave interface and enables the master interface. Using the master interface, the TAS3108/TAS3108IA automatically tests to see if an I^{2}C EEPROM is at address *1010xxx*. The value *xxx* can be chip select, other information, or don't cares, depending on the EEPROM selected. If a memory is present and it contains the correct header information and one or more blocks of program/memory data, the TAS3108/TAS3108IA loads the program, coefficient, and/or data memories from the EEPROM. If a memory is present, the download is complete when a header is read that has a zero-length data segment. At this point, the TAS3108/TAS3108IA disables the master I^{2}C interface, enables the slave I^{2}C interface, and starts normal operation.

If no memory is present or if an error occurred during the EEPROM read, TAS3108/TAS3108IA disables the master I^{2}C interface, enables the slave I^{2}C interface, and loads the unprogrammed default configuration. In this default configuration, the TAS3108/TAS3108IA streams eight channels of audio from input to output if the GPIO pin is LOW. The master and slave interfaces do not operate simultaneously.

In the slave mode, the I^{2}C bus is used to:

- Load the program and coefficient data
  - Microprocessor program memory
  - Microprocessor extended memory
  - Audio DSP core program memory
  - Audio DSP core coefficient memory
  - Audio DSP core data memory
- Update coefficient and other control values
- Read status flags

Once the microprocessor program memory has been loaded, it cannot be updated until the TAS3108/TAS3108IA has been reset.

The master and slave modes do not operate simultaneously.

When acting as an I^{2}C master, the data transfer rate is fixed at 375 kHz, assuming MCLKI or XTALI = 12.288 MHz, PLL0 = PLL1 = 0, and MICROCLK_DIV = 0.

When acting as an I^{2}C slave, the data transfer rate is determined by the master device on the bus. The I^{2}C communication protocol for the I^{2}C slave mode is shown in Figure 6-1.

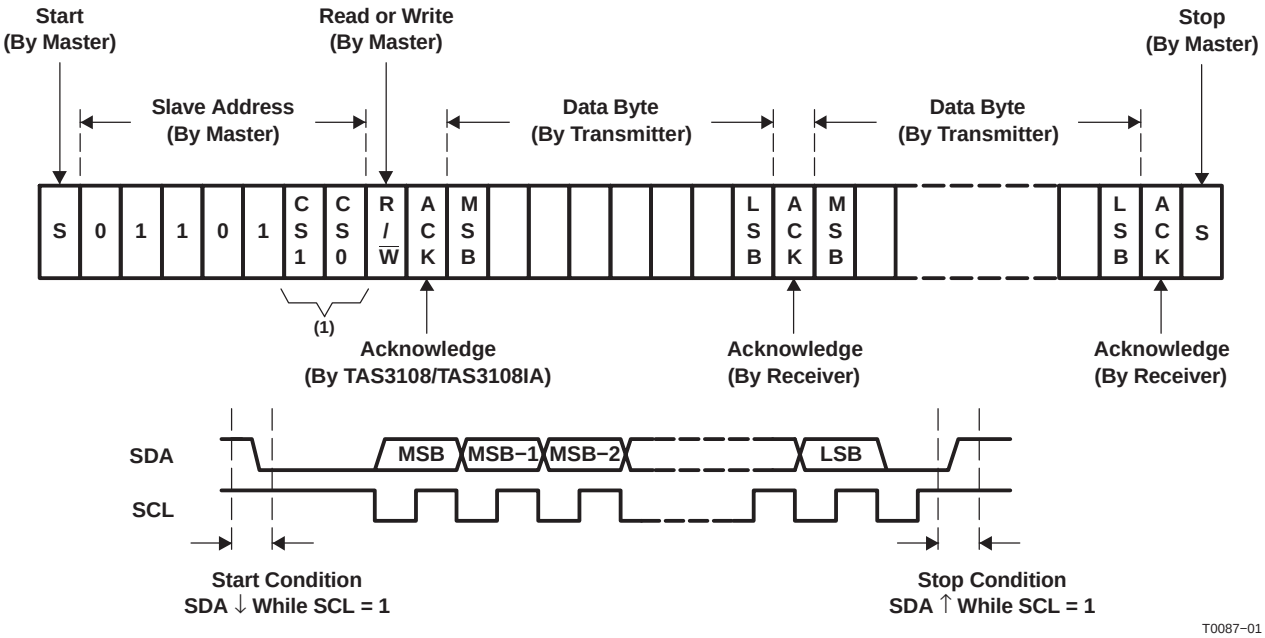


Figure 6-1. I²C Slave-Mode Communication Protocol

6.1 General I²C Operations

As shown in Figure 6-2, an I²C read transaction requires that the master device first issue a write transaction to give the TAS3108/TAS3108IA the subaddress to be used in the read transaction that follows. This subaddress assignment write transaction is then followed by the read transaction. For write transactions, the subaddress is supplied in the first byte of data written, and this byte is followed by the data to be written. For I²C write transactions, the subaddress must always be included in the data written. There cannot be a separate write transaction to supply the subaddress, as was required for read transactions. If a subaddress assignment-only write transaction is followed by a second write transaction supplying the data, erroneous behavior results. The first byte in the second write transaction is interpreted by the TAS3108/TAS3108IA as another subaddress replacing the one previously written.

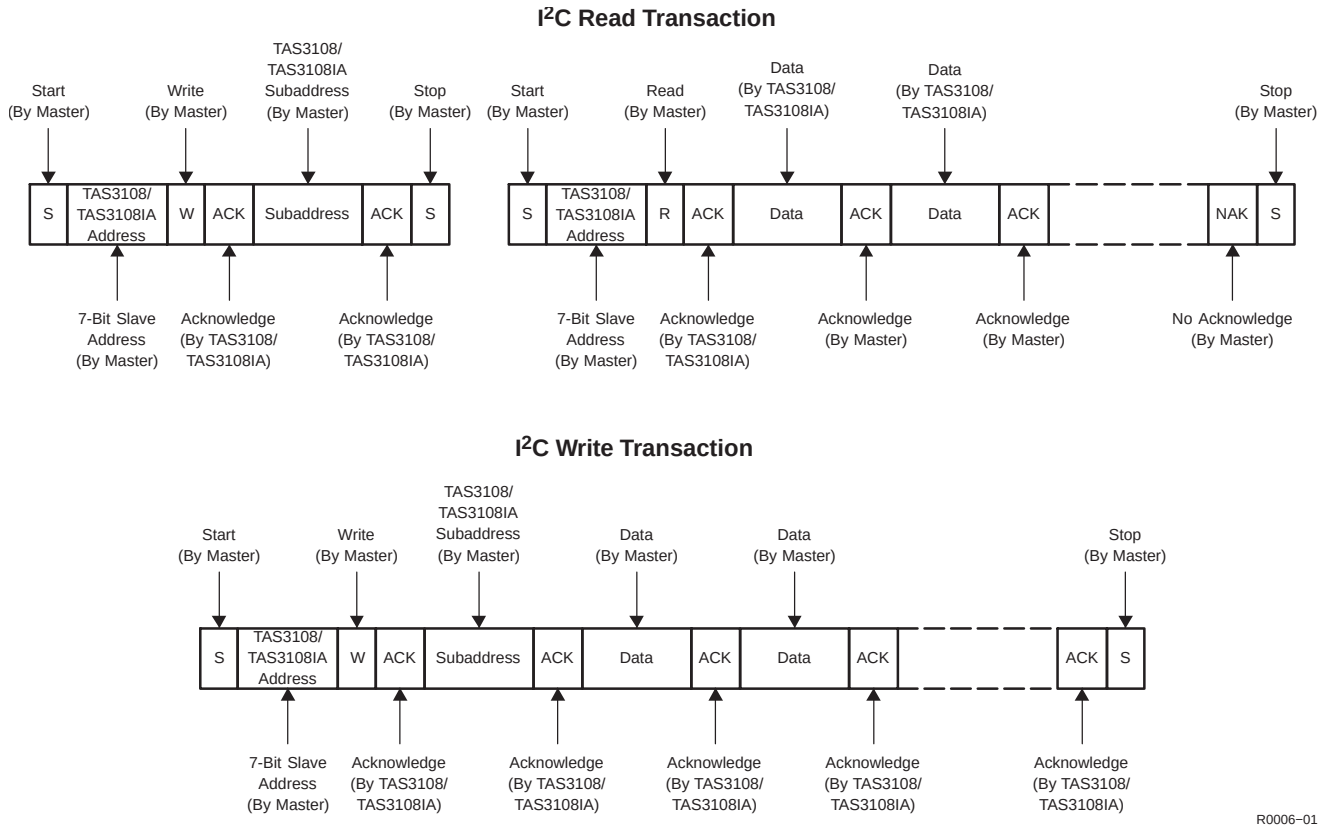


Figure 6-2. I²C Subaddress Access Protocol

6.2 Detailed I²C Operation

The I²C slave mode is the mode that is used to change configuration parameters during operation and to perform program and coefficient downloads from a master device. The latter can be used to replace the I²C master-mode EEPROM download. The TAS3108/TAS3108IA supports both random and sequential I²C transactions. The TAS3108/TAS3108IA I²C slave address is 011010xy, where the first six bits are the TAS3108/TAS3108IA device address and bit x is CS0, which is set by the TAS3108/TAS3108IA internal microprocessor at power up. Bit y is the R/$\overline{W}$ bit. The pulldown resistance of CS0 creates a default 00 address when no connection is made to the pin. Table 6-1 and Table 6-2 show all the legal addresses for I²C slave and master modes.

The TAS3108/TAS3108IA I²C block does respond to the broadcast address (00h).

Table 6-1. Slave Addresses

BASE ADDRESS	CS0	R/$\overline{W}$	SLAVE ADDRESS
0110 10	0	0	0x68
0110 10	0	1	0x69
0110 10	1	0	0x6A
0110 10	1	1	0x6B

Table 6-2. Master Addresses

BASE ADDRESS	CS0	R/$\overline{W}$	MASTER ADDRESS
1010 00	0	0	0xA0
1010 00	0	1	0xA1
1010 00	1	0	0xA2
1010 00	1	1	0xA3

The following is an example use of the I^2C master address to access an external EEPROM. The TAS3108/TAS3108IA can address up to two EEPROMs depending on the state of CS0. Initially, the TAS3108/TAS3108IA comes up in I^2C master mode. If it finds a memory such as the 24C512 EEPROM, it reads the headers and data as previously described. In this I^2C master mode, the TAS3108/TAS3108IA addresses the EEPROMs as shown in Table 6-3 and Table 6-4.

Table 6-3. EEPROM Address I^2C TAS3108/TAS3108IA Master Mode = 0xA1/A0

MSB					A0 (EEPROM)	CS0	R/$\overline{W}$
1	0	1	0	0	0	0	1/0

Table 6-4. EEPROM Address I^2C TAS3108/TAS3108IA Master Mode = 0xA3/A2

MSB					A0 (EEPROM)	CS0	R/$\overline{W}$
1	0	1	0	0	0	1	1/0

Random I^2C Transactions

Supplying a subaddress for each subaddress transaction is referred to as random I^2C addressing. For random I^2C read commands, the TAS3108/TAS3108IA responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a given subaddress does not use all 32 bits, the unused bits are read as logic 0. I^2C write commands, however, are treated in accordance with the data assignment for that address space. If a write command is received for a biquad subaddress, for example, the TAS3108/TAS3108IA expects to see five 32-bit words. If fewer than five data words have been received when a stop command (or another start command) is received, the data received is discarded.

Sequential I^2C Transactions

The TAS3108/TAS3108IA also supports sequential I^2C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential I^2C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS3108/TAS3108IA. For I^2C sequential write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted before a stop or start is transmitted determines how many subaddresses are written to. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; just the incomplete data is discarded.

Sequential read transactions do not have restrictions on outputting only complete subaddress data sets.

If the master does not issue enough data-received acknowledges to receive all the data for a given subaddress, the master device does not receive all the data.

If the master device issues more data-received acknowledges than required to receive the data for a given subaddress, the master device simply receives complete or partial sets of data, depending on how many data-received acknowledges are issued from the subaddress(es) that follow. I^2C read transactions, both sequential and random, can impose wait states.

For the standard I²C mode (SCL = 100 kHz), worst-case wait state time for an 8-MHz microprocessor clock is on the order of 2 µs. Nominal wait-state time for the same 8-MHz microprocessor clock is on the order of 1 µs. For the fast I²C mode (SCL = 400 kHz) and the same 8-MHz microprocessor clock, worst-case wait-state time can extend up to 10.5 µs in duration. Nominal wait-state time for this same case lies in a range from 2 µs to 4.6 µs. Increasing the microprocessor clock frequency lowers the wait-state time and for the standard I²C mode, a faster microprocessor clock can totally eliminate the presence of wait states.

For example, increasing the microprocessor clock to 16 MHz results in no wait states. For the fast I²C mode, faster microprocessor clocks shorten the wait-state time encountered, but do not totally eliminate wait states.

6.2.1 Multiple-Byte Write

Multiple data bytes are transmitted by the master device to slave as shown in Figure 6-3. After receiving each data byte, the TAS3108/TAS3108IA responds with an acknowledge bit.

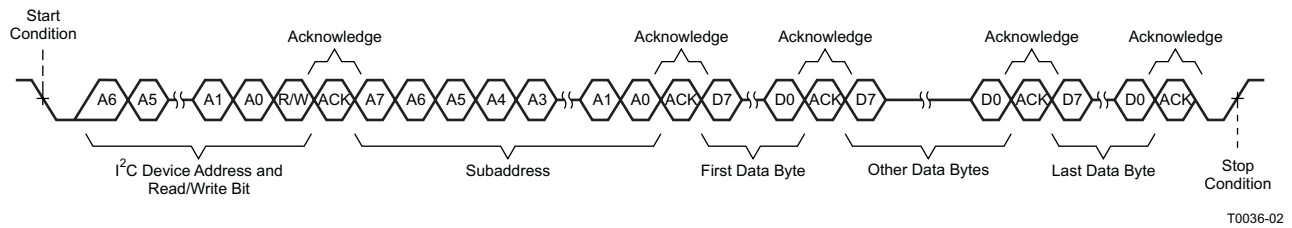


Figure 6-3. Multiple-Byte Write Transfer

6.2.2 Multiple-Byte Read

Multiple data bytes are transmitted by the TAS3108/TAS3108IA to the master device as shown in Figure 6-4. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

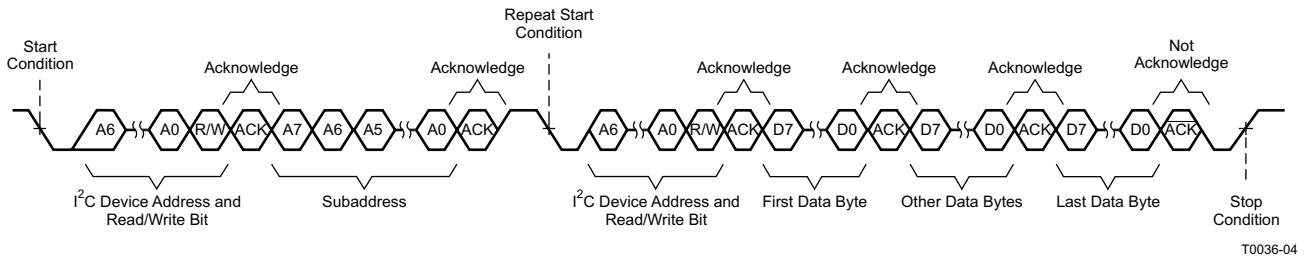


Figure 6-4. Multiple-Byte Read Transfer

6.3 I²C Master-Mode Device Initialization

I²C master-mode operation is enabled following a reset or power-on reset. Master-mode I²C transactions do not start until the I²C bus is idle.

The TAS3108/TAS3108IA uses the master mode to download from EEPROM the memory contents for the microprocessor program memory, microprocessor extended memory, audio DSP core program memory, audio DSP core coefficient memory, and audio DSP core data memory.

The TAS3108/TAS3108IA, when operating as an I²C master, can execute a complete download of any internal memory or any section of any internal memory without requiring any wait states.

When the TAS3108/TAS3108IA operates as an I^2C master, the TAS3108/TAS3108IA generates a repeated start without an intervening stop command while downloading program and memory data from EEPROM. When a repeated start is sent to the EEPROM in read mode, the EEPROM enters a sequential read mode to transfer large blocks of data quickly.

The TAS3108/TAS3108IA queries the bus for an I^2C EEPROM at address 1010xxx. The value xxx can be chip select, other information, or don't cares, depending on the EEPROM selected.

The first action of the TAS3108/TAS3108IA as master is to transmit a start condition along with the device address of the I^2C EEPROM with the read/write bit cleared (0) to indicate a write. The EEPROM acknowledges the address byte, and the TAS3108/TAS3108IA sends a subaddress byte, which the EEPROM acknowledges. Most EEPROMs have at least 2-byte addresses and acknowledge as many as are appropriate. At this point, the EEPROM sends a last acknowledge and becomes a slave transmitter. The TAS3108/TAS3108IA acknowledges each byte repeatedly to continue reading each data byte that is stored in memory.

The memory load information starts with reading the header and data information that starts at subaddress 0 of the EEPROM. This information must then be stored in sequential memory addresses with no intervening gaps. The data blocks are contiguous blocks of data that immediately follow the header locations.

The TAS3108/TAS3108IA memory data can be stored and loaded in (almost) any order. Additionally, this addressing scheme permits portions of the TAS3108/TAS3108IA internal memories to be loaded.

I^2C EEPROM Memory Map

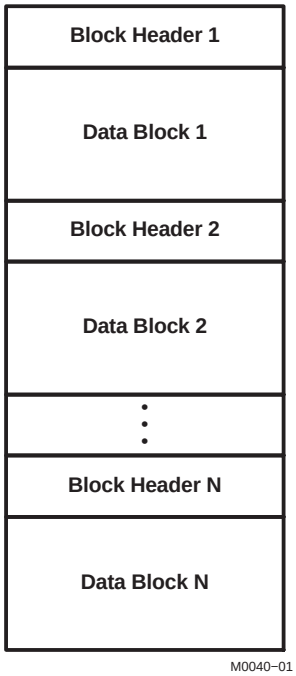


Figure 6-5. EEPROM Address Map

The TAS3108/TAS3108IA sequentially reads EEPROM memory and loads its internal memory unless it does not find a valid memory header block, is not able to read the next memory location because the end of memory was reached, detects a checksum error, or reads an end-of-program header block. When it encounters an invalid header or read error, the TAS3108/TAS3108IA attempts to read the header or memory location three times before it determines that it has an error. If the TAS3108/TAS3108IA encounters a checksum error it attempts to reread the entire block of memory two more times before it determines that it has an error.

Once the microprocessor program memory has been loaded, it cannot be reloaded until the TAS3108/TAS3108IA has been reset.

If an error is encountered, TAS3108/TAS3108IA terminates its memory-load operation, loads the default configuration, and disables further master I^2C bus operations.

If an end-of-program data block is read, the TAS3108/TAS3108IA has completed the initial program load.

The I^2C master mode uses the starting and ending I^2C checksums to verify a proper EEPROM download. The first 16-bit data word received from the EEPROM, the I^2C checksum at subaddress 0x00, is stored and compared against the 16-bit data word received for the last subaddress, the ending I^2C checksum, and the checksum that is computed during the download. These three values must be equal. If the read and computed values do not match, the TAS3108/TAS3108IA sets the memory read error bits in the status register and repeats the download from the EEPROM two more times. If the comparison check fails the third time, the TAS3108/TAS3108IA sets the microprocessor program to the default value.

Table 6-5 shows the format of the EEPROM or other external memory load file. Each line of the file is a byte (in ASCII format). The checksum is the summation of all the bytes (with beginning and ending checksum fields = 00). The final checksum inserted into the checksum field is the lowest significant four bytes of the checksum.

Example:

Given the following example 8051 data or program block (must be a multiple of 4 bytes for these blocks):

10h

20h

30h

40h

50h

60h

70h

80h

The checksum = 10h + 20h + 30h + 30h + 40h + 50h + 60h + 70h + 80h = 240h, so

the values put in the checksum fields are MS byte = 02h and LS byte = 40h.

If the checksum is > FFFFh, the 2-byte checksum field is the least-significant two bytes.

For example, if the checksum is 1D 45B6h, the checksum field is MS byte = 45h and LS byte = B6h.

Table 6-5. TAS3108/TAS3108IA Memory Block Structures

STARTING BYTE	DATA BLOCK FORMAT	SIZE	NOTES
12-Byte Header Block			
0	Checksum code MS byte	2 bytes	Checksum of bytes 2 through N + 12
	Checksum code LS byte		
2	Header ID byte 1 = 0x00	2 bytes	Must be 0x001F for the TAS3108/TAS3108IA to load
	Header ID byte 2 = 0x1F		
4	Memory to be loaded	1 byte	0x00 Microprocessor program memory or termination header 0x01 Microprocessor external data memory 0x02 Audio DSP core program memory 0x03 Audio DSP core coefficient memory 0x04 Audio DSP core data memory 0x05–0x0F Reserved for future expansion
5	0x00	1 byte	Unused
6	Start TAS3108/TAS3108IA memory address MS byte	2 bytes	If this is a termination header, this value is 0000.
	Start TAS3108/TAS3108IA memory address LS byte		
8	Total number of bytes transferred MS byte	2 bytes	12 + data bytes + last checksum bytes. If this is a termination header, this value is 0000.
	Total number of bytes transferred LS byte		
10	0x00	1 bytes	Unused
11	0x00	1 bytes	Unused
Data Block for Microprocessor Program or Data Memory (Following 12-Byte Header)			
12	Data byte 1 (LS byte)	4 bytes	1–4 microprocessor bytes
	Data byte 2		
	Data byte 3		
	Data byte 4 (MS byte)		
16	Data byte 5	4 bytes	5–8 microprocessor bytes
	Data byte 6		
	Data byte 7		
	Data byte 8		
	•		
	•		
	•		
N + 8	Data byte 4*(Z – 1) + 1	4 bytes	
	Data byte 4*(Z – 1) + 2		
	Data byte 4*(Z – 1) + 3		
	Data byte 4*(Z – 1) + 4 = N		
N + 12	0x00	4 bytes	Repeated checksum bytes 2 through N + 11
	0x00		
	Checksum code MS byte		
	Checksum code LS byte		
Data Block for Audio DSP Core Coefficient Memory (Following 12-Byte Header)			
12	Data byte 1 (LS byte)	4 bytes	Coefficient word 1 (valid data in D27–D0) D7–D0
	Data byte 2		D15–D8
	Data byte 3		D23–D16
	Data byte 4 (MS byte)		D31–D24

Table 6-5. TAS3108/TAS3108IA Memory Block Structures (continued)

STARTING BYTE	DATA BLOCK FORMAT	SIZE	NOTES
16	Data byte 5	4 bytes	Coefficient word 2
	Data byte 6		
	Data byte 7		
	Data byte 8		
	•		
	•		
	•		
N + 8	Data byte 4*(Z – 1) + 1	4 bytes	Coefficient word Z
	Data byte 4*(Z – 1) + 2		
	Data byte 4*(Z – 1) + 3		
	Data byte 4*(Z – 1) + 4 = N		
N + 12	0x00	4 bytes	Repeated checksum bytes 2 through N + 11
	0x00		
	Checksum code MS byte		
	Checksum code LS byte		
Data Block for Audio DSP Core Data Memory (Following 12-Byte Header)			
12	Data byte 1 (LS byte)	6 bytes	Data word 1 D7–D0
	Data byte 2		D15–D8
	Data byte 3		D23–D16
	Data byte 4		D31–D24
	Data byte 5		D39–D32
	Data byte 6 (MS byte)		D47–D40
18	Data byte 7	6 bytes	Data 2
	Data byte 8		
	Data byte 9		
	Data byte 10		
	Data byte 11		
	Data byte 12		
	•		
	•		
	•		
N + 6	Data byte 6*(Z – 1) + 1	6 bytes	Data Z
	Data byte 6*(Z – 1) + 2		
	Data byte 6*(Z – 1) + 3		
	Data byte 6*(Z – 1) + 4		
	Data byte 6*(Z – 1) + 5		
	Data byte 6*(Z – 1) + 6 = N		
N + 12	0x00	6 bytes	Repeated checksum bytes 2 through N + 11
	0x00		
	0x00		
	0x00		
	Checksum code MS byte		
	Checksum code LS byte		

Table 6-5. TAS3108/TAS3108IA Memory Block Structures (continued)

STARTING BYTE	DATA BLOCK FORMAT	SIZE	NOTES
Data Block for Audio DSP Core Program Memory (Following 12-Byte Header)			
12	Program byte 1 (LS byte)	7 bytes	Program word 1 (valid data in D53–D0) D7–D0
	Program byte 2		D15–D8
	Program byte 3		D23–D16
	Program byte 4		D31–D24
	Program byte 5		D39–D32
	Program byte 6		D47–D40
	Program byte 7 (MS byte)		D55–D48
19	Program byte 8	7 bytes	Program word 2
	Program byte 9		
	Program byte 10		
	Program byte 11		
	Program byte 12		
	Program byte 14		
	Program byte 15		
	•		
	•		
	•		
N + 5	Program byte 7*(Z – 1) + 1	7 bytes	Program word Z
	Program byte 7*(Z – 1) + 2		
	Program byte 7*(Z – 1) + 3		
	Program byte 7*(Z – 1) + 4		
	Program byte 7*(Z – 1) + 5		
	Program byte 7*(Z – 1) + 6		
	Program byte 7*(Z – 1) + 7 = N		
N + 12	0x00	7 bytes	Repeated checksum bytes 2 through N + 11
	0x00		
	0x00		
	0x00		
	0x00		
	Checksum code MS byte		
	Checksum code LS byte		
20-Byte Termination Block (Last Block of Entire Load Block)			
B_{LAST} – 19	0x00	2 bytes	First two bytes of termination block are always 0x0000.
	0x00		
B_{LAST} – 17	0x00	2 bytes	Second two bytes are always 0x001F.
	0x1F		
B_{LAST} – 15	0x00	1 byte	Last 16 bytes must each be 0x00.
B_{LAST} – 14	0x00	1 byte	
	•		
B_{LAST}	0x00	1 byte	

7 I²C Register Map

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	INITIALIZATION VALUE
0x00	Clock and SAP control register	4	Description shown in Section 7.1	0x01, 0x00, 0x1B, 0x22
0x01	Reserved	4	Reserved	0x00, 0x00, 0x00, 0x40
0x02	Status register	4	Description shown in Section 7.2	0x00, 0x00, 0x00, 0x00
0x03	Unused			0x00, 0x00, 0x00, 0x00
0x04	I²C memory load control register	8	Description shown in Section 7.3	
0x05	I²C memory load data register	8	Description shown in Section 7.3	
0x06	PEEK/POKE address	4	u(31:24)(1), MemSelect(23:16), Addr(15:8), Addr(7:0)	0x00, 0x00, 0x00, 0x00
0x07	PEEK/POKE data	16	D(63:56), D(55:48), D(47:40), D(39:32), D(31:24), D(23:16), D(15:8), D(7:0)	0x00, 0x00, 0x00, 0x00
0x08	Version number	4	TAS3108/TAS3108IA version	0x00, 0x00, 0x00, 0x01
0x09	User-defined	4, 8, 12, 16, or 20	User-defined register 1	User-defined
0x0A	User-defined	4, 8, 12, 16, or 20	User-defined register 2	User-defined
• • •			• • •	
0xFE	User-defined	4, 8, 12, 16, or 20	User-defined register 246	User-defined
0xFF	User-defined	4, 8, 12, 16, or 20	User-defined register 247	User-defined

(1) u indicates unused bits.

In the following sections, **BOLD** indicates the default state of the bit fields.

7.1 Clock Control Register (0x00)

Register 0x00 provides the user with control over MCLK, LRCLK, SCLKOUT1, SCLKOUT2, data-word size, and serial audio port modes. Register 0x00 default = **0x0100 1B22**.

Table 7-1. Clock Control Register (0x00)

D31	D30	D29	D28	D27	D26	D25	D24	DESCRIPTION
0	0	0						Not Used
			W1	W0				Master clock output divider
					Y2	Y1	Y0	Master mode LRCLK divider
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**DESCRIPTION**
ICS								SCLKOUT select (**default = 0**)
	IMS							SAP master/slave mux select (1 = master mode, **0 = slave mode**)
		X2	X1	X0				SCLKIN and SCLKOUT clock divide
					Z2	Z1	Z0	MCLK, SCLK ratio (master mode only)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**DESCRIPTION**
X	X							Don't care
		X						Don't care
			IW1	IW0				Input audio data word size
					X			Don't care
						OW1	OW0	Output audio data word size
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**DESCRIPTION**
IM3	IM2	IM1	IM0					Input data format
				OM3	OM2	OM1	OM0	Output data format

7.1.1 Master Clock Output Divider

Bits 28–27 (W1 and W0) define the ratio between MCLKI (or the crystal frequency) and MCLKO. This allows the accommodation of devices that require an MCLK = 128 LRCLK and devices that require an MCLK = 256 LRCLK, without having to use glue logic to divide that clock down. This bit has meaning whether in clock-master or clock-slave mode.

W1	W0	DESCRIPTION
0	**0**	**MCLKO = MCLKI**
0	1	MCLKO = MCLKI/2
1	0	MCLKO = MCLKI/4
1	1	MCLKO = MCLKI/4

7.1.2 Master Mode LRCLK Divider

Bits 26–24 (Y2, Y1, and Y0) define the ratio between SCLK and LRCLK, but only have meaning in the clock-master mode where LRCLK is an output. In the clock-slave mode, LRCLK is an input.

Y2	Y1	Y0	DESCRIPTION
0	0	0	LRCLK out = SCLK/32
0	**0**	**1**	**LRCLK out = SCLK/64**
0	1	0	LRCLK out = SCLK/128
0	1	1	LRCLK out = SCLK/192
1	0	0	LRCLK out = SCLK/256
1	0	1	LRCLK out = SCLK/384
1	1	0	LRCLK out = SCLK/512
1	1	1	LRCLK out = SCLK/32

7.1.3 SCLKIN and SCLKOUT Clock Divide

Bits 21–19 (X2, X1, and X0) define the ratio between SCLKIN and SCLKOUT. These control bits are only used when the input and output rates are different, which can happen if TDM and discrete modes are both used (for example, input is TDM and output is discrete). Normally, these bits are set to 000, so that SCLKOUT1 (input SCLK) and SLCKOUT2 (output SCLK) are the same. (Note that SCLKIN is not the input SCLK, but is used in clock-slave mode to derive SCLKOUT1.)

X2	X1	X0	DESCRIPTION
0	**0**	**0**	**X MUX out = IMS_MUX (master/slave SCLK)**
0	0	1	X MUX out = IMS_MUX/2
0	1	0	X MUX out = IMS_MUX/3
0	1	1	X MUX out = IMS_MUX/4
1	0	0	X MUX out = IMS_MUX/6
1	0	1	X MUX out = IMS_MUX/8
1	1	0	X MUX out = IMS_MUX/16
1	1	1	X MUX out = IMS_MUX/32

7.1.4 MCLK, SCLK Ratio (Master Mode Only)

Bits 18–16 (Z2, Z1, and Z0) define the ratio between MCLK and SCLK when the TAS3108/TAS3108IA is the clock master. In clock-slave mode, these bits are don't care.

Z2	Z1	Z0	DESCRIPTION
0	**0**	**0**	**Z MUX out = MCLK (MCLKI or crystal oscillator)**
0	0	1	Z MUX out = MCLK/2
0	1	0	Z MUX out = MCLK/3
0	1	1	Z MUX out = MCLK/4
1	0	0	Z MUX out = MCLK/6
1	0	1	Z MUX out = MCLK/8
1	1	0	Z MUX out = MCLK/16
1	1	1	Z MUX out = MCLK/32

7.1.5 Audio Data Word Size

Bits 12–11 (IW1 and IW0) define the data word size for the input SAP. Bits 9–8 (OW1 and OW0) define the data word size for the output SAP.

IW1/OW1	IW0/OW0	DESCRIPTION
0	0	32-bit audio data
0	1	16-bit audio data
1	0	20-bit audio data
1	**1**	**24-bit audio data**

7.1.6 Input and Output Data Format

Bits 7–4 (IM3, IM2, IM1, and IM0) define the input data format. Bits 3–0 (OM3, OM2, OM1, and OM0) define the output data format. The two formats need not be the same, only compatible.

IM3/OM3	IM2/OM2	IM1/OM1	IM0/OM0	DESCRIPTION
0	0	0	0	2 channel, left justified
0	0	0	1	2 channel, right justified
0	**0**	**1**	**0**	**2 channel, I^2S**
0	0	1	1	TDM, left justified (8 channels)
0	1	0	0	TDM, left justified (6 channels)
0	1	0	1	TDM, left justified (4 channels)
0	1	1	0	TDM, I^2S (8 channels)
0	1	1	1	TDM, I^2S (6 channels)
1	0	0	0	TDM, I^2S (4 channels)
1	0	0	1	2 channel, I^2S
1	0	1	0	2 channel, I^2S
1	0	1	1	2 channel, I^2S
1	1	0	0	2 channel, I^2S
1	1	0	1	2 channel, I^2S
1	1	1	0	2 channel, I^2S
1	1	1	1	2 channel, I^2S

7.2 Status Register (0x02)

During I²C download, the write operation to indicate that a particular memory is to be written causes the TAS3108/TAS3108IA to set an error bit to indicate a load for that memory type. This error bit is cleared when the operation completes successfully.

Table 7-2. Status Register (0x02)

D31	D30	D29	D28	D27	D26	D25	D24	DESCRIPTION
–	–	–	–	–	–	–	–	Firmware definable
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**DESCRIPTION**
–	–	–	–	–	–	–	–	Firmware definable
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**DESCRIPTION**
								Firmware definable
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**DESCRIPTION**
0	0	–	–	–	–	–	1	Microprocessor program memory load error
0	0	–	–	–	–	1	–	Microprocessor external data memory load error
0	0	–	–	–	1	–	–	Audio DSP core program memory load error
0	0	–	–	1	–	–	–	Audio DSP core coefficient memory load error
0	0	–	1	–	–	–	–	Audio DSP core data memory load error
0	0	1	–	–	–	–	–	Invalid memory select
1	1	1	1	0	0	0	0	End-of-load header error
1	1	1	1	1	1	1	1	No EPROM present
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**No errors**

7.3 I²C Memory Load Control and Data Registers (0x04 and 0x05)

Registers 0x04 (Table 7-3) and 0x05 (Table 7-4) allow the user to download TAS3108/TAS3108IA program code and data directly from the system I²C controller. This mode is called the I²C slave mode (from the TAS3108/TAS3108IA point-of-view). See the *TAS3108/TAS3108IA Firmware Programmer's Guide* (SLEU067) for more details.

Table 7-3. TAS3108/TAS3108IA Memory Load Control Register (0x04)

BYTE	DATA BLOCK FORMAT	SIZE	NOTES
1–2	Checksum code	2 bytes	Checksum of bytes 2 through N + 8. If this is a termination header, this value is 0000.
3–4	Memory to be loaded	2 bytes	0 Microprocessor program memory 1 Microprocessor external data memory 2 Audio DSP core program memory 3 Audio DSP core coefficient memory 4 Audio DSP core data memory 5–15 Reserved for future expansion
5	Unused	1 byte	Reserved for future expansion
6–7	Starting TAS3108/TAS3108IA memory address	2 bytes	If this is a termination header – this value is 0000.
7–8	Number of data bytes to be transferred	2 bytes	If this is a termination header – this value is 0000.

Table 7-4. TAS3108/TAS3108IA Memory Load Data Register (0x05)

BYTE	8-BIT DATA	28-BIT DATA	48-BIT DATA	54-BIT DATA
1	Datum 1 D7–D0	0000 D27–D24	0000 0000	0000 0000
2	Datum 2 D7–D0	D7–D0	0000 0000	00 D53–D48
3	Datum 3 D7–D0	D15–D8	D47–D40	D47–D40
4	Datum 4 D7–D0	D7–D0	D39–D32	D39–D32
5	Datum 5 D7–D0	0000 D27–D24	D31–D24	D31–D24
6	Datum 6 D7–D0	D23–D16	D23–D16	D23–D16
7	Datum 7 D7–D0	D15–D8	D15–D8	D15–D8
8	Datum 8 D7–D0	D7–D0	D7–D0	D7–D0

7.4 Memory Access Registers (0x06 and 0x07)

Registers 0x06 (Table 7-5) and 0x07 (Table 7-6) allow the user to access the internal resources of the TAS3108/TAS3108IA. See *TAS3108/TAS3108IA Firmware Programmer's Guide* (SLEU067) for more details.

Table 7-5. Memory Select and Address Register (0x06)

D31	D30	D29	D28	D27	D26	D25	D24	DESCRIPTION
–	–	–	–	–	–	–	–	Unused
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**DESCRIPTION**
0	0	0	0	0	0	0	1	Audio DSP core coefficient memory select
0	0	0	0	0	0	1	0	Audio DSP core data memory select
0	0	0	0	0	0	1	1	Reserved
0	0	0	0	0	1	0	0	Microprocessor internal data memory select
0	0	0	0	0	1	0	1	Microprocessor external data memory select
0	0	0	0	0	1	1	0	SFR select
0	0	0	0	0	1	1	1	Microprocessor program RAM select
0	0	0	0	1	0	0	0	Audio DSP core program RAM select
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**DESCRIPTION**
A0	A1	A2	A3	A4	A5	A6	A7	Memory address
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**DESCRIPTION**
A8	A9	A10	A11	A12	A13	A14	A15	Memory address

Table 7-6. Data Register (Peek and Poke) (0x07)

D63	D62	D61	D60	D59	D58	D57	D56	DESCRIPTION
D63	D62	D61	D60	D59	D58	D57	D56	Data to be written or read
D55	**D54**	**D53**	**D52**	**D51**	**D50**	**D49**	**D48**	**DESCRIPTION**
D55	D54	D53	D52	D51	D50	D49	D48	Data to be written or read
D47	**D46**	**D45**	**D44**	**D43**	**D42**	**D41**	**D40**	**DESCRIPTION**
D47	D46	D45	D44	D43	D42	D41	D40	Data to be written or read
D39	**D38**	**D37**	**D36**	**D35**	**D34**	**D33**	**D32**	**DESCRIPTION**
D39	D38	D37	D36	D35	D34	D33	D32	Data to be written or read
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**DESCRIPTION**
D31	D30	D29	D28	D27	D25	D26	D25	Data to be written or read
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**DESCRIPTION**
D23	D22	D21	D20	D19	D18	D17	D16	Data to be written or read
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**DESCRIPTION**
D15	D14	D13	D12	D11	D10	D9	D8	Data to be written or read
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**DESCRIPTION**
D7	D6	D5	D4	D3	D2	D1	D0	Data to be written or read

8 Electrical Specifications

8.1 Absolute Maximum Ratings Over Operating Temperature Range (unless otherwise noted)(1)

	Supply voltage range, DVDD		–0.5 V to 3.8 V
	Supply voltage, AVDD		–0.5 V to 3.8 V
V_I	Input voltage range	3.3-V TTL	–0.5 V to DVDD + 0.5 V
		1.8 V LVCMOS (XTLI)	–0.5 V to 2.3 V
V_O	Output voltage range	3.3 V TTL	–0.5 V to DVDD + 0.5 V
		1.8 V LVCMOS (XTLO)	–0.5 V to 2.3V(2)
I_{IK}	Input clamp current (V_I < 0 or V_I > DVDD		±20 µA
I_{OK}	Output clamp current (V_O < 0 or V_O > DVDD)		±20 µA
T_A	TAS3108 operating free-air temperature		0°C to 70°C
	TAS3108IA operating free-air temperature		–40°C to 105°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pin XTALO is the only TAS3108/TAS3108IA output that is derived from the internal 1.8-V logic supply. The absolute maximum rating listed is for reference; only a crystal should be connected to XTALO.

8.2 Package Dissipation Ratings (TAS3108/TAS3108IA)

PACKAGE			TAS3108IA(1)		TAS3108(2)	
TYPE	PIN COUNT	DESIGNATOR	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TSSOP	38	DCP	27.41	0.72	52.93	0.72

(1) Use 2 oz. trace and thermal pad with solder
(2) Use 2 oz. trace and thermal pad without solder

See *Application Information*, Section 9, for PCB recommendations for TAS3108IA applications.

8.3 Recommended Operating Conditions (TAS3108/TAS3108IA)

			MIN	NOM	MAX	UNIT
	Digital supply voltage, DVDD		3	3.3	3.6	V
V_{IH}	High-level input voltage	3.3 V TTL	2			V
		1.8 V LVCMOS (XTL_IN)	1.2			
V_{IL}	Low-level input voltage	3.3 V TTL			0.8	V
		1.8 V LVCMOS (XTL_IN)			0.5	
T_A	Operating ambient air temperature	TAS3108	0	25	70	°C
		TAS3108IA	–40	25	105	
T_J	Operating junction temperature	TAS3108	0		105	°C
		TAS3108IA	–40		125	

8.4 Electrical Characteristics (TAS3108/TAS3108IA)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	3.3-V TTL	I_{OH} = –4 mA	2.4			V
		1.8-V LVCMOS (XTL_OUT)	I_{OH} = –0.55 mA	1.44			
V_{OL}	Low-level output voltage	3.3-V TTL	I_{OL} = 4 mA			0.5	V
		1.8-V LVCMOS (XTL_OUT)	I_{OL} = 0.75 mA			0.4	
I_{OZ}	High-impedance output current	3.3-V TTL	$V_I = V_{IL}$			±20	µA
I_{IL}	Low-level input current	3.3-V TTL	$V_I = V_{IL}$			±1	µA
		1.8-V LVCMOS (XTL_IN)	$V_I = V_{IL}$			±1	
I_{IH}	High-level input current	3.3-V TTL	$V_I = V_{IH}$			±1	µA
		1.8-V LVCMOS (XTL_IN)	$V_I = V_{IH}$			±1	
I_{DVDD}	Digital supply current	Normal operation	MCLKI = 24.576 MHz, LRCLK = 192 kHz		110		mA
			MCLKI = 12.288 MHz, LRCLK = 48 kHz		100		
			MCLKI = 8.192 MHz, LRCLK = 32 kHz		70		
		Power down enabled	LRCLK, SCLK, MCLKI running		16		
I_{A_DVDD}	Analog supply current	Normal operation	MCLKI = 24.576 MHz, LRCLK = 192 kHz		3		mA
		Power down enabled	LRCLK, SCLK, MCLKI running		2		mA

8.5 Timing Characteristics

The following sections describe the timing characteristics of the TAS3108/TAS3108IA.

8.5.1 Master Clock Signals (TAS3108/TAS3108IA)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(XTALI)}$	Frequency, XTALI (1/ $t_{c(1)}$)		See (1)	6 (2)		20 (2)	MHz
$t_{c(1)}$	Cycle time, XTALI			50 (2)		166 (2)	ns
$f_{(MCLKI)}$	Frequency, MCLKI (1/ $t_{c(2)}$)			6 (2)		25	MHz
$t_{w(MCLKI)}$	Pulse duration, MCLKI high		See (3)	0.4 $t_{c(2)}$	0.5 $t_{c(2)}$	0.6 $t_{c(2)}$	ns
	MCLKI jitter					±5 (2)	ns
$f_{(MCLKO)}$	Frequency, MCLKO (1/ $t_{c(3)}$)			6 (2)		25 (2)	MHz
$t_{r(MCLKO)}$	Rise time, MCLKO		C_L = 30 pF			15 (2)	ns
$t_{f(MCLKO)}$	Fall time, MCLKO		C_L = 30 pF			15 (2)	ns
$t_{w(MCLKO)}$	Pulse duration, MCLKO high		See (4)		H_{MCLKO}		ns
	MCLKO jitter	XTALI master clock source			80		ps
		MCLKI master clock source	See (5)				ps
$t_{d(MI-MO)}$	Delay time, MCLKI rising edge to MCLKO rising edge	MCLKO = MCLKI	See (6)			20 (2)	ns
		MCLKO < MCLKI	See (6) (7)			20 (2)	ns

(1) Duty cycle is 50/50.
(2) This measurement is specified by design.
(3) Period of MCLKI = T_{MCLKI} = 1 / f_{MCLKI}
(4) H_{MCLKO} = 1/(2 × MCLKO). MCLKO has the same duty cycle as MCLKI when MCLKO = MCLKI. When MCLKO = 0.5 MCLKI or 0.25 MCLKI, the duty cycle of MCLKO is typically 50%.
(5) When MCLKO is derived from MCLKI, MCLKO jitter = MCLKI jitter
(6) Only applies when MCLKI is selected as master source clock
(7) Also applies to MCLKO falling edge when MCLKO = MCLKI/2 or MCLKI/4.

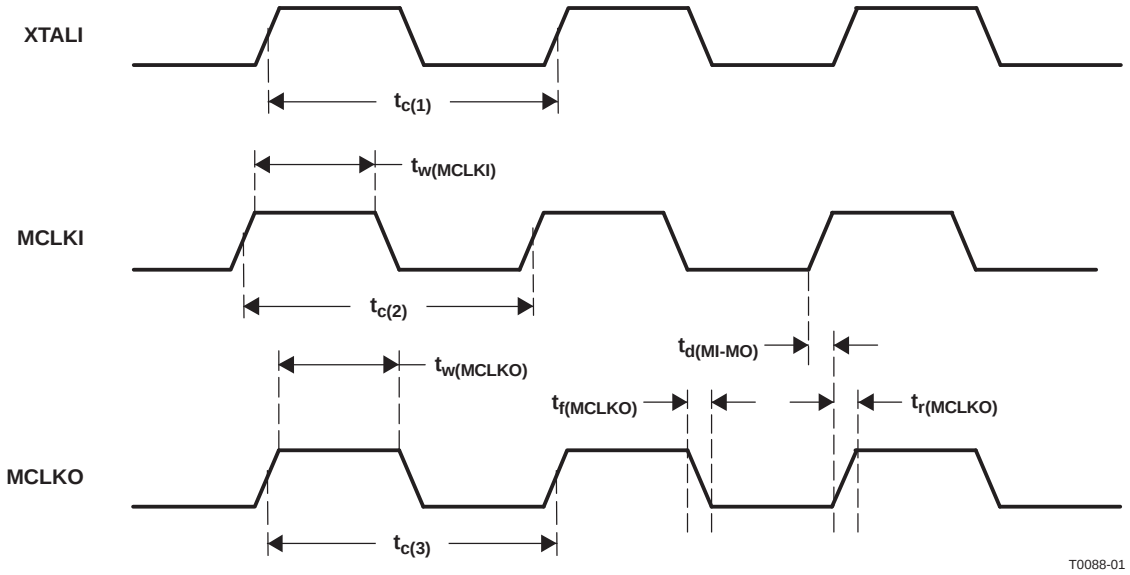


Figure 8-1. Master Clock Signal Timing Waveforms

8.5.2 Serial Audio Port Slave Mode Signals (TAS3108/TAS3108IA)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LRCLK}	Frequency, LRCLK (f_S)		32 (1)		192 (1)	kHz
$t_{w(SCLKIN)}$	Pulse duration, SCLKIN high	See (2)	0.4 $t_{c(SCLKIN)}$ (1)	0.5 $t_{c(SCLKIN)}$	0.6 $t_{c(SCLKIN)}$ (1)	ns
f_{SCLKIN}	Frequency, SCLKIN	See (3)	64 f_S (1)		25 (1)	MHz
t_{pd1}	Propagation delay, SCLKIN falling edge to SDOUT				15 (1)	ns
t_{su1}	Setup time, LRCLK to SCLKIN rising edge		10 (1)			ns
t_{h1}	Hold time, LRCLK from SCLKIN rising edge		0.5 $t_{c(SCLKIN)}$ (1)			ns
t_{su2}	Setup time, SDIN to SCLKIN rising edge		10 (1)			ns
t_{h2}	Hold time, SDIN from SCLKIN rising edge		10 (1)			ns
t_{pd2}	Propagation delay, SCLKIN falling edge to SCLKOUT2 falling edge				17 (1)	ns

(1) This measurement is specified by design.
(2) Period of SCLKIN = $T_{SCLKIN} = 1/f_{SCLKIN}$
(3) Duty cycle is 50/50.

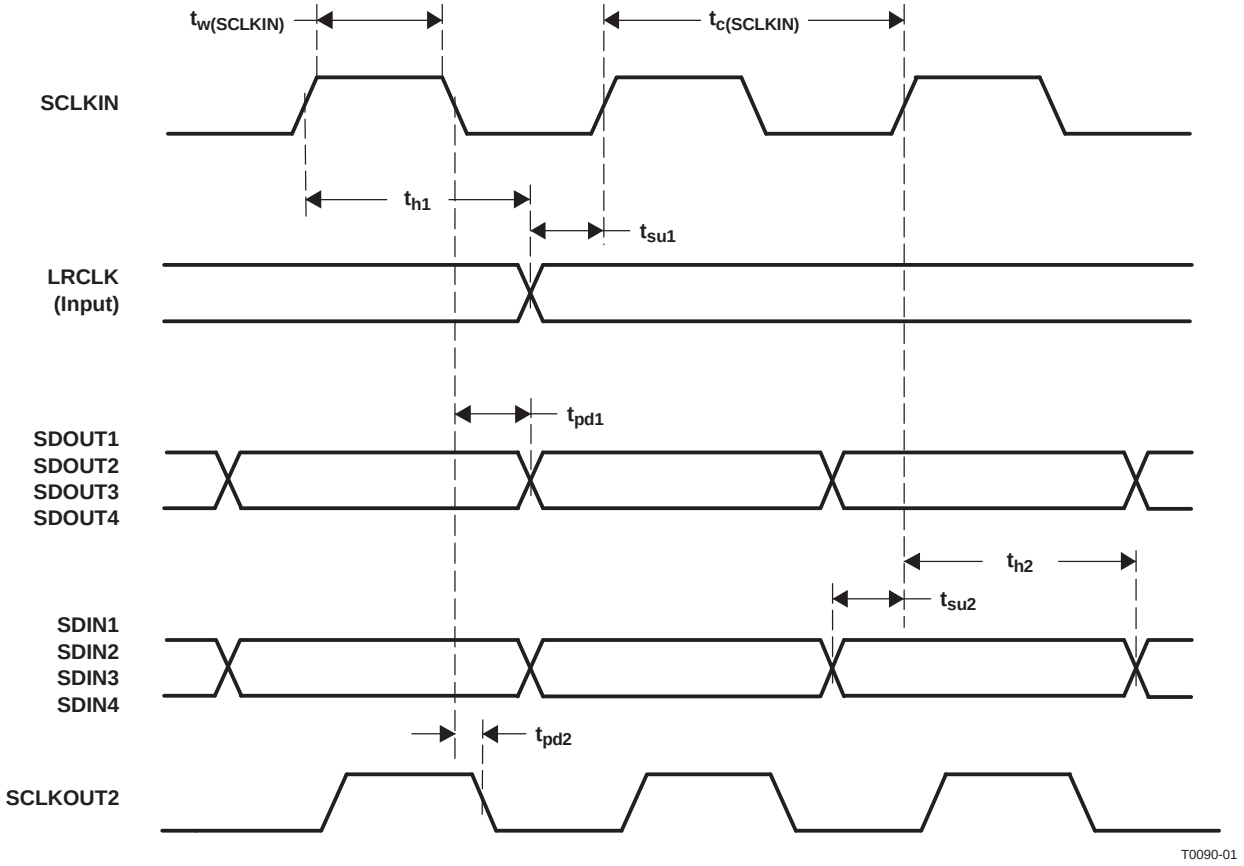


Figure 8-2. Serial Audio Port Slave Mode Timing Waveforms

8.5.3 Serial Audio Port Master Mode Signals (TAS3108/TAS3108IA)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LRCLK)}$	Frequency LRCLK	C_L = 30 pF	32 (1)		192 (1)	kHz
$t_{r(LRCLK)}$	Rise time, LRCLK (2)	C_L = 30 pF			12 (1)	ns
$t_{f(LRCLK)}$	Fall time, LRCLK (2)	Duty cycle is 50/50.			12 (1)	ns
$f_{(SCLKOUT)}$	Frequency, SCLKOUT1/SCLKOUT2	C_L = 30 pF	64 f_S (1)		25 (1)	MHz
$t_{r(SCLKOUT)}$	Rise time, SCLKOUT1/SCLKOUT2	C_L = 30 pF			20 (1)	ns
$t_{f(SCLKOUT)}$	Fall time, SCLKOUT1/SCLKOUT2	C_L = 30 pF			20 (1)	ns
$t_{pd1(SCLKOUT1)}$	Propagation delay, SCLKOUT1 falling edge to LRCLK edge				4 (1)	ns
$t_{pd1(SCLKOUT2)}$	Propagation delay, SCLKOUT2 falling edge to LRCLK edge				4 (1)	ns
t_{pd2}	Propagation delay, SCLKOUT2 falling edge to SDOUT				4 (1)	ns
t_{su}	Setup time, SDIN to SCLKOUT1 rising edge		20 (1)			ns
t_h	Hold time, SDIN from SCLKOUT1 rising edge		23 (1)			ns
$t_{(SKEW)}$	Skew time, SCLKOUT1 to SCLKOUT2				3 (1)	ns

(1) This measurement in specified by design.
(2) Rise time and fall time measured from 20% to 80% of maximum height of waveform.

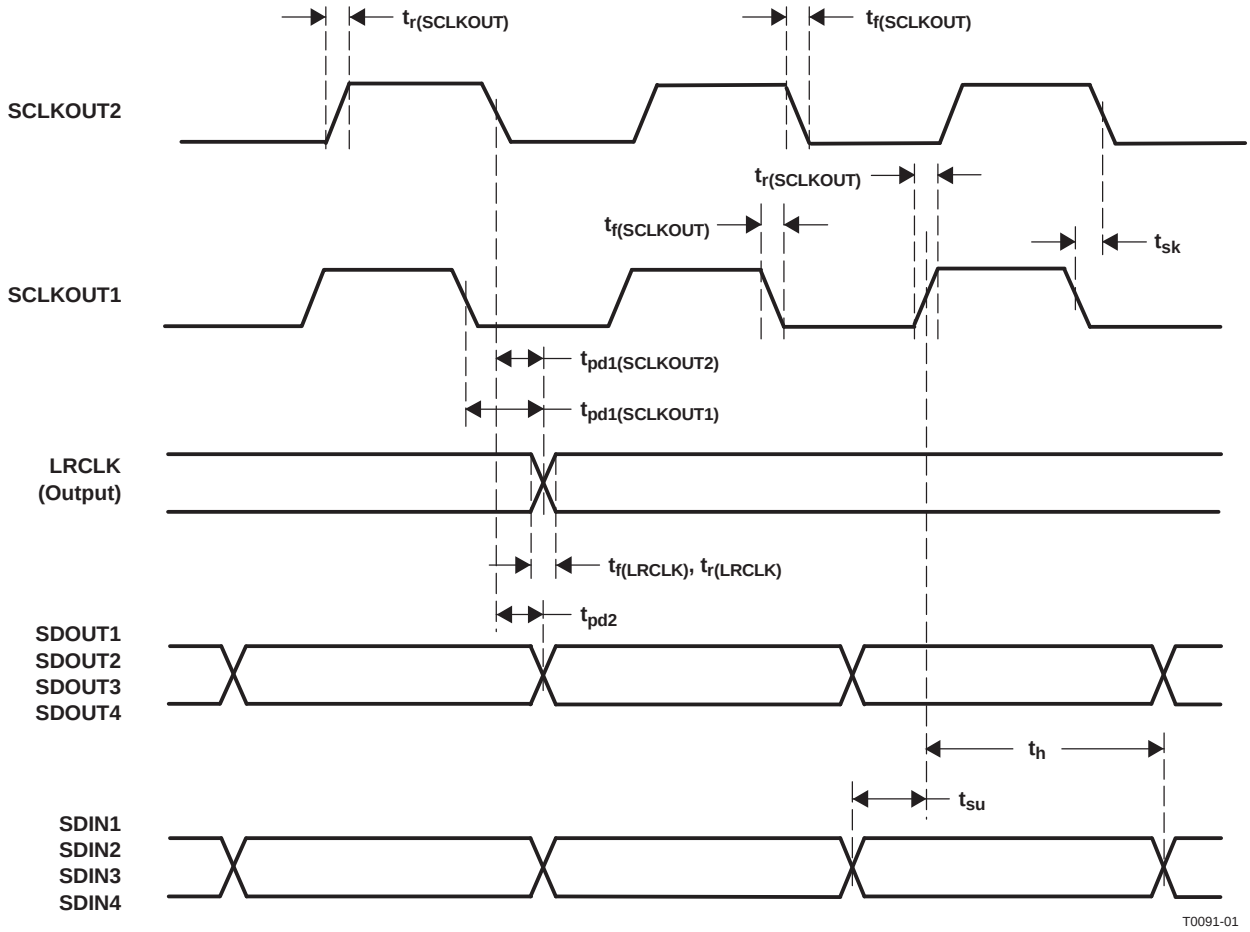


Figure 8-3. TAS3108/TAS3108IA Serial Audio Port Master Mode Timing Waveforms

8.5.4 Pin-Related Characteristics of the SDA and SCL I/O Stages for F/S-Mode I²C-Bus Devices

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
V_{IL}	LOW-level input voltage		–0.5 (1)	0.8	–0.5 (1)	0.8	V
V_{IH}	HIGH-level input voltage		2		2		V
V_{hys}	Hysteresis of inputs		N/A	N/A	0.05 V_{DD} (1)		V
V_{OL1}	LOW-level output voltage (open drain or open collector)	3-mA sink current			0	0.4 (1)	V
t_{of}	Output fall time from V_{IHmin} to $_{VILmax}$	Bus capacitance from 10 pF to 400 pF		250 (1)	7 + 0.1 C_b (2)(1)	250 (1)	ns
I_I	Input current, each I/O pin		–10	10	–10 (3)	10 (3)	µA
$t_{SP(SCL)}$	SCL pulse duration of spikes that must be suppressed by the input filter		N/A	N/A	14 (4)(1)		ns
$t_{SP(SDA)}$	SDA pulse duration of spikes that must be suppressed by the input filter		N/A	N/A	22 (4)(1)		ns
C_I	Capacitance, each I/O pin			10 (1)		10 (1)	pF

(1) This measurement in specified by design.
(2) C_b = capacitance of one bus line in pF. The output fall time is faster than the standard I²C specification.
(3) The I/O pins of fast-mode devices must not obstruct the SDA and SDL lines if V_{DD} is switched off.
(4) These values are valid at the 135-MHz DSP clock rate. If DSP clock is reduced by one half, the t_{SP} doubles.

NOTE

SDA does not have the standard I²C specification 300-ns internal hold time. SDA must be valid by the rising and falling edges of SCL.

8.5.5 Bus-Related Characteristics of the SDA and SCL I/O Stages for F/S-Mode I²C-Bus Devices

All values are referred to V_{IHmin} and V_{ILmax} (see Section 8.5.4).

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency (1)		0 (1)	100	0 (1)	400 (2)	kHz
t_{HD-STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.		4 (1)		0.6 (1)		µs
t_{LOW}	LOW period of the SCL clock		4.7 (1)		1.3 (1)		µs
t_{HIGH}	HIGH period of the SCL clock		4 (1)		0.6 (1)		µs
t_{SU-STA}	Setup time for repeated START		4.7 (1)		0.6 (1)		µs
t_{SU-DAT}	Data setup time		250 (1)		100 (1)		ns
t_{HD-DAT}	Data hold time (3)(4)		0 (1)	3.45 (1)	0 (1)	0.9 (1)	µs
t_r	Rise time of both SDA and SCL signals			1000 (1)	20 + 0.1 C_b (5)(1)	300 (1)	ns
t_f	Fall time of both SDA and SCL			300 (1)	20 + 0.1 C_b (5)(1)	300 (1)	ns
t_{SU-STO}	Setup time for STOP condition		4 (1)		0.6 (1)		µs
t_{BUF}	Bus free time between a STOP and START condition		4.7 (1)		1.3 (1)		µs
C_b	Capacitive load for each bus line			400 (1)		400 (1)	pF
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)		0.1 V_{DVDD} (1)		0.1 V_{DVDD} (1)		V
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)		0.2 V_{DVDD} (1)		0.2 V_{DVDD} (1)		V

(1) This measurement is specified by design.
(2) In master mode, the maximum speed is 375 kHz.
(3) Note that SDA does not have the standard I²C specification 300-ns internal hold time. SDA must be valid by the rising and falling edges of SCL. TI recommends that a 2-kΩ pullup resistor be used to avoid potential timing issues.
(4) A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU-DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r-max} + t_{SU-DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I²C bus specification) before the SCL line is released.
(5) C_b = total capacitance of one bus line in pF.

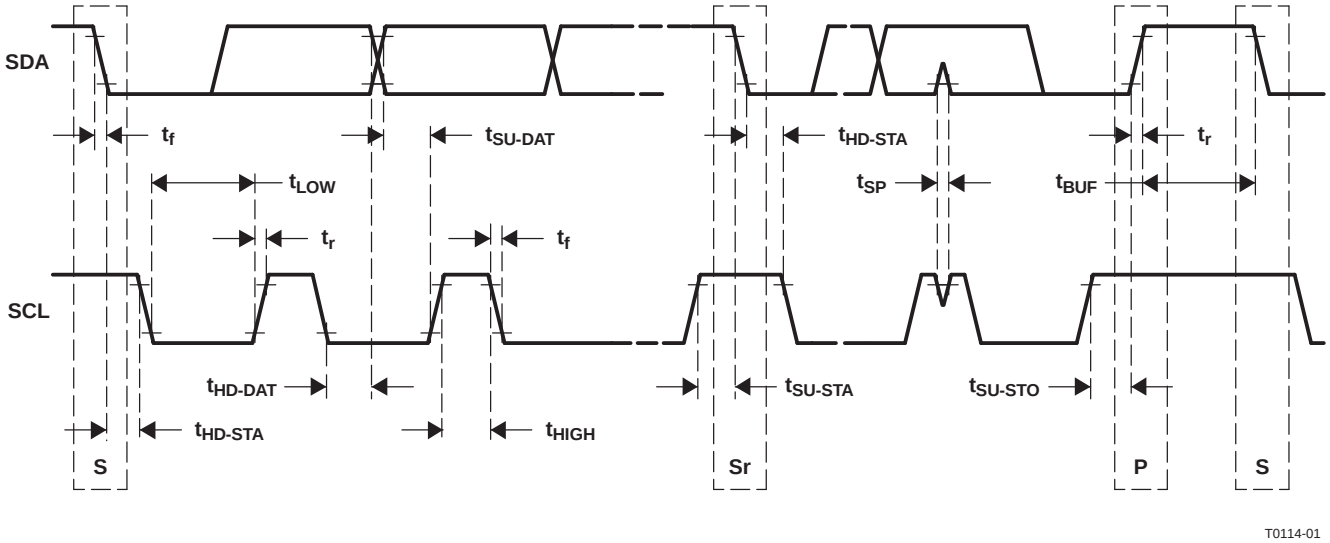


Figure 8-4. Start and Stop Conditions Timing Waveforms

8.5.5.1 Recommended I²C Pullup Resistors

It is recommended that the I²C pullup resistors R_P be 4.7 kΩ (see Figure 8-5). If a series resistor is in the circuit (see Figure 8-6), then the series resistor R_S should be less than or equal to 300 Ω.

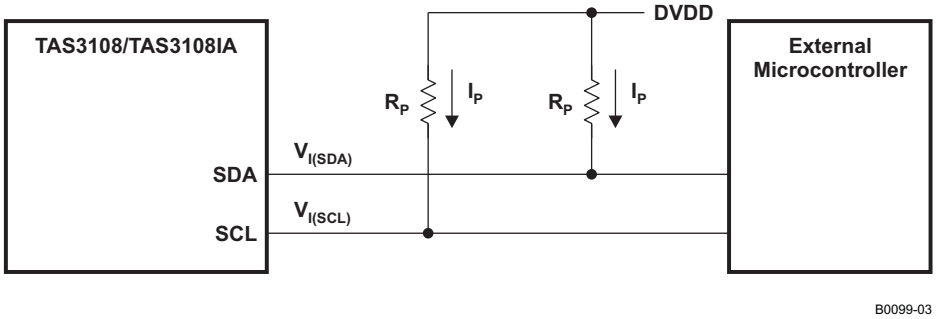
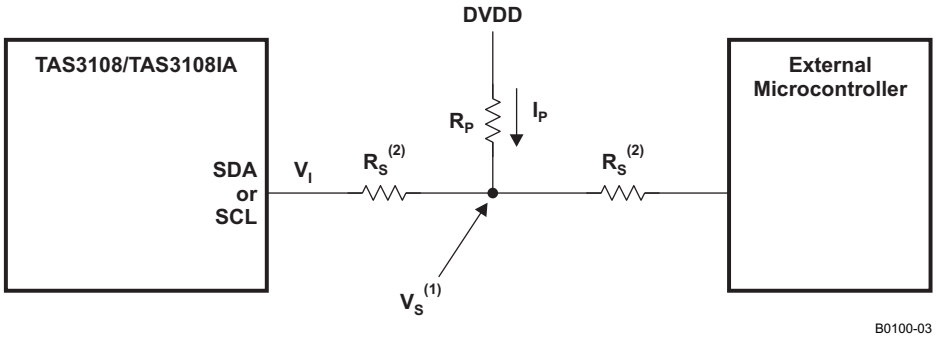


Figure 8-5. I²C Pullup Circuit (With No Series Resistor)



(1) V_S = DVDD × $R_S/_S$ = R_P). When driven low, V_S << V_{IL} requirements.

(2) $R_S \leq 300\ \Omega$

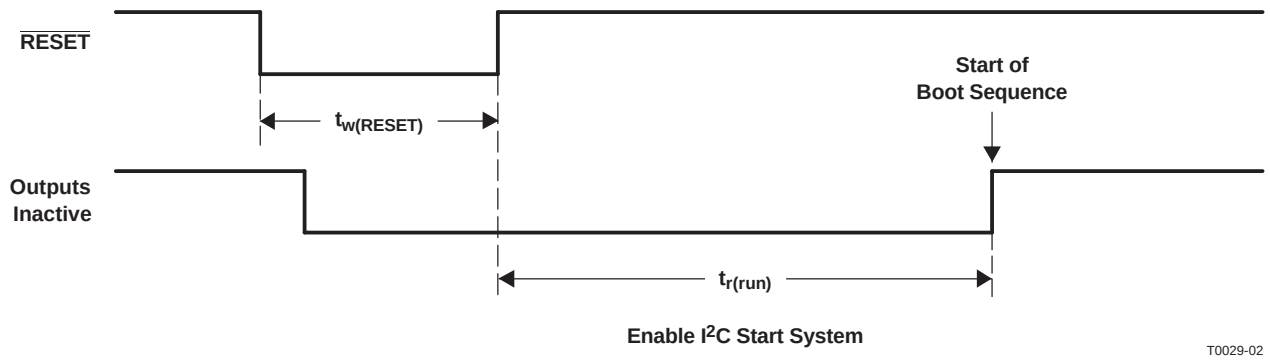
Figure 8-6. I²C Pullup Circuit (With Series Resistor)

8.5.6 Reset Timing (TAS3108/TAS3108IA)

control signal parameters over recommended operating conditions; these measurements are specified by design (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(RESET)}$	Pulse duration, RESET active		10(1)		ns
$t_{r(run)}$	Time to enable I²C	PLL0 = PLL1 = MICROCLK_DIV = 0	10(1)		ms

(1) This measurement is specified by design.



NOTE: MCLK input = 12.288 MHz

Figure 8-7. Reset Timing

9 Application Information

9.1 Schematics

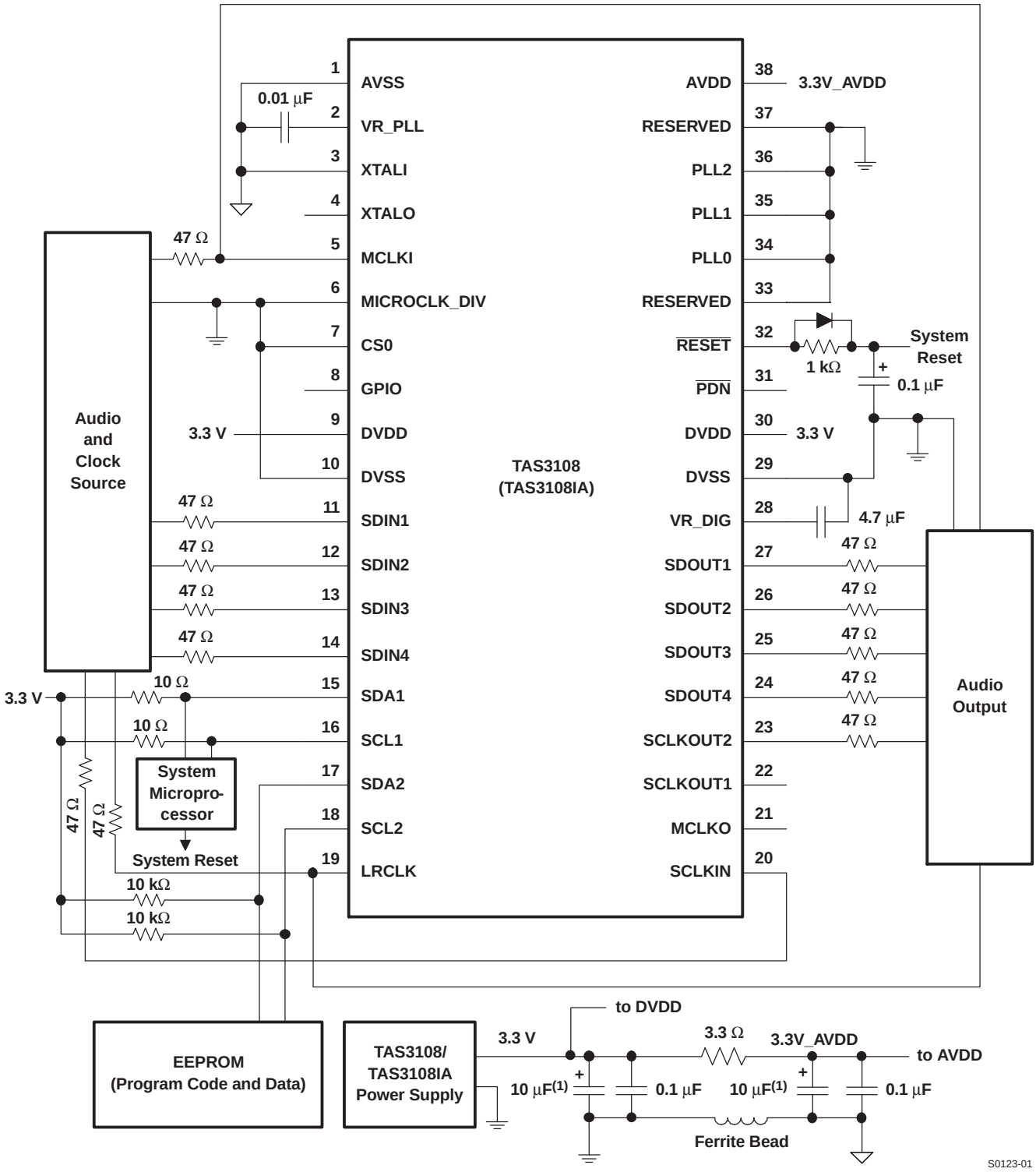
Figure 9-1 shows a typical TAS3108/TAS3108IA application. In this application, the following conditions apply:

- TAS3108/TAS3108IA is in clock-slave mode. The audio (SDIN1, SDIN2, SDIN3, SDIN4) and clock source (MCLKI) are external.
- MCLKI = 12.288 MHz
- Because MCLKI is sourced externally, the TAS3108/TAS3108IA crystal interface is not used. MCLKI and XTLI are logically ORed together, meaning that when the MCLKI pin is used, the XTALI pin must be grounded.
- I^2C register 0x00 contains the default settings which means:
  - Audio data word size is 24-bit input and 24-bit output.
  - Serial data format is 2 channel, I^2S for input and output.
  - I^2C data transfer is approximately 400 kbps for both master and slave I^2C interfaces.
  - PLL0 = PLL1 = PLL2 = 0 means that f_{DSPCLK} is 11 × MCLKI = 135.2 MHz and that f_{I2CSCL} = 375 kHz.
  - Sample frequency (f_S) is 48 kHz, which requires that f_{LRCLK} = 48 kHz and f_{SCLKIN} = 3.072 MHz.
- Application code and data are loaded from an external EEPROM using the master I^2C interface.
- Application commands come from the system microprocessor to the TAS3108/TAS3108IA using the slave I^2C interface.

Good design practice requires isolation between the digital and analog power as shown. Power-supply capacitors of 10 µF and 0.1 µF should be placed near the power-supply pins AVDD (AVSS) and DVDD (DVSS).

The TAS3108/TAS3108IA reset needs external glitch protection. Also, reset going HIGH should be delayed until TAS3108/TAS3108IA internal power is good (~200 µs). This is provided by the 1-kΩ resistor, 1-µF capacitor, and diode placed near the $\overline{\text{RESET}}$ pin.

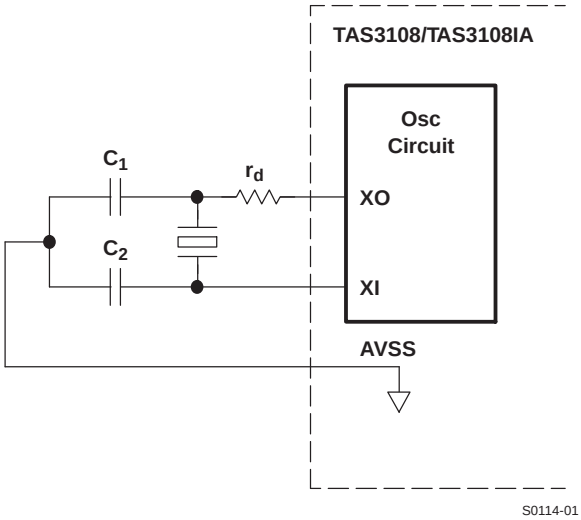
It is recommended that a 4.7-µF capacitor (fast ceramic type) be placed near pin 28 (VR_DIG). This pin must not be used to source external components.



(1) Capacitors should be placed as close as possible to the power-supply pins.

Figure 9-1. Typical Application Diagram

9.2 Recommended Oscillator Circuit



- MCLKI and XTLI are logically ORed together, meaning that when the XTALI pin is used, the MCLKI pin must be grounded.
- Crystal type = Parallel-mode, fundamental-mode crystal
- r_d = Drive-level control resistor – vendor specified
- C_L = Crystal load capacitance (capacitance of circuitry between the two terminals of the crystal)
- $C_L = (C_1 \times C_2)/C_1 + C_2) + C_S$ (where C_S = board stray capacitance, ~2 pF)

9.3 Recommended PCB Design for TAS3108IA Applications

Automotive applications require that the TAS3108IA operates properly while in an ambient temperature range of –40° C to 105°C. Under the high-temperature condition of 105°C ambient, the TAS3108IA thermal pad must be soldered to a copper area on the PCB designed for thermal relief.

High-temperature applications also require that the application be built on a high-K dielectric PCB.

High-K dielectric PCB requirements for using TAS3108IA with soldered thermal pad:

- 0.062 in thick
- Minimum 3-in × 3-in PCB
- 2-oz copper traces located on top of the board (0,071 mm thick)
- Copper area located on the top and bottom of the PCB for soldering
- Power and ground planes, 1-oz. copper (0,036 mm thick)
- Thermal vias, 0.3-mm diameter, 1.5-mm pitch
- Thermal isolation of power plane

  If the target application limits the ambient temperature to 0°C to 70°C (standard commercial temperature range), the thermal pad does not need to be soldered to the PCB.

For more information, see *PowerPAD™ Thermally Enhanced Package* (SLMA002) and *PowerPAD™ Made Easy* (SLMA004).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS3108DCP	Active	Production	HTSSOP (DCP) | 38	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS3108
TAS3108DCP.A	Active	Production	HTSSOP (DCP) | 38	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS3108
TAS3108DCPR	Active	Production	HTSSOP (DCP) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS3108
TAS3108DCPR.A	Active	Production	HTSSOP (DCP) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS3108
TAS3108IADCP	Active	Production	HTSSOP (DCP) | 38	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	TAS3108IA
TAS3108IADCP.A	Active	Production	HTSSOP (DCP) | 38	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	TAS3108IA
TAS3108IADCPR	Active	Production	HTSSOP (DCP) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 0	TAS3108IA
TAS3108IADCPR.A	Active	Production	HTSSOP (DCP) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 0	TAS3108IA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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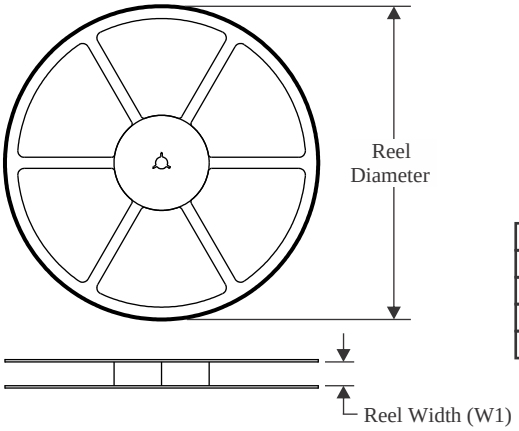
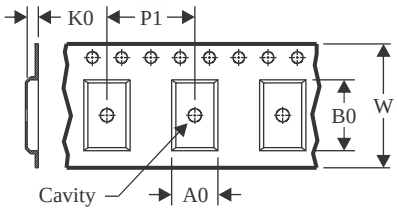
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

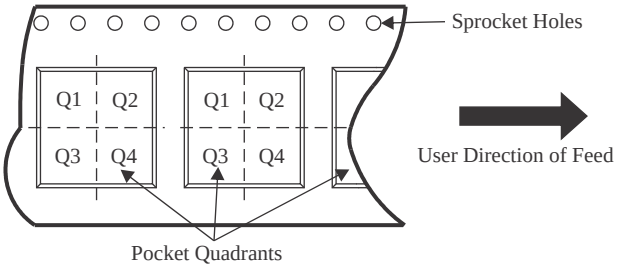


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

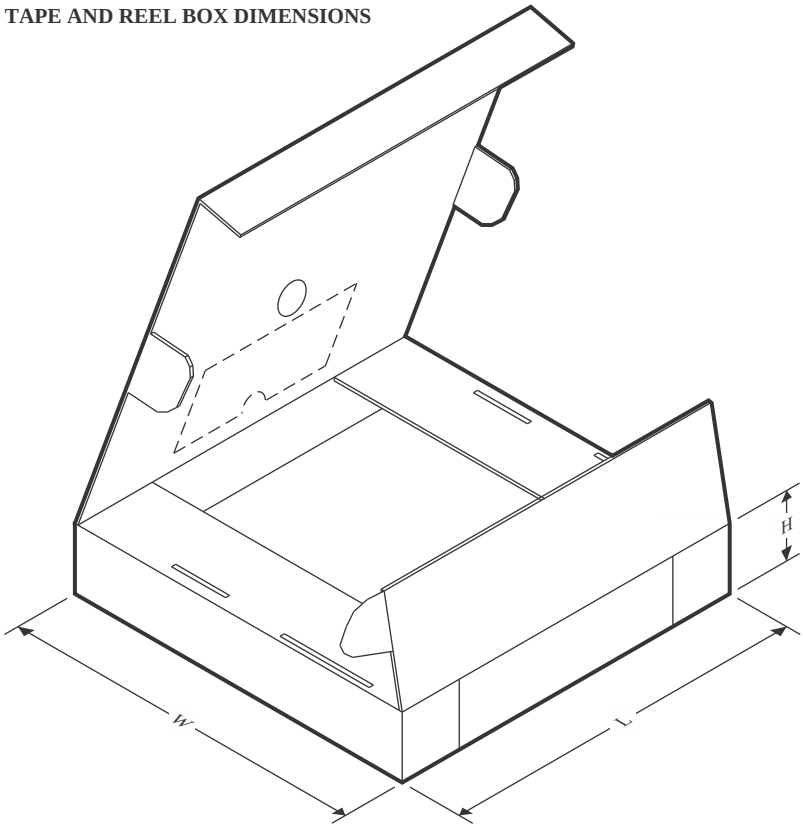
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS3108DCPR	HTSSOP	DCP	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TAS3108IADCPR	HTSSOP	DCP	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

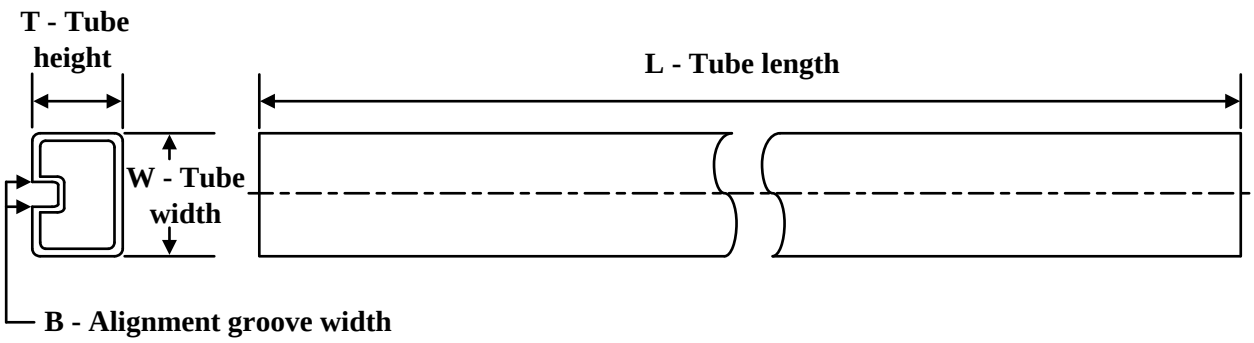
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS3108DCPR	HTSSOP	DCP	38	2000	367.0	367.0	38.0
TAS3108IADCPR	HTSSOP	DCP	38	2000	367.0	367.0	38.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TAS3108DCP	DCP	HTSSOP	38	50	530	10.2	3600	3.5
TAS3108DCP.A	DCP	HTSSOP	38	50	530	10.2	3600	3.5
TAS3108IADCP	DCP	HTSSOP	38	50	530	10.2	3600	3.5
TAS3108IADCP.A	DCP	HTSSOP	38	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

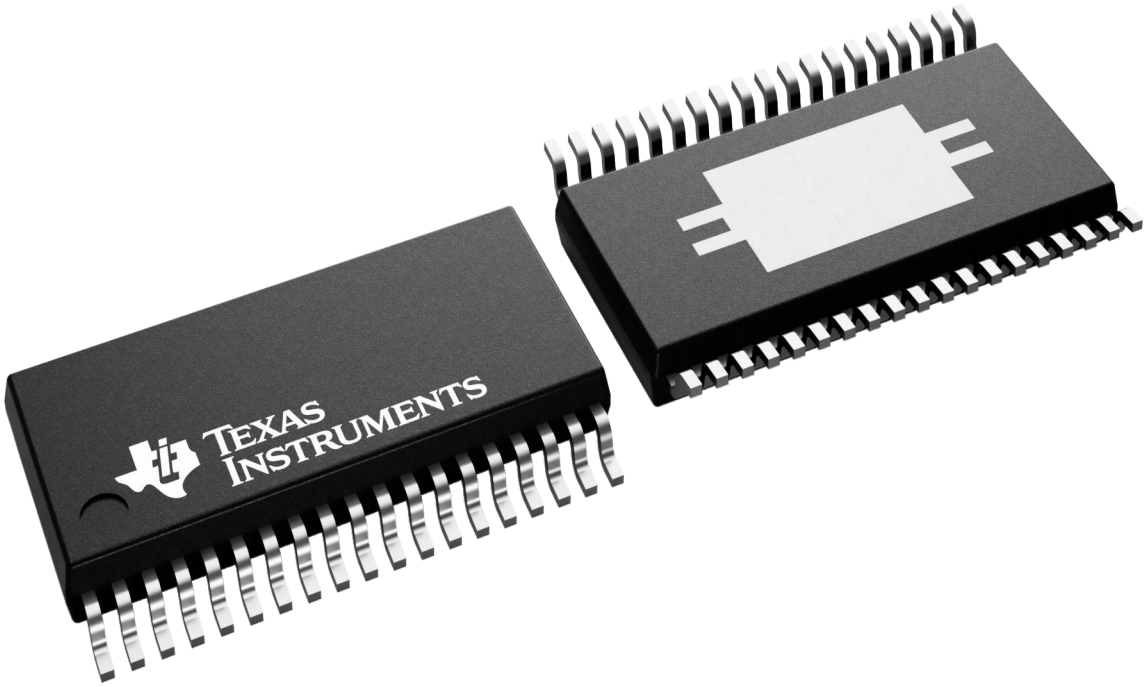
DCP 38

PowerPAD TSSOP - 1.2 mm max height

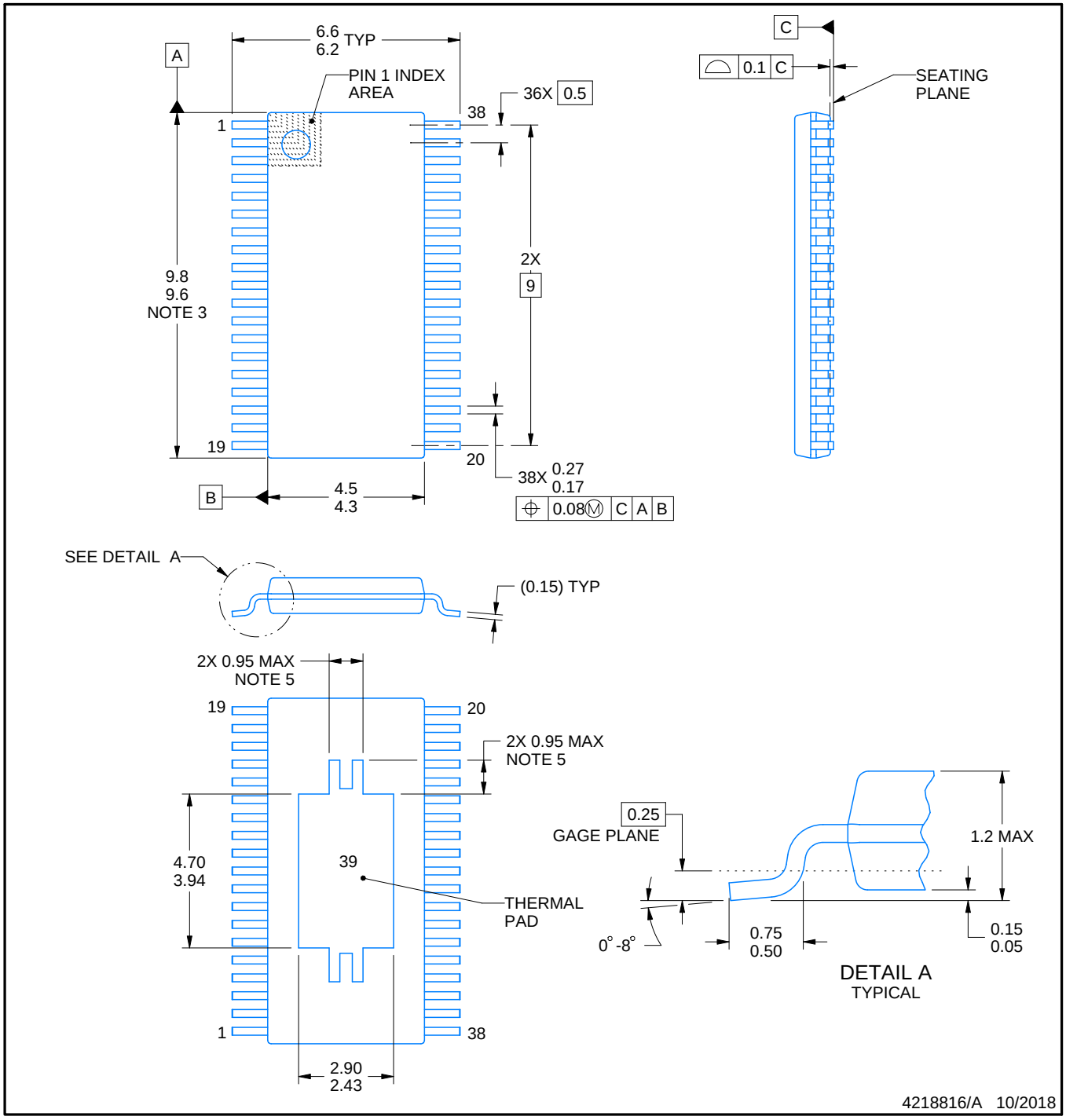
4.4 x 9.7, 0.5 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



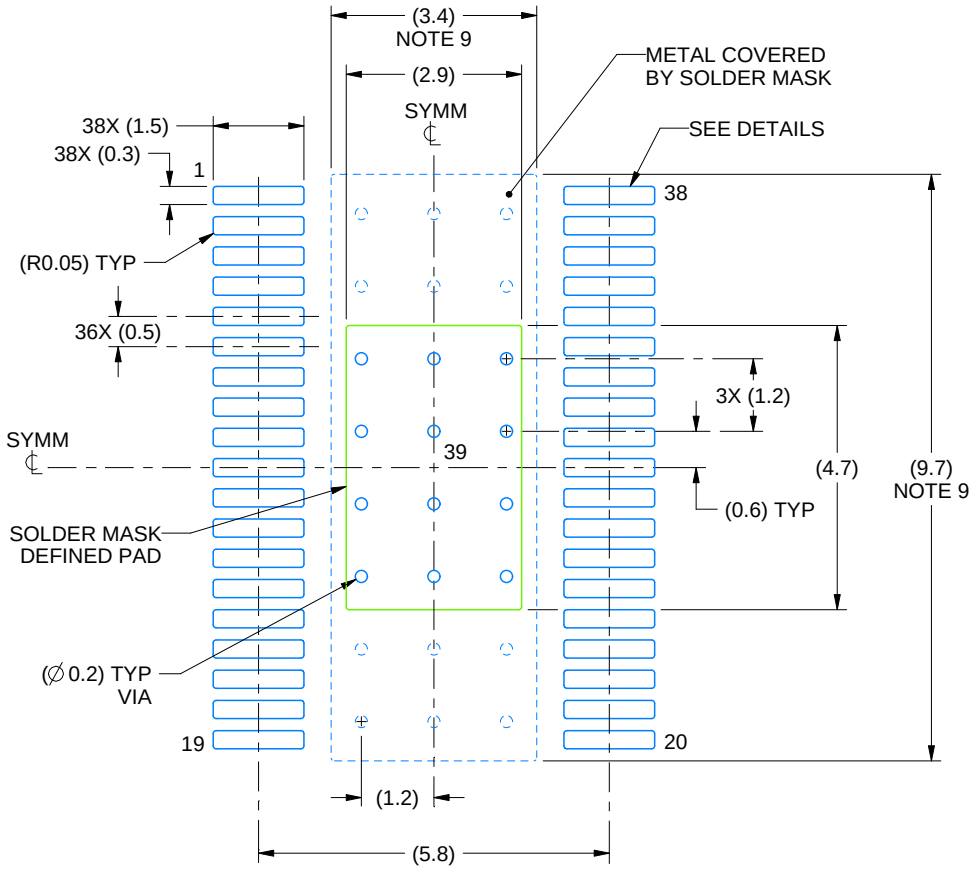
4224560/B



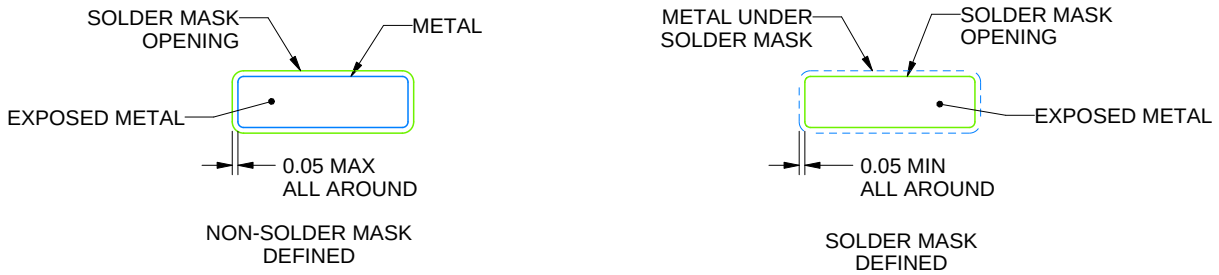
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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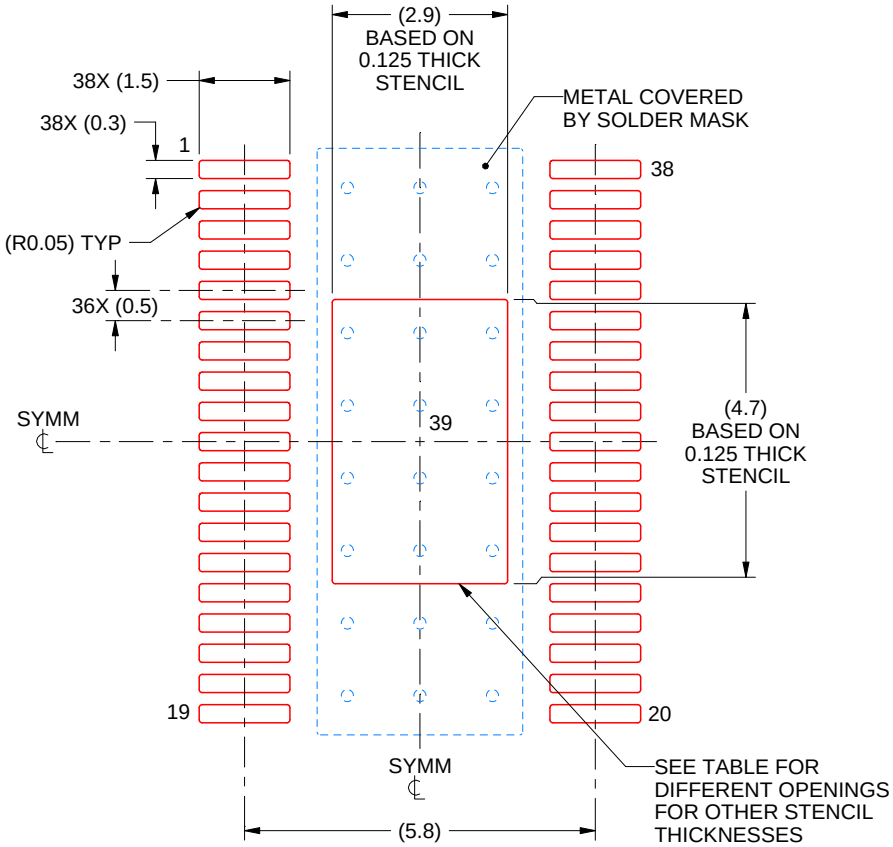
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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