# DAC121S101-SEP 12-Bit, Micro Power, RRO Digital-to-Analog Converter

## 1 Features

- Radiation tolerance:
  - Total ionizing dose (TID): 30krad (Si)
  - Single-event latch-up (SEL): 43MeV-cm$^2$/mg
  - Single-event functional interrupt (SEFI): 43MeV-cm$^2$/mg
- Space-enhanced plastic (space EP):
  - Outgassing test performed per ASTM E595
  - Vendor item drawing (VID) V62/24641
  - Supports defense and aerospace application temperature range: –55°C to +125°C
  - Controlled baseline
  - One assembly and test site
  - One fabrication site
  - Extended product life cycle
  - Product traceability
- Specified monotonicity
- Low-power operation
- Rail-to-rail voltage output
- Power-on reset to zero-scale output
- Wide power-supply range of 2.7V to 5.5V
- Small package:
  - 8-pin VSSOP (3mm × 3mm)
- Power-down feature
- Key specifications:
  - 12-bit resolution
  - DNL: −0.15LSB, +0.35LSB (typical)
  - 12µs output settling time (typical)
  - 4mV zero-code error (typical)
  - Full-scale error at −0.07%FSR (typical)

## 2 Applications

- Command and data handling (C and DH)
- Communications payload
- Optical imaging payload
- Radar imaging payload
- Satellite electrical power system (EPS)

## 3 Description

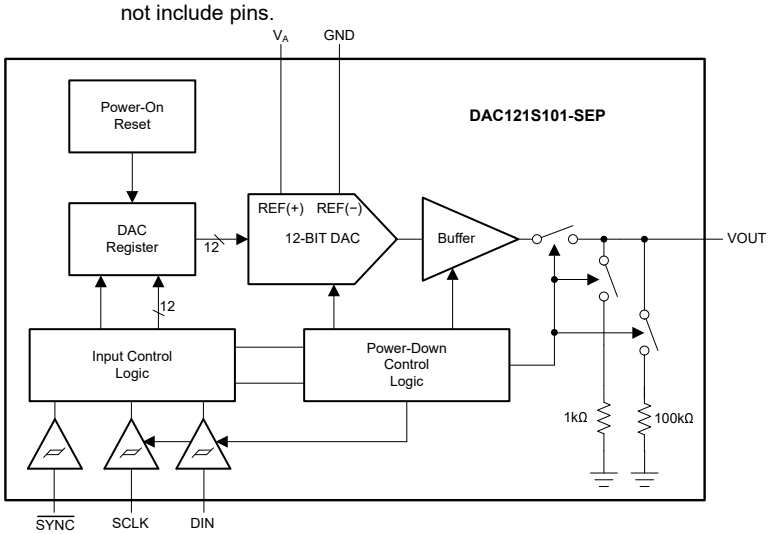
The DAC121S101-SEP device is a full-featured, general-purpose, 12-bit voltage-output digital-to-analog converter (DAC) that can operate from a single 2.7V to 5.5V supply and consumes just 177µA (typical) of current at 3.6V. The on-chip output amplifier allows rail-to-rail output swing and the three wire serial interface operates at clock rates up to 30MHz over the specified supply voltage range and is compatible with standard SPI, QSPI, MICROWIRE and DSP interfaces.

The supply voltage serves as the voltage reference for the DAC121S101-SEP, providing the widest possible output dynamic range. A power-on reset circuit powers up the DAC output to zero volts until there is a valid write to the device. A power-down feature reduces power consumption to less than a microwatt (typical).

**Package Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE(2) |
|---|---|---|
| DAC121S101-SEP | DGK (VSSOP, 8) | 3mm × 3mm |

(1) For more information, see Section 10.
(2) The body size (length × width) is a nominal value and does not include pins.




**Simplified Block Diagram**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Pin Configuration and Functions

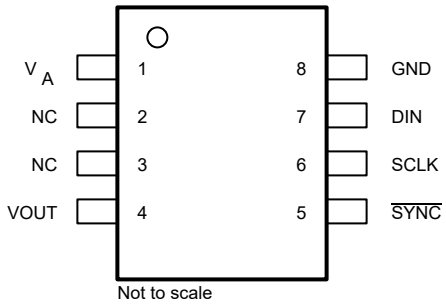


**Figure 4-1. DAC121S101-SEP DGK Package, 8-Pin VSSOP (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | $V_A$ | Power | Power supply and reference input. Decouple to the GND pin. |
| 2 | NC | — | Solder this pin to a pad. |
| 3 | NC | — | Solder this pin to a pad. |
| 4 | VOUT | Output | DAC analog output voltage |
| 5 | $\overline{\text{SYNC}}$ | Input | Frame synchronization input for the data input. When this pin goes low, this pin enables the input shift register and data are transferred on the falling edges of SCLK. The DAC is updated on the 16th clock cycle unless $\overline{\text{SYNC}}$ is brought high before the 16th clock, in which case the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the DAC. |
| 6 | SCLK | Input | Serial clock input. Data are clocked into the input shift register on the falling edges of this pin. |
| 7 | DIN | Input | Serial data input. Data are clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{\text{SYNC}}$. |
| 8 | GND | Ground | Ground reference for all on-chip circuitry. |


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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_A$ | Supply voltage, $V_A$ to GND | –0.3 | 6.5 | V |
| | Voltage on any input pin to GND | –0.3 | $V_A$ + 0.3 | V |
| | Input current at any pin[2] | | 10 | mA |
| | Package input current[2] | | 20 | mA |
| | Power consumption at $T_A$ = 25°C | | See[3] | |
| | Soldering temperature, infrared, 10s[4] | | 235 | °C |
| $T_J$ | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) When the input voltage at any pin exceeds the power supplies (that is, less than GND, or greater than $V_A$), the current at that pin must be limited to 10mA. The 20mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10mA to two.
(3) The absolute maximum junction temperature ($T_{JMAX}$) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_{JMAX}$, the junction-to-ambient thermal resistance ($\theta_{JA}$), and the ambient temperature ($T_A$), and can be calculated using the formula $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (for example, when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions must always be avoided.
(4) See the section entitled *Surface Mount* found in any post 1986 National Semiconductor Linear Data Book for methods of soldering surface mount devices.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | ±2500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2] | ±500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_A$ | Supply voltage to GND | 2.7 | | 5.5 | V |
| | Any input voltage to GND[1] | –0.1 | | ($V_A$ + 0.1) | V |
| $C_L$ | Output load capacitance | 0 | | 1500 | pF |
| $f_{SCLK}$ | SCLK frequency | | | 30 | MHz |
| $T_A$ | Operating ambient temperature | –55 | | 125 | °C |

(1) Errors in the conversion result can occur if any input goes greater tha $V_A$ or less than GND by more than 100mV. For example, if $V_A$ is 2.7VDC, make sure that −100mV ≤ input voltages ≤ +2.8VDC for accurate conversions.

## 5.4 Thermal Information

| THERMAL METRIC[1] | | DAC121S101-SEP DGK (VSSOP) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 240 | °C/W |

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report.*

## 5.5 Electrical Characteristics

all minimum and maximum values at –55°C ≤ $T_A$ ≤ +125°C and all typical values at $T_A$ = 25°C, 2.7V ≤ $V_A$ ≤ 5.5V, DAC output pin (VOUT) loaded with resistive load ($R_L$ = 2kΩ to AGND) and capacitive load ($C_L$ = 200pF to AGND), $f_{SCLK}$ = 30MHz, and input code range: 48d to 4047d (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE** | | | | | | | |
| | Resolution[1] | | | 12 | | | Bits |
| | Monotonicity[1] | | | 12 | | | Bits |
| INL | Integral nonlinearity | | | –11 | ±2.6 | 11 | LSB |
| DNL | Differential nonlinearity | $V_A$ = 2.7V | Minimum | –0.7 | –0.15 | | LSB |
| | | | Maximum | | 0.35 | 1 | |
| | | $V_A$ = 5.5V | Minimum | –0.7 | –0.15 | | |
| | | | Maximum | | 0.25 | 1 | |
| ZE | Zero-code error | $I_{OUT}$ = 0mA | | | 4 | 16 | mV |
| ZCED | Zero-code error drift | | | | –20 | | µV/°C |
| GE | Gain error | All ones loaded to DAC register | | | ±1 | | %FSR |
| TC GE | Gain-error temperature coefficient | $V_A$ = 3V | | | –0.7 | | ppm/°C |
| | | $V_A$ = 5V | | | –1 | | |
| FSE | Full-scale error | $I_{OUT}$ = 0mA | | | –0.07 | –1 | %FSR |
| **OUTPUT** | | | | | | | |
| | Output voltage[1] | | | 0 | | $V_A$ | V |
| ZCO | Zero-code output[1] | $V_A$ = 3V, $I_{OUT}$ = 10µA | | | | 1.8 | mV |
| | | $V_A$ = 3V, $I_{OUT}$ = 100µA | | | | 5 | |
| | | $V_A$ = 5V, $I_{OUT}$ = 10µA | | | | 3.7 | |
| | | $V_A$ = 5V, $I_{OUT}$ = 100µA | | | | 5.4 | |
| FSO | Full-scale output[1] | $V_A$ = 3V, $I_{OUT}$ = 10µA | | | | 2.997 | V |
| | | $V_A$ = 3V, $I_{OUT}$ = 100µA | | | | 2.99 | |
| | | $V_A$ = 5V, $I_{OUT}$ = 10µA | | | | 4.995 | |
| | | $V_A$ = 5V, $I_{OUT}$ = 100µA | | | | 4.992 | |
| $C_L$ | Capacitive load[1] | $R_L$ = ∞ | | | | 1500 | pF |
| $I_{OS}$ | Short-circuit current[1] | $V_A$ = 5V, $V_{OUT}$ = 0V, DAC code = FFFh | | | | –63 | mA |
| | | $V_A$ = 3V, $V_{OUT}$ = 0V, DAC code = FFFh | | | | –50 | |
| | | $V_A$ = 5V, $V_{OUT}$ = 5V, DAC code = 000h | | | | 74 | |
| | | $V_A$ = 3V, $V_{OUT}$ = 3V, DAC code = 000h | | | | 53 | |
| | DC output impedance[1] | | | | | 1.3 | Ω |


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## 5.5 Electrical Characteristics (continued)

all minimum and maximum values at –55°C ≤ $T_A$ ≤ +125°C and all typical values at $T_A$ = 25°C, 2.7V ≤ $V_A$ ≤ 5.5V, DAC output pin (VOUT) loaded with resistive load ($R_L$ = 2kΩ to AGND) and capacitive load ($C_L$ = 200pF to AGND), $f_{SCLK}$ = 30MHz, and input code range: 48d to 4047d (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DYNAMIC PERFORMANCE** | | | | | | | |
| $t_s$ | Output voltage settling time[1] | 400h to C00h code change | $C_L$ ≤ 200pF | | | 10 | µs |
| | | | $C_L$ = 500pF | | 12 | | |
| | | 00Fh to FF0h code change | $C_L$ ≤ 200pF | | 8 | | |
| | | | $C_L$ = 500pF | | 12 | | |
| SR | Output slew rate | | | | 1 | | V/µs |
| | Code change glitch impulse | 800h to 7FFh code change | | | 12 | | nV-s |
| | Digital feedthrough | 800h to 7FFh code change | | | 0.5 | | nV-s |
| $t_{WU}$ | Wake-up time | $V_A$ = 5V | | | 6 | | µs |
| | | $V_A$ = 3V | | | 39 | | |
| **DIGITAL INPUTS** | | | | | | | |
| $I_{IN}$ | Input current[1] | | | −1 | | 1 | µA |
| $V_{IL}$ | Input low voltage[1] | $V_A$ = 5V | | | | 0.8 | V |
| | | $V_A$ = 3V | | | | 0.5 | V |
| $V_{IH}$ | Input high voltage[1] | $V_A$ = 5V | | 2.4 | | | V |
| | | $V_A$ = 3V | | 2.1 | | | V |
| $C_{IN}$ | Pin capacitance[1] | | | | | 3 | pF |
| **POWER** | | | | | | | |
| $I_A$ | Supply current | Output unloaded, normal mode, $f_{SCLK}$ = 30MHz | $V_A$ = 5.5V | | | 312 | µA |
| | | | $V_A$ = 3.6V | | | 217 | |
| | | Output unloaded, normal mode, $f_{SCLK}$ = 20MHz[1] | $V_A$ = 5.5V | | | 279 | |
| | | | $V_A$ = 3.6V | | | 197 | |
| | | Output unloaded, normal mode, $f_{SCLK}$ = 0MHz[1] | $V_A$ = 5.5V | | | 153 | |
| | | | $V_A$ = 3.6V | | | 118 | |
| | | Output unloaded, all PD modes, $f_{SCLK}$ = 30MHz[1] | $V_A$ = 5V | | | 84 | |
| | | | $V_A$ = 3V | | | 42 | |
| | | Output unloaded, all PD modes, $f_{SCLK}$ = 20MHz[1] | $V_A$ = 5V | | | 56 | |
| | | | $V_A$ = 3V | | | 28 | |
| | | Output unloaded, all PD modes, $f_{SCLK}$ = 0MHz | $V_A$ = 5.5V | | 0.15 | 1.4 | |

## 5.5 Electrical Characteristics (continued)

all minimum and maximum values at –55°C ≤ $T_A$ ≤ +125°C and all typical values at $T_A$ = 25°C, 2.7V ≤ $V_A$ ≤ 5.5V, DAC output pin (VOUT) loaded with resistive load ($R_L$ = 2kΩ to AGND) and capacitive load ($C_L$ = 200pF to AGND), $f_{SCLK}$ = 30MHz, and input code range: 48d to 4047d (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $P_C$ | Power consumption | Output unloaded, normal mode, $f_{SCLK}$ = 30MHz | $V_A$ = 5.5V | | | 1.72 | mW |
| | | | $V_A$ = 3.6V | | | 0.78 | |
| | | Output unloaded, normal mode, $f_{SCLK}$ = 20MHz(1) | $V_A$ = 5.5V | | | 1.53 | |
| | | | $V_A$ = 3.6V | | | 0.71 | |
| | | Output unloaded, normal mode, $f_{SCLK}$ = 0MHz(1) | $V_A$ = 5.5V | | | 0.84 | |
| | | | $V_A$ = 3.6V | | | 0.42 | |
| | | Output unloaded, all PD modes, $f_{SCLK}$ = 30MHz(1) | $V_A$ = 5V | | | 0.42 | μW |
| | | | $V_A$ = 3V | | | 0.13 | |
| | | Output unloaded, all PD modes, $f_{SCLK}$ = 20MHz(1) | $V_A$ = 5V | | | 0.28 | |
| | | | $V_A$ = 3V | | | 0.08 | |
| | | Output unloaded, all PD modes, $f_{SCLK}$ = 0MHz | $V_A$ = 5.5V | | 0.825 | 7.7 | |
| $I_{OUT}$ / $I_A$ | Power efficiency | $I_{LOAD}$ = 2mA | $V_A$ = 5V | | 91 | | % |
| | | | $V_A$ = 3V | | 94 | | |

(1) Specified by design and characterization, not production tested.


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## 5.6 Timing Requirements

all input signals are specified at 2.7V ≤ $V_A$ ≤ 5.5V, $T_A$ = 25°C, and $f_{SCLK}$ = 30MHz (unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCLK}$ | SCLK frequency(1) | | | | 30 | MHz |
| $1/f_{SCLK}$ | SCLK cycle time(1) | | 33 | | | ns |
| $t_H$ | SCLK high time(1) | | 5 | | | ns |
| $t_L$ | SCLK low time(1) | | 5 | | | ns |
| $t_{SUD}$ | $D_{IN}$ setup time(1) | | 2.5 | | | ns |
| $t_{DHD}$ | $D_{IN}$ hold time(1) | | 2.5 | | | ns |
| $t_{SUCL}$ | $\overline{SYNC}$ to SCLK rising edge setup time(1) | | −15 | | | ns |
| $t_{CS}$ | SCLK falling edge to $\overline{SYNC}$ rising edge(1) | $V_A$ = 5V | 0 | | | ns |
| | | $V_A$ = 3V | −2 | | | |
| $t_{SYNC}$ | $\overline{SYNC}$ high time(1) | 2.7V ≤ $V_A$ ≤ 3.6V | 9 | | | ns |
| | | 3.6V ≤ $V_A$ ≤ 5.5V | 5 | | | |

(1) Specified by design and characterization, not production tested.

## 5.7 Timing Diagram

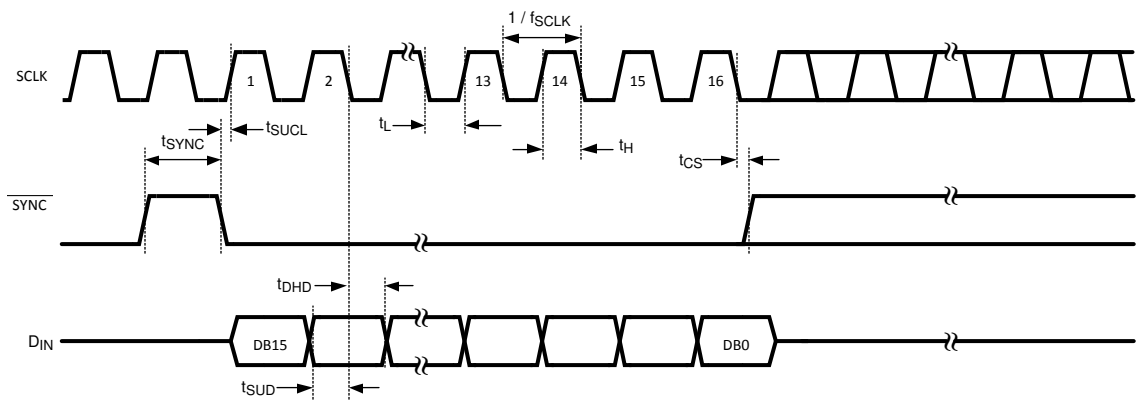


**Figure 5-1. Timing Diagram**

## 5.8 Typical Characteristics

at $f_{SCLK}$ = 30MHz, $T_A$ = 25°C, and input code range = 48 to 4047 (unless otherwise noted)

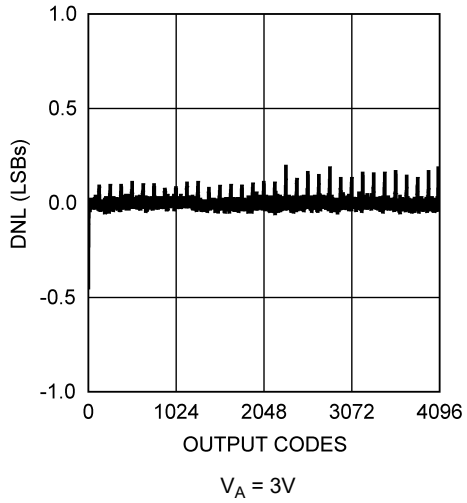


**Figure 5-2. DNL vs Output Code**

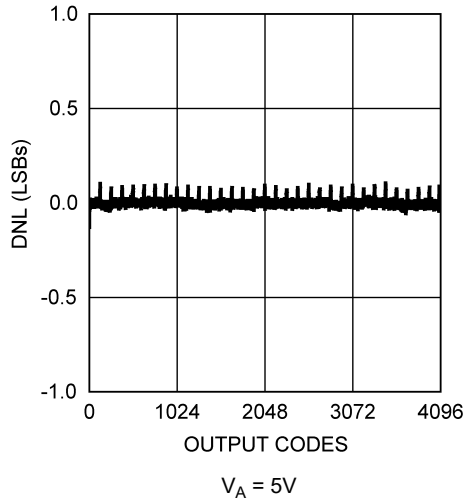


**Figure 5-3. DNL vs Output Code**

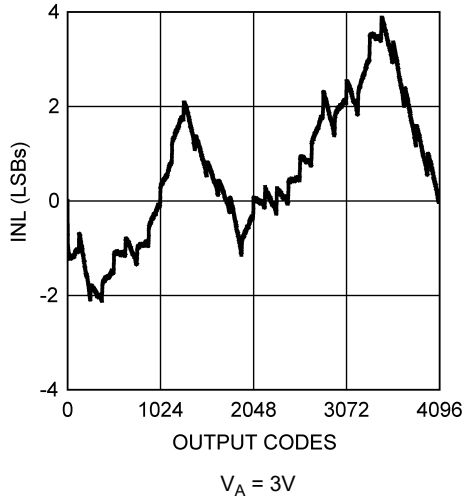


**Figure 5-4. INL vs Output Code**

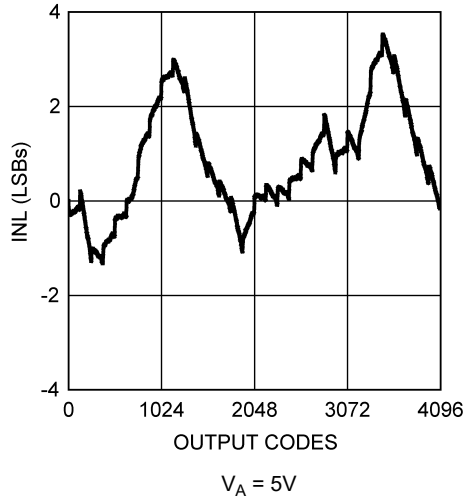


**Figure 5-5. INL vs Output Code**

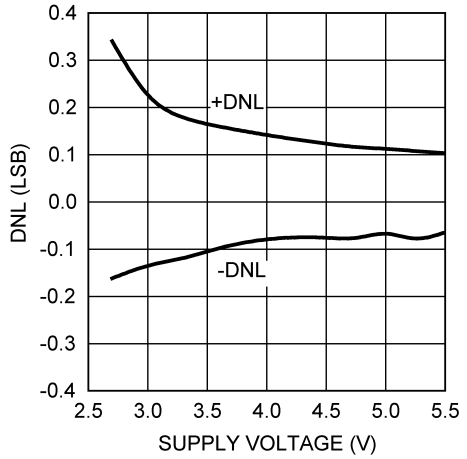


**Figure 5-6. DNL vs Supply Voltage**

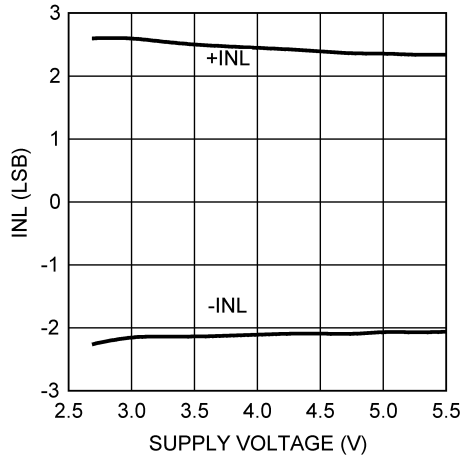


**Figure 5-7. INL vs Supply Voltage**


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## 5.8 Typical Characteristics (continued)

at $f_{SCLK}$ = 30MHz, $T_A$ = 25°C, and input code range = 48 to 4047 (unless otherwise noted)

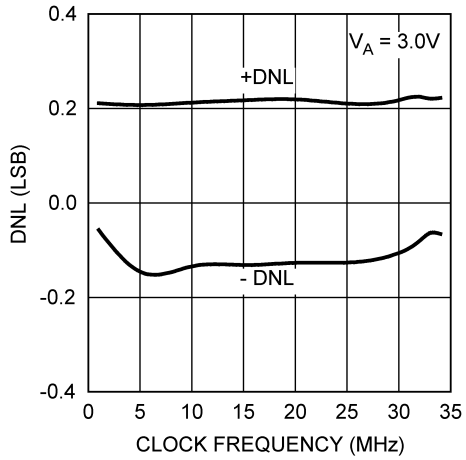


**Figure 5-8. 3V DNL vs Clock Frequency**

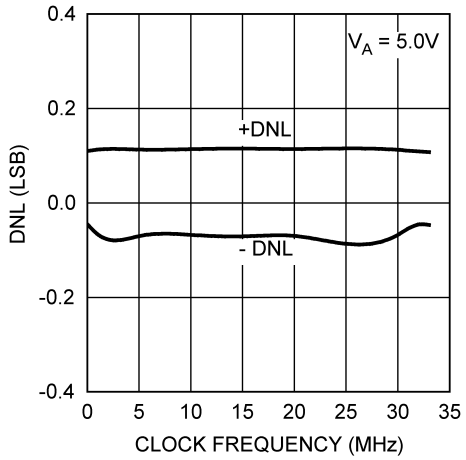


**Figure 5-9. 5V DNL vs Clock Frequency**

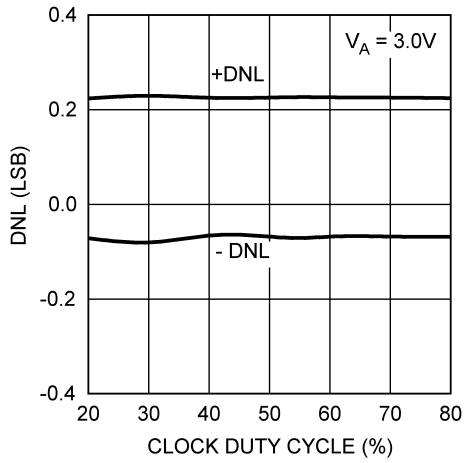


**Figure 5-10. 3V DNL vs Clock Duty Cycle**

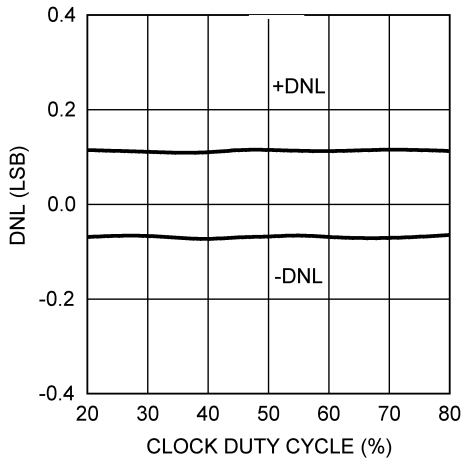


**Figure 5-11. 5V DNL vs Clock Duty Cycle**

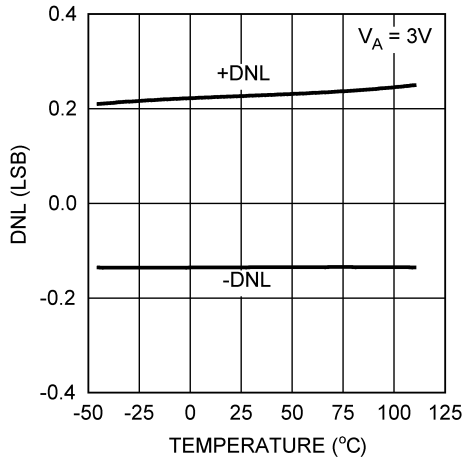


**Figure 5-12. 3V DNL vs Temperature**

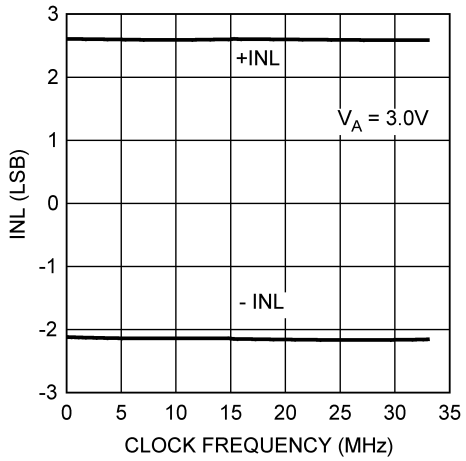


**Figure 5-13. 3V INL vs Clock Frequency**

## 5.8 Typical Characteristics (continued)

at $f_{SCLK}$ = 30MHz, $T_A$ = 25°C, and input code range = 48 to 4047 (unless otherwise noted)

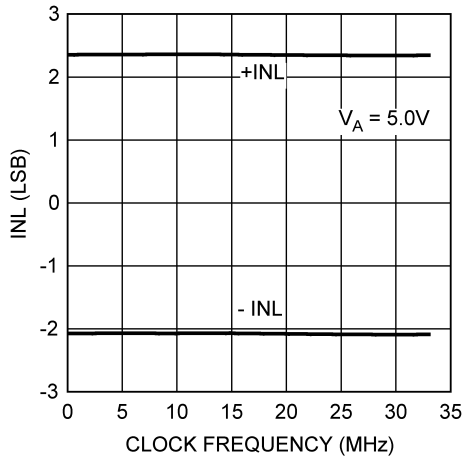


**Figure 5-14. 5V INL vs Clock Frequency**

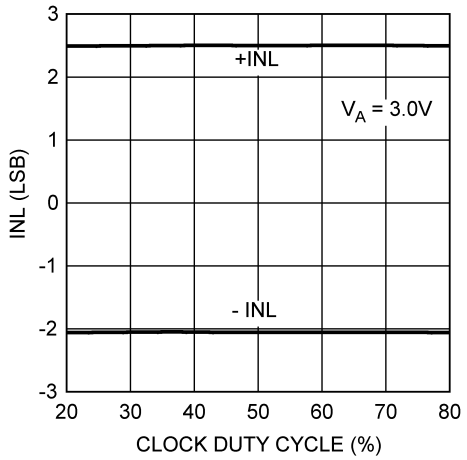


**Figure 5-15. 3V INL vs Clock Duty Cycle**

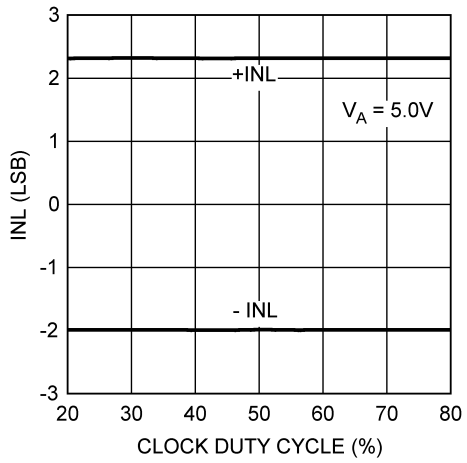


**Figure 5-16. 5V INL vs Clock Duty Cycle**

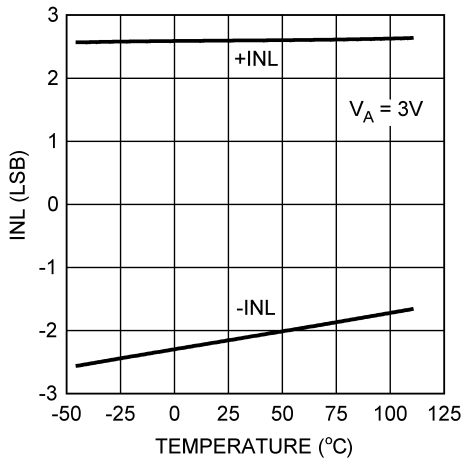


**Figure 5-17. 3V INL vs Temperature**

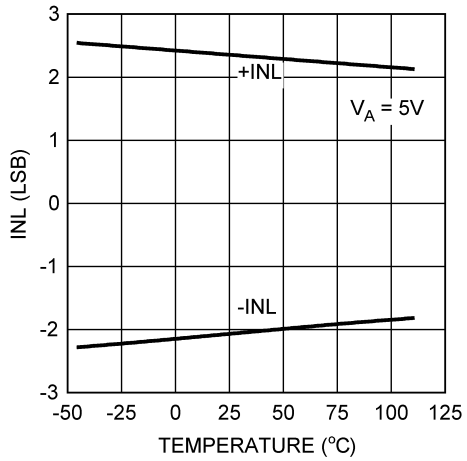


**Figure 5-18. 5V INL vs Temperature**

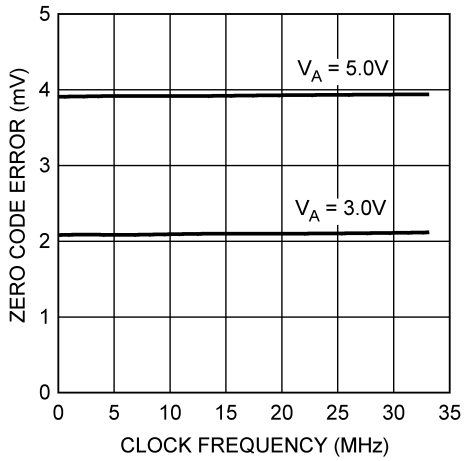


**Figure 5-19. Zero Code Error vs Clock Frequency**


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## 5.8 Typical Characteristics (continued)

at $f_{SCLK}$ = 30MHz, $T_A$ = 25°C, and input code range = 48 to 4047 (unless otherwise noted)

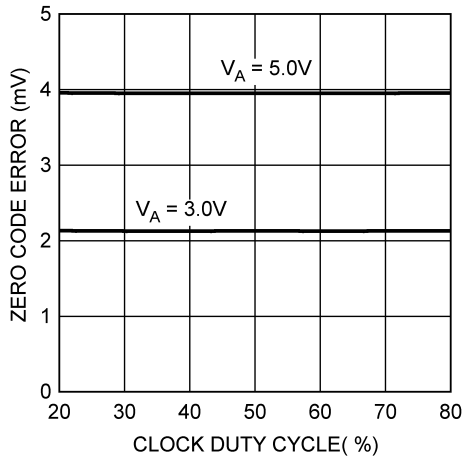


**Figure 5-20. Zero Code Error vs Clock Duty Cycle**

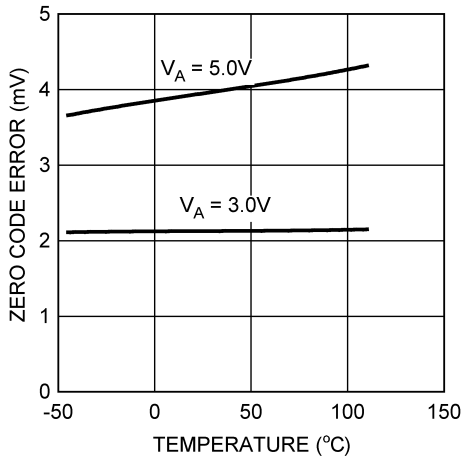


**Figure 5-21. Zero Code Error vs Temperature**

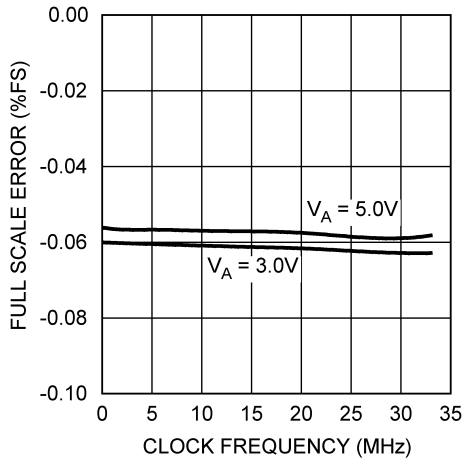


**Figure 5-22. Full-Scale Error vs Clock Frequency**

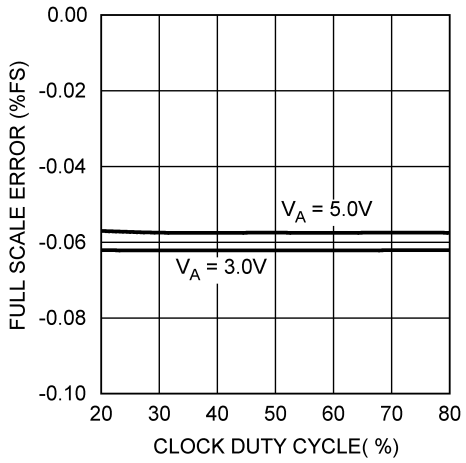


**Figure 5-23. Full-Scale Error vs Clock Duty Cycle**

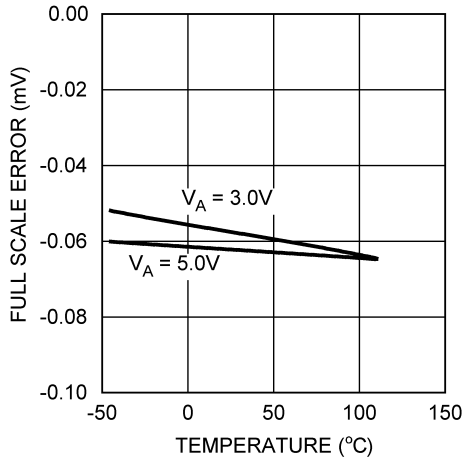


**Figure 5-24. Full-Scale Error vs Temperature**

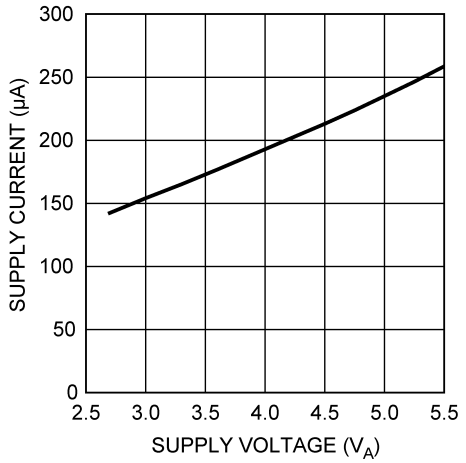


**Figure 5-25. Supply Current vs Supply Voltage**

## 5.8 Typical Characteristics (continued)

at $f_{SCLK}$ = 30MHz, $T_A$ = 25°C, and input code range = 48 to 4047 (unless otherwise noted)

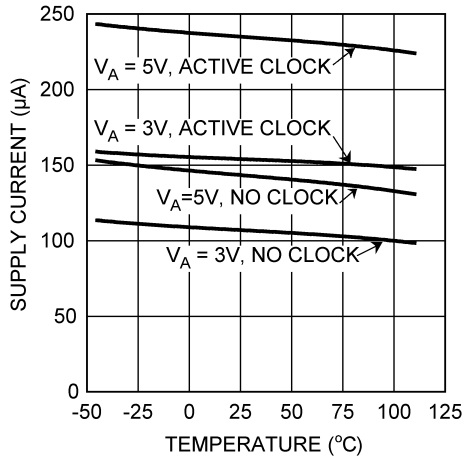


**Figure 5-26. Supply Current vs Temperature**

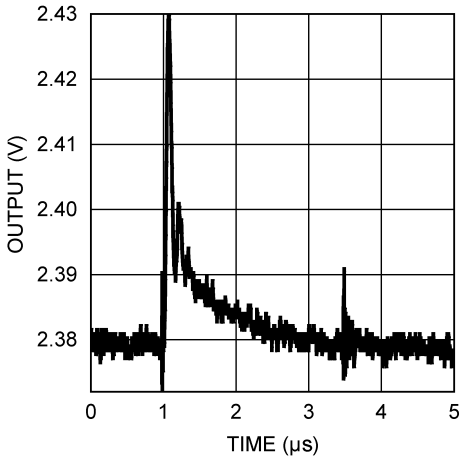


**Figure 5-27. 5V Glitch Response**

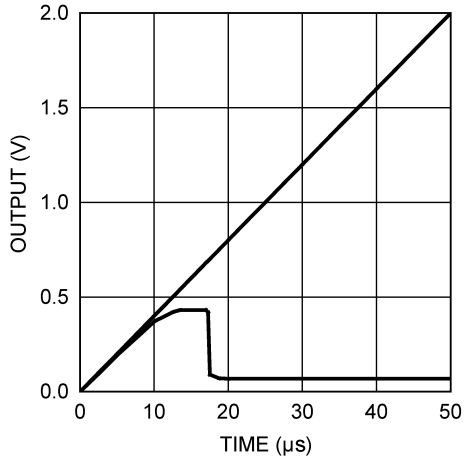


**Figure 5-28. Power-On Reset**

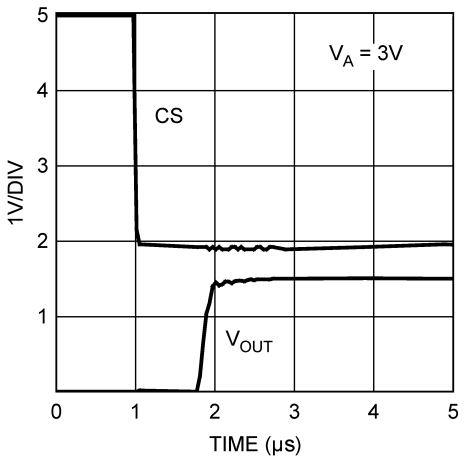


**Figure 5-29. 3V Wake-Up Time**

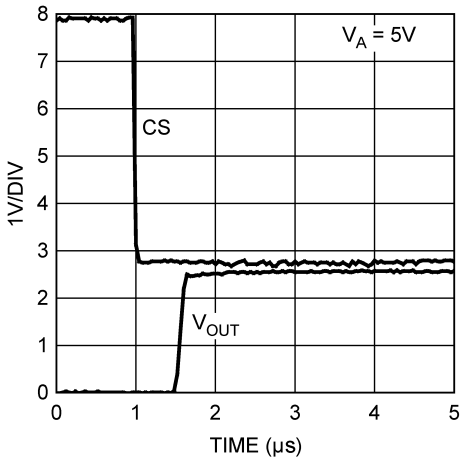


**Figure 5-30. 5V Wake-Up Time**


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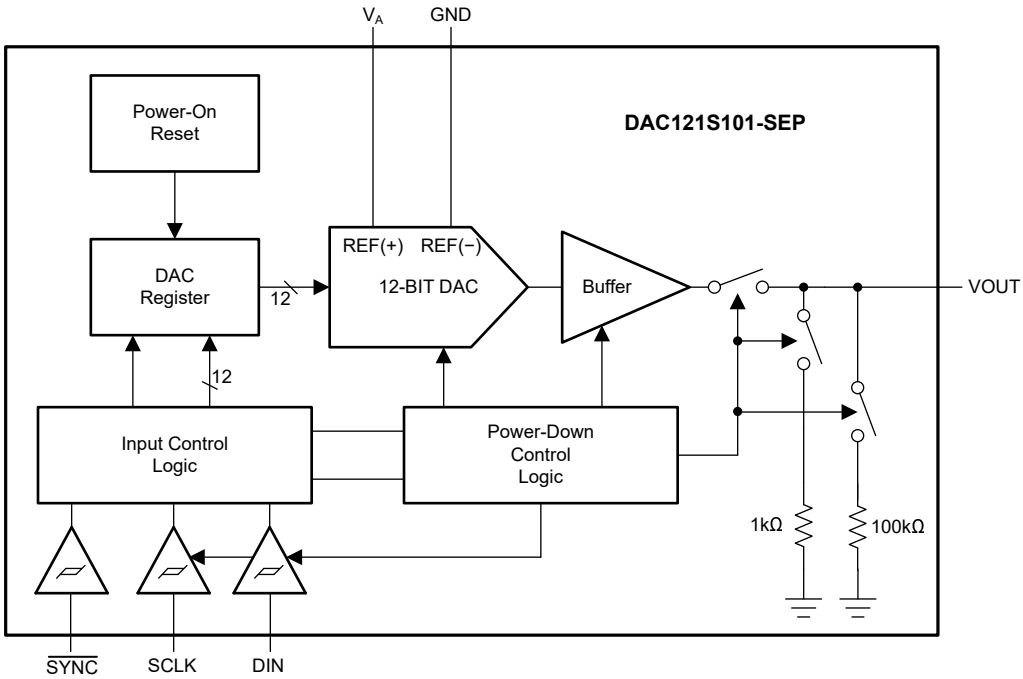
# 6 Detailed Description

## 6.1 Overview

The DAC121S101-SEP device is a full-featured, general-purpose, 12-bit voltage-output digital-to-analog converter (DAC) with a 12µs (typ) settling time. Control of the output of the DAC is achieved over a 3-wire SPI. After the DAC output is set, additional communication with the DAC is not required unless the output condition must be changed. Likewise, the DAC121S101-SEP power-on state is 0V. The DAC output remains at 0V until a valid write sequence is made.

A unique benefit of the DAC121S101-SEP is the logic levels of the SPI input pins. The logic levels of SCLK, DIN, and SYNCB are independent of $V_A$. As a result, the DAC121S101-SEP can operate at a supply voltage ($V_A$) that is higher than the microcontroller controlling the DAC. This feature is advantageous in applications where the analog circuitry is being run at 5V to maximize signal-to-noise ratio, and digital logic is running at 3V to conserve power.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

### *6.3.1 DAC Section*

The DAC121S101-SEP is fabricated on a CMOS process with an architecture that consists of switches and a resistor string that are followed by an output buffer. The power supply serves as the reference voltage. The input coding is straight binary with an ideal output voltage of Equation 1:

$$V_{OUT} = V_A \times \left(\frac{D}{4096}\right) \tag{1}$$

where

- *D* is the decimal equivalent of the binary code that is loaded into the DAC register and can take on any value between 0 and 4095.

### 6.3.2 Resistor String

Figure 6-1 shows the resistor string. This string consists of 4096 equal-valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. This configuration keeps the DAC monotonic.

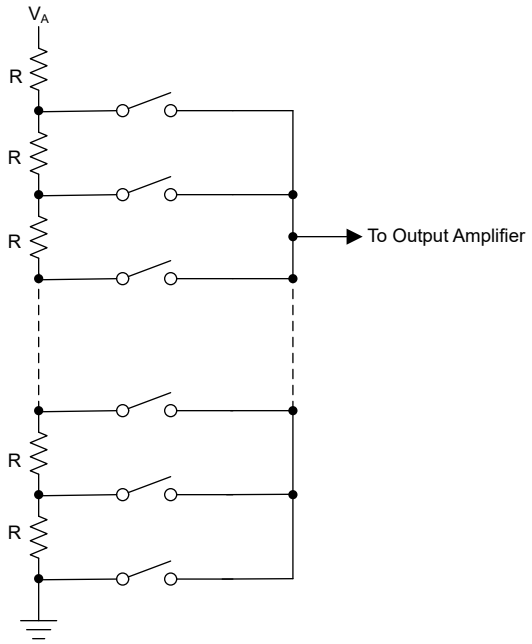



**Figure 6-1. DAC Resistor String**

### 6.3.3 Output Amplifier

The output buffer amplifier is a rail-to-rail type, providing an output voltage range of 0V to $V_A$. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0V and $V_A$, in this case). For this reason, linearity is specified over less than the full output range of the DAC. The output capabilities of the amplifier are described in the *Electrical Characteristics*.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## 6.4 Device Functional Modes

### *6.4.1 Power-On Reset*

The power-on reset circuit controls the output voltage during power-up. Upon application of power the DAC register is filled with zeros and the output voltage is 0V and remains there until a valid write sequence is made to the DAC.

### *6.4.2 Power-Down Modes*

Table 6-1 lists the DAC121S101-SEP four modes of operation. These modes are set with two bits (DB13 and DB12) in the control register.

**Table 6-1. Modes of Operation**

| DB13 | DB12 | OPERATING MODE |
|---|---|---|
| 0 | 0 | Normal operation |
| 0 | 1 | Power-down with 1kΩ to GND |
| 1 | 0 | Power-down with 100kΩ to GND |
| 1 | 1 | Power-down with Hi-Z |

When both DB13 and DB12 are 0, the device operates normally. For the other three possible combinations of these bits the supply current drops to the power-down level and the output is pulled down with either a 1kΩ or a 100kΩ resistor, or is in a high-impedance state, as described in Table 6-1.

The bias generator, output amplifier, the resistor string and other linear circuitry are shut down in any of the power-down modes. However, the contents of the DAC register are unaffected when in power-down; therefore, when coming out of power down, the output voltage returns to the same voltage before entering power down. Minimum power consumption is achieved in the power-down mode with SCLK disabled and $\overline{\text{SYNC}}$ and DIN idled low. The time to exit power-down (the wake-up time) is typically $t_{WU}$ (µs) as stated in the *Dynamic Performance* section of the *Electrical Characteristics* table.

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## 6.5 Programming

### *6.5.1 Serial Interface*

The three-wire interface is compatible with SPI, QSPI and MICROWIRE, as well as most DSPs. See Figure 5-1 for information on a write sequence.

A write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. After $\overline{\text{SYNC}}$ is low, the data on the DIN line is clocked into the 16-bit serial input register on the falling edges of SCLK. On the 16th falling clock edge, the last data bit is clocked in, and the programmed function (a change in the mode of operation, a change in the DAC register contents, or both) is executed. At this point, the $\overline{\text{SYNC}}$ line can be kept low or brought high. In either case, bring the $\overline{\text{SYNC}}$ line high for the minimum specified time before the next write sequence because a falling edge of $\overline{\text{SYNC}}$ can initiate the next write cycle.

The $\overline{\text{SYNC}}$ and DIN buffers draw more current when high; therefore, idle these buffers low between write sequences to minimize power consumption.

### *6.5.2 Input Shift Register*

The input shift register, Figure 6-2, has sixteen bits. The first two bits are *don't care* bits, and are followed by two bits that determine the mode of operation (normal mode or one-of-three power-down modes). The contents of the serial input register are transferred to the DAC register on the sixteenth falling edge of SCLK. See also Figure 5-1.

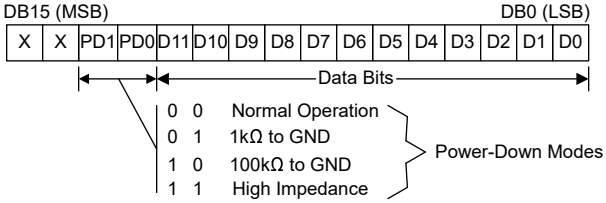


**Figure 6-2. Input Register Contents**

Normally, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th SCLK falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, the shift register is reset and the write sequence is invalid. In this case, the DAC register is not updated, and there is no change in the mode of operation or in the output voltage.


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# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

### *7.1.1 Bipolar Operation*

The DAC121S101-SEP is designed for single-supply operation, and thus has a unipolar output. However, a bipolar output can be obtained with the circuit in Figure 7-1. This circuit provides an output voltage range of ±5V.

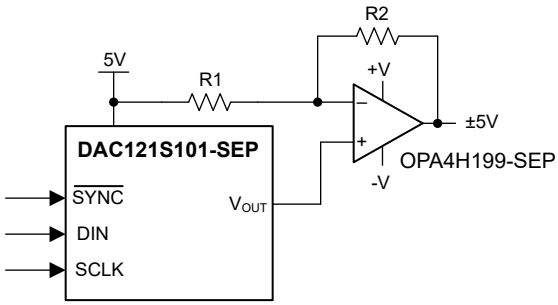


**Figure 7-1. Bipolar Operation**

The output voltage of this circuit for any code is found using Equation 2:

$$V_O = V_A \times \left(\frac{D}{4096}\right) \times \left(\frac{R1 + R2}{R1}\right) - V_A \times \frac{R2}{R} \tag{2}$$

where

- D is the input code in decimal form.

With $V_A$ = 5V and R1 = R2, Equation 3 shows the result:

$$V_O = \left(\frac{10 \times D}{4096}\right) - 5V \tag{3}$$

## 7.2 Typical Application

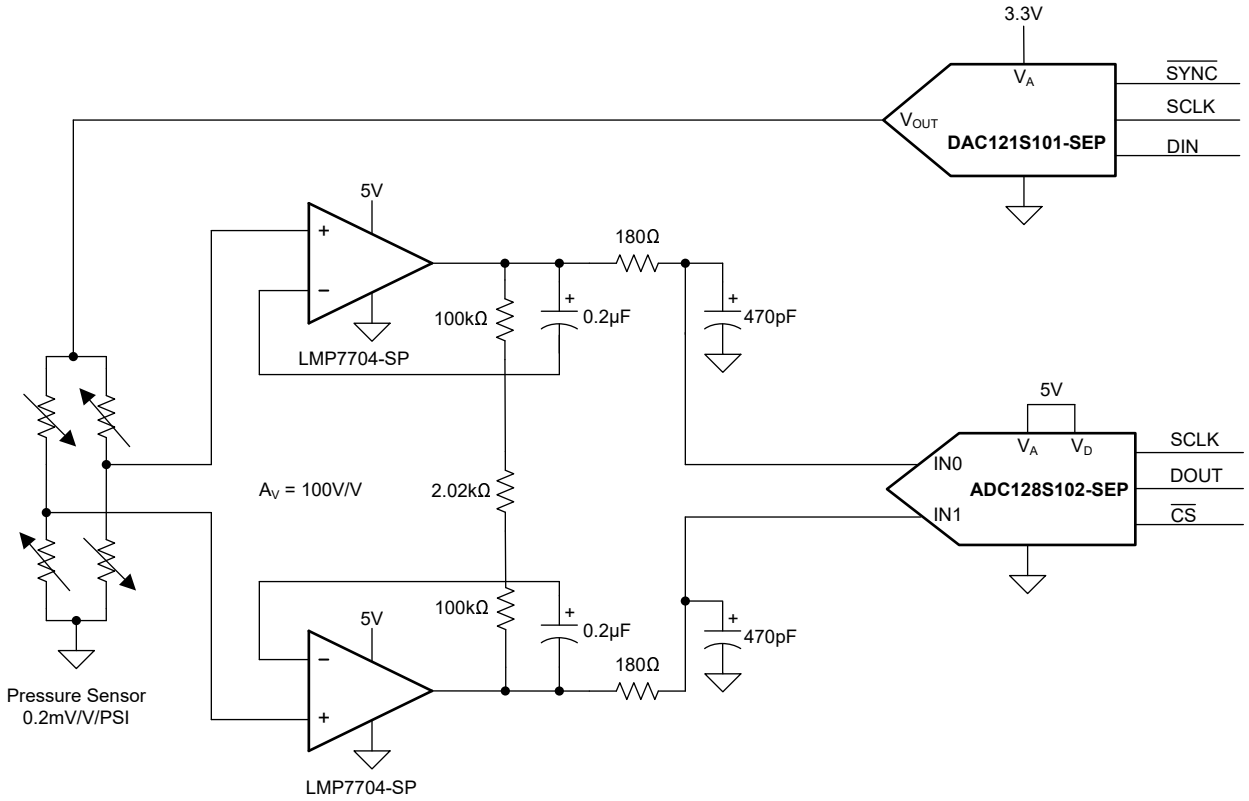


**Figure 7-2. Pressure Sensor Gain Adjust**

### *7.2.1 Design Requirements*

Design a single supply data acquisition system capable of digitizing a pressure sensor output. In addition to digitizing the pressure sensor output, use the DAC121S101-SEP to correct gain errors in the pressure sensor output by adjusting the bias voltage to the bridge pressure sensor. Table 7-1 lists the design parameters for DAC121S101-SEP.

**Table 7-1. DAC121S101-SEP Design Parameters**

| PARAMETER | VALUE |
|---|---|
| $V_A$ | 3.3V to 5V |
| DAC output range | 0V to 5V |


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### 7.2.2 Detailed Design Procedure

Equation 4 shows that the output of the pressure sensor is relative to the imbalance of the resistive bridge times the output of the DAC121S101-SEP, thus providing the desired gain correction.

$$\text{Pressure Sensor Output} = \text{DAC_Output} \times \left[\left(\frac{\text{R1}}{\text{R1} + \text{R2}}\right) - \left(\frac{\text{R4}}{\text{R3} + \text{R4}}\right)\right] \quad (4)$$

Likewise for the ADC128S102-SEP, Equation 5 shows that the ADC output is function of the pressure sensor output times relative to the ratio of the ADC input divided by the DAC121S101-SEP output voltage.

$$\text{ADC128S102-SEP Output} = \left(\text{Pressure Sensor Output} \times \left(\frac{100}{2 \times \text{VREF}}\right)\right) \times 2^{12} \quad (5)$$

### 7.2.3 Application Curve

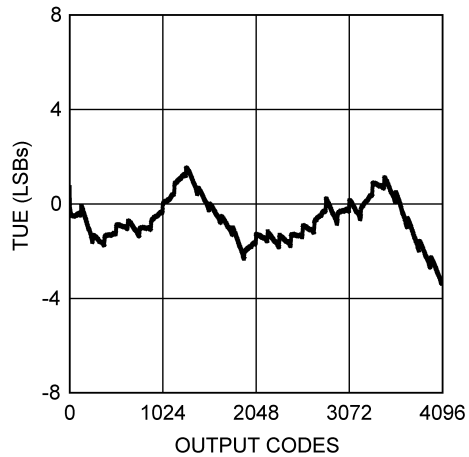


**Figure 7-3. Total Unadjusted Error vs Output Code**

## 7.3 Power Supply Recommendations

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The power applied to the $V_A$ pin must be well regulated and low noise. Switching power supplies and DC/DC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as internal logic states switch. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. As with the ground connection, connect $V_A$ to a power supply plane or trace that is separate from the connection for digital logic until $V_A$ is connected at the power entry point.

Bypass the DAC121S101-SEP power supply with 10µF and 0.1µF capacitors, as close as possible to the device with the 0.1µF directly at the device supply pin. The 0.1µF capacitor must be a low ESL, low ESR type. Decouple the power supply of DAC121S101-SEP from noisy circuits.

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## 7.4 Layout

### 7.4.1 Layout Guidelines

For best accuracy and minimum noise, the printed-circuit-board (PCB) that contains the DAC121S101-SEP must have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes must be located in the same board layer. Use a single ground plane; a single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design uses a *fencing* technique to prevent the mixing of analog and digital ground current. Only use separate ground planes when the fencing technique is inadequate. Connect the separate ground planes in one place, preferably near the DAC121S101-SEP. Take special care to make sure digital signals with fast edge rates do not pass over split ground planes. The digital signals must always have a continuous return path below the traces.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. The clock and data lines must have controlled impedance.

### 7.4.2 Layout Example

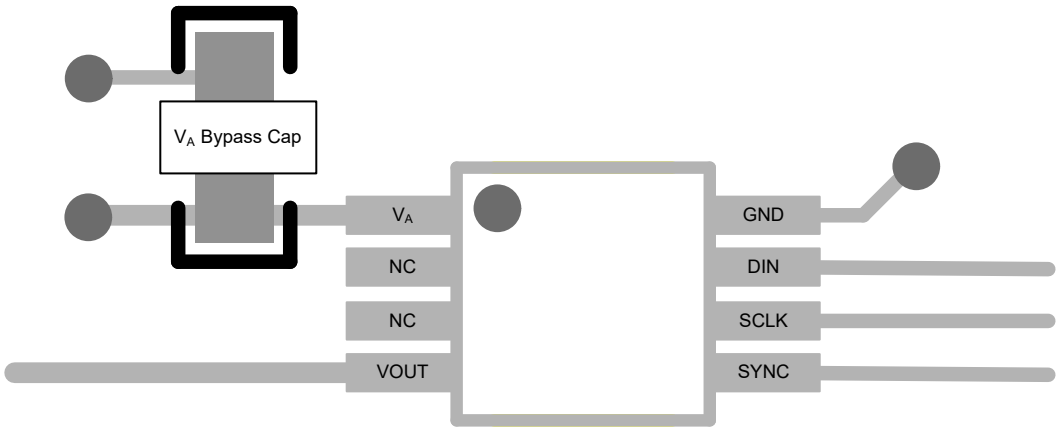


**Figure 7-4. Typical Layout**


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# 8 Device and Documentation Support

## 8.1 Documentation Support

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 8.4 Trademarks

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## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| December 2024 | * | Initial Release |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DAC121S101DGKTSEP | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 121S |
| DAC121S101DGKTSEP.A | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | See DAC121S101DGKTSEP | 121S |
| V62/24641-01XE | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | See DAC121S101DGKTSEP | 121S |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF DAC121S101-SEP :**

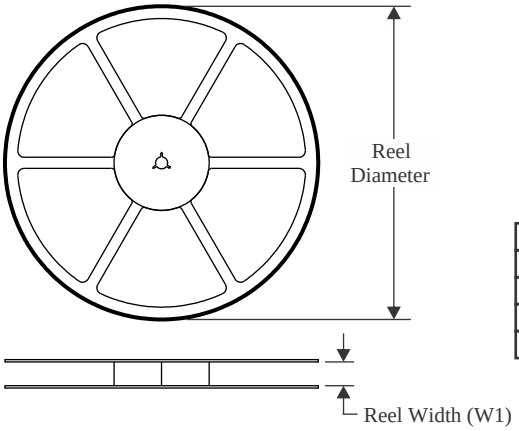
- Automotive : DAC121S101-Q1

NOTE: Qualified Version Definitions:

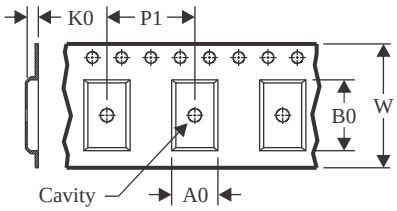
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

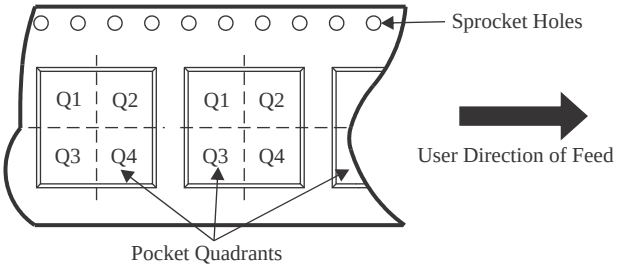



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

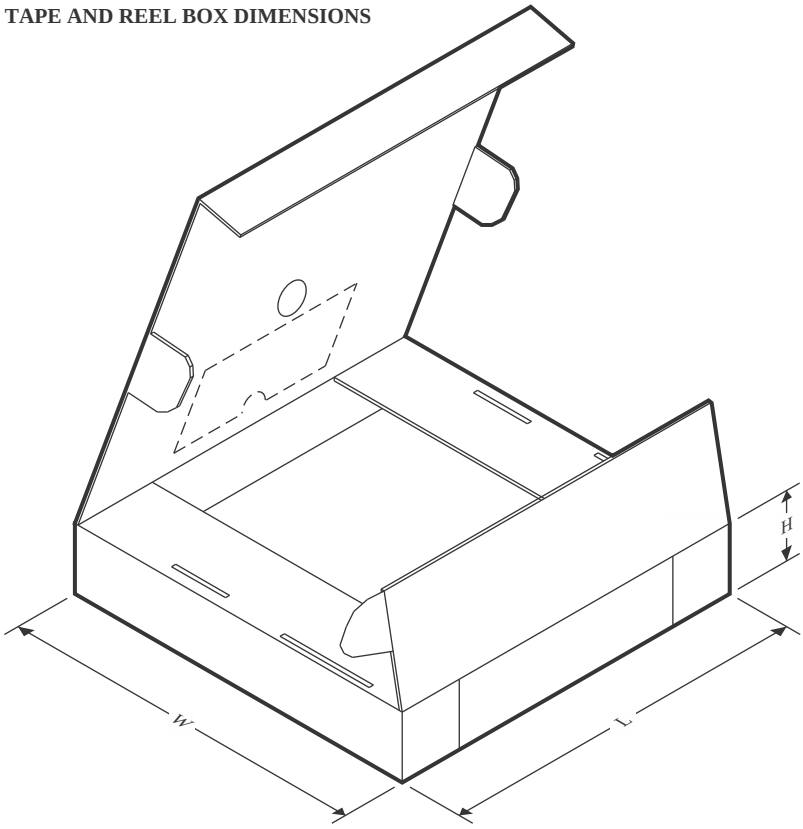
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DAC121S101DGKTSEP | VSSOP | DGK | 8 | 250 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

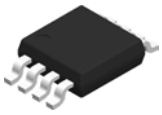



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DAC121S101DGKTSEP | VSSOP | DGK | 8 | 250 | 208.0 | 191.0 | 35.0 |

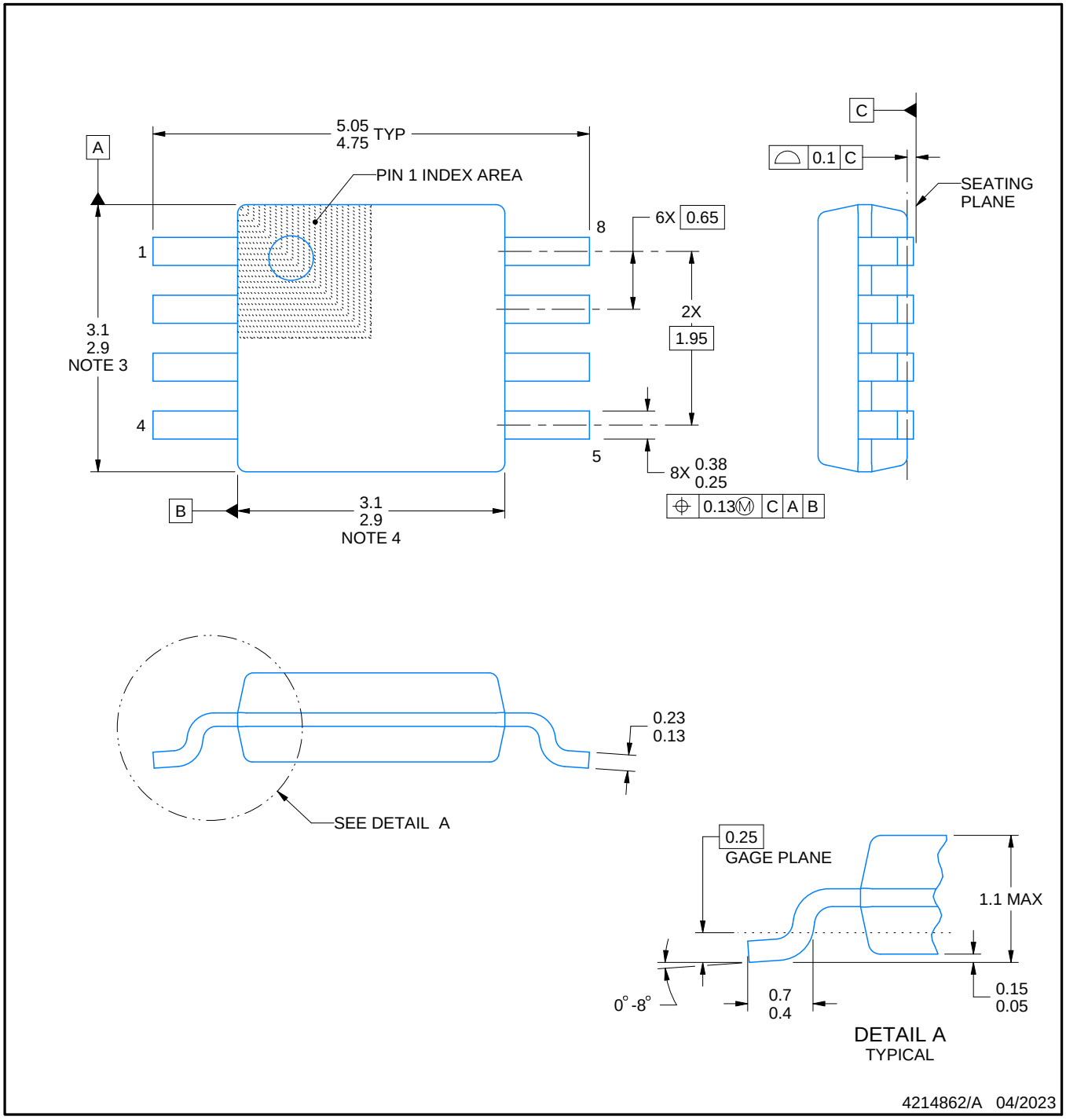
# PACKAGE OUTLINE

## DGK0008A



## VSSOP - 1.1 mm max height

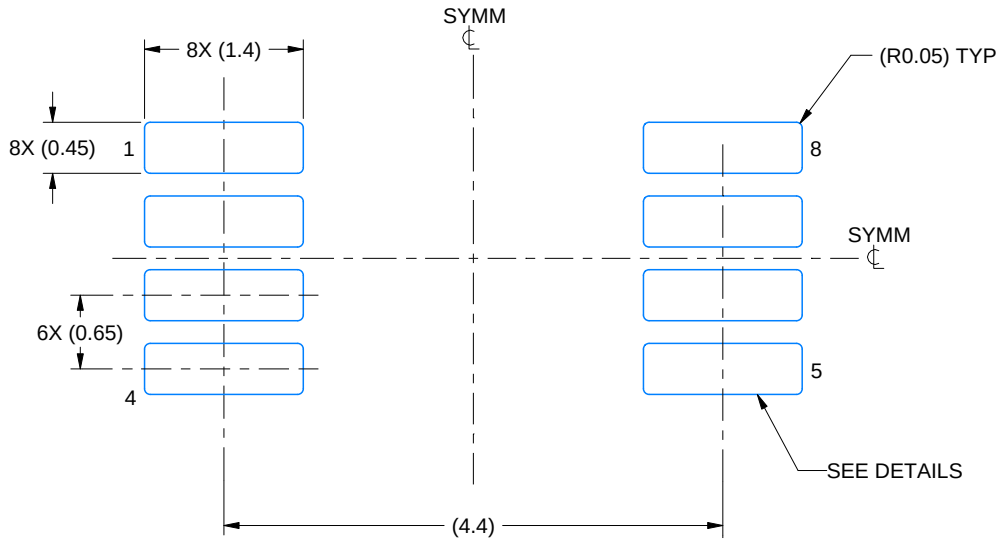
SMALL OUTLINE PACKAGE



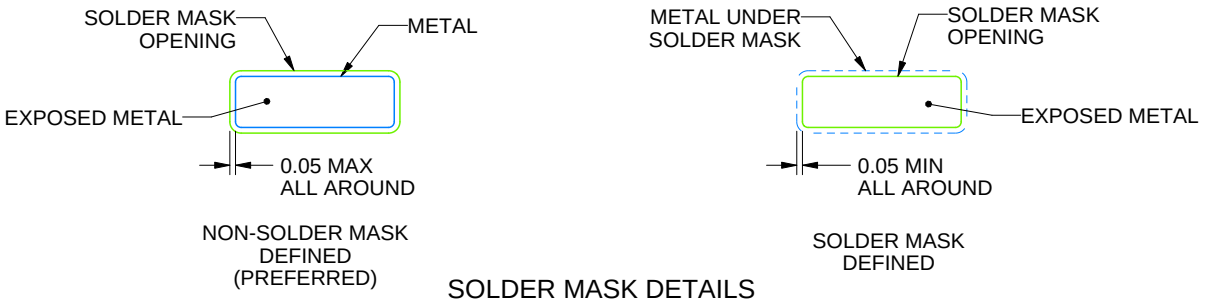

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X




SOLDER MASK DETAILS

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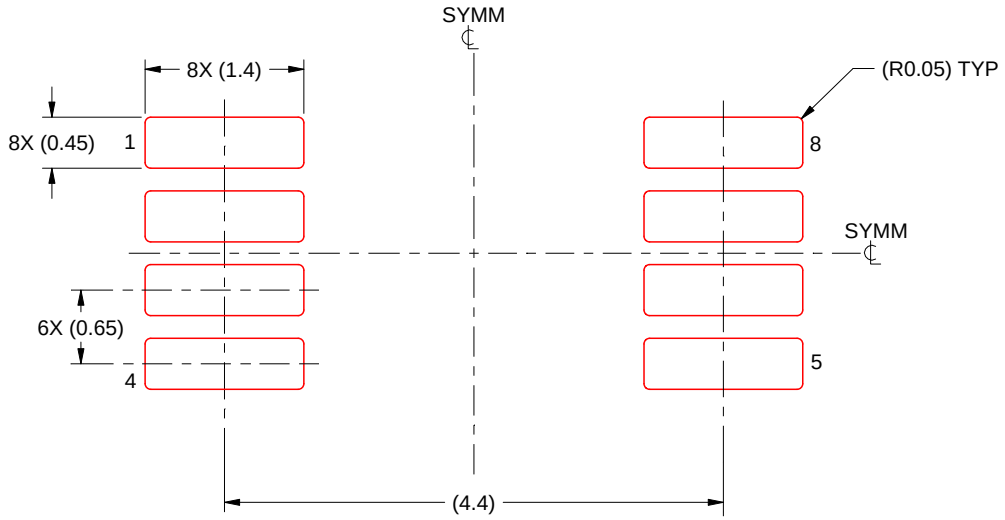
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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