

## REF200 Dual Current Source and Current Sink

### 1 Features

- Completely floating: no power supply or ground connections
- High accuracy:  $100\ \mu\text{A} \pm 0.5\%$
- Low temperature coefficient:  $\pm 25\ \text{ppm}/^\circ\text{C}$
- Wide voltage compliance: 2.5 V to 40 V
- Includes current mirror

### 2 Applications

- [Sensor excitation](#)
- [Biasing circuitry](#)
- [Offsetting current loops](#)
- [Low voltage references](#)
- [Charge-pump circuitry](#)
- [Hybrid microcircuits](#)

### 3 Description

The REF200 combines three circuit building-blocks on a single monolithic chip: two  $100\text{-}\mu\text{A}$  current sources and a current mirror. The sections are dielectrically isolated, making them completely independent. Also, because the current sources are two-terminal devices, they can be used equally well as current sinks. The performance of each section is individually measured and laser-trimmed to achieve high accuracy at low cost.

The sections can be pin-strapped for currents of  $50\ \mu\text{A}$ ,  $100\ \mu\text{A}$ ,  $200\ \mu\text{A}$ ,  $300\ \mu\text{A}$ , or  $400\ \mu\text{A}$ . External circuitry can obtain virtually any current. These and many other circuit techniques are shown in the [Application Information](#) section of this data sheet.

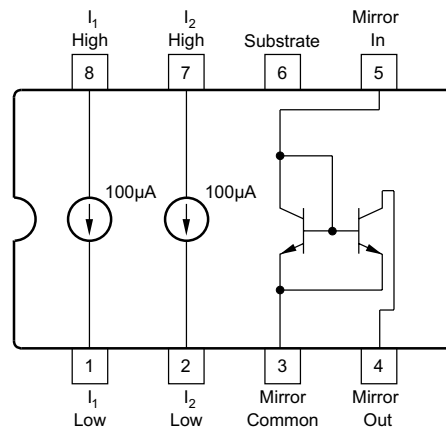
The REF200 is available in an SOIC package.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE  | BODY SIZE (NOM)   |
|-------------|----------|-------------------|
| REF200      | SOIC (8) | 3.91 mm × 4.90 mm |

(1) For all available packages, see the package addendum at the end of the data sheet.

#### Functional Block Diagram



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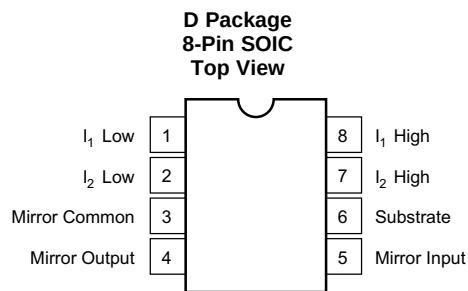
|                                                |          |                                                                  |           |
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (July 2015) to Revision C                                                                                                                                                                                                                                                                                                                  | Page |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Changed storage temperature.....                                                                                                                                                                                                                                                                                                                                 | 4    |
| Changes from Revision A (August 2013) to Revision B                                                                                                                                                                                                                                                                                                                | Page |
| • Changed multiple instances of "mA" in data sheet back to "μA" (typo) .....                                                                                                                                                                                                                                                                                       | 1    |
| Changes from Original (September 2000) to Revision A                                                                                                                                                                                                                                                                                                               | Page |
| • Added <i>ESD Ratings</i> and <i>Recommended Operating Conditions</i> tables, and <i>Feature Description</i> , <i>Device Functional Modes</i> , <i>Application and Implementation</i> , <i>Power Supply Recommendations</i> , <i>Layout</i> , <i>Device and Documentation Support</i> , and <i>Mechanical, Packaging, and Orderable Information</i> sections..... | 1    |

## 5 Pin Configuration and Functions



### Pin Functions

| PIN           |     | DESCRIPTION                                                            |
|---------------|-----|------------------------------------------------------------------------|
| NAME          | NO. |                                                                        |
| $I_1$ Low     | 1   | Current source 1 low terminal                                          |
| $I_2$ Low     | 2   | Current source 2 low terminal                                          |
| Mirror Common | 3   | Current mirror common terminal                                         |
| Mirror Output | 4   | Current mirror output terminal                                         |
| Mirror Input  | 5   | Current mirror input terminal                                          |
| Substrate     | 6   | Substrate (Usually connected to most negative potential in the system) |
| $I_2$ High    | 7   | Current source 2 high terminal                                         |
| $I_1$ High    | 8   | Current source 1 high terminal                                         |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                      | MIN | MAX  | UNIT |
|--------------------------------------|-----|------|------|
| Applied voltage                      | –6  | 40   | V    |
| Reverse current                      |     | –350 | μA   |
| Voltage between any two sections     |     | ±80  | V    |
| Operating temperature                | –40 | 85   | °C   |
| T <sub>stg</sub> Storage temperature | –55 | 150  | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                                                                                                                           | VALUE | UNIT |
|---------------------------------------------------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(1)</sup> | ±750  | V    |

- (1) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                            | MIN | NOM | MAX | UNIT |
|--------------------------------------------|-----|-----|-----|------|
| V <sub>COMP</sub> Compliance voltage       | 2.5 |     | 40  | V    |
| T <sub>A</sub> Specified temperature range | –25 |     | 85  | °C   |

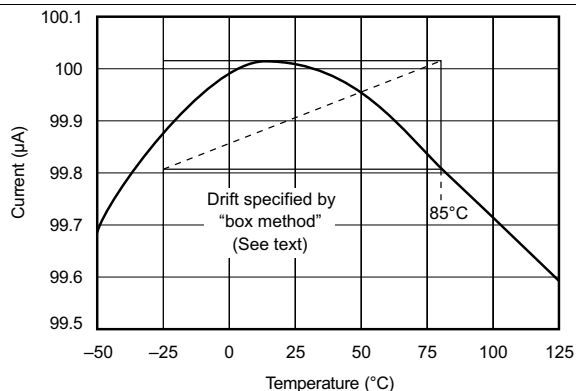
### 6.4 Electrical Characteristics

at T<sub>A</sub> = 25°C, V<sub>S</sub> = 15 V (unless otherwise noted)

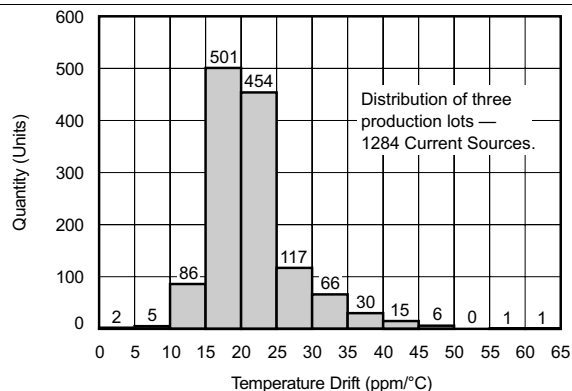
| PARAMETER                                                 | TEST CONDITIONS                      | MIN                                         | TYP    | MAX   | UNIT   |
|-----------------------------------------------------------|--------------------------------------|---------------------------------------------|--------|-------|--------|
| <b>CURRENT SOURCES</b>                                    |                                      |                                             |        |       |        |
| Current accuracy                                          |                                      |                                             | ±0.25% | ±1%   |        |
| Current match                                             |                                      |                                             | ±0.25% | ±1%   |        |
| Temperature drift                                         | Specified temperature range          |                                             | 25     |       | ppm/°C |
| Output impedance                                          | 2.5 V to 40 V                        | 20                                          | 100    |       | MΩ     |
|                                                           | 3.5 V to 30 V                        | 200                                         |        | 500   |        |
| Noise                                                     | BW = 0.1 Hz to 10 Hz                 |                                             | 1      |       | nAp-p  |
|                                                           | f = 10 kHz                           |                                             | 20     |       | pA/√Hz |
| Voltage compliance (1%)                                   | T <sub>MIN</sub> to T <sub>MAX</sub> | See <a href="#">Typical Characteristics</a> |        |       |        |
| Capacitance                                               |                                      |                                             | 10     |       | pF     |
| <b>CURRENT MIRROR – I = 100 μA unless otherwise noted</b> |                                      |                                             |        |       |        |
| Gain                                                      |                                      | 0.995                                       | 1      | 1.005 |        |
| Temperature drift                                         |                                      |                                             | 25     |       | ppm/°C |
| Impedance (output)                                        | 2 V to 40 V                          | 40                                          | 100    |       | MΩ     |
| Nonlinearity                                              | I = 0 μA to 250 μA                   |                                             | 0.05%  |       |        |
| Input voltage                                             |                                      |                                             | 1.4    |       | V      |
| Output compliance voltage                                 |                                      | See <a href="#">Typical Characteristics</a> |        |       |        |
| Frequency response (–3 dB)                                | Transfer                             |                                             | 5      |       | MHz    |

## 6.5 Typical Characteristics

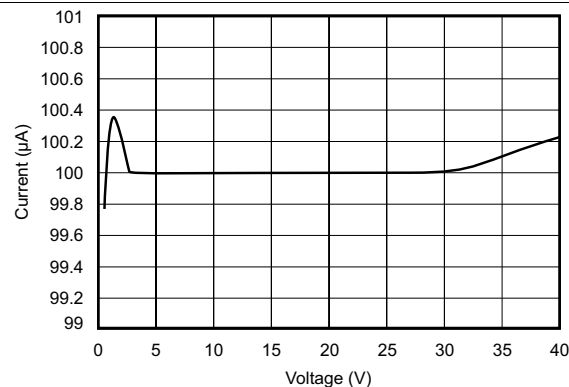
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 15\text{ V}$  (unless otherwise noted)



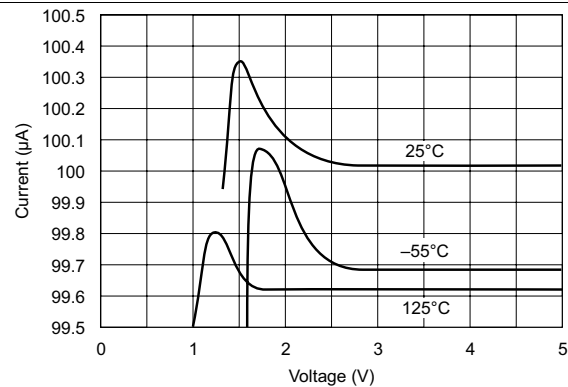
**Figure 1. Current Source Typical Drift vs Temperature**



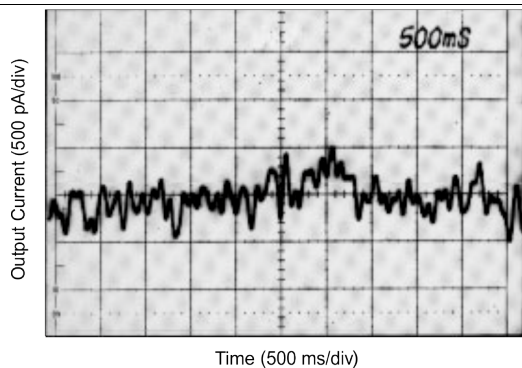
**Figure 2. Current Source Temperature Drift Distribution**



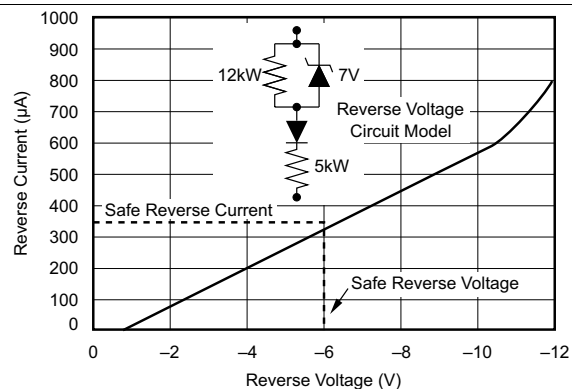
**Figure 3. Current Source Output Current vs Voltage**



**Figure 4. Current Source Output Current vs Voltage**



**Figure 5. Current Source Current Noise (0.1 Hz to 10 Hz)**



**Figure 6. Current Source Reverse Current vs Reverse Voltage**

## Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 15\text{ V}$  (unless otherwise noted)

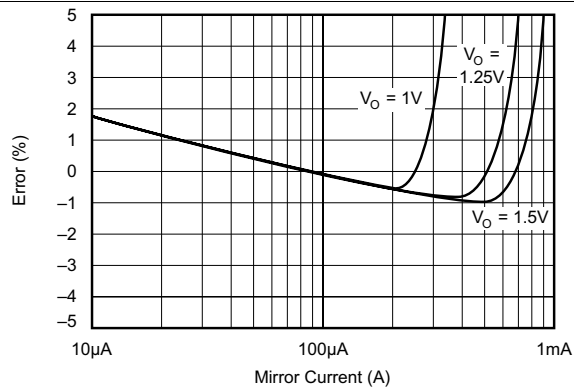


Figure 7. Mirror Gain Error vs Current

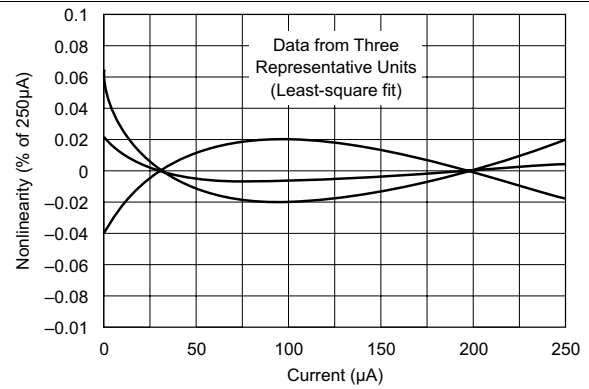


Figure 8. Mirror Transfer Nonlinearity

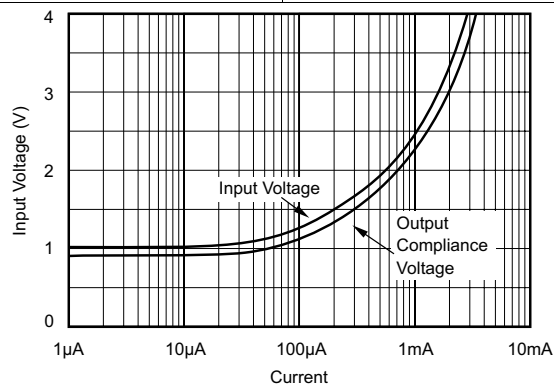


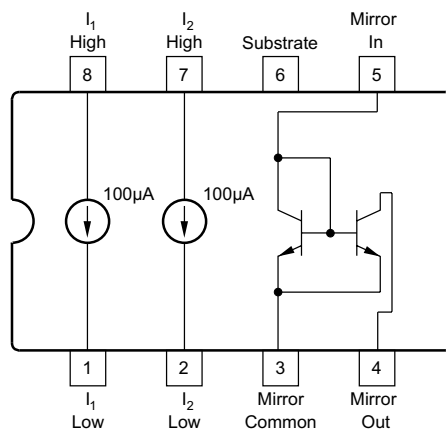
Figure 9. Mirror Input Voltage and Output Compliance Voltage vs Current

## 7 Detailed Description

### 7.1 Overview

The REF200 device combines three circuit building-blocks on a single monolithic chip—two 100- $\mu$ A current sources and a current mirror. The sections are dielectrically isolated, making them completely independent. Also, because the current sources are two terminal devices, they can be used equally well as current sinks. The performance of each section is individually measured and laser-trimmed to achieve high accuracy at low cost.

### 7.2 Functional Block Diagram



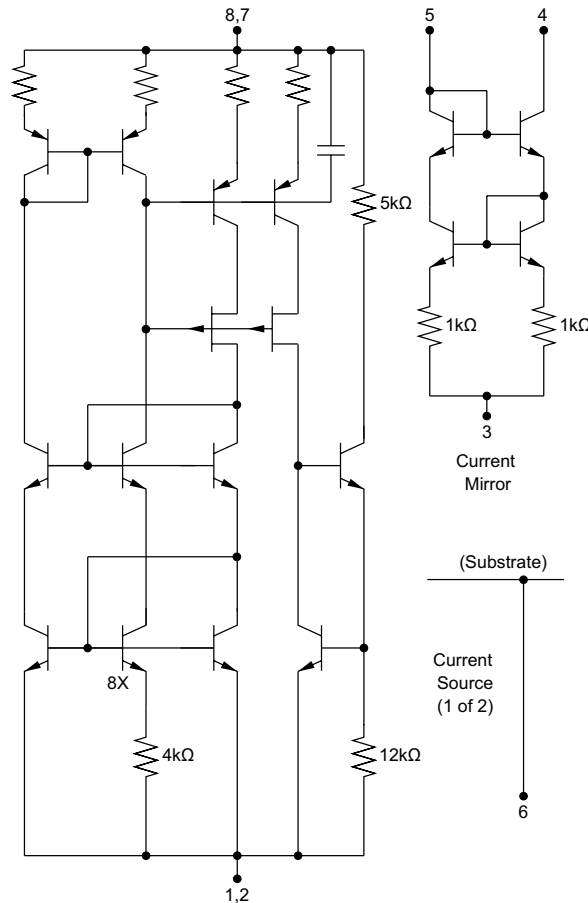
### 7.3 Feature Description

#### 7.3.1 Temperature Drift

Drift performance is specified by the *box method*, as illustrated in [Figure 1](#). The upper and lower current extremes measured over temperature define the top and bottom of the box. The sides are determined by the specified temperature range of the device. The drift of the unit is the slope of the diagonal, typically 25 ppm/ $^{\circ}$ C from  $-25^{\circ}$ C to  $+85^{\circ}$ C.

## 7.4 Device Functional Modes

The three circuit sections of the REF200 are electrically isolated from one another, using a dielectrically-isolated fabrication process. A substrate connection is provided (pin 6), which is isolated from all circuitry. This pin should be connected to a defined circuit potential to assure rated DC performance. The preferred connection is to the most negative constant potential in the system. In most analog systems, this would be  $-V_S$ . For best ac performance, leave pin 6 open and leave unused sections unconnected. Figure 10 shows the simplified circuit diagram of the REF200.



**Figure 10. Simplified Circuit Diagram**

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

Applications for the REF200 are limitless. Application Bulletin AB-165 ([SBOA046](#)) shows additional REF200 circuits as well as other related current source techniques. In this section, a collection of circuits are shown to illustrate some techniques.

If the current sources are subjected to reverse voltage, a protection diode may be required. A reverse voltage circuit model of the REF200 is shown in [Figure 6](#). If reverse voltage is limited to less than 6 V or reverse current is limited to less than 350  $\mu\text{A}$ , then no protection circuitry is required. A parallel diode (see (a) in [Figure 17](#)) protects the device by limiting the reverse voltage across the current source to approximately 0.7 V. In some applications, a series diode may be preferable (see (b) in [Figure 17](#)), because it allows no reverse current. This configuration, however, reduces the compliance voltage range by one diode drop.

### 8.2 Typical Application

[Figure 11](#) shows the schematic of a circuit that translates RTD resistance to a voltage level convenient for an ADC input. The REF200 precision current reference provides excitation and an instrumentation amplifier scales the signal. The design also uses a 3-wire RTD configuration to minimize errors due to wiring resistance.

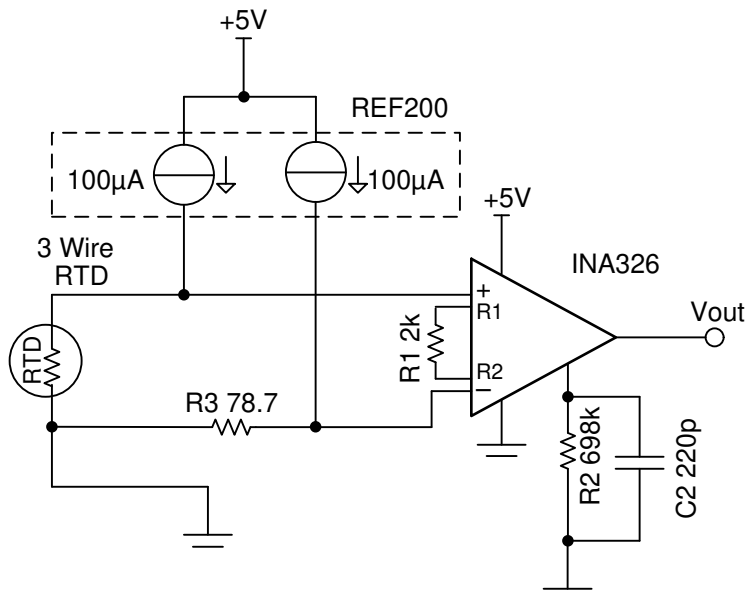


Figure 11. RTD Resistance to Voltage Converter Schematic

## Typical Application (continued)

### 8.2.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5 V
- RTD temperature range:  $-50^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- RTD resistance range  $80.3\ \Omega$  to  $147.9\ \Omega$
- Output: 0.1 V to 4.9 V

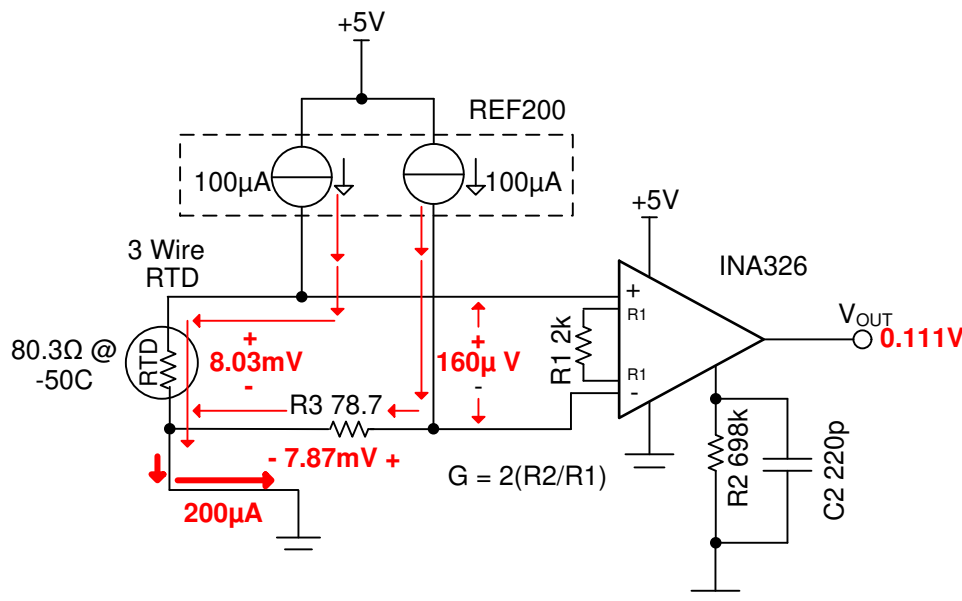
The design goals and performance are summarized in Table 1. Figure 15 depicts the measured transfer function of the design.

**Table 1. Comparison of Design Goals, Calculations, Simulation, and Measured Performance**

| $V_{\text{OUT}}$               | RTD             | GOAL  | CALCULATED | SIMULATED | MEASURED |
|--------------------------------|-----------------|-------|------------|-----------|----------|
| $V_{\text{OUT}}$ maximum scale | $80.3\ \Omega$  | 0.1 V | 0.112 V    | 0.117 V   | 0.113 V  |
| $V_{\text{OUT}}$ minimum scale | $142.9\ \Omega$ | 4.9 V | 4.83 V     | 4.82 V    | 4.862 V  |

### 8.2.2 Detailed Design Procedure

Figure 12 and Figure 13 shows the schematic of the RTD amplifier for minimum and maximum output conditions. This circuit was designed for a  $-50^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  RTD temperature range. At  $-50^{\circ}\text{C}$  the RTD resistance is  $80.3\ \Omega$  and the voltage across it is 8.03 mV ( $V_{\text{RTD}} = (100\ \mu\text{A})(80.3\ \Omega)$ , see Figure 2). Notice that R3 develops a voltage drop that opposes the RTD drop. The drop across R3 is used to shift amplifiers input differential voltage to a minimum level. The output is the differential input multiplied by the gain ( $V_{\text{out}} = 698 \cdot 160\ \mu\text{V} = 0.111\ \text{V}$ ). At  $150^{\circ}\text{C}$ , the RTD resistance is  $148\ \Omega$  and the voltage across it is 14.8 mV ( $V_{\text{RTD}} = (100\ \mu\text{A} \times 148\ \Omega)$ ). This produces a differential input of 6.93 mV and an output voltage of 4.84 V ( $V_{\text{OUT}} = 698 \cdot 6.93\ \text{mV} = 4.84\ \text{V}$ , see Figure 13). For more detailed design procedures and results, refer to the reference guide, *RTD to Voltage Reference Design Using Instrumentation Amplifier and Current Reference* (TIDU969).



**Figure 12. RTD Amplifier with Minimum Output Condition**

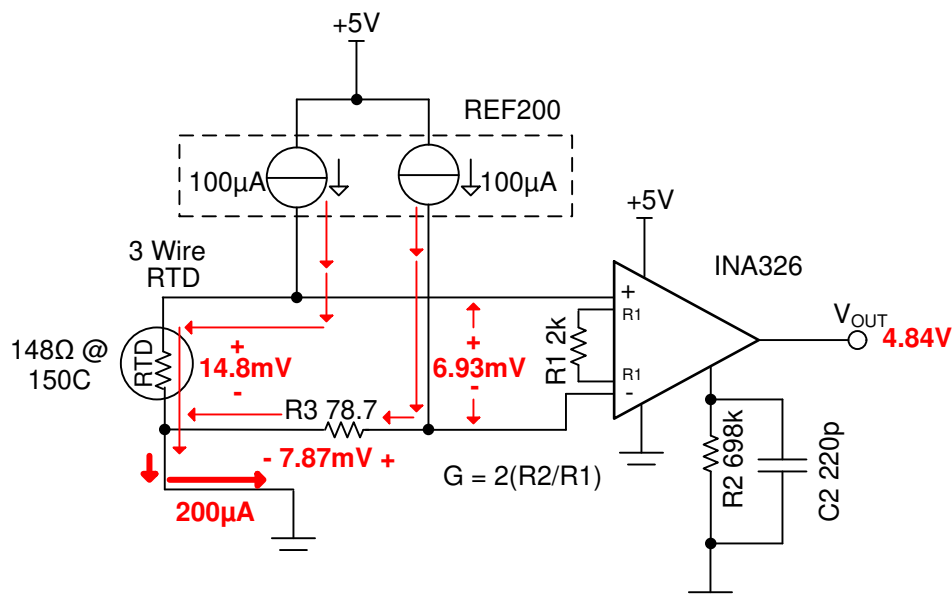


Figure 13. RTD Amplifier with Maximum Output Condition

#### 8.2.2.1 Lead Resistance Cancellation (3-Wire RTD)

Figure 14 shows the 3-wire RTD configuration can be used to cancel lead resistance. The resistance in each lead must be equal to cancel the error. Also, the two current sources in the REF200 must be equal. Notice that the voltage developed on the two top leads of the RTD are equal and opposite polarity so that the amplifiers input is only from the RTD voltage. In this example, the RTD drop is 14.8 mV and the leads each have 1 mV. Notice that the 1 mV drops cancel. Finally, notice that the voltage on the 3rd lead (2 mV) creates a small shift in the common mode voltage. In some applications, a larger resistor is intentionally added to shift the common-mode voltage. However, the INA326 has a rail-to-rail common mode range, so it can accept common-mode voltages near ground.

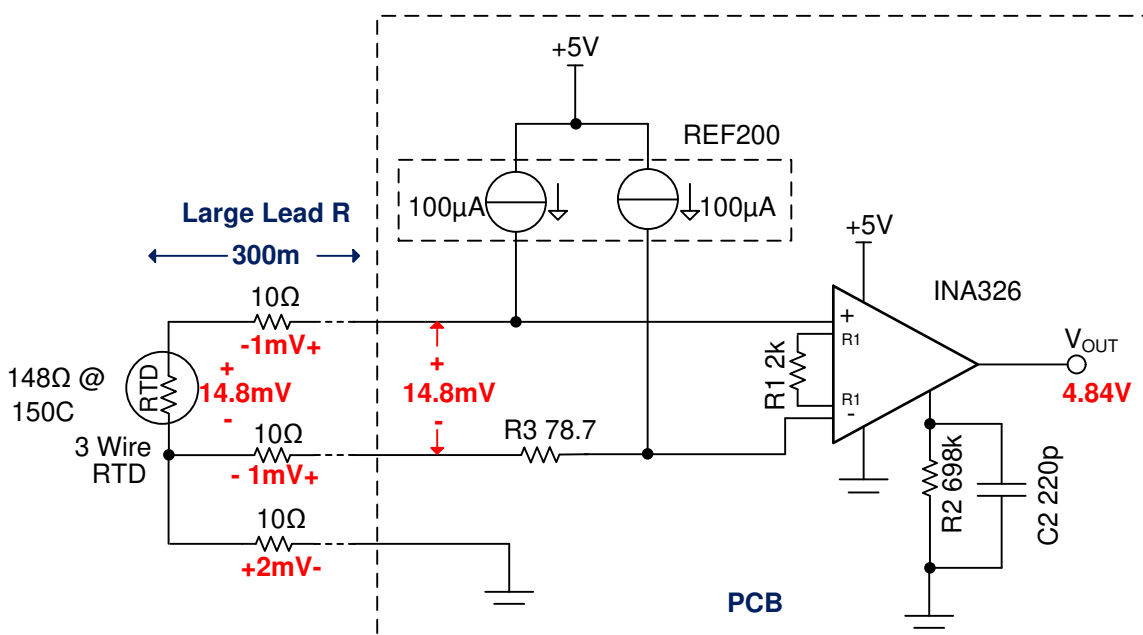
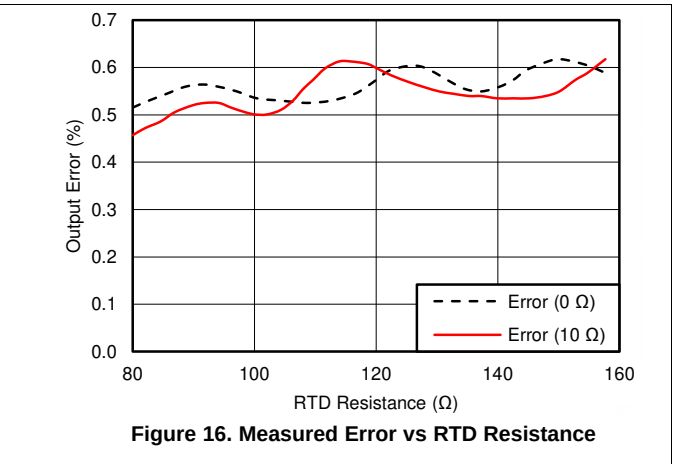
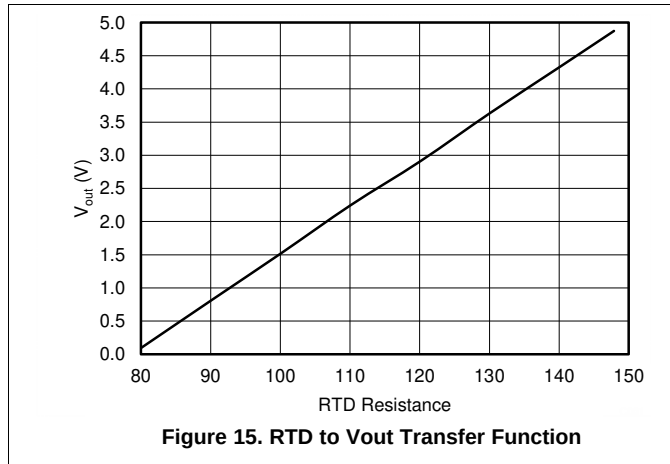
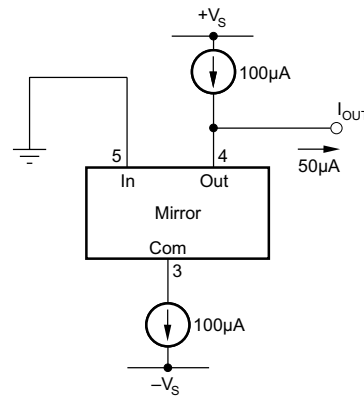
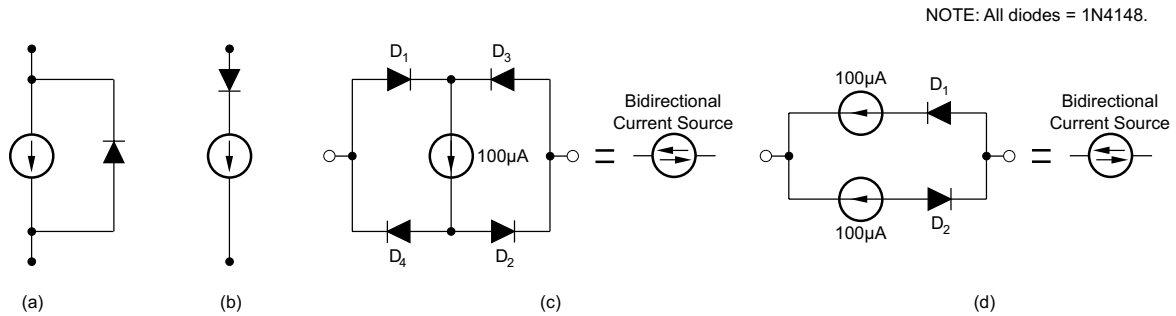


Figure 14. 3-Wire RTD Configuration Cancels Lead Resistance

### 8.2.3 Application Curves



### 8.3 System Examples



## System Examples (continued)

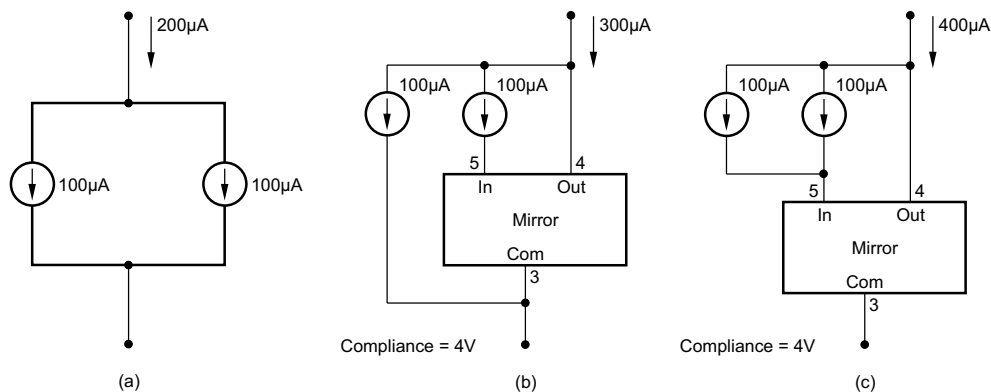


Figure 19. 200- $\mu$ A, 300- $\mu$ A, and 400- $\mu$ A Floating Current Sources

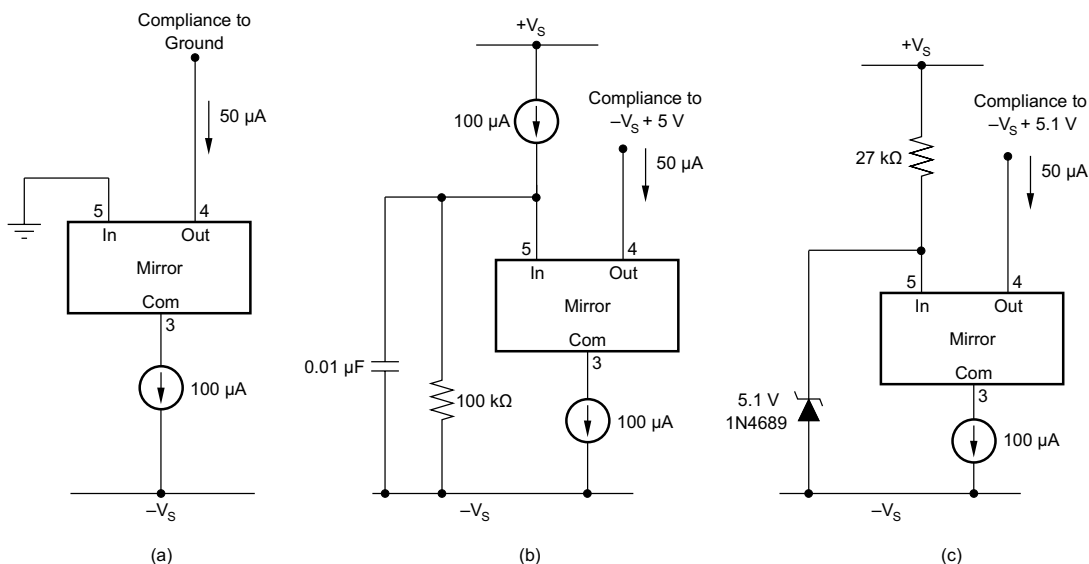


Figure 20. 50- $\mu$ A Current Sinks

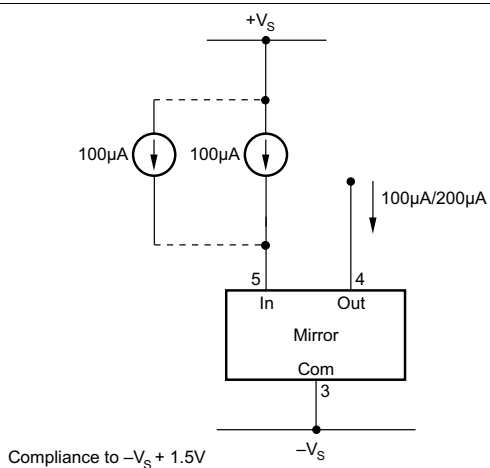


Figure 21. Improved Low-Voltage Compliance

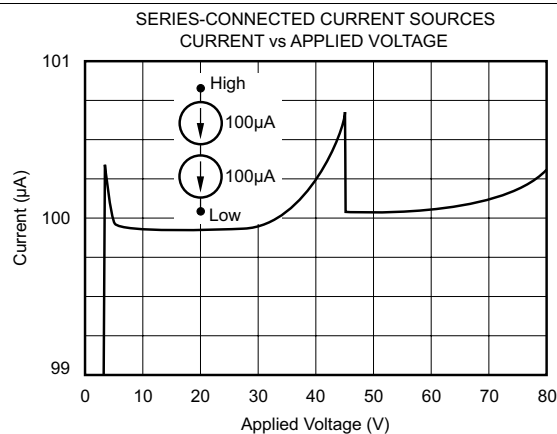
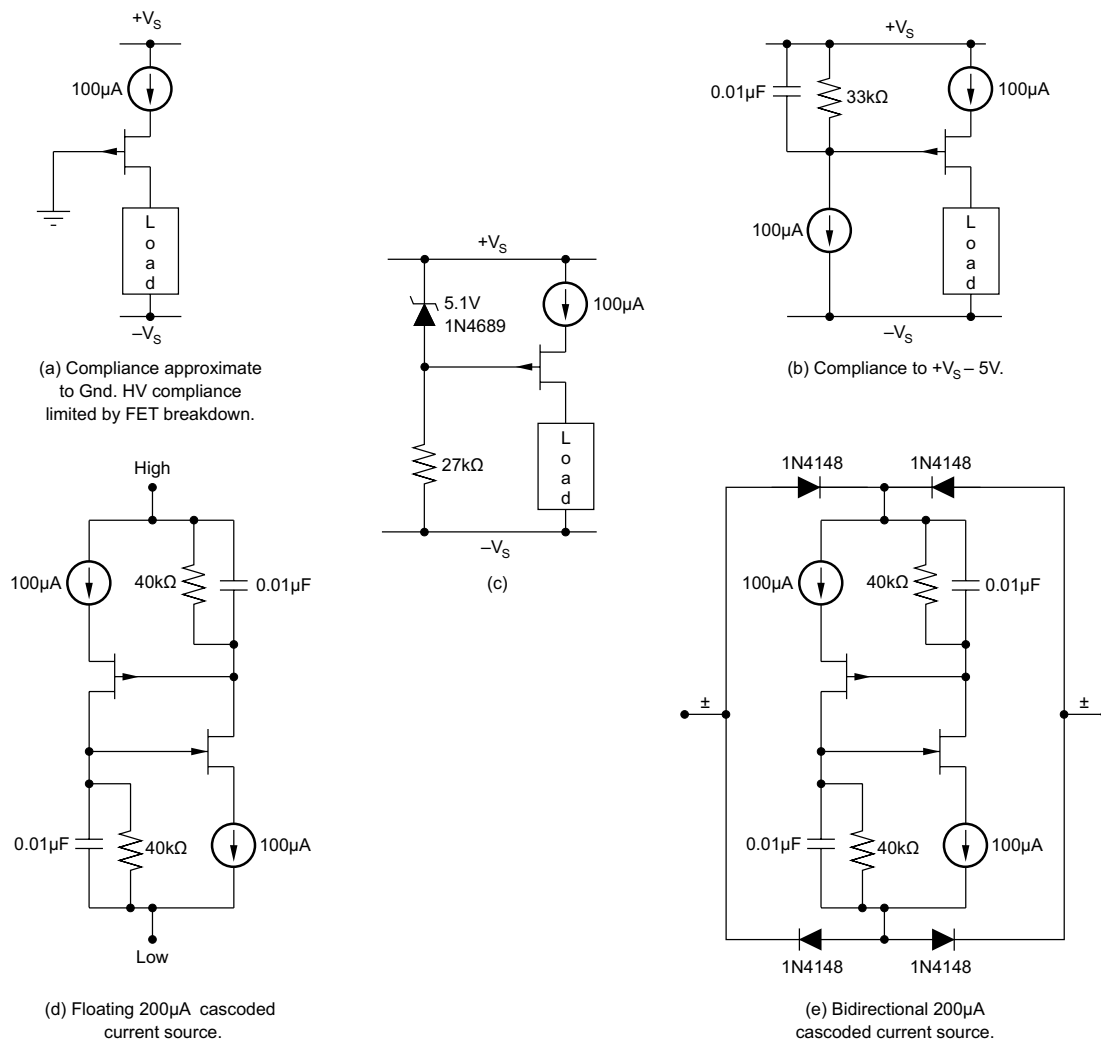


Figure 22. 100- $\mu$ A Current Source—80-V Compliance

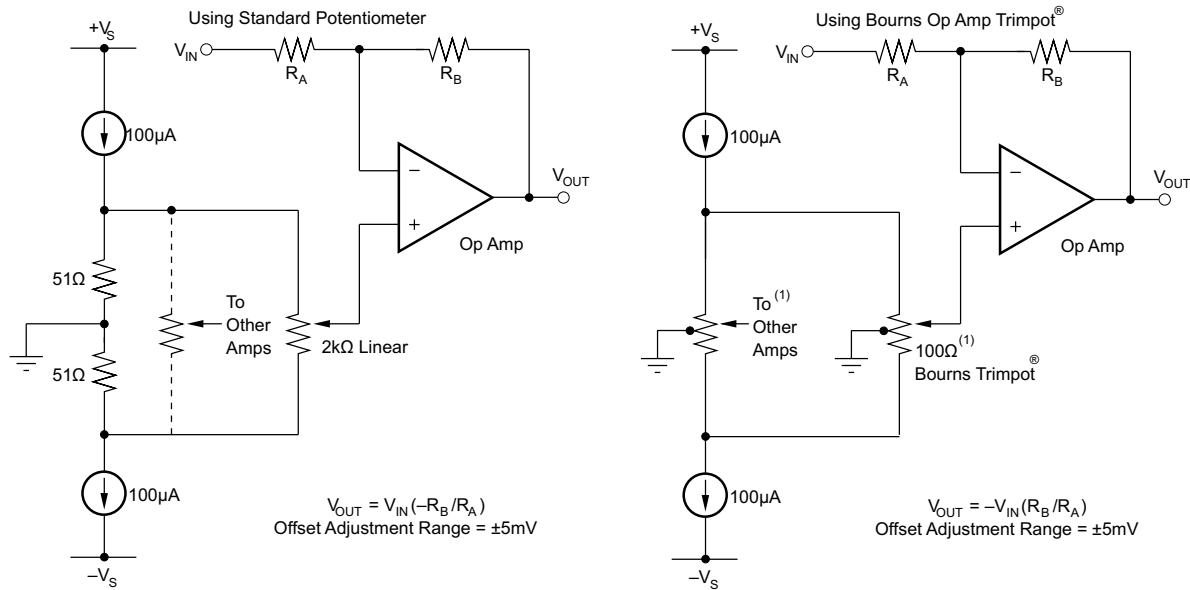
## System Examples (continued)



NOTES: (1) FET cascoded current sources offer improved output impedance and high frequency operation. Circuit in (b) also provides improved PSRR. (2) For current sinks (Circuits (a) and (b) only), invert circuits and use "N" channel JFETS.

**Figure 23. FET Cascode Circuits**

## System Examples (continued)



NOTE: (1) For N Op Amps, use Potentiometer Resistance =  $N \cdot 100\Omega$ .

**Figure 24. Operational Amplifier Offset Adjustment Circuits**

## System Examples (continued)

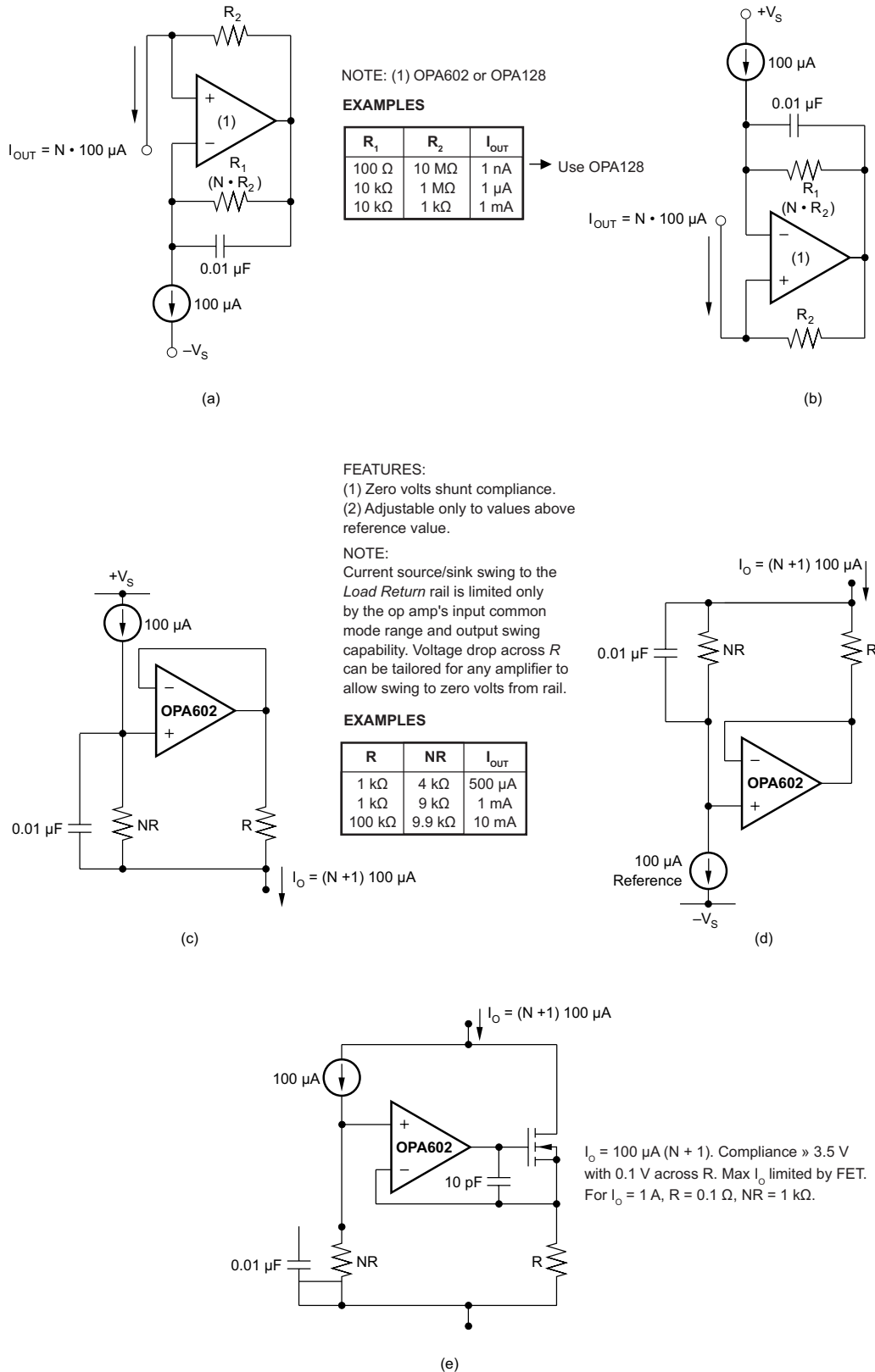


Figure 25. Adjustable Current Sources

## System Examples (continued)

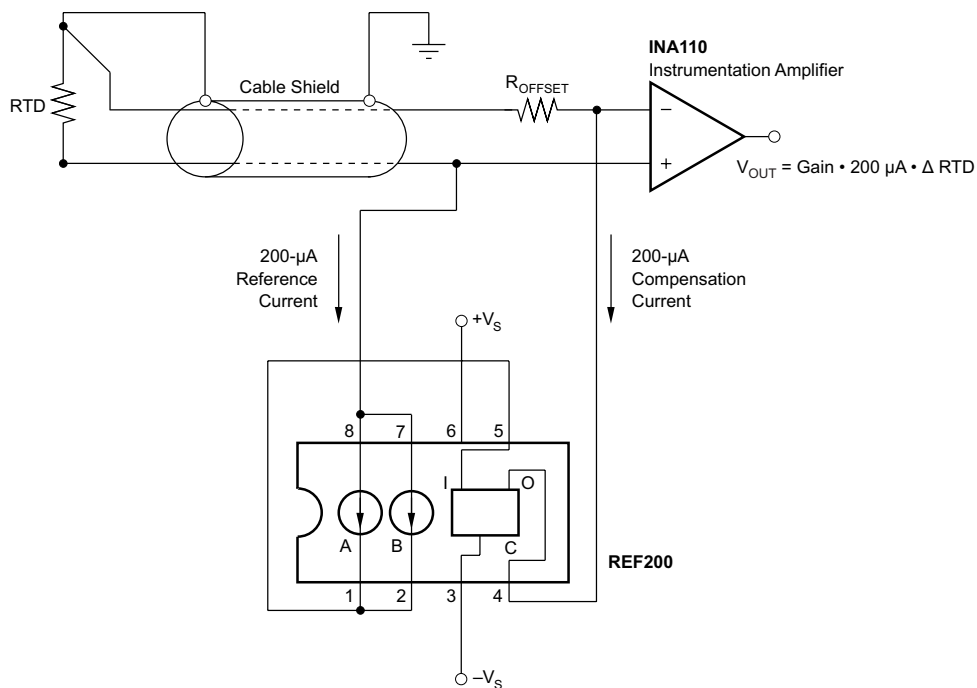
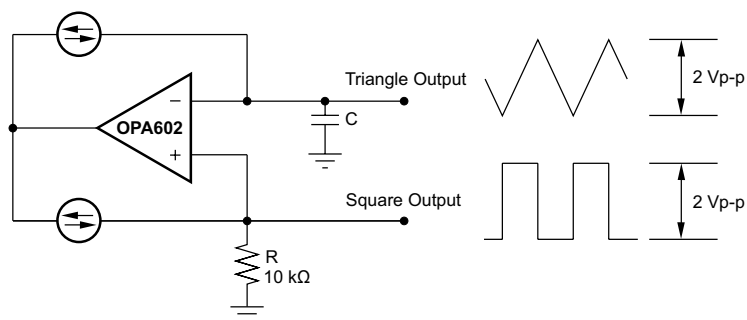


Figure 26. RTD Excitation With Three-Wire Lead Resistance Compensation



Frequency =  $1/4RC$  (Hz)  
Frequency =  $25/C$  (Hz)  
(C is in  $\mu\text{F}$  and R = 10 k $\Omega$ )

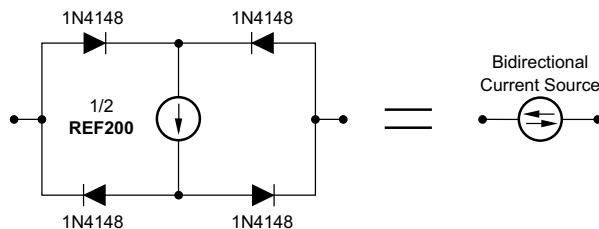
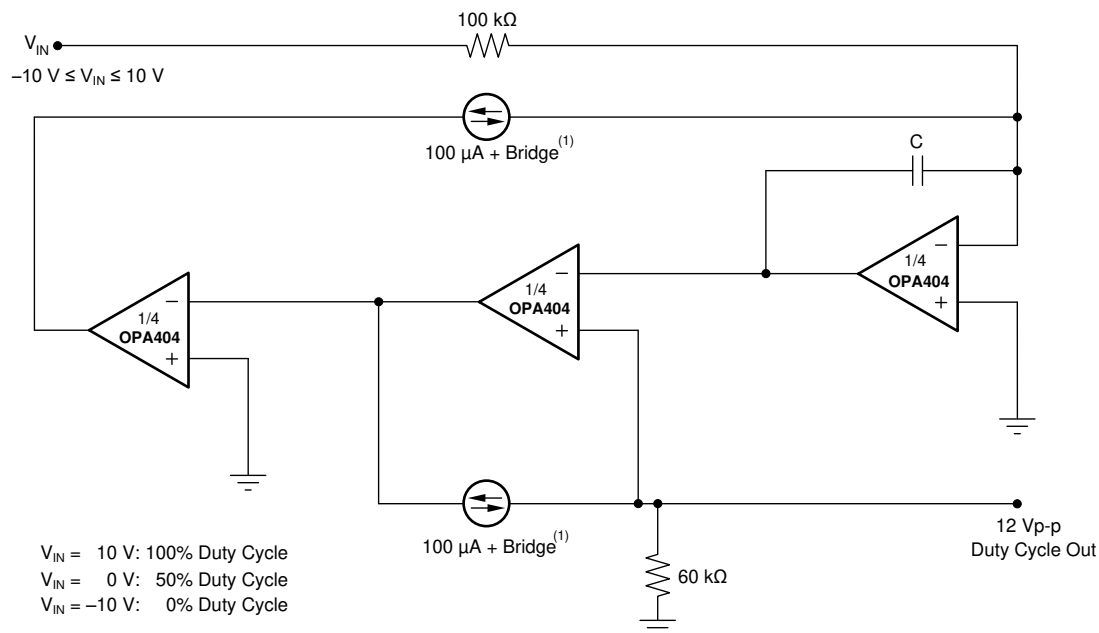


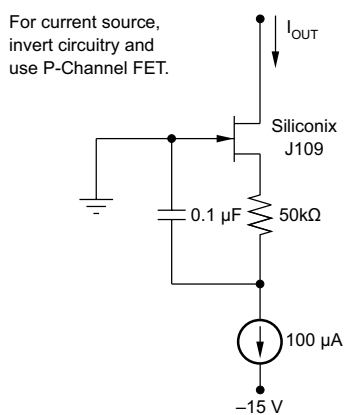
Figure 27. Precision Triangle Waveform Generator

## System Examples (continued)



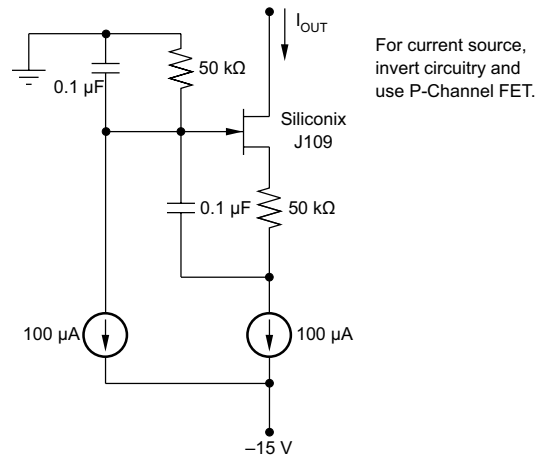
(1) See [Figure 27](#).

**Figure 28. Precision Duty-Cycle Modulator**

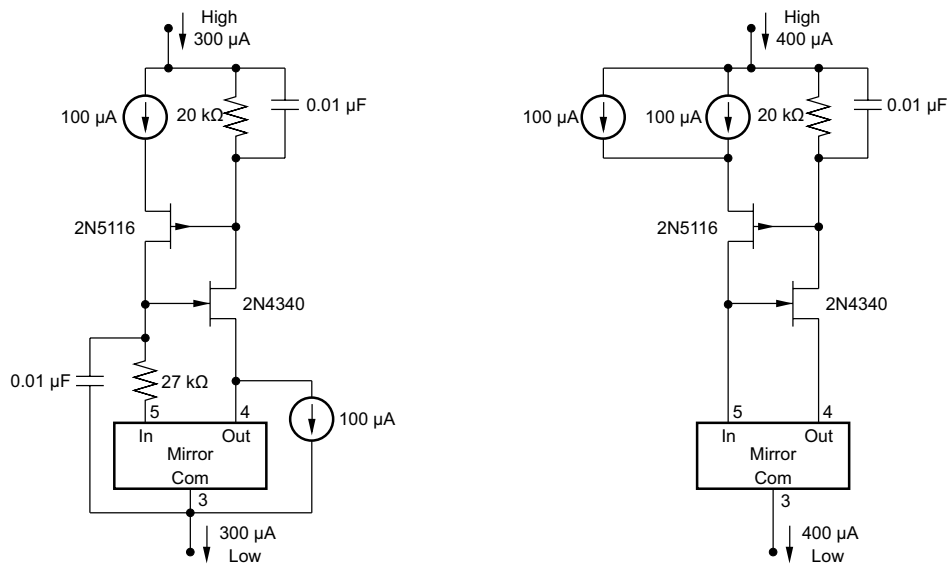


**Figure 29. Low Noise Current Sink**

## System Examples (continued)



**Figure 30. Low Noise Current Sink With Compliance Below Ground**

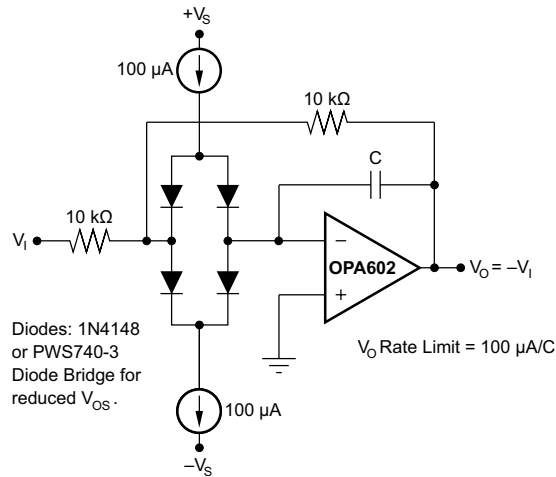


(a) Regulation (15 V to 30 V = 0.00003%/V (10 GW)

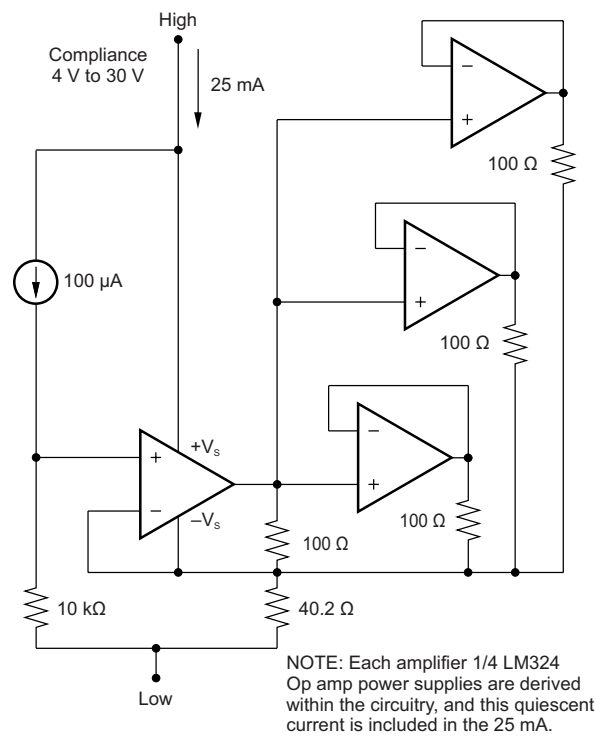
(a) Regulation (15 V to 30 V = 0.000025%/V (10 GW)

**Figure 31. Floating 300-μA and 400-μA Cascoded Current Sources**

## System Examples (continued)



### Figure 32. Rate Limiter



### Figure 33. 25-mA Floating Current Source

## System Examples (continued)

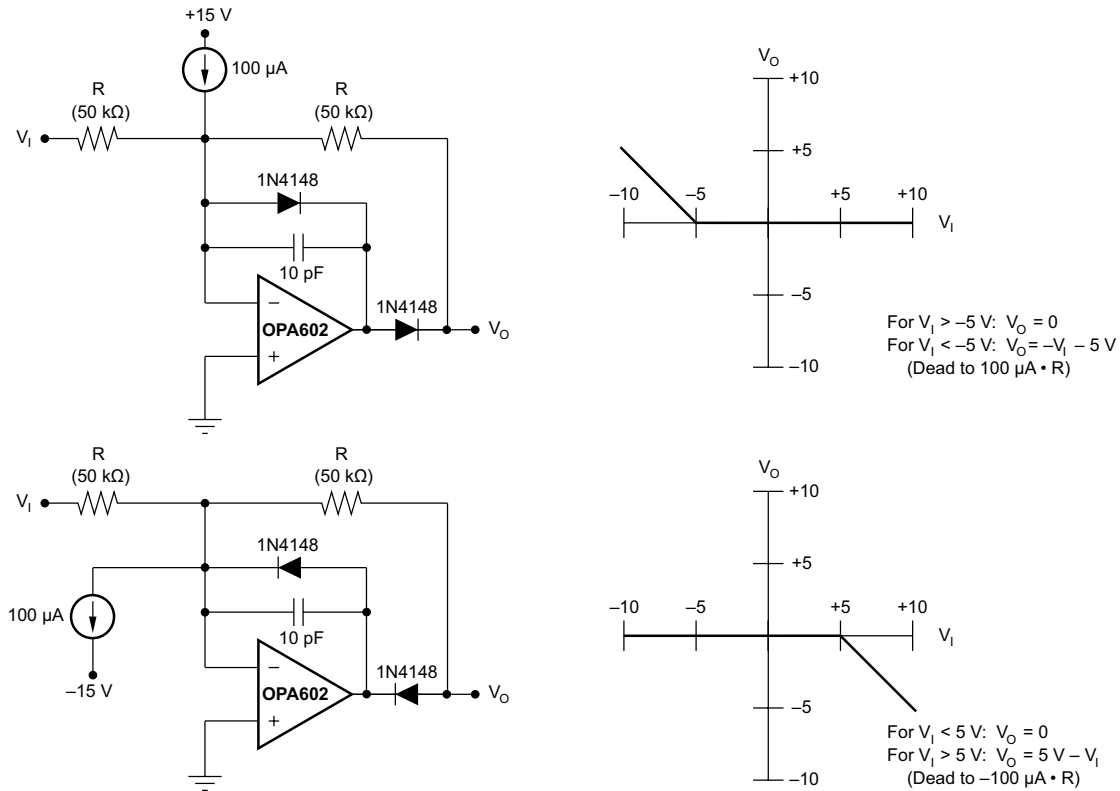
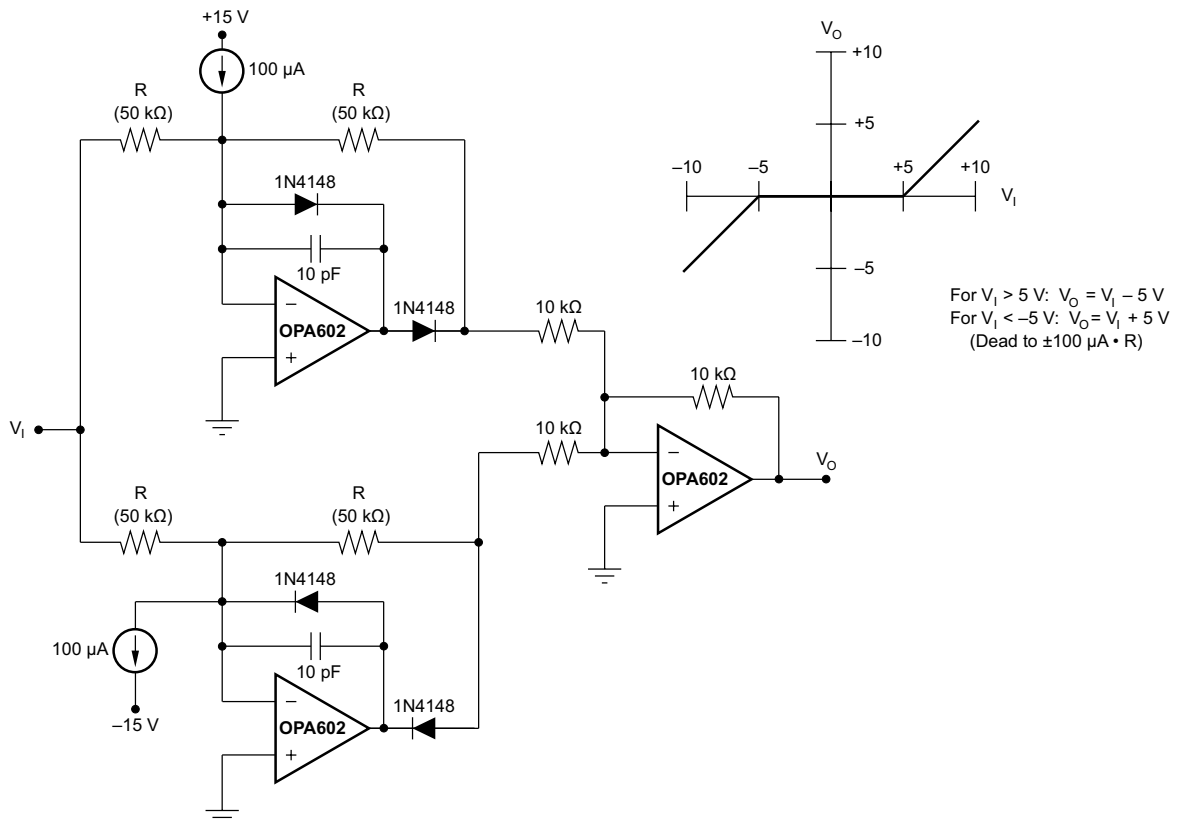
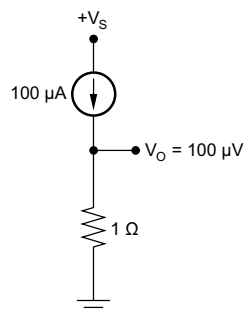


Figure 34. Dead-Band Circuit

## System Examples (continued)

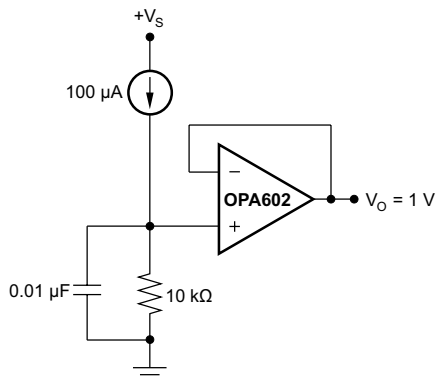


**Figure 35. Double Dead-Band Circuit**

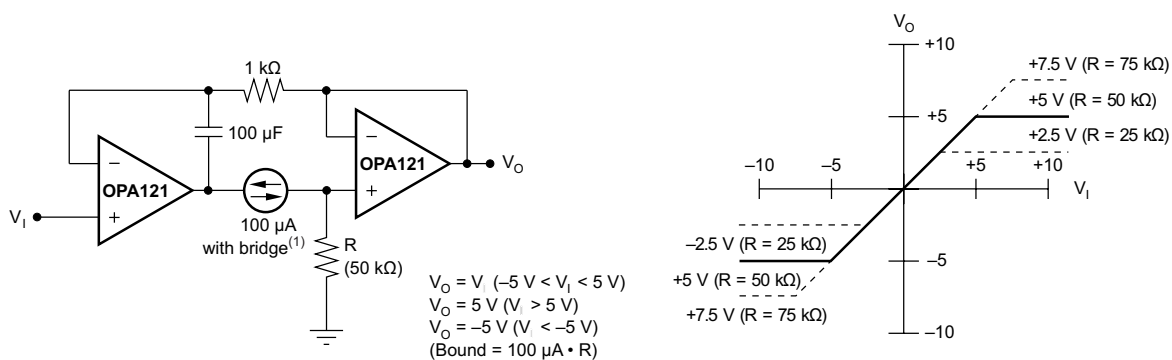


**Figure 36. Low-Voltage Reference**

## System Examples (continued)

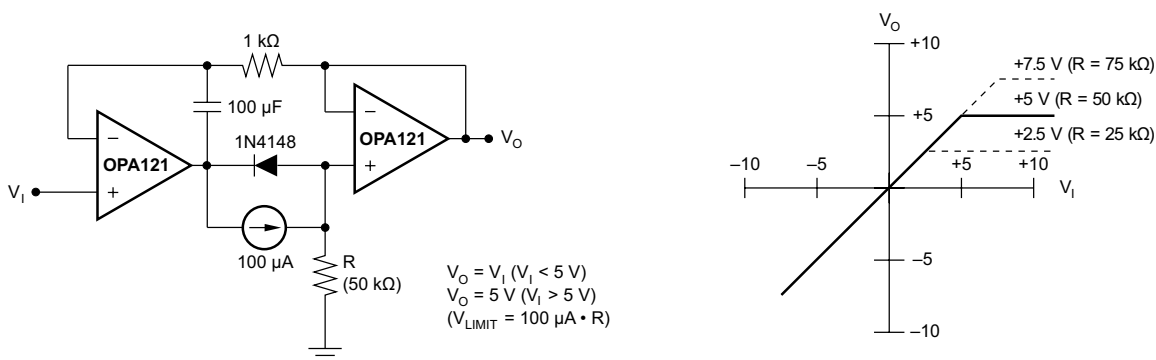


**Figure 37. Voltage Reference**



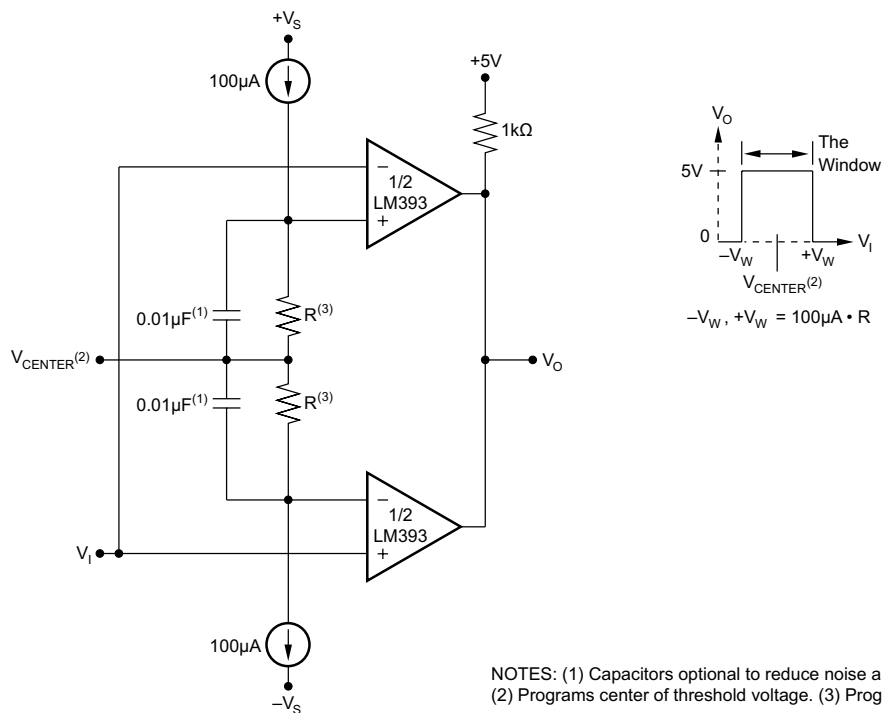
(1) See Figure 17.

**Figure 38. Bipolar Limiting Circuit**

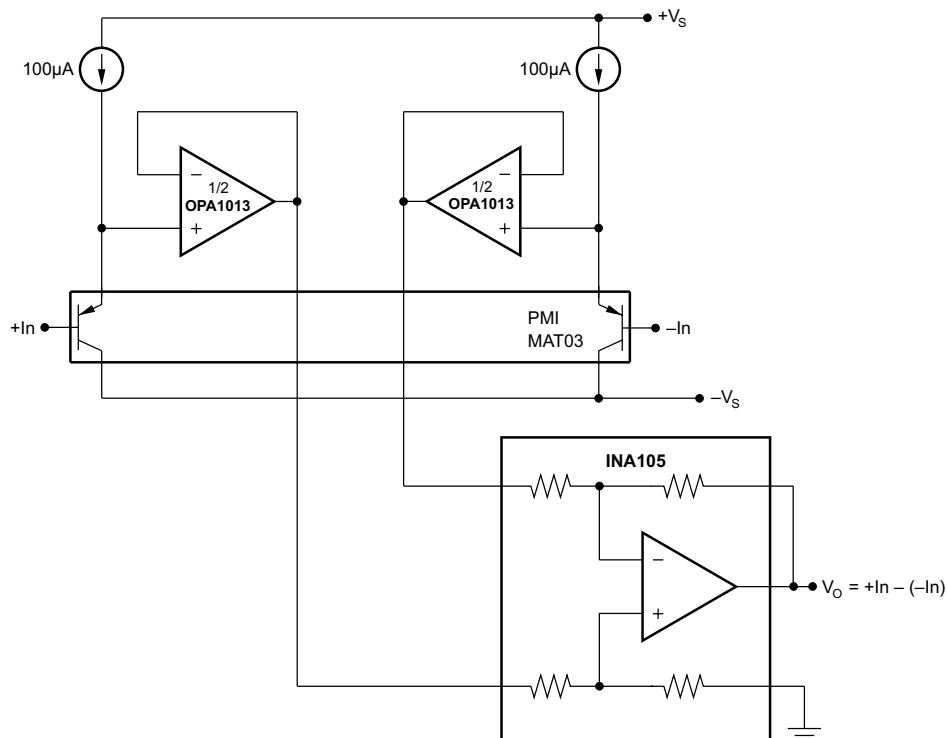


**Figure 39. Limiting Circuit**

## System Examples (continued)



**Figure 40. Window Comparator**



**Figure 41. Instrumentation Amplifier With Compliance to  $-V_S$**

## 9 Power Supply Recommendations

The REF200 device has completely floating current sources and current mirror. The REF200 device has a wide compliance voltage range from 2.5 V to 40 V.

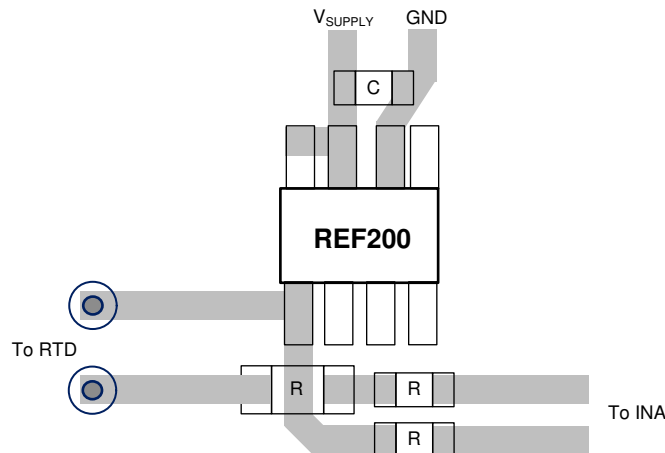
## 10 Layout

### 10.1 Layout Guidelines

Figure 42 illustrates an example of a printed-circuit-board (PCB) layout for a data acquisition system using the REF2030. Some key considerations are:

- Minimize trace lengths in the current source and current mirror paths to reduce impedance.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

### 10.2 Layout Example



**Figure 42. Example Layout of REF200 in a RTD Measurement System**

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

- *RTD to Voltage Reference Design Using Instrumentation Amplifier and Current Reference*, [TIDU969](#)
- *Implementation and Applications of Current Sources and Current Receivers*, [SBOA046](#)

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">REF200AU</a>     | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -25 to 85    | REF<br>200U         |
| REF200AU.B                   | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -25 to 85    | REF<br>200U         |
| <a href="#">REF200AU/2K5</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -25 to 85    | REF<br>200U         |
| REF200AU/2K5.B               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -25 to 85    | REF<br>200U         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

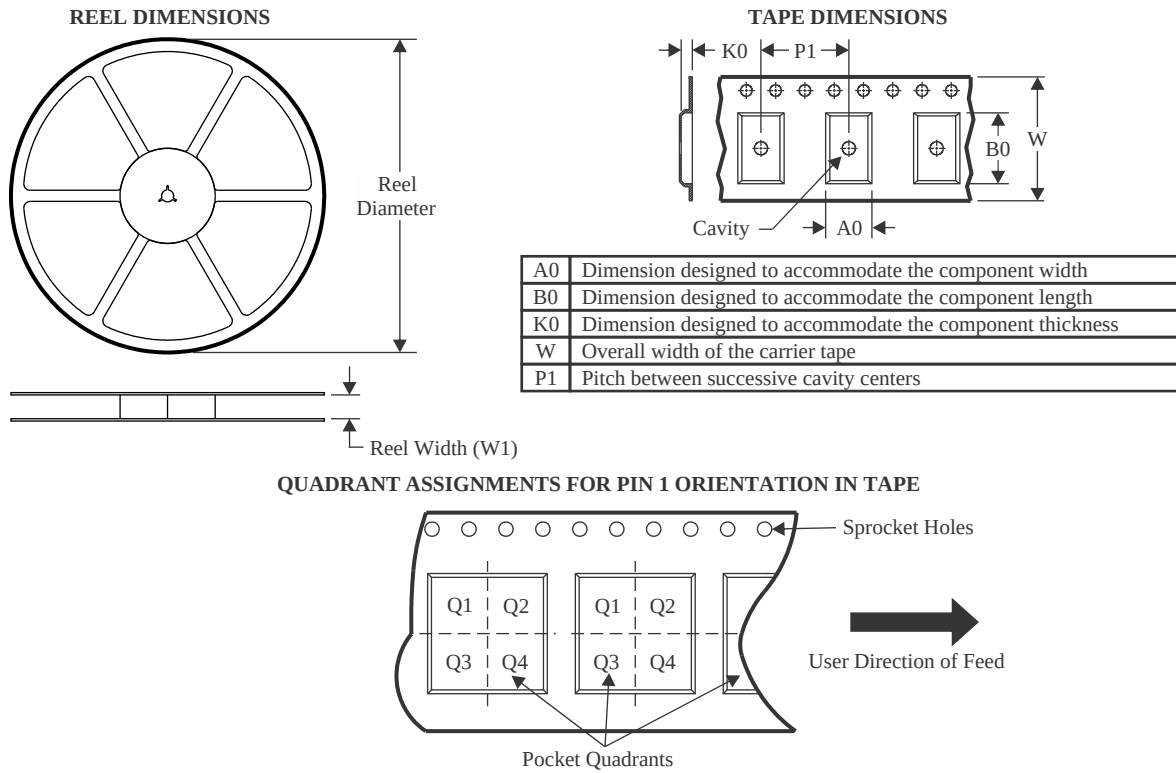
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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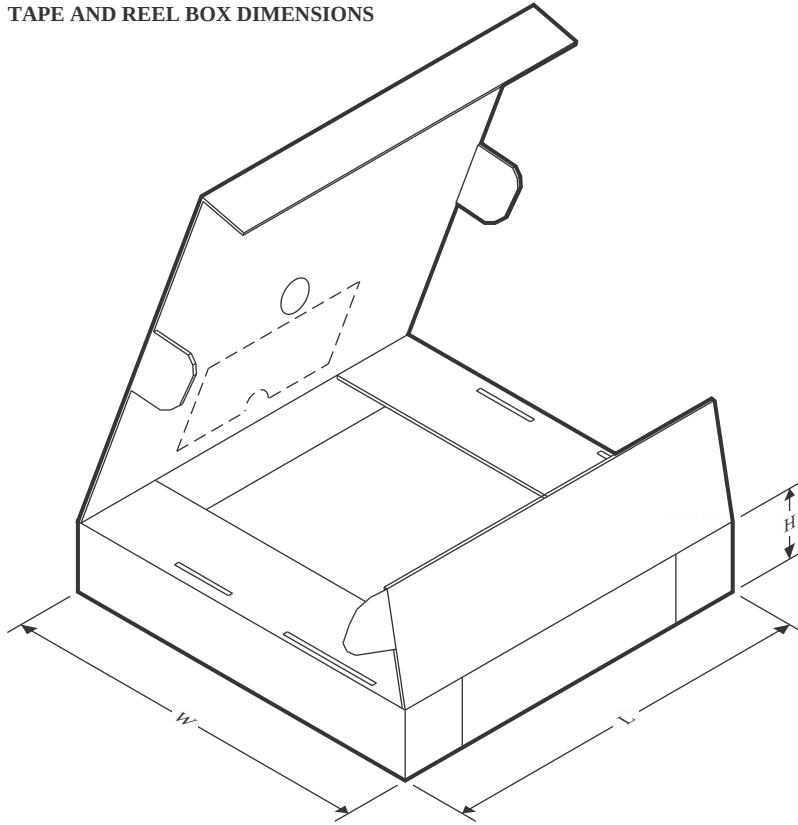
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| REF200AU/2K5 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

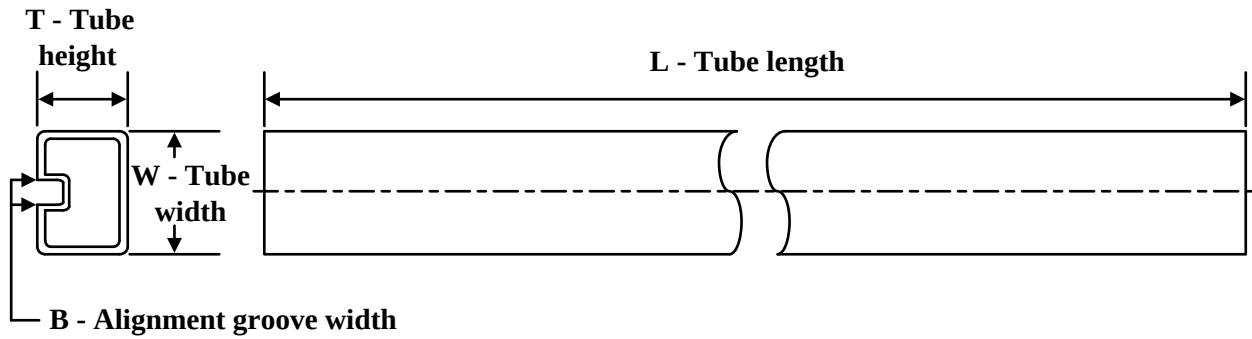
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| REF200AU/2K5 | SOIC         | D               | 8    | 2500 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device     | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| REF200AU   | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| REF200AU.B | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |



## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



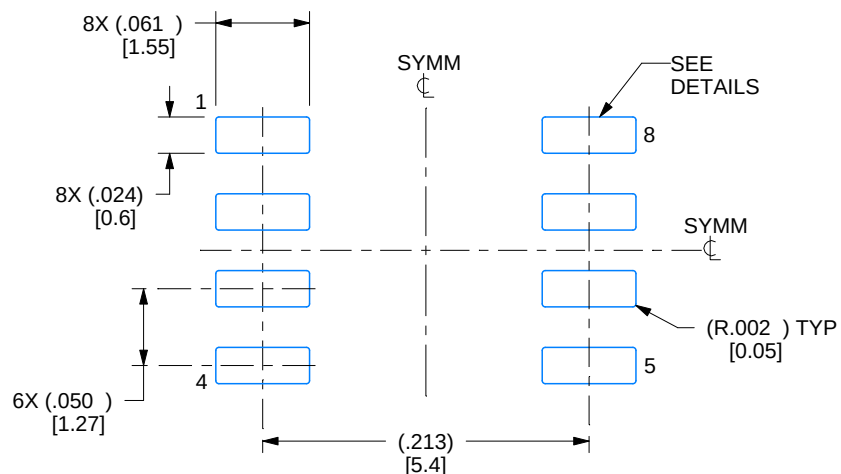
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

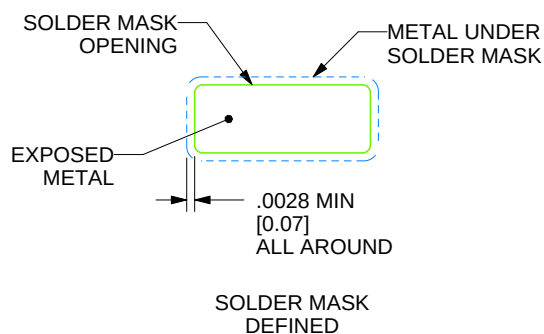
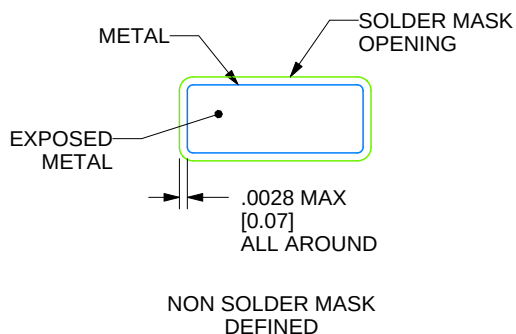
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

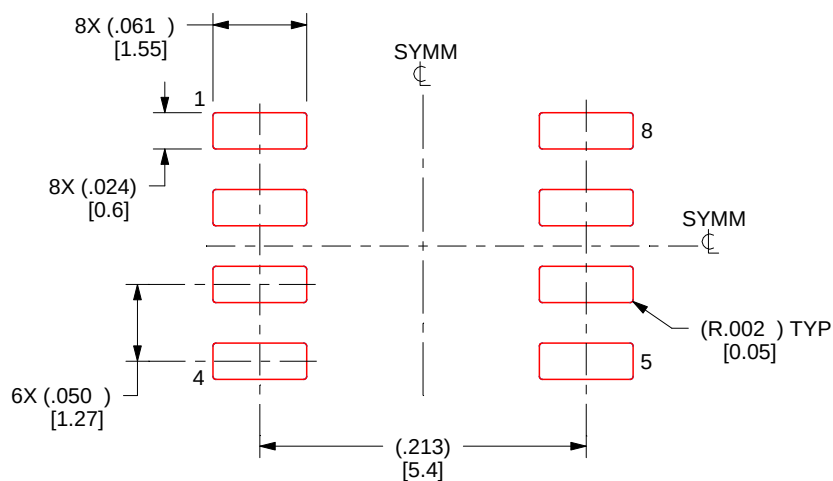
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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