

# DRV8317 Three-Phase PWM Motor Driver

## 1 Features

- Three-phase BLDC motor driver
  - Configurable slew rate for EMI mitigation
  - Programmable gain current sensing
  - Supports up to 200-kHz PWM frequency
  - Integrated shoot through protection
- 4.5-V to 20-V operating voltage
  - 24-V absolute maximum voltage
- High output current capability
  - 5-A peak current drive
- Low on-state resistance MOSFETs
  - $R_{DS(ON)}$  (HS + LS) at  $T_A = 25^\circ\text{C}$  : 130-m $\Omega$  (typical)
- Ultra-low Q-current sleep mode
  - 3- $\mu\text{A}$  (max.) at  $V_{VM} = 12\text{-V}$ ,  $T_A = 25^\circ\text{C}$
- Multiple control interface options
  - 6x PWM control interface
  - 3x PWM control interface
- Integrated current sensing
  - No external current sense resistor required
  - Three-phase current sense outputs
- SPI and hardware device variants
  - 10-MHz SPI interface variant for flexibility
  - Pin configurable variant for simplicity
- Supports 1.8-V, 3.3-V, and 5-V logic inputs
- Built-in 3.3-V  $\pm$  4.5%, 80-mA LDO regulator
- Integrated protection features
  - VM under voltage lockout (UVLO)
  - VM over voltage protection (OVP)
  - Charge pump under voltage (CPUV)
  - Over current protection (OCP)
  - Over temperature warning and shutdown (OTW/OTS)
  - Fault condition indication pin (nFAULT)

## 2 Applications

- **Brushless-DC (BLDC) Motor Modules**
- **Air Purifiers**
- **Dishwasher Pumps**
- **Vacuum Robots**
- **Washer and Dryer Pumps**
- **Drones and Hand-held Gimbals**
- **Laptop, Desktop, and Server Fans**
- **Coffee Machines**

## 3 Description

DRV8317 provides three integrated MOSFET half-bridges for driving three-phase brushless DC (BLDC) motors with 5-V, 9-V, 12-V, or 18-V DC rails or 2s to 4s batteries. The device provides integrated three-phase current sensing which eliminates the need for external sense resistors. DRV8317 has an integrated LDO that provides a regulated 3.3-V rail capable of delivering up to 80mA for external loads like MCU, logic circuits, hall sensors etc.,

DRV8317 provides a configurable 6x or 3x PWM control scheme which can be used to implement sensed or sensorless field-oriented control (FOC), sinusoidal control, or trapezoidal control using an external microcontroller. DRV8317 is capable of driving a PWM frequency of up to 200 kHz. DRV8317 is highly configurable either through SPI (DRV8317S) or pins (DRV8317H) - PWM mode, slew rate, current sense gain are some of the configurable features.

A number of protection features including supply under voltage lockout (UVLO), over voltage protection (OVP), charge pump under voltage (CPUV), over current protection (OCP), over temperature warning (OTW) and over temperature shutdown (OTS) are integrated into DRV8317 to protect the device, motor, and system against fault events. Fault conditions are indicated by the nFAULT pin.

### Device Variant Information<sup>(1)</sup>

| PART NUMBER             | PACKAGE   | BODY SIZE (NOM)          |
|-------------------------|-----------|--------------------------|
| DRV8317S <sup>(2)</sup> | WQFN (36) | 5.00 mm $\times$ 4.00 mm |
| DRV8317H                | WQFN (36) | 5.00 mm $\times$ 4.00 mm |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) Device available for preview only.

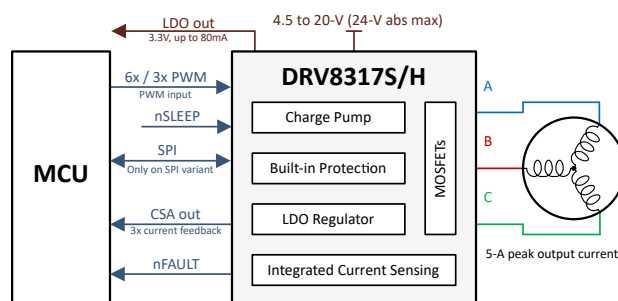


**Figure 3-1. DRV8317S/H Simplified Schematic**



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## 4 Revision History

| DATE       | REVISION | NOTES           |
|------------|----------|-----------------|
| April 2022 | *        | Initial release |

## 5 Device Comparison Table

| DEVICE   | PACKAGES                  | INTERFACE      |
|----------|---------------------------|----------------|
| DRV8317S | 36-pin WQFN (5-mm x 4-mm) | SPI            |
| DRV8317H |                           | Hardware (Pin) |

**Table 5-1. DRV8317S vs DRV8317H Configuration Comparison**

| Parameters                                    | DRV8317S                                                                                                                                                              | DRV8317H                                                                                                    |
|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|
| PWM control mode                              | PWM_MODE (4 settings)                                                                                                                                                 | MODE pin (2 settings)                                                                                       |
| Slew rate                                     | SLEW_RATE (4 settings)                                                                                                                                                | SLEW pin (4 settings)                                                                                       |
| Current sense amplifier gain                  | CSA_GAIN (4 settings)                                                                                                                                                 | GAIN pin (4 settings)                                                                                       |
| OCP blanking time                             | OCP_TBLANK (4 settings)                                                                                                                                               | Fixed to 0.7-μs                                                                                             |
| OCP deglitch time                             | OCP_DEG (4 settings)                                                                                                                                                  | Fixed to 0.6-μs                                                                                             |
| OCP mode                                      | OCP_MODE (4 settings), Configurable retry time                                                                                                                        | 5-ms automatic retry                                                                                        |
| Dead time                                     | Fixed based on SLEW_RATE setting                                                                                                                                      | Fixed based on SLEW pin setting                                                                             |
| Propagation delay                             | Fixed based on SLEW_RATE setting                                                                                                                                      | Fixed based on SLEW pin setting                                                                             |
| Driver delay compensation                     | DLYCMP_EN (2 settings)                                                                                                                                                | Disabled                                                                                                    |
| Spread Spectrum Clock for internal oscillator | SSC_DIS (2 settings)                                                                                                                                                  | Enabled                                                                                                     |
| VM under voltage lockout                      | VM under voltage protection always enabled. VM under voltage protection mode set by UVP_MODE (2 settings); configurable retry time using SLOW_TRETRY and FAST_TRETRY. | VM under voltage protection always enabled. Auto-retry mode for VM under voltage with 5-ms retry time.      |
| VIN_AVDD, AVDD under voltage lockout          | VIN_AVDD and AVDD under voltage protection always enabled. Device resets on VIN_AVDD or AVDD under voltage.                                                           | VIN_AVDD and AVDD under voltage protection always enabled. Device resets on VIN_AVDD or AVDD under voltage. |
| CP under voltage lockout                      | CP under voltage protection always enabled. CP under voltage protection mode set by UVP_MODE (2 settings); configurable retry time using SLOW_TRETRY and FAST_TRETRY. | CP under voltage protection always enabled. Auto-retry mode for CP under voltage with 5-ms retry time.      |
| VM over voltage                               | OVP_MODE (2 settings); configurable retry time using SLOW_TRETRY and FAST_TRETRY                                                                                      | 5-ms automatic retry                                                                                        |
| SPI fault                                     | SPIFLT_MODE (2 settings)                                                                                                                                              | N/A                                                                                                         |
| FET over temperature warning (OTW_FET)        | Enable/disable using OTW_FET_EN. If enabled, over temperature warning is reported on nFAULT pin and OTW_FET bit in OT_STS register.                                   | Disabled                                                                                                    |
| FET over temperature shutdown (OTS_FET)       | OTF_MODE (2 settings); configurable retry time using SLOW_TRETRY and FAST_TRETRY                                                                                      | 5-ms automatic retry                                                                                        |

## 6 Pin Configuration and Functions

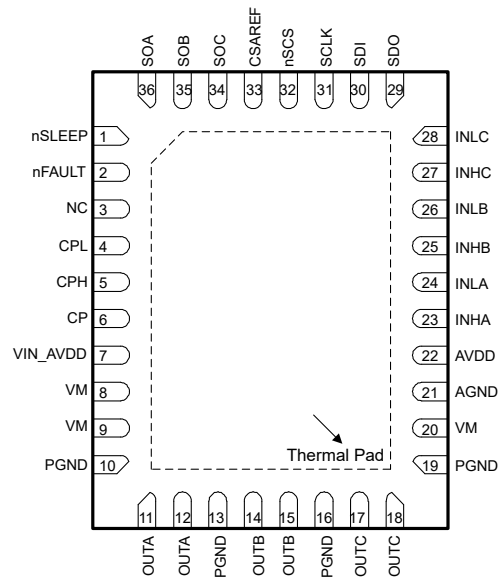


Figure 6-1. DRV8317S 36-Pin WQFN With Exposed Thermal Pad Top View

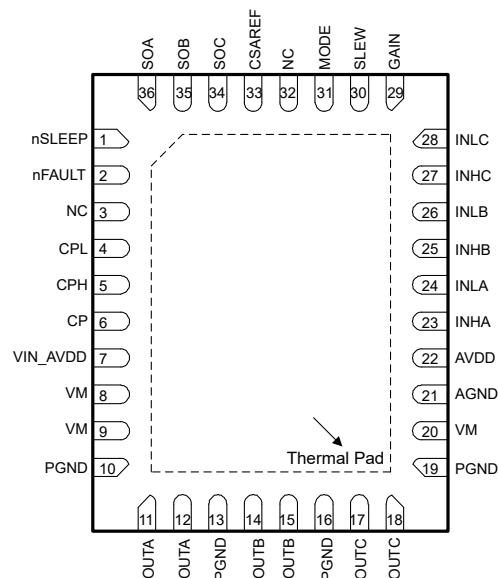


Figure 6-2. DRV8317H 36-Pin WQFN With Exposed Thermal Pad Top View

Table 6-1. Pin Functions

| PIN<br>NAME | 36-pin package |          | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                  |
|-------------|----------------|----------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|             | DRV8317S       | DRV8317H |                     |                                                                                                                                                                                                              |
| AGND        | 21             | 21       | GND                 | Device analog ground. Connect to a separate ground plane. <sup>(1)</sup>                                                                                                                                     |
| AVDD        | 22             | 22       | PWR O               | 3.3V regulator output. Connect a X5R or X7R, 2.2-μF (no load) or 4.7-μF (up to 80mA load), 6.3-V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 80 mA for external loads. |
| CP          | 6              | 6        | PWR                 | Charge pump output. Connect a X5R or X7R, 1-μF, 16-V ceramic capacitor between the CP and VM pins.                                                                                                           |
| CPH         | 5              | 5        | PWR                 | Charge pump switching node. Connect a X5R or X7R, 100-nF, (2xVM)- rated ceramic capacitor between the CPH and CPL pins.                                                                                      |
| CPL         | 4              | 4        | PWR                 |                                                                                                                                                                                                              |

**Table 6-1. Pin Functions (continued)**

| PIN<br>NAME | 36-pin package |                | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                              |
|-------------|----------------|----------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|             | DRV8317S       | DRV8317H       |                     |                                                                                                                                                                                                                                          |
| CSAREF      | 33             | 33             | PWR I               | Current sense amplifier power supply input/reference. Connect a X5R or X7R, 0.1- $\mu$ F, 6.3-V ceramic capacitor between the CSAREF and AGND pins.                                                                                      |
| GAIN        | —              | 29             | I                   | Available only in hardware variant (DRV8317H). The pin is a 4-level input pin for current sense amplifier gain setting.                                                                                                                  |
| INHA        | 23             | 23             | I                   | High-side driver control input for OUTA. This pin controls the state of the high-side MOSFET in 6x/3x PWM Mode.                                                                                                                          |
| INHB        | 25             | 25             | I                   | High-side driver control input for OUTB. This pin controls the state of the high-side MOSFET in 6x/3x PWM Mode.                                                                                                                          |
| INHC        | 27             | 27             | I                   | High-side driver control input for OUTC. This pin controls the state of the high-side MOSFET in 6x/3x PWM Mode.                                                                                                                          |
| INLA        | 24             | 24             | I                   | Low-side driver control input for OUTA. This pin controls the state of the low-side MOSFET in 6x PWM Mode.                                                                                                                               |
| INLB        | 26             | 26             | I                   | Low-side driver control input for OUTB. This pin controls the state of the low-side MOSFET in 6x PWM Mode.                                                                                                                               |
| INLC        | 28             | 28             | I                   | Low-side driver control input for OUTC. This pin controls the state of the low-side MOSFET in 6x PWM Mode.                                                                                                                               |
| MODE        | —              | 31             | I                   | Available only in hardware variant (DRV8317H). This is a 4-level input pin for PWM mode setting.                                                                                                                                         |
| NC          | 3              | 3, 32          | —                   | No connect. Leave the pin floating.                                                                                                                                                                                                      |
| nFAULT      | 2              | 2              | O                   | Fault indication pin. Pulled low during fault condition. Open-drain output; requires an external pull-up resistor to AVDD.                                                                                                               |
| nSCS        | 32             | —              | I                   | Available only in SPI variant (DRV8317S). Serial chip select. A logic low on this pin enables serial interface communication.                                                                                                            |
| nSLEEP      | 1              | 1              | I                   | When this pin is logic low the device goes to a low-power sleep mode. A 15 to 50- $\mu$ s low pulse on nSLEEP pin can be used to reset fault conditions without entering sleep mode.                                                     |
| OUTA        | 11, 12         | 11, 12         | O                   | Half-bridge output A. Connect to motor winding.                                                                                                                                                                                          |
| OUTB        | 14, 15         | 14, 15         | O                   | Half-bridge output B. Connect to motor winding.                                                                                                                                                                                          |
| OUTC        | 17, 18         | 17, 18         | O                   | Half-bridge output C. Connect to motor winding.                                                                                                                                                                                          |
| PGND        | 10, 13, 16, 19 | 10, 13, 16, 19 | PWR                 | Device power ground. Connect to a separate ground plane. <sup>(1)</sup>                                                                                                                                                                  |
| SCLK        | 31             | —              | I                   | Available only in SPI variant (DRV8317S). Serial clock input. Serial data is shifted out on the rising edge and captured on the falling edge of SCLK.                                                                                    |
| SDI         | 30             | —              | I                   | Available only in SPI variant (DRV8317S). Serial data input. Data (input) is captured on the falling edge of the SCLK pin (SPI devices).                                                                                                 |
| SDO         | 29             | —              | O                   | Available only in SPI variant (DRV8317S). Serial data output. Data (output) is shifted out on the rising edge of the SCLK pin.                                                                                                           |
| SLEW        | —              | 30             | I                   | Available only in hardware variant (DRV8317H). This pin is a 4-level input pin for OUTx voltage slew rate setting.                                                                                                                       |
| SOA         | 36             | 36             | O                   | Current sense amplifier output for OUTA.                                                                                                                                                                                                 |
| SOB         | 35             | 35             | O                   | Current sense amplifier output for OUTB.                                                                                                                                                                                                 |
| SOC         | 34             | 34             | O                   | Current sense amplifier output for OUTC.                                                                                                                                                                                                 |
| VIN_AVDD    | 7              | 7              | PWR                 | Input supply for AVDD LDO                                                                                                                                                                                                                |
| VM          | 8, 9, 20       | 8, 9, 20       | PWR                 | Device and motor power supply. Connect to motor supply voltage; bypass to PGND with a 0.1- $\mu$ F capacitor plus one bulk capacitor. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device |
| Thermal pad |                |                | PWR                 | Must be connected to AGND.                                                                                                                                                                                                               |

(1) I = input, O = output, PWR = power, GND = ground, NC = no connect

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                                                 | MIN  | MAX                               | UNIT |
|---------------------------------------------------------------------------------|------|-----------------------------------|------|
| Power supply pin voltage (VM, VIN_AVDD)                                         | −0.3 | 24                                | V    |
| Power supply voltage ramp during power up (VM)                                  |      | 2                                 | V/μs |
| Voltage difference between ground pins (PGND, AGND)                             | −0.3 | 0.3                               | V    |
| Charge pump voltage (CP)                                                        | −0.3 | V <sub>M</sub> + 6                | V    |
| Analog regulator pin voltage (AVDD)                                             | −0.3 | 4                                 | V    |
| Logic pin input voltage (INHx, INLx, nSCS, nSLEEP, SCLK, SDI, GAIN, MODE, SLEW) | −0.3 | 6                                 | V    |
| Logic pin output voltage (SDO)                                                  | −0.3 | 6                                 | V    |
| Open drain pin output voltage (nFAULT)                                          | −0.3 | 6                                 | V    |
| Open drain output current range (nFAULT)                                        | 0    | 5                                 | mA   |
| Current sense amplifier reference supply input (CSAREF)                         | −0.3 | 4                                 | V    |
| Current sense amplifier output (SOx)                                            | −0.3 | 4                                 | V    |
| Output pin voltage (OUTA, OUTB, OUTC)                                           | −1   | V <sub>M</sub> + 1 <sup>(2)</sup> | V    |
| Ambient temperature, T <sub>A</sub>                                             | −40  | 125                               | °C   |
| Junction temperature, T <sub>J</sub>                                            | −40  | 150                               | °C   |
| Storage temperature, T <sub>stg</sub>                                           | −65  | 150                               | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
- (2) Maximum voltage supported on OUTx pin is 24V

### 7.2 ESD Ratings

|                    |                         | VALUE                                                                          | UNIT  |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2500 |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±750  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

|                                 |                                      |                                                 | MIN  | NOM | MAX | UNIT |
|---------------------------------|--------------------------------------|-------------------------------------------------|------|-----|-----|------|
| V <sub>VM</sub>                 | Power supply voltage                 | V <sub>VM</sub> , V <sub>VIN_AVDD</sub>         | 4.5  | 12  | 20  | V    |
| I <sub>OUT</sub> <sup>(1)</sup> | Peak output winding current          | V <sub>VM</sub> ≥ 6 V, OUTA, OUTB, OUTC         |      |     | 5   | A    |
|                                 |                                      | 4.5 V ≤ V <sub>VM</sub> < 6 V, OUTA, OUTB, OUTC |      |     | 3   | A    |
| V <sub>OD</sub>                 | Open drain pullup voltage            | nFAULT                                          | −0.3 |     | 5.5 | V    |
| I <sub>OD</sub>                 | Open drain output current capability | nFAULT                                          |      |     | 5   | mA   |
| T <sub>A</sub>                  | Operating ambient temperature        |                                                 | −40  |     | 125 | °C   |
| T <sub>J</sub>                  | Operating Junction temperature       |                                                 | −40  |     | 150 | °C   |

- (1) Power dissipation and thermal limits must be observed

## 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                                                            | DRV8317    | UNIT |
|-------------------------------|----------------------------------------------------------------------------|------------|------|
|                               |                                                                            | REE (WQFN) |      |
|                               |                                                                            | 36         |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance (JEDEC 4-layer PCB, 6 thermal vias) | 36.4       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance                                  | 23.7       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance                                       | 14         | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter                                 | 0.6        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter                               | 14         | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance                               | 4.1        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

T<sub>J</sub> = –40°C to +150°C, V<sub>VM</sub> = 4.5 to 20 V (unless otherwise noted). Typical limits apply for T<sub>A</sub> = 25°C, V<sub>VM</sub> = 12 V

| PARAMETER                                   |                                | TEST CONDITIONS                                                                                  | MIN  | TYP      | MAX  | UNIT |
|---------------------------------------------|--------------------------------|--------------------------------------------------------------------------------------------------|------|----------|------|------|
| <b>POWER SUPPLIES</b>                       |                                |                                                                                                  |      |          |      |      |
| I <sub>VMQ</sub>                            | VM sleep mode current          | V <sub>VM</sub> = 12 V, nSLEEP = 0, T <sub>A</sub> = 25 °C                                       |      | 1.7      | 3    | μA   |
|                                             |                                | nSLEEP = 0, T <sub>A</sub> = 125 °C                                                              |      |          | 10   | μA   |
| I <sub>VMS</sub>                            | VM standby mode current        | V <sub>VM</sub> = 12 V, nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF', T <sub>A</sub> = 25 °C         |      | 8        | 10   | mA   |
|                                             |                                | nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF'                                                         |      | 8        | 10   | mA   |
| I <sub>VM</sub>                             | VM operating mode current      | V <sub>VM</sub> = 12 V, nSLEEP = 1, f <sub>PWM</sub> = 25 kHz, T <sub>A</sub> = 25 °C            |      | 10       | 12   | mA   |
|                                             |                                | V <sub>VM</sub> = 12 V, nSLEEP = 1, f <sub>PWM</sub> = 200 kHz, T <sub>A</sub> = 25 °C           |      | 10       | 14   | mA   |
|                                             |                                | nSLEEP = 1, f <sub>PWM</sub> = 25 kHz                                                            |      | 10       | 12   | mA   |
|                                             |                                | nSLEEP = 1, f <sub>PWM</sub> = 200 kHz                                                           |      | 10       | 15   | mA   |
| V <sub>AVDD</sub>                           | Analog regulator voltage       | V <sub>VM</sub> ≥ 6V, V <sub>VIN_AVDD</sub> ≥ 6V, 0 mA ≤ I <sub>AVDD</sub> ≤ 80 mA               | 3.15 | 3.3      | 3.45 | V    |
| V <sub>AVDD</sub>                           | Analog regulator voltage       | 4.5V ≤ V <sub>VM</sub> < 6V, 4.5V ≤ V <sub>VIN_AVDD</sub> < 6V, 0 mA ≤ I <sub>AVDD</sub> ≤ 80 mA | 3.15 | 3.3      | 3.45 | V    |
| I <sub>AVDD</sub>                           | Analog regulator external load | 4.5V ≤ V <sub>VM</sub> < 6V, 4.5V ≤ V <sub>VIN_AVDD</sub> < 6V                                   |      |          | 80   | mA   |
| I <sub>AVDD</sub>                           | Analog regulator external load | V <sub>VM</sub> ≥ 6V, V <sub>VIN_AVDD</sub> ≥ 6V                                                 |      |          | 80   | mA   |
| I <sub>AVDD_LIM</sub>                       | Analog regulator current limit | V <sub>AVDD</sub> ≥ 2.7V, soft short to GND                                                      | 100  | 125      | 150  | mA   |
| C <sub>AVDD</sub>                           | Capacitance for AVDD           | External load I <sub>AVDD</sub> = 0 mA                                                           | 0.5  | 2.2      | 7.05 | μF   |
|                                             |                                | External load 0mA ≤ I <sub>AVDD</sub> ≤ 80 mA                                                    | 2.35 | 4.7      | 7.05 | μF   |
| V <sub>CP</sub>                             | Charge pump regulator voltage  | 4.5V ≤ V <sub>VM</sub> < 6V, CP with respect to VM                                               | 3    | 5        | 5.5  | V    |
| V <sub>CP</sub>                             | Charge pump regulator voltage  | V <sub>VM</sub> ≥ 6V, CP with respect to VM                                                      | 4.5  | 5        | 5.5  | V    |
| t <sub>WAKE</sub>                           | Wakeup time                    | V <sub>VM</sub> > V <sub>UVLO</sub> , nSLEEP = 1 to output ready                                 |      | 1        | 3    | ms   |
| t <sub>WAKE_CSA</sub>                       | Wakeup time for CSA            | V <sub>CSAREF</sub> > V <sub>CSAREF_UV</sub> to SOx ready, when nSLEEP = 1                       |      | 30       |      | μs   |
| t <sub>SLEEP</sub>                          | Turn-off time                  | nSLEEP = 0 to driver tri-stated                                                                  |      | 100      | 200  | μs   |
| t <sub>RST</sub>                            | Reset Pulse time               | nSLEEP = 0 period to reset faults                                                                | 15   |          | 50   | μs   |
| <b>FOUR-LEVEL INPUTS (GAIN, MODE, SLEW)</b> |                                |                                                                                                  |      |          |      |      |
| V <sub>L1</sub>                             | Input mode 1 voltage           | Tied to AGND                                                                                     | 0    | 0.2*AVDD |      | V    |

**DRV8317**

SLVSGT3 – DECEMBER 2022

 $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{VM} = 4.5$  to  $20\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{VM} = 12\text{ V}$ 

| PARAMETER             |                                                                             | TEST CONDITIONS                                                                                                                                                  | MIN                          | TYP                          | MAX                          | UNIT             |
|-----------------------|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|------------------------------|------------------------------|------------------|
| $V_{L2}$              | Input mode 2 voltage                                                        | $47\text{ k}\Omega \pm 5\%$ tied to AGND                                                                                                                         | $0.27 \cdot \text{AV}_{DD}$  | $0.4 \cdot \text{AV}_D$      | $0.545 \cdot \text{AV}_{DD}$ | V                |
| $V_{L3}$              | Input mode 3 voltage                                                        | Hi-Z                                                                                                                                                             | $0.606 \cdot \text{AV}_{DD}$ | $0.757 \cdot \text{AV}_{DD}$ | $0.909 \cdot \text{AV}_{DD}$ | V                |
| $V_{L4}$              | Input mode 4 voltage                                                        | Tied to AVDD                                                                                                                                                     | $0.94 \cdot \text{AV}_{DD}$  |                              | AVDD                         | V                |
| $R_{PU}$              | Input pullup resistance                                                     | To AVDD                                                                                                                                                          |                              | 48                           |                              | k $\Omega$       |
| $R_{PD}$              | Input pulldown resistance                                                   | To AGND                                                                                                                                                          |                              | 160                          |                              | k $\Omega$       |
| <b>DRIVER OUTPUTS</b> |                                                                             |                                                                                                                                                                  |                              |                              |                              |                  |
| $R_{DS(ON)}$          | Total MOSFET on resistance (High-side + Low-side)                           | $V_{VM} \geq 6\text{ V}$ , $I_{OUT} = 1\text{ A}$ , $T_J = 25^{\circ}\text{C}$ , includes bond wire and metallization resistance                                 |                              | 130                          | 157                          | m $\Omega$       |
|                       |                                                                             | $V_{VM} \geq 6\text{ V}$ , $I_{OUT} = 1\text{ A}$ , $T_J = 125^{\circ}\text{C}$ , across process, includes bond wire and metallization resistance                |                              | 180                          | 221.5                        | m $\Omega$       |
| $R_{DS(ON)}$          | Total MOSFET on resistance (High-side + Low-side)                           | $4.5\text{ V} \leq V_{VM} < 6\text{ V}$ , $I_{OUT} = 1\text{ A}$ , $T_J = 25^{\circ}\text{C}$ , includes bond wire and metallization resistance                  |                              | 155                          | 210                          | m $\Omega$       |
|                       |                                                                             | $4.5\text{ V} \leq V_{VM} < 6\text{ V}$ , $I_{OUT} = 1\text{ A}$ , $T_J = 125^{\circ}\text{C}$ , across process, includes bond wire and metallization resistance |                              | 225                          | 290                          | m $\Omega$       |
| SR_RISE               | Phase pin slew rate switching low to high (Rising from 20 % to 80 % of VM)  | $V_{VM} = 12\text{ V}$ , SLEW_RATE = 00b (SPI Variant) or SLEW pin tied to AGND (HW Variant)                                                                     | 13.75                        | 25                           | 36.25                        | V/ $\mu\text{s}$ |
|                       |                                                                             | $V_{VM} = 12\text{ V}$ , SLEW_RATE = 01b (SPI Variant) or SLEW pin to $47\text{ k}\Omega \pm 5\%$ tied to AGND (HW Variant)                                      | 27.5                         | 50                           | 72.5                         | V/ $\mu\text{s}$ |
|                       |                                                                             | $V_{VM} = 12\text{ V}$ , SLEW_RATE = 10b (SPI Variant) or SLEW pin to Hi-Z (HW Variant)                                                                          | 62.5                         | 125                          | 187.5                        | V/ $\mu\text{s}$ |
|                       |                                                                             | $V_{VM} = 12\text{ V}$ , SLEW_RATE = 11b (SPI Variant) or SLEW pin tied to AVDD (HW Variant)                                                                     | 80                           | 200                          | 320                          | V/ $\mu\text{s}$ |
| SR_FALL               | Phase pin slew rate switching high to low (Falling from 80 % to 20 % of VM) | $V_{VM} = 12\text{ V}$ , SLEW_RATE = 00b (SPI Variant) or SLEW pin tied to AGND (HW Variant)                                                                     | 13.75                        | 25                           | 48                           | V/ $\mu\text{s}$ |
|                       |                                                                             | $V_{VM} = 12\text{ V}$ , SLEW_RATE = 01b (SPI Variant) or SLEW pin to $47\text{ k}\Omega \pm 5\%$ tied to AGND (HW Variant)                                      | 27.5                         | 50                           | 72.5                         | V/ $\mu\text{s}$ |
|                       |                                                                             | $V_{VM} = 12\text{ V}$ , SLEW_RATE = 10b (SPI Variant) or SLEW pin to Hi-Z (HW Variant)                                                                          | 62.5                         | 125                          | 187.5                        | V/ $\mu\text{s}$ |
|                       |                                                                             | $V_{VM} = 12\text{ V}$ , SLEW_RATE = 11b (SPI Variant) or SLEW pin tied to AVDD (HW Variant)                                                                     | 80                           | 200                          | 320                          | V/ $\mu\text{s}$ |
| $I_{LEAK}$            | Leakage current OUTx                                                        | $V_{VM} = V_{OUTx} = 20\text{ V}$ , Standby State                                                                                                                |                              | 0.7                          | 2                            | mA               |
| $I_{LEAK}$            | Leakage current OUTx                                                        | $V_{OUTx} = 0\text{ V}$ , Standby State                                                                                                                          | -50                          | -10                          |                              | $\mu\text{A}$    |

$T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{VM} = 4.5$  to  $20\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{VM} = 12\text{ V}$

| PARAMETER                      |                                                             | TEST CONDITIONS                                                                                                                              | MIN  | TYP  | MAX                     | UNIT |
|--------------------------------|-------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------------------------|------|
| $t_{\text{DEAD}}$              | Dead time (high to low / low to high)                       | $V_{VM} = 12\text{V}$ , SLEW_RATE = 00b (SPI Variant) or SLEW pin tied to AGND (HW Variant)                                                  |      | 575  | 1500                    | ns   |
|                                |                                                             | $V_{VM} = 12\text{V}$ , SLEW_RATE = 01b (SPI Variant) or SLEW pin to 47 k $\Omega$ +/- 5% tied to AGND (HW Variant)                          |      | 325  | 750                     | ns   |
|                                |                                                             | $V_{VM} = 12\text{V}$ , SLEW_RATE = 10b (SPI Variant) or SLEW pin to Hi-Z (HW Variant)                                                       |      | 250  | 600                     | ns   |
|                                |                                                             | $V_{VM} = 12\text{V}$ , SLEW_RATE = 11b (SPI Variant) or SLEW pin tied to AVDD (HW Variant)                                                  |      | 250  | 600                     | ns   |
| $t_{\text{PD}}$                | Propagation delay (high-side / low-side ON/OFF)             | INHx = 1 to OUTx transission, $V_{VM} = 12\text{V}$ , SLEW = 00b (SPI Variant) or SLEW pin tied to AGND (HW Variant)                         |      | 1300 | 1750                    | ns   |
|                                |                                                             | INHx = 1 to OUTx transission, $V_{VM} = 12\text{V}$ , SLEW = 01b (SPI Variant) or SLEW pin to 47 k $\Omega$ +/- 5% tied to AGND (HW Variant) |      | 800  | 1050                    | ns   |
|                                |                                                             | INHx = 1 to OUTx transission, $V_{VM} = 12\text{V}$ , SLEW = 10b (SPI Variant) or SLEW pin to Hi-Z (HW Variant)                              |      | 450  | 600                     | ns   |
|                                |                                                             | INHx = 1 to OUTx transission, $V_{VM} = 12\text{V}$ , SLEW = 11b (SPI Variant) or SLEW pin tied to AVDD (HW Variant)                         |      | 425  | 500                     | ns   |
| $t_{\text{MIN\_PULSE}}$        | Minimum output pulse width                                  | SLEW = 11b (SPI Variant) or SLEW pin tied to AVDD (HW Variant)                                                                               | 500  |      |                         | ns   |
| <b>CURRENT SENSE AMPLIFIER</b> |                                                             |                                                                                                                                              |      |      |                         |      |
| $G_{\text{CSA}}$               | Current sense gain                                          | CSA_GAIN = 00b (SPI Variant) or GAIN pin tied to AGND (HW Variant)                                                                           |      | 0.25 |                         | V/A  |
|                                |                                                             | CSA_GAIN = 01b (SPI Variant) or GAIN pin to 47 k $\Omega$ +/- 5% tied to AGND (HW Variant)                                                   |      | 0.5  |                         | V/A  |
|                                |                                                             | CSA_GAIN = 10b (SPI Variant) or GAIN pin to Hi-Z (HW Variant)                                                                                |      | 1    |                         | V/A  |
|                                |                                                             | CSA_GAIN = 11b (SPI Variant) or GAIN pin tied to AVDD (HW Variant)                                                                           |      | 2    |                         | V/A  |
| $G_{\text{CSA\_ERR}}$          | Current sense gain error                                    | $T_A = 25^{\circ}\text{C}$ , $I_{\text{PHASE}} \leq 2.5\text{ A}$                                                                            | -3   |      | 3                       | %    |
| $G_{\text{CSA\_ERR}}$          | Current sense gain error                                    | $T_A = 25^{\circ}\text{C}$ , $2.5\text{ A} < I_{\text{PHASE}} \leq 4\text{ A}$                                                               | -3.5 |      | 3.5                     | %    |
| $G_{\text{CSA\_ERR}}$          | Current sense gain error                                    | $T_A = 25^{\circ}\text{C}$ , $4\text{ A} < I_{\text{PHASE}} \leq 5\text{ A}$                                                                 | -3.5 |      | 4.5                     | %    |
| $G_{\text{CSA\_ERR}}$          | Current sense gain error                                    | $I_{\text{PHASE}} \leq 2.5\text{ A}$                                                                                                         | -4.5 |      | 4.5                     | %    |
| $G_{\text{CSA\_ERR}}$          | Current sense gain error                                    | $2.5\text{ A} < I_{\text{PHASE}} \leq 4\text{ A}$                                                                                            | -5   |      | 6                       | %    |
| $G_{\text{CSA\_ERR}}$          | Current sense gain error                                    | $4\text{ A} < I_{\text{PHASE}} \leq 5\text{ A}$                                                                                              | -5   |      | 8                       | %    |
| $I_{\text{MATCH}}$             | Current sense gain error matching between phases A, B and C | $T_J = 25^{\circ}\text{C}$                                                                                                                   | -3   |      | 3                       | %    |
|                                |                                                             |                                                                                                                                              | -5   |      | 5                       | %    |
| $\text{FS}_{\text{POS}}$       | Full scale positive current measurement                     |                                                                                                                                              | 5    |      |                         | A    |
| $\text{FS}_{\text{NEG}}$       | Full scale negative current measurement                     |                                                                                                                                              |      |      | -5                      | A    |
| $V_{\text{LINEAR}}$            | SOX output voltage linear range                             |                                                                                                                                              | 0.25 |      | $V_{\text{REF}} - 0.25$ | V    |

$T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{VM} = 4.5$  to  $20\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{VM} = 12\text{ V}$

| PARAMETER               |                                                                | TEST CONDITIONS                                                                      | MIN  | TYP | MAX | UNIT                           |
|-------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------------------|------|-----|-----|--------------------------------|
| $I_{\text{OFFSET\_RT}}$ | Current sense offset low side current input (Room Temperature) | $T_J = 25^{\circ}\text{C}$ , Phase current = 0 A, $G_{\text{CSA}} = 0.25\text{ V/A}$ | -100 |     | 100 | mA                             |
|                         |                                                                | $T_J = 25^{\circ}\text{C}$ , Phase current = 0 A, $G_{\text{CSA}} = 0.5\text{ V/A}$  | -50  |     | 50  | mA                             |
|                         |                                                                | $T_J = 25^{\circ}\text{C}$ , Phase current = 0 A, $G_{\text{CSA}} = 1\text{ V/A}$    | -30  |     | 30  | mA                             |
|                         |                                                                | $T_J = 25^{\circ}\text{C}$ , Phase current = 0 A, $G_{\text{CSA}} = 2\text{ V/A}$    | -30  |     | 30  | mA                             |
| $I_{\text{OFFSET}}$     | Current sense offset low side current input                    | Phase current = 0 A, $G_{\text{CSA}} = 0.25\text{ V/A}$                              | -140 |     | 140 | mA                             |
|                         |                                                                | Phase current = 0 A, $G_{\text{CSA}} = 0.5\text{ V/A}$                               | -70  |     | 70  | mA                             |
|                         |                                                                | Phase current = 0 A, $G_{\text{CSA}} = 1\text{ V/A}$                                 | -50  |     | 50  | mA                             |
|                         |                                                                | Phase current = 0 A, $G_{\text{CSA}} = 2\text{ V/A}$                                 | -50  |     | 50  | mA                             |
| $t_{\text{SET}}$        | Settling time to $\pm 1\%$ , 30 pF                             | Step on SOX = 1.2 V, $G_{\text{CSA}} = 0.25\text{ V/A}$                              |      |     | 1   | $\mu\text{s}$                  |
|                         |                                                                | Step on SOX = 1.2 V, $G_{\text{CSA}} = 0.5\text{ V/A}$                               |      |     | 1   | $\mu\text{s}$                  |
|                         |                                                                | Step on SOX = 1.2 V, $G_{\text{CSA}} = 1\text{ V/A}$                                 |      |     | 1   | $\mu\text{s}$                  |
|                         |                                                                | Step on SOX = 1.2 V, $G_{\text{CSA}} = 2\text{ V/A}$                                 |      |     | 1   | $\mu\text{s}$                  |
| $V_{\text{DRIFT}}$      | Drift offset                                                   | Phase current = 0 A                                                                  | -360 |     | 360 | $\mu\text{A}/^{\circ}\text{C}$ |
| $I_{\text{CSAREF}}$     | CSAREF input current                                           | $V_{\text{REF}} = 3.0\text{ V}$                                                      |      | 12  | 20  | $\mu\text{A}$                  |

$T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{VM} = 4.5$  to  $20\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{VM} = 12\text{ V}$

| PARAMETER                  |                                             | TEST CONDITIONS                   | MIN   | TYP   | MAX   | UNIT          |
|----------------------------|---------------------------------------------|-----------------------------------|-------|-------|-------|---------------|
| <b>PROTECTION CIRCUITS</b> |                                             |                                   |       |       |       |               |
| $V_{OVP}$                  | Supply overvoltage protection (OVP)         | VM rising                         | 21    | 22    | 23    | V             |
|                            |                                             | VM falling                        | 20    | 21    | 22    | V             |
| $V_{OVP\_HYS}$             | Supply overvoltage protection hysteresis    | Falling to rising threshold       | 900   | 1000  | 1200  | mV            |
| $t_{OVP}$                  | Supply overvoltage protection deglitch time |                                   | 3     | 5     | 7     | $\mu\text{s}$ |
| $V_{UVLO}$                 | Supply undervoltage lockout (UVLO)          | VM rising                         | 4.25  | 4.4   | 4.61  | V             |
|                            |                                             | VM falling                        | 4.1   | 4.2   | 4.35  | V             |
| $V_{UVLO\_HYS}$            | Supply undervoltage lockout hysteresis      | Rising to falling threshold       | 140   | 210   | 350   | mV            |
| $t_{UVLO}$                 | Supply undervoltage lockout deglitch time   |                                   | 3     | 5     | 7     | $\mu\text{s}$ |
| $V_{VMUV\_WARN\_RISE}$     | Supply (VM) undervoltage warning, rising    | VM rising, VMUV_WARN_RISE = 0000b | 5.4   | 5.62  | 6     | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 0001b | 6     | 6.25  | 6.6   | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 0010b | 6.6   | 6.87  | 7.25  | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 0011b | 7.15  | 7.5   | 7.95  | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 0100b | 7.8   | 8.12  | 8.6   | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 0101b | 8.4   | 8.75  | 9.3   | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 0110b | 9     | 9.37  | 9.9   | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 0111b | 9.6   | 10    | 10.6  | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 1000b | 10.2  | 10.62 | 11.2  | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 1001b | 10.8  | 11.25 | 11.9  | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 1010b | 11.35 | 11.87 | 12.55 | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 1011b | 11.95 | 12.5  | 13.15 | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 1100b | 13.2  | 13.75 | 14.5  | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 1101b | 14.3  | 15.00 | 15.9  | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 1110b | 15.5  | 16.25 | 17.1  | V             |
|                            |                                             | VM rising, VMUV_WARN_RISE = 1111b | 16.7  | 17.5  | 18.6  | V             |

$T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{VM} = 4.5$  to  $20\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{VM} = 12\text{ V}$

| PARAMETER                |                                                               | TEST CONDITIONS                    | MIN   | TYP  | MAX   | UNIT          |
|--------------------------|---------------------------------------------------------------|------------------------------------|-------|------|-------|---------------|
| $V_{VMUV\_WARN\_FALL}$   | Supply (VM) undervoltage warning, falling                     | VM falling, VMUV_WARN_FALL = 0000b | 5.1   | 5.4  | 5.75  | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 0001b | 5.7   | 6.0  | 6.3   | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 0010b | 6.25  | 6.6  | 6.95  | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 0011b | 6.8   | 7.2  | 7.6   | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 0100b | 7.4   | 7.8  | 8.2   | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 0101b | 7.95  | 8.4  | 8.85  | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 0110b | 8.5   | 9.0  | 9.5   | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 0111b | 9.05  | 9.6  | 10.15 | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 1000b | 9.7   | 10.2 | 10.7  | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 1001b | 10.15 | 10.8 | 11.4  | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 1010b | 10.75 | 11.4 | 12    | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 1011b | 11.3  | 12.0 | 12.6  | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 1100b | 12.5  | 13.2 | 13.8  | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 1101b | 13.5  | 14.4 | 15.3  | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 1110b | 14.7  | 15.6 | 16.4  | V             |
|                          |                                                               | VM falling, VMUV_WARN_FALL = 1111b | 15.9  | 16.8 | 17.8  | V             |
| $t_{VMUV\_WARN\_DG}$     | Supply undervoltage warning deglitch time                     | VMUV_TDG = 00b                     | 0.1   | 0.3  | 0.45  | $\mu\text{s}$ |
|                          |                                                               | VMUV_TDG = 01b                     | 0.35  | 0.6  | 0.8   | $\mu\text{s}$ |
|                          |                                                               | VMUV_TDG = 10b                     | 0.55  | 0.9  | 1.35  | $\mu\text{s}$ |
|                          |                                                               | VMUV_TDG = 11b                     | 1.4   | 2    | 2.5   | $\mu\text{s}$ |
| $t_{VMUV\_WARN\_DG}$     | Supply undervoltage warning deglitch time (HW variant)        |                                    | 0.35  | 0.6  | 0.8   | $\mu\text{s}$ |
| $V_{VIN\_AVDD\_UV}$      | AVDD supply input undervoltage lockout ( $V_{IN\_AVDD\_UV}$ ) | VIN_AVDD rising                    | 4.25  | 4.4  | 4.61  | V             |
|                          |                                                               | VIN_AVDD falling                   | 4.1   | 4.2  | 4.35  | V             |
| $V_{VIN\_AVDD\_UV\_HYS}$ | Supply undervoltage lockout hysteresis                        | Rising to falling threshold        | 140   | 210  | 350   | mV            |
| $V_{CPUV}$               | Charge pump undervoltage lockout (above VM)                   | Supply rising                      | 2.64  | 2.8  | 2.95  | V             |
|                          |                                                               | Supply falling                     | 2.35  | 2.6  | 2.7   | V             |
| $V_{CPUV\_HYS}$          | Charge pump undervoltage lockout hysteresis                   | Rising to falling threshold        | 160   | 210  | 245   | mV            |
| $t_{CPUV}$               | Charge pump undervoltage lockout deglitch time                |                                    | 3     | 5    | 7     | $\mu\text{s}$ |
| $V_{AVDD\_UV}$           | Analog regulator undervoltage lockout                         | Supply rising                      | 2.7   | 2.8  | 2.9   | V             |
|                          |                                                               | Supply falling                     | 2.6   | 2.7  | 2.8   | V             |
| $V_{AVDD\_UV\_HYS}$      | Analog regulator undervoltage lockout hysteresis              | Rising to falling threshold        | 80    | 100  | 150   | mV            |
| $I_{OCP}$                | Overcurrent protection trip point                             |                                    | 6     | 9.5  | 12    | A             |
| $t_{BLANK}^{(1)}$        | Overcurrent protection blanking time                          | OCP_TBLANK = 00b                   | 0.15  | 0.3  | 0.45  | $\mu\text{s}$ |
|                          |                                                               | OCP_TBLANK = 01b                   | 0.45  | 0.7  | 0.85  | $\mu\text{s}$ |
|                          |                                                               | OCP_TBLANK = 10b                   | 0.7   | 1    | 1.25  | $\mu\text{s}$ |
|                          |                                                               | OCP_TBLANK = 10b                   | 0.9   | 1.2  | 1.5   | $\mu\text{s}$ |
| $t_{BLANK}^{(1)}$        | Overcurrent protection blanking time (HW Variant)             |                                    | 0.45  | 0.7  | 0.85  | $\mu\text{s}$ |

$T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{VM} = 4.5$  to  $20\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{VM} = 12\text{ V}$

| PARAMETER                                                 |                                                   | TEST CONDITIONS                                                       | MIN  | TYP  | MAX  | UNIT               |
|-----------------------------------------------------------|---------------------------------------------------|-----------------------------------------------------------------------|------|------|------|--------------------|
| $t_{OCP}^{(1)}$                                           | Overcurrent protection deglitch time              | OCP_DEG = 00b                                                         | 0.1  | 0.3  | 0.45 | $\mu\text{s}$      |
|                                                           |                                                   | OCP_DEG = 01b                                                         | 0.35 | 0.6  | 0.85 | $\mu\text{s}$      |
|                                                           |                                                   | OCP_DEG = 10b                                                         | 0.6  | 0.9  | 1.25 | $\mu\text{s}$      |
|                                                           |                                                   | OCP_DEG = 11b                                                         | 0.8  | 1.2  | 1.5  | $\mu\text{s}$      |
| $t_{OCP}^{(1)}$                                           | Overcurrent protection deglitch time (HW Variant) |                                                                       | 0.35 | 0.6  | 0.85 | $\mu\text{s}$      |
| $t_{RETRY}$                                               | Overcurrent protection retry time                 | FAST_TRETRY = 00b                                                     | 0.35 | 0.5  | 0.7  | ms                 |
|                                                           |                                                   | FAST_TRETRY = 01b                                                     | 0.75 | 1    | 1.3  | ms                 |
|                                                           |                                                   | FAST_TRETRY = 10b                                                     | 1.65 | 2    | 2.45 | ms                 |
|                                                           |                                                   | FAST_TRETRY = 11b                                                     | 4.35 | 5    | 5.85 | ms                 |
| $t_{RETRY}$                                               | Overcurrent protection retry time                 | SLOW_TRETRY = 00b                                                     | 350  | 500  | 700  | ms                 |
|                                                           |                                                   | SLOW_TRETRY = 01b                                                     | 750  | 1000 | 1300 | ms                 |
|                                                           |                                                   | SLOW_TRETRY = 10b                                                     | 1650 | 2000 | 2450 | ms                 |
|                                                           |                                                   | SLOW_TRETRY = 11b                                                     | 4350 | 5000 | 5850 | ms                 |
| $t_{RETRY}$                                               | Overcurrent protection retry time (HW Variant)    |                                                                       | 4.35 | 5    | 5.85 | ms                 |
| $T_{OTW\_FET}$                                            | Overtemperature warning threshold (FET)           | Die temperature ( $T_J$ ) Rising                                      | 110  | 125  | 140  | $^{\circ}\text{C}$ |
| $T_{OTW\_HYS\_FET}$                                       | Overtemperature warning hysteresis (FET)          | Die temperature ( $T_J$ )                                             | 15   | 20   | 25   | $^{\circ}\text{C}$ |
| $T_{OTS\_FET}$                                            | Overtemperature shutdown threshold (FET)          | Die temperature ( $T_J$ ) Rising                                      | 145  | 160  | 175  | $^{\circ}\text{C}$ |
| $T_{OTS\_HYS\_FET}$                                       | Overtemperature shutdown hysteresis (FET)         | Die temperature ( $T_J$ )                                             | 14   | 20   | 25   | $^{\circ}\text{C}$ |
| $T_{OTS\_LDO}$                                            | Overtemperature shutdown threshold (LDO)          | Die temperature ( $T_J$ ) Rising                                      | 145  | 160  | 175  | $^{\circ}\text{C}$ |
| $T_{OTS\_HYS\_LDO}$                                       | Overtemperature shutdown hysteresis (LDO)         | Die temperature ( $T_J$ )                                             | 14   | 20   | 25   | $^{\circ}\text{C}$ |
| <b>LOGIC-LEVEL INPUTS (INHx, INLx, nSLEEP, SCLK, SDI)</b> |                                                   |                                                                       |      |      |      |                    |
| $V_{IL}$                                                  | Input logic low voltage                           | nSLEEP                                                                | 0    |      | 0.7  | V                  |
| $V_{IL}$                                                  | Input logic low voltage                           | SDI, INLx, INHx, SCLK                                                 | 0    |      | 0.65 | V                  |
| $V_{IH}$                                                  | Input logic high voltage                          | nSLEEP                                                                | 1.7  |      | 5.5  | V                  |
| $V_{IH}$                                                  | Input logic high voltage                          | SDI, INLx, INHx, SCLK                                                 | 1.5  |      | 3.6  | V                  |
| $V_{HYS}$                                                 | Input logic hysteresis                            | nSLEEP                                                                | 200  |      | 600  | mV                 |
| $V_{HYS}$                                                 | Input logic hysteresis                            | SDI, INLx, INHx, SCLK                                                 | 200  |      | 500  | mV                 |
| $I_{IL}$                                                  | Input logic low current                           | nSLEEP, SDI, INLx, INHx, SCLK (Pin Voltage) = 0 V                     | -1   |      | 1    | $\mu\text{A}$      |
| $I_{IH}$                                                  | Input logic high current                          | nSLEEP (Pin Voltage) = 5V                                             |      |      | 40   | $\mu\text{A}$      |
|                                                           |                                                   | Other pins, $3\text{V} \leq V_{PIN}$ (Pin Voltage) $\leq 3.6\text{V}$ |      |      | 30   | $\mu\text{A}$      |
| $R_{PD}$                                                  | Input pulldown resistance                         | nSLEEP                                                                |      | 150  | 300  | k $\Omega$         |
|                                                           |                                                   | SDI, SCLK, INHx, INLx                                                 |      | 150  | 300  | k $\Omega$         |
| $C_{ID}$                                                  | Input capacitance                                 | nSLEEP, SDI, SCLK, INHx, INLx                                         |      | 30   |      | pF                 |
| <b>LOGIC-LEVEL INPUTS (nSCS)</b>                          |                                                   |                                                                       |      |      |      |                    |
| $V_{IL}$                                                  | Input logic low voltage                           |                                                                       | 0    |      | 0.7  | V                  |
| $V_{IH}$                                                  | Input logic high voltage                          |                                                                       | 1.5  |      | 3.6  | V                  |
| $V_{HYS}$                                                 | Input logic hysteresis                            |                                                                       | 200  |      | 500  | mV                 |
| $I_{IL}$                                                  | Input logic low current                           | $V_{PIN}$ (Pin Voltage) = 0 V                                         |      |      | 95   | $\mu\text{A}$      |
| $I_{IH}$                                                  | Input logic high current                          | $3\text{V} \leq V_{PIN}$ (Pin Voltage) $\leq 3.6\text{V}$             | -1   |      | 1    | $\mu\text{A}$      |

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 $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{VM} = 4.5$  to  $20\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{VM} = 12\text{ V}$ 

| PARAMETER                          |                           | TEST CONDITIONS                                                        | MIN              | TYP | MAX | UNIT          |
|------------------------------------|---------------------------|------------------------------------------------------------------------|------------------|-----|-----|---------------|
| $R_{PU}$                           | Input pullup resistance   |                                                                        | 35               | 48  | 75  | $k\Omega$     |
| $C_{ID}$                           | Input capacitance         |                                                                        |                  | 30  |     | pF            |
| <b>OPEN-DRAIN OUTPUTS (nFAULT)</b> |                           |                                                                        |                  |     |     |               |
| $V_{OL}$                           | Output logic low voltage  | $I_{OD} = -5\text{ mA}$                                                |                  |     | 0.4 | V             |
| $I_{OH}$                           | Output logic high current | $3\text{ V} \leq V_{OD} \leq 3.6\text{ V}$                             | -1               |     | 1   | $\mu\text{A}$ |
| $C_{OD}$                           | Output capacitance        |                                                                        |                  | 30  |     | pF            |
| <b>PUSH-PULL OUTPUTS (SDO)</b>     |                           |                                                                        |                  |     |     |               |
| $V_{OL}$                           | Output logic low voltage  | $I_{OP} = -5\text{ mA}$ , $3\text{ V} \leq V_{AVDD} \leq 3.6\text{ V}$ | 0                |     | 0.5 | V             |
| $V_{OH}$                           | Output logic high voltage | $I_{OP} = 5\text{ mA}$ , $3\text{ V} \leq V_{AVDD} \leq 3.6\text{ V}$  | $V_{AVDD} - 0.5$ |     | 3.6 | V             |
| $I_{OL}$                           | Output logic low current  | $V_{OP} = 0\text{ V}$                                                  | -1               |     | 1   | $\mu\text{A}$ |
| $I_{OH}$                           | Output logic high current | $V_{OP} = 5\text{ V}$                                                  | -2               |     | 2   | $\mu\text{A}$ |
| $C_{OD}$                           | Output capacitance        |                                                                        |                  | 30  |     | pF            |

(1)  $(t_{OCP} + t_{BLANK})$  must not exceed  $2.2\text{ }\mu\text{s}$

## 8 Detailed Description

### 8.1 Overview

The DRV8317 is an integrated MOSFET driver for 3-phase motor-drive applications. The combined high-side and low-side FETs' on-state resistance is 130-m $\Omega$  (typical). The device reduces system component count, cost, and complexity by integrating three MOSFET half-bridges, gate drivers, charge pump, current sense amplifiers and linear regulator for external loads. In DRV8317S, a standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault status information through an external controller. In DRV8317H, a hardware (pin-based) interface allows configuring the PWM mode (6x or 3x), current sense amplifier gain and output slew rate through pin voltage levels.

The gate driver architecture is designed to protect against short-circuit events and dV/dt parasitic turn-on of the internal power MOSFETs.

The DRV8317 integrates three bi-directional low-side current sense amplifiers for monitoring the current through each of the half-bridges using a built-in current sense circuit; no external current sense resistors are needed. The gain of the current sense amplifiers can be adjusted through the SPI or hardware interface.

In addition to the high level of device integration, the DRV8317 provides a wide range of integrated protection features. These features include power supply undervoltage lockout (UVLO), over voltage protection (OVP), charge pump undervoltage lockout (CPUV), over current protection (OCP), AVDD under voltage lockout (AVDD\_UV) and over temperature warning and shutdown (OTW and OTS). Fault events are indicated by the nFAULT pin with detailed information available in the status registers in the SPI variant.

The DRV8317S, DRV8317H devices are available in 0.4-mm pin pitch, WQFN surface-mount packages. The WQFN package size is 5.00-mm  $\times$  4.00-mm with a height of 0.8-mm.

## 8.2 Functional Block Diagram

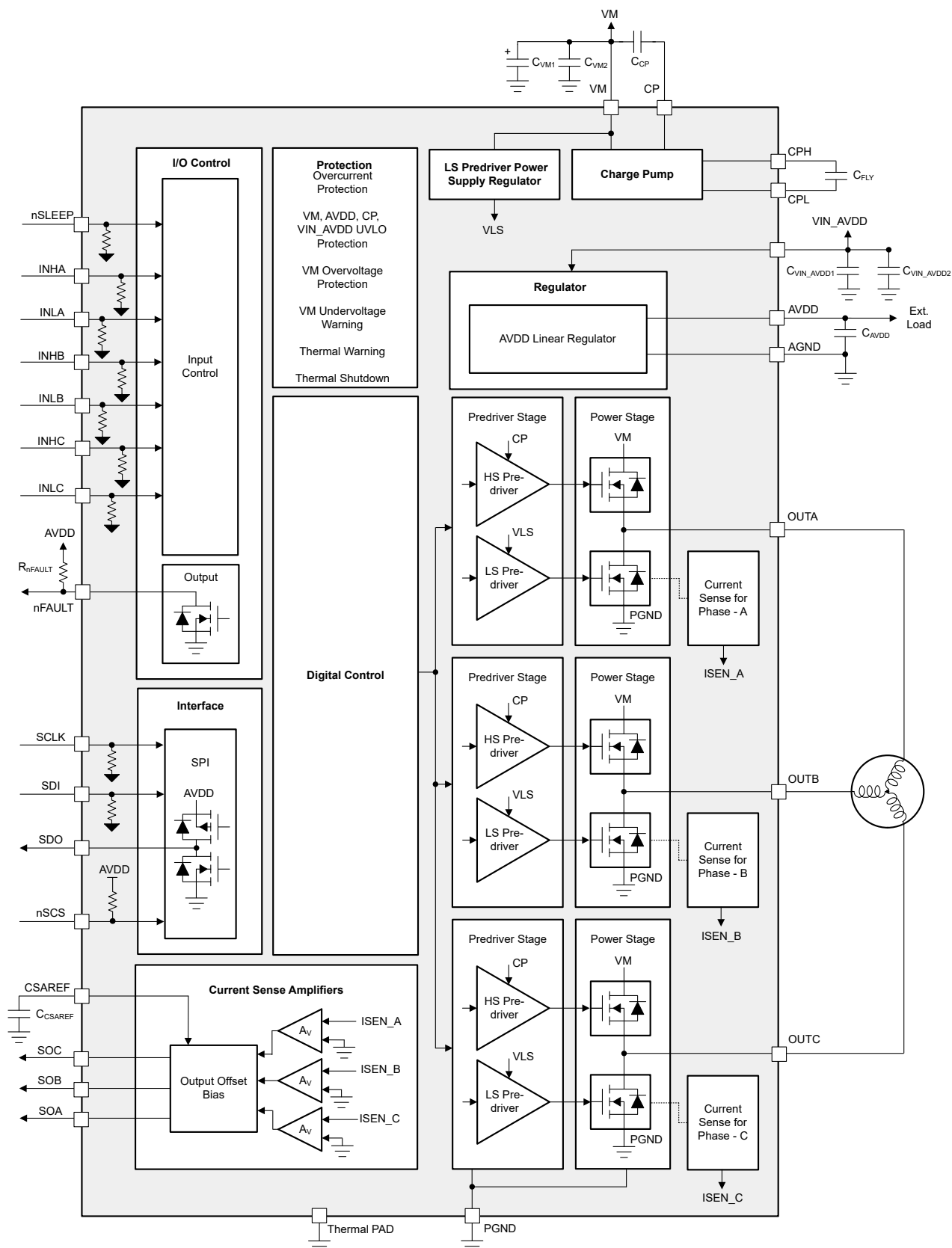


Figure 8-1. DRV8317S Functional Block Diagram

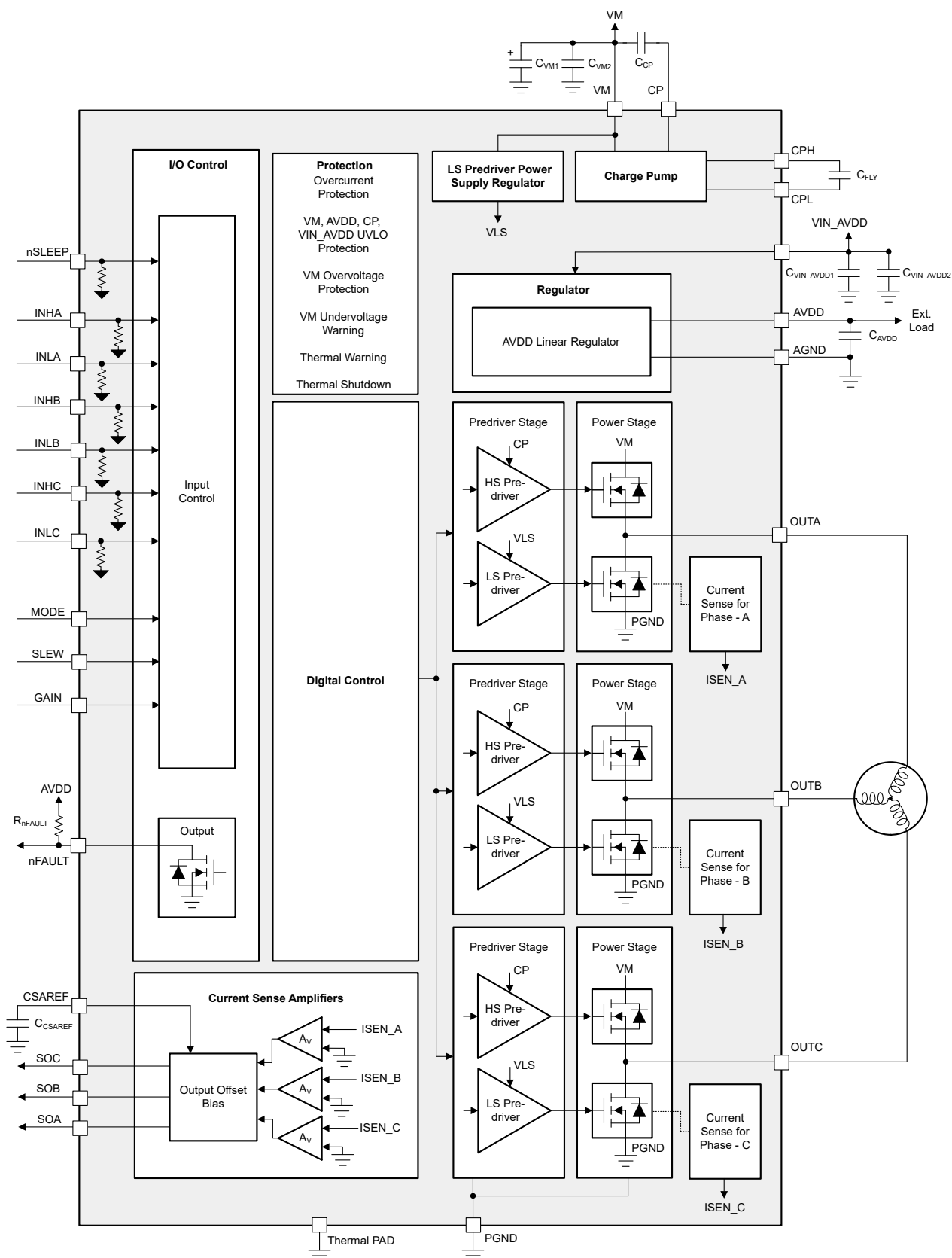


**Figure 8-2. DRV8317H Functional Block Diagram**

## 8.3 Feature Description

Table 8-1 lists the recommended values of the external components for the driver.

**Table 8-1. DRV8317 External Components**

| COMPONENTS             | PIN 1    | PIN 2  | RECOMMENDED                                                                     |
|------------------------|----------|--------|---------------------------------------------------------------------------------|
| C <sub>VM1</sub>       | VM       | PGND   | X5R or X7R, 0.1-μF, (2 x VM)-rated capacitor                                    |
| C <sub>VM2</sub>       | VM       | PGND   | ≥ 10-μF, (2 x VM)-rated electrolytic capacitor                                  |
| C <sub>VIN_AVDD1</sub> | VIN_AVDD | AGND   | X5R or X7R, 0.1-μF, (2 x VIN_AVDD)-rated capacitor                              |
| C <sub>VIN_AVDD2</sub> | VIN_AVDD | AGND   | ≥ 10-μF, (2 x VIN_AVDD)-rated capacitor                                         |
| C <sub>FLY</sub>       | CPH      | CPL    | X5R or X7R, 0.1-μF, (2 x VM)-rated capacitor                                    |
| C <sub>CP</sub>        | CP       | VM     | X5R or X7R, 16-V, 1-μF capacitor                                                |
| C <sub>AVDD</sub>      | AVDD     | AGND   | X5R or X7R, 2.2-μF (no external load) 4.7-μF (up to 80mA load), 6.3-V capacitor |
| R <sub>nFAULT</sub>    | AVDD     | nFAULT | 5.1-kΩ, Pull-up resistor                                                        |
| R <sub>MODE</sub>      | MODE     | AGND   | <a href="#">Section 8.3.3.2</a>                                                 |
| R <sub>SLEW</sub>      | SLEW     | AGND   | <a href="#">Section 8.3.3.2</a>                                                 |
| R <sub>GAIN</sub>      | GAIN     | AGND   | <a href="#">Section 8.3.3.2</a>                                                 |
| C <sub>CSAREF</sub>    | CSAREF   | AGND   | X5R or X7R, 0.1-μF, (2 x CSAREF)-rated capacitor                                |

### 8.3.1 Output Stage

The DRV8317 consists of integrated N-channel FETs (high-side and low-side) connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side N-channel FETs across a wide operating (VM) voltage range in addition to providing 100% duty-cycle support. An internal linear regulator operating from the VM supply provides the gate-bias voltage (VLS) for the low-side N-channel FETs.

### 8.3.2 Control Modes

The DRV8317 family of devices provides three different control modes to support various commutation and control methods. Table 8-2 shows the various modes of the DRV8317 device.

**Table 8-2. PWM Control Modes**

| PWM Control Mode | PWM_MODE register (DRV8317S) | MODE Pin (DRV8317H)                                               |
|------------------|------------------------------|-------------------------------------------------------------------|
| 6x PWM           | PWM_MODE = 00b               | MODE pin tied to AGND directly or tied to AGND via 47-kΩ resistor |
| 6x direct PWM    | PWM_MODE = 01b               | Not Available                                                     |
| 3x PWM           | PWM_MODE = 10b               | MODE pin floating (Hi-Z) or tied to AVDD                          |
| 3x direct PWM    | PWM_MODE = 11b               | Not Available                                                     |

The difference between 6x PWM (or 3x PWM) and 6x direct PWM (or 3x direct PWM) is that in the direct (6x or 3x) PWM mode, the delay compensation logic circuit is bypassed and the inputs at INHx, INLx are directly passed on to the gate driver circuit. In the gate driver circuit, a dead time (t<sub>DRV\_DEAD</sub>) is added before driving the FETs to prevent shoot through faults - this dead time is available in all the four PWM control modes.

#### Note

TI does not recommend changing the MODE pin or PWM\_MODE register during power up of the device (during t<sub>WAKE</sub>). The MODE pin setting on DRV8317H is latched at power up, so set nSLEEP = 0 before changing the MODE pin configuration on the DRV8317H. In DRV8317S, set all INHx and INLx pins to logic low before changing the PWM\_MODE register.

### 8.3.2.1 6x PWM Mode

In 6x PWM mode, each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). To configure DRV8317H in 6x PWM mode, connect the MODE pin to AGND or connect the MODE pin to AGND via 47-k $\Omega$  resistor. To enable 6x PWM mode in DRV8317S, configure the MODE bits with PWM\_MODE = 00b or 01b. The corresponding INHx and INLx signals control the output state as listed in [Table 8-3](#).

**Table 8-3. 6x PWM Mode Truth Table**

| INHx | INLx | OUTx |
|------|------|------|
| 0    | 0    | Hi-Z |
| 0    | 1    | L    |
| 1    | 0    | H    |
| 1    | 1    | Hi-Z |

[Figure 8-3](#) shows the application diagram of DRV8317 configured in 6x PWM mode.

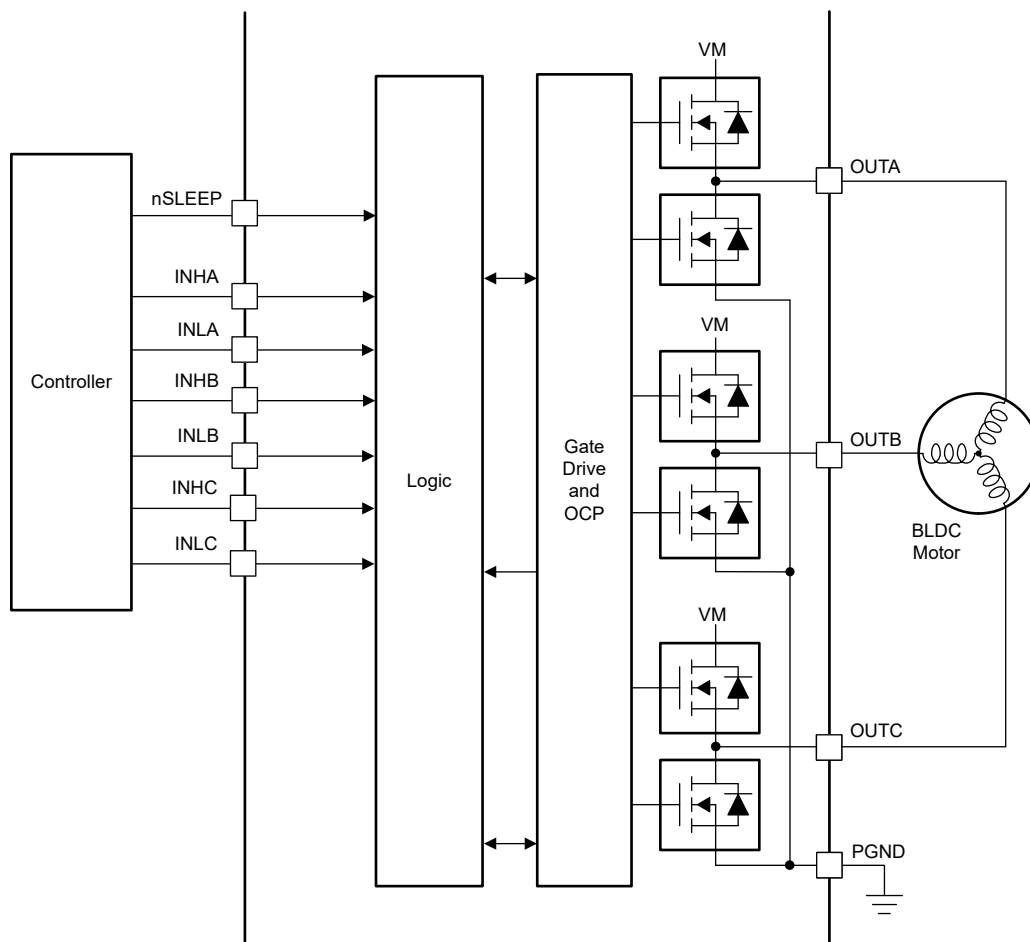


**Figure 8-3. 6x PWM Mode**

### 8.3.2.2 3x PWM Mode

In 3x PWM mode, the INHx pin controls each half-bridge and supports two output states: low or high. To configure DRV8317H in 3x PWM mode, connect the MODE pin to AVDD or keep the MODE pin floating (Hi-Z). To enable 3x PWM mode in DRV8317S, set PWM\_MODE to 10b or 11b. The INLx pin is used to put the half bridge in the Hi-Z state. If the Hi-Z state is not required, tie all INLx pins to logic high (for example, by tying them to AVDD). The corresponding INHx and INLx signals control the output state as listed in [Table 8-4](#).

**Table 8-4. 3x PWM Mode Truth Table**

| INLx | INHx | OUTx |
|------|------|------|
| 0    | X    | Hi-Z |
| 1    | 0    | L    |
| 1    | 1    | H    |

[Figure 8-4](#) shows the typical application diagram of the DRV8317 configured in 3x PWM mode.

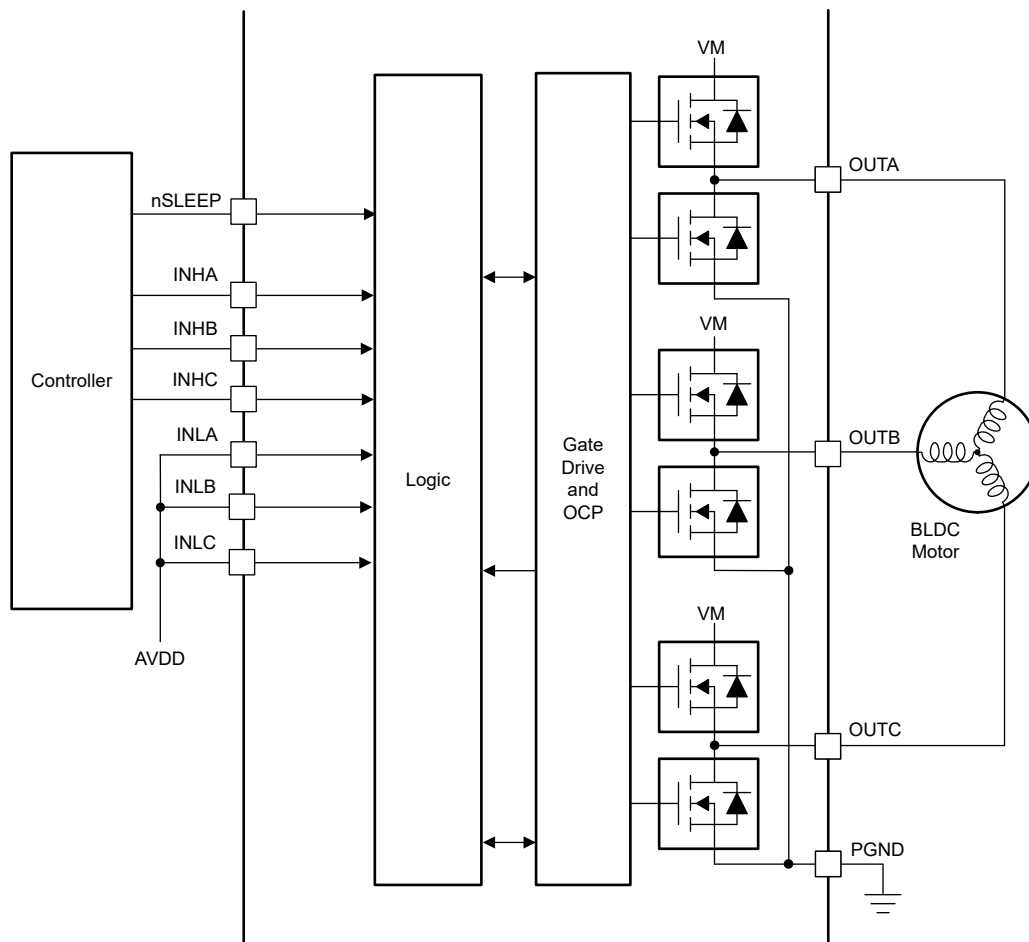


**Figure 8-4. 3x PWM Mode**

### 8.3.3 Device Interface Modes

The DRV8317 family of devices supports two different interface modes (SPI and hardware) to offer either increased simplicity (hardware interface) or greater flexibility (SPI interface). The SPI (DRV8317S) and hardware (DRV8317H) interface modes share the same four pins, allowing the different versions to be pin-to-pin compatible. Designers are encouraged to evaluate with the SPI interface version due to ease of changing settings, and may consider switching to the hardware interface with minimal modifications to the design.

### 8.3.3.1 Serial Peripheral Interface (SPI)

The SPI variant (DRV8317S) supports a serial communication bus that allows an external controller to send and receive data with DRV8317. This enables the external controller to configure device settings and read detailed fault information. The interface is a four wire interface using the SCLK, SDI, SDO, and nSCS pins which are described as follows:

- The SCLK (serial clock) pin is an input that accepts a clock signal to determine when data is captured and propagated on the SDI and SDO pins.
- The SDI (serial data in) pin is the data input.
- The SDO (serial data out) pin is the data output.
- The nSCS (serial chip select) pin is the chip select input. A logic low signal on this pin enables SPI communication with the DRV8317.

For more information on the SPI, see [Section 8.5](#).

### 8.3.3.2 Hardware Interface

The hardware variant (DRV8317H) replaces the four SPI pins with three resistor-configurable pins, namely, GAIN, SLEW and MODE (one of the four SPI pins is NC in hardware variant).

PWM control mode, CSA gain and driver output slew rate can be adjusted on the hardware interface by tying the respective pins to AGND, AVDD, pulling down to AGND with a 47-k $\Omega$  resistor or by leaving the pin floating (Hi-Z). In DRV8317H, fault conditions are reported on the nFAULT pin, but detailed fault information is not available.

- The GAIN pin configures the gain of the current sense amplifier.
- The SLEW pin configures the slew rate of the output voltage to motor.
- The MODE pin configures the PWM control mode.

For more information on the hardware interface, see [Section 8.3.9](#).

**Table 8-5. Hardware Pins Decode**

| Configuration                        | GAIN     | SLEW           | MODE        |
|--------------------------------------|----------|----------------|-------------|
| Pin tied to AGND                     | 0.25-V/A | 25-V/ $\mu$ s  | 6x PWM mode |
| Pin pulled to AGND via 47-k $\Omega$ | 0.5-V/A  | 50-V/ $\mu$ s  | 6x PWM mode |
| Pin floating (Hi-Z)                  | 1-V/A    | 125-V/ $\mu$ s | 3x PWM mode |
| Pin tied to AVDD                     | 2-V/A    | 200-V/ $\mu$ s | 3x PWM mode |

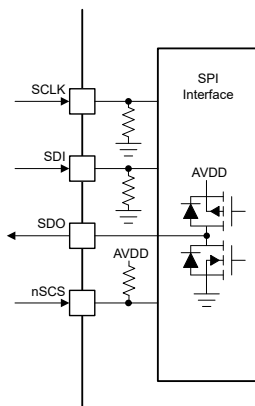


**Figure 8-5. DRV8317S SPI Interface**

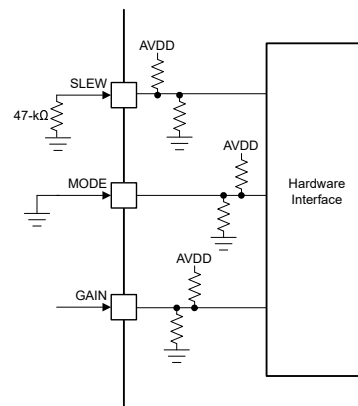


**Figure 8-6. DRV8317H Hardware Interface**

### 8.3.4 AVDD Linear Voltage Regulator

A 3.3-V, 80mA linear regulator is integrated in the DRV8317 and is available to power external circuits. The AVDD regulator is used for powering up the internal circuits of DRV8317 and can also provide power to external

circuits like MCU, logic, hall sensors, LEDs for up to 80 mA. The output of the AVDD regulator should be bypassed near the AVDD pin with a X5R or X7R, up to 7.05µF (4.7µF typical), 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3 V.

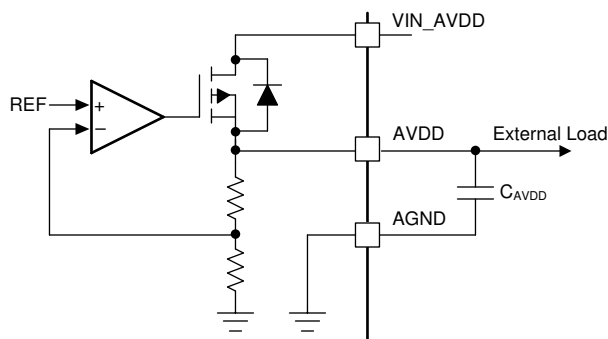


**Figure 8-7. AVDD Linear Regulator Block Diagram**

Use [Equation 1](#) to calculate the power dissipated in the device by the AVDD linear regulator.

$$P = (V_{VIN\_AVDD} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

The supply input voltage for AVDD regulator (VIN\_AVDD) can be same as VM supply voltage, or lower or higher than VM supply voltage.

### 8.3.5 Charge Pump

The DRV8317 requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully because the output stages uses N-channel FETs for both high-side and low-side. The DRV8317 integrates a charge pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. See [Table 8-1](#) for details on the capacitor value.

The charge pump shuts down when nSLEEP is low.

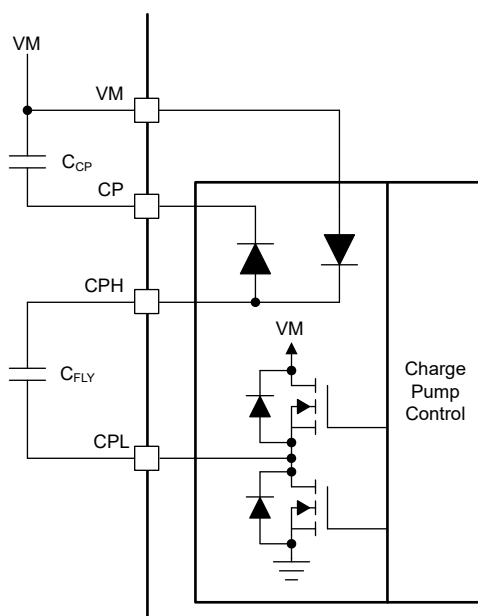


**Figure 8-8. DRV8317 Charge Pump**

### 8.3.6 Slew Rate Control

An adjustable gate-drive current to the MOSFETs allows for driver output slew rate control. The MOSFET VDS slew rate is a critical factor in optimizing radiated emissions, energy and duration of diode recovery spikes and switching voltage transients related to parasitics. This slew rate is predominantly determined by the rate of gate charge to the MOSFETs as shown in Figure 8-9.

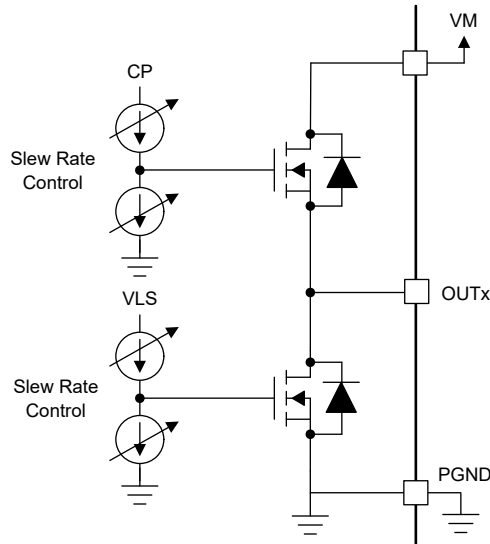


Figure 8-9. Slew Rate Control

The slew rate of each half-bridge can be adjusted by SLEW pin in hardware variant or by SLEW\_RATE register in SPI variant. The slew rate is calculated by the rise-time and fall-time of the voltage on OUTx pin as shown in Figure 8-10.

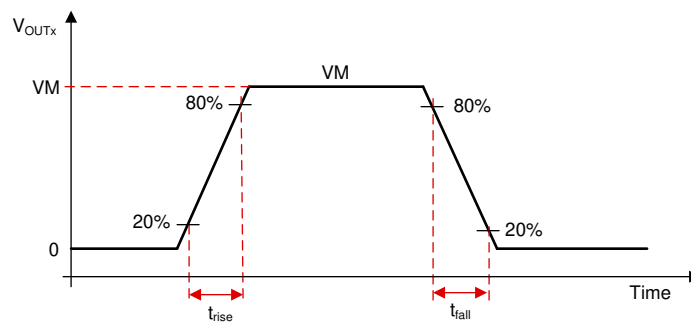


Figure 8-10. Slew Rate Measurement

### 8.3.7 Cross Conduction (Dead Time)

The device is fully protected against any cross conduction of MOSFETs - during the switching of high-side and low-side MOSFETs, DRV8317 avoids shoot-through events by inserting a dead time ( $t_{dead}$ ). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and ensuring that VGS of high-side MOSFET has dropped below turn-off level before switching on the low-side MOSFET of same half-bridge (or vice-versa) as shown in Figure 8-11 and Figure 8-12. The VGS of the high-side and low-side MOSFETs (VGS\_HS and VGS\_LS) shown in Figure 8-12 are DRV8317 internal signals.

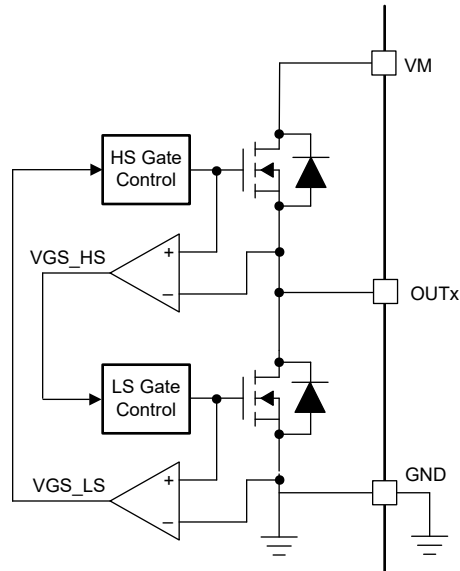


**Figure 8-11. Cross Conduction Protection**

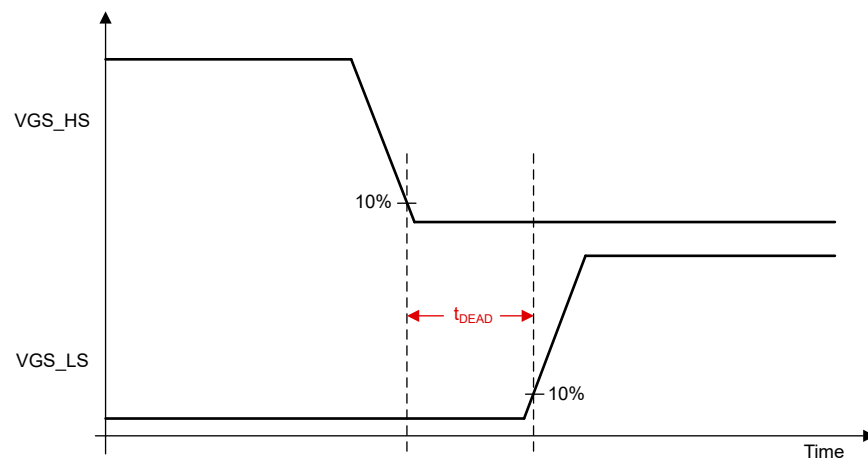


**Figure 8-12. Dead Time**

### 8.3.8 Propagation Delay

The propagation delay time ( $t_{pd}$ ) is measured as the time between an input logic edge to change in OUTx voltage. The propagation delay time includes the input deglitch delay, analog driver delay, and depends on the slew rate setting. The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. To support multiple control modes, a small digital delay is added as the input command propagates through the device.

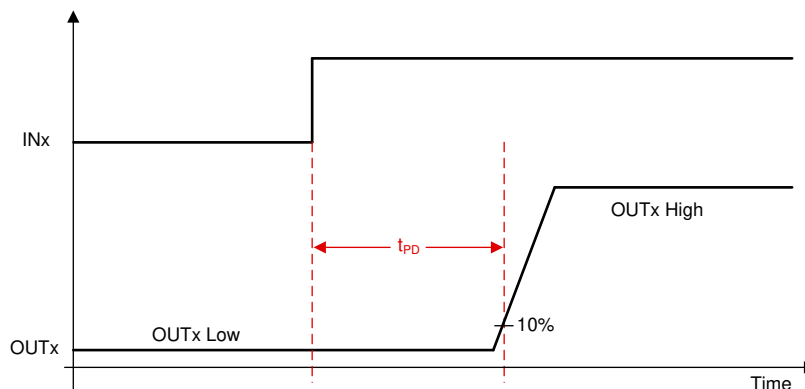


**Figure 8-13. Propagation Delay**

### 8.3.9 Pin Diagrams

This section presents the I/O structure of all digital input and output pins.

#### 8.3.9.1 Logic Level Input Pin (Internal Pulldown)

Figure 8-14 shows the input structure for the logic levels pins  $INHx$ ,  $INLx$ ,  $nSLEEP$ ,  $SCLK$  and  $SDI$ . The input can be driven with an external resistor to GND or an external logic voltage supply. It is recommended to pull these pins low in device sleep mode to reduce leakage current through the internal pull-down resistors.

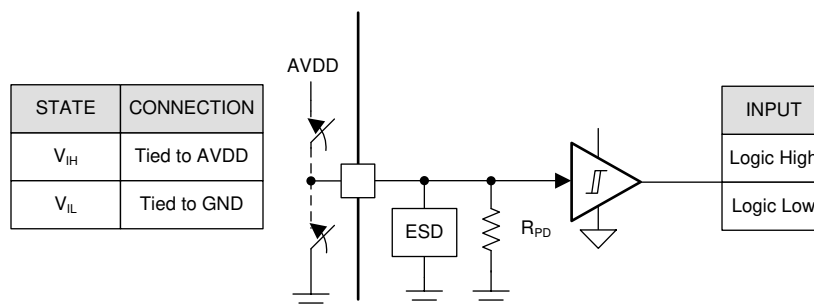


**Figure 8-14. Logic-Level Input Pin Structure**

#### 8.3.9.2 Logic Level Input Pin (Internal Pullup)

Figure 8-15 shows the input structure for the logic level pin  $nSCS$ . The input can be driven with an external resistor to GND or an external logic voltage supply.

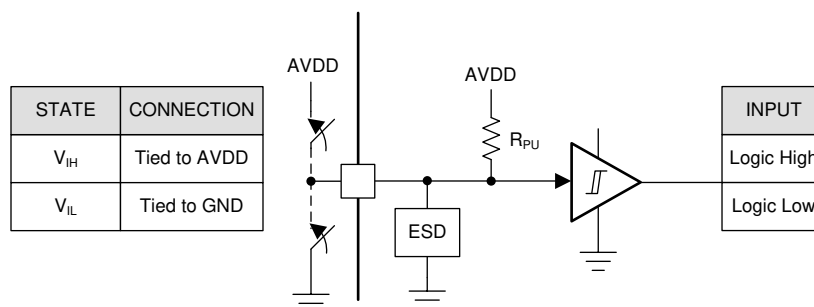


**Figure 8-15. nSCS Input Pin Structure**

### 8.3.9.3 Open Drain Pin

Figure 8-16 shows the structure of the open-drain output pin nFAULT. The open-drain output requires an external pullup resistor to a logic voltage supply to function properly.

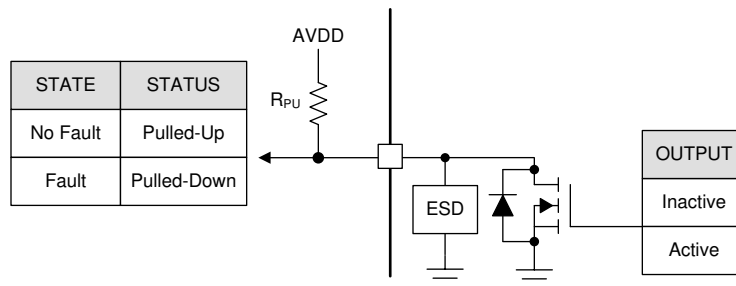


Figure 8-16. Open Drain Output Pin Structure

### 8.3.9.4 Push Pull Pin

Figure 8-17 shows the structure of the push-pull pin SDO.

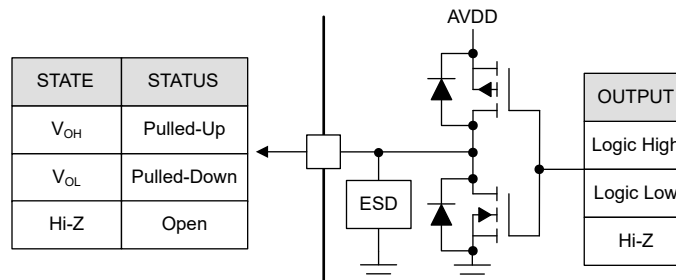


Figure 8-17. Push-Pull Output Pin Structure

### 8.3.9.5 Four Level Input Pin

Figure 8-18 shows the structure of the four level input pins GAIN, MODE and SLEW on hardware interface devices. The input can be set by tying the pin to AGND or AVDD, leaving the pin unconnected, or connecting an external resistor from the pin to ground.

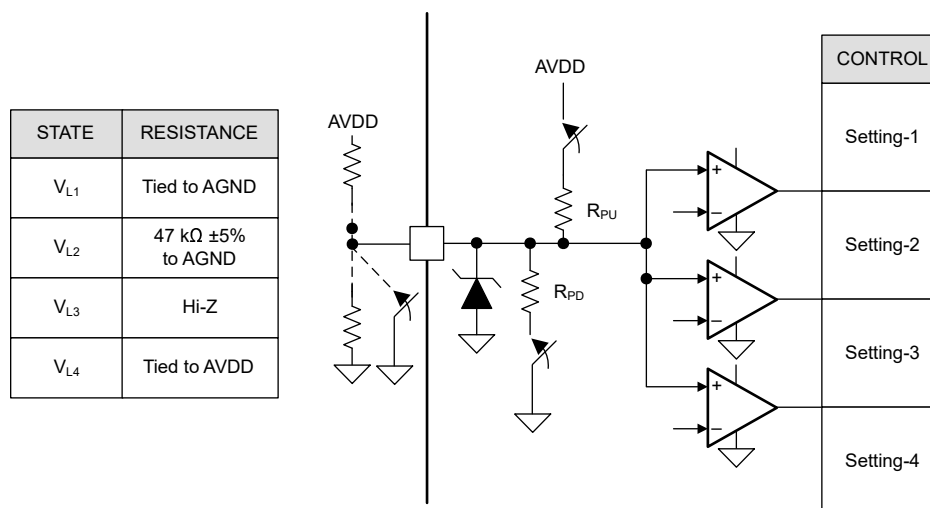


Figure 8-18. Four Level Input Pin Structure

### 8.3.10 Current Sense Amplifiers

The DRV8317 integrates three high-performance low-side current sense amplifiers for current measurements using built-in current sense. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless DC commutation with the external controller. Each amplifier senses the current in the corresponding half-bridge when the low-side MOSFET is conducting. The current sense amplifiers include features such as configurable gain (through CSA\_GAIN register or GAIN pin) and an external voltage reference (VREF) provided through CSAREF pin.

#### 8.3.10.1 Current Sense Amplifier Operation

The SOx pin on the DRV8317 provides an analog voltage proportional to the current flowing in the low side MOSFETs ( $I_{OUTx}$ ) multiplied by the gain setting ( $G_{CSA}$ ) of the current sense amplifier. The gain setting is adjustable between four different levels which can be set by the GAIN pin (hardware variant) or the CSA\_GAIN register (SPI variant).

Figure 8-19 shows the internal architecture of the current sense amplifiers. The current sense is implemented with a sense FET on each low-side FET of the DRV8317 device. This current information is converted in to a voltage based on the CSAREF pin (VREF) input and the CSA gain setting; this voltage is available on the SOx pin. The CSA output voltage can be calculated using Equation 2

$$SOx = V_{REF}/2 + (G_{CSA} * I_{OUTx}), \text{ wherein } I_{OUTx} \text{ is considered positive in the direction shown in Figure 8-19.} \quad (2)$$

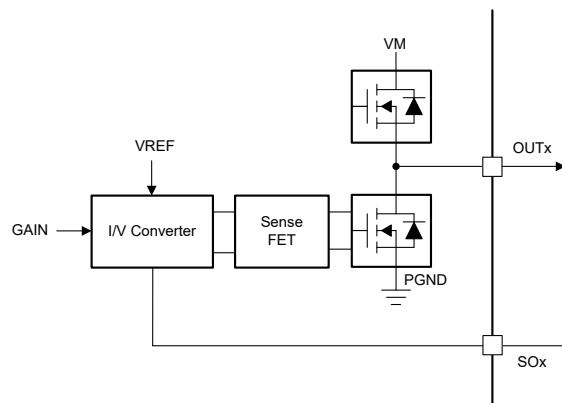


Figure 8-19. Integrated Current Sense Amplifier

Figure 8-20 shows the  $I_{OUTx}$  to CSA output transfer function. In bi-directional operation, the amplifier output for 0-A input is set at  $V_{REF}/2$ . Any change in the output phase current results in a corresponding change in the amplifier output as given in Equation 2.

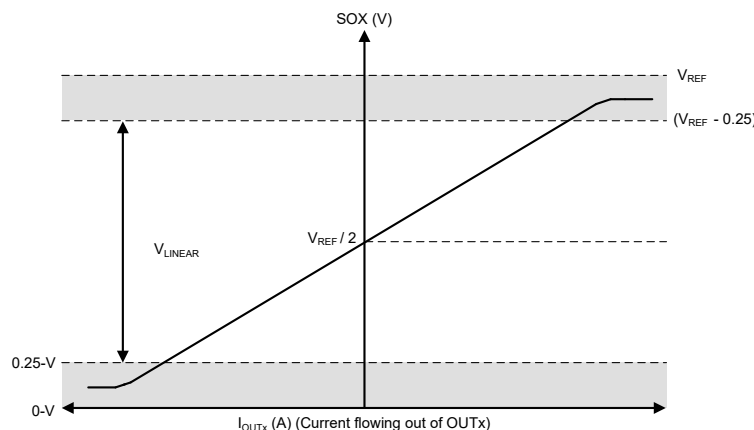


Figure 8-20. IOUtx to CSA Transfer Function

The amplifier has a defined linear region as shown in Figure 8-21.

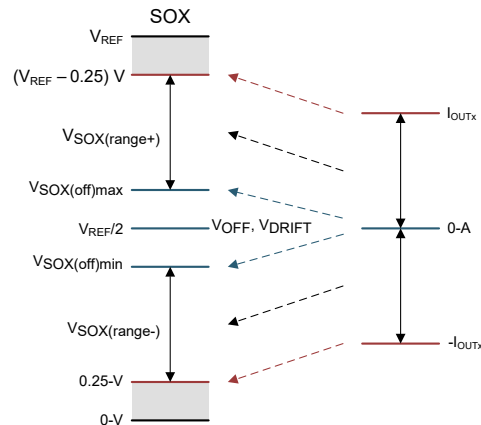


**Figure 8-21. Bi-directional Current Sense Linear Region**

**Note**

The current sense amplifiers use the external voltage reference (VREF) provided at the CSAREF pin.

### 8.3.11 Protections

The DRV8317 is protected against VM, VIN\_AVDD, AVDD, CP under voltage, VM over voltage, SPI fault, OTP read fault, FET over current and FET, LDO over temperature events. Table 8-6 summarizes various fault details.

**Table 8-6. Fault Action and Response**

| FAULT                                | CONDITION                                     | CONFIGURATION        | REPORT | PRE-DRIVER | FAULT STATUS BITS | DIGITAL | RECOVERY                                                   |
|--------------------------------------|-----------------------------------------------|----------------------|--------|------------|-------------------|---------|------------------------------------------------------------|
| VM under voltage lockout (VM_UV)     | $V_{VM} < V_{UVLO}$ (falling)                 | UVP_MODE = 00b       | nFAULT | Hi-Z       | Latched           | Active  | Automatic: SLOW_TRETRY and $V_{VM} > V_{UVLO}$ (rising)    |
|                                      |                                               | UVP_MODE = 01b       | nFAULT | Hi-Z       | Latched           | Active  | Automatic: FAST_TRETRY and $V_{VM} > V_{UVLO}$ (rising)    |
| VM under voltage warning (VMUV_WARN) | $V_{VM} < V_{VMUV\_WARN\_FALL}$               | VMUV_WARN_MODE = 00b | nFAULT | Hi-Z       | Latched           | Active  | Automatic: SLOW_TRETRY and $V_{VM} > V_{VMUV\_WARN\_RISE}$ |
|                                      |                                               | VMUV_WARN_MODE = 01b | nFAULT | Hi-Z       | Latched           | Active  | Automatic: FAST_TRETRY and $V_{VM} > V_{VMUV\_WARN\_RISE}$ |
|                                      |                                               | VMUV_WARN_MODE = 10b | nFAULT | Active     | Latched           | Active  | No action; report only mode                                |
|                                      |                                               | VMUV_WARN_MODE = 11b | —      | Active     | —                 | Active  | —                                                          |
| VIN_AVDD under voltage (VIN_AVDD_UV) | $V_{VIN\_AVDD} < V_{VIN\_AVDD\_UV}$ (falling) | —                    | —      | Hi-Z       | —                 | Reset   | Automatic: $V_{VIN\_AVDD} > V_{VIN\_AVDD\_UV}$ (rising)    |
| AVDD under voltage (AVDD_UV)         | $V_{AVDD} < V_{AVDD\_UV}$ (falling)           | —                    | —      | Hi-Z       | —                 | Reset   | Automatic: $V_{AVDD} > V_{AVDD\_UV}$ (rising)              |
| Charge pump under voltage (CP_UV)    | $V_{CP} < V_{CPUV}$ (falling)                 | UVP_MODE = 00b       | nFAULT | Hi-Z       | Latched           | Active  | Automatic: SLOW_TRETRY and $V_{CP} > V_{CPUV}$ (rising)    |
|                                      |                                               | UVP_MODE = 01b       | nFAULT | Hi-Z       | Latched           | Active  | Automatic: FAST_TRETRY and $V_{CP} > V_{CPUV}$ (rising)    |
| Over current protection (OCP)        | $I_{PHASE} > I_{OCP}$                         | OCP_MODE = 000b      | nFAULT | Hi-Z       | Latched           | Active  | Automatic: SLOW_TRETRY                                     |
|                                      |                                               | OCP_MODE = 001b      | nFAULT | Hi-Z       | Latched           | Active  | Automatic: FAST_TRETRY                                     |
|                                      |                                               | OCP_MODE = 010b      | nFAULT | Hi-Z       | Latched           | Active  | Latched: Cleared by FLT_CLR bit or nSLEEP reset pulse      |
|                                      |                                               | OCP_MODE = 011b      | nFAULT | Active     | Latched           | Active  | No action; report only mode                                |

**Table 8-6. Fault Action and Response (continued)**

| FAULT                                        | CONDITION                   | CONFIGURATION    | REPORT | PRE-DRIVER | FAULT STATUS BITS | DIGITAL | RECOVERY                                                               |
|----------------------------------------------|-----------------------------|------------------|--------|------------|-------------------|---------|------------------------------------------------------------------------|
| VM over voltage protection (VM_OV)           | $V_{VM} > V_{OVP}$ (rising) | OVP_MODE = 00b   | nFAULT | Hi-Z       | Latched           | Active  | Automatic:<br>SLOW_TRETRY and $V_{VM} < V_{OVP}$ (falling)             |
|                                              |                             | OVP_MODE = 01b   | nFAULT | Hi-Z       | Latched           | Active  | Automatic:<br>FAST_TRETRY and $V_{VM} < V_{OVP}$ (falling)             |
| SPI fault (SPIFLT)                           | SCLK fault and ADDR fault   | SPIFLT_MODE = 0b | nFAULT | Active     | Latched           | Active  | No action; report only mode                                            |
|                                              |                             | SPIFLT_MODE = 1b | —      | Active     | —                 | Active  | —                                                                      |
| System (OTP read) (SYSFLT)                   | OTP read parity fault       | —                | nFAULT | Disabled   | Latched           | Active  | Latched:<br>Cleared by FLT_CLR bit or nSLEEP reset pulse               |
| FET over temperature warning (OTW_FET)       | $T_J > T_{OTW\_FET}$        | OTF_MODE = 00b   | nFAULT | Hi-Z       | Latched           | Active  | Automatic:<br>SLOW_TRETRY and $T_J < T_{OTW\_FET} - T_{OTW\_FET\_HYS}$ |
|                                              |                             | OTF_MODE = 01b   | nFAULT | Hi-Z       | Latched           | Active  | Automatic:<br>FAST_TRETRY and $T_J < T_{OTW\_FET} - T_{OTW\_FET\_HYS}$ |
| FET over temperature shutdown (OTS_FET)      | $T_J > T_{OTS\_FET}$        | OTF_MODE = 00b   | nFAULT | Hi-Z       | Latched           | Active  | Automatic:<br>SLOW_TRETRY and $T_J < T_{OTS\_FET} - T_{OTS\_FET\_HYS}$ |
|                                              |                             | OTF_MODE = 01b   | nFAULT | Hi-Z       | Latched           | Active  | Automatic:<br>FAST_TRETRY and $T_J < T_{OTS\_FET} - T_{OTS\_FET\_HYS}$ |
| AVDD LDO over temperature shutdown (OTS_LDO) | $T_J > T_{OTS\_LDO}$        | —                | —      | Hi-Z       | —                 | Reset   | Automatic:<br>$T_J < T_{OTS\_LDO} - T_{OTS\_LDO\_HYS}$                 |

### 8.3.11.1 Under Voltage Protection (UVP)

DRV8317 has under voltage protection enabled for VM, VIN\_AVDD, AVDD and CP voltage rails - these fault protections cannot be disabled. VM, VIN\_AVDD and AVDD under voltage faults result in device reset; CP under voltage fault response is user configurable through UVP mode.

#### VM, VIN\_AVDD, AVDD Under Voltage Protection (VIN\_AVDD\_UV, AVDD\_UV)

If at any time, the voltage on VIN\_AVDD or AVDD pin falls below the corresponding under voltage falling threshold ( $V_{VIN\_AVDD\_UV}$  or  $V_{AVDD\_UV}$ ), DRV8317 enters reset - in reset, FETs are in Hi-Z, pre-driver, charge pump, current sense amplifier and digital logic are disabled. Normal device operation resumes automatically after the respective rail voltage rises above the corresponding under voltage rising threshold ( $V_{VIN\_AVDD\_UV}$  or  $V_{AVDD\_UV}$ ) as shown in Figure 8-22.

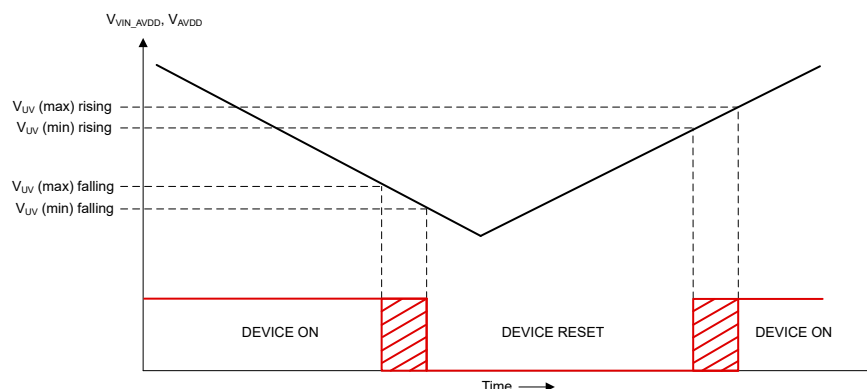


**Figure 8-22. VIN\_AVDD, AVDD Under Voltage Protection**

#### VM, CP Under Voltage Protection (VM\_UV, CP\_UV)

If at any time the voltage on VM or CP pin falls below the corresponding under voltage falling threshold ( $V_{VM\_UV}$  or  $V_{CP\_UV}$ ), FETs are in Hi-Z, charge pump is disabled, nFAULT pin is driven low, FAULT and UVP in DEV\_STS

and VM\_UV or CP\_UV in SUP\_STS are set to 1b. Normal operation resumes automatically (pre-driver, charge pump operation and the nFAULT pin is released) once the retry time ( $t_{RETRY}$ ) lapses after VM or CP voltage is above the corresponding under voltage rising threshold ( $V_{VM\_UV}$  or  $V_{CP\_UV}$ ) as shown in Figure 8-23. The FAULT, UVP and UV\_UV or CP\_UV bits stay set to 1b until a clear fault command is issued either through the FLT\_CLR bit or an nSLEEP reset pulse ( $t_{RST}$ ).

Retry time ( $t_{RETRY}$ ) is set by,

- Slow retry time (SLOW\_TRETRY) by configuring UVP\_MODE to 00b
- Fast retry time (FAST\_TRETRY) by configuring UVP\_MODE to 01b

IN DRV8317H, UVP\_MODE is set to 01b and FAST\_TRETRY is fixed at 5-ms.

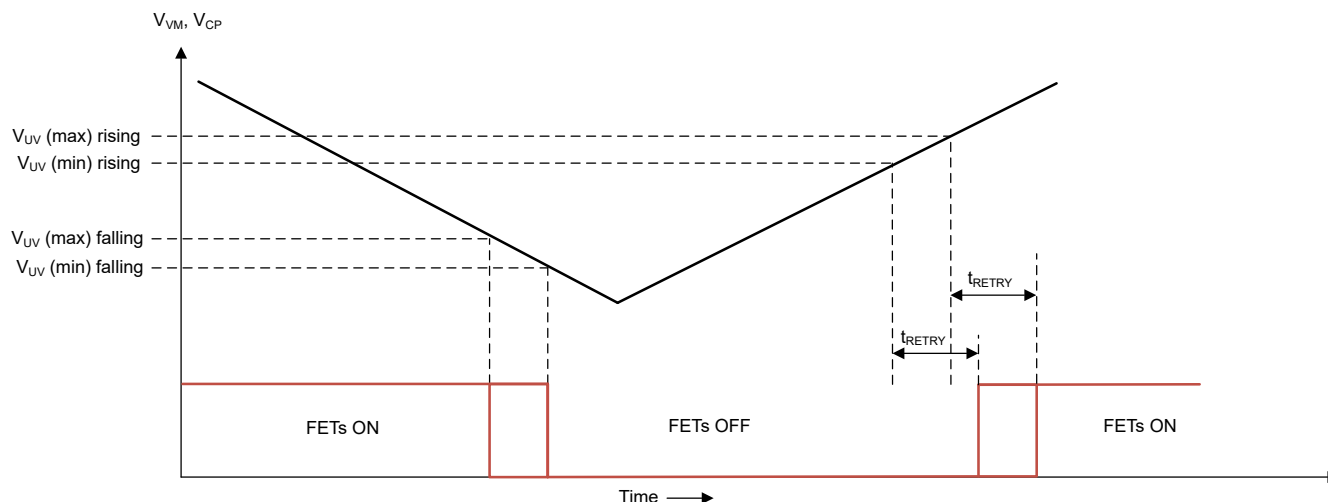


**Figure 8-23. VM, CP Under Voltage Protection**

### 8.3.11.2 VM Under Voltage Warn (VMUV\_WARN) Protection

DRV8317 provides user configurable thresholds ( $V_{VMUV\_WARN\_FALL}$ ,  $V_{VMUV\_WARN\_RISE}$ ) for VM under voltage warn protection. If at any time, voltage on VM pin falls below the  $V_{VMUV\_WARN\_FALL}$  threshold, action is taken as per VMUV\_WARN\_MODE configuration. There are four settings for VMUV\_WARN\_MODE: automatic retry with slow and fast retry time, report only and disabled. The threshold for the VM under voltage warn fault condition to be removed is set by  $V_{VMUV\_WARN\_RISE}$ . This fault can be enabled/ disabled using VMUV\_WARN\_EN. In DRV8317H, this fault is enabled by default and set to report only mode (VMUV\_WARN\_MODE set to 10b).

#### 8.3.11.2.1 VM Under Voltage Warn Automatic Retry (VMUV\_WARN\_MODE = 00b or 01b)

After a VM under voltage warn event in this mode, all the FETs are in Hi-Z and the nFAULT pin is driven low. The FAULT, UVW bits (in DEV\_STS register) and VMUV\_WARN bit (in SUP\_STS register) are set to 1b. Normal operation resumes automatically (pre-driver operation and the nFAULT pin is released) once the retry time ( $t_{RETRY}$ ) time lapses after the VM pin voltage rises above the  $V_{VMUV\_WARN\_RISE}$  threshold as shown in Figure 8-24. The FAULT, UVW and VMUV\_WARN bits stay set to 1b until clear fault command is issued either through the FLT\_CLR bit or an nSLEEP reset pulse ( $t_{RST}$ ).

Retry time ( $t_{RETRY}$ ) is set by,

- Slow retry time (SLOW\_TRETRY) by configuring VPWR\_MODE to 00b
- Fast retry time (FAST\_TRETRY) by configuring VPWR\_MODE to 01b

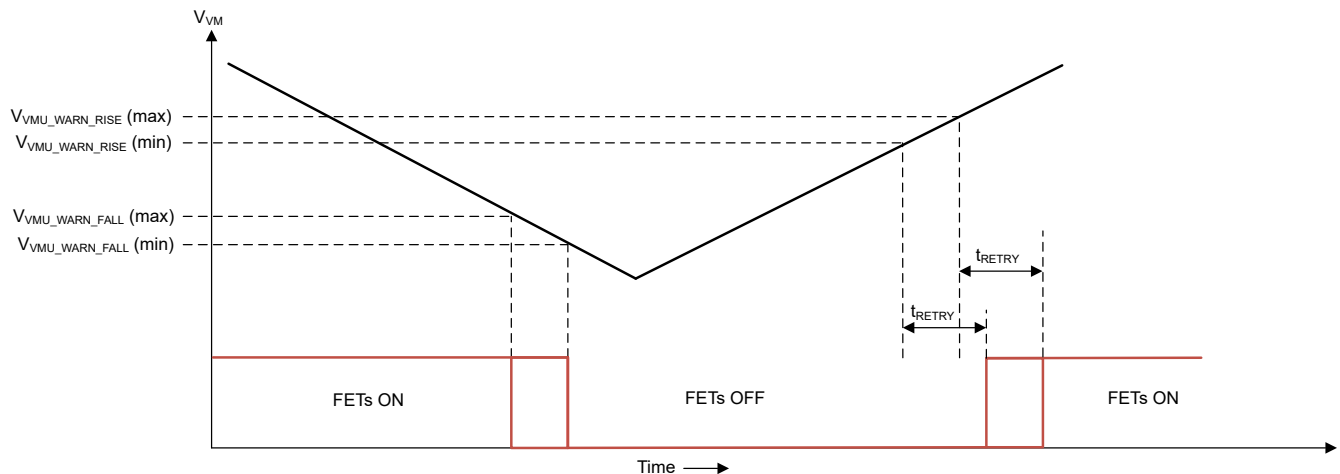


**Figure 8-24. VM Under Voltage Warning**

#### 8.3.11.2.2 VM Under Voltage Warn Report Only (VMUV\_WARN\_MODE = 10b)

No protective action occurs after a VM under voltage warn event in this mode. The VM under voltage warn event is reported by driving the nFAULT pin low and setting the FAULT, UVW bits (in DEV\_STS register) and VMUV\_WARN bit (in SUP\_STS register) to 1b. DRV8317 continues to operate as usual. The external controller manages the VM under voltage warn condition by acting appropriately. The reporting clears (nFAULT pin is released, FAULT, UVW and VMUV\_WARN bits are set to 0b) when a clear fault command is issued either through the FLT\_CLR bit or an nSLEEP reset pulse ( $t_{RST}$ ).

#### 8.3.11.2.3 VM Under Voltage Warn Disabled (VMUV\_WARN\_MODE = 11b)

No action is taken and no reporting (nFAULT pin, status register bits) is done after a VM under voltage warn event in this mode.

### 8.3.11.3 Over Current Protection (OCP)

A MOSFET over current event is sensed by monitoring the current flowing through each of the FETs. If the current through a FET exceeds the OCP threshold ( $I_{OCP}$ ) for longer than the OCP deglitch time ( $t_{OCP}$ ), an OCP event is recognized and action is taken according to OCP\_MODE. In order to avoid false trigger of OCP at PWM transitions, due to ringing in the phase voltage, there is a blanking time ( $t_{BLANK}$ ) applied after each PWM edge. During blanking time, OCP events are ignored.

In DRV8317H, the  $t_{OCP}$  is fixed at 0.6- $\mu$ s (typical),  $t_{BLANK}$  is fixed at 0.7- $\mu$ s (typical) and the OCP\_MODE is set to 001b with retry time of 5-ms. In DRV8317S, the  $t_{OCP}$  is configured by OCP\_DEG, the  $t_{BLANK}$  is configured by OCP\_TBLANK and the OCP\_MODE can be configured in four different modes: OCP latched shutdown, OCP automatic retry with fast and slow retry times and OCP report only.

#### Note

( $t_{OCP} + t_{BLANK}$ ) should not exceed 2- $\mu$ s

#### 8.3.11.3.1 OCP Latched Fault (OCP\_MODE = 010b)

After an OCP event in this mode, all MOSFETs are in Hi-Z and the nFAULT pin is driven low. The FAULT, OCP bits (in DEV\_STS register) and corresponding FETs' OCP bits (in DRV\_STS register) are set to 1b. Normal operation resumes (pre-driver operation, FAULT, OCP, corresponding FETs' OCP bits set to 0b and the nFAULT pin is released) when a clear fault command is issued either through the FLT\_CLR bit or an nSLEEP reset pulse ( $t_{RST}$ ).

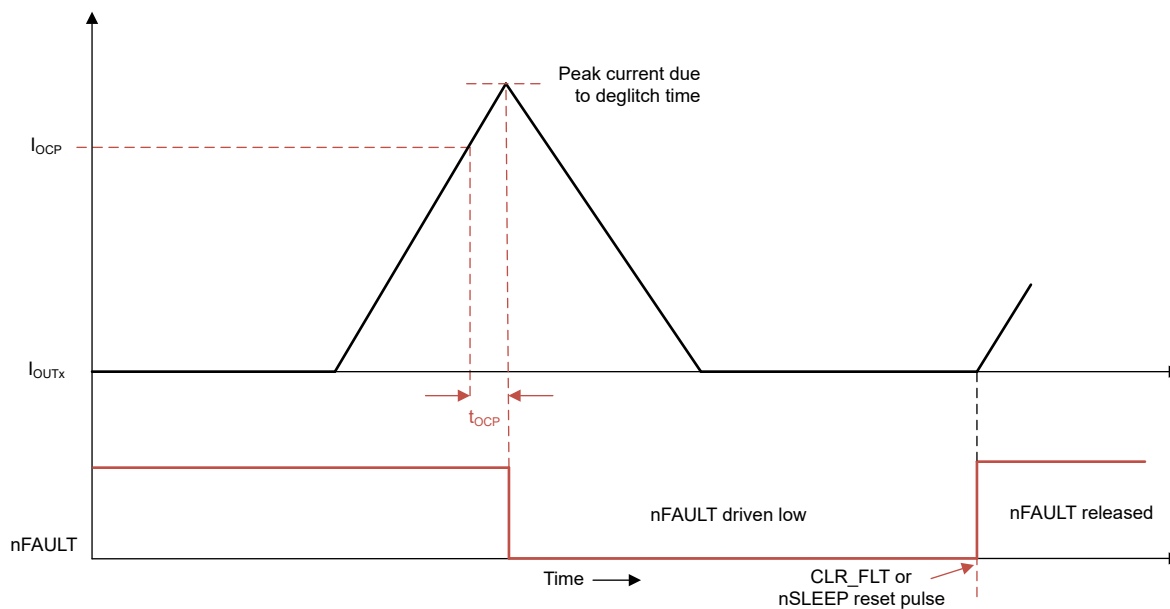


**Figure 8-25. Over Current Protection - Latched Mode**

#### 8.3.11.3.2 OCP Automatic Retry (OCP\_MODE = 000b or 001b)

After an OCP event in this mode, all the FETs are in Hi-Z and the nFAULT pin is driven low. The FAULT, OCP bits (in DEV\_STS register) and corresponding FETs' OCP bits (in DRV\_STS register) are set to 1b. Normal operation resumes automatically (pre-driver operation, the nFAULT pin is released and corresponding FETs' OCP bits are set to 1b) after the retry time ( $t_{RETRY}$ ) time elapses. The FAULT and OCP bits stay set to 1b until clear fault command is issued either through the FLT\_CLR bit or an nSLEEP reset pulse ( $t_{RST}$ ).

Retry time ( $t_{RETRY}$ ) is set by,

- Slow retry time (SLOW\_TRETRY) by configuring OCP\_MODE to 000b
- Fast retry time (FAST\_TRETRY) by configuring OCP\_MODE to 001b

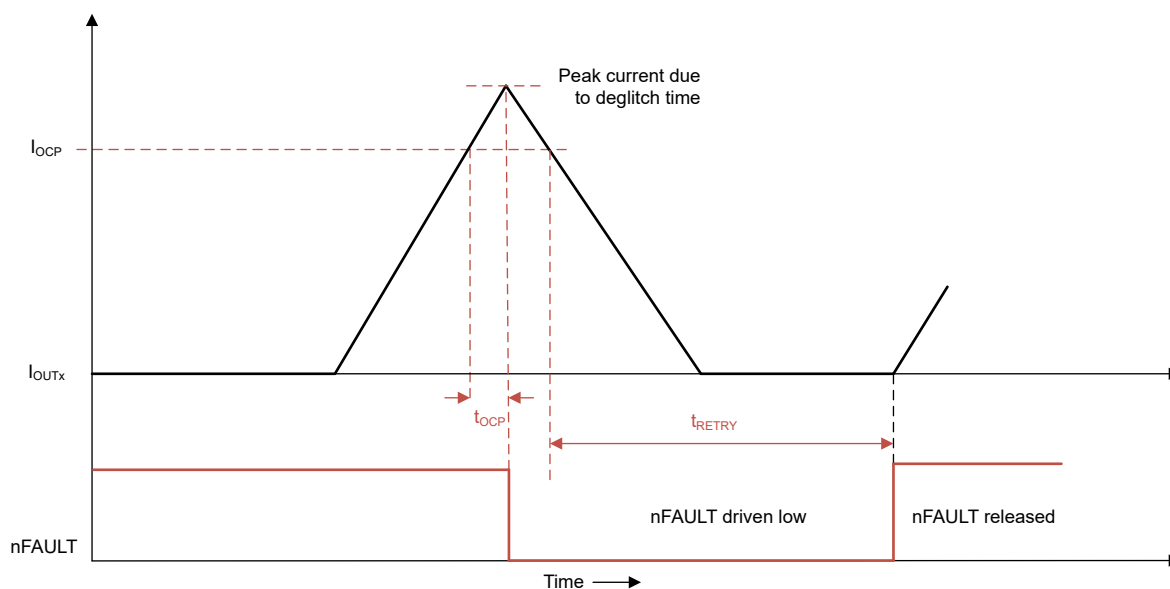


**Figure 8-26. Over Current Protection - Automatic Retry Mode**

### 8.3.11.3.3 OCP Report Only (OCP\_MODE = 011b)

No protective action occurs after an OCP event in this mode. The over current event is reported by driving the nFAULT pin low and setting the FAULT, OCP bits (in DEV\_STS register) and corresponding FETs' OCP bits (in DRV\_STS register) to 1b. DRV8317 continues to operate as usual. The external controller manages the over current condition by acting appropriately. The reporting clears (nFAULT pin is released, FAULT, OCP, and corresponding FETs' OCP bits are set to 0b) when a clear fault command is issued either through the FLT\_CLR bit or an nSLEEP reset pulse ( $t_{RST}$ ).

### 8.3.11.4 VM Over Voltage Protection (OVP)

If at any time, input supply voltage on the VM pin rises higher than the  $V_{OVP}$  rising threshold, all the integrated FETs are in Hi-Z, FAULT, OVP bits (in DEV\_STS register) and VM\_OV (in SUP\_STS register) are set to 1b and the nFAULT pin is driven low. Normal operation resumes automatically (pre-driver operation and the nFAULT pin is released) once retry time ( $t_{RETRY}$ ) lapses after VM pin voltage is below the  $V_{OVP}$  falling threshold as shown in Figure 8-27. The FAULT, OVP and VM\_OV bits stay set to 1b until clear fault command is issued either through the FLT\_CLR bit or an nSLEEP reset pulse ( $t_{RST}$ ).

Retry time ( $t_{RETRY}$ ) is set by,

- Slow retry time (SLOW\_TRETRY) by configuring OVP\_MODE to 00b
- Fast retry time (FAST\_TRETRY) by configuring OVP\_MODE to 01b

IN DRV8317H, OVP\_MODE is set to 01b and FAST\_TRETRY is fixed at 5-ms.

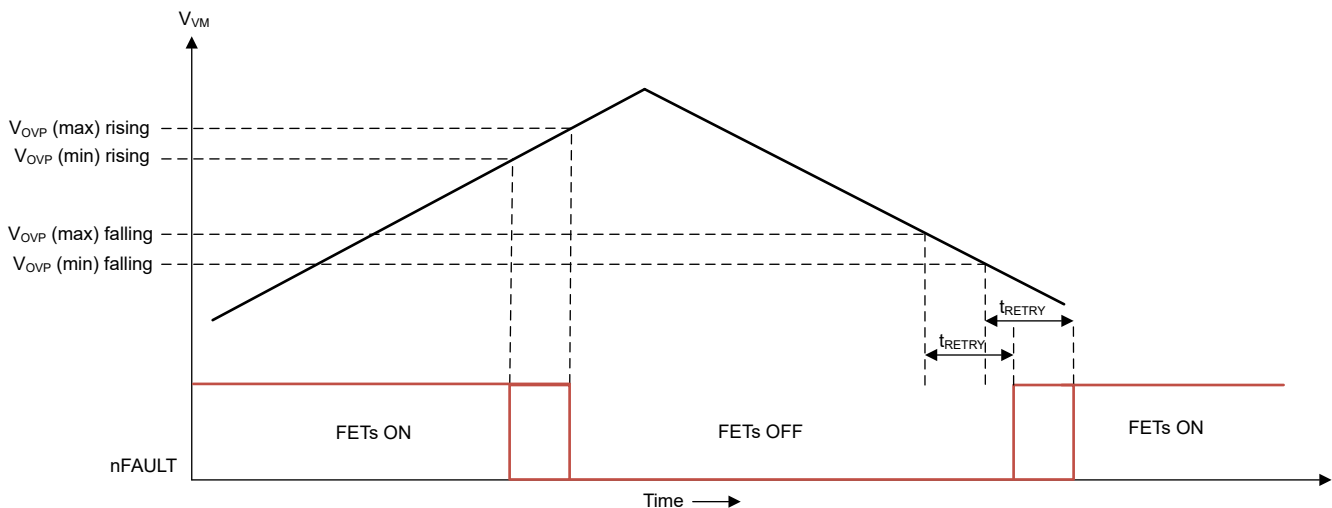


**Figure 8-27. VM Over Voltage Protection**

### 8.3.11.5 SPI Fault

In the event of a SPI transaction fault (parity, frame or bus contention error), if SPLIFLT\_MODE is set to 0b, nFAULT is driven low, FAULT, SPIFLT bits (in DEV\_STS register) and SPI\_PARITY/ BUS\_CNT/ FRM\_ERR bits (in SYSIF\_STS register) are set to 1b. DRV8317 continues to operate as usual. The external controller manages the SPI fault event by acting appropriately. The reporting clears (nFAULT pin is released, FAULT, SPIFLT, and SPI\_PARITY/ BUS\_CNT/ FRM\_ERR bits are set to 0b) when a clear fault command is issued either through the FLT\_CLR bit or an nSLEEP reset pulse ( $t_{RST}$ ).

If SPIFLT\_MODE is set to 1b, SPI fault is disabled and reporting (nFAULT, status register bits) does not happen on a SPI fault event.

### 8.3.11.6 System (OTP Read) Fault

DRV8317 loads the configurable register settings from the OTP on every power-up cycle. If an OTP read fault is encountered while configuring the registers, pre-driver is disabled, FAULT, SYSFLT bits (in DEV\_STS register) and OTPLD\_ERR bit (in SYSIF\_STS register) are set to 1b and nFAULT is driven low. Normal operation resumes (pre-driver, FAULT, SYSFLT, OTPLD\_ERR bits set to 0b and nFAULT pin is released) when a clear

fault command is issued either through the FLT\_CLR bit or an nSLEEP reset pulse ( $t_{RST}$ ). It is advisable not to operate DRV8317 by issuing a clear fault command in the event of a OTP read fault since the register settings may be in an unknown state and may lead to unexpected device operation.

### 8.3.11.7 Thermal Protection

DRV8317 has over temperature warning (OTW) and over temperature shutdown (OTS) features for protection against over temperature events. OTW is available for FET protection (OTW\_FET) while OTS is available for FET (OTS\_FET) and AVDD LDO (OTS\_LDO) protection.

#### 8.3.11.7.1 FET Over Temperature Warning (OTW\_FET)

If the FET temperature exceeds the over temperature warning ( $T_{OTW\_FET}$ ) threshold, the FAULT, OTF bits (in DEV\_STS register) and OTW\_FET bit (in OT\_STS register) are set to 1b and the nFAULT pin is driven low. The nFAULT pin is released and OTW\_FET is set to 0b once retry time ( $t_{RETRY}$ ) elapses after the FET temperature falls below the over temperature warning ( $T_{OTW\_FET} - T_{OTW\_FET\_HYS}$ ) threshold. The FAULT, OTF bits stay set to 1b until cleared through the CLR\_FLT bit or an nSLEEP reset pulse ( $t_{RST}$ ).

Retry time ( $t_{RETRY}$ ) is set by,

- Slow retry time (SLOW\_TRETRY) by configuring OTF\_MODE to 00b
- Fast retry time (FAST\_TRETRY) by configuring OTF\_MODE to 01b

In DRV8317H, FET over temperature warning is disabled.

#### 8.3.11.7.2 FET Over Temperature Shutdown (OTS\_FET)

If the FET temperature exceeds the shutdown threshold ( $T_{OTS\_FET}$ ), all the integrated FETs are in Hi-Z, the FAULT, OTF bits (in DEV\_STS register) and OTS\_FET bit (in OT\_STS register) are set to 1b and the nFAULT pin is driven low. Normal operation resumes automatically (pre-driver operation, nFAULT pin is released and OTS\_FET is set to 0b) after retry time ( $t_{RETRY}$ ) elapses, if FET temperature falls below the over temperature shutdown ( $T_{OTS\_FET} - T_{OTS\_FET\_HYS}$ ) threshold. The FAULT, OTF bits stay set to 1b until cleared through the CLR\_FLT bit or an nSLEEP reset pulse ( $t_{RST}$ ). This feature cannot be disabled.

Retry time ( $t_{RETRY}$ ) is set by,

- Slow retry time (SLOW\_TRETRY) by configuring OTF\_MODE to 00b
- Fast retry time (FAST\_TRETRY) by configuring OTF\_MODE to 01b

IN DRV8317H,  $t_{RETRY}$  period is fixed at 5-ms.

#### 8.3.11.7.3 LDO Over Temperature Shutdown

If AVDD LDO temperature exceeds the LDO over temperature shutdown ( $T_{OTS\_LDO}$ ) threshold, all the integrated FETs are in Hi-Z and device enters reset. Normal operation resumes automatically when AVDD LDO temperature falls below the over temperature shutdown threshold ( $T_{OTS\_LDO} - T_{OTS\_LDO\_HYS}$ ). This feature cannot be disabled.

## 8.4 Device Functional Modes

### 8.4.1 Functional Modes

#### 8.4.1.1 Sleep Mode

The nSLEEP pin manages the state of DRV8317. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode MOSFETs, current sense amplifiers, charge pump, AVDD regulator and SPI bus are disabled. The  $t_{SLEEP}$  time must elapse after a falling edge on the nSLEEP pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The  $t_{WAKE}$  time must elapse before the device is ready for PWM inputs.

### Note

During power up and power down of the device through the nSLEEP pin, the nFAULT pin is held low as the internal regulators are enabled or disabled. After the regulators have enabled or disabled, the nFAULT pin is automatically released. The duration that the nFAULT pin is low does not exceed the  $t_{SLEEP}$  or  $t_{WAKE}$  time.

#### 8.4.1.2 Operating Mode

When the nSLEEP pin is high and the  $V_{VM}$  voltage is greater than the  $V_{UVLO}$  voltage, the device goes to operating mode. The  $t_{WAKE}$  time must elapse before the device is ready for inputs. In this mode the charge pump, AVDD regulator and SPI bus are active.

#### 8.4.1.3 Fault Reset (FLT\_CLR or nSLEEP Reset Pulse)

In the case of latched faults, DRV8317 turns off the MOSFETs (Hi-Z) and the motor coasts to a stop.

When the fault condition clears, the device can go to the operating state again by either setting the FLT\_CLR bit to 1b in the SPI variant or by issuing a reset pulse on the nSLEEP pin in the hardware variant. The nSLEEP reset pulse ( $t_{RST}$ ) consists of a high-to-low-to-high transition on the nSLEEP pin. The low period of the sequence should fall with the  $t_{RST}$  time window or else the device will start the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks.

### 8.5 SPI Communication

#### 8.5.1 Programming

##### 8.5.1.1 SPI Format

#### SPI Format - with Parity

The SDI input data word is 24 bits long and consists of the following format:

- 1 read or write bit, W (bit B23)
- 6 address bits, A (bits B22 through B17)
- Parity bit, P (bit B16)
- 15 data bits with 1 parity bit, D (bits B15 through B0)

The SDO output data word is 24 bits long. The most significant bits are status bits and the least significant 16 bits are the data content of the register being accessed.

**Table 8-7. SDI Input Data Word Format for SPI**

| R/W | ADDRESS |     |     |     |     |     | PAR<br>ITY | PAR<br>ITY | DATA |     |     |     |     |    |    |    |    |    |    |    |    |    |    |
|-----|---------|-----|-----|-----|-----|-----|------------|------------|------|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| B23 | B22     | B21 | B20 | B19 | B18 | B17 | B16        | B15        | B14  | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| W0  | A5      | A4  | A3  | A2  | A1  | A0  | P          | P          | D14  | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 8-8. SDO Output Data Word Format**

| STATUS |     |     |     |     |     |     |     | DATA |     |     |     |     |     |    |    |    |    |    |    |    |    |    |    |
|--------|-----|-----|-----|-----|-----|-----|-----|------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| B23    | B22 | B21 | B20 | B19 | B18 | B17 | B16 | B15  | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| S7     | S6  | S5  | S4  | S3  | S2  | S1  | S0  | D15  | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

The details of the bits used in SPI frame format are detailed below.

**Read/Write Bit (R/W):** R/W (W0) bit set to 0b indicates a SPI write transaction. For a SPI read operation, R/W bit needs to be set to 1b.

**Address Bits (A):** A SPI secondary device takes a 6-bit register address.

**Parity Bit (P):** Both header and data fields of a SPI input data frame include a parity bit for single bit error detection - in [Table 8-7](#), B16 is parity bit for the header field, while B15 is the parity bit for the data field. The

parity scheme used is even parity - the number of ones in a block of 16-bits (including the parity bit) is even. Data will be written to the internal registers only if the parity check is successful. Parity checks can be enabled or disabled by configuring the SPI\_PEN bit of SYS\_CTRL register. Parity checks are disabled by default.

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**Note**

Though parity checks are disabled by default, TI recommends enabling parity checks to safeguard against single-bit errors.

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**Error Handling**

**Parity Error:** Upon detecting a parity error, the secondary device responds in the following ways. Parity error gets latched and reported on nFAULT. The error status is available for read on SPI\_PARITY field of SYS\_STS register. A parity error in the header will not prevent the secondary device from responding with data. The SDO will be driven by the secondary device being addressed. Updates to write address pointer and the device registers will be ignored when parity error is detected. In a sequential write, upon detection of parity error any subsequent register writes will be ignored.

**Frame Error:** Any incomplete SPI Frame will be reported as Frame error. Frame errors will be latched in FRM\_ERR field of SYSIF\_STS register and indicated on nFAULT.

**SPI Read/Write Sequence**

**SPI Read Sequence:** The SPI read transaction comprises of an 8-bit header (R/W - 1 bit, Address - 6 bits, and parity -1 bit) followed by 16-bit dummy data words. Upon receiving the first byte of header, the secondary device responds with an 8-bit device status information. The read address pointer gets updated immediately after receiving the address field of the header. The read address from the header acts as the starting address for the register reads. The read address pointer gets incremented automatically upon completion of a 16-bit transfer. The length of data transfer is not restricted by the secondary device. The secondary device responds with data as long as the primary device transmits dummy words. If parity error check is enabled, the MSB of read data will be replaced with computed parity bit

**SPI Write Sequence:** SPI write transaction comprises of an 8-bit header followed by 16-bit data words to be written into the register bank. Similar to a read transaction, the addressed secondary device responds with an 8-bit device status information upon receiving the first byte of header. Once the header bytes are received, the write address pointer gets updated. The write address from the header acts as the starting address for sequential register writes. The read address pointer will retain the address of the register being read in the previous SPI transaction. The length of data transfer is not restricted by the secondary device. Both read and write address pointers will be incremented automatically upon completion of a 16-bit transfer. While receiving data from the primary device, the SDO will be driven with the register data addressed by read address pointer.

## 8.6 DRV8317 Registers

[Table 8-9](#) lists the memory-mapped registers for the DRV8317 registers. All register offset addresses not listed in [Table 8-9](#) should be considered as reserved locations and the register contents should not be modified.

**Table 8-9. DRV8317 Registers**

| Offset | Acronym       | Register Name                            | Section                        |
|--------|---------------|------------------------------------------|--------------------------------|
| 0h     | DEV_STS       | Device Status Register                   | <a href="#">Section 8.6.1</a>  |
| 2h     | DEV_RSTS      | Device Raw Status Register               | <a href="#">Section 8.6.2</a>  |
| 4h     | OT_STS        | Over Temperature Status Register         | <a href="#">Section 8.6.3</a>  |
| 5h     | SUP_STS       | Supply Status Register                   | <a href="#">Section 8.6.4</a>  |
| 6h     | DRV_STS       | Driver Status Register                   | <a href="#">Section 8.6.5</a>  |
| 7h     | SYSIF_STS     | System Interface Status Register         | <a href="#">Section 8.6.6</a>  |
| 10h    | FLT_MODE      | Fault Mode Register                      | <a href="#">Section 8.6.7</a>  |
| 12h    | SYSF_CTRL     | System Fault Control Register            | <a href="#">Section 8.6.8</a>  |
| 13h    | DRVF_TCTRL    | Driver Fault Control Register            | <a href="#">Section 8.6.9</a>  |
| 16h    | FLT_TCTRL     | Fault Timing Control Register            | <a href="#">Section 8.6.10</a> |
| 17h    | FLT_CLR       | Fault Clear Register                     | <a href="#">Section 8.6.11</a> |
| 18h    | VMUV_WARN_THR | VM Under Voltage Warn Threshold Register | <a href="#">Section 8.6.12</a> |
| 20h    | PWM_CTRL      | PWM Control Register                     | <a href="#">Section 8.6.13</a> |
| 22h    | DRV_CTRL      | Predriver control Register               | <a href="#">Section 8.6.14</a> |
| 23h    | CSA_CTRL      | CSA Control Register                     | <a href="#">Section 8.6.15</a> |
| 3Fh    | SYS_CTRL      | System Control Register                  | <a href="#">Section 8.6.16</a> |

Complex bit access types are encoded to fit into small table cells. [Table 8-10](#) shows the codes that are used for access types in this section.

**Table 8-10. DRV8317 Access Type Codes**

| Access Type                   | Code | Description                            |
|-------------------------------|------|----------------------------------------|
| <b>Read Type</b>              |      |                                        |
| R                             | R    | Read                                   |
| R-0                           | R-0  | Read<br>Returns 0s                     |
| <b>Write Type</b>             |      |                                        |
| W                             | W    | Write                                  |
| <b>Reset or Default Value</b> |      |                                        |
| -n                            |      | Value after reset or the default value |

### 8.6.1 DEV\_STS Register (Offset = 0h) [Reset = 0280h]

DEV\_STS is shown in [Figure 8-28](#) and described in [Table 8-11](#).

Return to the [Table 8-9](#).

**Figure 8-28. DEV\_STS Register**

|        |          |      |      |      |      |           |        |
|--------|----------|------|------|------|------|-----------|--------|
| 15     | 14       | 13   | 12   | 11   | 10   | 9         | 8      |
| PARITY | RESERVED |      |      |      |      | DNRDY_STS | SYSFLT |
| R-0h   | R-0-0h   |      |      |      |      | R-0-1h    | R-0h   |
| 7      | 6        | 5    | 4    | 3    | 2    | 1         | 0      |
| RESET  | SPIFLT   | OCP  | UVW  | OVP  | UVP  | OTF       | FAULT  |
| R-1h   | R-0h     | R-0h | R-0h | R-0h | R-0h | R-0h      | R-0h   |

**Table 8-11. DEV\_STS Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                         |
|-------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | PARITY    | R    | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                                                                                                                                                              |
| 14-10 | RESERVED  | R-0  | 0h    | Reserved                                                                                                                                                                                                                            |
| 9     | DNRDY_STS | R-0  | 1h    | Device not ready status<br>0h = Device is ready to spin motor<br>1h = Device is not ready                                                                                                                                           |
| 8     | SYSFLT    | R    | 0h    | OTP read fault occurred. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP<br>0h = No OTP read fault is detected<br>1h = OTP read fault detected                                                    |
| 7     | RESET     | R    | 1h    | Device power on status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP<br>0h = Cleared by writing 1b to FLT_CLR bit after power-up<br>1h = Device has undergone power on reset                   |
| 6     | SPIFLT    | R    | 0h    | SPI fault status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP<br>0h = No SPI fault is detected<br>1h = SPI fault is detected                                                                  |
| 5     | OCP       | R    | 0h    | Driver over current Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP<br>0h = No over current condition is detected<br>1h = Over current condition is detected                              |
| 4     | UVW       | R    | 0h    | VM under voltage warning fault status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP<br>0h = No VM under voltage warn condition is detected<br>1h = VM under voltage warn condition is detected |
| 3     | OVP       | R    | 0h    | Over voltage status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP<br>0h = No over voltage condition is detected<br>1h = Over voltage condition is detected                                     |
| 2     | UVP       | R    | 0h    | Supply under voltage status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP<br>0h = No under voltage condition is detected on VM or CP<br>1h = Under voltage condition is detected on VM or CP   |
| 1     | OTF       | R    | 0h    | Over temperature fault status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP<br>0h = No over temperature warning / shutdown is detected<br>1h = Over temperature warning / shutdown is detected |
| 0     | FAULT     | R    | 0h    | Device fault status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP<br>0h = No fault condition is detected<br>1h = Fault condition is detected                                                   |

## 8.6.2 DEV\_RSTS Register (Offset = 2h) [Reset = 0000h]

DEV\_RSTS is shown in [Figure 8-29](#) and described in [Table 8-12](#).

Return to the [Table 8-9](#).

**Figure 8-29. DEV\_RSTS Register**

|          |           |          |            |          |          |            |           |
|----------|-----------|----------|------------|----------|----------|------------|-----------|
| 15       | 14        | 13       | 12         | 11       | 10       | 9          | 8         |
| RESERVED |           |          |            |          |          | DNRDY_RSTS | SYSF_RSTS |
| R-0-0h   |           |          |            |          |          | R-0h       | R-0h      |
| 7        | 6         | 5        | 4          | 3        | 2        | 1          | 0         |
| RESERVED | SPIF_RSTS | OCP_RSTS | VMUV_WRSTS | OVP_RSTS | UVP_RSTS | OTF_RSTS   | RESERVED  |
| R-0-0h   | R-0h      | R-0h     | R-0-0h     | R-0-0h   | R-0h     | R-0h       | R-0-0h    |

**Table 8-12. DEV\_RSTS Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                 |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-10 | RESERVED   | R-0  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                    |
| 9     | DNRDY_RSTS | R    | 0h    | Device not ready indicator<br>0h = Device not ready to drive PWMs<br>1h = Device ready to drive PWMs                                                                                                                                                                                                                                        |
| 8     | SYSF_RSTS  | R    | 0h    | OTP parity error during load, raw status. Cleared by write to FLT_CLR or reset pulse on nSLEEP<br>0h = No parity error during OTP load<br>1h = Parity error occurred during OTP load                                                                                                                                                        |
| 7     | RESERVED   | R-0  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                    |
| 6     | SPIF_RSTS  | R    | 0h    | SPI fault raw status. Cleared by write to FLT_CLR or reset pulse on nSLEEP<br>0h = No SPI fault is detected<br>1h = SPI fault is detected                                                                                                                                                                                                   |
| 5     | OCP_RSTS   | R    | 0h    | Driver OCP raw status. Auto cleared if retry is enabled in OCP_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No over current condition is detected<br>1h = Over current condition is detected                                                                                                             |
| 4     | VMUV_WRSTS | R-0  | 0h    | VM under voltage warning fault raw status. Auto cleared if retry is enabled in VMUV_WARN_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No VM under voltage warn condition is detected (VM > VMUV_WARN_RISE threshold)<br>1h = VM under voltage warn condition is detected (VM < VMUV_WARN_FALL threshold) |
| 3     | OVP_RSTS   | R-0  | 0h    | Over voltage protection fault raw status. Auto cleared if retry is enabled in OVP_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No over voltage condition on VM is detected<br>1h = VM over voltage condition is detected                                                                                 |
| 2     | UVP_RSTS   | R    | 0h    | Under voltage protection fault raw status. Auto cleared if retry is enabled in UVP_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No under voltage condition is detected on VM or CP<br>1h = Under voltage condition is detected on VM or CP                                                               |
| 1     | OTF_RSTS   | R    | 0h    | Over temperature fault raw status. Auto cleared if retry is enabled in OTF_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No over temperature warning/shutdown is detected<br>1h = Over temperature warning/shutdown is detected                                                                           |
| 0     | RESERVED   | R-0  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                    |

### 8.6.3 OT\_STS Register (Offset = 4h) [Reset = 0000h]

OT\_STS is shown in [Figure 8-30](#) and described in [Table 8-13](#).

Return to the [Table 8-9](#).

**Figure 8-30. OT\_STS Register**

|          |          |    |    |          |         |         |   |
|----------|----------|----|----|----------|---------|---------|---|
| 15       | 14       | 13 | 12 | 11       | 10      | 9       | 8 |
| PARITY   | RESERVED |    |    |          |         |         |   |
| R-0h     | R-0-0h   |    |    |          |         |         |   |
| 7        | 6        | 5  | 4  | 3        | 2       | 1       | 0 |
| RESERVED |          |    |    | RESERVED | OTW_FET | OTS_FET |   |
| R-0-0h   |          |    |    | R-0h     | R-0h    | R-0h    |   |

**Table 8-13. OT\_STS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                        |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | PARITY   | R    | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                                                                                                                                                                                             |
| 14-3 | RESERVED | R-0  | 0h    | Reserved                                                                                                                                                                                                                                                           |
| 2    | RESERVED | R    | 0h    | Reserved                                                                                                                                                                                                                                                           |
| 1    | OTW_FET  | R    | 0h    | FET over temperature warning fault status. Auto cleared if retry is enabled in OTF_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No FET over temperature warning is detected<br>1h = FET over temperature warning is detected    |
| 0    | OTS_FET  | R    | 0h    | FET over temperature shutdown fault status. Auto cleared if retry is enabled in OTF_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No FET over temperature shutdown is detected<br>1h = FET over temperature shutdown is detected |

## 8.6.4 SUP\_STS Register (Offset = 5h) [Reset = 0000h]

SUP\_STS is shown in [Figure 8-31](#) and described in [Table 8-14](#).

Return to the [Table 8-9](#).

**Figure 8-31. SUP\_STS Register**

|           |          |          |       |          |          |        |          |
|-----------|----------|----------|-------|----------|----------|--------|----------|
| 15        | 14       | 13       | 12    | 11       | 10       | 9      | 8        |
| PARITY    | RESERVED |          |       |          |          |        |          |
| R-0h      | R-0-0h   |          |       |          |          |        |          |
| 7         | 6        | 5        | 4     | 3        | 2        | 1      | 0        |
| VMUV_WARN | VM_OV    | RESERVED | CP_UV | RESERVED | RESERVED | VM_UV  | RESERVED |
| R-0-0h    | R-0-0h   | R-0-0h   | R-0h  | R-0-0h   | R-0h     | R-0-0h | R-0h     |

**Table 8-14. SUP\_STS Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                 |
|------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | PARITY    | R    | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                                                                                                                                                                                                      |
| 14-8 | RESERVED  | R-0  | 0h    | Reserved                                                                                                                                                                                                                                                                    |
| 7    | VMUV_WARN | R-0  | 0h    | VM under voltage warning fault status. This bit is not auto cleared even when retry is enabled in VMUV_WARN_MODE. Can be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No VM under voltage warning is detected<br>1h = VM under voltage warning is detected |
| 6    | VM_OV     | R-0  | 0h    | VM over voltage fault status. This bit is not auto cleared even when retry is enabled in OVP_MODE. Can be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No VM over voltage is detected<br>1h = VM over voltage is detected                                  |
| 5    | RESERVED  | R-0  | 0h    | Reserved                                                                                                                                                                                                                                                                    |
| 4    | CP_UV     | R    | 0h    | Charge pump under voltage fault status. This bit is not auto cleared even when retry is enabled in UVP_MODE. Can be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No charge pump under voltage is detected<br>1h = Charge pump under voltage is detected    |
| 3    | RESERVED  | R-0  | 0h    | Reserved                                                                                                                                                                                                                                                                    |
| 2    | RESERVED  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                    |
| 1    | VM_UV     | R-0  | 0h    | VM under voltage fault status. This bit is not auto cleared even when retry is enabled in UVP_MODE. Can be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No VM under voltage is detected<br>1h = VM under voltage is detected                               |
| 0    | RESERVED  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                    |

### 8.6.5 DRV\_STS Register (Offset = 6h) [Reset = 0000h]

DRV\_STS is shown in [Figure 8-32](#) and described in [Table 8-15](#).

Return to the [Table 8-9](#).

**Figure 8-32. DRV\_STS Register**

|          |          |         |           |          |         |         |           |
|----------|----------|---------|-----------|----------|---------|---------|-----------|
| 15       | 14       | 13      | 12        | 11       | 10      | 9       | 8         |
| PARITY   | RESERVED |         |           |          |         |         |           |
| R-0h     | R-0-0h   |         |           |          |         |         |           |
| 7        | 6        | 5       | 4         | 3        | 2       | 1       | 0         |
| RESERVED | OCPC_HS  | OCPB_HS | OCA_PA_HS | RESERVED | OCPC_LS | OCPB_LS | OCA_PA_LS |
| R-0-0h   | R-0h     | R-0h    | R-0h      | R-0-0h   | R-0h    | R-0h    | R-0h      |

**Table 8-15. DRV\_STS Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                             |
|------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | PARITY    | R    | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                                                                                                                                                                                                                  |
| 14-7 | RESERVED  | R-0  | 0h    | Reserved                                                                                                                                                                                                                                                                                |
| 6    | OCPC_HS   | R    | 0h    | Over current status on high-side MOSFET of OUTC. Auto cleared if retry is enabled in OCP_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No over current detected on high-side MOSFET of OUTC<br>1h = Over current detected on high-side MOSFET of OUTC |
| 5    | OCPB_HS   | R    | 0h    | Over current status on high-side MOSFET of OUTB. Auto cleared if retry is enabled in OCP_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No over current detected on high-side MOSFET of OUTB<br>1h = Over current detected on high-side MOSFET of OUTB |
| 4    | OCA_PA_HS | R    | 0h    | Over current status on high-side MOSFET of OUTA. Auto cleared if retry is enabled in OCP_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No over current detected on high-side MOSFET of OUTA<br>1h = Over current detected on high-side MOSFET of OUTA |
| 3    | RESERVED  | R-0  | 0h    | Reserved                                                                                                                                                                                                                                                                                |
| 2    | OCPC_LS   | R    | 0h    | Over current status on low-side MOSFET of OUTC. Auto cleared if retry is enabled in OCP_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No over current detected on low-side MOSFET of OUTC<br>1h = Over current detected on low-side MOSFET of OUTC    |
| 1    | OCPB_LS   | R    | 0h    | Over current status on low-side MOSFET of OUTB. Auto cleared if retry is enabled in OCP_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No over current detected on low-side MOSFET of OUTB<br>1h = Over current detected on low-side MOSFET of OUTB    |
| 0    | OCA_PA_LS | R    | 0h    | Over current status on low-side MOSFET of OUTA. Auto cleared if retry is enabled in OCP_MODE. Can also be cleared by write to FLT_CLR or reset pulse on nSLEEP.<br>0h = No over current detected on low-side MOSFET of OUTA<br>1h = Over current detected on low-side MOSFET of OUTA    |

### 8.6.6 SYSIF\_STS Register (Offset = 7h) [Reset = 0000h]

SYSIF\_STS is shown in [Figure 8-33](#) and described in [Table 8-16](#).

Return to the [Table 8-9](#).

**Figure 8-33. SYSIF\_STS Register**

|          |          |    |           |          |            |         |         |
|----------|----------|----|-----------|----------|------------|---------|---------|
| 15       | 14       | 13 | 12        | 11       | 10         | 9       | 8       |
| PARITY   | RESERVED |    |           |          |            |         |         |
| R-0h     | R-0-0h   |    |           |          |            |         |         |
| 7        | 6        | 5  | 4         | 3        | 2          | 1       | 0       |
| RESERVED |          |    | OTPLD_ERR | RESERVED | SPI_PARITY | BUS_CNT | FRM_ERR |
| R-0-0h   |          |    | R-0h      | R-0-0h   | R-0h       | R-0h    | R-0h    |

**Table 8-16. SYSIF\_STS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                           |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 15   | PARITY     | R    | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                                                |
| 14-5 | RESERVED   | R-0  | 0h    | Reserved                                                                                                              |
| 4    | OTPLD_ERR  | R    | 0h    | OTP parity error during load<br>0h = No OTP read error is detected<br>1h = OTP read error is detected                 |
| 3    | RESERVED   | R-0  | 0h    | Reserved                                                                                                              |
| 2    | SPI_PARITY | R    | 0h    | SPI parity error<br>0h = No SPI Parity Error is detected<br>1h = SPI Parity Error is detected                         |
| 1    | BUS_CNT    | R    | 0h    | SPI bus contention error<br>0h = No SPI Bus Contention Error is detected<br>1h = SPI Bus Contention Error is detected |
| 0    | FRM_ERR    | R    | 0h    | SPI frame error<br>0h = No SPI Frame Error is detected<br>1h = SPI Frame Error is detected                            |

### 8.6.7 FLT\_MODE Register (Offset = 10h) [Reset = 0015h]

FLT\_MODE is shown in [Figure 8-34](#) and described in [Table 8-17](#).

Return to the [Table 8-9](#).

**Figure 8-34. FLT\_MODE Register**

|             |          |    |                |          |          |          |          |
|-------------|----------|----|----------------|----------|----------|----------|----------|
| 15          | 14       | 13 | 12             | 11       | 10       | 9        | 8        |
| PARITY      | RESERVED |    | VMUV_WARN_MODE |          | OVP_MODE |          | RESERVED |
| R/W-0h      | R-0-0h   |    | R/W-0h         |          | R/W-0h   |          | R/W-0h   |
| 7           | 6        | 5  | 4              | 3        | 2        | 1        | 0        |
| SPIFLT_MODE | OCP_MODE |    |                | UVP_MODE |          | OTF_MODE |          |
| R/W-0h      | R/W-1h   |    |                | R/W-1h   |          | R/W-1h   |          |

**Table 8-17. FLT\_MODE Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | PARITY         | R/W  | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 14-13 | RESERVED       | R-0  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 12-11 | VMUV_WARN_MODE | R/W  | 0h    | VM under voltage warning fault mode<br>0h = Report on nFAULT, latch into status register, pre-driver Hi-Z, auto recovery with slow retry time (in ms)<br>1h = Report on nFAULT, latch into status register, pre-driver Hi-Z, auto recovery with fast retry time (in ms)<br>2h = Report on nFAULT, latch into status register, no action on pre-driver<br>3h = Disabled                                                                                                                                                             |
| 10-9  | OVP_MODE       | R/W  | 0h    | Over voltage protection fault mode<br>0h = Report on nFAULT, latch into status register, pre-driver Hi-Z, auto recovery with slow retry time (in ms)<br>1h = Report on nFAULT, latch into status register, pre-driver Hi-Z, auto recovery with fast retry time (in ms)<br>2h = Reserved<br>3h = Reserved                                                                                                                                                                                                                           |
| 8     | RESERVED       | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 7     | SPIFLT_MODE    | R/W  | 0h    | SPI fault mode<br>0h = Report on nFAULT, latch into status register, no action on pre-driver<br>1h = Disabled                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 6-4   | OCP_MODE       | R/W  | 1h    | Over current protection fault mode<br>0h = Report on nFAULT, Latch into status register, pre-driver Hi-Z, auto recovery with slow retry time (in ms)<br>1h = Report on nFAULT, Latch into status register, pre-driver Hi-Z, auto recovery with fast retry time (in ms)<br>2h = Report on nFAULT, Latch into status register, pre-driver Hi-Z, no auto recovery, wait for CLR_FLT<br>3h = Report on nFAULT, Latch into status register, No action on pre-driver<br>4h = Reserved<br>5h = Reserved<br>6h = Reserved<br>7h = Reserved |
| 3-2   | UVP_MODE       | R/W  | 1h    | Under voltage protection fault mode<br>0h = Report on nFAULT, Latch into status register, pre-driver Hi-Z, auto recovery with slow retry time (in ms)<br>1h = Report on nFAULT, Latch into status register, pre-driver Hi-Z, auto recovery with fast retry time (in ms)<br>2h = Reserved<br>3h = Reserved                                                                                                                                                                                                                          |

**Table 8-17. FLT\_MODE Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                     |
|-----|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1-0 | OTF_MODE | R/W  | 1h    | Over temperature fault mode<br>0h = Report on nFAULT, Latch into status register, pre-driver Hi-Z, auto recover with Slow Retry time (in ms)<br>1h = Report on nFAULT, Latch into status register, pre-driver Hi-Z, auto recover with Fast Retry time (in ms)<br>2h = Reserved<br>3h = Reserved |

### 8.6.8 SYSF\_CTRL Register (Offset = 12h) [Reset = 0553h]

SYSF\_CTRL is shown in [Figure 8-35](#) and described in [Table 8-18](#).

Return to the [Table 8-9](#).

**Figure 8-35. SYSF\_CTRL Register**

|              |          |          |          |          |          |            |          |
|--------------|----------|----------|----------|----------|----------|------------|----------|
| 15           | 14       | 13       | 12       | 11       | 10       | 9          | 8        |
| PARITY       | RESERVED |          |          |          | DNRDY_EN | OTW_FET_EN | RESERVED |
| R/W-0h       | R-0-0h   |          |          |          | R/W-1h   | R/W-0h     | R/W-1h   |
| 7            | 6        | 5        | 4        | 3        | 2        | 1          | 0        |
| VMUV_WARN_EN | RESERVED | RESERVED | RESERVED | RESERVED |          | RESERVED   | RESERVED |
| R/W-0h       | R/W-1h   | R-0-0h   | R/W-1h   | R-0-0h   |          | R/W-1h     | R/W-1h   |

**Table 8-18. SYSF\_CTRL Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                |
|-------|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | PARITY       | R/W  | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                                                                     |
| 14-11 | RESERVED     | R-0  | 0h    | Reserved                                                                                                                                   |
| 10    | DNRDY_EN     | R/W  | 1h    | Device not ready fault enable<br>0h = Device not ready fault is disabled<br>1h = Device not ready fault is enabled                         |
| 9     | OTW_FET_EN   | R/W  | 0h    | FET over temperature warning fault enable<br>0h = FET over temperature warning is disabled<br>1h = FET over temperature warning is enabled |
| 8     | RESERVED     | R/W  | 1h    | Reserved                                                                                                                                   |
| 7     | VMUV_WARN_EN | R/W  | 0h    | VM under voltage warn fault enable<br>0h = VM under voltage warning fault is disabled<br>1h = VM under voltage warning fault is enabled    |
| 6     | RESERVED     | R/W  | 1h    | Reserved                                                                                                                                   |
| 5     | RESERVED     | R-0  | 0h    | Reserved                                                                                                                                   |
| 4     | RESERVED     | R/W  | 1h    | Reserved                                                                                                                                   |
| 3-2   | RESERVED     | R-0  | 0h    | Reserved                                                                                                                                   |
| 1     | RESERVED     | R/W  | 1h    | Reserved                                                                                                                                   |
| 0     | RESERVED     | R/W  | 1h    | Reserved                                                                                                                                   |

### 8.6.9 DRVF\_TCTRL Register (Offset = 13h) [Reset = 0155h]

DRVF\_TCTRL is shown in [Figure 8-36](#) and described in [Table 8-19](#).

Return to the [Table 8-9](#).

**Figure 8-36. DRVF\_TCTRL Register**

|          |          |         |    |            |    |               |   |
|----------|----------|---------|----|------------|----|---------------|---|
| 15       | 14       | 13      | 12 | 11         | 10 | 9             | 8 |
| PARITY   | RESERVED |         |    |            |    | RESERVED      |   |
| R/W-0h   | R-0-0h   |         |    |            |    | R/W-1h        |   |
| 7        | 6        | 5       | 4  | 3          | 2  | 1             | 0 |
| RESERVED |          | OCP_DEG |    | OCP_TBLANK |    | VMUV_WARN_TDG |   |
| R/W-1h   |          | R/W-1h  |    | R/W-1h     |    | R/W-1h        |   |

**Table 8-19. DRVF\_TCTRL Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                          |
|-------|---------------|------|-------|----------------------------------------------------------------------------------------------------------------------|
| 15    | PARITY        | R/W  | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                                               |
| 14-10 | RESERVED      | R-0  | 0h    | Reserved                                                                                                             |
| 9-8   | RESERVED      | R/W  | 1h    | Reserved                                                                                                             |
| 7-6   | RESERVED      | R/W  | 1h    | Reserved                                                                                                             |
| 5-4   | OCP_DEG       | R/W  | 1h    | OCP deglitch time<br>0h = 0.3 $\mu$ s<br>1h = 0.6 $\mu$ s<br>2h = 0.9 $\mu$ s<br>3h = 1.2 $\mu$ s                    |
| 3-2   | OCP_TBLANK    | R/W  | 1h    | OCP blanking time<br>0h = 0.3 $\mu$ s<br>1h = 0.7 $\mu$ s<br>2h = 2 $\mu$ s<br>3h = 1.2 $\mu$ s                      |
| 1-0   | VMUV_WARN_TDG | R/W  | 1h    | VM under voltage warning deglitch time<br>0h = 0.3 $\mu$ s<br>1h = 0.6 $\mu$ s<br>2h = 0.9 $\mu$ s<br>3h = 2 $\mu$ s |

### 8.6.10 FLT\_TCTRL Register (Offset = 16h) [Reset = 0003h]

FLT\_TCTRL is shown in [Figure 8-37](#) and described in [Table 8-20](#).

Return to the [Table 8-9](#).

**Figure 8-37. FLT\_TCTRL Register**

|          |          |    |    |             |    |             |   |
|----------|----------|----|----|-------------|----|-------------|---|
| 15       | 14       | 13 | 12 | 11          | 10 | 9           | 8 |
| PARITY   | RESERVED |    |    |             |    |             |   |
| R/W-0h   | R-0-0h   |    |    |             |    |             |   |
| 7        | 6        | 5  | 4  | 3           | 2  | 1           | 0 |
| RESERVED |          |    |    | SLOW_TRETRY |    | FAST_TRETRY |   |
| R-0-0h   |          |    |    | R/W-0h      |    | R/W-3h      |   |

**Table 8-20. FLT\_TCTRL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                   |
|------|-------------|------|-------|---------------------------------------------------------------------------------------------------------------|
| 15   | PARITY      | R/W  | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                                        |
| 14-4 | RESERVED    | R-0  | 0h    | Reserved                                                                                                      |
| 3-2  | SLOW_TRETRY | R/W  | 0h    | Retry time (typical) for slow recovery from fault condition<br>0h = 0.5s<br>1h = 1s<br>2h = 2s<br>3h = 5s     |
| 1-0  | FAST_TRETRY | R/W  | 3h    | Retry time (typical) for fast recovery from fault condition<br>0h = 0.5ms<br>1h = 1ms<br>2h = 2ms<br>3h = 5ms |

### 8.6.11 FLT\_CLR Register (Offset = 17h) [Reset = 0000h]

FLT\_CLR is shown in [Figure 8-38](#) and described in [Table 8-21](#).

Return to the [Table 8-9](#).

**Figure 8-38. FLT\_CLR Register**

|          |          |    |    |    |    |   |         |
|----------|----------|----|----|----|----|---|---------|
| 15       | 14       | 13 | 12 | 11 | 10 | 9 | 8       |
| RESERVED | RESERVED |    |    |    |    |   |         |
| R/W-0h   | R-0-0h   |    |    |    |    |   |         |
| 7        | 6        | 5  | 4  | 3  | 2  | 1 | 0       |
| RESERVED |          |    |    |    |    |   | FLT_CLR |
| R-0-0h   |          |    |    |    |    |   | W-0h    |

**Table 8-21. FLT\_CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                               |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | RESERVED | R/W  | 0h    | Reserved                                                                                                                                                  |
| 14-1 | RESERVED | R-0  | 0h    | Reserved                                                                                                                                                  |
| 0    | FLT_CLR  | W    | 0h    | Clear latched faults<br>0h = No clear fault command is issued<br>1h = To clear the latched fault bits. This bit automatically resets after being written. |

### 8.6.12 VMUV\_WARN\_THR Register (Offset = 18h) [Reset = 0000h]

VMUV\_WARN\_THR is shown in [Figure 8-39](#) and described in [Table 8-22](#).

Return to the [Table 8-9](#).

**Figure 8-39. VMUV\_WARN\_THR Register**

|               |          |    |    |               |    |   |   |
|---------------|----------|----|----|---------------|----|---|---|
| 15            | 14       | 13 | 12 | 11            | 10 | 9 | 8 |
| PARITY        | RESERVED |    |    |               |    |   |   |
| R/W-0h        | R-0-0h   |    |    |               |    |   |   |
| 7             | 6        | 5  | 4  | 3             | 2  | 1 | 0 |
| VMUV_WARN_RTH |          |    |    | VMUV_WARN_FTH |    |   |   |
| R/W-0h        |          |    |    | R/W-0h        |    |   |   |

**Table 8-22. VMUV\_WARN\_THR Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                     |
|------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | PARITY        | R/W  | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                                                                                                                                                                                                          |
| 14-8 | RESERVED      | R-0  | 0h    | Reserved                                                                                                                                                                                                                                                                        |
| 7-4  | VMUV_WARN_RTH | R/W  | 0h    | VM under voltage warning rising threshold<br>0h = 5.62V<br>1h = 6.25V<br>2h = 6.87V<br>3h = 7.5V<br>4h = 8.12V<br>5h = 8.75V<br>6h = 9.37V<br>7h = 10.00V<br>8h = 10.62V<br>9h = 11.25V<br>Ah = 11.87V<br>Bh = 12.5V<br>Ch = 13.75V<br>Dh = 15.00V<br>Eh = 16.25V<br>Fh = 17.5V |
| 3-0  | VMUV_WARN_FTH | R/W  | 0h    | VM under voltage warning falling threshold<br>0h = 5.4V<br>1h = 6.0V<br>2h = 6.6V<br>3h = 7.2V<br>4h = 7.8V<br>5h = 8.4V<br>6h = 9.0V<br>7h = 9.6V<br>8h = 10.2V<br>9h = 10.8V<br>Ah = 11.4V<br>Bh = 12.0V<br>Ch = 13.2V<br>Dh = 14.4V<br>Eh = 15.6V<br>Fh = 16.8V              |

### 8.6.13 PWM\_CTRL Register (Offset = 20h) [Reset = 0000h]

PWM\_CTRL is shown in [Figure 8-40](#) and described in [Table 8-23](#).

Return to the [Table 8-9](#).

**Figure 8-40. PWM\_CTRL Register**

|          |          |    |    |    |         |          |   |
|----------|----------|----|----|----|---------|----------|---|
| 15       | 14       | 13 | 12 | 11 | 10      | 9        | 8 |
| PARITY   | RESERVED |    |    |    |         |          |   |
| R/W-0h   | R-0-0h   |    |    |    |         |          |   |
| 7        | 6        | 5  | 4  | 3  | 2       | 1        | 0 |
| RESERVED |          |    |    |    | SSC_DIS | PWM_MODE |   |
| R-0-0h   |          |    |    |    | R/W-0h  | R/W-0h   |   |

**Table 8-23. PWM\_CTRL Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                      |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------|
| 15   | PARITY   | R/W  | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                           |
| 14-3 | RESERVED | R-0  | 0h    | Reserved                                                                                         |
| 2    | SSC_DIS  | R/W  | 0h    | Disable SSC on oscillator<br>0h = SSC enabled<br>1h = SSC disabled                               |
| 1-0  | PWM_MODE | R/W  | 0h    | PWM mode selection<br>0h = 6x mode<br>1h = 6x direct mode<br>2h = 3x mode<br>3h = 3x direct mode |

### 8.6.14 DRV\_CTRL Register (Offset = 22h) [Reset = 0003h]

DRV\_CTRL is shown in [Figure 8-41](#) and described in [Table 8-24](#).

Return to the [Table 8-9](#).

**Figure 8-41. DRV\_CTRL Register**

|           |          |    |    |            |    |           |   |
|-----------|----------|----|----|------------|----|-----------|---|
| 15        | 14       | 13 | 12 | 11         | 10 | 9         | 8 |
| PARITY    | RESERVED |    |    | DLY_TARGET |    |           |   |
| R/W-0h    | R-0-0h   |    |    | R/W-0h     |    |           |   |
| 7         | 6        | 5  | 4  | 3          | 2  | 1         | 0 |
| DLYCMP_EN | RESERVED |    |    |            |    | SLEW_RATE |   |
| R/W-0h    | R-0-0h   |    |    |            |    | R/W-3h    |   |

**Table 8-24. DRV\_CTRL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                              |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | PARITY     | R/W  | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                                                                   |
| 14-12 | RESERVED   | R-0  | 0h    | Reserved                                                                                                                                 |
| 11-8  | DLY_TARGET | R/W  | 0h    | Delay Target : DLY_TARGET * 0.2μs                                                                                                        |
| 7     | DLYCMP_EN  | R/W  | 0h    | Driver Delay Compensation enable<br>0h = Delay compensation disabled<br>1h = Delay compensation enabled                                  |
| 6-2   | RESERVED   | R-0  | 0h    | Reserved                                                                                                                                 |
| 1-0   | SLEW_RATE  | R/W  | 3h    | Slew rate settings<br>0h = Slew rate is 25 V/μs<br>1h = Slew rate is 50 V/μs<br>2h = Slew rate is 125 V/μs<br>3h = Slew rate is 200 V/μs |

### 8.6.15 CSA\_CTRL Register (Offset = 23h) [Reset = 0008h]

CSA\_CTRL is shown in [Figure 8-42](#) and described in [Table 8-25](#).

Return to the [Table 8-9](#).

**Figure 8-42. CSA\_CTRL Register**

|          |          |    |    |        |          |          |   |
|----------|----------|----|----|--------|----------|----------|---|
| 15       | 14       | 13 | 12 | 11     | 10       | 9        | 8 |
| PARITY   | RESERVED |    |    |        |          |          |   |
| R/W-0h   | R-0-0h   |    |    |        |          |          |   |
| 7        | 6        | 5  | 4  | 3      | 2        | 1        | 0 |
| RESERVED |          |    |    | CSA_EN | RESERVED | CSA_GAIN |   |
| R-0-0h   |          |    |    | R/W-1h | R-0-0h   | R/W-0h   |   |

**Table 8-25. CSA\_CTRL Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                    |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 15   | PARITY   | R/W  | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                                                                         |
| 14-4 | RESERVED | R-0  | 0h    | Reserved                                                                                                                       |
| 3    | CSA_EN   | R/W  | 1h    | Enable CSA<br>0h = CSA is disabled<br>1h = CSA is enabled                                                                      |
| 2    | RESERVED | R-0  | 0h    | Reserved                                                                                                                       |
| 1-0  | CSA_GAIN | R/W  | 0h    | CSA Gain settings<br>0h = CSA gain is 0.25 V/A<br>1h = CSA gain is 0.5 V/A<br>2h = CSA gain is 1 V/A<br>3h = CSA gain is 2 V/A |

### 8.6.16 SYS\_CTRL Register (Offset = 3Fh) [Reset = 5008h]

SYS\_CTRL is shown in [Figure 8-43](#) and described in [Table 8-26](#).

Return to the [Table 8-9](#).

**Figure 8-43. SYS\_CTRL Register**

|          |           |          |    |          |          |          |          |
|----------|-----------|----------|----|----------|----------|----------|----------|
| 15       | 14        | 13       | 12 | 11       | 10       | 9        | 8        |
| PARITY   | WRITE_KEY |          |    | RESERVED |          | RESERVED | RESERVED |
| R/W-0h   | W-5h      |          |    | R-0-0h   |          | R/W-0h   | R/W-0h   |
| 7        | 6         | 5        | 4  | 3        | 2        | 1        | 0        |
| REG_LOCK | SPI_PEN   | RESERVED |    | RESERVED | RESERVED |          |          |
| R/W-0h   | R/W-0h    | R/W-0h   |    | R/W-1h   | R/W-0h   |          |          |

**Table 8-26. SYS\_CTRL Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                           |
|-------|-----------|------|-------|-----------------------------------------------------------------------|
| 15    | PARITY    | R/W  | 0h    | Parity Bit if SPI_PEN is set to '1' otherwise reserved                |
| 14-12 | WRITE_KEY | W    | 5h    | 0x5 : Write Key specific to this register.                            |
| 11-10 | RESERVED  | R-0  | 0h    | Reserved                                                              |
| 9     | RESERVED  | R/W  | 0h    | Reserved                                                              |
| 8     | RESERVED  | R/W  | 0h    | Reserved                                                              |
| 7     | REG_LOCK  | R/W  | 0h    | Register Lock Bit<br>0h = Registers Unlocked<br>1h = Registers Locked |
| 6     | SPI_PEN   | R/W  | 0h    | Parity Enable for SPI<br>0h = Parity Disabled<br>1h = Parity Enabled  |
| 5-4   | RESERVED  | R/W  | 0h    | Reserved                                                              |
| 3     | RESERVED  | R/W  | 1h    | Reserved                                                              |
| 2-0   | RESERVED  | R/W  | 0h    | Reserved                                                              |

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The DRV8317 can be used to drive brushless-DC motors. The following design procedure can be used to configure the DRV8317.

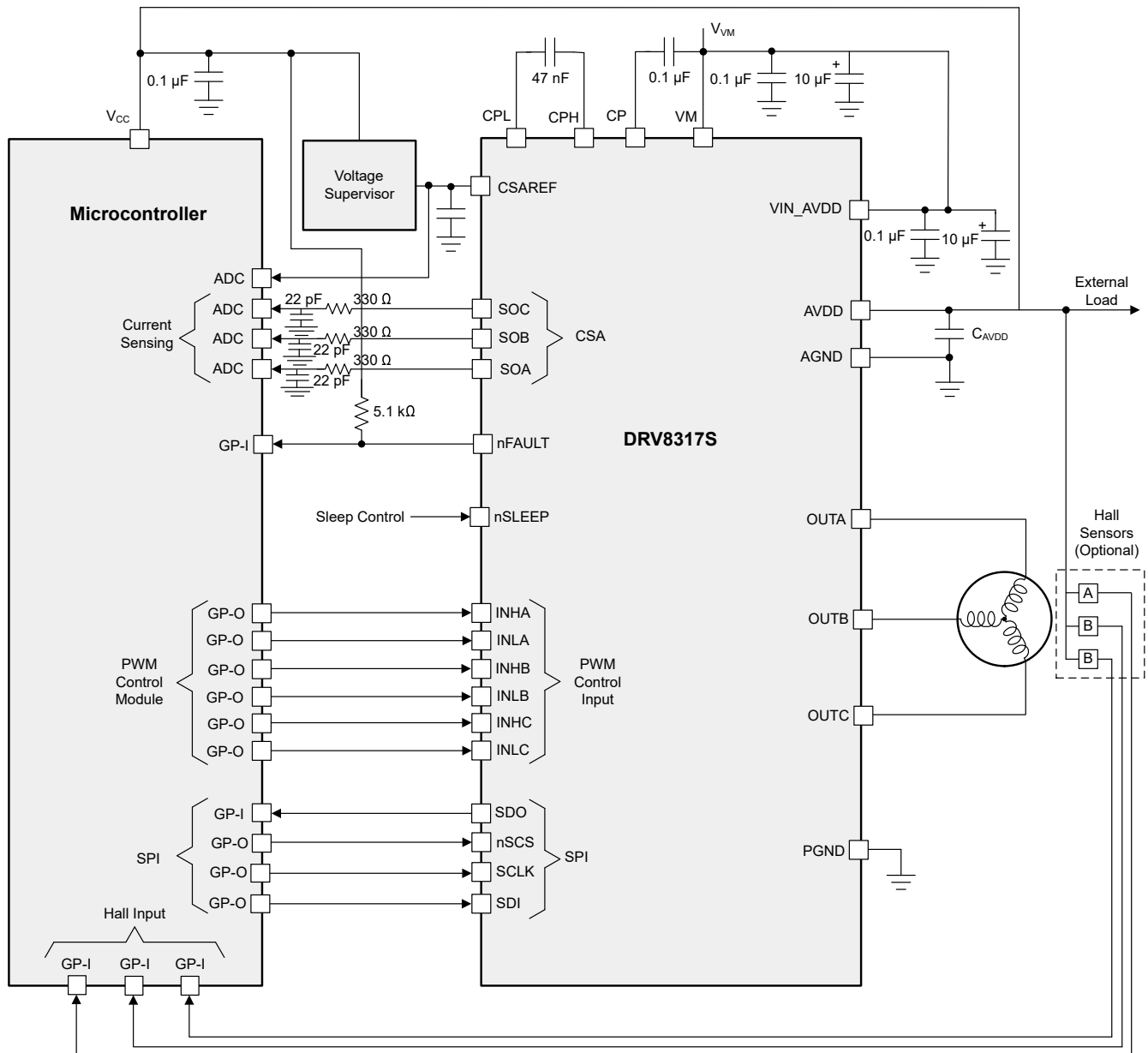


**Figure 9-1. Application Schematics (DRV8317S)**

## 9.2 Typical Applications

### 9.2.1 Three-Phase Brushless-DC Motor Control

In this application, the DRV8317 is used to drive a brushless-DC motor using PWMs from an external microcontroller.

#### 9.2.1.1 Detailed Design Procedure

Table 9-1 lists the example input parameters for the system design.

**Table 9-1. Design Parameters**

| DESIGN PARAMETERS          | REFERENCE       | EXAMPLE VALUE  |
|----------------------------|-----------------|----------------|
| Supply voltage             | $V_{VM}$        | 12 V           |
| Motor RMS current          | $I_{RMS}$       | 2 A            |
| Motor peak current         | $I_{PEAK}$      | 3 A            |
| PWM Frequency              | $f_{PWM}$       | 50 kHz         |
| Slew Rate Setting          | SR              | 200 V/ $\mu$ s |
| VIN_AVDD supply voltage    | $V_{VIN\_AVDD}$ | 12 V           |
| CSA reference voltage      | $V_{CSA\_REF}$  | 3.0 V          |
| System ambient temperature | $T_A$           | -20°C to +50°C |

##### 9.2.1.1.1 Motor Voltage

Brushless-DC motors are typically rated for a certain voltage (for example, 5V or 12V). The DRV8317 allows for a range of possible operating voltages from 4.5-V to 20-V.

##### 9.2.1.2 Driver Propagation Delay and Dead Time

The propagation delay is defined as the time taken for changing input logic edges INHx and INLx (whichever changes first, if MCU dead time is added) to change the half-bridge output voltage (OUTx). Driver propagation delay ( $t_{PD}$ ) and dead time ( $t_{dead}$ ) are specified with a typical and maximum value, but not with a minimum value. This is because the propagation delay can be smaller than typical depending on the direction of current at the OUTx pin during synchronous switching. Driver propagation delay and dead time can be more than typical values due to slower internal turn-on of the high-side or low-side internal MOSFETs to avoid parasitic dV/dt coupling.

For more information and examples of how propagation delay and dead time differs for input PWM and output configurations, refer to [Delay and Dead Time in Integrated MOSFET Drivers](#).

The dead time from the external microcontroller's (MCU) PWM inputs (INHx, INLx) can be used as an extra precaution in addition to the DRV8317 internal shoot-through (cross conduction) protection. If the MCU dead time is less than the DRV8317 driver dead time, actual output (OUTx voltage) dead time will be decided by the DRV8317 dead time ( $t_{DEAD}$ ). If the MCU dead time is larger than the driver dead time, actual output (OUTx voltage) dead time will be decided by the MCU dead time.

A summary of the DRV8317 delay times with respect to synchronous inputs INHx and INLx, OUTx current direction, and MCU dead time are listed in Table 9-2.

**Table 9-2. Summary of Delay Times in DRV8317 Depending on Logic Inputs and Output Current Direction**

| OUTx Current Direction | INHx    | INLx    | Propagation Delay ( $t_{PD}$ ) | Dead Time ( $t_{DEAD}$ )       | Inserted MCU Dead Time ( $t_{DEAD(MCU)}$ )      |                                    |
|------------------------|---------|---------|--------------------------------|--------------------------------|-------------------------------------------------|------------------------------------|
|                        |         |         |                                |                                | $t_{DEAD(MCU)} \leq t_{DEAD}$                   | $t_{DEAD(MCU)} > t_{DEAD}$         |
| Out of OUTx            | Rising  | Falling | $\leq t_{PD} \text{ (max)}$    | $\leq t_{DEAD} \text{ (max)}$  | Output dead time $\leq t_{DEAD} \text{ (max)}$  | Output dead time = $t_{DEAD(MCU)}$ |
|                        | Falling | Rising  | $\leq t_{PD} \text{ (typ.)}$   | $\leq t_{DEAD} \text{ (typ.)}$ | Output dead time $\leq t_{DEAD} \text{ (typ.)}$ | Output dead time < $t_{DEAD(MCU)}$ |

**Table 9-2. Summary of Delay Times in DRV8317 Depending on Logic Inputs and Output Current Direction (continued)**

| OUTx Current Direction | INHx    | INLx    | Propagation Delay (t <sub>PD</sub> ) | Dead Time (t <sub>DEAD</sub> ) | Inserted MCU Dead Time (t <sub>DEAD(MCU)</sub> ) |                                            |
|------------------------|---------|---------|--------------------------------------|--------------------------------|--------------------------------------------------|--------------------------------------------|
|                        |         |         |                                      |                                | t <sub>DEAD(MCU)</sub> ≤ t <sub>DEAD</sub>       | t <sub>DEAD(MCU)</sub> > t <sub>DEAD</sub> |
| Into OUTx              | Rising  | Falling | ≤ t <sub>PD</sub> (typ.)             | ≤ t <sub>DEAD</sub> (typ.)     | Output dead time ≤ t <sub>DEAD</sub> (typ.)      | Output dead time < t <sub>DEAD(MCU)</sub>  |
|                        | Falling | Rising  | ≤ t <sub>PD</sub> (max)              | ≤ t <sub>DEAD</sub> (max)      | Output dead time ≤ t <sub>DEAD</sub> (max)       | Output dead time = t <sub>DEAD(MCU)</sub>  |

### 9.2.1.3 Delay Compensation

Differences in delays of dead time and propagation delay can cause mismatch in the output timings of PWMs, which can lead to duty cycle distortion. In order to accommodate differences in propagation delay between the conditions mentioned in [Table 9-2](#), DRV8317 integrates a delay compensation feature.

Delay compensation is used to match delay times for currents going into and out of phase (OUTx) by adding a variable delay time (t<sub>var</sub>) to match a preset target delay time equal to the propagation delay plus driver dead time (t<sub>PD</sub> + t<sub>DRV\_DEAD</sub>). This (t<sub>var</sub>) setting is automatically configured by the DRV8317 when the DLYCMP\_EN bit is set to 1b.

### 9.2.1.4 Current Sensing and Output Filtering

The SOx pins are typically sampled by an analog-to-digital converter in the MCU to calculate the phase current. Phase current information is used for closed-loop control such as Field-Oriented Control (FOC).

An example calculation for phase current is shown in [Equation 3](#).

$$SOx = V_{REF}/2 + G_{CSA} * I_{OUTx} \quad (3)$$

For example, in a system with VREF = 3-V, CSA gain = 0.5 V/A, and a SOx voltage of 1.2-V, phase current (I<sub>OUTx</sub>) = -0.6A.

Sometimes high frequency noise can appear at the SOx signals based on voltage ripple at VREF, added inductance at the SOx traces, or routing of SOx traces near high frequency components. It is recommended to add a low-pass RC filter close to the MCU with cut-off frequency at least 10 times the PWM switching frequency for trapezoidal commutation and 100 times the PWM switching frequency for sinusoidal commutation to filter high frequency noise. A recommended RC filter is 330-ohms, 22-pF to add minimal parallel capacitance to the ADC and current mirroring circuitry without increasing the settling time of the CSA output.

The cutoff frequency for the low-pass RC filter is in [Equation 4](#).

$$f_c = \frac{1}{2\pi RC} \quad (4)$$

### 9.2.1.5 Application Curves



**Figure 9-2. Device Power up with VM (VM, nFAULT, nSLEEP, AVDD)**



**Figure 9-3. Device Power up with nSLEEP (VM, nFAULT, nSLEEP, AVDD)**

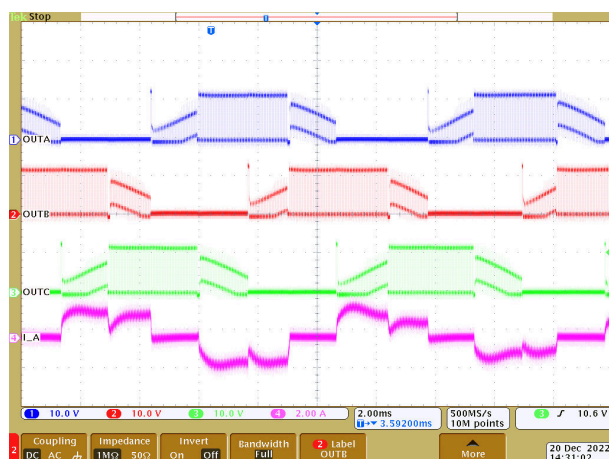


**Figure 9-4. Driver PWM Operation (OUTA, OUTB, OUTC, I\_A)**

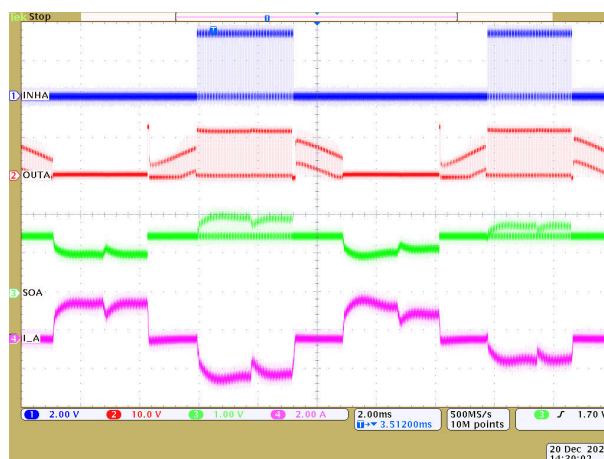


**Figure 9-5. Driver PWM Operation with Current Sense Feedback (INHA, OUTA, SOA, I\_A)**

### 9.3 Alternate Applications

The DRV8317 can be used to drive brushed-DC motors and solenoid loads. The following design procedure can be used to configure the DRV8317.

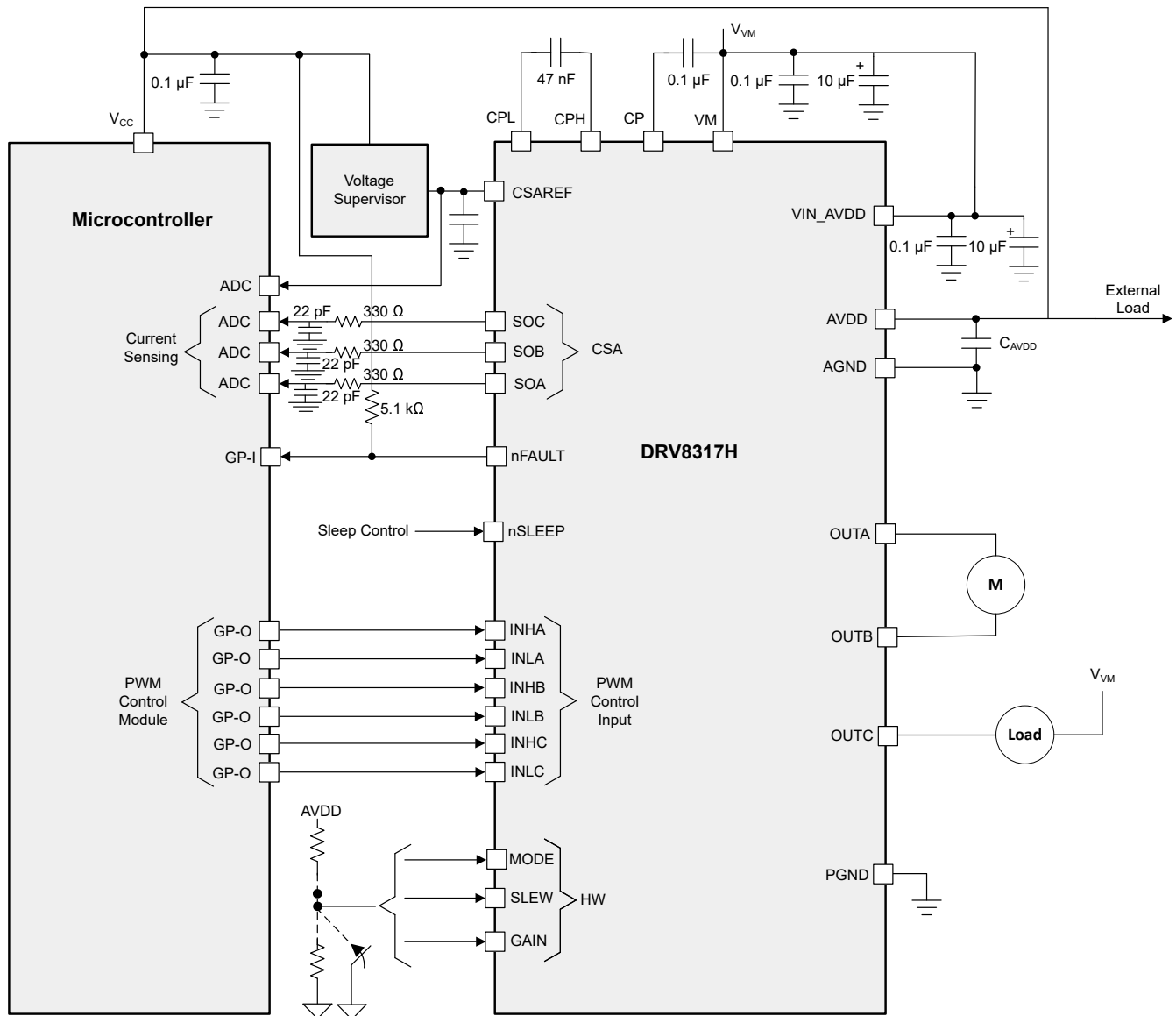


**Figure 9-6. Application Schematics (DRV8317H) - Brushed-DC and Solenoid Load Drive Block Diagram**

6x PWM mode or 3x PWM mode can be used to drive brushed-DC and/or solenoid loads depending on the application. A Brushed-DC motor can be connected to two OUTx phases to create an integrated full H-bridge configuration to drive the motor in both direction.

Solenoid loads can be connected from OUTx to VM or GND to use the DRV8317 as a push-pull driver in 6x PWM or 3x PWM mode. When the load is connected from OUTx to GND, the HS MOSFET sources current into the solenoid, and the LS MOSFET acts as a recirculation diode to recirculate current from the solenoid. When the load is connected from OUTx to VM, the LS MOSFET sink current from the solenoid to GND, and the HS MOSFET acts as a recirculation diode to recirculate current from the solenoid.

## 10 Power Supply Recommendations

### 10.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

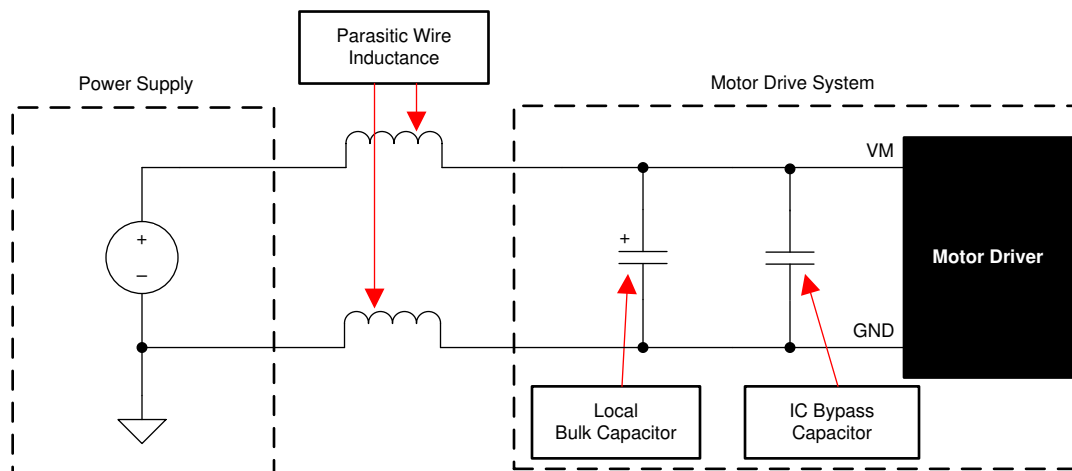


**Figure 10-1. Example Setup of Motor Drive System With External Power Supply**

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

## 11 Layout

### 11.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins including, AVDD, charge pump, CSAREF, VINAVDD and VM.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Ensure grounds are connected through net-ties to reduce voltage offsets and maintain gate driver performance. A common ground plane can also be used for PGND and AGND to minimize inductance in the grounding, but it is recommended to place motor switching outputs as far away from analog and digital signals so motor noise does not couple into the analog and digital circuits.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

[Figure 11-1](#) shows a recommended layout example.

## 11.2 Layout Example

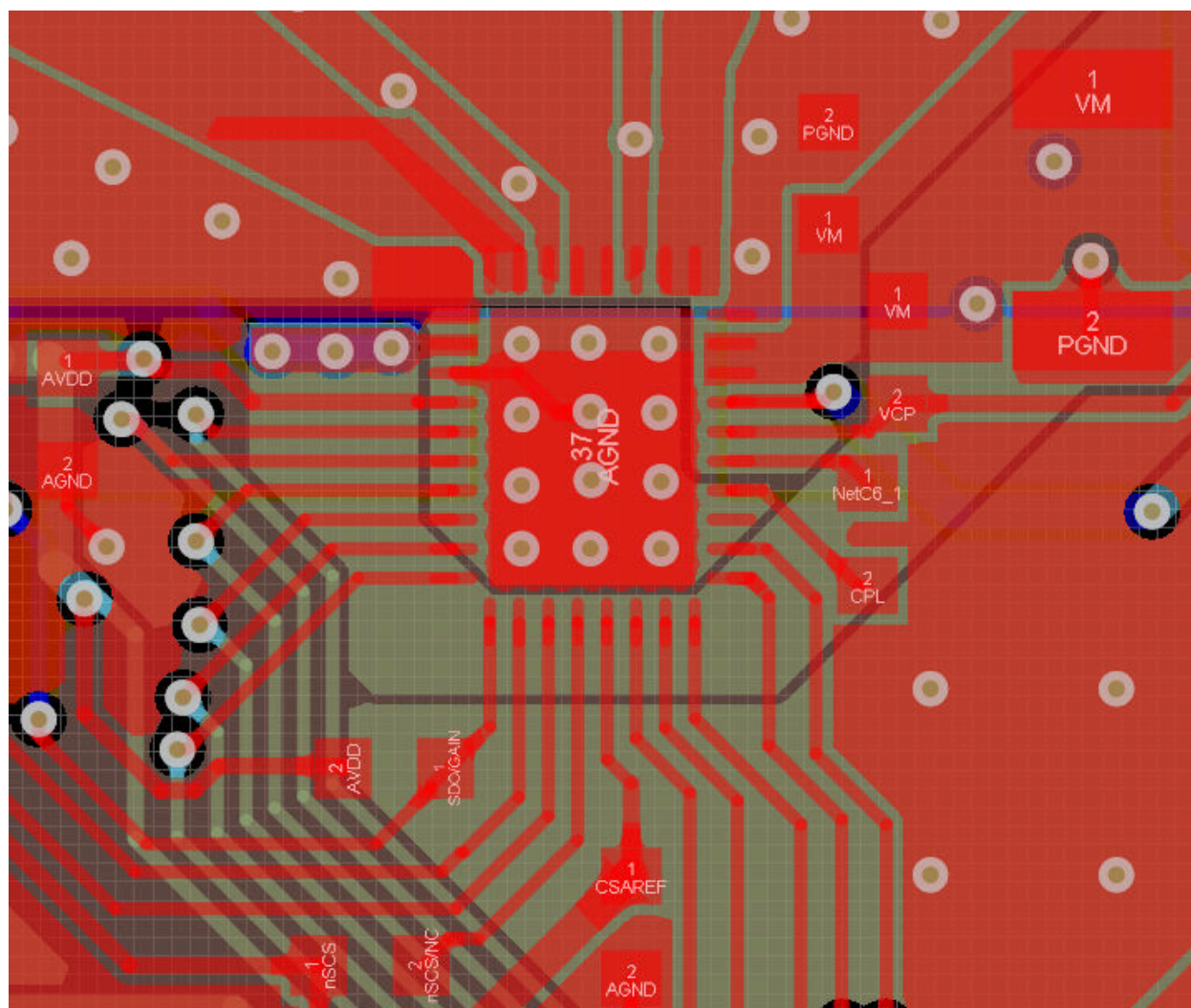


Figure 11-1. Recommended Layout Example

## 11.3 Thermal Considerations

The DRV8317 has thermal shutdown (OTS) as previously described. A die temperature in excess of 145°C (min.) can disable the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

### 11.3.1 Power Dissipation and Junction Temperature Estimation

#### Power Dissipation

The power loss in DRV8317 include standby losses, LDO losses, FET conduction and switching losses, and diode losses. The FET conduction loss dominates the total power dissipation in DRV8317. At start-up and fault conditions, the output current is much higher than normal current; remember to take these peak currents and their duration into consideration. The total device dissipation is the power dissipated in each of the three half bridges added together. The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking. Note that  $R_{DS,ON}$  increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when designing the PCB and heatsinking.

A summary of equations for calculating each loss is listed in [Table 11-1](#) for trapezoidal control and field-oriented control.

**Table 11-1. DRV8317 Power Losses for Trapezoidal and Field-oriented Control**

| Loss type         | Trapezoidal control                                                                    | Field-oriented control                                                                  |
|-------------------|----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| Standby power     | $P_{standby} = V_{VM} \times I_{VMS}$                                                  |                                                                                         |
| AVDD LDO          | $P_{LDO} = (V_{VIN\_AVDD} - V_{AVDD}) \times I_{AVDD}$                                 |                                                                                         |
| FET conduction    | $P_{CON} = 2 \times (I_{PK(trap)})^2 \times R_{DS,ON(TJ)}$                             | $P_{CON} = 3 \times (I_{RMS(FOC)})^2 \times R_{DS,ON(TJ)}$                              |
| FET switching     | $P_{SW} = I_{PK(trap)} \times V_{PK(trap)} \times t_{rise/fall} \times f_{PWM}$        | $P_{SW} = 3 \times I_{RMS(FOC)} \times V_{PK(FOC)} \times t_{rise/fall} \times f_{PWM}$ |
| Diode (dead time) | $P_{diode} = 2 \times I_{PK(trap)} \times V_{F(diode)} \times t_{DEAD} \times f_{PWM}$ | $P_{diode} = 6 \times I_{RMS(FOC)} \times V_{F(diode)} \times t_{DEAD} \times f_{PWM}$  |

#### Note

$R_{DS,ON(TJ)}$  is the on-state resistance of a single FET at operating junction temperature.

#### Junction Temperature Estimation

To calculate the junction temperature of the die from power losses, use [Equation 5](#). Note that the thermal resistance  $R_{\theta JA}$  depends on PCB configuration such as the numbers of PCB layers, copper thickness, ground plane area and the PCB size.

$$T_J(^{\circ}C) = P_{LOSS}(W) \times R_{\theta JA}(^{\circ}C/W) + T_A(^{\circ}C) \quad (5)$$

Refer to [BLDC integrated MOSFET thermal calculator](#) for estimating the approximate device power dissipation and junction temperature at different use cases.

## 12 Device and Documentation Support

### 12.1 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.2 Trademarks

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### 12.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

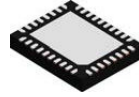
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

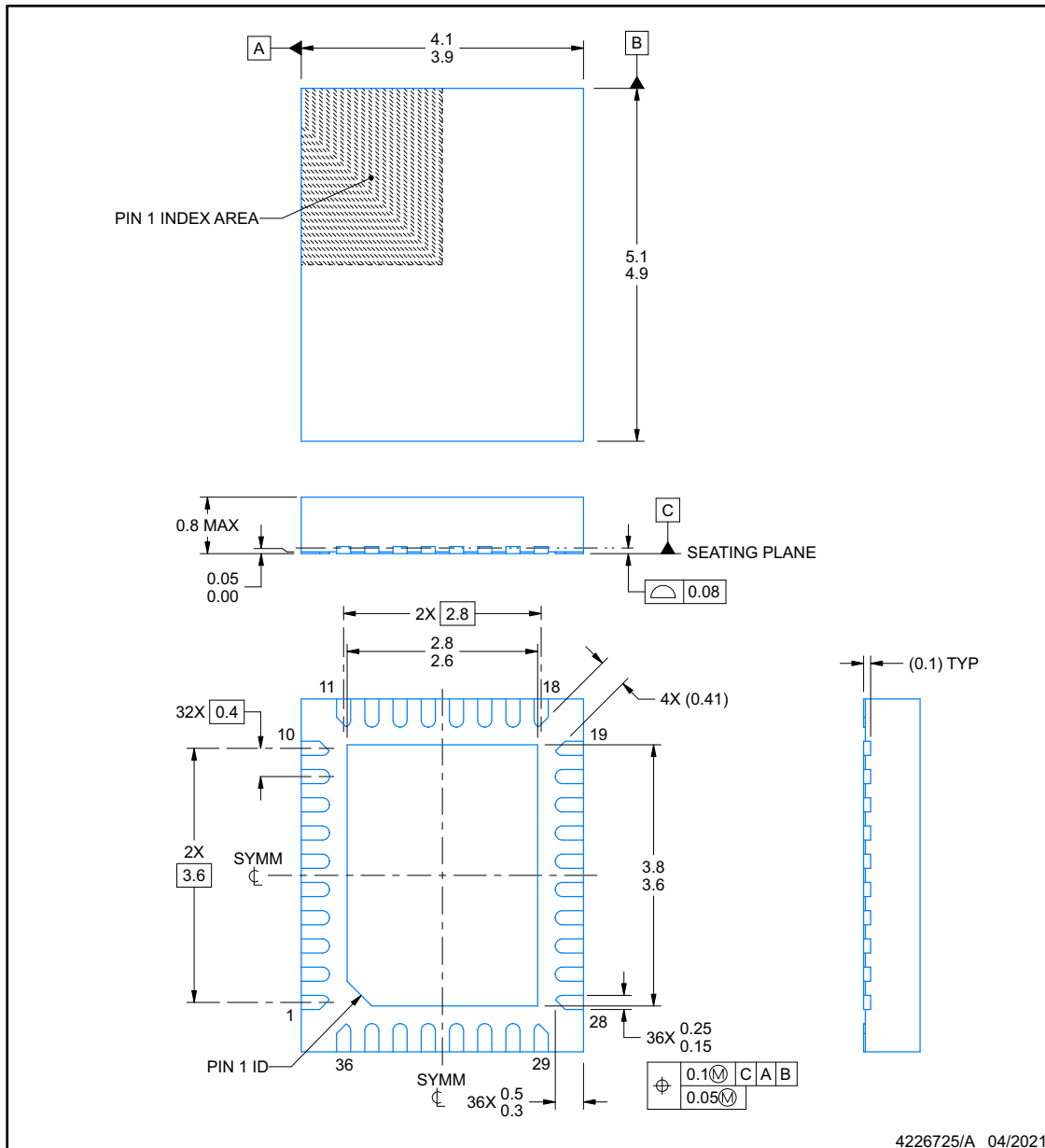
The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.



**REE0036A**

**PACKAGE OUTLINE**  
**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

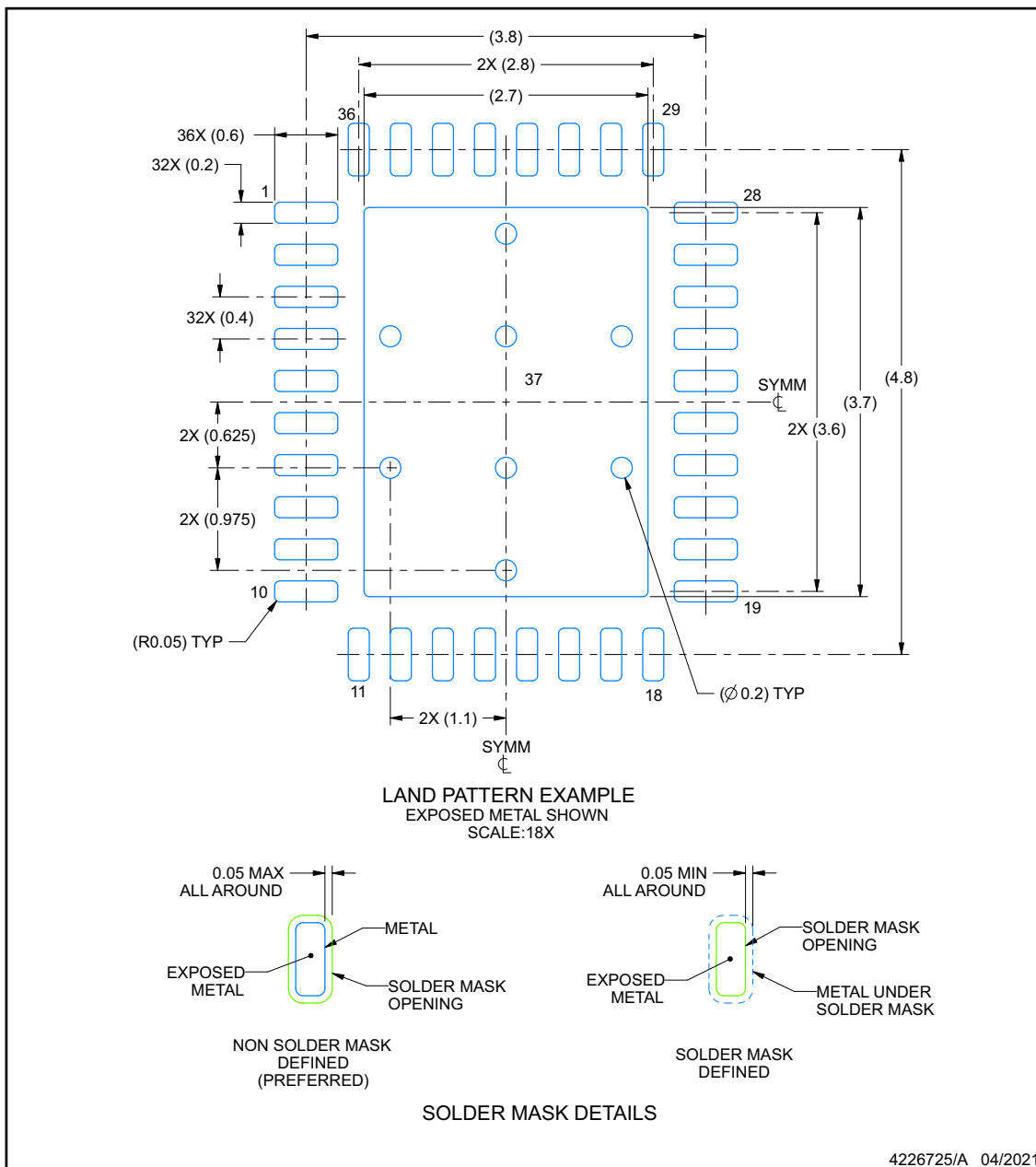
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

**REE0036A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

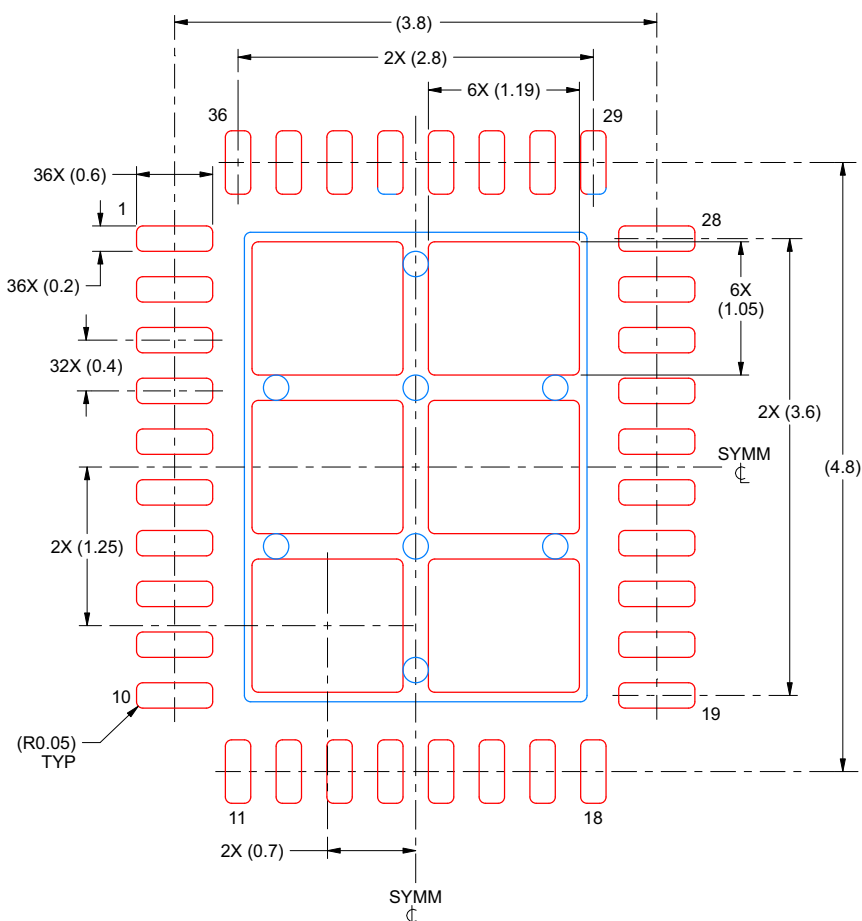
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

## EXAMPLE STENCIL DESIGN

**REE0036A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
**BASED ON 0.125 mm THICK STENCIL**

**EXPOSED PAD**  
**75% PRINTED SOLDER COVERAGE BY AREA**  
**SCALE:20X**

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">DRV8317HREER</a> | Active        | Production           | WQFN (REE)   36 | 5000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | DRV<br>8317H        |
| DRV8317HREER.A               | Active        | Production           | WQFN (REE)   36 | 5000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | DRV<br>8317H        |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

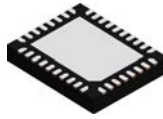
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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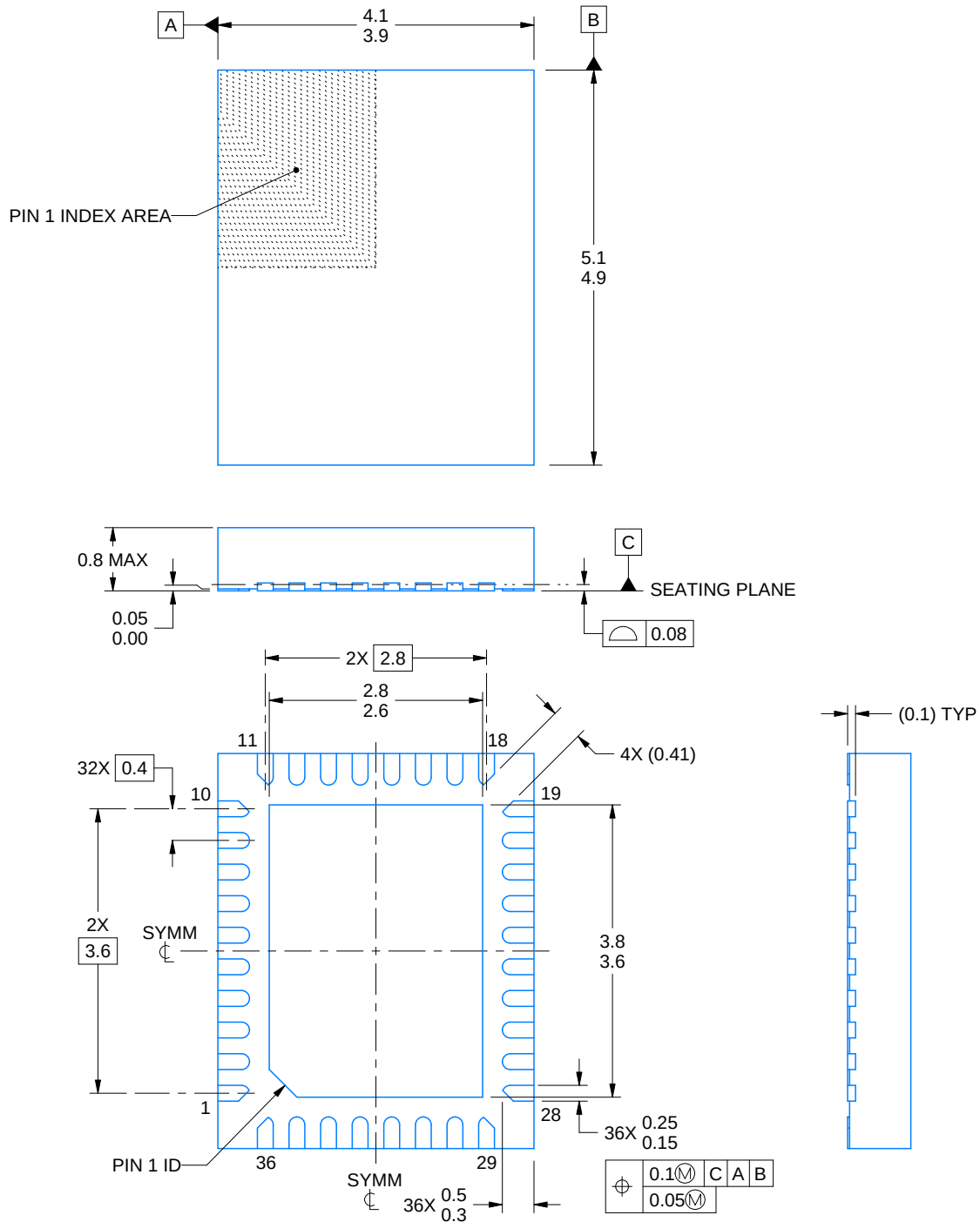
REE0036A



# PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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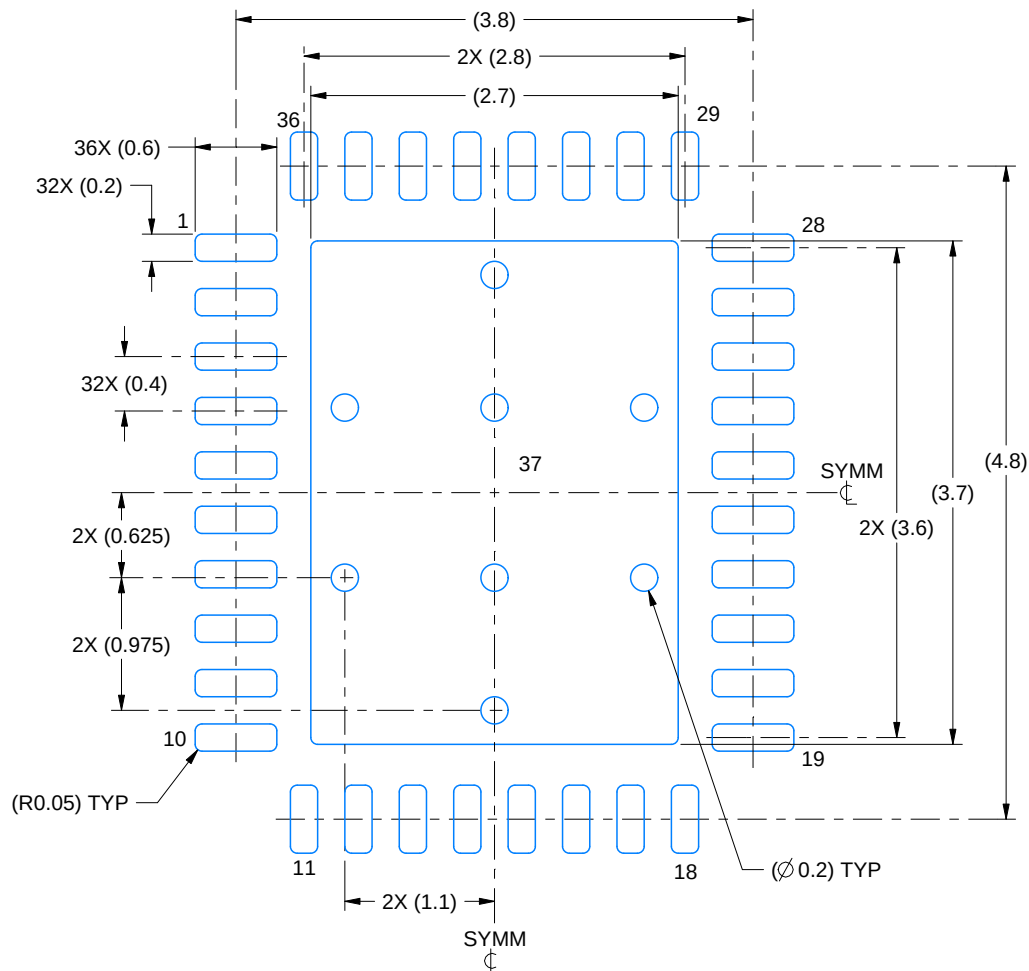
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

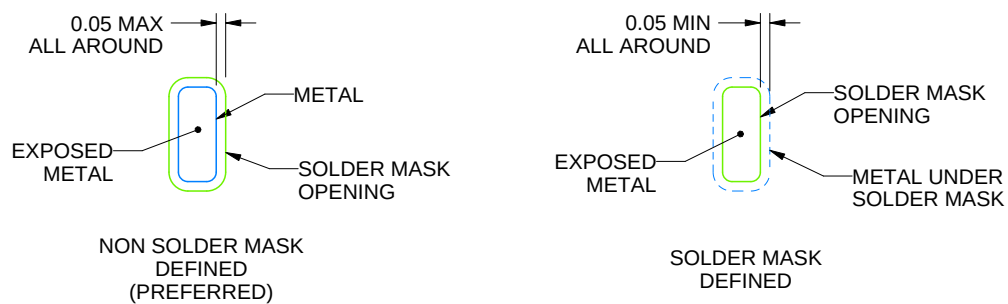
**REE0036A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



## SOLDER MASK DETAILS

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NOTES: (continued)

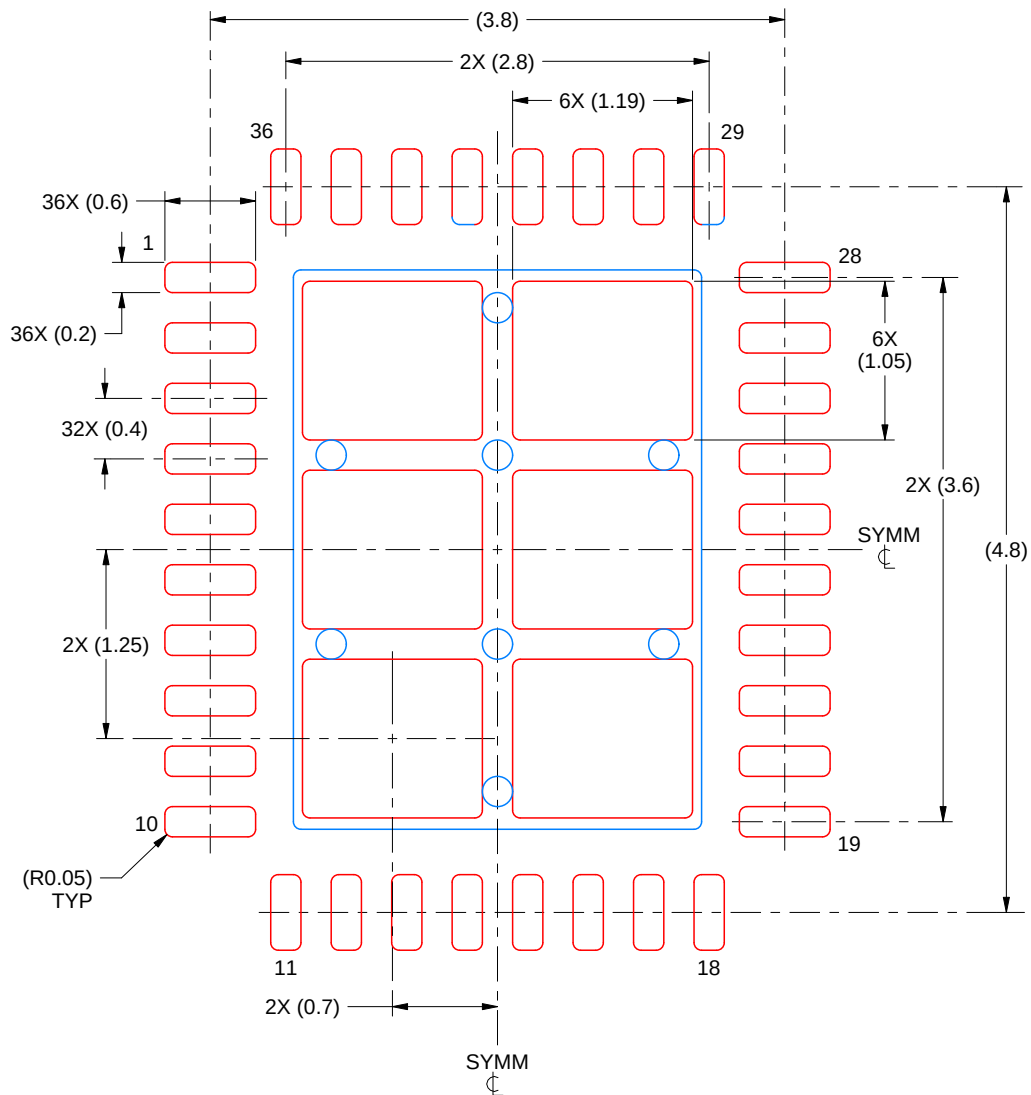
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

REE0036A

WQFN - 0.8 mm max height

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4226725/A 04/2021

NOTES: (continued)

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