DRV8818 Stepper Motor Controller IC

1 Features

- Pulse Width Modulation (PWM) Microstepping Motor Driver
  - Built-In Microstepping Indexer
  - Up to 8 Microsteps/Step
  - Step and Direction Control
  - Programmable Mixed Decay, Blanking, and Off Time
- Up to 2.5A Current Per Winding
- Low 0.37Ω (HS + LS) MOSFET $R_{DS(ON)}$ (25°C)
- 8V to 35V Operating Supply Voltage Range
- Pin to Pin Upgrade for DRV8811 With Lower $R_{DS(ON)}$
- Thermally-Enhanced Surface Mount Package
- Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)

2 Applications

- Printers
- Textile Machinery
- Positioning/Tracking
- Factory Automation
- Robotics

3 Description

The DRV8818 provides an integrated stepper motor driver for printers, scanners, and other automated equipment applications. The device has two H-bridge drivers, as well as microstepping indexer logic to control a stepper motor.

The output driver block for each consists of N-channel power MOSFETs configured as full H-bridges to drive the motor windings.

A simple STEP/DIRECTION interface allows easy interfacing to controller circuits. The mode pins allow for configuration of the motor in full-step, half-step, quarter-step, or eighth-step modes. Decay mode and PWM off time are programmable.

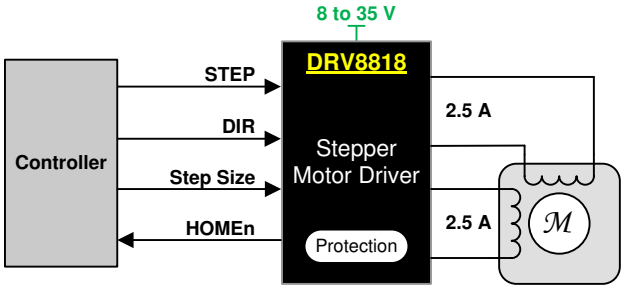
Internal shutdown functions are provided for over current protection, short circuit protection, under-voltage lockout and overtemperature.

The DRV8818 is packaged in a 28-pin HTSSOP package with PowerPAD™.

Device Information (1)

PART NUMBER	PACKAGE	PACKAGE SIZE (2)
DRV8818	HTSSOP (28)	9.70mm x 6.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

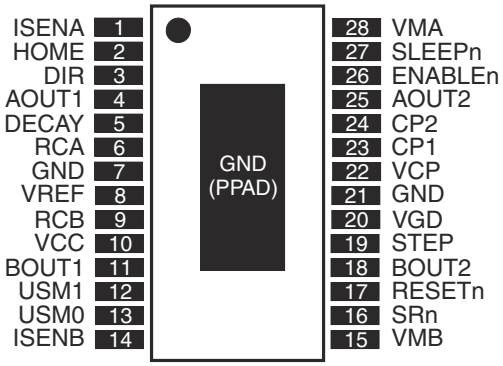

Figure 4-1. PWP Package 28-Pin HTSSOP Top View

Pin Functions

PIN		TYPE[1]	DESCRIPTION	
NAME	NO.			
POWER AND GROUND				
CP1	23	IO	Charge pump flying capacitor	Connect a 0.22µF capacitor between CP1 and CP2.
CP2	24	IO	Charge pump flying capacitor	Connect a 0.22µF capacitor between CP1 and CP2.
GND	7, 21	—	Device ground	
VCC	10	—	Logic supply voltage	Connect to 3V to 5V logic supply. Bypass to GND with a 0.1µF ceramic capacitor.
VCP	22	IO	High-side gate drive voltage	Connect a 0.22µF ceramic capacitor to V_M.
VGD	20	IO	Low-side gate drive voltage	Bypass to GND with a 0.22µF ceramic capacitor.
VMA	28	—	Bridge A power supply	Connect to motor supply (8V to 35V). Both VMA and VMB must be connected to same supply.
VMB	15	—	Bridge B power supply	
CONTROL				
DECAY	5	I	Decay mode select	Voltage applied sets decay mode - see motor driver description for details. Bypass to GND with a 0.1µF ceramic capacitor. Weak internal pulldown.
DIR	3	I	Direction input	Level sets the direction of stepping. Weak internal pulldown.
ENABLEn	26	I	Enable input	Logic high to disable device outputs, logic low to enable outputs. Weak internal pullup to VCC.
ISENA	1	—	Bridge A ground / Isense	Connect to current sense resistor for bridge A
ISENB	14	—	Bridge B ground / Isense	Connect to current sense resistor for bridge B
RCA	6	I	Bridge A blanking and off time adjust	Connect a parallel resistor and capacitor to GND - see motor driver description for details.
RCB	9	I	Bridge B blanking and off time adjust	Connect a parallel resistor and capacitor to GND - see motor driver description for details.
RESETn	17	I	Reset input	Active-low reset input initializes the indexer logic and disables the H-bridge outputs. Weak internal pullup to VCC.
SLEEPn	27	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Weak internal pulldown.
SRn	16	I	Sync. Rect. enable input	Active-low. When low, synchronous rectification is enabled. Weak internal pulldown.
STEP	19	I	Step input	Rising edge causes the indexer to move one step. Weak internal pulldown.
USM0	13	I	Microstep mode 0	USM0 and USM1 set the step mode - full step, half step, quarter step, or eight microsteps/step. Weak internal pulldown.
USM1	12	I	Microstep mode 1	USM0 and USM1 set the step mode - full step, half step, quarter step, or eight microsteps/step. Weak internal pulldown.
VREF	8	I	Current set reference input	Reference voltage for winding current set

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PIN		TYPE[1]	DESCRIPTION	
NAME	NO.			
OUTPUTS				
AOUT1	4	O	Bridge A output 1	Connect to bipolar stepper motor winding
AOUT2	25	O	Bridge A output 2	Positive current is AOUT1 → AOUT2
BOUT1	11	O	Bridge B output 1	Connect to bipolar stepper motor winding
BOUT2	18	O	Bridge B output 2	Positive current is BOUT1 → BOUT2
HOMEn	2	O	Home position	Logic low when at home state of step table, logic high at other states

(1) Directions: I = input, O = output, OZ = 3-state output, OD = open-drain output, IO = input/output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
V_{MX}	Power supply voltage	–0.3	35	V
V_{CC}	Power supply voltage	–0.3	7	V
	Digital pin voltage	–0.5	7	V
V_{REF}	Input voltage	0	V_{CC}	V
ISENSEx(4)	Pin voltage	–0.875	0.875	V
$I_{O(peak)}$	Peak motor drive output current	Internally limited		
P_D	Continuous total power dissipation	See *Section 5.4*		
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.
(4) Transients of ±1V for less than 25ns are acceptable.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage(1)	8		35	V
V_{CC}	Logic power supply voltage	3		5.5	V
V_{REF}	VREF input voltage	0.05		V_{CC}	V
R_X	R_X resistance value	12	56	100	kΩ
C_X	C_X capacitance value	470	680	1500	pF

(1) All V_M pins must be connected to the same supply voltage.

5.4 Thermal Information

THERMAL METRIC(1)		DRV8818 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.5 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	V_M operating supply current	V_M = 35V, f_{PWM} < 50kHz		7	10	mA
I_{VCC}	V_{CC} operating supply current	f_{PWM} < 50kHz		0.4	4	mA
I_{VMQ}	V_M sleep mode supply current	V_M = 35V		3	20	µA
I_{VCCQ}	V_{CC} sleep mode supply current			0.5	20	µA
V_{UVLO}	V_M undervoltage lockout voltage	V_M rising		6.7	7.5	V
	V_{CC} undervoltage lockout voltage	V_{CC} rising		2.75	2.95	
VREF INPUT/CURRENT CONTROL ACCURACY						
I_{REF}	VREF input current	VREF = 3.3V	–3		3	µA
ΔI_{CHOP}	Chopping current accuracy	VREF = 2.0V, 70% to 100% current	–5%		5%	
		VREF = 2.0V, 20% to 56% current	–10%		10%	
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage				0.3 × V_{CC}	V
V_{IH}	Input high voltage		0.7 × V_{CC}			V
V_{HYS}	Input hysteresis			300		mV
I_{IL}	Input low current	VIN = 0.3 × V_{CC}	–20		20	µA
I_{IH}	Input high current	VIN = 0.3 × V_{CC}	–20		20	µA
R_{PU}	Pullup resistance	ENABLEn, RESETn		1		MΩ
R_{PD}	Pulldown resistance	DIR, STEP, SLEEPn, USM1, USM0, SRn		1		MΩ
HOMEn OUTPUT						
V_{OL}	Output low voltage	I_O = 200µA			0.3 × VCC	V
V_{OH}	Output high voltage	I_O = –200 µA	0.7 × VCC			V
DECAY INPUT						
V_{IL}	Input low threshold voltage	For fast decay mode		0.21 × VCC		V
V_{IH}	Input high threshold voltage	For slow decay mode		0.6 × VCC		V
H-BRIDGE FETS						
$R_{ds(on)}$	HS FET on resistance	V_M = 24V, I_O = 2.5A, T_J = 25°C		0.22	0.30	Ω
$R_{ds(on)}$	LS FET on resistance	V_M = 24V, I_O = 2.5A, T_J = 25°C		0.15	0.24	Ω
I_{LEAK}	Output leakage current to ground in disable mode	H-bridges are Hi-Z, V_{VM} = 35V			4400	µA
PROTECTION CIRCUITS						
T_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
I_{OCP}	Overcurrent protection level		3.5			A
t_{OCP}	OCP deglitch time			1.5		µs
t_{RET}	OCP retry time			800		µs

5.6 Timing Requirements

T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
1	f_{STEP}	Step frequency			500	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	1			µs
3	$t_{WL(STEP)}$	Pulse duration, STEP low	1			µs
4	$t_{SU(STEP)}$	Setup time, command before STEP rising	200			ns
5	$t_{H(STEP)}$	Hold time, command after STEP rising	264			ns

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T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
6	t_{WAKE}	Wakeup time, SLEEPn inactive high to STEP input accepted			1	ms
7	t_{SLEEP}	Sleep time, SLEEPn active low to outputs disabled			5	µs
8	t_{ENABLE}	Enable time, ENABLEn logic low to outputs active			20	µs
9	$t_{DISABLE}$	Disable time, ENABLEn logic high to outputs disabled (Hi-Z)			20	µs
10	t_{RESETR}	Reset release time, RESETn inactive high to outputs enabled			80	µs
11	t_{RESET}	Reset time, RESETn active low to outputs disabled			7	µs

5.7 Motor Driver Timing Switching Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFF}	Off time	Rx = 56kΩ, Cx = 680pF	35	44	53	µs
t_{BLANK}	Current sense blanking time	Rx = 56kΩ, Cx = 680pF	900	1250	1500	ns
t_{DT}	Dead time	SRn = 0	100	475	800	ns
t_R	Rise time		10		80	ns
t_F	Fall time		10		80	ns

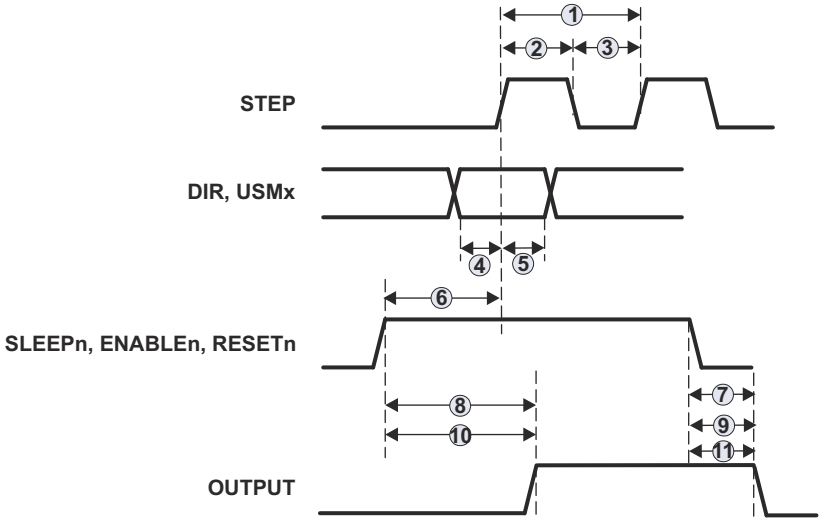

Figure 5-1. Timing Diagram

5.8 Typical Characteristics

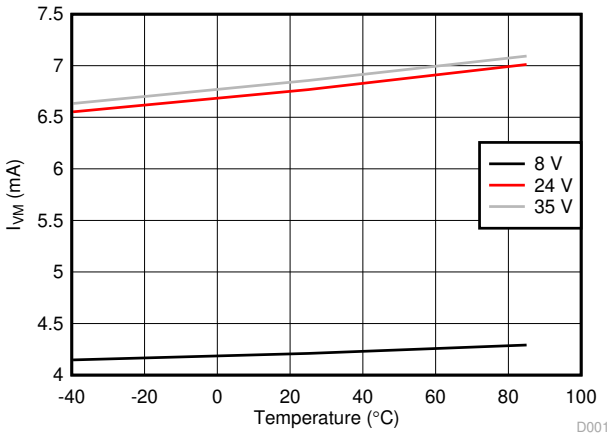

Figure 5-2. I_{VM} vs Temperature

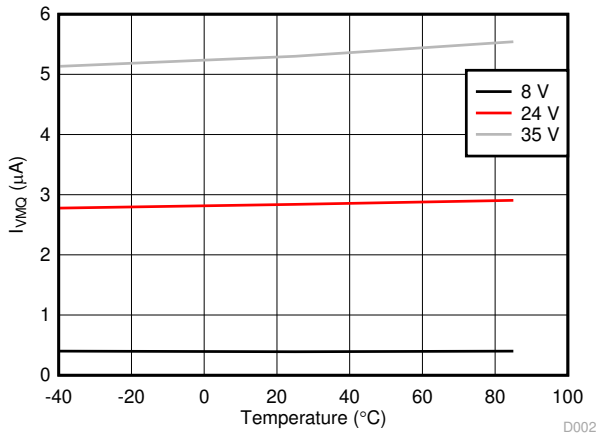

Figure 5-3. I_{VMQ} vs Temperature

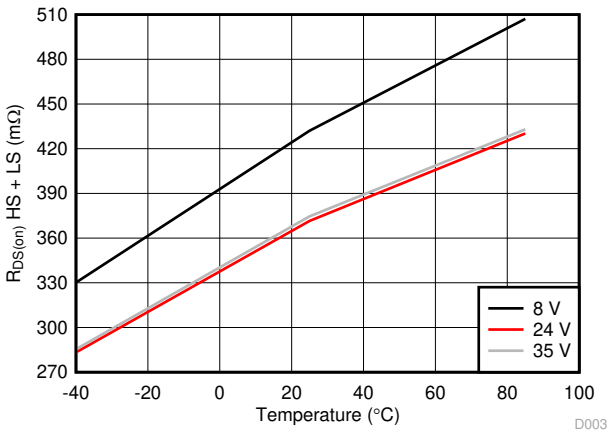

Figure 5-4. $R_{DS(ON)}$ HS + LS vs Temperature

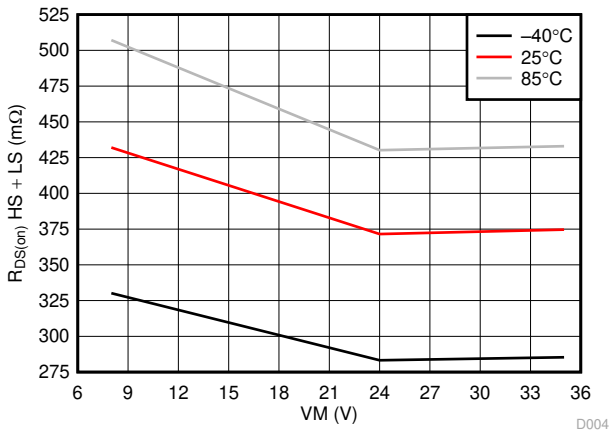

Figure 5-5. $R_{DS(ON)}$ HS + LS vs VM

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6 Detailed Description

6.1 Overview

The DRV8818 is a highly configurable, integrated motor driver for bipolar stepper motors. The device integrates two H-bridges, current sense and regulation circuitry, and a microstepping indexer. The DRV8818 can be powered with a supply voltage between 8V and 35V and is capable of providing an output current up to 2.5A full-scale.

A simple STEP/DIR interface allows for easy interfacing to the controller. The internal indexer is able to execute high-accuracy microstepping without requiring the controller to manage the current regulation loop.

The current regulation is highly configurable, with three decay modes of operation that can be selected depending on the application requirements: Fast Decay, Slow Decay, and Mixed Decay. The DRV8818 also provides configurable mixed decay, blanking time, and off time to adjust to a wide range of motors.

A low-power sleep mode is incorporated which allows for minimal power consumption when the system is idle.

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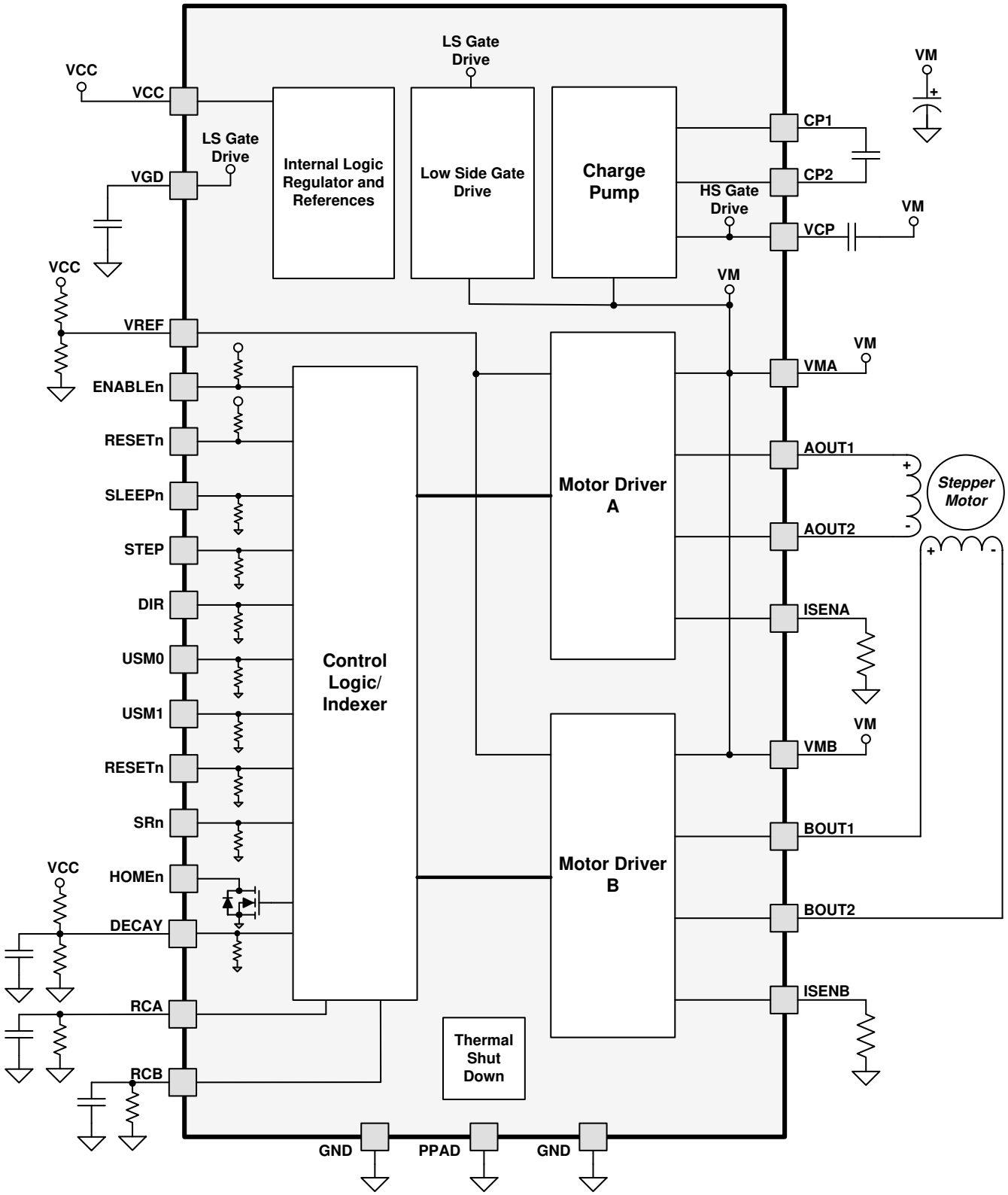
6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 PWM H-Bridge Drivers

DRV8818 contains two H-bridge motor drivers with current-control PWM circuitry, and a microstepping indexer. A block diagram of the motor control circuitry is shown below.

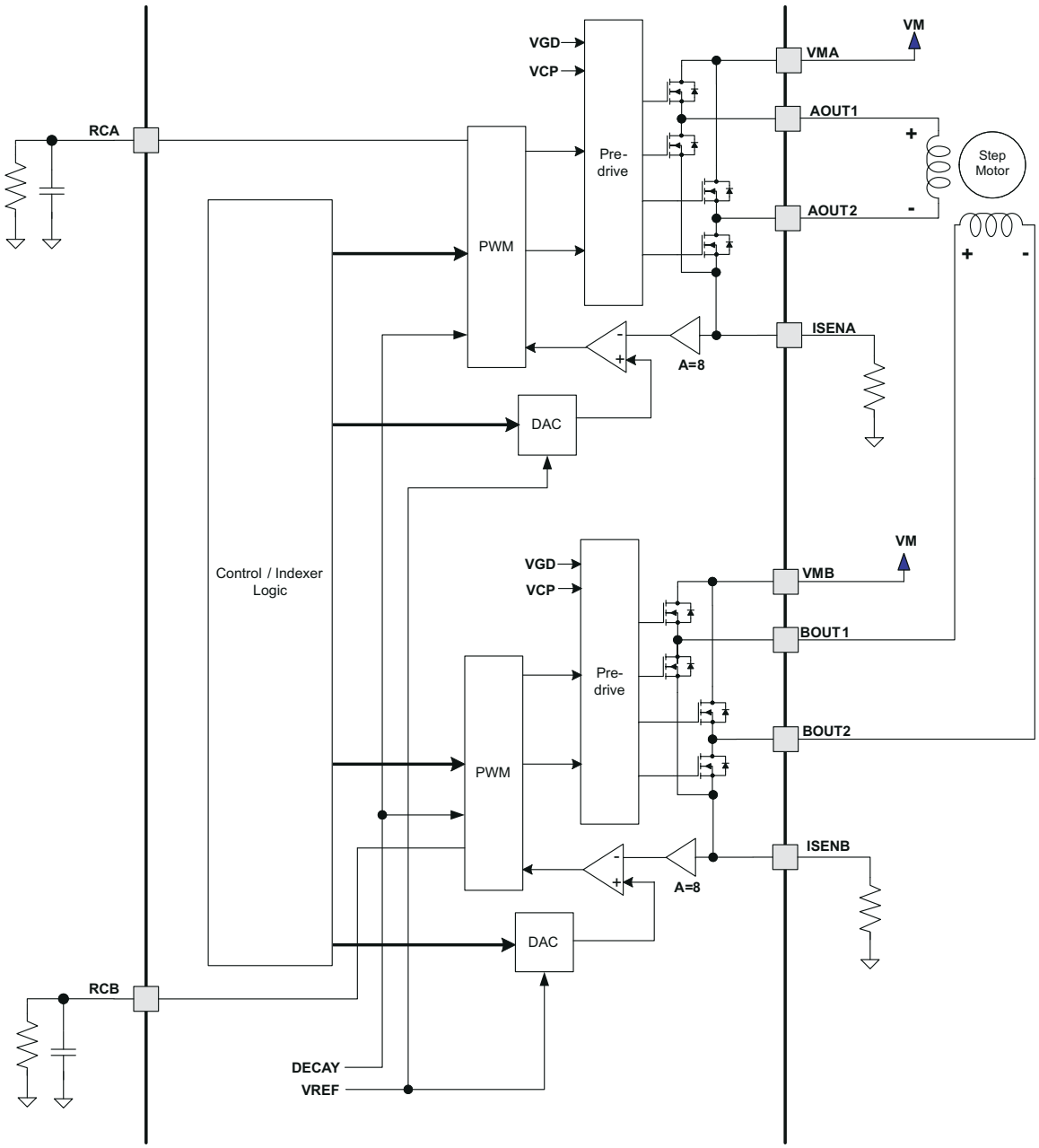

Figure 6-1. Motor Control Circuitry

6.3.2 Current Regulation

The PWM chopping current is set by a comparator, which compares the voltage across a current sense resistor, multiplied by a factor of 8, with a reference voltage. The reference voltage is input from the VREF pin. The full-scale (100%) chopping current is calculated as follows:

$$I_{CHOP}\ (A) = \frac{V_{VREF}\ (V)}{8 \times R_{SENSE}\ (\Omega)} \quad (1)$$

Example:

If a 0.22Ω sense resistor is used and the VREFx pin is 3.3V, the full-scale (100%) chopping current is 3.3V / (8 × 0.22Ω) = 1.875A.

The reference voltage is also scaled by an internal DAC that allows torque control for fractional stepping of a bipolar stepper motor, as described in the *Section 6.3.4* section.

When a winding is activated, the current through the winding rises until the chopping current threshold described above is reached, then the current is switched off for a fixed off time. The off time is determined by the values of a resistor and capacitor connected to the RCA (for bridge A) and RCB (for bridge B) pins. The off time is approximated by:

$$t_{OFF}\ (\mu s) = R\ (\Omega) \times C\ (nF) \quad (2)$$

To avoid falsely tripping on transient currents when the winding is first activated, a blanking period is used immediately after turning on the FETs, during which the state of the current sense comparator is ignored. The blanking time is determined by the value of the capacitor connected to the RCx pin and is approximated by:

$$t_{BLANK}\ (ns) = 1400\ (\Omega) \times C\ (nF) \quad (3)$$

6.3.3 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 6-2, Item 1. The current flow direction shown indicates positive current flow in the step table below.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. If synchronous rectification is enabled (SRn pin logic low), the opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. If SRn is high, current is recirculated through the body diodes, or through external Schottky diodes. Fast-decay mode is shown in Figure 6-2, Item 2.

In slow-decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 6-2, Item 3.

If SRn is high, current is recirculated only through the body diodes, or through external Schottky diodes. In this case fast decay is always used.

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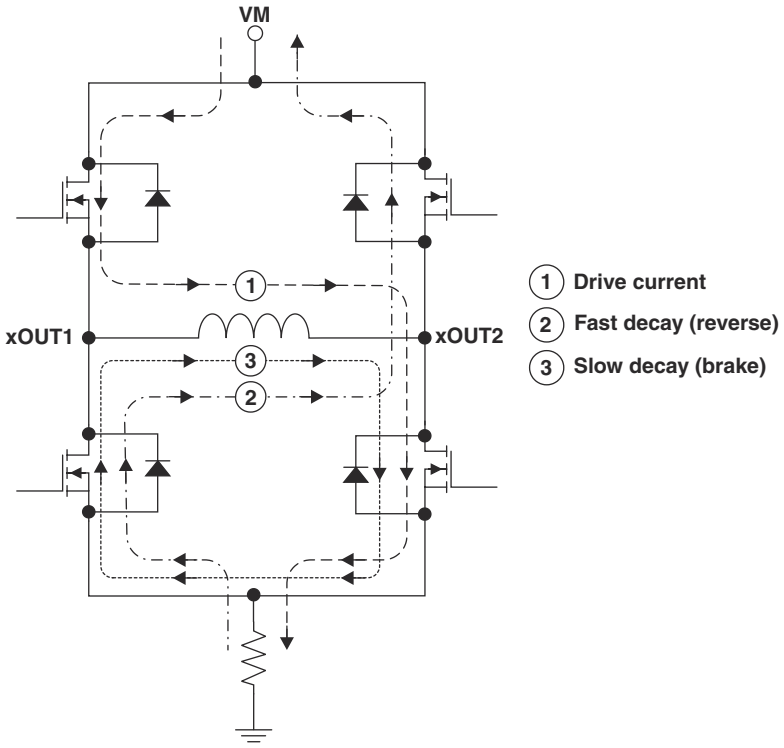

Figure 6-2. Decay Mode

The DRV8818 also supports a mixed decay mode. Mixed decay mode begins as fast decay, but after a period of time switches to slow decay mode for the remainder of the fixed off time.

Fast and mixed decay modes are only active if the current through the winding is decreasing; if the current is increasing, then slow decay is always used.

Which decay mode is used is selected by the voltage on the DECAY pin. If the voltage is greater than 0.6 × V_{CC}, slow decay mode is always used. If DECAY is less than 0.21 × V_{CC}, the device operates in fast decay mode when the current through the winding is decreasing. If the voltage is between these levels, mixed decay mode is enabled.

In mixed decay mode, the voltage on the DECAY pin sets the point in the cycle that the change to slow decay mode occurs. This time can be approximated by:

$$t_{FD}\ (\mu s) = R\ (\Omega) \times C\ (nF) \times \ln\left(\frac{0.6 \times V_{CC}\ (V)}{V_{DECAY}\ (V)}\right) \quad (4)$$

Mixed decay mode is only used while the current though the winding is decreasing; slow decay is used while the current is increasing.

Operation of the blanking, fixed off time, and mixed decay mode is illustrated in Figure 6-3.

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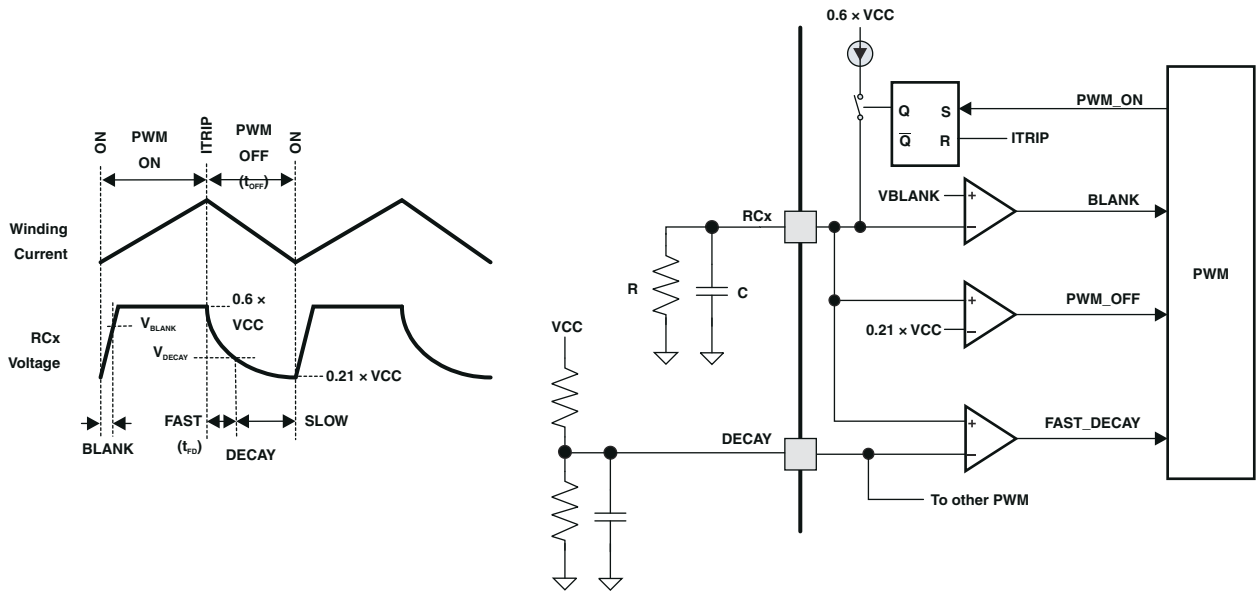

Figure 6-3. PWM

6.3.4 Microstepping Indexer

Built-in indexer logic in the DRV8818 allows a number of different stepping configurations. The USM1 and USM0 pins are used to configure the stepping format as shown in Table 6-1:

Table 6-1. Microstepping Selection Bits

USM1	USM0	STEP MODE
0	0	Full step (2-phase excitation)
0	1	1/2 step (1-2 phase excitation)
1	0	1/4 step (W1-2 phase excitation)
1	1	Eight microsteps/step

Table 6-2 shows the relative current and step directions for different settings of USM1 and USM0. At each rising edge of the STEP input, the indexer travels to the next state in the table. The direction is shown with the DIR pin high; if the DIR pin is low the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

Note that the home state is 45°. This state is entered at power-up or device reset. The HOMEn output pin is driven low in this state. In all other states the HOMEn pin is driven logic high.

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Table 6-2. Microstepping Indexer

FULL STEP USM = 00	1/2 STEP USM = 01	1/4 STEP USM = 10	1/8 STEP USM = 11	AOUTx CURRENT (% FULL-SCALE)	BOUTx CURRENT (% FULL-SCALE)	STEP ANGLE (°)
	1	1	1	100	0	0
			2	98	20	11.325
		2	3	92	38	22.5
			4	83	56	33.75
1	2	3	5	71	71	45 (home state)
			6	56	83	56.25
		4	7	38	92	67.5
			8	20	98	78.75
	3	5	9	0	100	90
			10	–20	98	101.25
		6	11	–38	92	112.5
			12	–56	83	123.75
2	4	7	13	–71	71	135
			14	–83	56	146.25
		8	15	–92	38	157.5
			16	–98	20	168.75
	5	9	17	–100	0	180
			18	–98	–20	191.25
		10	19	–92	–38	202.5
			20	–83	–56	213.75
3	6	11	21	–71	–71	225
			22	–56	–83	236.25
		12	23	–38	–92	247.5
			24	–20	–98	258.75
	7	13	25	0	–100	270
			26	20	–98	281.25
		14	27	38	–92	292.5
			28	56	–83	303.75
4	8	15	29	71	–71	315
			30	83	–56	326.25
		16	31	92	–38	337.5
			32	98	–20	348.75

6.3.5 Protection Circuits

6.3.5.1 Overcurrent Protection (OCP)

If the current through any FET exceeds the preset overcurrent threshold, all FETs in the H-bridge are disabled for a period of approximately 800µs, or until the ENABLEn pin has been brought inactive high and then back low, or power is removed and reapplied. Overcurrent conditions are sensed in both directions; that is, a short to ground, supply, or across the motor winding all result in an overcurrent shutdown.

Note that overcurrent protection does not use the current sense circuitry used for PWM current control and is independent of the Isense resistor value or VREF voltage. Additionally, in the case of an overcurrent event, the microstepping indexer is reset to the home state.

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6.3.5.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all drivers in the device are shut down and the indexer is reset to the home state. Once the die temperature has fallen to a safe level operation resumes.

6.3.5.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM or VCC pins falls below the VM or VCC undervoltage lockout threshold voltage, all circuitry in the device is disabled, and the indexer is reset to the home state. Operation resumes when VM and VCC both rise above each UVLO threshold.

6.4 Device Functional Modes

6.4.1 Sleep Mode

When the SLEEPn pin is low, the device enters a low-power sleep mode. In sleep mode all the internal MOSFETs are disabled (Hi-Z) and the internal logic regulator, charge pump, and internal clocks are all disabled. The t_{SLEEP} time must elapse after a falling edge on the SLEEPn pin before the device enters sleep mode. The device is brought out of sleep automatically if the SLEEPn pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

6.4.2 Disable Mode

The ENABLEn pin is used to control the outputs of the device. When ENABLEn is low, the output H-bridges are enabled. When ENABLEn is high, the H-bridges are disabled and the outputs are in a high-impedance state.

Note that when ENABLEn is high, the input pins and control logic, including the indexer (STEP and DIR pins) are still functional.

Table 6-3. Conditions to Enable or Disable Output Drivers

SLEEPn	ENABLEn	H-BRIDGE
0	X	Disabled
1	1	Disabled
1	0	Enabled

6.4.3 Active Mode

After the supply voltage on the VM pin has crossed the undervoltage threshold V_{UVLO}, the SLEEPn pin is logic high, and t_{WAKE} has elapsed, the device enters active operating mode. In this mode, the H-Bridge, charge pump, and internal logic are active and the device is ready to receive inputs.

This mode is enabled when -

- SLEEPn pin is logic high
- ENABLEn pin is logic low
- RESETn pin is logic high
- $V_M > V_{UVLO}$ for V_M
- $V_{CC} > V_{UVLO}$ for V_{CC}

The t_{WAKE} time must elapse before the device is ready for inputs.

6.4.4 Decay Modes

The DRV8818 supports three different decay modes: slow decay, fast decay, and mixed decay. The current through the motor windings is regulated using a fixed off time scheme.

This means that the current will increase until it reaches the current chopping threshold (I_{TRIP}), after which it will enter the set decay mode for a fixed period of time. The cycle will then repeat after the decay period expires.

The blanking time t_{BLANK} defines the minimum drive time for the current chopping. I_{TRIP} is ignored during t_{BLANK}, so the winding current may overshoot the trip level.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant the accuracy or completeness of this information. Customers are responsible for determining the appropriateness of components for the intended purposes, as well as validating and testing the design implementation to confirm system functionality

7.1 Application Information

The DRV8818 is used for bipolar stepper motor control. The microstepping motor driver provides precise regulation of the coil current and maintains a smooth rotation from the stepper motor.

7.2 Typical Application

Figure 7-1 shows a common system application of the DRV8818.

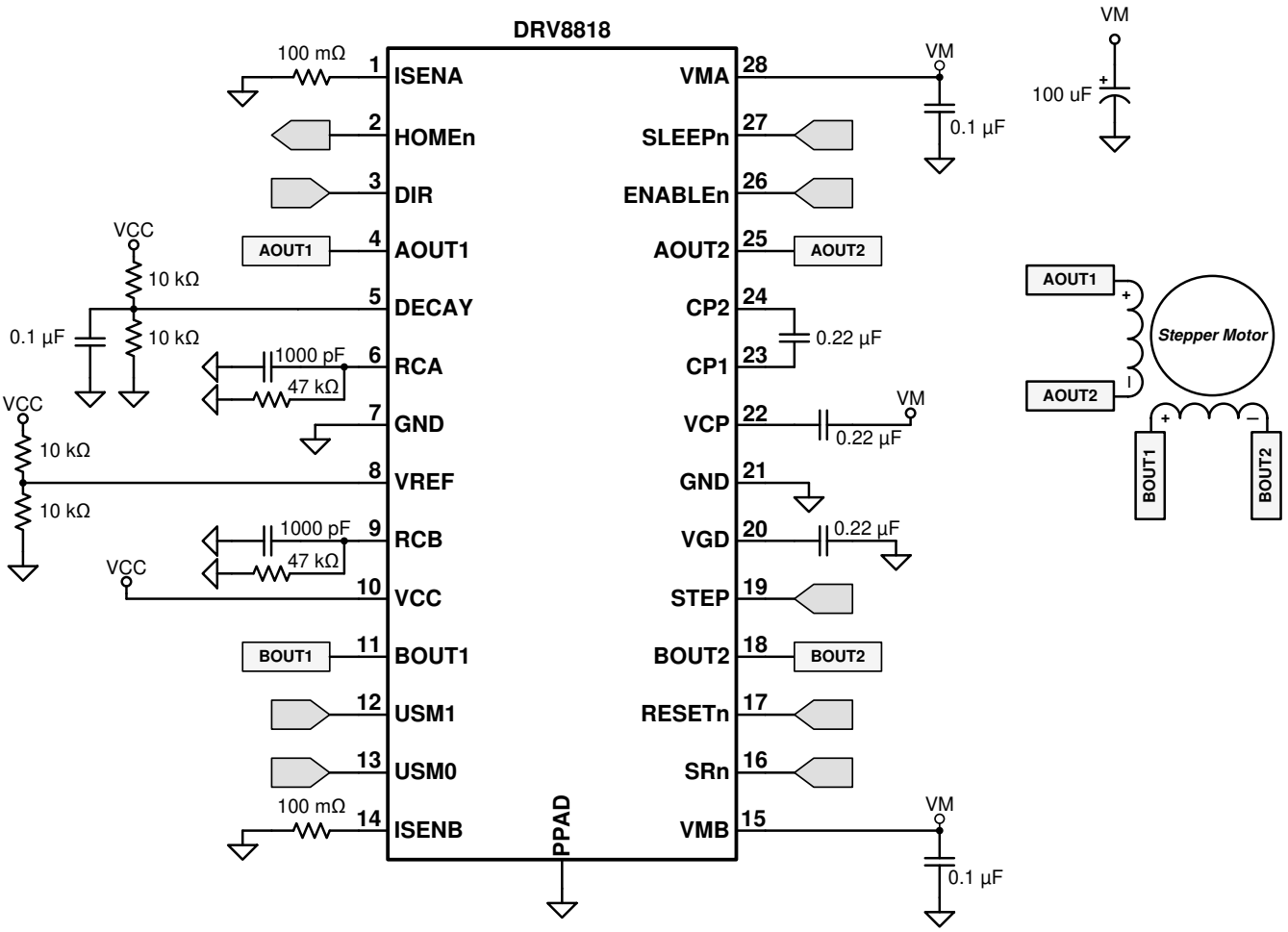

Figure 7-1. Typical Application Schematic

7.2.1 Design Requirements

See Table 7-1 for the design parameters.

Table 7-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	VM	24V
Motor Winding Resistance	R_L	4.0Ω
Motor Winding Inductance	I_L	3.7mH
Motor Full Step Angle	θ_{step}	1.8°/step
Target Microstepping Level	n_m	8 µsteps per step
Target Motor Speed	v	120 RPM
Target Full-Scale Current	I_{FS}	1.25A

7.2.2 Detailed Design Procedure

7.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8818 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin.

A high target motor start-up speed causes the motor to fail to spin. Make sure that the motor can support the target speed or implement an acceleration profile to bring the motor up to speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}\left(\mu steps / second\right) = \frac{v\left(\frac{rotations}{minute}\right) \times 360\left(\frac{^\circ}{rotation}\right) \times n_m\left(\frac{\mu steps}{step}\right)}{60\left(\frac{seconds}{minute}\right) \times \theta_{step}\left(\frac{^\circ}{step}\right)} \quad (5)$$

$$f_{step}\left(\mu steps / second\right) = \frac{120\left(\frac{rotations}{minute}\right) \times 360\left(\frac{^\circ}{rotation}\right) \times 8\left(\frac{\mu steps}{step}\right)}{60\left(\frac{seconds}{minute}\right) \times 1.8\left(\frac{^\circ}{step}\right)} \quad (6)$$

θ_{step} can be found in the stepper motor data sheet or written on the motor body.

For the DRV8818, the microstepping level is set by the USMx pins. Higher microstepping results in smoother motor motion and less audible noise, but increasing switching losses and requires a higher f_{step} to achieve the same motor speed.

7.2.2.2 Current Regulation

In a stepper motor, the set full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the VREF analog voltage and the sense resistor value (R_{SENSE}). During stepping, I_{FS} defines the current chopping threshold (ITRIP) for the maximum current step. The gain of DRV8818 is set for 8V/V.

$$I_{FS}\left(A\right) = \frac{VREF(V)}{A_v \; x \; R_{SENSE}\left(\Omega\right)} = \frac{VREF(V)}{8 \; x \; R_{SENSE}\left(\Omega\right)} \quad (7)$$

To achieve I_{FS} = 1.25A with R_{SENSE} of 0.1Ω, set VREF to 1.56V.

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7.2.3 Application Curves

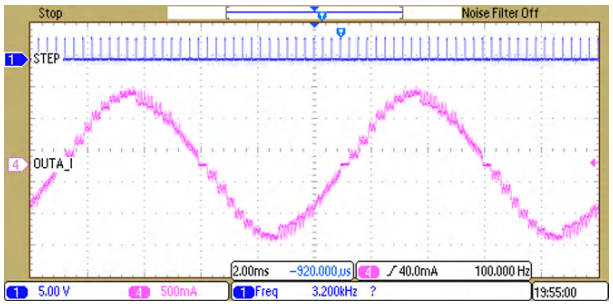

Figure 7-2. Mixed Decay

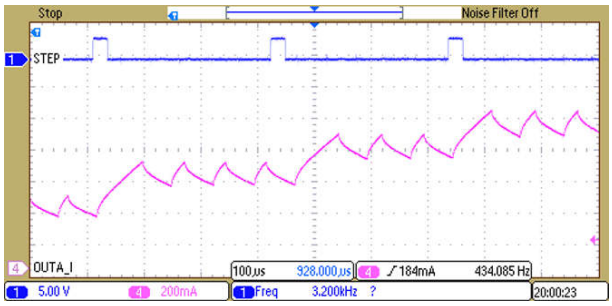

Figure 7-3. Slow Decay on Increasing Steps

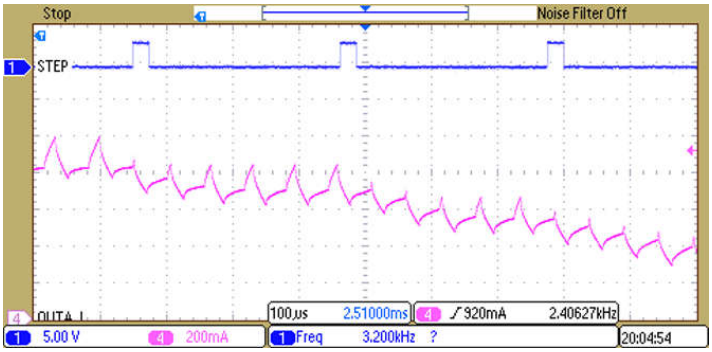

Figure 7-4. Mixed Decay on Decreasing Steps

7.3 Power Supply Recommendations

7.3.1 Bulk Capacitance

Appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, although the disadvantages include increased cost and physical size. Bulk capacitors near the motor driver act as a local reservoir of electrical charge to smooth out the motor current variation.

Experienced engineers often use general guidelines about bulk capacitance to select the capacitor values. One such guideline says to use at least 1 to 4µF of capacitance for each Watt of motor power. For example, a motor which draws 10 Amps from a 12V supply has a power of 120 Watts, leading to bulk capacitance of 120 to 480µF, using this general guideline.

The voltage rating for bulk capacitors must be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

A large value of bulk capacitance is desired to provide a constant motor supply voltage during current transitions, such as motor start-up, changes in load torque, or PWM operation. A working estimate of the required capacitance for consistent supply is essential to reduce complexity, cost and size of board electronics. We can use a general guideline method to find an appropriate capacitor size based on the expected load current variation and allowable motor supply voltage variation:

$$C_{BULK} > k \times \Delta I_{MOTOR} \times T_{PWM} / \Delta V_{SUPPLY} \quad (8)$$

Where:

C_{BULK} is the bulk capacitance

k is a scale factor to account for the ESR for typical capacitors in this type of application; based on the lab measurements with DRV8718-Q1EVM, k ≈ 3 is practical for these cases.

ΔI_{MOTOR} is the expected variation in motor current, $i_{max} - i_{min}$

T_{PWM} is the PWM period which is the reciprocal of the PWM frequency

ΔV_{SUPPLY} is the allowable variation in the motor supply voltage

Figure 7-5 plots several data points and applies this general guideline, showing relatively good agreement.

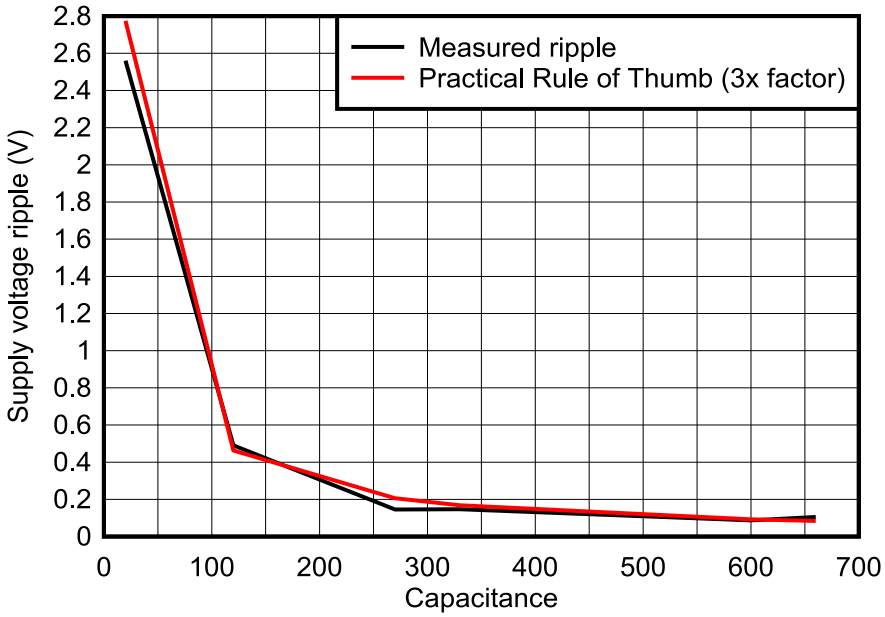

Figure 7-5. Measured Results and 3x General Guideline, Accounting for Real-World Non-Zero ESR Values of Electrolytic Capacitors

For more information please see the Application Note Bulk Capacitor Sizing for DC Motor Drive Applications .

7.4 Layout

7.4.1 Layout Guidelines

Bypass the VMA and VMB pins to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1µF rated for VM. Place this capacitor as close to the VMA and VMB pins as possible with a thick trace or ground plane connection to the device GND pin.

Bypass the VMA and VMB pins to GND using an appropriate bulk capacitor. This component is often an electrolytic and is best located close to the DRV8818.

A low-ESR ceramic capacitor must be placed in between the CP1 and CP2 pins. TI recommends a value of 0.22µF rated for VM. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 0.22µF rated for 16V. Place this component as close to the pins as possible.

The PowerPAD must be securely connected to a copper plane that is connected to system GND. For best performance, use a copper place with a large area to allow for thermal dissipation from the DRV8818A. See Application Note - Best Practices for Board Layout of Motor Drivers for more information on thermal management, routing techniques, capacitor placement, and grounding optimization for motor drivers.

7.4.1.1 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area

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is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI Application Report SLMA002, *PowerPAD™ Thermally Enhanced Package* and TI Application Brief SLMA004, *PowerPAD™ Made Easy*, available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

7.4.2 Layout Example

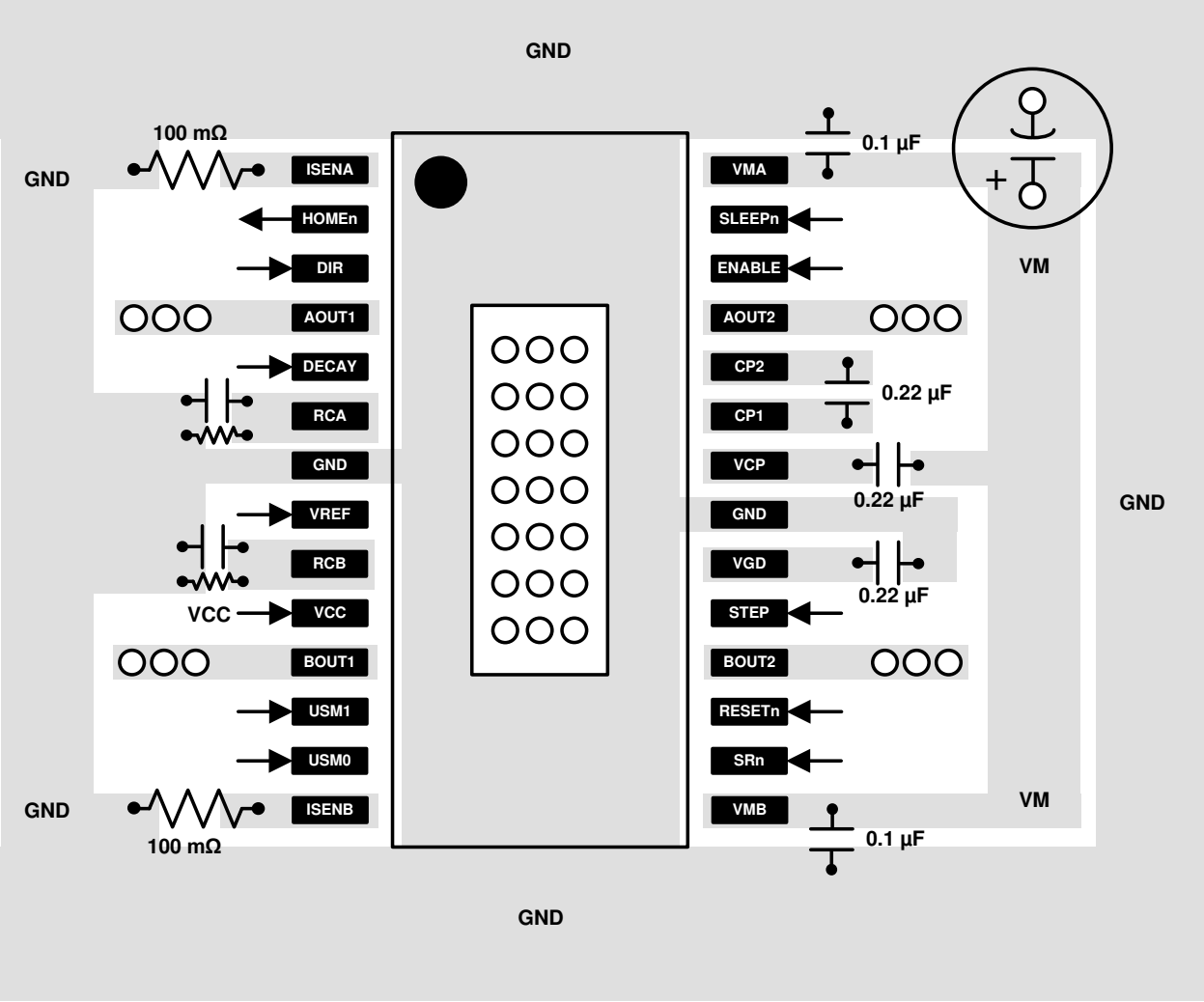

Figure 7-6. Layout Example Schematic

7.4.3 Thermal Considerations

The DRV8818 has thermal shutdown (TSD) as described previously. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high ambient temperature.

7.4.3.1 Power Dissipation

Power dissipation in the DRV8818 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by:

$$P_{TOT} = 4 \times r_{DS(on)} \times (I_{OUT(RMS)})^2 \quad (9)$$

where

- P_{TOT} is the total power dissipation.
- $R_{DS(ON)}$ is the resistance of each FET.
- $I_{OUT(RMS)}$ is the RMS output current being applied to each winding.

$I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the DRV8818 is dependent on ambient temperature and heatsinking. The thermal dissipation ratings table in the data sheet can be used to estimate the temperature rise for typical PCB constructions.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

1. *PowerPAD™ Thermally Enhanced Package*, SLMA002
2. *PowerPAD™ Made Easy*, SLMA004
3. *Current Recirculation and Decay Modes*, SLVA321
4. *Calculating Motor Driver Power Dissipation*, SLVA504
5. *Understanding Motor Driver Current Ratings*, SLVA505

8.2 Community Resources

8.3 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
is a trademark of Texas Instruments.
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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2016) to Revision F (February 2025) **Page**

- Changed V_{REF} minimum voltage from 0V to 0.05V 5
- Renamed I_{OFF} to I_{LEAK}, updated description and limits 6
- Changed *Timing Requirements* enable time and disable time descriptions. Updated hold time, reset release time, and reset time limits 6
- Added *Sleep Mode* section, *Disable Mode* section, and *Active Mode* section within *Device Functional Modes* section 16
- Updated bulk capacitance description 19

Changes from Revision D (January 2015) to Revision E (January 2016) **Page**

- Removed nFAULT from *Features* 1
- Changed the minimum value for V_{REF} input voltage 5
- Moved the motor driver timing to the *Switching Characteristics* table 7
- Added *Section 8.2* 23

Changes from Revision C (November 2013) to Revision D (July 2014) **Page**

- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 5

Changes from Revision B (October 2012) to Revision C (November 2013) **Page**

- Changed Features section 1
- Changed Logic-Level Inputs test conditions in the Electrical Characteristics table 6
- Changed *Timing Requirements* 6

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8818PWP	Obsolete	Production	HTSSOP (PWP) | 28	-	-	Call TI	Call TI	-40 to 85	DRV8818
DRV8818PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8818
DRV8818PWPR.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8818
DRV8818PWPR.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8818
DRV8818PWPRG4.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8818
DRV8818PWPRG4.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8818

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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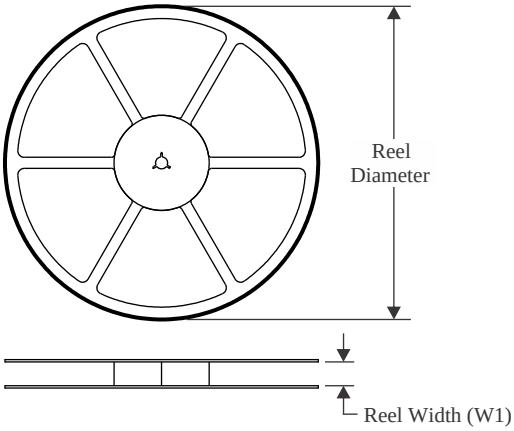
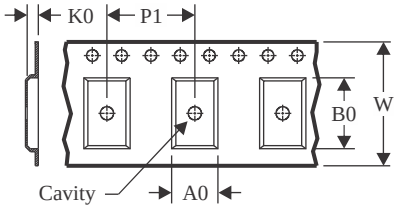
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

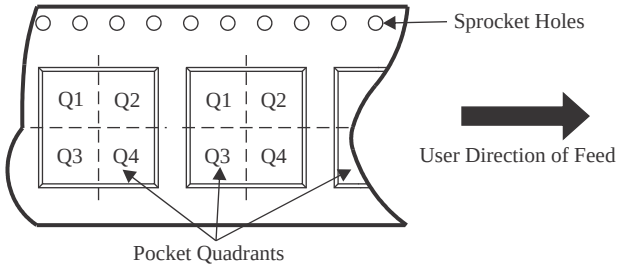


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

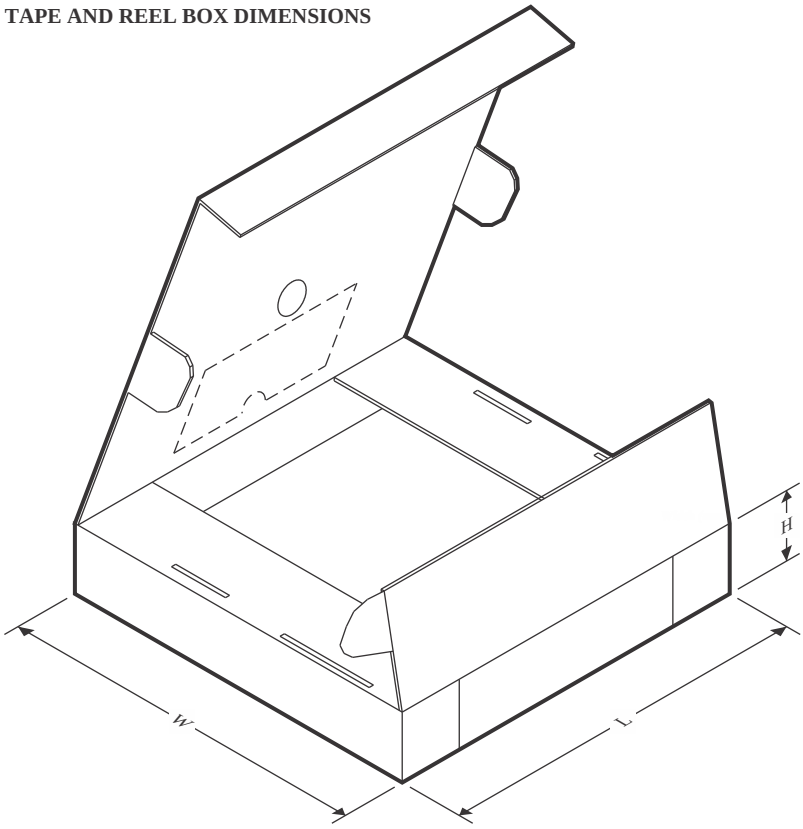
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8818PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8818PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

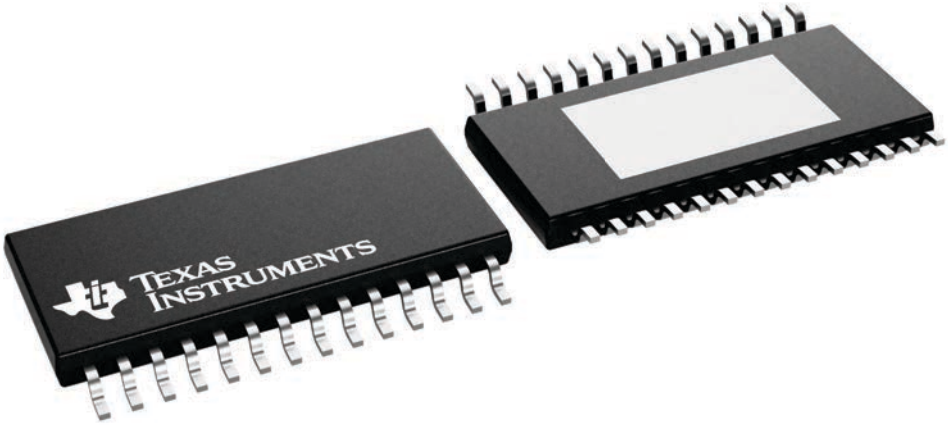
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

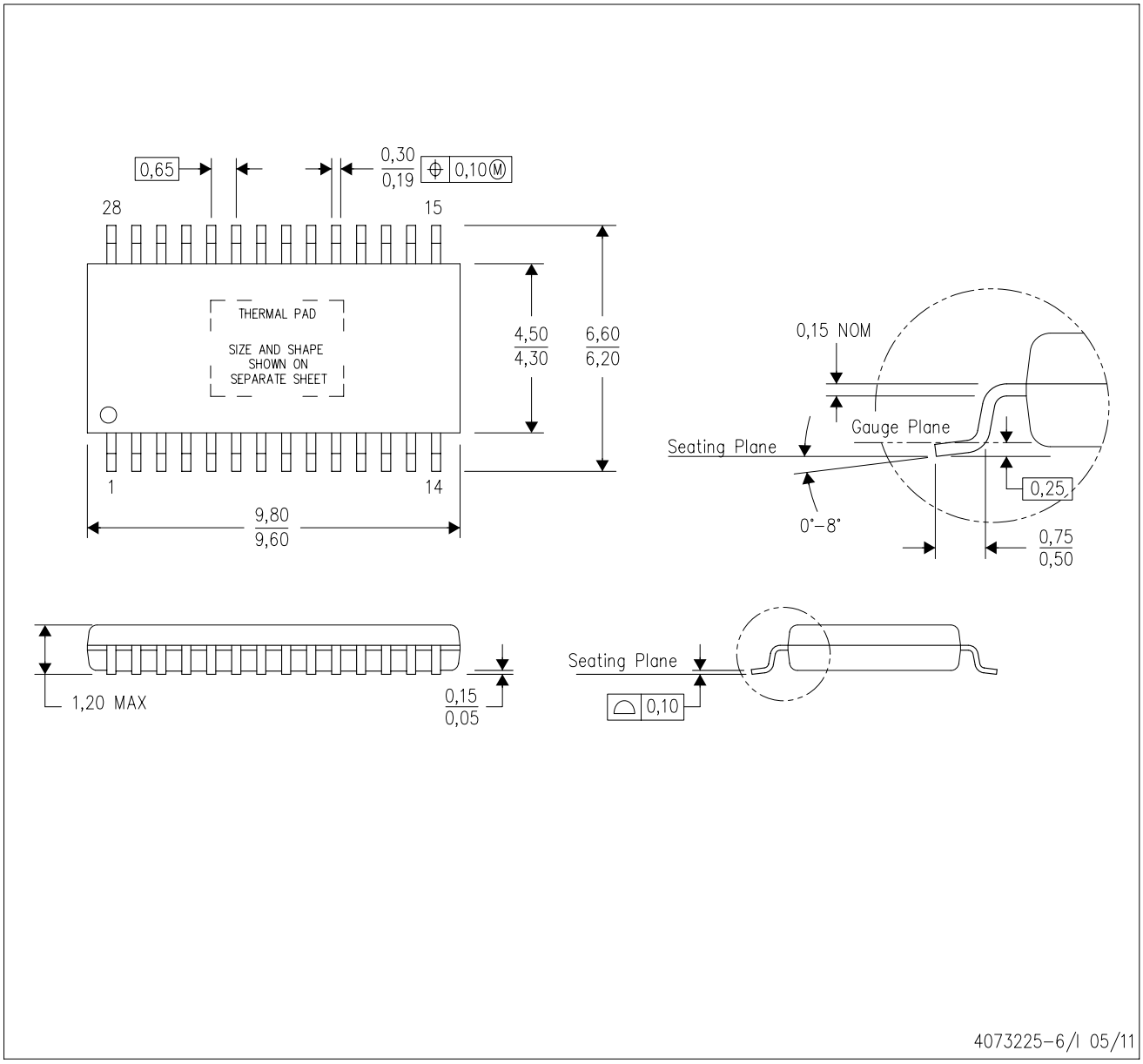
4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

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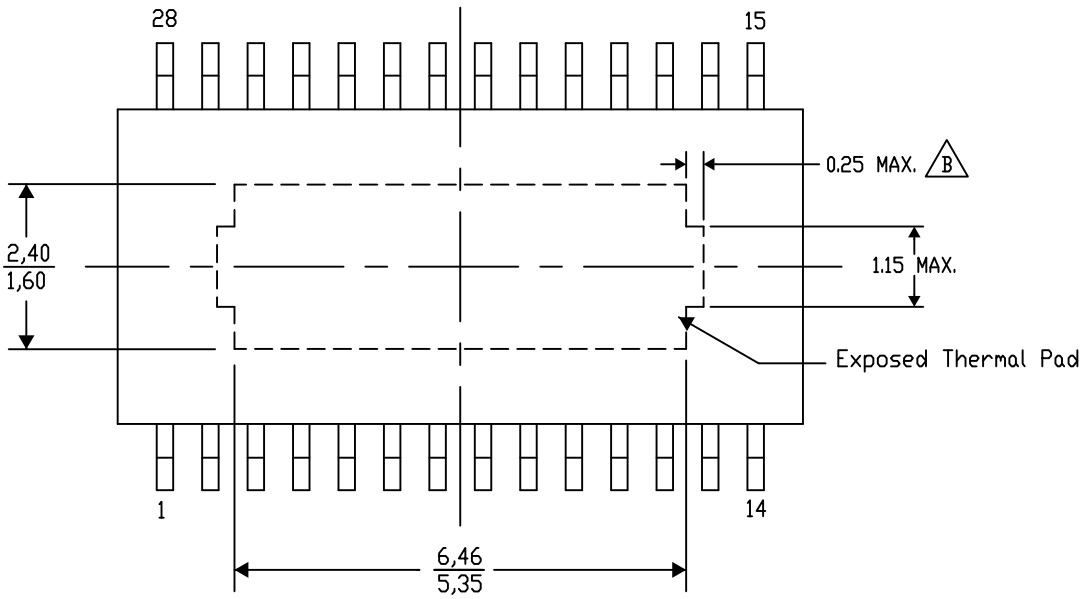
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–34/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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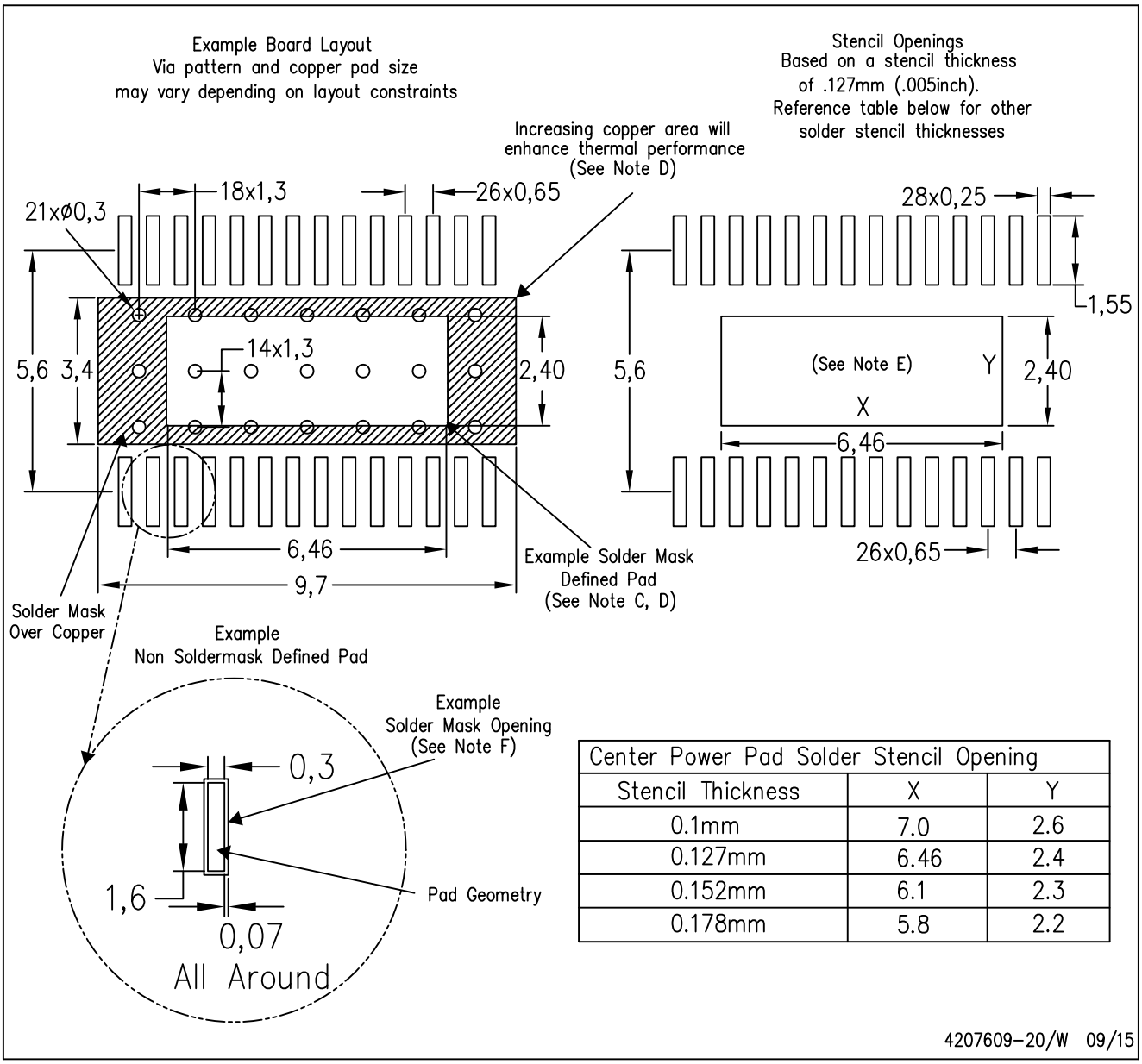
PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.0	2.6
0.127mm	6.46	2.4
0.152mm	6.1	2.3
0.178mm	5.8	2.2

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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