

- Low Supply Voltage Range 1.8 V to 3.6 V
- Ultralow-Power Consumption:
  - Active Mode: 200  $\mu$ A at 1 MHz, 2.2 V
  - Standby Mode: 0.7  $\mu$ A
  - Off Mode (RAM Retention): 0.1  $\mu$ A
- Five Power Saving Modes
- Wake-Up From Standby Mode in less than 6  $\mu$ s
- 16-Bit RISC Architecture, 125 ns Instruction Cycle Time
- Basic Clock Module Configurations:
  - Various Internal Resistors
  - Single External Resistor
  - 32-kHz Crystal
  - High Frequency Crystal
  - Resonator
  - External Clock Source
- 16-Bit Timer\_A With Three Capture/Compare Registers
- 10-Bit, 200-ksps A/D Converter With Internal Reference, Sample-and-Hold, Autoscan, and Data Transfer Controller
- Serial Communication Interface (USART0) With Software-Selectable Asynchronous UART or Synchronous SPI (MSP430x12x2 Only)
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- Supply Voltage Brownout Protection
- MSP430x11x2 Family Members Include:
  - MSP430F1122: 4KB + 256B Flash Memory 256B RAM
  - MSP430F1132: 8KB + 256B Flash Memory 256B RAMAvailable in 20-Pin Plastic SOWB, 20-Pin Plastic TSSOP and 32-Pin QFN Packages
- MSP430x12x2 Family Members Include:
  - MSP430F1222: 4KB + 256B Flash Memory 256B RAM
  - MSP430F1232: 8KB + 256B Flash Memory 256B RAMAvailable in 28-Pin Plastic SOWB, 28-Pin Plastic TSSOP, and 32-Pin QFN Packages
- For Complete Module Descriptions, See the *MSP430x1xx Family User's Guide*, Literature Number SLAU049

## description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 $\mu$ s.

The MSP430x11x2 and MSP430x12x2 series are ultralow-power mixed signal microcontrollers with a built-in 16-bit timer, 10-bit A/D converter with integrated reference and data transfer controller (DTC) and fourteen or twenty-two I/O pins. In addition, the MSP430x12x2 series microcontrollers have built-in communication capability using asynchronous (UART) and synchronous (SPI) protocols.

Digital signal processing with the 16-bit RISC performance enables effective system solutions such as glass breakage detection with signal analysis (including wave digital filter algorithm). Another area of application is in stand-alone RF sensors.



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# MSP430x11x2, MSP430x12x2 MIXED SIGNAL MICROCONTROLLER

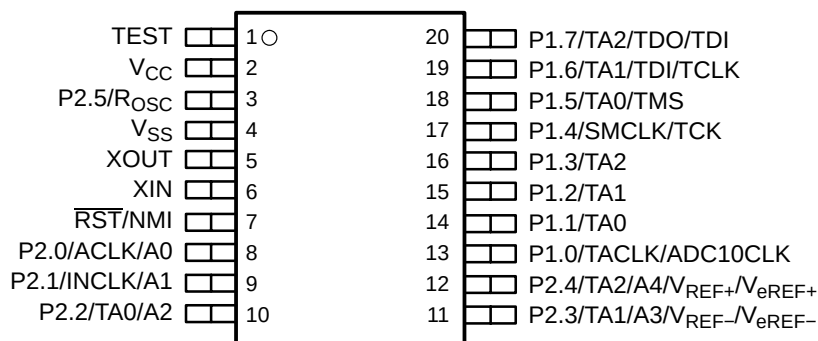
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## AVAILABLE OPTIONS

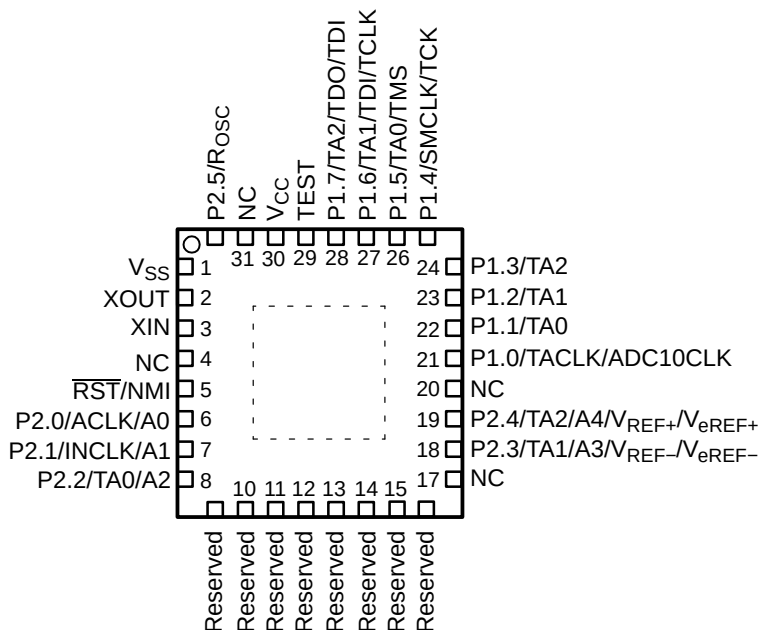
| T <sub>A</sub> | PACKAGED DEVICES                 |                                  |                                  |                                  |                                                                          |
|----------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|--------------------------------------------------------------------------|
|                | PLASTIC 20-PIN<br>SOWB (DW)      | PLASTIC 20-PIN<br>TSSOP (PW)     | PLASTIC 28-PIN<br>SOWB (DW)      | PLASTIC 28-PIN<br>TSSOP (PW)     | PLASTIC 32-PIN<br>QFN (RHB)                                              |
| –40°C to 85°C  | MSP430F1122IDW<br>MSP430F1132IDW | MSP430F1122IPW<br>MSP430F1132IPW | MSP430F1222IDW<br>MSP430F1232IDW | MSP430F1222IPW<br>MSP430F1232IPW | MSP430F1122IRHB<br>MSP430F1132IRHB<br>MSP430F1222IRHB<br>MSP430F1232IRHB |

pin designation, MSP430x11x2 (see Notes 1, 2 and 3)

### DW or PW PACKAGE (TOP VIEW)



### RHB PACKAGE (TOP VIEW)



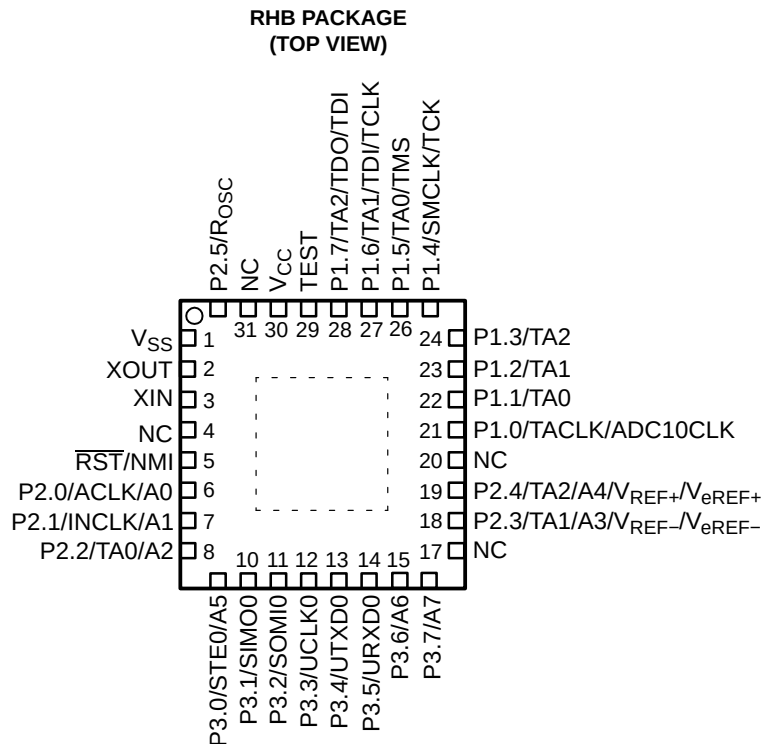
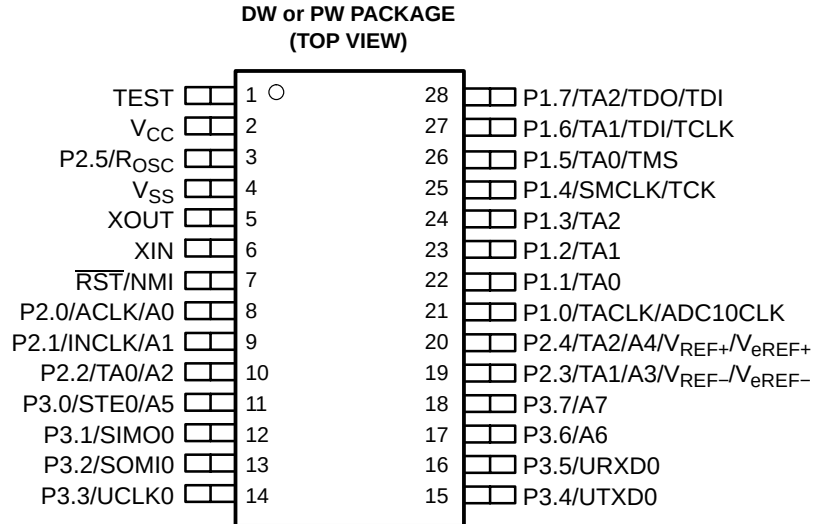
- NOTES: 1. NC pins are not internally connected. Recommended connection to V<sub>SS</sub>.  
 2. Recommended connection to V<sub>SS</sub> for all pins labeled "Reserved" to avoid floating nodes, otherwise increased current consumption may occur.  
 3. Power pad connection to V<sub>SS</sub> recommended.



# MSP430x11x2, MSP430x12x2 MIXED SIGNAL MICROCONTROLLER

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pin designation, MSP430x12x2 (see Notes 1 and 2)

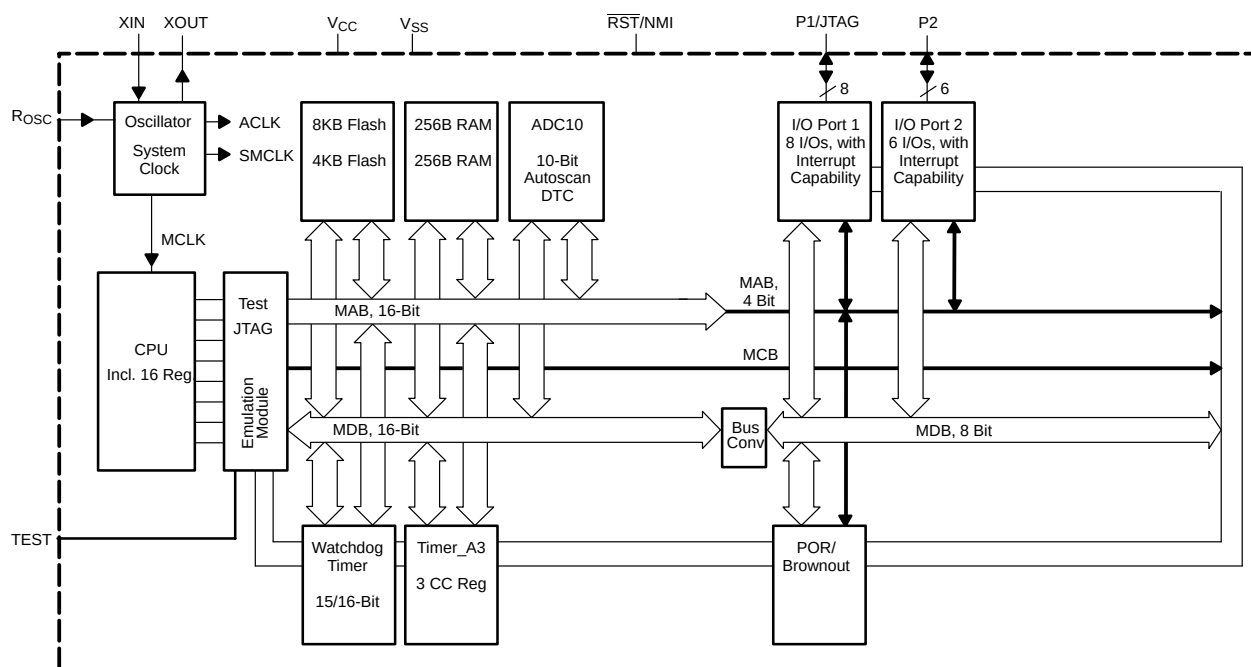


- NOTES: 1. NC pins are not internally connected. Recommended connection to V<sub>SS</sub>.  
2. Power pad connection to V<sub>SS</sub> recommended.

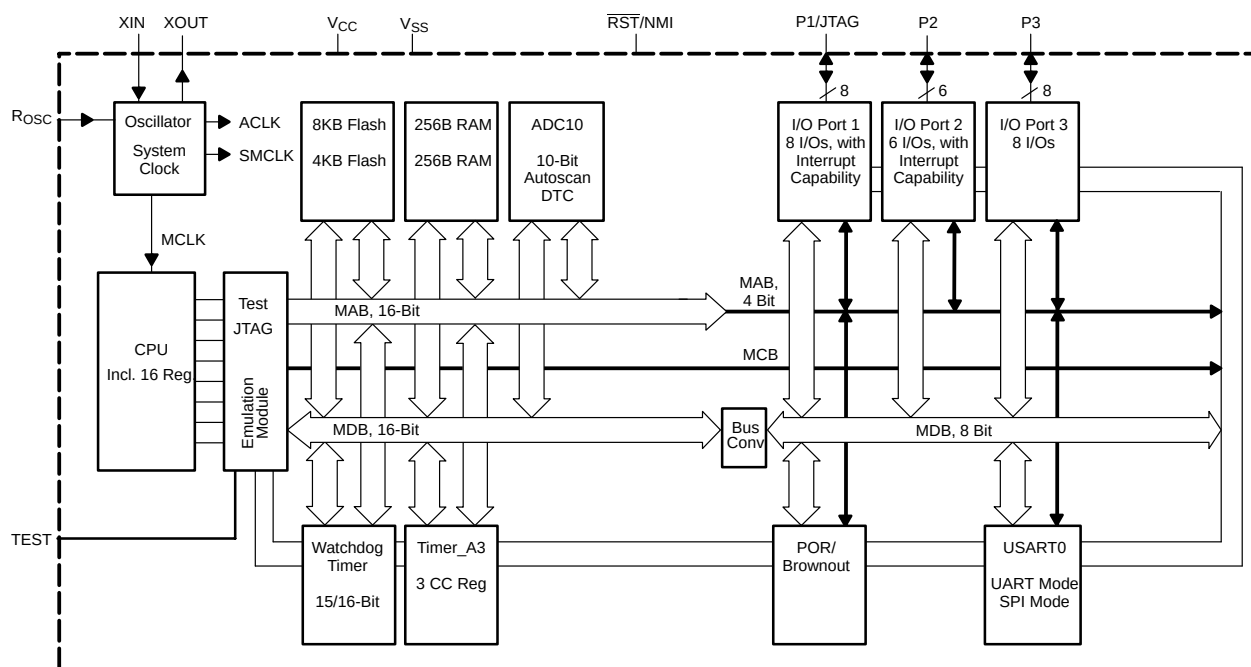
# MSP430x11x2, MSP430x12x2 MIXED SIGNAL MICROCONTROLLER

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## functional block diagram, MSP430x11x2



## functional block diagram, MSP430x12x2



# MSP430x11x2, MSP430x12x2 MIXED SIGNAL MICROCONTROLLER

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## Terminal Functions, MSP430x11x2

| TERMINAL                                             |         |             | I/O | DESCRIPTION                                                                                                                                                  |
|------------------------------------------------------|---------|-------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                                 | DW & PW | RHB         |     |                                                                                                                                                              |
| P1.0/TACLK/<br>ADC10CLK                              | 13      | 21          | I/O | General-purpose digital I/O pin/Timer_A, clock signal TACLK input/conversion clock—10-bit ADC                                                                |
| P1.1/TA0                                             | 14      | 22          | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit                                                             |
| P1.2/TA1                                             | 15      | 23          | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output                                                                          |
| P1.3/TA2                                             | 16      | 24          | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output                                                                          |
| P1.4/SMCLK/TCK                                       | 17      | 25          | I/O | General-purpose digital I/O pin/SMCLK signal output/test clock, input terminal for device programming and test                                               |
| P1.5/TA0/TMS                                         | 18      | 26          | I/O | General-purpose digital I/O pin/Timer_A, compare: Out0 output/test mode select, input terminal for device programming and test                               |
| P1.6/TA1/TDI/TCLK                                    | 19      | 27          | I/O | General-purpose digital I/O pin/Timer_A, compare: Out1 output/test data input terminal or test clock input                                                   |
| P1.7/TA2/TDO/TDI <sup>†</sup>                        | 20      | 28          | I/O | General-purpose digital I/O pin/Timer_A, compare: Out2 output/test data output terminal or data input during programming                                     |
| P2.0/ACLK/A0                                         | 8       | 6           | I/O | General-purpose digital I/O pin/ACLK output/analog input to 10-bit ADC input A0                                                                              |
| P2.1/INCLK/A1                                        | 9       | 7           | I/O | General-purpose digital I/O pin/Timer_A, clock signal at INCLK/analog input to 10-bit ADC input A1                                                           |
| P2.2/TA0/A2                                          | 10      | 8           | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI0B input, compare: Out0 output/analog input to 10-bit ADC input A2/BSL receive                          |
| P2.3/TA1/A3/V <sub>REF-</sub> /<br>V <sub>REF-</sub> | 11      | 18          | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI1B input, compare: Out1 output/analog input to 10-bit ADC input A3/negative reference voltage terminal. |
| P2.4/TA2/A4/V <sub>REF+</sub> /<br>V <sub>REF+</sub> | 12      | 19          | I/O | General-purpose digital I/O pin/Timer_A, compare: Out2 output/analog input to 10-bit ADC input A4/I/O of positive reference voltage terminal                 |
| P2.5/R <sub>OSC</sub>                                | 3       | 32          | I/O | General-purpose digital I/O pin/Input for external resistor that defines the DCO nominal frequency                                                           |
| RST/NMI                                              | 7       | 5           | I   | Reset or nonmaskable interrupt input                                                                                                                         |
| TEST                                                 | 1       | 29          | I   | Selects test mode for JTAG pins on P1.x                                                                                                                      |
| V <sub>CC</sub>                                      | 2       | 30          |     | Supply voltage                                                                                                                                               |
| V <sub>SS</sub>                                      | 4       | 1           |     | Ground reference                                                                                                                                             |
| XIN                                                  | 6       | 3           | I   | Input terminal of crystal oscillator                                                                                                                         |
| XOUT                                                 | 5       | 2           | O   | Output terminal of crystal oscillator                                                                                                                        |
| NC                                                   | NA      | 4,17,20,31  |     | Not connected internally. Recommended connection to V <sub>SS</sub> .                                                                                        |
| Reserved                                             | NA      | 9 - 16      |     | Reserved pins. Recommended connection to V <sub>SS</sub> to avoid floating nodes, otherwise increased current consumption may occur.                         |
| QFN Pad                                              | NA      | Package Pad |     | QFN package pad connection to V <sub>SS</sub> recommended.                                                                                                   |

<sup>†</sup> TDO or TDI is selected via JTAG instruction.



# MSP430x11x2, MSP430x12x2 MIXED SIGNAL MICROCONTROLLER

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## Terminal Functions, MSP430x12x2

| TERMINAL                                             |         |            | I/O | DESCRIPTION                                                                                                                                                  |
|------------------------------------------------------|---------|------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                                 | DW & PW | RHB        |     |                                                                                                                                                              |
| P1.0/TACLK/<br>ADC10CLK                              | 21      | 21         | I/O | General-purpose digital I/O pin/Timer_A, clock signal TACLK input/conversion clock—10-bit ADC                                                                |
| P1.1/TA0                                             | 22      | 22         | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit                                                             |
| P1.2/TA1                                             | 23      | 23         | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output                                                                          |
| P1.3/TA2                                             | 24      | 24         | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output                                                                          |
| P1.4/SMCLK/TCK                                       | 25      | 25         | I/O | General-purpose digital I/O pin/SMCLK signal output/test clock, input terminal for device programming and test                                               |
| P1.5/TA0/TMS                                         | 26      | 26         | I/O | General-purpose digital I/O pin/Timer_A, compare: Out0 output/test mode select, input terminal for device programming and test                               |
| P1.6/TA1/TDI/TCLK                                    | 27      | 27         | I/O | General-purpose digital I/O pin/Timer_A, compare: Out1 output/test data input terminal or test clock input                                                   |
| P1.7/TA2/TDO/TDI <sup>†</sup>                        | 28      | 28         | I/O | General-purpose digital I/O pin/Timer_A, compare: Out2 output/test data output terminal or data input during programming                                     |
| P2.0/ACLK/A0                                         | 8       | 6          | I/O | General-purpose digital I/O pin/ACLK output/analog input to 10-bit ADC input A0                                                                              |
| P2.1/INCLK/A1                                        | 9       | 7          | I/O | General-purpose digital I/O pin/Timer_A, clock signal at INCLK/analog input to 10-bit ADC input A1                                                           |
| P2.2/TA0/A2                                          | 10      | 8          | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI0B input, compare: Out0 output/analog input to 10-bit ADC input A2/BSL receive                          |
| P2.3/TA1/A3/V <sub>REF-</sub> /<br>V <sub>REF-</sub> | 19      | 18         | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI1B input, compare: Out1 output/analog input to 10-bit ADC input A3/negative reference voltage terminal. |
| P2.4/TA2/A4/V <sub>REF+</sub> /<br>V <sub>REF+</sub> | 20      | 19         | I/O | General-purpose digital I/O pin/Timer_A, compare: Out2 output/analog input to 10-bit ADC input A4/I/O of positive reference voltage terminal                 |
| P2.5/R <sub>OSC</sub>                                | 3       | 32         | I/O | General-purpose digital I/O pin/Input for external resistor that defines the DCO nominal frequency                                                           |
| P3.0/STE0/A5                                         | 11      | 9          | I/O | General-purpose digital I/O pin/slave transmit enable—USART0/SPI mode/analog input to 10-bit ADC input A5                                                    |
| P3.1/SIM00                                           | 12      | 10         | I/O | General-purpose digital I/O pin/slave in/master out of USART0/SPI mode                                                                                       |
| P3.2/SOMI0                                           | 13      | 11         | I/O | General-purpose digital I/O pin/slave out/master in of USART0/SPI mode                                                                                       |
| P3.3/UCLK0                                           | 14      | 12         | I/O | General-purpose digital I/O pin/external clock input—USART0/UART or SPI mode, clock output—USART0/SPI mode clock input                                       |
| P3.4/UTXD0                                           | 15      | 13         | I/O | General-purpose digital I/O pin/transmit data out—USART0/UART mode                                                                                           |
| P3.5/URXD0                                           | 16      | 14         | I/O | General-purpose digital I/O pin/receive data in—USART0/UART mode                                                                                             |
| P3.6/A6                                              | 17      | 15         | I/O | General-purpose digital I/O pin/analog input to 10-bit ADC input A6                                                                                          |
| P3.7/A7                                              | 18      | 16         | I/O | General-purpose digital I/O pin/analog input to 10-bit ADC input A7                                                                                          |
| RST/NMI                                              | 7       | 5          | I   | Reset or nonmaskable interrupt input                                                                                                                         |
| TEST                                                 | 1       | 29         | I   | Selects test mode for JTAG pins on P1.x                                                                                                                      |
| V <sub>CC</sub>                                      | 2       | 30         |     | Supply voltage                                                                                                                                               |
| V <sub>SS</sub>                                      | 4       | 1          |     | Ground reference                                                                                                                                             |
| XIN                                                  | 6       | 3          | I   | Input terminal of crystal oscillator                                                                                                                         |
| XOUT                                                 | 5       | 2          | O   | Output terminal of crystal oscillator                                                                                                                        |
| NC                                                   | NA      | 4,17,20,31 |     | Not connected internally. Recommended connection to V <sub>SS</sub> .                                                                                        |
| QFN Pad                                              | NA      |            |     | QFN package pad connection to V <sub>SS</sub> recommended.                                                                                                   |

<sup>†</sup> TDO or TDI is selected via JTAG instruction.



## short-form description

### CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

### instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

**Table 1. Instruction Word Formats**

|                                   |                |                       |
|-----------------------------------|----------------|-----------------------|
| Dual operands, source-destination | e.g. ADD R4,R5 | R4 + R5 ----> R5      |
| Single operands, destination only | e.g. CALL R8   | PC -->(TOS), R8--> PC |
| Relative jump, un/conditional     | e.g. JNE       | Jump-on-equal bit = 0 |

**Table 2. Address Mode Descriptions**

| ADDRESS MODE           | S | D | SYNTAX          | EXAMPLE          | OPERATION                       |
|------------------------|---|---|-----------------|------------------|---------------------------------|
| Register               | ● | ● | MOV Rs,Rd       | MOV R10,R11      | R10 --> R11                     |
| Indexed                | ● | ● | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6)  | M(2+R5)--> M(6+R6)              |
| Symbolic (PC relative) | ● | ● | MOV EDE,TONI    |                  | M(EDC)--> M(TONI)               |
| Absolute               | ● | ● | MOV &MEM,&TCDAT |                  | M(MEM)--> M(TCDAT)              |
| Indirect               | ● |   | MOV @Rn,Y(Rm)   | MOV @R10,Tab(R6) | M(R10)--> M(Tab+R6)             |
| Indirect autoincrement | ● |   | MOV @Rn+,Rm     | MOV @R10+,R11    | M(R10)--> R11<br>R10 + 2--> R10 |
| Immediate              | ● |   | MOV #X,TONI     | MOV #45,TONI     | #45 --> M(TONI)                 |

NOTE: S = source D = destination

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## operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled  
ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1);
  - CPU is disabled  
ACLK and SMCLK remain active. MCLK is disabled  
DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2);
  - CPU is disabled  
MCLK and SMCLK are disabled  
DCO's dc-generator remains enabled  
ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled  
MCLK and SMCLK are disabled  
DCO's dc-generator is disabled  
ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled  
ACLK is disabled  
MCLK and SMCLK are disabled  
DCO's dc-generator is disabled  
Crystal oscillator is stopped

## interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh-0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

| INTERRUPT SOURCE                                         | INTERRUPT FLAG                                                                         | SYSTEM INTERRUPT                                   | WORD ADDRESS | PRIORITY    |
|----------------------------------------------------------|----------------------------------------------------------------------------------------|----------------------------------------------------|--------------|-------------|
| Power-up<br>External reset<br>Watchdog<br>Flash memory   | WDTIFG (see Note1)<br>KEYV (see Note 1)                                                | Reset                                              | 0FFFEh       | 15, highest |
| NMI<br>Oscillator fault<br>Flash memory access violation | NMIIFG (see Notes 1 and 4)<br>OFIFG (see Notes 1 and 4)<br>ACCVIFG (see Notes 1 and 4) | (Non)-maskable<br>(Non)-maskable<br>(Non)-maskable | 0FFFCh       | 14          |
|                                                          |                                                                                        |                                                    | 0FFFAh       | 13          |
|                                                          |                                                                                        |                                                    | 0FFF8h       | 12          |
|                                                          |                                                                                        |                                                    | 0FFF6h       | 11          |
| Watchdog timer                                           | WDTIFG                                                                                 | Maskable                                           | 0FFF4h       | 10          |
| Timer_A3                                                 | TACCR0 CCIFG (see Note 2)                                                              | Maskable                                           | 0FFF2h       | 9           |
| Timer_A3                                                 | TACCR1 and TACCR2<br>CCIFGs, TAIFG<br>(see Notes 1 and 2)                              | Maskable                                           | 0FFF0h       | 8           |
| USART0 receive (see Note 5)                              | URXIFG0                                                                                | Maskable                                           | 0FFEEh       | 7           |
| USART0 transmit (see Note 5)                             | UTXIFG0                                                                                | Maskable                                           | 0FFECCh      | 6           |
| ADC10                                                    | ADC10IFG                                                                               | Maskable                                           | 0FFEAh       | 5           |
|                                                          |                                                                                        |                                                    | 0FFE8h       | 4           |
| I/O Port P2<br>(eight flags – see Note 3)                | P2IFG.0 to P2IFG.7<br>(see Notes 1 and 2)                                              | Maskable                                           | 0FFE6h       | 3           |
| I/O Port P1<br>(eight flags)                             | P1IFG.0 to P1IFG.7<br>(see Notes 1 and 2)                                              | Maskable                                           | 0FFE4h       | 2           |
|                                                          |                                                                                        |                                                    | 0FFE2h       | 1           |
|                                                          |                                                                                        |                                                    | 0FFE0h       | 0, lowest   |

- NOTES: 1. Multiple source flags  
2. Interrupt flags are located in the module  
3. There are eight Port P2 interrupt flags, but only six Port P2 I/O pins (P2.0–5) are implemented on the '11x2 and '12x2 devices.  
4. (Non)-maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable cannot.  
5. USART0 is implemented in MSP430x12x2 devices only.

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## special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

### interrupt enable 1 and 2

| Address | 7 | 6 | 5      | 4     | 3 | 2 | 1    | 0     |
|---------|---|---|--------|-------|---|---|------|-------|
| 0h      |   |   | ACCVIE | NMIIE |   |   | OFIE | WDTIE |
|         |   |   | rw-0   | rw-0  |   |   | rw-0 | rw-0  |

WDTIE: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.

OFIE: Oscillator fault enable

NMIIE: (Non)maskable interrupt enable

ACCVIE: Flash access violation interrupt enable

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1      | 0      |
|---------|---|---|---|---|---|---|--------|--------|
| 01h     |   |   |   |   |   |   | UTXIE0 | URXIE0 |
|         |   |   |   |   |   |   | rw-0   | rw-0   |

URXIE0: USART0: UART and SPI receive-interrupt enable (MSP430x12x2 devices only)

UTXIE0: USART0: UART and SPI transmit-interrupt enable (MSP430x12x2 devices only)

### interrupt flag register 1 and 2

| Address | 7 | 6 | 5 | 4      | 3 | 2 | 1     | 0      |
|---------|---|---|---|--------|---|---|-------|--------|
| 02h     |   |   |   | NMIIFG |   |   | OFIFG | WDTIFG |
|         |   |   |   | rw-0   |   |   | rw-1  | rw-(0) |

WDTIFG: Set on Watchdog Timer overflow (in watchdog mode) or security key violation.  
Reset on  $V_{CC}$  power-up or a reset condition at  $\overline{RST}/NMI$  pin in reset mode.

OFIFG: Flag set on oscillator fault

NMIIFG: Set via  $\overline{RST}/NMI$ -pin

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1       | 0       |
|---------|---|---|---|---|---|---|---------|---------|
| 03h     |   |   |   |   |   |   | UTXIFG0 | URXIFG0 |
|         |   |   |   |   |   |   | rw-1    | rw-0    |

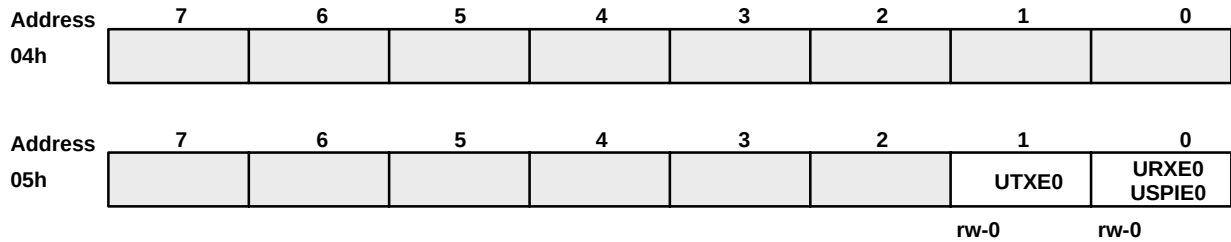
URXIFG0: USART0: UART and SPI receive flag (MSP430x12x2 devices only)

UTXIFG0: USART0: UART and SPI transmit flag (MSP430x12x2 devices only)



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## module enable registers 1 and 2



URXE0: USART0: UART mode receive enable (MSP430x12x2 devices only)  
 UTXE0: USART0: UART mode transmit enable (MSP430x12x2 devices only)  
 USPIE0: USART0: SPI mode transmit and receive enable (MSP430x12x2 devices only)

**Legend**    **rw:** Bit can be read and written.  
               **rw-0,1:** Bit can be read and written. It is Reset or Set by PUC  
               **rw-(0,1):** Bit can be read and written. It is Reset or Set by POR  
                SFR bit is not present in device.

## memory organization

|                        |           | MSP430F1122     | MSP430F1132     | MSP430F1222     | MSP430F1232     |
|------------------------|-----------|-----------------|-----------------|-----------------|-----------------|
| Memory                 | Size      | 4KB Flash       | 8KB Flash       | 4KB Flash       | 8KB Flash       |
|                        | Flash     | 0FFFFh–0FFE0h   | 0FFFFh–0FFE0h   | 0FFFFh–0FFE0h   | 0FFFFh–0FFE0h   |
| Main: interrupt vector | Flash     | 0FFFFh–0F000h   | 0FFFFh–0E000h   | 0FFFFh–0F000h   | 0FFFFh–0E000h   |
| Main: code memory      | Flash     | 0FFFFh–0F000h   | 0FFFFh–0E000h   | 0FFFFh–0F000h   | 0FFFFh–0E000h   |
| Information memory     | Size      | 256 Byte        | 256 Byte        | 256 Byte        | 256 Byte        |
|                        | Flash     | 010FFh – 01000h | 010FFh – 01000h | 010FFh – 01000h | 010FFh – 01000h |
| Boot memory            | Size      | 1KB             | 1KB             | 1KB             | 1KB             |
|                        | ROM       | 0FFFh – 0C00h   | 0FFFh – 0C00h   | 0FFFh – 0C00h   | 0FFFh – 0C00h   |
| RAM                    | Size      | 256 Byte        | 256 Byte        | 256 Byte        | 256 Byte        |
|                        |           | 02FFh – 0200h   | 02FFh – 0200h   | 02FFh – 0200h   | 02FFh – 0200h   |
| Peripherals            | 16-bit    | 01FFh – 0100h   | 01FFh – 0100h   | 01FFh – 0100h   | 01FFh – 0100h   |
|                        | 8-bit     | 0FFh – 010h     | 0FFh – 010h     | 0FFh – 010h     | 0FFh – 010h     |
|                        | 8-bit SFR | 0Fh – 00h       | 0Fh – 00h       | 0Fh – 00h       | 0Fh – 00h       |

## bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

| BSL Function  | MSP430x11x2<br>DW & PW Package<br>(20 Pins) | MSP430x12x2<br>DW & PW Package<br>(28 Pins) | MSP430x11x2/12x2<br>RHB Package<br>(32 Pins) |
|---------------|---------------------------------------------|---------------------------------------------|----------------------------------------------|
| Data Transmit | 14 - P1.1                                   | 22 - P1.1                                   | 22 - P1.1                                    |
| Data Receive  | 10 - P2.2                                   | 10 - P2.2                                   | 8 - P2.2                                     |

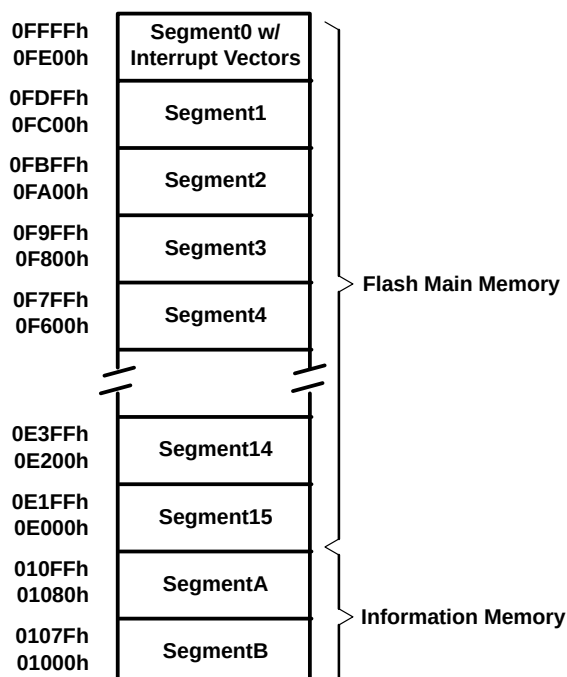
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## flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



NOTE: All segments not implemented on all devices.

## peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, see the *MSP430x1xx Family User's Guide*, literature number SLAU049.

## oscillator and system clock

The clock system in the MSP430x11x2 and MSP430x12x2 devices is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6  $\mu$ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

## digital I/O

There are 3 8-bit I/O ports implemented—ports P1, P2, and P3 (only six port P2 I/O signals are available on external pins; port P3 is implemented only on 'x12x2 devices):

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and six bits of port P2.
- Read/write access to port-control registers is supported by all instructions.

### NOTE:

Six bits of port P2, P2.0 to P2.5, are available on external pins, but all control and data bits for port P2 are implemented. Port P3 has no interrupt capability. Port P3 is implemented in MSP430x12x2 only.

## brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

## watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

## USART0 (MSP430x12x2 Only)

The MSP430x12x2 devices have one hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

## ADC10

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling allowing ADC samples to be converted and stored without any CPU intervention.

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## timer\_A3

Timer\_A3 is a 16-bit timer/counter with three capture/compare registers. Timer\_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| Timer_A3 Signal Connections |              |                   |                     |                   |              |                      |                   |              |                   |
|-----------------------------|--------------|-------------------|---------------------|-------------------|--------------|----------------------|-------------------|--------------|-------------------|
| Input Pin Number            |              |                   | Device Input Signal | Module Input Name | Module Block | Module Output Signal | Output Pin Number |              |                   |
| DW and PW                   |              | RHB               |                     |                   |              |                      | DW and PW         |              | RHB               |
| '11x2 20-Pin                | '12x2 28-Pin | '11x2/12x2 32-Pin |                     |                   |              |                      | '11x2 20-Pin      | '12x2 28-Pin | '11x2/12x2 32-Pin |
| 13 - P1.0                   | 21 - P1.0    | 21 - P1.0         | TACLK               | TACLK             | Timer        | NA                   |                   |              |                   |
|                             |              |                   | ACLK                | ACLK              |              |                      |                   |              |                   |
|                             |              |                   | SMCLK               | SMCLK             |              |                      |                   |              |                   |
| 9 - P2.1                    | 9 - P2.1     | 7 - P2.1          | INCLK               | INCLK             |              |                      |                   |              |                   |
| 14 - P1.1                   | 22 - P1.1    | 22 - P1.1         | TA0                 | CCI0A             | CCR0         | TA0                  | 14 - P1.1         | 22 - P1.1    | 22 - P1.1         |
| 10 - P2.2                   | 10 - P2.2    | 8 - P2.2          | TA0                 | CCI0B             |              |                      | 18 - P1.5         | 26 - P1.5    | 26 - P1.5         |
|                             |              |                   | DV <sub>SS</sub>    | GND               |              |                      | 10 - P2.2         | 10 - P2.2    | 8 - P2.2          |
|                             |              |                   | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      | ADC10 Internal    |              |                   |
| 15 - P1.2                   | 23 - P1.2    | 23 - P1.2         | TA1                 | CCI1A             | CCR1         | TA1                  | 15 - P1.2         | 23 - P1.2    | 23 - P1.2         |
| 11 - P2.3                   | 19 - P2.3    | 18 - P2.3         | TA1                 | CCI1B             |              |                      | 19 - P1.6         | 27 - P1.6    | 27 - P1.6         |
|                             |              |                   | DV <sub>SS</sub>    | GND               |              |                      | 11 - P2.3         | 19 - P2.3    | 18 - P2.3         |
|                             |              |                   | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      | ADC10 Internal    |              |                   |
| 16 - P1.3                   | 24 - P1.3    | 24 - P1.3         | TA2                 | CCI2A             | CCR2         | TA2                  | 16 - P1.3         | 24 - P1.3    | 24 - P1.3         |
|                             |              |                   | ACLK (internal)     | CCI2B             |              |                      | 20 - P1.7         | 28 - P1.7    | 28 - P1.7         |
|                             |              |                   | DV <sub>SS</sub>    | GND               |              |                      | 12 - P2.4         | 20 - P2.4    | 19 - P2.4         |
|                             |              |                   | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      | ADC10 Internal    |              |                   |

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## peripheral file map

| PERIPHERALS WITH WORD ACCESS            |                                      |           |       |
|-----------------------------------------|--------------------------------------|-----------|-------|
| <b>ADC10</b>                            | ADC data transfer start address      | ADC10SA   | 1BCh  |
|                                         | ADC memory                           | ADC10MEM  | 1B4h  |
|                                         | ADC control register 1               | ADC10CTL1 | 1B2h  |
|                                         | ADC control register 0               | ADC10CTL0 | 1B0h  |
|                                         | ADC analog enable                    | ADC10AE   | 04Ah  |
|                                         | ADC data transfer control register 1 | ADC10DTC1 | 049h  |
|                                         | ADC data transfer control register 0 | ADC10DTC0 | 048h  |
| <b>Timer_A</b>                          | Reserved                             |           | 017Eh |
|                                         | Reserved                             |           | 017Ch |
|                                         | Reserved                             |           | 017Ah |
|                                         | Reserved                             |           | 0178h |
|                                         | Capture/compare register             | TACCR2    | 0176h |
|                                         | Capture/compare register             | TACCR1    | 0174h |
|                                         | Capture/compare register             | TACCR0    | 0172h |
|                                         | Timer_A register                     | TAR       | 0170h |
|                                         | Reserved                             |           | 016Eh |
|                                         | Reserved                             |           | 016Ch |
|                                         | Reserved                             |           | 016Ah |
|                                         | Reserved                             |           | 0168h |
|                                         | Capture/compare control              | TACCTL2   | 0166h |
|                                         | Capture/compare control              | TACCTL1   | 0164h |
|                                         | Capture/compare control              | TACCTL0   | 0162h |
| <b>Flash Memory</b>                     | Flash control 3                      | FCTL3     | 012Ch |
|                                         | Flash control 2                      | FCTL2     | 012Ah |
|                                         | Flash control 1                      | FCTL1     | 0128h |
| <b>Watchdog</b>                         | Watchdog/timer control               | WDTCTL    | 0120h |
| PERIPHERALS WITH BYTE ACCESS            |                                      |           |       |
| <b>USART0<br/>(in MSP430x12x2 only)</b> | Transmit buffer                      | U0TXBUF   | 077h  |
|                                         | Receive buffer                       | U0RXBUF   | 076h  |
|                                         | Baud rate                            | U0BR1     | 075h  |
|                                         | Baud rate                            | U0BR0     | 074h  |
|                                         | Modulation control                   | U0MCTL    | 073h  |
|                                         | Receive control                      | U0RCTL    | 072h  |
|                                         | Transmit control                     | U0TCTL    | 071h  |
|                                         | USART control                        | U0CTL     | 070h  |
| <b>Basic Clock</b>                      | Basic clock sys. control2            | BCSCTL2   | 058h  |
|                                         | Basic clock sys. control1            | BCSCTL1   | 057h  |
|                                         | DCO clock freq. control              | DCOCTL    | 056h  |
| <b>Port P2</b>                          | Port P2 selection                    | P2SEL     | 02Eh  |
|                                         | Port P2 interrupt enable             | P2IE      | 02Dh  |
|                                         | Port P2 interrupt edge select        | P2IES     | 02Ch  |
|                                         | Port P2 interrupt flag               | P2IFG     | 02Bh  |
|                                         | Port P2 direction                    | P2DIR     | 02Ah  |
|                                         | Port P2 output                       | P2OUT     | 029h  |
|                                         | Port P2 input                        | P2IN      | 028h  |
| <b>Port P1</b>                          | Port P1 selection                    | P1SEL     | 026h  |
|                                         | Port P1 interrupt enable             | P1IE      | 025h  |
|                                         | Port P1 interrupt edge select        | P1IES     | 024h  |
|                                         | Port P1 interrupt flag               | P1IFG     | 023h  |
|                                         | Port P1 direction                    | P1DIR     | 022h  |
|                                         | Port P1 output                       | P1OUT     | 021h  |
|                                         | Port P1 input                        | P1IN      | 020h  |



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## peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS (CONTINUED) |                       |       |      |
|------------------------------------------|-----------------------|-------|------|
| <b>Port P3</b><br>(in MSP430x12x2 only)  | Port P3 selection     | P3SEL | 01Bh |
|                                          | Port P3 direction     | P3DIR | 01Ah |
|                                          | Port P3 output        | P3OUT | 019h |
|                                          | Port P3 input         | P3IN  | 018h |
| <b>Special Function</b>                  | Module enable2        | ME2   | 005h |
|                                          | Module enable1        | ME1   | 004h |
|                                          | SFR interrupt flag2   | IFG2  | 003h |
|                                          | SFR interrupt flag1   | IFG1  | 002h |
|                                          | SFR interrupt enable2 | IE2   | 001h |
|                                          | SFR interrupt enable1 | IE1   | 000h |

## absolute maximum ratings<sup>†</sup>

|                                                      |                            |
|------------------------------------------------------|----------------------------|
| Voltage applied at $V_{CC}$ to $V_{SS}$              | –0.3 V to 4.1 V            |
| Voltage applied to any pin (see Note)                | –0.3 V to $V_{CC} + 0.3$ V |
| Diode current at any device terminal                 | $\pm 2$ mA                 |
| Storage temperature, $T_{stg}$ (unprogrammed device) | –55°C to 150°C             |
| Storage temperature, $T_{stg}$ (programmed device)   | –40°C to 85°C              |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to  $V_{SS}$ . The JTAG fuse-blow voltage,  $V_{FB}$ , is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

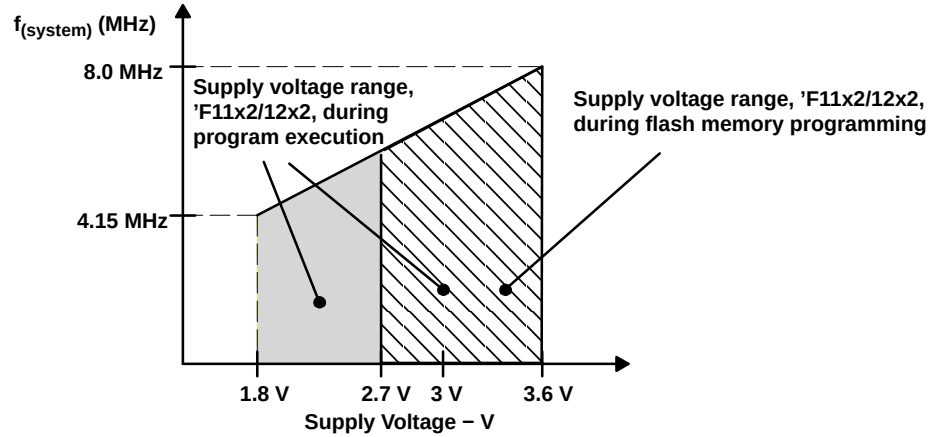
## recommended operating conditions

|                                                                        |                          |                                                        | MIN    | NOM | MAX  | UNITS |
|------------------------------------------------------------------------|--------------------------|--------------------------------------------------------|--------|-----|------|-------|
| Supply voltage during program execution, V <sub>CC</sub> (see Note 1)  |                          | MSP430F11x2                                            | 1.8    |     | 3.6  | V     |
| Supply voltage during program/erase flash memory, V <sub>CC</sub>      |                          | MSP430F12x2                                            | 2.7    |     | 3.6  | V     |
| Supply voltage, V <sub>SS</sub>                                        |                          |                                                        | 0      |     |      | V     |
| Operating free-air temperature range, T <sub>A</sub>                   |                          | MSP430F11x2<br>MSP430F12x2                             | −40    |     | 85   | °C    |
| LFXT1 crystal frequency, f <sub>(LFXT1)</sub><br>(see Note 1 & Note 2) | LF mode selected, XTS=0  | Watch crystal                                          | 32 768 |     |      | Hz    |
|                                                                        | XT1 selected mode, XTS=1 | Ceramic resonator                                      | 450    |     | 8000 | kHz   |
|                                                                        |                          | Crystal                                                | 1000   |     | 8000 |       |
| Processor frequency f <sub>(system)</sub> (MCLK signal)                |                          | V <sub>CC</sub> = 1.8 V,<br>MSP430F11x2<br>MSP430F12x2 | dc     |     | 4.15 | MHz   |
|                                                                        |                          | V <sub>CC</sub> = 3.6 V,<br>MSP430F11x2<br>MSP430F12x2 | dc     |     | 8    |       |

NOTES: 1. The LFXT1 oscillator in LF-mode requires a resistor of 5.1 M $\Omega$  from XOUT to  $V_{SS}$  when  $V_{CC} < 2.5$  V.  
The LFXT1 oscillator in XT1-mode accepts a ceramic resonator or a crystal frequency of 4 MHz at  $V_{CC} \geq 2.2$  V.  
The LFXT1 oscillator in XT1-mode accepts a ceramic resonator or a crystal frequency of 8 MHz at  $V_{CC} \geq 2.8$  V.  
2. The LFXT1 oscillator in LF-mode requires a watch crystal.  
The LFXT1 oscillator in XT1-mode accepts a ceramic resonator or a crystal.



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum  $V_{CC}$  of 2.7 V.

**Figure 1. Frequency vs Supply Voltage**

supply current (into  $V_{CC}$ ) excluding external current

| PARAMETER                             | TEST CONDITIONS                                                                                                                                                     | MIN                                | TYP | MAX | UNIT          |
|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|-----|-----|---------------|
| $I_{(AM)}$ Active mode                | $T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$ ,<br>$f_{(MCLK)} = f_{(SMCLK)} = 1\text{ MHz}$ ,<br>$f_{(ACLK)} = 32,768\text{ Hz}$ ,<br>Program executes in Flash | $V_{CC} = 2.2\text{ V}$            | 200 | 250 | $\mu\text{A}$ |
|                                       |                                                                                                                                                                     | $V_{CC} = 3\text{ V}$              | 300 | 350 |               |
|                                       | $T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$ ,<br>$f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)} = 4096\text{ Hz}$ ,<br>Program executes in Flash                       | $V_{CC} = 2.2\text{ V}$            | 3   | 5   | $\mu\text{A}$ |
|                                       |                                                                                                                                                                     | $V_{CC} = 3\text{ V}$              | 11  | 18  |               |
| $I_{(CPUOff)}$ Low-power mode, (LPM0) | $T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$ ,<br>$f_{(MCLK)} = 0$ , $f_{(SMCLK)} = 1\text{ MHz}$ ,<br>$f_{(ACLK)} = 32,768\text{ Hz}$                          | $V_{CC} = 2.2\text{ V}$            | 32  | 45  | $\mu\text{A}$ |
|                                       |                                                                                                                                                                     | $V_{CC} = 3\text{ V}$              | 55  | 70  |               |
| $I_{(LPM2)}$ Low-power mode, (LPM2)   | $T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$ ,<br>$f_{(MCLK)} = f_{(SMCLK)} = 0\text{ MHz}$ ,<br>$f_{(ACLK)} = 32,768\text{ Hz}$ , $SCG0 = 0$                   | $V_{CC} = 2.2\text{ V}$            | 11  | 14  | $\mu\text{A}$ |
|                                       |                                                                                                                                                                     | $V_{CC} = 3\text{ V}$              | 17  | 22  |               |
| $I_{(LPM3)}$ Low-power mode, (LPM3)   | $T_A = -40^{\circ}\text{C}$                                                                                                                                         | $V_{CC} = 2.2\text{ V}$            | 0.8 | 1.2 | $\mu\text{A}$ |
|                                       | $T_A = 25^{\circ}\text{C}$                                                                                                                                          |                                    | 0.7 | 1   |               |
|                                       | $T_A = 85^{\circ}\text{C}$                                                                                                                                          |                                    | 1.6 | 2.3 |               |
|                                       | $T_A = -40^{\circ}\text{C}$                                                                                                                                         | $V_{CC} = 3\text{ V}$              | 1.8 | 2.2 | $\mu\text{A}$ |
|                                       | $T_A = 25^{\circ}\text{C}$                                                                                                                                          |                                    | 1.6 | 1.9 |               |
|                                       | $T_A = 85^{\circ}\text{C}$                                                                                                                                          |                                    | 2.3 | 3.4 |               |
| $I_{(LPM4)}$ Low-power mode, (LPM4)   | $T_A = -40^{\circ}\text{C}$                                                                                                                                         | $V_{CC} = 2.2\text{ V}/3\text{ V}$ | 0.1 | 0.5 | $\mu\text{A}$ |
|                                       | $T_A = 25^{\circ}\text{C}$                                                                                                                                          |                                    | 0.1 | 0.5 |               |
|                                       | $T_A = 85^{\circ}\text{C}$                                                                                                                                          |                                    | 0.8 | 1.9 |               |

NOTES: 1. All inputs are tied to 0 V or  $V_{CC}$ . Outputs do not source or sink any current.

current consumption of active mode versus system frequency

$$I_{AM} = I_{AM[1\text{ MHz}]} \times f_{\text{system}} [\text{MHz}]$$

current consumption of active mode versus supply voltage

$$I_{AM} = I_{AM[3\text{ V}]} + 120\text{ }\mu\text{A/V} \times (V_{CC} - 3\text{ V})$$

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

## Schmitt-trigger inputs Port P1 to Port P3; P1.0 to P1.7, P2.0 to P2.5, P3.0 to P3.7

| PARAMETER                                                   | TEST CONDITIONS         | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------------|-------------------------|-----|-----|-----|------|
| $V_{IT+}$ Positive-going input threshold voltage            | $V_{CC} = 2.2\text{ V}$ | 1.1 |     | 1.5 | V    |
|                                                             | $V_{CC} = 3\text{ V}$   | 1.5 |     | 1.9 |      |
| $V_{IT-}$ Negative-going input threshold voltage            | $V_{CC} = 2.2\text{ V}$ | 0.4 |     | 0.9 | V    |
|                                                             | $V_{CC} = 3\text{ V}$   | 0.9 |     | 1.3 |      |
| $V_{hys}$ Input voltage hysteresis, ( $V_{IT+} - V_{IT-}$ ) | $V_{CC} = 2.2\text{ V}$ | 0.3 |     | 1.1 | V    |
|                                                             | $V_{CC} = 3\text{ V}$   | 0.5 |     | 1   |      |

## standard inputs – $\overline{RST}/NMI$ , TEST; JTAG: TCK, TMS, TDI/TCLK

| PARAMETER                         | TEST CONDITIONS                      | MIN                 | TYP | MAX          | UNIT |
|-----------------------------------|--------------------------------------|---------------------|-----|--------------|------|
| $V_{IL}$ Low-level input voltage  | $V_{CC} = 2.2\text{ V} / 3\text{ V}$ | $V_{SS}$            |     | $V_{SS}+0.6$ | V    |
| $V_{IH}$ High-level input voltage |                                      | $0.8 \times V_{CC}$ |     | $V_{CC}$     | V    |

## inputs Px.x, TAx

| PARAMETER                                                       | TEST CONDITIONS                                                                         | $V_{CC}$  | MIN | TYP | MAX | UNIT  |
|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|-----------|-----|-----|-----|-------|
| $t_{(int)}$ External interrupt timing                           | Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag, (see Note 1) | 2.2 V/3 V | 1.5 |     |     | cycle |
|                                                                 |                                                                                         | 2.2 V     | 62  |     |     | ns    |
|                                                                 |                                                                                         | 3 V       | 50  |     |     |       |
| $t_{(cap)}$ Timer_A, capture timing                             | TA0, TA1, TA2                                                                           | 2.2 V     | 62  |     |     | ns    |
|                                                                 |                                                                                         | 3 V       | 50  |     |     |       |
| $f_{(TAext)}$ Timer_A clock frequency externally applied to pin | TACLK, INCLK $t_{(H)} = t_{(L)}$                                                        | 2.2 V     |     |     | 8   | MHz   |
|                                                                 |                                                                                         | 3 V       |     |     | 10  |       |
| $f_{(TAint)}$ Timer_A clock frequency                           | SMCLK or ACLK signal selected                                                           | 2.2 V     |     |     | 8   | MHz   |
|                                                                 |                                                                                         | 3 V       |     |     | 10  |       |

NOTES: 1. The external signal sets the interrupt flag every time the minimum  $t_{(int)}$  cycle and time parameters are met. It may be set even with trigger signals shorter than  $t_{(int)}$ . Both the cycle and timing specifications must be met to ensure the flag is set.  $t_{(int)}$  is measured in MCLK cycles.

## leakage current

| PARAMETER                                      | TEST CONDITIONS                                      | $V_{CC}$  | MIN | TYP | MAX      | UNIT |
|------------------------------------------------|------------------------------------------------------|-----------|-----|-----|----------|------|
| $I_{lkg}(Px.x)$ High-impedance leakage current | Port P1: P1.x, $0 \leq x \leq 7$ (see Notes 1 and 2) | 2.2 V/3 V |     |     | $\pm 50$ | nA   |
|                                                | Port P2: P2.x, $0 \leq x \leq 5$ (see Notes 1 and 2) | 2.2 V/3 V |     |     | $\pm 50$ |      |

NOTES: 1. The leakage current is measured with  $V_{SS}$  or  $V_{CC}$  applied to the corresponding pin(s), unless otherwise noted.  
2. The leakage of the digital port pins is measured individually. The port pin must be selected for input and there must be no optional pullup or pulldown resistor.



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs Port 1 to Port 3; P1.0 to P1.7, P2.0 to P2.5, P3.0 to P3.7

| PARAMETER                          | TEST CONDITIONS                 |                          |            | MIN           | TYP | MAX           | UNIT |
|------------------------------------|---------------------------------|--------------------------|------------|---------------|-----|---------------|------|
| $V_{OH}$ High-level output voltage | $I_{OH(max)} = -1.5 \text{ mA}$ | $V_{CC} = 2.2 \text{ V}$ | See Note 1 | $V_{CC}-0.25$ |     | $V_{CC}$      | V    |
|                                    | $I_{OH(max)} = -6 \text{ mA}$   |                          | See Note 2 | $V_{CC}-0.6$  |     | $V_{CC}$      |      |
|                                    | $I_{OH(max)} = -1.5 \text{ mA}$ | $V_{CC} = 3 \text{ V}$   | See Note 1 | $V_{CC}-0.25$ |     | $V_{CC}$      |      |
|                                    | $I_{OH(max)} = -6 \text{ mA}$   |                          | See Note 2 | $V_{CC}-0.6$  |     | $V_{CC}$      |      |
| $V_{OL}$ Low-level output voltage  | $I_{OL(max)} = 1.5 \text{ mA}$  | $V_{CC} = 2.2 \text{ V}$ | See Note 1 | $V_{SS}$      |     | $V_{SS}+0.25$ | V    |
|                                    | $I_{OL(max)} = 6 \text{ mA}$    |                          | See Note 2 | $V_{SS}$      |     | $V_{SS}+0.6$  |      |
|                                    | $I_{OL(max)} = 1.5 \text{ mA}$  | $V_{CC} = 3 \text{ V}$   | See Note 1 | $V_{SS}$      |     | $V_{SS}+0.25$ |      |
|                                    | $I_{OL(max)} = 6 \text{ mA}$    |                          | See Note 2 | $V_{SS}$      |     | $V_{SS}+0.6$  |      |

NOTES: 1. The maximum total current,  $I_{OH(max)}$  and  $I_{OL(max)}$ , for all outputs combined, should not exceed  $\pm 12 \text{ mA}$  to hold the maximum voltage drop specified.  
2. The maximum total current,  $I_{OH(max)}$  and  $I_{OL(max)}$ , for all outputs combined, should not exceed  $\pm 48 \text{ mA}$  to hold the maximum voltage drop specified.

outputs P1.x, P2.x, P3.x, TAx

| PARAMETER    | TEST CONDITIONS             |                                                                                                    | $V_{CC}$                          | MIN       | TYP | MAX          | UNIT |
|--------------|-----------------------------|----------------------------------------------------------------------------------------------------|-----------------------------------|-----------|-----|--------------|------|
| $f_{(P20)}$  | Output frequency            | P2.0/ACLK, $C_L = 20 \text{ pF}$                                                                   | 2.2 V/3 V                         |           |     | $f_{System}$ | MHz  |
| $f_{(TAX)}$  |                             | TA0, TA1, TA2, $C_L = 20 \text{ pF}$ ,<br>Internal clock source, SMCLK signal applied (see Note 1) | 2.2 V/3 V                         | dc        |     | $f_{System}$ |      |
| $t_{(Xdc)}$  | Duty cycle of O/P frequency | P1.4/SMCLK,<br>$C_L = 20 \text{ pF}$                                                               | $f_{SMCLK} = f_{LFXT1} = f_{XT1}$ | 2.2 V/3 V |     | 40%          | 60%  |
|              |                             |                                                                                                    | $f_{SMCLK} = f_{LFXT1} = f_{LF}$  |           |     | 35%          |      |
|              |                             |                                                                                                    | $f_{SMCLK} = f_{LFXT1/n}$         |           |     | 50%–15 ns    |      |
|              |                             |                                                                                                    | $f_{SMCLK} = f_{DCOCLK}$          |           |     | 50%–15 ns    |      |
|              |                             | P2.0/ACLK,<br>$C_L = 20 \text{ pF}$                                                                | $f_{P20} = f_{LFXT1} = f_{XT1}$   | 2.2 V/3 V |     | 40%          | 60%  |
|              |                             |                                                                                                    | $f_{P20} = f_{LFXT1} = f_{LF}$    |           |     | 30%          |      |
|              |                             |                                                                                                    | $f_{P20} = f_{LFXT1/n}$           |           |     | 50%          |      |
|              |                             |                                                                                                    |                                   |           |     |              |      |
| $t_{(TAdc)}$ |                             | TA0, TA1, TA2, $C_L = 20 \text{ pF}$ , Duty cycle = 50%                                            | 2.2 V/3 V                         |           | 0   | $\pm 50$     | ns   |

NOTES: 1. The limits of the system clock MCLK has to be met. MCLK and SMCLK can have different frequencies.

# MSP430x11x2, MSP430x12x2 MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, and P3 (see Note)

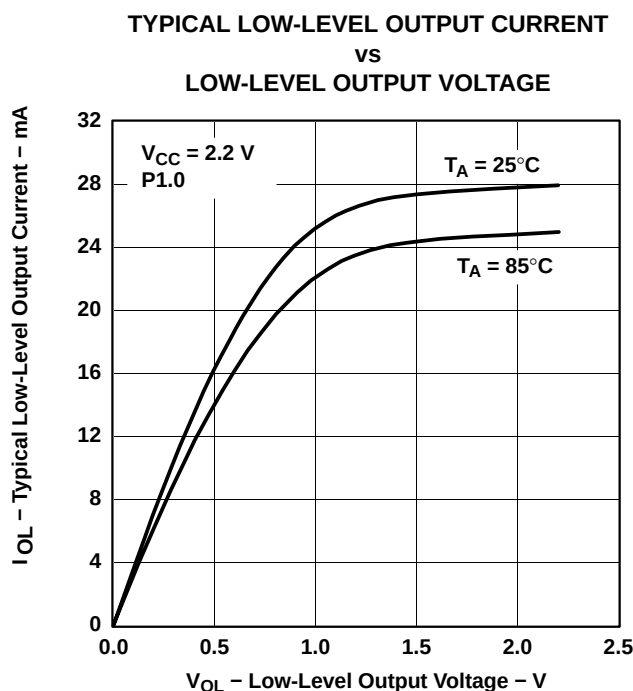


Figure 2

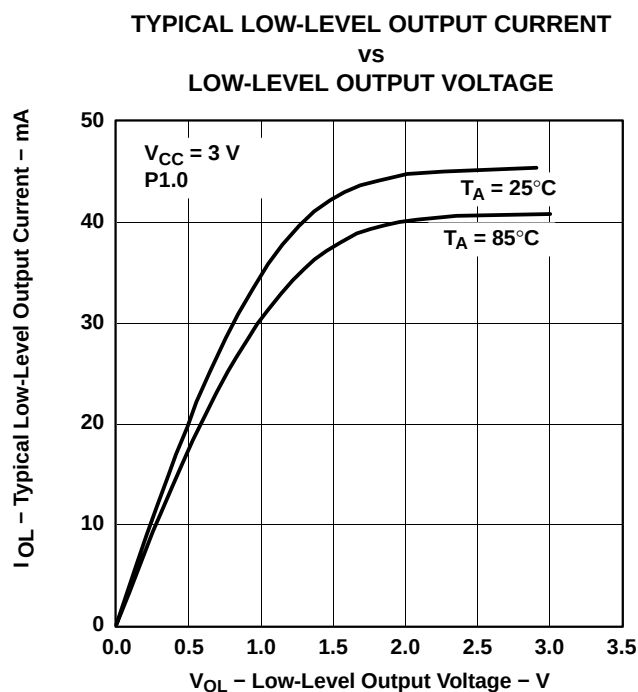


Figure 3

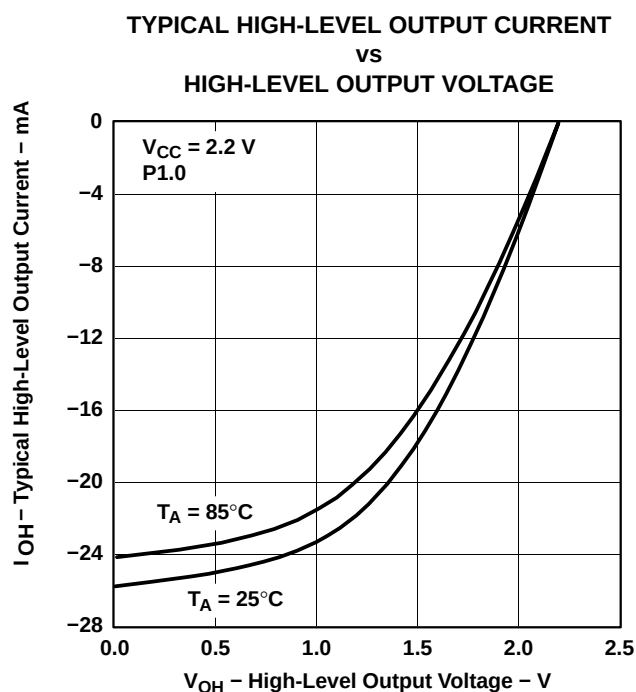


Figure 4

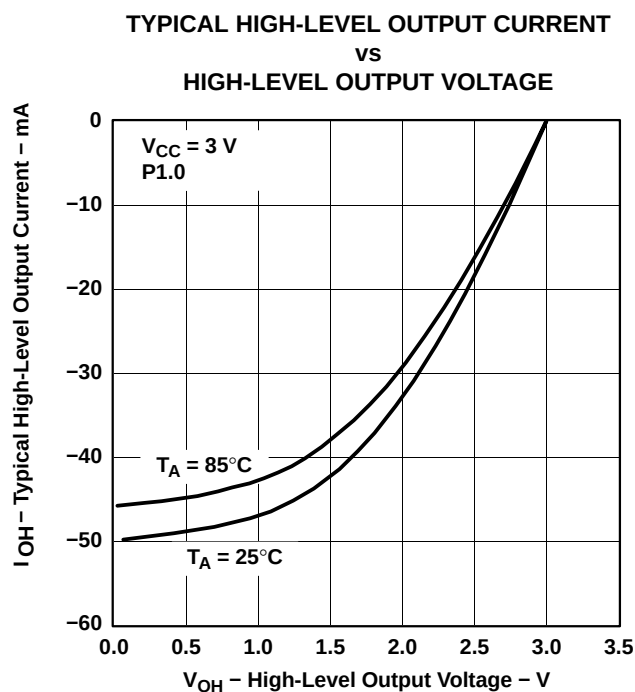


Figure 5

NOTE: Only one output is loaded at a time.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**wake-up from lower power modes (LPMx)**

| PARAMETER |                         | TEST CONDITIONS                                          | MIN | TYP | MAX | UNIT |
|-----------|-------------------------|----------------------------------------------------------|-----|-----|-----|------|
| t(LPM0)   | Delay time (see Note 1) | V <sub>CC</sub> = 2.2 V/3 V                              |     | 100 |     | ns   |
| t(LPM2)   |                         | V <sub>CC</sub> = 2.2 V/3 V                              |     | 100 |     |      |
| t(LPM3)   |                         | f <sub>(MCLK)</sub> = 1 MHz, V <sub>CC</sub> = 2.2 V/3 V |     |     | 6   | μs   |
|           |                         | f <sub>(MCLK)</sub> = 2 MHz, V <sub>CC</sub> = 2.2 V/3 V |     |     | 6   |      |
|           |                         | f <sub>(MCLK)</sub> = 3 MHz, V <sub>CC</sub> = 2.2 V/3 V |     |     | 6   |      |
| t(LPM4)   |                         | f <sub>(MCLK)</sub> = 1 MHz, V <sub>CC</sub> = 2.2 V/3 V |     |     | 6   | μs   |
|           |                         | f <sub>(MCLK)</sub> = 2 MHz, V <sub>CC</sub> = 2.2 V/3 V |     |     | 6   |      |
|           |                         | f <sub>(MCLK)</sub> = 3 MHz, V <sub>CC</sub> = 2.2 V/3 V |     |     | 6   |      |

NOTES: 1. Parameter applicable only if DCOCLK is used for MCLK.

**USART (see Note 1)**

| PARAMETER |                      | TEST CONDITIONS          | MIN | TYP | MAX | UNIT |
|-----------|----------------------|--------------------------|-----|-----|-----|------|
| $t_{(r)}$ | USART: deglitch time | $V_{CC} = 2.2 \text{ V}$ | 200 | 430 | 800 | ns   |
|           |                      | $V_{CC} = 3 \text{ V}$   | 150 | 280 | 500 |      |

NOTES: 1. The signal applied to the USART receive signal/terminal (URXD) should meet the timing requirements of  $t_{(r)}$  to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of  $t_{(r)}$ . The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD line.

**RAM**

| PARAMETER    |                         | MIN | NOM | MAX | UNIT |
|--------------|-------------------------|-----|-----|-----|------|
| $V_{(RAMh)}$ | CPU halted (see Note 1) | 1.6 |     |     | V    |

NOTES: 1. This parameter defines the minimum supply voltage  $V_{CC}$  when the data in the program memory RAM remains unchanged. No program execution should happen during this supply voltage condition.

**POR brownout, reset (see Notes 1 and 2)**

| PARAMETER         |          | TEST CONDITIONS                                                                                                                  | MIN | TYP                       | MAX  | UNIT          |
|-------------------|----------|----------------------------------------------------------------------------------------------------------------------------------|-----|---------------------------|------|---------------|
| $t_{d(BOR)}$      | Brownout |                                                                                                                                  |     |                           | 2000 | $\mu\text{s}$ |
| $V_{CC(start)}$   |          | $dV_{CC}/dt \leq 3 \text{ V/s}$                                                                                                  |     | $0.7 \times V_{(B\_IT-)}$ |      | V             |
| $V_{(B\_IT-)}$    |          | $dV_{CC}/dt \leq 3 \text{ V/s}$                                                                                                  |     |                           | 1.71 | V             |
| $V_{hys(B\_IT-)}$ |          | $dV_{CC}/dt \leq 3 \text{ V/s}$                                                                                                  | 70  | 130                       | 180  | mV            |
| $t_{(reset)}$     |          | Pulse length needed at $\overline{\text{RST}}/\text{NMI}$ pin to accepted reset internally, $V_{CC} = 2.2 \text{ V}/3 \text{ V}$ | 2   |                           |      | $\mu\text{s}$ |

NOTES: 1. The current consumption of the brown-out module is already included in the  $I_{CC}$  current consumption data.  
2. During power up, the CPU begins code execution following a period of  $t_{d(BOR)}$  after  $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$ . The default DCO settings must not be changed until  $V_{CC} \geq V_{CC(min)}$ , where  $V_{CC(min)}$  is the minimum supply voltage for the desired operating frequency. See the *MSP430x1xx Family User's Guide* for more information on the brownout circuit.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

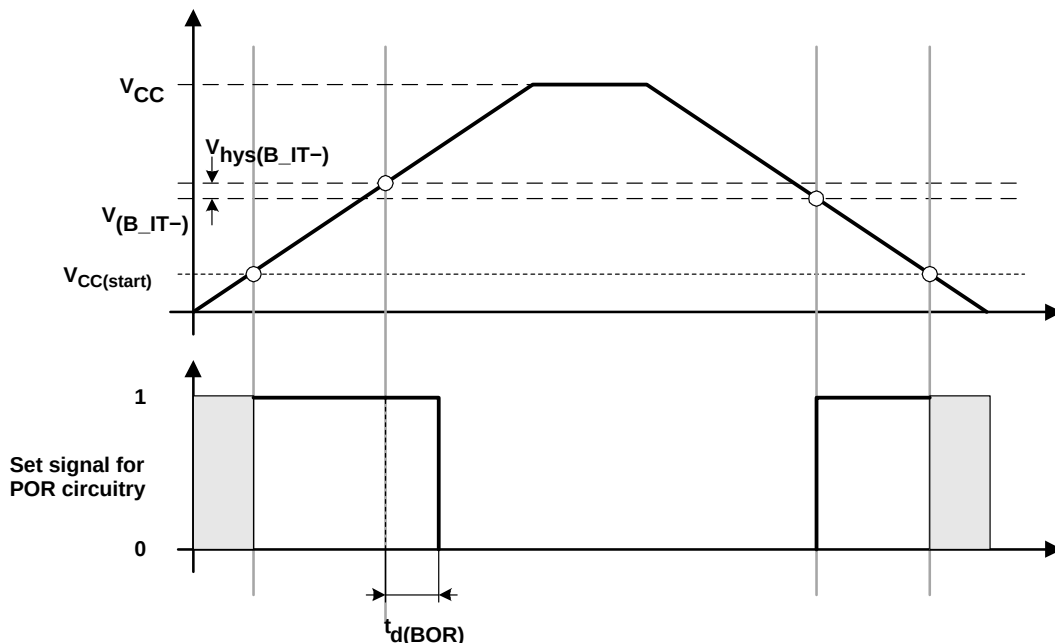


Figure 6. POR/Brownout Reset (BOR) vs Supply Voltage

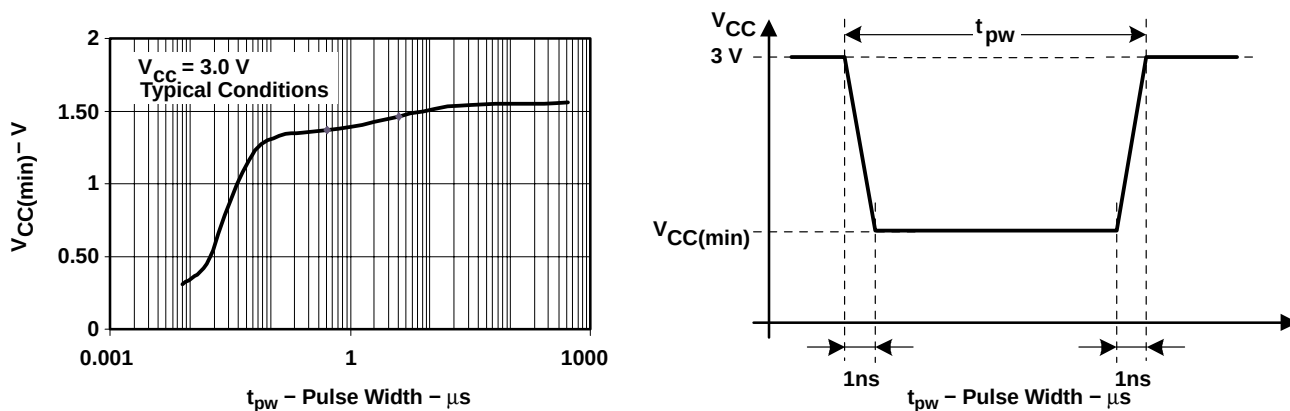


Figure 7.  $V_{CC(min)}$  Level With a Square Voltage Drop to Generate a POR/Brownout Signal

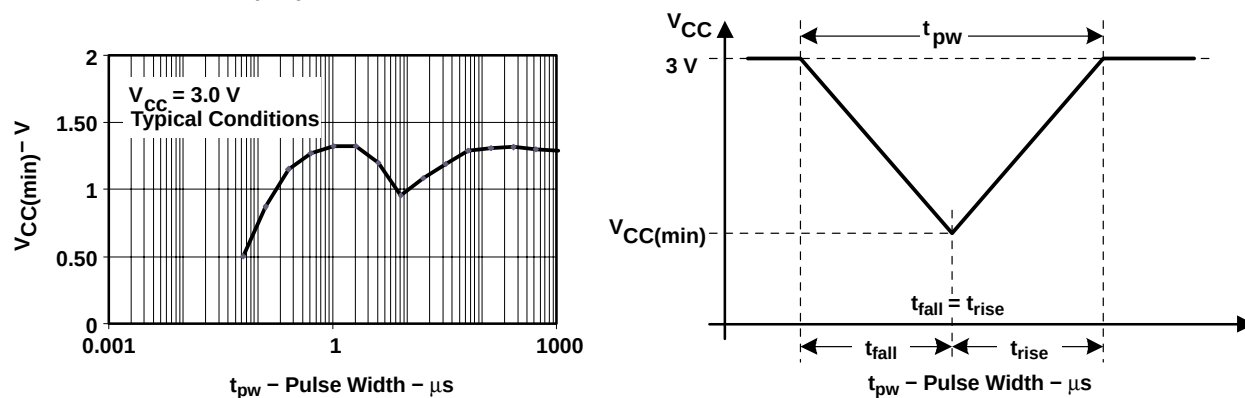


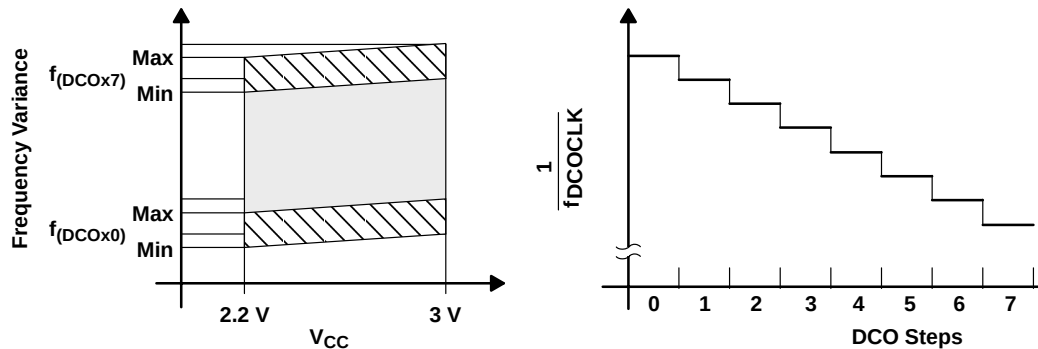
Figure 8.  $V_{CC(min)}$  Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

**DCO**

| PARAMETER            | TEST CONDITIONS                                                                           | V <sub>CC</sub> | MIN                        | TYP                        | MAX                        | UNIT  |
|----------------------|-------------------------------------------------------------------------------------------|-----------------|----------------------------|----------------------------|----------------------------|-------|
| f <sub>(DCO03)</sub> | R <sub>sel</sub> = 0, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                   | 2.2 V           | 0.08                       | 0.12                       | 0.15                       | MHz   |
|                      |                                                                                           | 3 V             | 0.08                       | 0.13                       | 0.16                       |       |
| f <sub>(DCO13)</sub> | R <sub>sel</sub> = 1, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                   | 2.2 V           | 0.14                       | 0.19                       | 0.23                       | MHz   |
|                      |                                                                                           | 3 V             | 0.14                       | 0.18                       | 0.22                       |       |
| f <sub>(DCO23)</sub> | R <sub>sel</sub> = 2, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                   | 2.2 V           | 0.22                       | 0.3                        | 0.36                       | MHz   |
|                      |                                                                                           | 3 V             | 0.22                       | 0.28                       | 0.34                       |       |
| f <sub>(DCO33)</sub> | R <sub>sel</sub> = 3, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                   | 2.2 V           | 0.37                       | 0.49                       | 0.59                       | MHz   |
|                      |                                                                                           | 3 V             | 0.37                       | 0.47                       | 0.56                       |       |
| f <sub>(DCO43)</sub> | R <sub>sel</sub> = 4, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                   | 2.2 V           | 0.61                       | 0.77                       | 0.93                       | MHz   |
|                      |                                                                                           | 3 V             | 0.61                       | 0.75                       | 0.9                        |       |
| f <sub>(DCO53)</sub> | R <sub>sel</sub> = 5, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                   | 2.2 V           | 1                          | 1.2                        | 1.5                        | MHz   |
|                      |                                                                                           | 3 V             | 1                          | 1.3                        | 1.5                        |       |
| f <sub>(DCO63)</sub> | R <sub>sel</sub> = 6, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                   | 2.2 V           | 1.6                        | 1.9                        | 2.2                        | MHz   |
|                      |                                                                                           | 3 V             | 1.69                       | 2                          | 2.29                       |       |
| f <sub>(DCO73)</sub> | R <sub>sel</sub> = 7, DCO = 3, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                   | 2.2 V           | 2.4                        | 2.9                        | 3.4                        | MHz   |
|                      |                                                                                           | 3 V             | 2.7                        | 3.2                        | 3.65                       |       |
| f <sub>(DCO77)</sub> | R <sub>sel</sub> = 7, DCO = 7, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                   | 2.2 V           | 4                          | 4.5                        | 4.9                        | MHz   |
|                      |                                                                                           | 3 V             | 4.4                        | 4.9                        | 5.4                        |       |
| f <sub>(DCO47)</sub> | R <sub>sel</sub> = 4, DCO = 7, MOD = 0, DCOR = 0, T <sub>A</sub> = 25°C                   | 2.2 V/3 V       | f <sub>DCO40</sub><br>x1.7 | f <sub>DCO40</sub><br>x2.1 | f <sub>DCO40</sub><br>x2.5 | MHz   |
| S <sub>(Rsel)</sub>  | S <sub>R</sub> = f <sub>Rsel+1</sub> /f <sub>Rsel</sub>                                   | 2.2 V/3 V       | 1.35                       | 1.65                       | 2                          | ratio |
| S <sub>(DCO)</sub>   | S <sub>DCO</sub> = f <sub>DCO+1</sub> /f <sub>DCO</sub>                                   | 2.2 V/3 V       | 1.07                       | 1.12                       | 1.16                       |       |
| D <sub>t</sub>       | Temperature drift, R <sub>sel</sub> = 4, DCO = 3, MOD = 0 (see Note 1)                    | 2.2 V           | -0.31                      | -0.36                      | -0.4                       | %/°C  |
|                      |                                                                                           | 3 V             | -0.33                      | -0.38                      | -0.43                      |       |
| D <sub>V</sub>       | Drift with V <sub>CC</sub> variation, R <sub>sel</sub> = 4, DCO = 3, MOD = 0 (see Note 1) | 2.2 V/3 V       |                            |                            | ±5                         | %/V   |

NOTES: 1. These parameters are not production tested.



**Figure 9. DCO Characteristics**

# MSP430x11x2, MSP430x12x2 MIXED SIGNAL MICROCONTROLLER

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## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

### main DCO characteristics

- Individual devices have a minimum and maximum operation frequency. The specified parameters for  $f_{(DCOx0)}$  to  $f_{(DCOx7)}$  are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1): Rsel0 overlaps Rsel1, ... Rsel6 overlaps Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter  $S_{DCO}$ .
- Modulation control bits MOD0 to MOD4 select how often  $f_{(DCO+1)}$  is used within the period of 32 DCOCLK cycles. The frequency  $f_{(DCO)}$  is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{(DCO)} \times f_{(DCO+1)}}{MOD \times f_{(DCO)} + (32 - MOD) \times f_{(DCO+1)}}$$

### DCO when using $R_{OSC}$ (see Note 1)

| PARAMETER                             | TEST CONDITIONS                                                         | $V_{CC}$  | MIN | NOM      | MAX | UNIT |
|---------------------------------------|-------------------------------------------------------------------------|-----------|-----|----------|-----|------|
| $f_{DCO}$ , DCO output frequency      | $R_{sel} = 4$ , DCO = 3, MOD = 0, DCOR = 1,<br>$T_A = 25^\circ\text{C}$ | 2.2 V     |     | 1.8±15%  |     | MHz  |
|                                       |                                                                         | 3 V       |     | 1.95±15% |     | MHz  |
| $D_t$ , Temperature drift             | $R_{sel} = 4$ , DCO = 3, MOD = 0, DCOR = 1                              | 2.2 V/3 V |     | ±0.1     |     | %/°C |
| $D_v$ , Drift with $V_{CC}$ variation | $R_{sel} = 4$ , DCO = 3, MOD = 0, DCOR = 1                              | 2.2 V/3 V |     | 10       |     | %/V  |

NOTES: 1.  $R_{OSC} = 100\text{k}\Omega$ . Metal film resistor, type 0257. 0.6 watt with 1% tolerance and  $T_K = \pm 50\text{ppm}/^\circ\text{C}$ .

### crystal oscillator, LFXT1

| PARAMETER  | TEST CONDITIONS                       | $V_{CC}$    | MIN                 | TYP | MAX                 | UNIT |
|------------|---------------------------------------|-------------|---------------------|-----|---------------------|------|
| $C_{XIN}$  | Pin load capacitance                  |             |                     |     |                     | pF   |
|            | XTS=0; LF mode selected               | 2.2 V / 3 V |                     | 12  |                     |      |
|            | XTS=1; XT1 mode selected (see Note 1) | 2.2 V / 3 V |                     | 2   |                     |      |
| $C_{XOUT}$ | Pin load capacitance                  |             |                     |     |                     | pF   |
|            | XTS=0; LF mode selected               | 2.2 V / 3 V |                     | 12  |                     |      |
|            | XTS=1; XT1 mode selected (see Note 1) | 2.2 V / 3 V |                     | 2   |                     |      |
| $V_{IL}$   | Input levels at XIN                   | 2.2 V / 3 V | $V_{SS}$            |     | $0.2 \times V_{CC}$ | V    |
| $V_{IH}$   |                                       |             | $0.8 \times V_{CC}$ |     | $V_{CC}$            | V    |

NOTES: 1. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.  
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**10-bit ADC, power supply and input range conditions (see Note 1)**

| PARAMETER       |                                                                            | TEST CONDITIONS                                                                                                                     | MIN  | NOM  | MAX      | UNIT     |
|-----------------|----------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|------|------|----------|----------|
| $V_{CC}$        | Analog supply voltage                                                      | $V_{SS} = 0\text{ V}$                                                                                                               | 2.2  |      | 3.6      | V        |
| $V_{(P6.x/Ax)}$ | Analog input voltage range (see Note 2)                                    | All Ax terminals. Analog inputs selected in ADC10AE register and PxSel.x=1<br>$V_{SS} \leq V_{Px.x/Ax} \leq V_{CC}$                 | 0    |      | $V_{CC}$ | V        |
| $I_{ADC10}$     | Operating supply current into $V_{CC}$ terminal (see Note 3)               | $f_{ADC10CLK} = 5.0\text{ MHz}$<br><b>ADC10ON = 1, REFON = 0</b><br>ADC10SHT0=1, ADC10SHT1=0, ADC10DIV=0<br>$V_{CC} = 2.2\text{ V}$ | 0.52 | 1.05 |          | mA       |
|                 |                                                                            | $V_{CC} = 3\text{ V}$                                                                                                               | 0.6  | 1.2  |          |          |
| $I_{REF+}$      | Reference operating supply current, reference buffer disabled (see Note 4) | $f_{ADC10CLK} = 5.0\text{ MHz}$<br>ADC10ON = 0, REFON = 1, REF2_5V = x;<br>REFOUT = 0<br>$V_{CC} = 2.2\text{V}/3\text{ V}$          | 0.25 | 0.4  |          | mA       |
| $I_{REFB}$      | Reference buffer operating supply current (see Note 4)                     | $f_{ADC10CLK} = 5.0\text{ MHz}$<br>ADC10ON = 0, REFON = 1, REF2_5V = 0<br>REFOUT = 1<br>ADC10SR = 0                                 | 1.1  | 1.4  |          | mA       |
|                 |                                                                            | ADC10SR = 1                                                                                                                         | 0.46 | 0.55 |          |          |
| $C_I^\dagger$   | Input capacitance                                                          | Only one terminal can be selected at one time, Px.x/Ax<br>$V_{CC} = 2.2\text{ V}$                                                   |      |      | 27       | pF       |
| $R_I^\dagger$   | Input MUX ON resistance                                                    | $0\text{V} \leq V_{Ax} \leq V_{CC}$<br>$V_{CC} = 3\text{ V}$                                                                        |      |      | 2000     | $\Omega$ |

<sup>†</sup> Not production tested, limits verified by design

- NOTES: 1. The leakage current is defined in the leakage current table with Px.x/Ax parameter.  
2. The analog input voltage range must be within the selected reference voltage range  $V_{R+}$  to  $V_{R-}$  for valid conversion results.  
3. The internal reference supply current is not included in current consumption parameter  $I_{ADC10}$ .  
4. The internal reference current is supplied via terminal  $V_{CC}$ . Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

**10-bit ADC, external reference (see Note 1)**

| PARAMETER                          | TEST CONDITIONS                                                                                | $V_{CC}$  | MIN | NOM | MAX      | UNIT          |
|------------------------------------|------------------------------------------------------------------------------------------------|-----------|-----|-----|----------|---------------|
| $V_{eREF+}$                        | Positive external reference voltage input<br>$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 2)     |           | 1.4 |     | $V_{CC}$ | V             |
| $V_{REF-}/V_{eREF-}$               | Negative external reference voltage input<br>$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 3)     |           | 0   |     | 1.2      | V             |
| $(V_{eREF+} - V_{REF-}/V_{eREF-})$ | Differential external reference voltage input<br>$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 4) |           | 1.4 |     | $V_{CC}$ | V             |
| $I_{VeREF+}$                       | Static input current<br>$0\text{V} \leq V_{eREF+} \leq V_{CC}$                                 | 2.2 V/3 V |     |     | $\pm 1$  | $\mu\text{A}$ |
| $I_{VREF-}/V_{eREF-}$              | Static input current<br>$0\text{V} \leq V_{eREF-} \leq V_{CC}$                                 | 2.2 V/3 V |     |     | $\pm 1$  | $\mu\text{A}$ |

- NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance,  $C_I$ , is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.  
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.  
3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.  
4. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

# MSP430x11x2, MSP430x12x2 MIXED SIGNAL MICROCONTROLLER

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**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

## 10-bit ADC, built-in reference

| PARAMETER                                                                                      | TEST CONDITIONS                                                                                                                                                                                     | MIN               | NOM | MAX       | UNIT          |
|------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-----|-----------|---------------|
| $V_{REF+}$<br>Positive built-in reference voltage output                                       | REF2_5V = 1 for 2.5 V<br>$I_{VREF+} \leq I_{VREF+max}$<br>$V_{CC} = 3\text{ V}$                                                                                                                     | 2.35              | 2.5 | 2.65      | V             |
|                                                                                                | REF2_5V = 0 for 1.5 V<br>$I_{VREF+} \leq I_{VREF+max}$<br>$V_{CC} = 2.2\text{ V}/3\text{ V}$                                                                                                        | 1.41              | 1.5 | 1.59      |               |
| $V_{CC(min)}$<br>$V_{CC}$ minimum voltage, Positive built-in reference active                  | REF2_5V = 0, $I_{VREF+} \leq 1\text{ mA}$                                                                                                                                                           | 2.2               |     |           | V             |
|                                                                                                | REF2_5V = 1, $I_{VREF+} \leq 0.5\text{ mA}$                                                                                                                                                         | $V_{REF+} + 0.15$ |     |           |               |
|                                                                                                | REF2_5V = 1, $I_{VREF+} \leq 1\text{ mA}$                                                                                                                                                           | $V_{REF+} + 0.15$ |     |           |               |
| $I_{VREF+}$<br>Load current out of $V_{REF+}$ terminal                                         | $V_{CC} = 2.2\text{ V}$                                                                                                                                                                             |                   |     | $\pm 0.5$ | mA            |
|                                                                                                | $V_{CC} = 3\text{ V}$                                                                                                                                                                               |                   |     | $\pm 1$   |               |
| $I_{L(VREF)+}^{\dagger}$<br>Load-current regulation $V_{REF+}$ terminal                        | $I_{VREF+} = 500\text{ }\mu\text{A} \pm 100\text{ }\mu\text{A}$<br>Analog input voltage $\sim 0.75\text{ V}$ ;<br>REF2_5V = 0<br>$V_{CC} = 2.2\text{ V}$                                            |                   |     | $\pm 2$   | LSB           |
|                                                                                                | $V_{CC} = 3\text{ V}$                                                                                                                                                                               |                   |     | $\pm 2$   |               |
|                                                                                                | $I_{VREF+} = 500\text{ }\mu\text{A} \pm 100\text{ }\mu\text{A}$<br>Analog input voltage $\sim 1.25\text{ V}$ ;<br>REF2_5V = 1<br>$V_{CC} = 3\text{ V}$                                              |                   |     | $\pm 2$   | LSB           |
| $t_{DL(VREF)+}^{\ddagger}$<br>Load current regulation $V_{REF+}$ terminal                      | $I_{VREF+} = 100\text{ }\mu\text{A} \rightarrow 900\text{ }\mu\text{A}$ ,<br>$V_{CC} = 3\text{ V}$ , $Ax \sim 0.5 \times V_{REF+}$<br>Error of conversion result $\leq 1\text{ LSB}$<br>ADC10SR = 0 |                   |     | 400       | ns            |
|                                                                                                | ADC10SR = 1                                                                                                                                                                                         |                   |     | 2000      |               |
| $C_{VREF+}$<br>Capacitance at pin $V_{REF+}$ (see Note 1)                                      | REFON = 1, $I_{VREF+} \leq \pm 1\text{ mA}$<br>$V_{CC} = 2.2\text{ V}/3\text{ V}$                                                                                                                   |                   |     | 100       | pF            |
| $T_{REF+}^{\dagger}$<br>Temperature coefficient of built-in reference                          | $I_{VREF+}$ is a constant in the range of $0\text{ mA} \leq I_{VREF+} \leq 1\text{ mA}$<br>$V_{CC} = 2.2\text{ V}/3\text{ V}$                                                                       |                   |     | $\pm 100$ | ppm/°C        |
| $t_{REFON}^{\dagger}$<br>Settle time of internal reference voltage and $V_{REF+}$ (see Note 2) | $I_{VREF+} = 0.5\text{ mA}$ , $V_{REF+} = 1.5\text{ V}$ , $V_{CC} = 3.6\text{ V}$ ,<br>REFON = 0 $\rightarrow$ 1                                                                                    |                   |     | 30        | $\mu\text{s}$ |
|                                                                                                | $I_{VREF+} = 0.5\text{ mA}$ , $V_{REF+} = 1.5\text{ V}$ ,<br>$V_{CC} = 2.2\text{ V}$ , REFON = 1<br>ADC10SR = 0                                                                                     |                   |     | 0.8       |               |
|                                                                                                | ADC10SR = 1                                                                                                                                                                                         |                   |     | 2.5       |               |

<sup>†</sup> Not production tested, limits characterized

<sup>‡</sup> Not production tested, limits verified by design

NOTES: 1. The capacitance applied to the internal buffer operational amplifier, if switched to terminal P2.4/TA2/A4/ $V_{REF+}$ / $V_{eREF+}$  (REFOUT=1), must be limited; the reference buffer may become unstable otherwise.  
2. The condition is that the error in a conversion started after  $t_{REFON}$  is less than  $\pm 0.5\text{ LSB}$ .

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**10-bit ADC, timing parameters**

| PARAMETER                                                       | TEST CONDITIONS                                                                                                   |                                               | MIN                                                      | NOM | MAX  | UNIT          |
|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|----------------------------------------------------------|-----|------|---------------|
| $f_{\text{ADC10CLK}}$                                           | For specified performance of ADC10 linearity parameters                                                           | ADC10SR = 0                                   | 0.450                                                    |     | 6.3  | MHz           |
|                                                                 |                                                                                                                   | ADC10SR = 1                                   | 0.450                                                    |     | 1.5  |               |
| $f_{\text{ADC10OSC}}$                                           | ADC10DIV=0,<br>$f_{\text{ADC10CLK}}=f_{\text{ADC10OSC}}$                                                          | $V_{\text{CC}} = 2.2 \text{ V} / 3 \text{ V}$ | 3.7                                                      |     | 6.3  | MHz           |
| $t_{\text{CONVERT}}$ Conversion time                            | Internal oscillator,<br>$f_{\text{ADC10OSC}} = 3.7 \text{ MHz}$ to 6.3 MHz                                        | $V_{\text{CC}} = 2.2 \text{ V} / 3 \text{ V}$ | 2.06                                                     |     | 3.51 | $\mu\text{s}$ |
|                                                                 | External $f_{\text{ADC10CLK}}$ from ACLK, MCLK or SMCLK:<br>ADC10SSEL $\neq 0$                                    |                                               | $13 \times \text{ADC10DIV} \times 1/f_{\text{ADC10CLK}}$ |     |      | $\mu\text{s}$ |
| $t_{\text{ADC10ON}}^{\dagger}$ Turn on settling time of the ADC | (see Note 1)                                                                                                      |                                               |                                                          |     | 100  | ns            |
| $t_{\text{Sample}}^{\ddagger}$ Sampling time                    | $R_{\text{S}} = 400 \, \Omega$ , $R_{\text{I}} = 2000 \, \Omega$ ,<br>$C_{\text{I}} = 20 \text{ pF}$ (see Note 2) | $V_{\text{CC}} = 3 \text{ V}$                 | 1400                                                     |     |      | ns            |
|                                                                 |                                                                                                                   | $V_{\text{CC}} = 2.2 \text{ V}$               | 1400                                                     |     |      |               |

$^{\dagger}$  Not production tested, limits characterized

$^{\ddagger}$  Not production tested, limits verified by design

NOTES: 1. The condition is that the error in a conversion started after  $t_{\text{ADC10ON}}$  is less than  $\pm 0.5$  LSB. The reference and input signal are already settled.

2. Approximately eight Tau ( $\tau$ ) are needed to get an error of less than  $\pm 0.5$  LSB.

$t_{\text{Sample}} = \ln(2^{n+1}) \times (R_{\text{S}} + R_{\text{I}}) \times C_{\text{I}} + 800 \text{ ns}$ . (ADC10SR = 0,  $n$  = ADC resolution = 10,  $R_{\text{S}}$  = external source resistance)

$t_{\text{Sample}} = \ln(2^{n+1}) \times (R_{\text{S}} + R_{\text{I}}) \times C_{\text{I}} + 2.5 \, \mu\text{s}$ . (ADC10SR = 1,  $n$  = ADC resolution = 10,  $R_{\text{S}}$  = external source resistance)

**10-bit ADC, linearity parameters**

| PARAMETER                                   | TEST CONDITIONS                                                                                                                                                                              | $V_{\text{CC}}$ | MIN | NOM       | MAX     | UNIT |
|---------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----------|---------|------|
| $E_{\text{I}}$ Integral linearity error     | $1.4 \text{ V} \leq (V_{\text{eREF}+} - V_{\text{REF-}}/V_{\text{eREF-}}) \min \leq 1.6 \text{ V}$                                                                                           | 2.2 V/3 V       |     |           | $\pm 1$ | LSB  |
|                                             | $1.6 \text{ V} < (V_{\text{eREF}+} - V_{\text{REF-}}/V_{\text{eREF-}}) \min \leq [V_{\text{CC}}]$                                                                                            |                 |     |           | $\pm 1$ |      |
| $E_{\text{D}}$ Differential linearity error | $(V_{\text{eREF}+} - V_{\text{REF-}}/V_{\text{eREF-}})_{\min} \leq (V_{\text{eREF}+} - V_{\text{REF-}}/V_{\text{eREF-}})$                                                                    | 2.2 V/3 V       |     |           | $\pm 1$ | LSB  |
| $E_{\text{O}}$ Offset error                 | $(V_{\text{eREF}+} - V_{\text{REF-}}/V_{\text{eREF-}})_{\min} \leq (V_{\text{eREF}+} - V_{\text{REF-}}/V_{\text{eREF-}})$ ,<br>Internal impedance of source $R_{\text{S}} < 100 \, \Omega$ , | 2.2 V/3 V       |     | $\pm 2$   | $\pm 4$ | LSB  |
| $E_{\text{G}}$ Gain error                   | $(V_{\text{eREF}+} - V_{\text{REF-}}/V_{\text{eREF-}})_{\min} \leq (V_{\text{eREF}+} - V_{\text{REF-}}/V_{\text{eREF-}})$ ,                                                                  | 2.2 V/3 V       |     | $\pm 1.1$ | $\pm 2$ | LSB  |
| $E_{\text{T}}$ Total unadjusted error       | $(V_{\text{eREF}+} - V_{\text{REF-}}/V_{\text{eREF-}})_{\min} \leq (V_{\text{eREF}+} - V_{\text{REF-}}/V_{\text{eREF-}})$ ,                                                                  | 2.2 V/3 V       |     | $\pm 2$   | $\pm 5$ | LSB  |

# MSP430x11x2, MSP430x12x2 MIXED SIGNAL MICROCONTROLLER

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**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

## 10-bit ADC, temperature sensor and built-in $V_{MID}$

| PARAMETER                    | TEST CONDITIONS                                              | $V_{CC}$                                                       | MIN   | NOM  | MAX             | UNIT                 |
|------------------------------|--------------------------------------------------------------|----------------------------------------------------------------|-------|------|-----------------|----------------------|
| $I_{SENSOR}$                 | Operating supply current into $V_{CC}$ terminal (see Note 1) | REFON = 0, INCH = 0Ah,<br>ADC10ON=NA, $T_A = 25^\circ\text{C}$ | 2.2 V | 40   | 120             | $\mu\text{A}$        |
|                              |                                                              |                                                                | 3 V   | 60   | 160             |                      |
| $V_{SENSOR}^\dagger$         | ADC10ON = 1, INCH = 0Ah,<br>$T_A = 0^\circ\text{C}$          | 2.2 V                                                          |       | 986  | 986 $\pm$ 5%    | mV                   |
|                              |                                                              | 3 V                                                            |       | 986  | 986 $\pm$ 5%    |                      |
| $TC_{SENSOR}^\dagger$        | ADC10ON = 1, INCH = 0Ah                                      | 2.2 V                                                          |       | 3.55 | 3.55 $\pm$ 3%   | mV/ $^\circ\text{C}$ |
|                              |                                                              | 3 V                                                            |       | 3.55 | 3.55 $\pm$ 3%   |                      |
| $t_{SENSOR(sample)}^\dagger$ | Sample time required if channel 10 is selected (see Note 2)  | 2.2 V                                                          | 30    |      |                 | $\mu\text{s}$        |
|                              |                                                              | 3 V                                                            | 30    |      |                 |                      |
| $I_{VMID}$                   | Current into divider at channel 11 (see Note 3)              | 2.2 V                                                          |       |      | NA              | $\mu\text{A}$        |
|                              |                                                              | 3 V                                                            |       |      | NA              |                      |
| $V_{MID}$                    | $V_{CC}$ divider at channel 11                               | 2.2 V                                                          |       | 1.1  | 1.1 $\pm$ 0.04  | V                    |
|                              |                                                              | 3 V                                                            |       | 1.5  | 1.50 $\pm$ 0.04 |                      |
| $t_{VMID(sample)}$           | Sample time required if channel 11 is selected (see Note 4)  | 2.2 V                                                          | 1400  |      |                 | ns                   |
|                              |                                                              | 3 V                                                            | 1220  |      |                 |                      |

$^\dagger$  Not production tested, limits characterized

- NOTES:
1. The sensor current  $I_{SENSOR}$  is consumed if (ADC10ON = 1 and REFON = 1), or (ADC10ON=1 and INCH=0Ah and sample signal is high). When REFON = 1,  $I_{SENSOR}$  is included in  $I_{REF+}$ . When REFON = 0,  $I_{SENSOR}$  applies during conversion of the temperature sensor input (INCH = 0Ah).
  2. The typical equivalent impedance of the sensor is 51 k $\Omega$ . The sample time required includes the sensor-on time  $t_{SENSOR(on)}$ .
  3. No additional current is needed. The  $V_{MID}$  is used during sampling.
  4. The on-time  $t_{VMID(on)}$  is included in the sampling time  $t_{VMID(sample)}$ ; no additional on time is needed.

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**Flash Memory**

| PARAMETER                  |                                                     | TEST CONDITIONS       | V <sub>CC</sub> | MIN             | NOM             | MAX | UNIT             |
|----------------------------|-----------------------------------------------------|-----------------------|-----------------|-----------------|-----------------|-----|------------------|
| V <sub>CC(PGM/ERASE)</sub> | Program and Erase supply voltage                    |                       |                 | 2.7             |                 | 3.6 | V                |
| f <sub>FTG</sub>           | Flash Timing Generator frequency                    |                       |                 | 257             |                 | 476 | kHz              |
| I <sub>PGM</sub>           | Supply current from V <sub>CC</sub> during program  |                       | 2.7 V/ 3.6 V    |                 | 3               | 5   | mA               |
| I <sub>ERASE</sub>         | Supply current from V <sub>CC</sub> during erase    |                       | 2.7 V/ 3.6 V    |                 | 3               | 7   | mA               |
| t <sub>CPT</sub>           | Cumulative program time                             | see Note 1            | 2.7 V/ 3.6 V    |                 |                 | 4   | ms               |
| t <sub>CMErase</sub>       | Cumulative mass erase time                          | see Note 2            | 2.7 V/ 3.6 V    | 200             |                 |     | ms               |
|                            | Program/Erase endurance                             |                       |                 | 10 <sup>4</sup> | 10 <sup>5</sup> |     | cycles           |
| t <sub>Retention</sub>     | Data retention duration                             | T <sub>J</sub> = 25°C |                 | 100             |                 |     | years            |
| t <sub>Word</sub>          | Word or byte program time                           | see Note 3            |                 |                 | 35              |     | t <sub>FTG</sub> |
| t <sub>Block, 0</sub>      | Block program time for 1 <sup>st</sup> byte or word |                       |                 |                 | 30              |     |                  |
| t <sub>Block, 1-63</sub>   | Block program time for each additional byte or word |                       |                 |                 | 21              |     |                  |
| t <sub>Block, End</sub>    | Block program end-sequence wait time                |                       |                 |                 | 6               |     |                  |
| t <sub>Mass Erase</sub>    | Mass erase time                                     |                       |                 |                 | 5297            |     |                  |
| t <sub>Seg Erase</sub>     | Segment erase time                                  |                       |                 |                 | 4819            |     |                  |

- NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms ( = 5297x1/f<sub>FTG,max</sub> = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine; t<sub>FTG</sub> = 1/f<sub>FTG</sub>.

**JTAG Interface**

| PARAMETER             |                                       | TEST CONDITIONS | V <sub>CC</sub> | MIN | NOM | MAX | UNIT |
|-----------------------|---------------------------------------|-----------------|-----------------|-----|-----|-----|------|
| f <sub>TCK</sub>      | TCK input frequency                   | see Note 1      | 2.2 V           | 0   |     | 5   | MHz  |
|                       |                                       |                 | 3 V             | 0   |     | 10  | MHz  |
| R <sub>Internal</sub> | Internal pull-down resistance on TEST | see Note 2      | 2.2 V/ 3 V      | 25  | 60  | 90  | kΩ   |

- NOTES: 1. f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.
2. TEST pull-down resistor implemented in all Flash versions.

**JTAG Fuse (see Note 1)**

| PARAMETER           |                                           | TEST CONDITIONS       | V <sub>CC</sub> | MIN | NOM | MAX | UNIT |
|---------------------|-------------------------------------------|-----------------------|-----------------|-----|-----|-----|------|
| V <sub>CC(FB)</sub> | Supply voltage during fuse-blow condition | T <sub>A</sub> = 25°C |                 | 2.5 |     |     | V    |
| V <sub>FB</sub>     | Voltage level on TEST for fuse-blow       |                       |                 | 6   |     | 7   | V    |
| I <sub>FB</sub>     | Supply current into TEST during fuse blow |                       |                 |     |     | 100 | mA   |
| t <sub>FB</sub>     | Time to blow fuse                         |                       |                 |     |     | 1   | ms   |

- NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

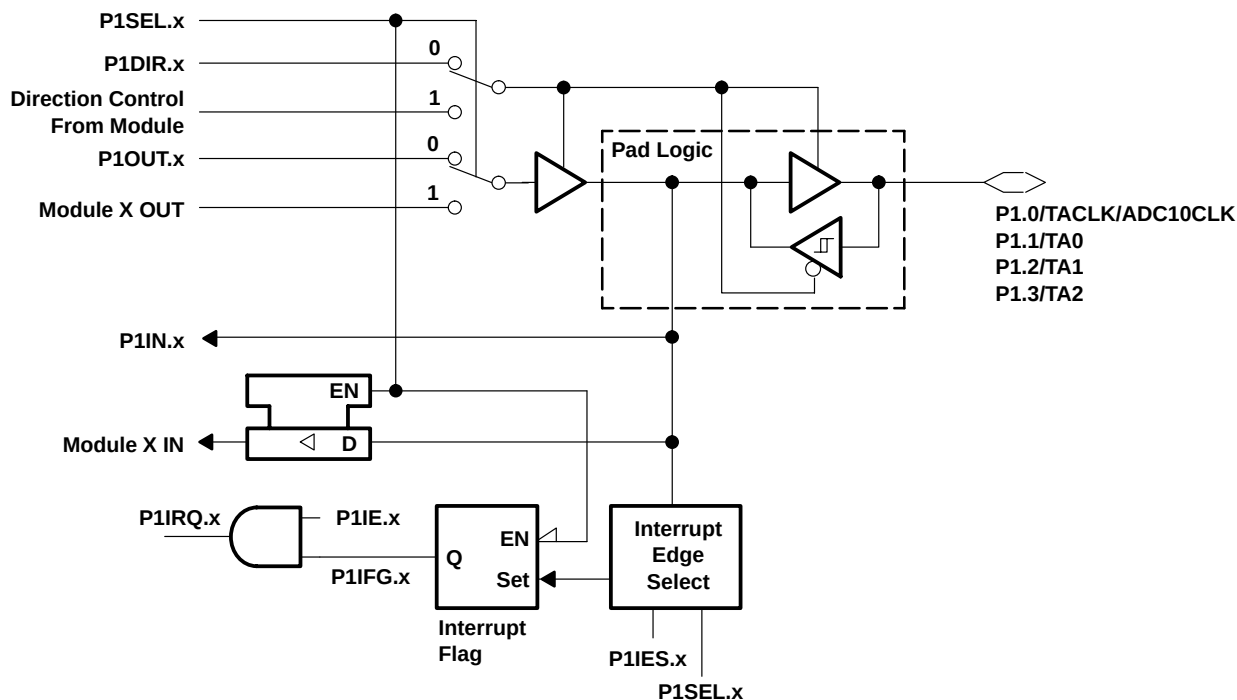
## MSP430x11x2, MSP430x12x2

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## APPLICATION INFORMATION

## input/output schematic

### Port P1, P1.0 to P1.3, input/output with Schmitt-trigger



NOTE: x = Bit/identifier, 0 to 3 for port P1

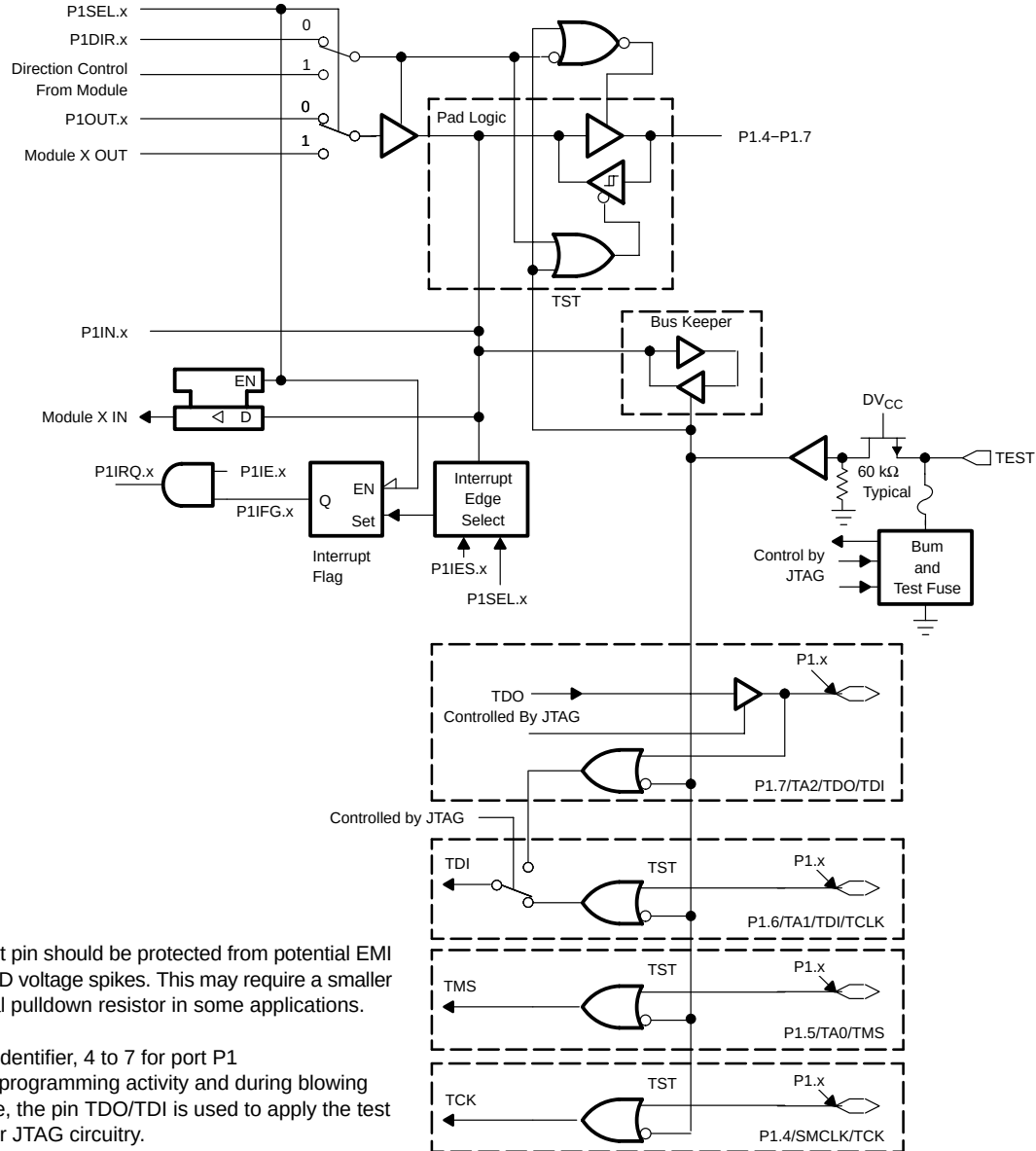
| PnSel.x | PnDIR.x | DIRECTION<br>CONTROL FROM<br>MODULE | PnOUT.x | MODULE X OUT             | PnIN.x | MODULE X IN        | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------------|---------|--------------------------|--------|--------------------|--------|---------|---------|
| P1Sel.0 | P1DIR.0 | P1DIR.0                             | P1OUT.0 | ADC10CLK                 | P1IN.0 | TACLK <sup>†</sup> | P1IE.0 | P1IFG.0 | P1IES.0 |
| P1Sel.1 | P1DIR.1 | P1DIR.1                             | P1OUT.1 | Out0 signal <sup>†</sup> | P1IN.1 | CCI0A <sup>†</sup> | P1IE.1 | P1IFG.1 | P1IES.1 |
| P1Sel.2 | P1DIR.2 | P1DIR.2                             | P1OUT.2 | Out1 signal <sup>†</sup> | P1IN.2 | CCI1A <sup>†</sup> | P1IE.2 | P1IFG.2 | P1IES.2 |
| P1Sel.3 | P1DIR.3 | P1DIR.3                             | P1OUT.3 | Out2 signal <sup>†</sup> | P1IN.3 | CCI2A <sup>†</sup> | P1IE.3 | P1IFG.3 | P1IES.3 |

<sup>†</sup> Signal from or to Timer A

**APPLICATION INFORMATION**

**input/output schematic (continued)**

**Port P1, P1.4 to P1.7, input/output with Schmitt-trigger and in-system access features**



NOTE: The test pin should be protected from potential EMI and ESD voltage spikes. This may require a smaller external pulldown resistor in some applications.

x = Bit identifier, 4 to 7 for port P1  
 During programming activity and during blowing the fuse, the pin TDO/TDI is used to apply the test input for JTAG circuitry.

| PnSel.x | PnDIR.x | DIRECTION CONTROL FROM MODULE | PnOUT.x | MODULE X OUT             | PnIN.x | MODULE X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|--------------------------|--------|-------------|--------|---------|---------|
| P1Sel.4 | P1DIR.4 | P1DIR.4                       | P1OUT.4 | SMCLK                    | P1IN.4 | unused      | P1IE.4 | P1IFG.4 | P1IES.4 |
| P1Sel.5 | P1DIR.5 | P1DIR.5                       | P1OUT.5 | Out0 signal <sup>†</sup> | P1IN.5 | unused      | P1IE.5 | P1IFG.5 | P1IES.5 |
| P1Sel.6 | P1DIR.6 | P1DIR.6                       | P1OUT.6 | Out1 signal <sup>†</sup> | P1IN.6 | unused      | P1IE.6 | P1IFG.6 | P1IES.6 |
| P1Sel.7 | P1DIR.7 | P1DIR.7                       | P1OUT.7 | Out2 signal <sup>†</sup> | P1IN.7 | unused      | P1IE.7 | P1IFG.7 | P1IES.7 |

<sup>†</sup> Signal from or to Timer\_A

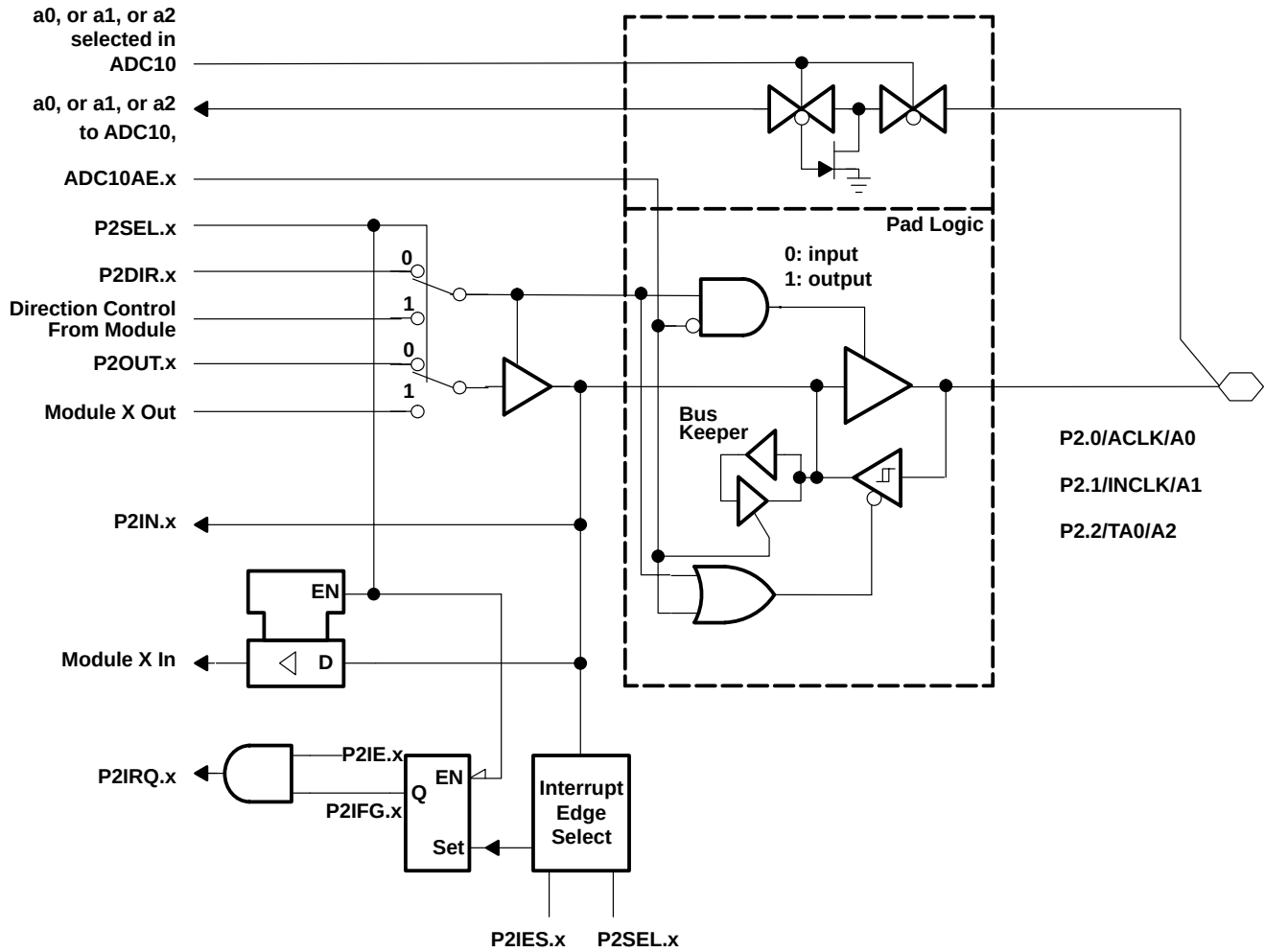
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APPLICATION INFORMATION

input/output schematic (continued)

Port P2, P2.0 to P2.2, input/output with Schmitt-trigger



NOTE:  $0 \leq x \leq 2$

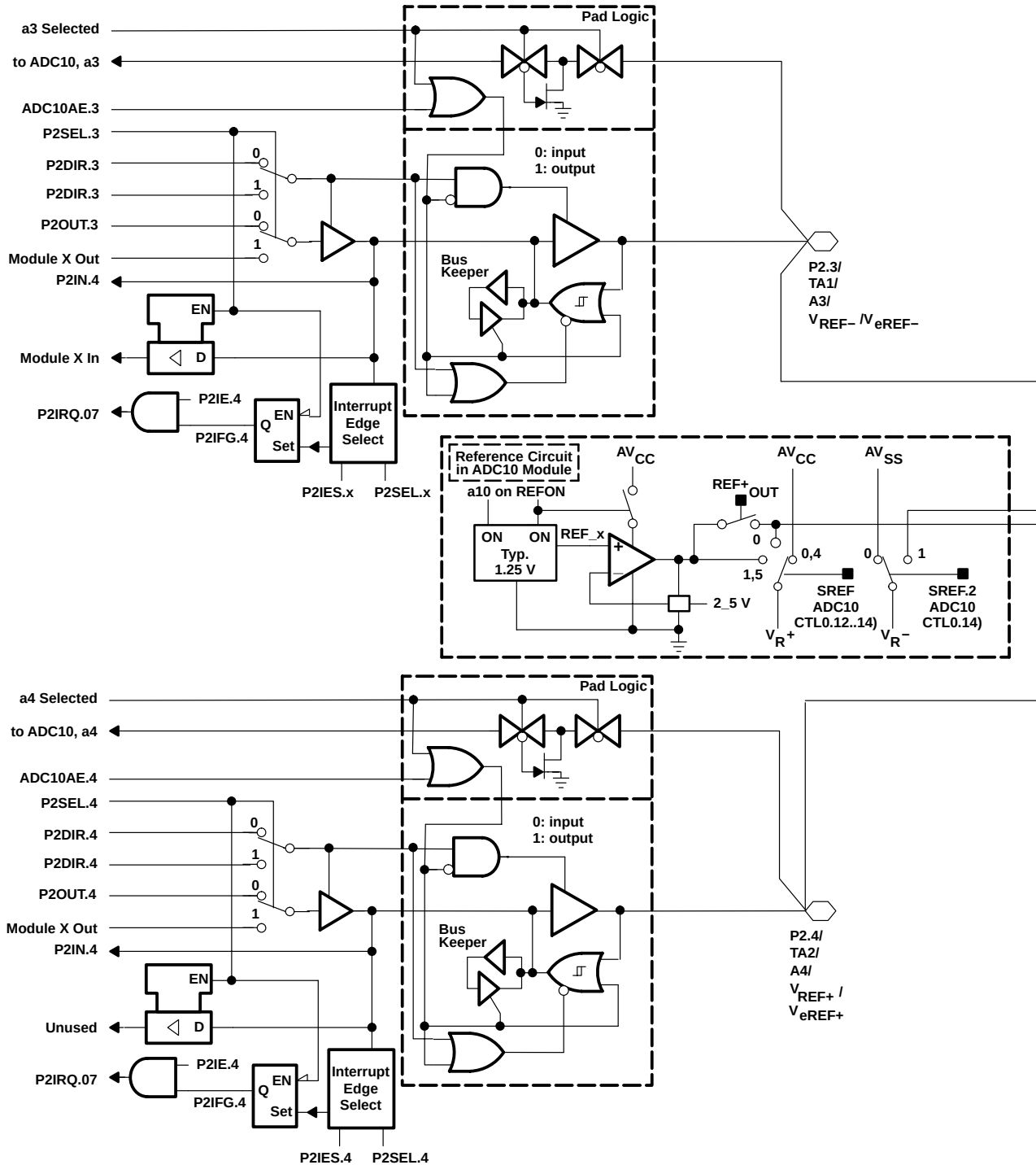
| PnSel.x | PnDIR.x | DIRECTION<br>CONTROL<br>FROM MODULE | PnOUT.x | MODULE X OUT             | PnIN.x | MODULE X IN        | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------------|---------|--------------------------|--------|--------------------|--------|---------|---------|
| P2Sel.0 | P2DIR.0 | P2DIR.0                             | P2OUT.0 | ACLK <sup>†</sup>        | P2IN.0 | unused             | P2IE.0 | P2IFG.0 | P1IES.0 |
| P2Sel.1 | P2DIR.1 | P2DIR.1                             | P2OUT.1 | V <sub>SS</sub>          | P2IN.1 | INCLK <sup>†</sup> | P2IE.1 | P2IFG.1 | P1IES.1 |
| P2Sel.2 | P2DIR.2 | P2DIR.2                             | P2OUT.2 | OUT0 signal <sup>†</sup> | P2IN.2 | CCI0B <sup>†</sup> | P2IE.2 | P2IFG.2 | P1IES.2 |

<sup>†</sup> Timer\_A

**APPLICATION INFORMATION**

**input/output schematic (continued)**

**Port P2, P2.3 to P2.4, input/output with Schmitt-trigger**



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APPLICATION INFORMATION

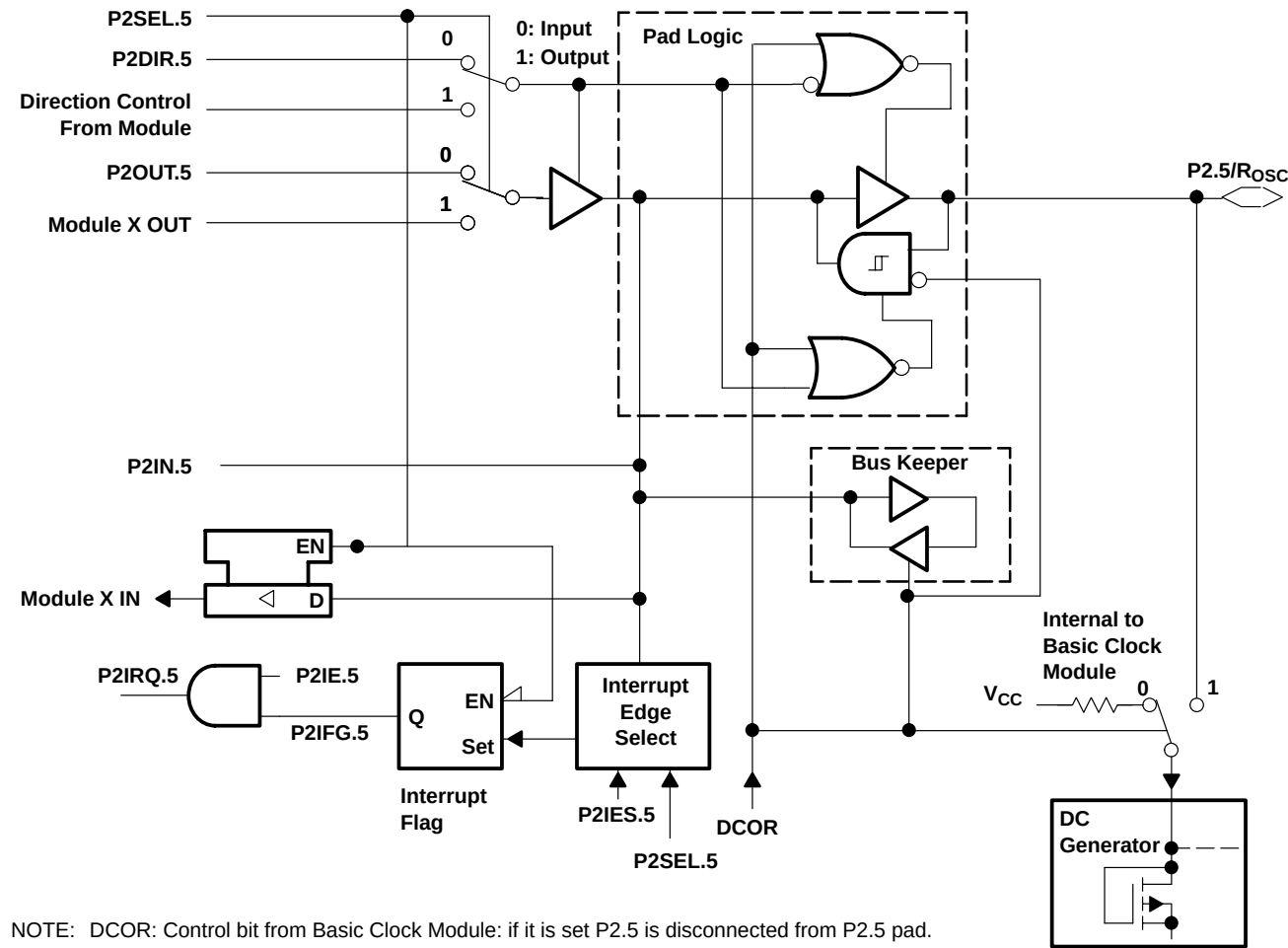
Port P2, P2.3 to P2.4, input/output with Schmitt-trigger (continued)

| PnSel.x | PnDIR.x | DIRECTION CONTROL FROM MODULE | PnOUT.x | MODULE X OUT             | PnIN.x | MODULE X IN        | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|--------------------------|--------|--------------------|--------|---------|---------|
| P2Sel.3 | P2DIR.3 | P2DIR.3                       | P2OUT.3 | Out1 signal <sup>†</sup> | P2IN.3 | CCI1B <sup>†</sup> | P2IE.3 | P2IFG.3 | P1IES.3 |
| P2Sel.4 | P2DIR.4 | P2DIR.4                       | P2OUT.4 | Out2 signal <sup>†</sup> | P2IN.4 | Unused             | P2IE.4 | P2IFG.4 | P1IES.4 |

<sup>†</sup> Timer\_A

input/output schematic (continued)

Port P2, P2.5, input/output with Schmitt-trigger and R<sub>OSC</sub> function for the Basic Clock Module



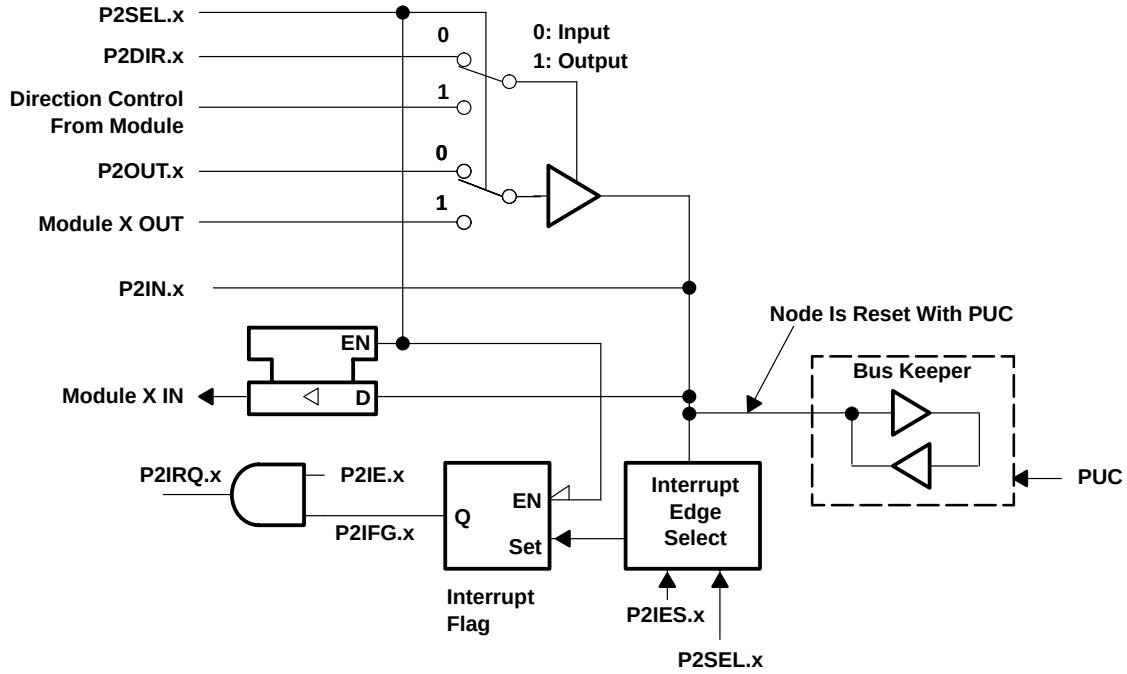
NOTE: DCOR: Control bit from Basic Clock Module: if it is set P2.5 is disconnected from P2.5 pad.

| PnSel.x | PnDIR.x | DIRECTION CONTROL FROM MODULE | PnOUT.x | MODULE X OUT    | PnIN.x | MODULE X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|-----------------|--------|-------------|--------|---------|---------|
| P2Sel.5 | P2DIR.5 | P2DIR.5                       | P2OUT.5 | V <sub>SS</sub> | P2IN.5 | unused      | P2IE.5 | P2IFG.5 | P2IES.5 |

**APPLICATION INFORMATION**

**input/output schematic (continued)**

**Port P2, unbonded bits P2.6 and P2.7**



NOTE: x = Bit/identifier, 6 to 7 for port P2 without external pins

| P2Sel.x | P2DIR.x | DIRECTION CONTROL FROM MODULE | P2OUT.x | MODULE X OUT    | P2IN.x | MODULE X IN | P2IE.x | P2IFG.x | P2IES.x |
|---------|---------|-------------------------------|---------|-----------------|--------|-------------|--------|---------|---------|
| P2Sel.6 | P2DIR.6 | P2DIR.6                       | P2OUT.6 | V <sub>SS</sub> | P2IN.6 | unused      | P2IE.6 | P2IFG.6 | P2IES.6 |
| P2Sel.7 | P2DIR.7 | P2DIR.7                       | P2OUT.7 | V <sub>SS</sub> | P2IN.7 | unused      | P2IE.7 | P2IFG.7 | P2IES.7 |

NOTE: Unbonded bits 6 and 7 of port P2 can be used as interrupt flags. Only software can affect the interrupt flags. They work as software interrupts.

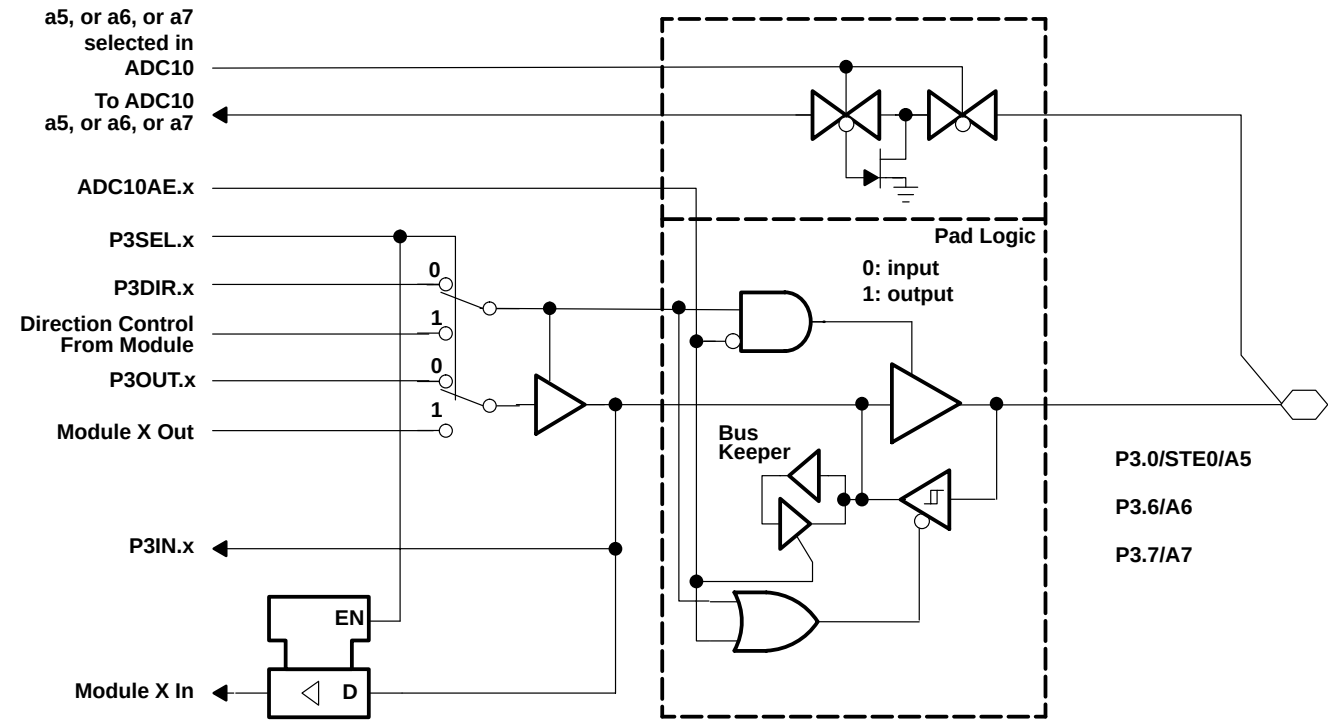
MSP430x11x2, MSP430x12x2  
MIXED SIGNAL MICROCONTROLLER

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APPLICATION INFORMATION

input/output schematic (continued)

port P3, P3.0, P3.6 and P3.7 input/output with Schmitt-trigger



NOTE: x (0,6,7)

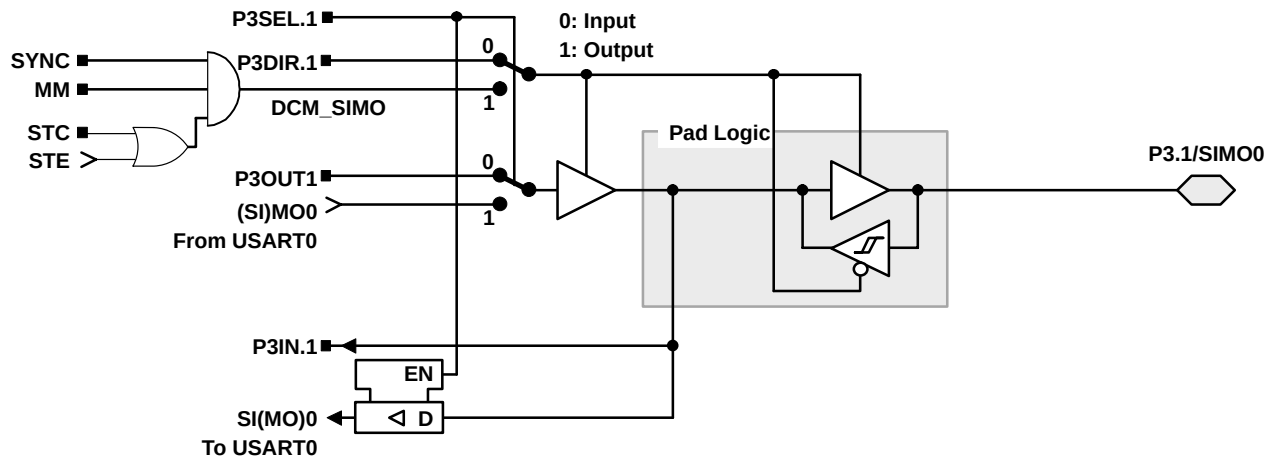
| PnSel.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT    | PnIN.x | Module X IN       |
|---------|---------|-------------------------------|---------|-----------------|--------|-------------------|
| P3Sel.0 | P3DIR.0 | V <sub>SS</sub>               | P3OUT.0 | V <sub>SS</sub> | P3IN.0 | STE0 <sup>†</sup> |
| P3Sel.6 | P3DIR.1 | P3DIR.6                       | P3OUT.6 | V <sub>SS</sub> | P3IN.6 | Unused            |
| P3Sel.7 | P3DIR.2 | P3DIR.7                       | P3OUT.7 | V <sub>SS</sub> | P3IN.7 | Unused            |

<sup>†</sup> USART0

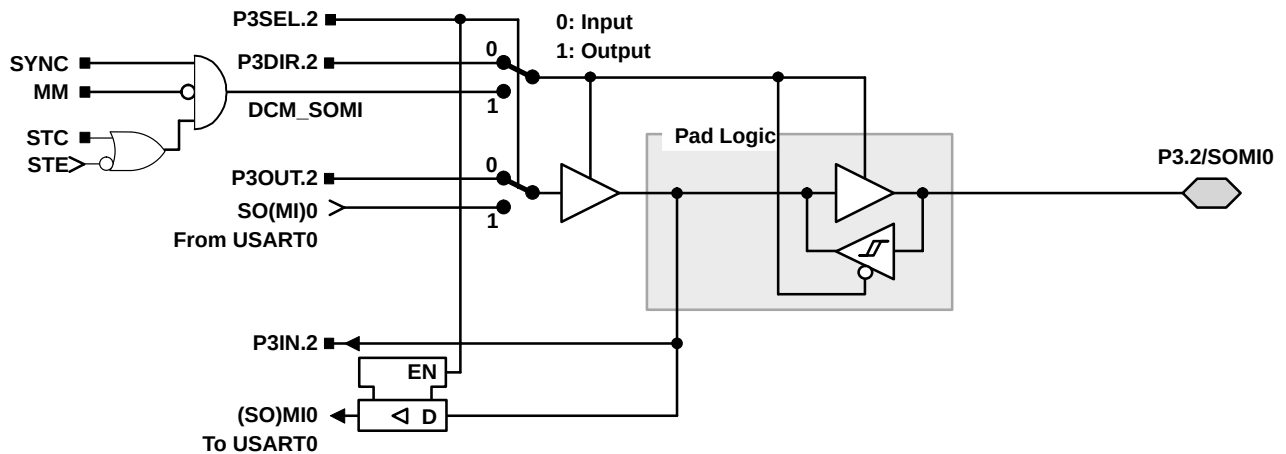
**APPLICATION INFORMATION**

**input/output schematic (continued)**

**port P3, P3.1 input/output with Schmitt-trigger**



**port P3, P3.2, input/output with Schmitt-trigger**



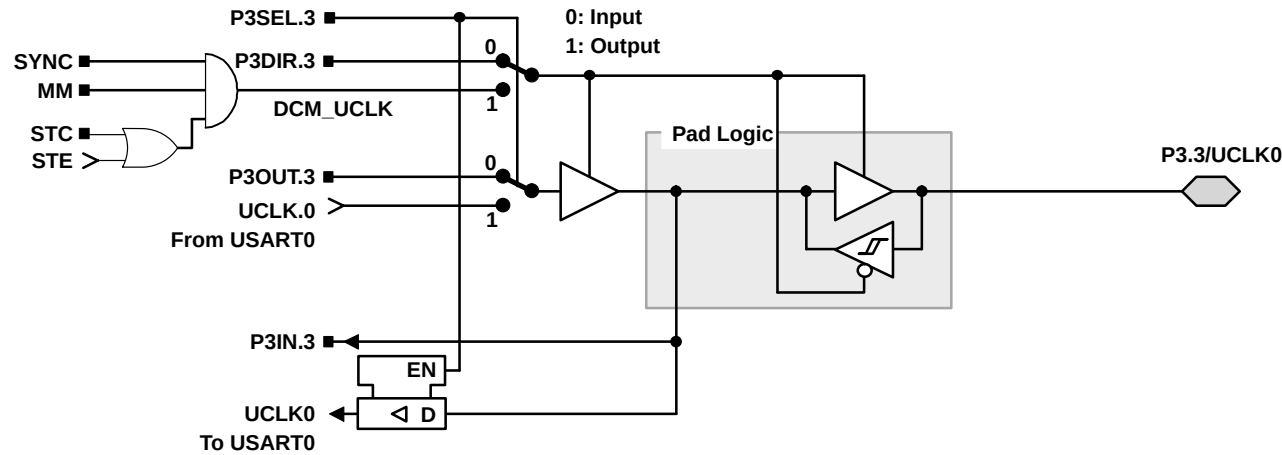
MSP430x11x2, MSP430x12x2  
MIXED SIGNAL MICROCONTROLLER

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APPLICATION INFORMATION

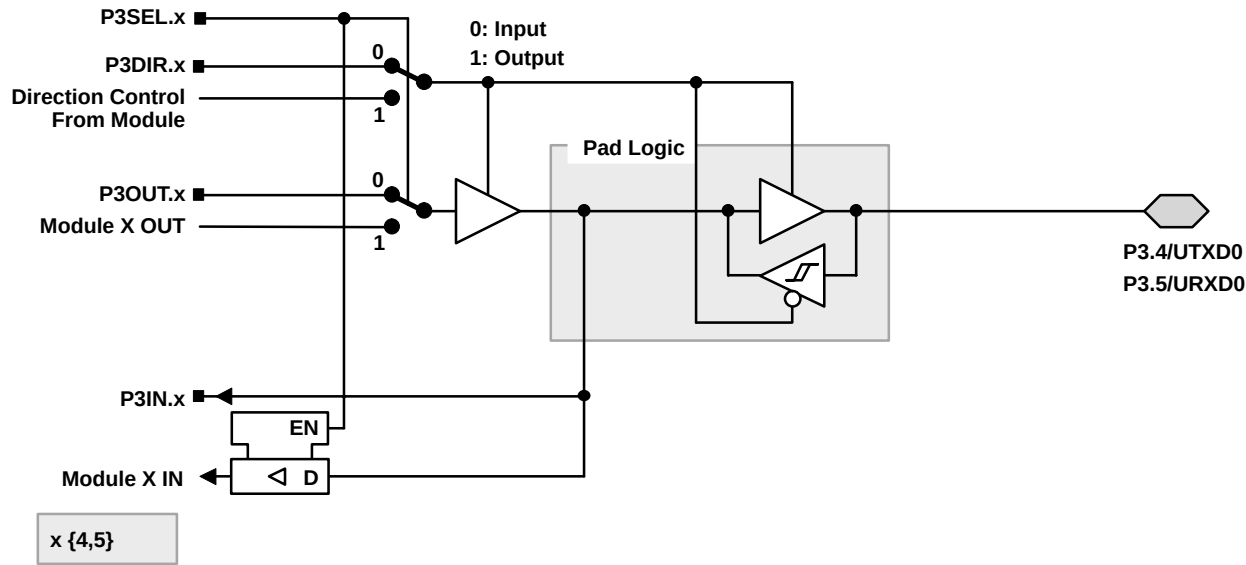
input/output schematic (continued)

port P3, P3.3, input/output with Schmitt-trigger



NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, the P3.3/UCLK0 is always an input.  
SPI, slave mode: The clock applied to UCLK0 is used to shift data in and out.  
SPI, master mode: The clock to shift data in and out is supplied to connected devices on pin P3.3/UCLK0 (in slave mode).

port P3, P3.4, and P3.5 input/output with Schmitt-trigger



| PnSel.x | PnDIR.x | DIRECTION<br>CONTROL<br>FROM MODULE | PnOUT.x | MODULE X OUT       | PnIN.x | MODULE X IN        |
|---------|---------|-------------------------------------|---------|--------------------|--------|--------------------|
| P3Sel.4 | P3DIR.4 | V <sub>CC</sub>                     | P3OUT.4 | UTXD0 <sup>†</sup> | P3IN.4 | Unused             |
| P3Sel.5 | P3DIR.5 | V <sub>SS</sub>                     | P3OUT.5 | V <sub>SS</sub>    | P3IN.5 | URXD0 <sup>‡</sup> |

<sup>†</sup> Output from USART0 module

<sup>‡</sup> Input to USART0 module

## APPLICATION INFORMATION

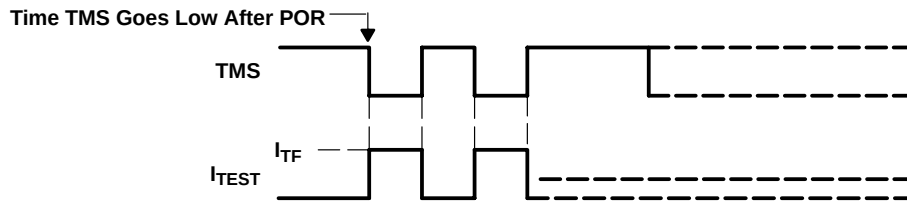
### JTAG fuse check mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current,  $I_{TF}$ , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is taken back low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 10). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).



**Figure 10. Fuse Check Mode Current, MSP430F11x2, MSP430F12x2**

**NOTE:**

The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the *bootstrap loader* section for more information.

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">MSP430F1122IDW</a>   | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1122           |
| MSP430F1122IDW.B                 | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1122           |
| <a href="#">MSP430F1122IDWR</a>  | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1122           |
| MSP430F1122IDWR.B                | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1122           |
| <a href="#">MSP430F1122IPW</a>   | Active        | Production           | TSSOP (PW)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 430F1122            |
| MSP430F1122IPW.B                 | Active        | Production           | TSSOP (PW)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 430F1122            |
| <a href="#">MSP430F1122IPWR</a>  | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 430F1122            |
| MSP430F1122IPWR.B                | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 430F1122            |
| <a href="#">MSP430F1122IRHBT</a> | Active        | Production           | VQFN (RHB)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1122     |
| MSP430F1122IRHBT.B               | Active        | Production           | VQFN (RHB)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1122     |
| <a href="#">MSP430F1132IDW</a>   | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1132           |
| MSP430F1132IDW.B                 | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1132           |
| <a href="#">MSP430F1132IDWR</a>  | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1132           |
| MSP430F1132IDWR.B                | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1132           |
| <a href="#">MSP430F1132IPW</a>   | Active        | Production           | TSSOP (PW)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 430F1132            |
| MSP430F1132IPW.B                 | Active        | Production           | TSSOP (PW)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 430F1132            |
| <a href="#">MSP430F1132IPWR</a>  | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 430F1132            |
| MSP430F1132IPWR.B                | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 430F1132            |
| <a href="#">MSP430F1132IRHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1132     |
| MSP430F1132IRHBR.B               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1132     |
| <a href="#">MSP430F1132IRHBT</a> | Active        | Production           | VQFN (RHB)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1132     |
| MSP430F1132IRHBT.B               | Active        | Production           | VQFN (RHB)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1132     |
| <a href="#">MSP430F1222IDW</a>   | Active        | Production           | SOIC (DW)   28  | 20   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1222           |
| MSP430F1222IDW.B                 | Active        | Production           | SOIC (DW)   28  | 20   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1222           |
| <a href="#">MSP430F1222IDWR</a>  | Active        | Production           | SOIC (DW)   28  | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1222           |

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| MSP430F1222IDWR.B                | Active        | Production           | SOIC (DW)   28  | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1222           |
| <a href="#">MSP430F1222IPW</a>   | Active        | Production           | TSSOP (PW)   28 | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1222           |
| MSP430F1222IPW.B                 | Active        | Production           | TSSOP (PW)   28 | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1222           |
| <a href="#">MSP430F1222IPWR</a>  | Active        | Production           | TSSOP (PW)   28 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1222           |
| MSP430F1222IPWR.B                | Active        | Production           | TSSOP (PW)   28 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1222           |
| <a href="#">MSP430F1222IRHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1222     |
| MSP430F1222IRHBR.B               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1222     |
| <a href="#">MSP430F1222IRHBT</a> | Active        | Production           | VQFN (RHB)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1222     |
| MSP430F1222IRHBT.B               | Active        | Production           | VQFN (RHB)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1222     |
| MSP430F1232CY.B                  | Active        | Production           | DIESALE (Y)   0 | 650   NOT REQUIRED    | Yes         | Call TI                              | N/A for Pkg Type                  | -40 to 85    |                     |
| <a href="#">MSP430F1232IDW</a>   | Active        | Production           | SOIC (DW)   28  | 20   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1232           |
| MSP430F1232IDW.B                 | Active        | Production           | SOIC (DW)   28  | 20   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1232           |
| <a href="#">MSP430F1232IDWR</a>  | Active        | Production           | SOIC (DW)   28  | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1232           |
| MSP430F1232IDWR.B                | Active        | Production           | SOIC (DW)   28  | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1232           |
| <a href="#">MSP430F1232IPW</a>   | Active        | Production           | TSSOP (PW)   28 | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1232           |
| MSP430F1232IPW.B                 | Active        | Production           | TSSOP (PW)   28 | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1232           |
| <a href="#">MSP430F1232IPWR</a>  | Active        | Production           | TSSOP (PW)   28 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1232           |
| MSP430F1232IPWR.B                | Active        | Production           | TSSOP (PW)   28 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1232           |
| MSP430F1232IPWRG4.B              | Active        | Production           | TSSOP (PW)   28 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | M430F1232           |
| <a href="#">MSP430F1232IRHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1232     |
| MSP430F1232IRHBR.B               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1232     |
| MSP430F1232IRHBRG4               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1232     |
| MSP430F1232IRHBRG4.B             | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1232     |
| <a href="#">MSP430F1232IRHBT</a> | Active        | Production           | VQFN (RHB)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1232     |

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| MSP430F1232IRHBT.B    | Active        | Production           | VQFN (RHB)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | MSP430<br>F1232     |

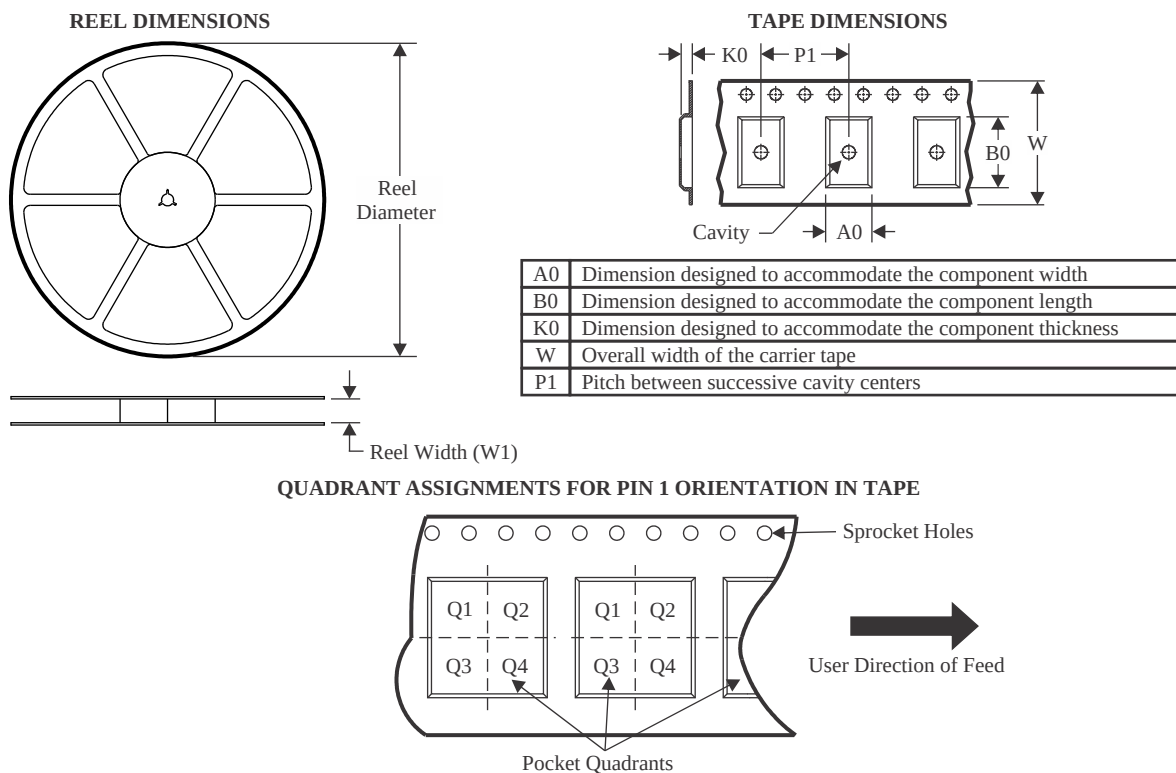
- (1) Status:** For more details on status, see our [product life cycle](#).
- (2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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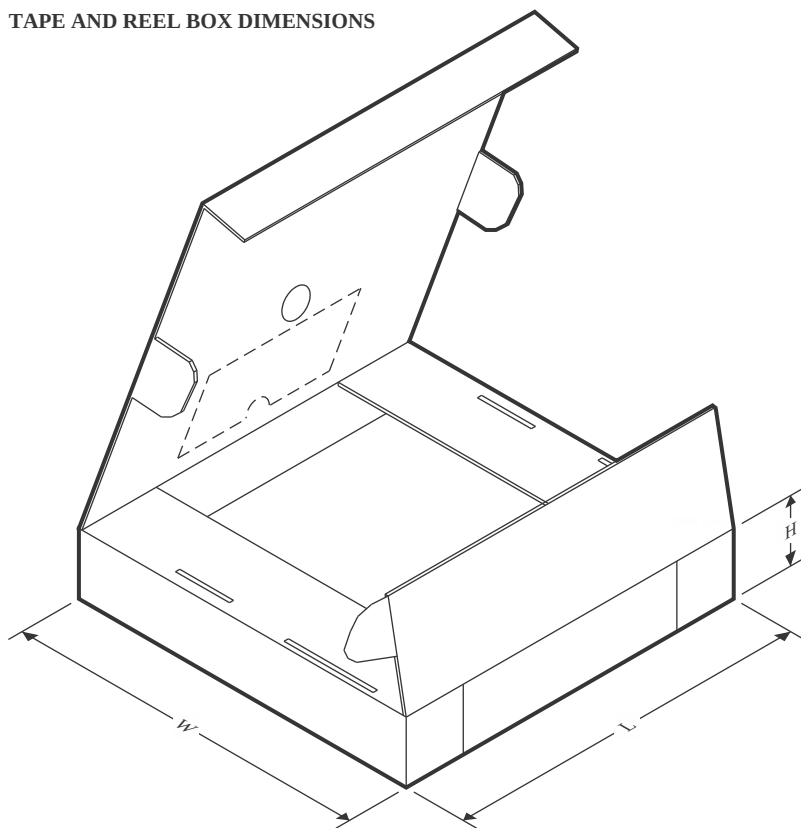
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F1122IDWR    | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| MSP430F1122IPWR    | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| MSP430F1122IRHBT   | VQFN         | RHB             | 32   | 250  | 180.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |
| MSP430F1132IDWR    | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| MSP430F1132IPWR    | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| MSP430F1132IRHBR   | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |
| MSP430F1132IRHBT   | VQFN         | RHB             | 32   | 250  | 180.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |
| MSP430F1222IDWR    | SOIC         | DW              | 28   | 1000 | 330.0              | 32.4               | 11.35   | 18.67   | 3.1     | 16.0    | 32.0   | Q1            |
| MSP430F1222IPWR    | TSSOP        | PW              | 28   | 2000 | 330.0              | 16.4               | 6.9     | 10.2    | 1.8     | 12.0    | 16.0   | Q1            |
| MSP430F1222IRHBR   | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |
| MSP430F1222IRHBT   | VQFN         | RHB             | 32   | 250  | 180.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |
| MSP430F1232IDWR    | SOIC         | DW              | 28   | 1000 | 330.0              | 32.4               | 11.35   | 18.67   | 3.1     | 16.0    | 32.0   | Q1            |
| MSP430F1232IPWR    | TSSOP        | PW              | 28   | 2000 | 330.0              | 16.4               | 6.9     | 10.2    | 1.8     | 12.0    | 16.0   | Q1            |
| MSP430F1232IRHBR   | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |
| MSP430F1232IRHBRG4 | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |
| MSP430F1232IRHBT   | VQFN         | RHB             | 32   | 250  | 180.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |

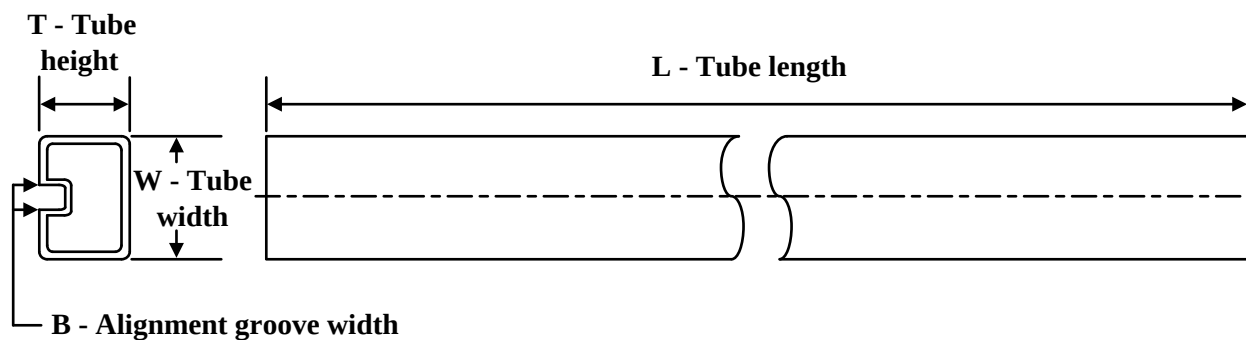
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F1122IDWR    | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| MSP430F1122IPWR    | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| MSP430F1122IRHBT   | VQFN         | RHB             | 32   | 250  | 213.0       | 191.0      | 35.0        |
| MSP430F1132IDWR    | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| MSP430F1132IPWR    | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| MSP430F1132IRHBR   | VQFN         | RHB             | 32   | 3000 | 356.0       | 356.0      | 35.0        |
| MSP430F1132IRHBT   | VQFN         | RHB             | 32   | 250  | 213.0       | 191.0      | 35.0        |
| MSP430F1222IDWR    | SOIC         | DW              | 28   | 1000 | 350.0       | 350.0      | 66.0        |
| MSP430F1222IPWR    | TSSOP        | PW              | 28   | 2000 | 350.0       | 350.0      | 43.0        |
| MSP430F1222IRHBR   | VQFN         | RHB             | 32   | 3000 | 356.0       | 356.0      | 35.0        |
| MSP430F1222IRHBT   | VQFN         | RHB             | 32   | 250  | 210.0       | 185.0      | 35.0        |
| MSP430F1232IDWR    | SOIC         | DW              | 28   | 1000 | 350.0       | 350.0      | 66.0        |
| MSP430F1232IPWR    | TSSOP        | PW              | 28   | 2000 | 350.0       | 350.0      | 43.0        |
| MSP430F1232IRHBR   | VQFN         | RHB             | 32   | 3000 | 356.0       | 356.0      | 35.0        |
| MSP430F1232IRHBRG4 | VQFN         | RHB             | 32   | 3000 | 356.0       | 356.0      | 35.0        |
| MSP430F1232IRHBT   | VQFN         | RHB             | 32   | 250  | 210.0       | 185.0      | 35.0        |

## TUBE

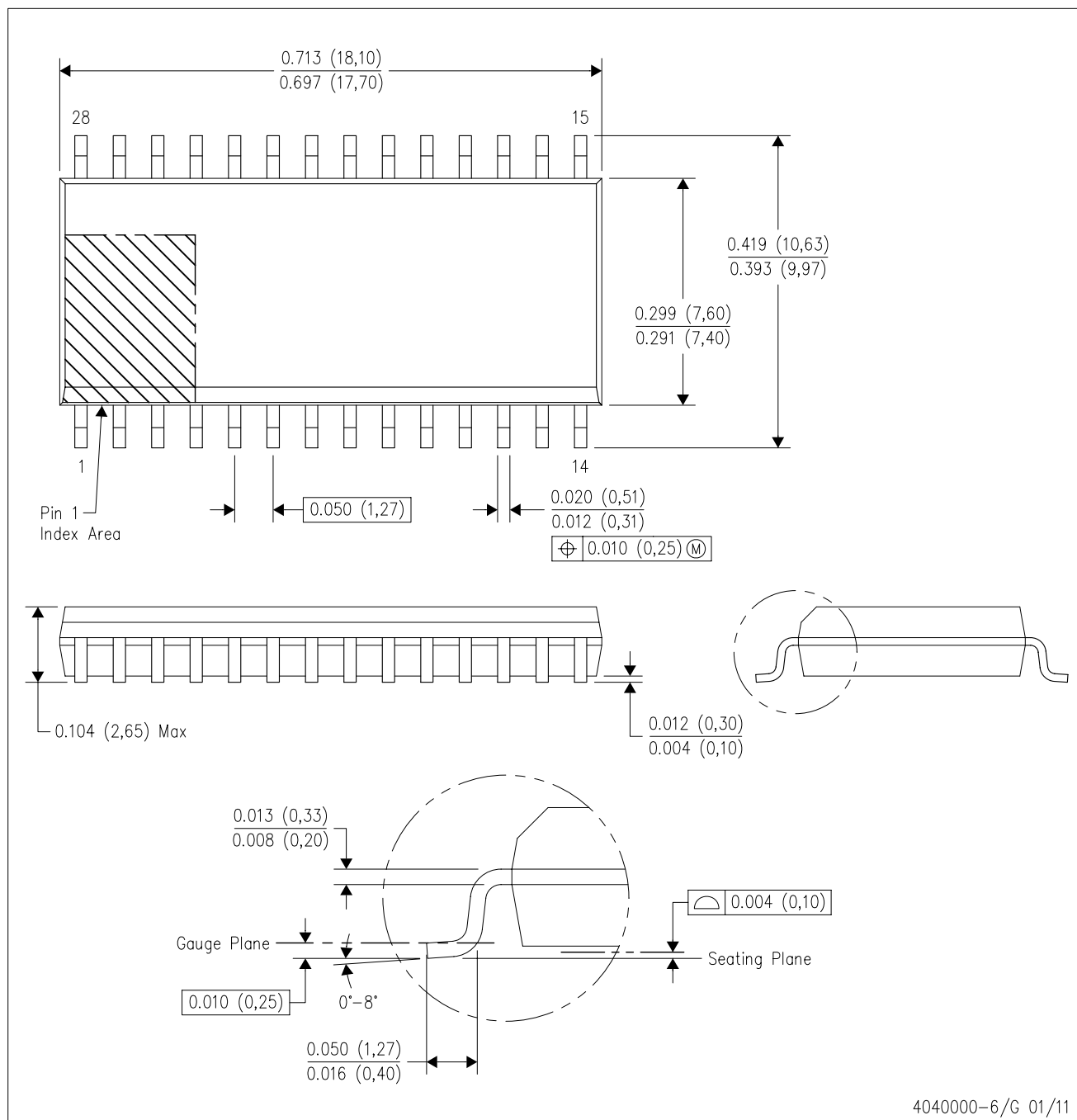


\*All dimensions are nominal

| Device           | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| MSP430F1122IDW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| MSP430F1122IDW.B | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| MSP430F1122IPW   | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| MSP430F1122IPW.B | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| MSP430F1132IDW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| MSP430F1132IDW.B | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| MSP430F1132IPW   | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| MSP430F1132IPW.B | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| MSP430F1222IDW   | DW           | SOIC         | 28   | 20  | 506.98 | 12.7   | 4826   | 6.6    |
| MSP430F1222IDW.B | DW           | SOIC         | 28   | 20  | 506.98 | 12.7   | 4826   | 6.6    |
| MSP430F1222IPW   | PW           | TSSOP        | 28   | 50  | 530    | 10.2   | 3600   | 3.5    |
| MSP430F1222IPW.B | PW           | TSSOP        | 28   | 50  | 530    | 10.2   | 3600   | 3.5    |
| MSP430F1232IDW   | DW           | SOIC         | 28   | 20  | 506.98 | 12.7   | 4826   | 6.6    |
| MSP430F1232IDW.B | DW           | SOIC         | 28   | 20  | 506.98 | 12.7   | 4826   | 6.6    |
| MSP430F1232IPW   | PW           | TSSOP        | 28   | 50  | 530    | 10.2   | 3600   | 3.5    |
| MSP430F1232IPW.B | PW           | TSSOP        | 28   | 50  | 530    | 10.2   | 3600   | 3.5    |

DW (R-PDSO-G28)

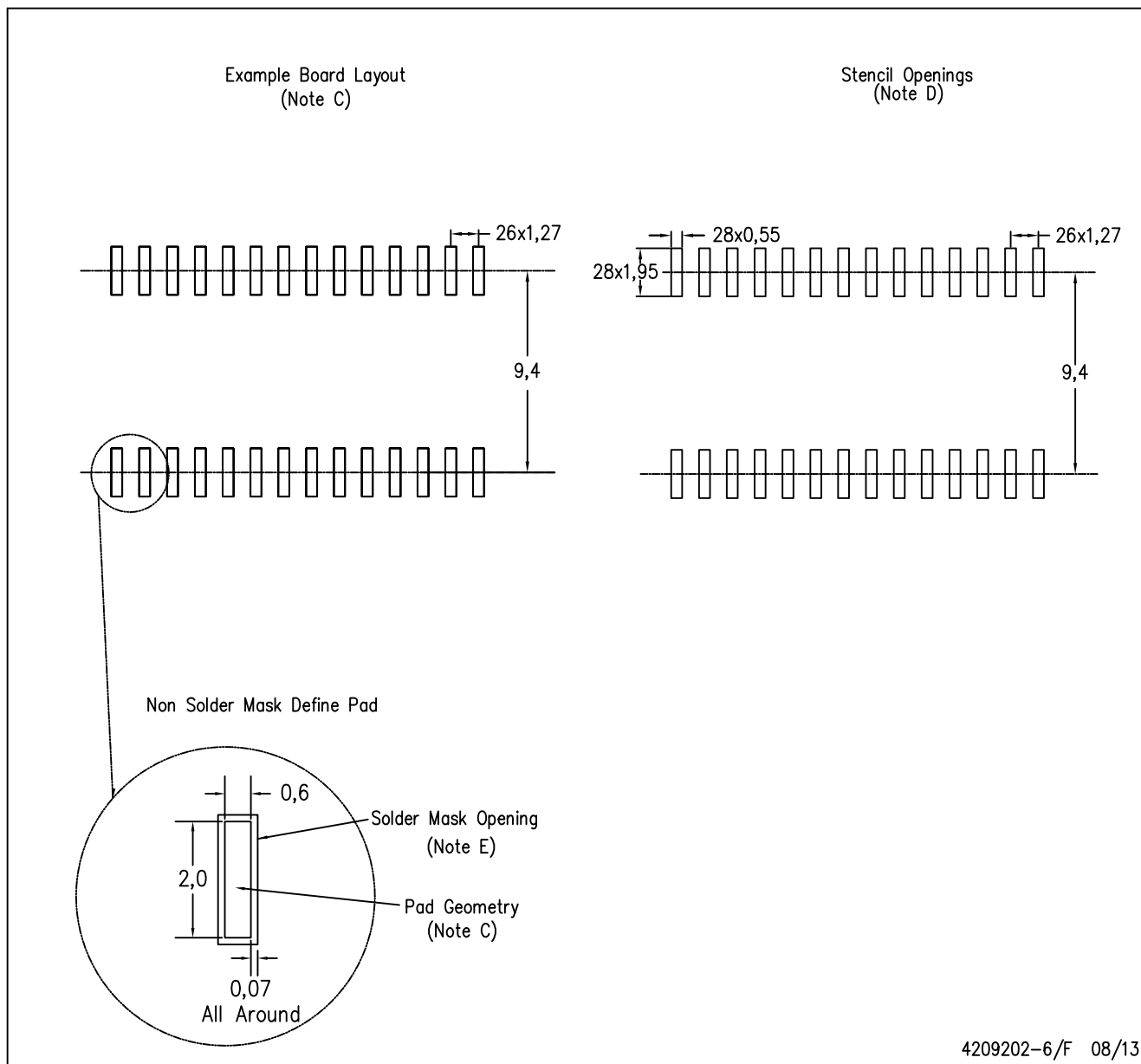
PLASTIC SMALL OUTLINE



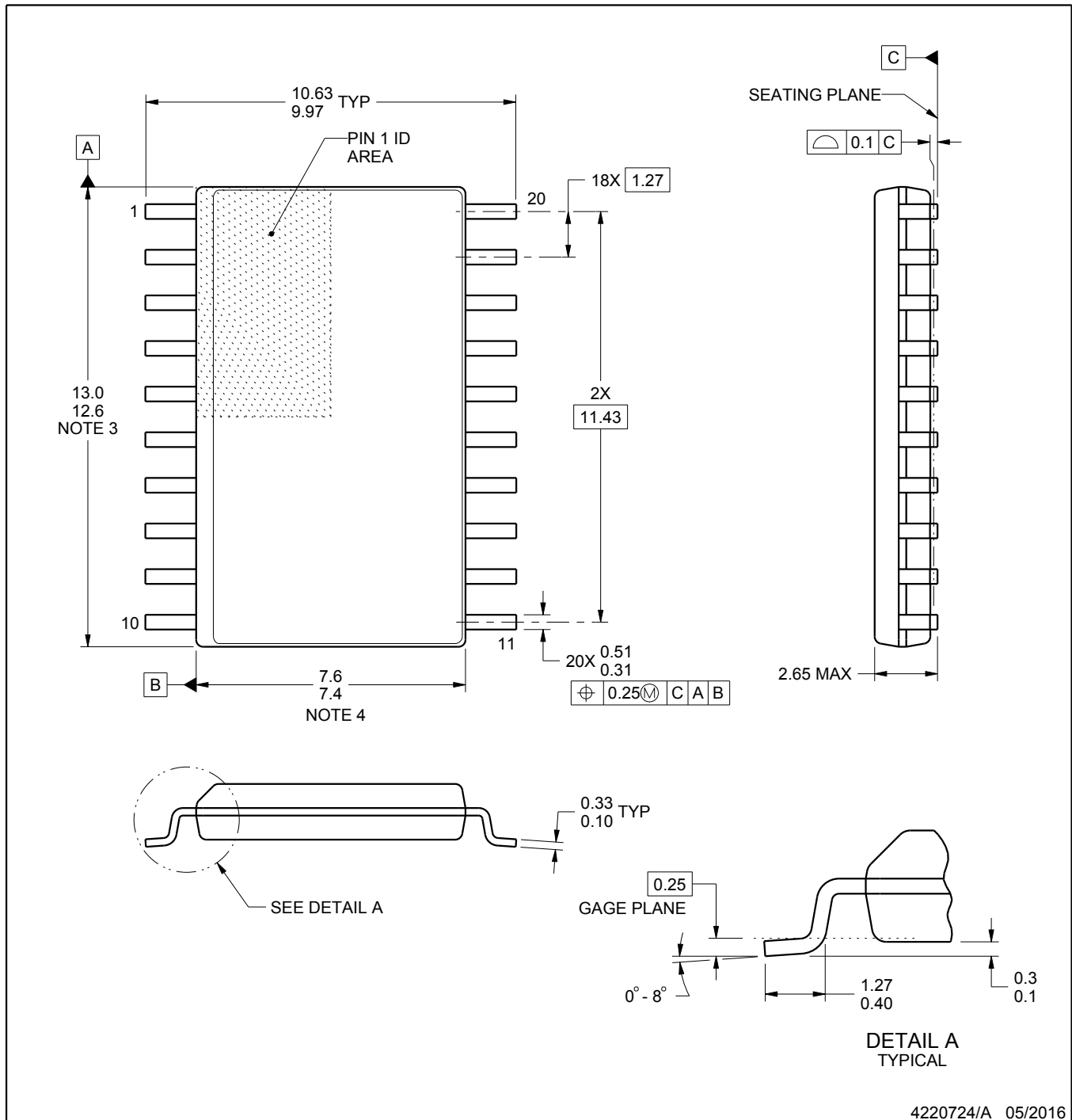
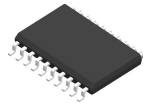
- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AE.

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## NOTES:

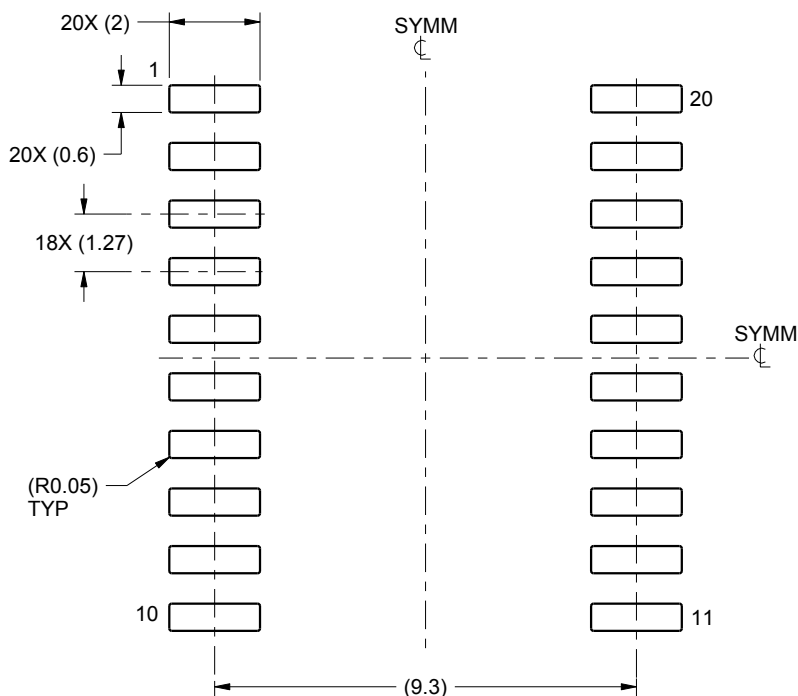
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

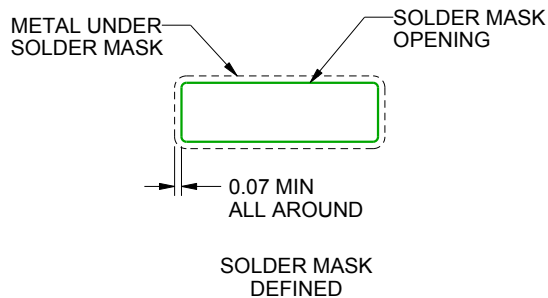
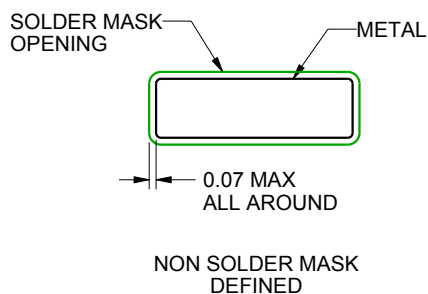
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

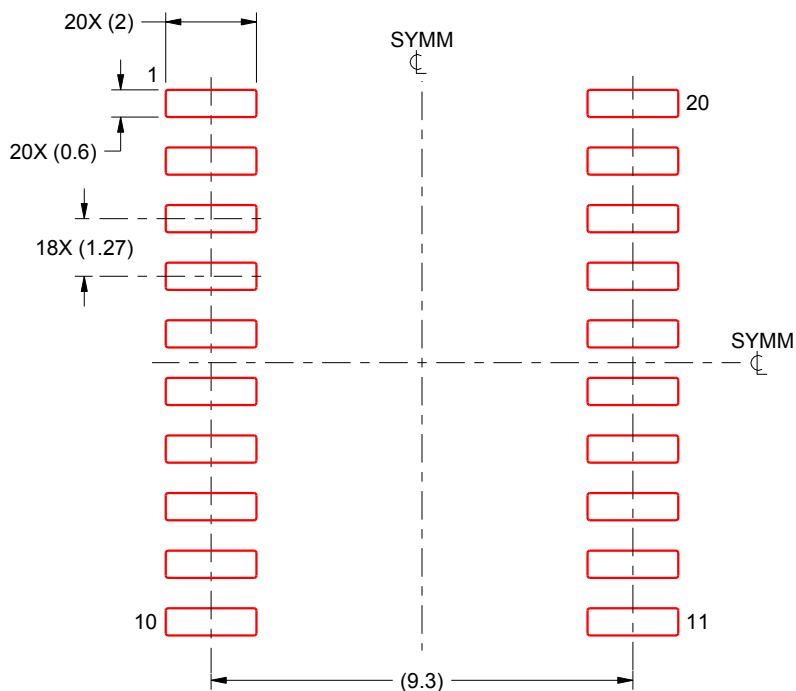
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

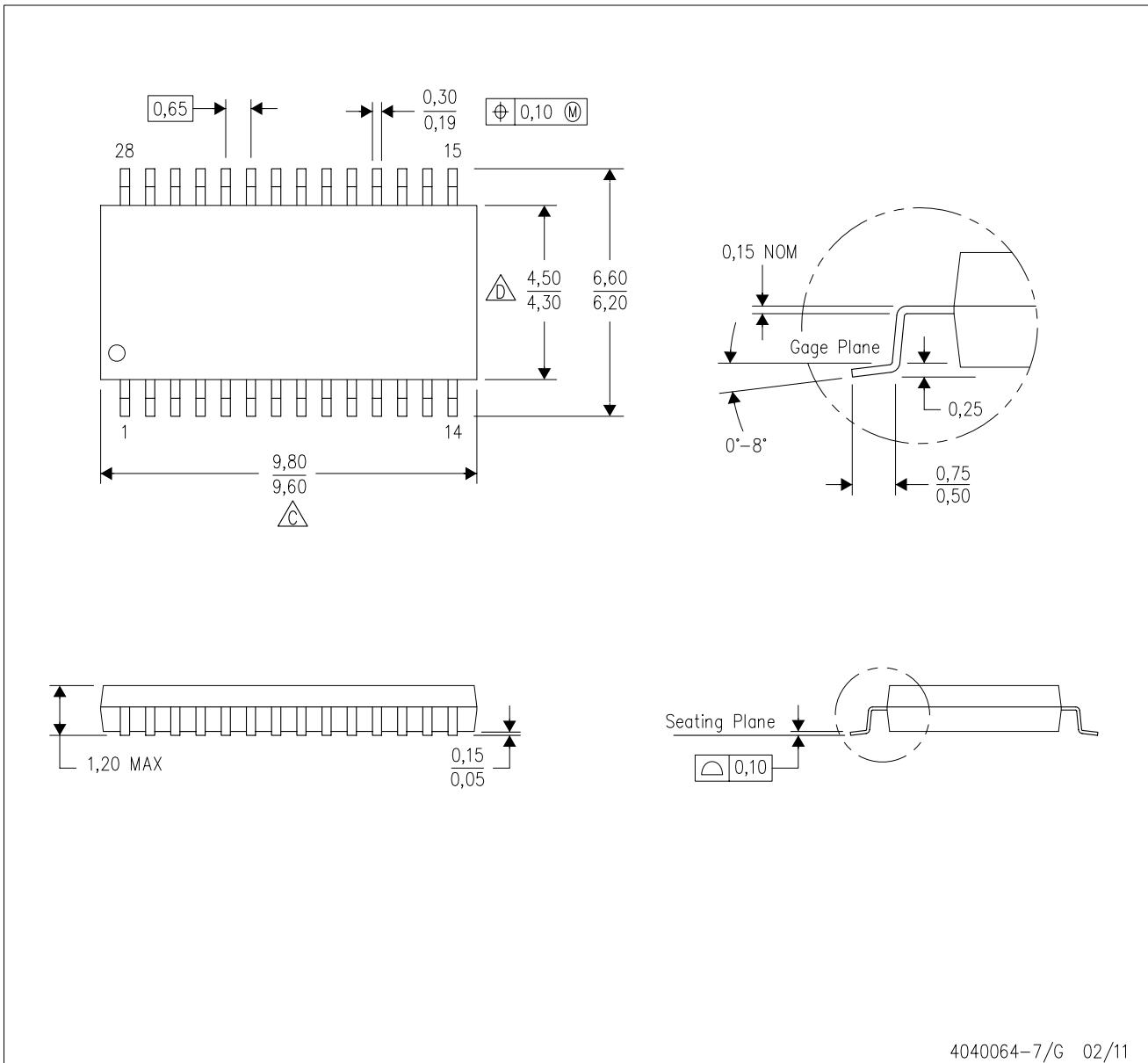
4220724/A 05/2016

NOTES: (continued)

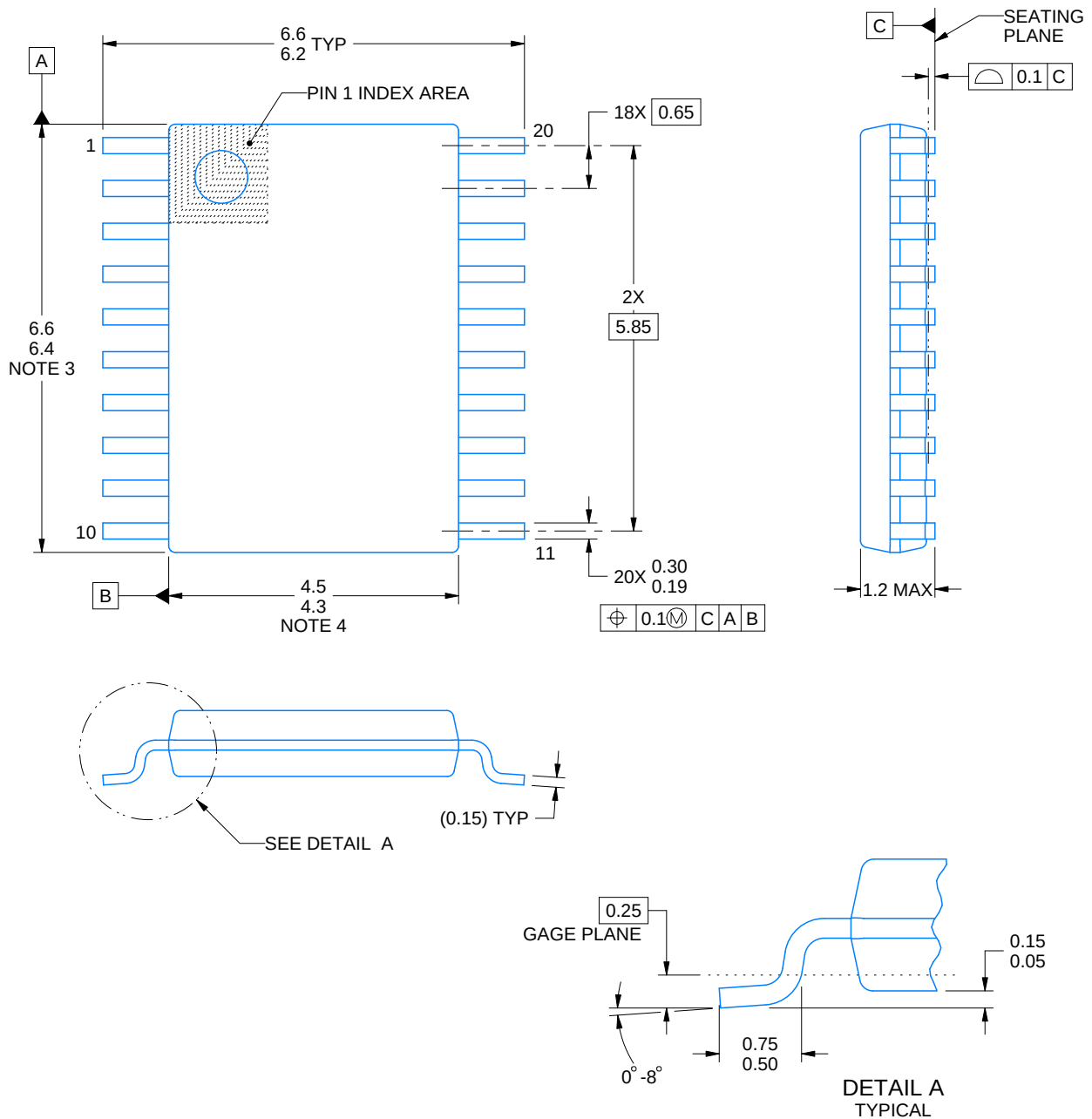
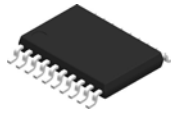
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



4220206/A 02/2017

## NOTES:

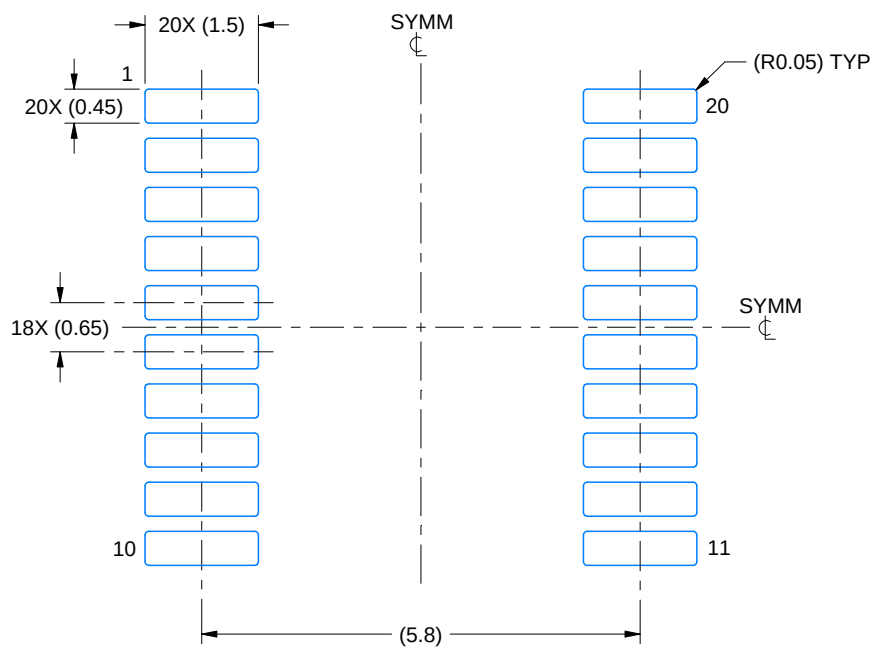
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

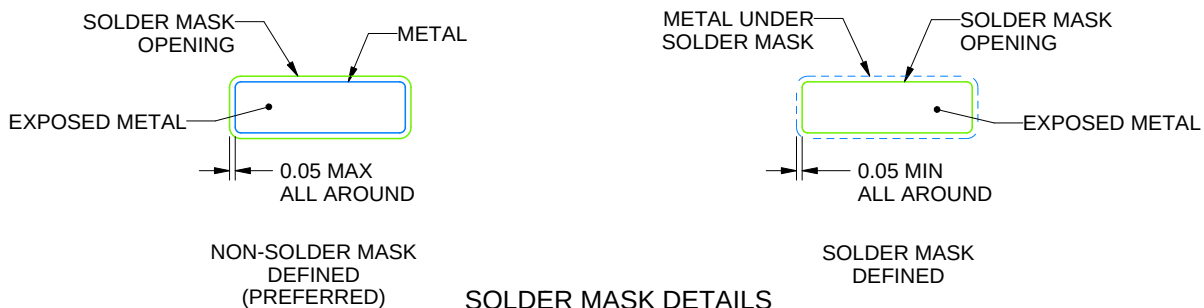
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

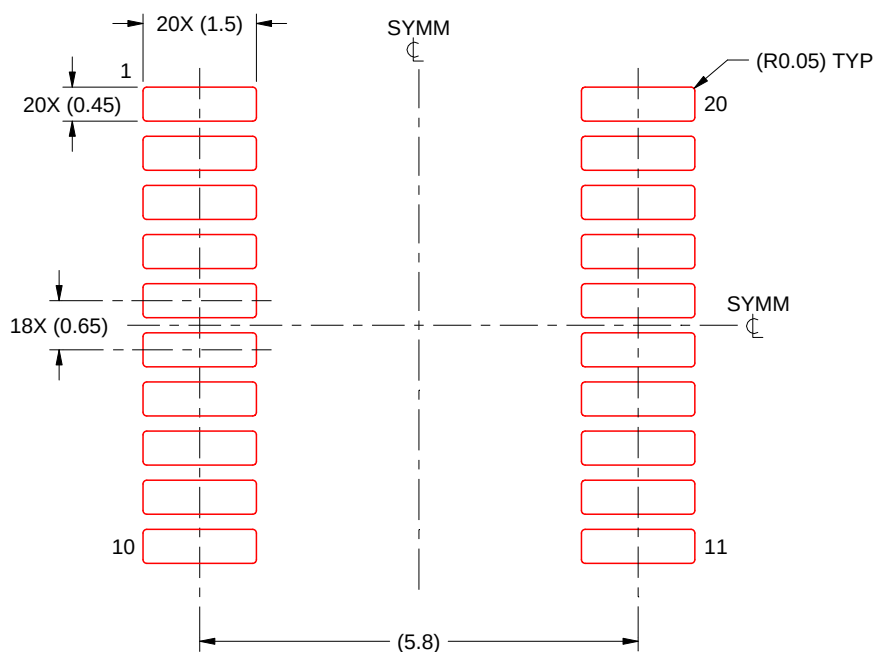
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

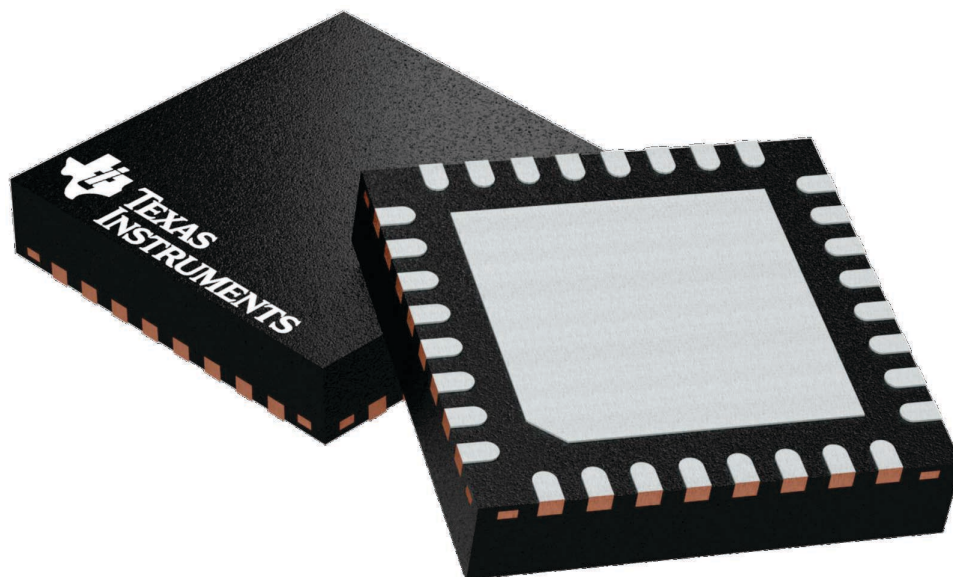
## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

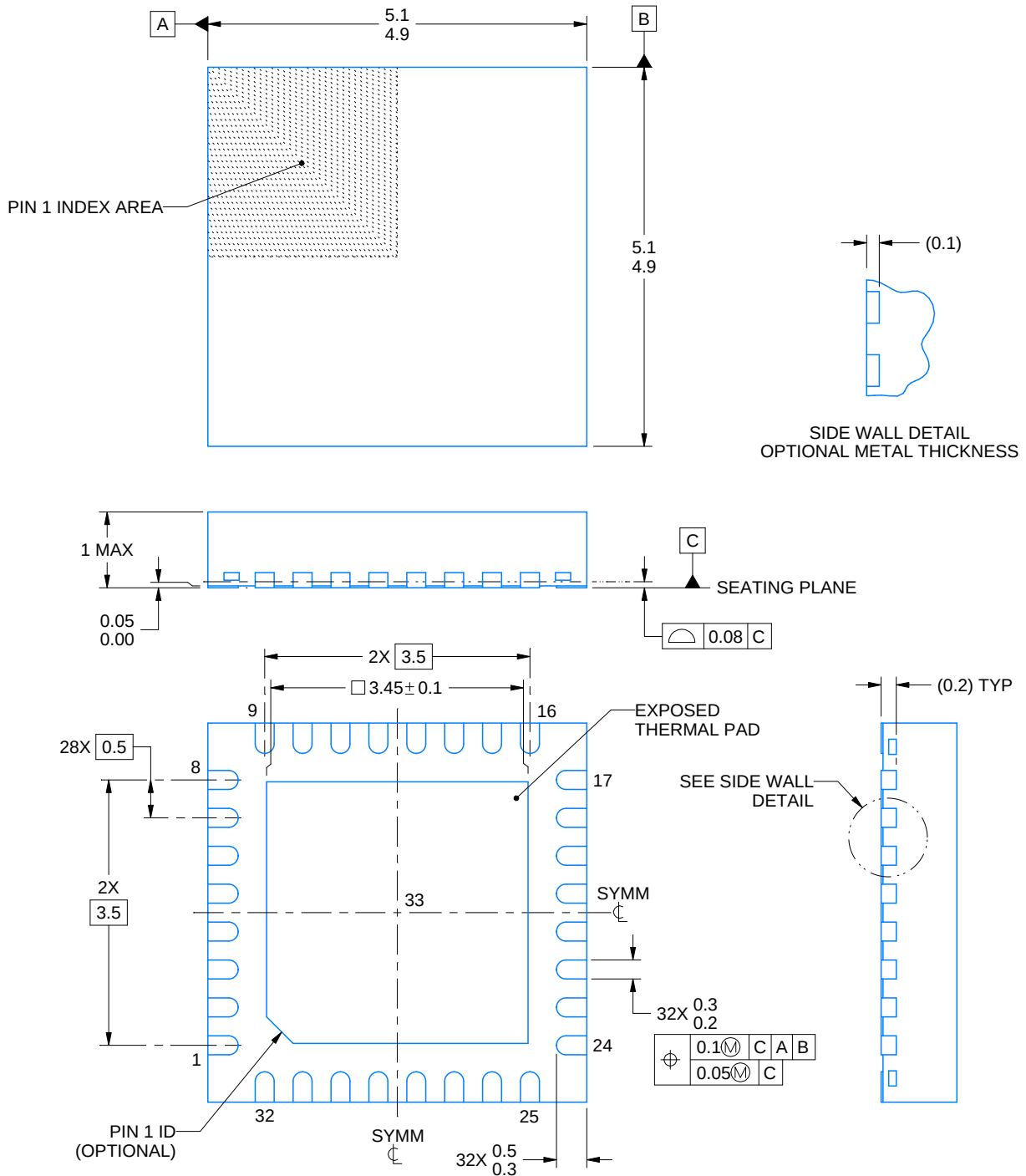
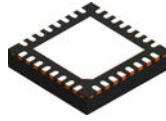
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224745/A



4223442/B 08/2019

## NOTES:

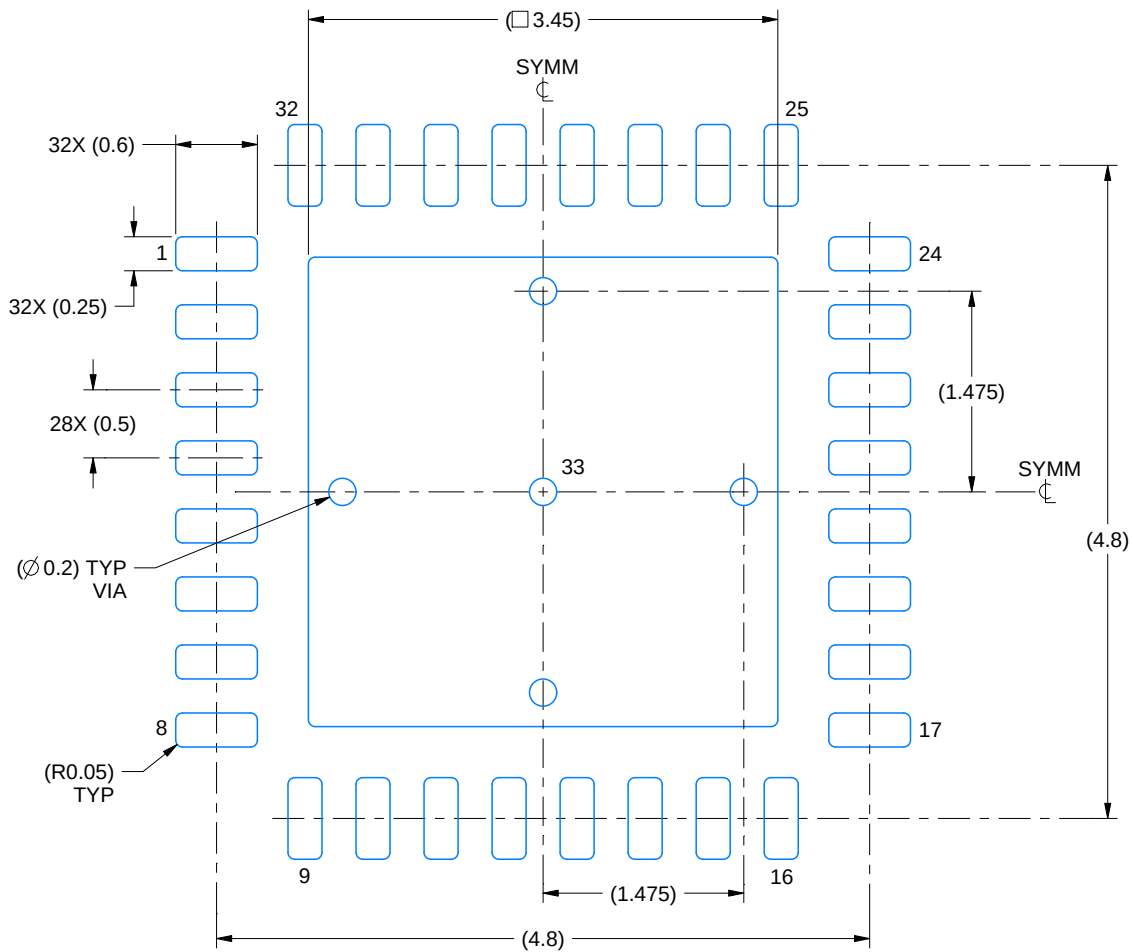
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

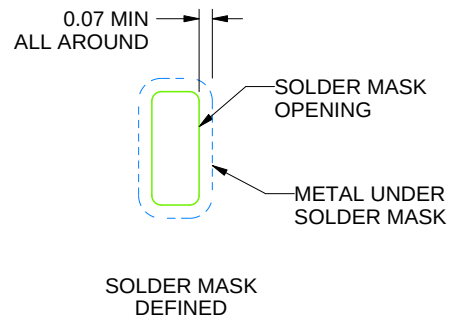
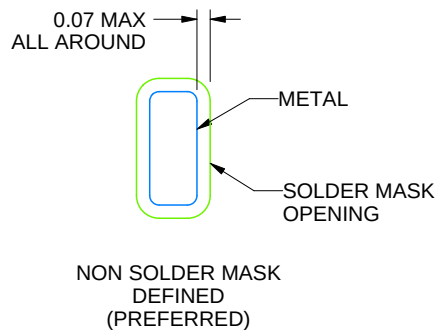
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:18X



SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

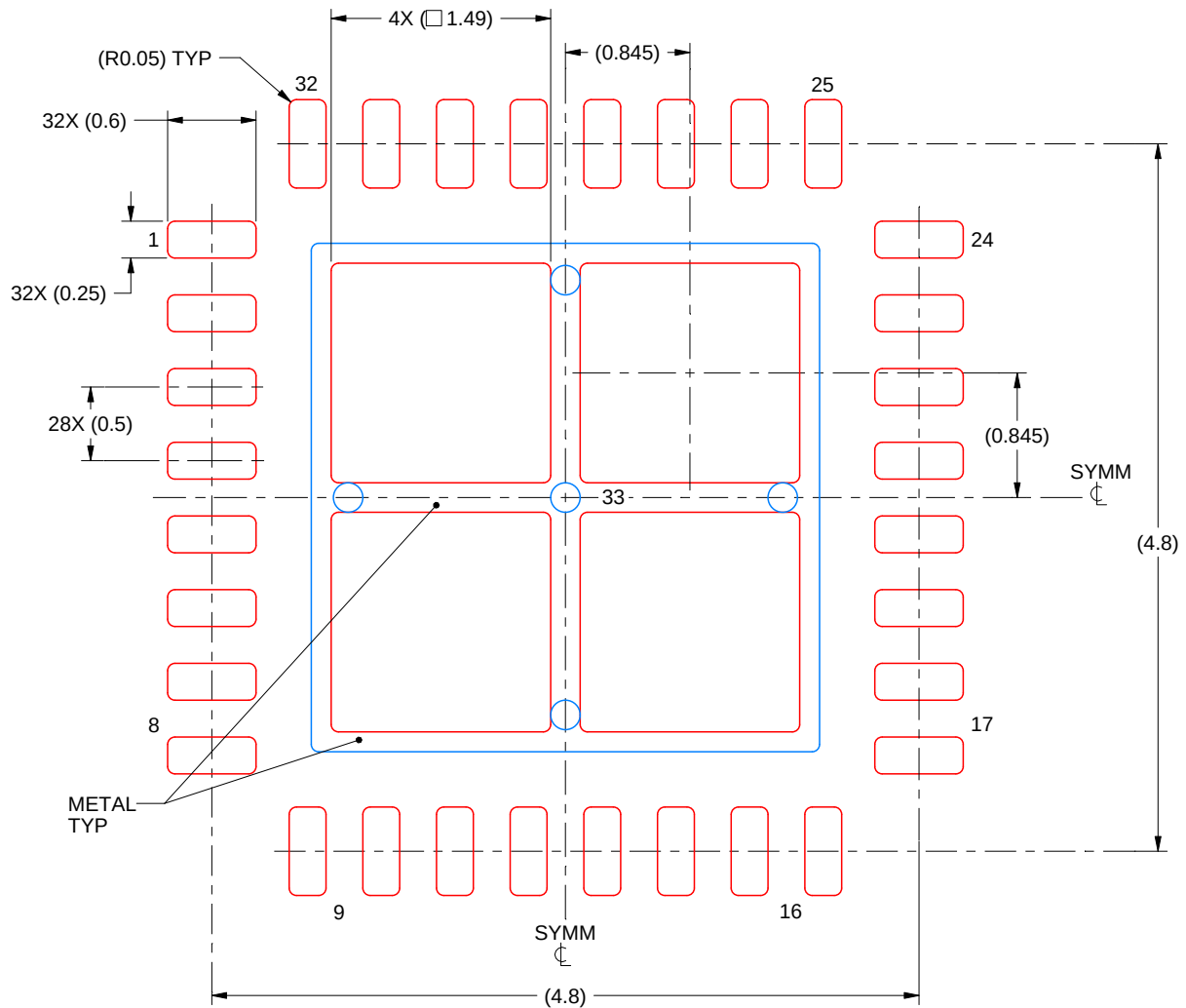
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:  
 75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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