

BQ77205 Overvoltage Protection for 3-Series to 5-Series Cell Li-Ion Batteries with Internal Delay Timer

1 Features

- 3-series cell to 5-series cell protection
- High-accuracy overvoltage protection
 - ± 10 mV at 25°C
 - ± 20 mV from 0°C to 60°C
- Overvoltage protection options from 3.55 V to 5.1 V
- Open-wire connection detection
- Random cell connection
- Functional safety-capable
- Fixed internal delay timers
- Fixed detection thresholds
- Fixed output drive type
 - Active high or active low
 - Active high drive to 6 V
 - Open drain with the ability to be pulled up externally to VDD
- Low power consumption $I_{CC} \approx 1 \mu\text{A}$ ($V_{\text{CELL(ALL)}} < V_{\text{OV}}$)
- Low leakage current per cell input < 100 nA with open wire detection disabled
- Package footprint options:
 - 8-pin DGK with 0.65-mm lead pitch

2 Applications

- Protection for Li-ion battery packs used in:
 - [Handheld garden tools](#)
 - [Handheld power tools](#)
 - [Cordless vacuum cleaners](#)
 - [UPS battery backup](#)
 - [Light electric vehicles \(eBike, eScooter, pedal-assist bicycles\)](#)

3 Description

The BQ77205 family of products provides a range of voltage and temperature monitoring, including overvoltage protection (OVP) and open-wire (OW) protection for Li-ion battery pack systems. Each cell is monitored independently for overvoltage and open-wire conditions.

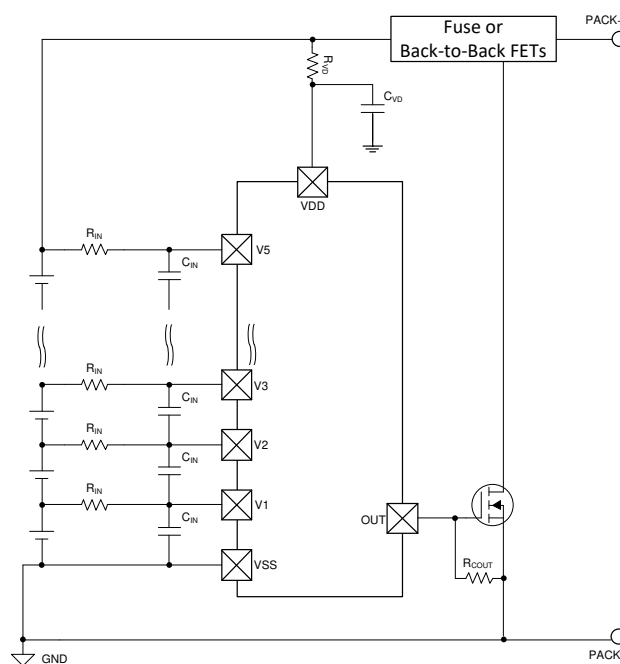
In the BQ77205 device, an internal delay timer is initiated upon detection of an overvoltage or open-wire condition. Upon expiration of the delay timer, the respective output is triggered into its active state (either high or low, depending on the configuration).

The overvoltage triggers the OUT pin if a fault is detected. If an open-wire fault is detected, then the OUT is triggered. For quicker production-line testing, the BQ77205 device provides a Customer Test Mode (CTM) with significantly reduced delay time.

Device Information Table

PART NUMBER	PACKAGE ⁽²⁾	PACKAGE SIZE
BQ77205xy ⁽¹⁾	VSSOP (DGK-8)	5.0 mm × 3.0 mm

- (1) Contact TI for more information.
- (2) For available catalog packages, see the orderable addendum at the end of the data sheet and the [Device Comparison Table](#).



Simplified Schematic



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4 Device Comparison Table

Part Number	T _A	Package	Package Designator	OVP (V)	OV Hysteresis (V)	Output Delay (s)	OW	Latch	Output Drive	Tape and Reel
BQ7720500	–40°C to 110°C	8-Pin VSSOP	DGK	4.2	0.050	1	Enabled	Disabled	Active Low	BQ7720500DGKR
BQ7720501	–40°C to 110°C	8-Pin VSSOP	DGK	4.275	0.050	2	Enabled	Disabled	Active Low	BQ7720501DGKR
BQ77205xy	–40°C to 110°C	8-Pin VSSOP	DGK	3.55V - 5.1V	0.050, 0.100	0.25, 0.5, 1, 2, 4	Enabled, Disabled	Enabled, Disabled	Active Low, Active High 6V, Active High VDD, Active Open-Drain Inactive Pulldown	TBD

5 Pin Configuration and Functions

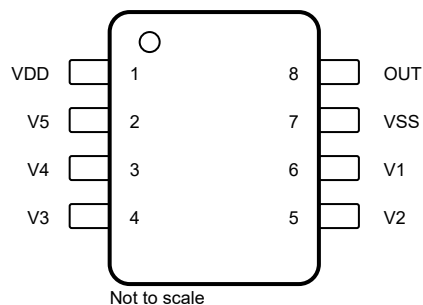


Figure 5-1. Pinout Diagram

Table 5-1. Pin Functions

NO.	NAME	TYPE (1)	DESCRIPTION
1	VDD	P	Power supply
2	V5	I	Sense input for positive voltage of the fifth cell from the bottom of the stack
3	V4	I	Sense input for positive voltage of the fourth cell from the bottom of the stack
4	V3	I	Sense input for positive voltage of the third cell from the bottom of the stack
5	V2	I	Sense input for positive voltage of the second cell from the bottom of the stack
6	V1	I	Sense input for positive voltage of the first cell from the bottom of the stack
7	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
8	OUT	O	Output drive for overvoltage, open wire

(1) I = Input, O = Output, P = Power Connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage range	VDD – VSS ⁽¹⁾	–0.3	30	V
Input voltage range	V _n – VSS where n = 1 to 5	–0.3	30	V
Output voltage range	OUT – VSS	–0.3	30	V
Functional temperature, T _{FUNC}		–40	110	°C
Storage temperature, T _{STG}		–65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) DC Voltage applied on this pin should be limited to a maximum of 40 V. Stresses to this pin at voltages beyond this level, up to the 45-V specified maximum level, should be limited to short transients.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage ⁽¹⁾	5		27.5	V
V _{IN}	Input voltage range of V _n – V _{n-1} where n = 2 to 5 and V ₁ – VSS	0		5	V
V _{CTM}	Customer Test Mode Entry V _{DD} > V ₅ + V _{CTM}	12		13	V
T _A	Ambient temperature	–40		85	°C
T _J	Junction temperature	–65		150	°C

- (1) V_{DD} is equal to top-of-stack voltage.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		BQ77205	UNIT
		DGK	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	180	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	55	°C/W
R _{θJB}	Junction-to-board thermal resistance	130	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	12.3	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	96.7	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		BQ77205	UNIT
		DGK	
		8 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 DC Characteristics

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{DD} = 18\text{ V}$, MIN/MAX values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{DD} = 5\text{ V}$ to 27.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERVOLTAGE PROTECTION (OV)						
V _{OV}	OV Detection Range		3.55		5.1	V
V _{OV_STEP}	OV Detection Steps			25		mV
V _{OV_HYS}	OV Detection Hysteresis	Selected OV Hysteresis depends on the part number. See the device selection table for details.		V _{OV} – 50		mV
		Selected OV Hysteresis depends on the part number. See the device selection table for details.		V _{OV} – 100		mV
V _{OV_ACC}	OV Detection Accuracy	T _A = 25°C	–10		10	mV
	OV Detection Accuracy	0°C ≤ T _A ≤ 60°C	–20		20	mV
	OV Detection Accuracy	–40°C ≤ T _A ≤ 110°C	–50		50	mV
OPEN-WIRE PROTECTION (OW)						
V _{OW}	OW Detection Threshold	V _n < V _{n-1} where n = 2 to 5		–200		mV
		V1 – VSS		500		mV
V _{OW_HYS}	OW Detection Hysteresis	V _n < V _{n-1} where n = 1 to 5		V _{OW} +100		mV
V _{OW_ACC}	OW Detection Accuracy	–40 °C ≤ T _A ≤ 110°C	–25		25	mV
SUPPLY AND LEAKAGE CURRENT						
I _{CC}	Supply Current	No fault detected		2	2.5	μA
I _{IN} ⁽¹⁾	Input Current at Vx Pins	V _n – V _{n-1} and V1 – VSS = 4 V, where n = 2 to 5, Open Wire Enabled	–0.3		0.3	μA
		V _n – V _{n-1} and V1 – VSS = 4 V, where n = 2 to 5, Open Wire Disabled	–0.1		0.1	μA
OUTPUT DRIVE, OUT pin, CMOS ACTIVE HIGH VERSIONS ONLY						
V _{OUT_AH}	Output Drive Voltage for OUT, Active High 6 V	V _n – V _{n-1} or V1 – VSS > V _{OV} , where n = 2 to 5, VDD = 18 V, I _{OH} = 100 μA measured out of the OUT pin	6			V
	Output Drive Voltage for OUT, Active High VDD	VDD – V _{OUT} , V _n – V _{n-1} or V1 – VSS > V _{OV} , where n = 2 to 5, I _{OH} = 10 μA measured out of the OUT pin	0	1	1.5	V
	Output Drive Voltage for DOUT, Active High 6 V	VDD – V _{OUT} , If 4 of 5 cells are short-circuited and only one cell remains powered and > V _{OV} , VDD = Vx (cell voltage), I _{OH} = 100 μA,	0	1	1.5	V
	Output Drive Voltage for OUT, Active High 6 V and VDD	V _n – V _{n-1} and V1 – VSS < V _{OV} , where n = 2 to 5, VDD = 18 V, I _{OH} = 100 μA measured into the pin		250	400	mV

6.5 DC Characteristics (continued)

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{DD} = 18\text{ V}$, MIN/MAX values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{DD} = 5\text{ V}$ to 27.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{OUT_AH}	Internal Pullup Resistor		80	100	120	k Ω
$I_{OUT_AH_H}$	OUT Source Current (during OV)	$V_n - V_{n-1}$ or $V_1 - V_{SS} > V_{OV}$, where $n = 2$ to 5 , $V_{DD} = 18\text{ V}$, $OUT = 0\text{ V}$. Measured out of the OUT pin			6.5	mA
$I_{OUT_AH_L}$	OUT Sink Current (no OV)	$V_n - V_{n-1}$ and $V_1 - V_{SS} < V_{OV}$, where $n = 2$ to 5 , $V_{DD} = 18\text{ V}$, $OUT = V_{DD}$. Measured into the OUT pin	0.3		3	mA
OUTPUT DRIVE, OUT pin, NCH OPEN DRAIN ACTIVE LOW VERSIONS ONLY						
V_{OUT_AL}	Output Drive Voltage for OUT, Active Low	$V_n - V_{n-1}$ or $V_1 - V_{SS} > V_{OV}$, where $n = 2$ to 5 , $V_{DD} = 18\text{ V}$, $I_{OH} = 100\text{ }\mu\text{A}$ measured into the OUT pin		250	400	mV
$I_{OUT_AL_L}$	OUT Source Current (during OV)	$V_n - V_{n-1}$ or $V_1 - V_{SS} > V_{OV}$, where $n = 2$ to 5 , $V_{DD} = 18\text{ V}$, $OUT = V_{DD}$. Measured into the OUT pin	0.3		3	mA
$I_{OUT_AL_H}$	OUT Sink Current (no OV)	$V_n - V_{n-1}$ and $V_1 - V_{SS} < V_{OV}$, where $n = 2$ to 5 , $V_{DD} = 18\text{ V}$, $OUT = V_{DD}$. Measured out of the OUT pin			100	nA

(1) Specified by design

6.6 Timing Requirements

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{DD} = 18\text{ V}$, MIN/MAX values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{DD} = 5\text{ V}$ to 27.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OV_DELAY}	OV Delay Time			0.25		s
				0.5		s
				1		s
				2		s
				4		s
t_{OW_DELAY}	OW Delay Time			4		s
t_{DELAY_ACC}	Delay Time Accuracy	For 0.25-s, 0.5-s delays	-128		128	ms
t_{DELAY_ACC}	Delay Time Accuracy	For 1-s delays	-150		150	ms
t_{DELAY_DR}	Delay time drift across operating temp	For all delays other than 0.25-s, 0.5-s, 1-s delays	-10%		10%	
t_{CTM_DELAY}	Fault Detection Delay Time during Customer Test Mode	See Customer Test Mode.		50		ms

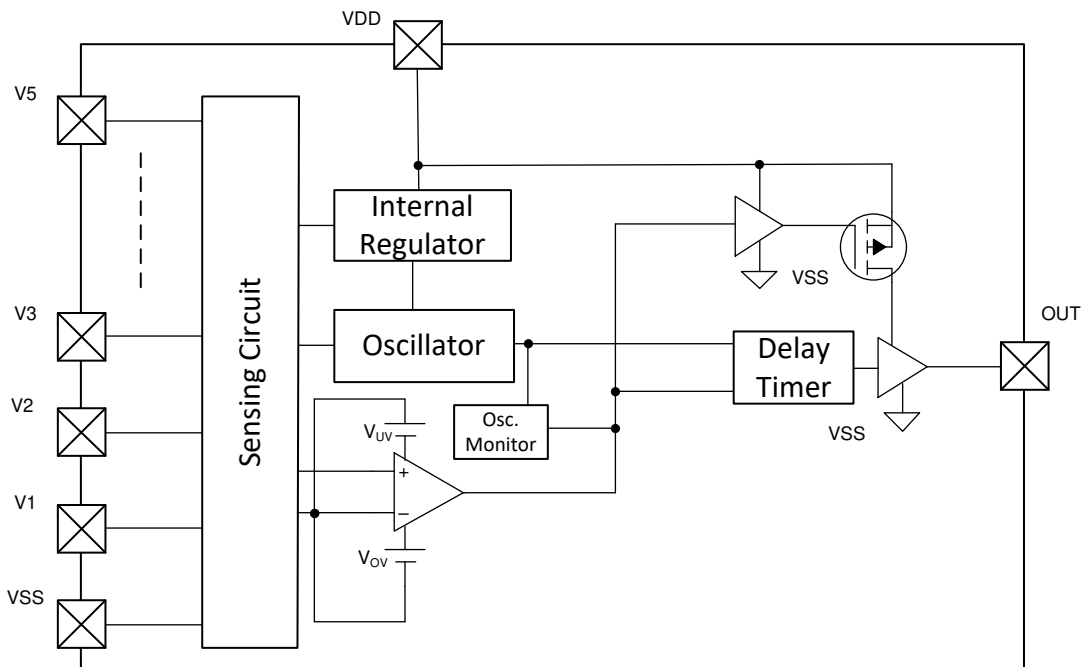
7 Detailed Description

7.1 Overview

The BQ77205 family of devices provides a range of voltage and temperature monitoring including overvoltage (OVP), open-wire (OW) protection for Li-ion battery pack systems. Each cell is monitored independently for overvoltage, and open-wire conditions. An internal delay timer is initiated upon detection of an overvoltage, open-wire, condition. Upon expiration of the delay timer, the respective output is triggered into its active state (either high or low depending on the configuration). The overvoltage triggers the OUT pin if a fault is detected. If an open-wire fault is detected, then the OUT is triggered.

For quicker production-line testing, the BQ77205 device provides a Customer Test Mode (CTM) with greatly reduced delay time.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Voltage Fault Detection

In the BQ77205 device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV} . If any cell voltage exceeds the programmed OV value, a timer circuit is activated. When the timer expires, the OUT pin goes from inactive to active state. The timer is reset if the cell voltage falls below the recovery threshold ($V_{OV} - V_{OV_HYS}$).

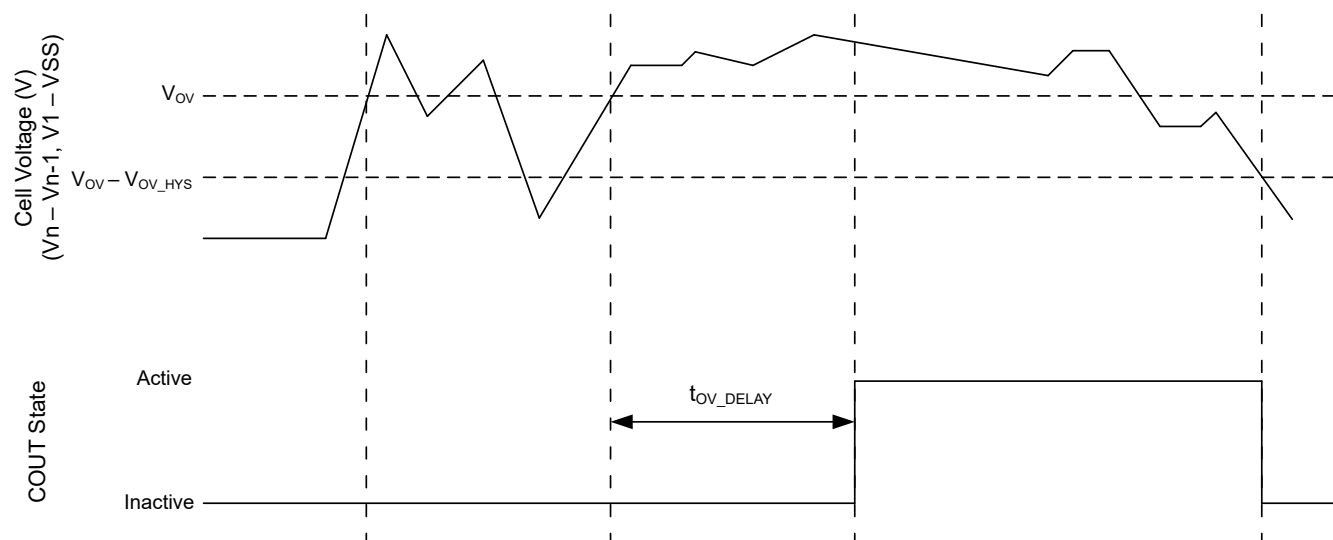


Figure 7-1. Timing for Overvoltage Sensing

7.3.2 Open Wire Fault Detection

In the BQ77205 device, each cell input is monitored independently to determine if the input is connected to a cell or not by applying a 50- μ A pulldown current to ground that is activated for 128 μ s every 128 ms. If the device detects that $V_n < V_{n-1} - V_{OV}$ V, then a timer is activated. When the timer expires, the OUT pin goes from an inactive to active state. The timer is reset if the cell input rises above the recovery threshold ($V_{OV} + V_{OV_HYS}$). To recover the OUT output from active to inactive state, the open wire fault must be cleared (such as the broken connection from the device to the battery needs to be restored), and any other remaining faults (such as existing OVP fault) need to be cleared as well.

7.3.3 Oscillator Health Check

The device can detect if the internal oscillator slows down below the f_{OSC_FAULT} threshold. When this occurs then the OUT goes from inactive to active state. If the oscillator returns to normal then the fault recovers.

7.3.4 Sense Positive Input for V_x

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input are required for noise filtering and stable voltage monitoring.

7.3.5 Output Drive, OUT

This pin serves as the fault signal output and may be ordered in either active HIGH with drive to 6 V or active LOW options configured through internal OTP.

The OUT responds per the following table when a fault is detected if the specific fault is enabled.

Table 7-1. Fault Detection vs OUT Action

FAULT DETECTED	OUT
Overvoltage	Active
Open Wire	Active
Oscillator Health	Active

7.3.6 The LATCH Function

The device can be enabled to latch the fault signal, which effectively disables the recovery functions of all fault detections. The only way to recover from a fault state when the latch is enabled is a POR of the device.

7.3.7 Supply Input, VDD

This pin is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

7.4 Device Functional Modes

7.4.1 NORMAL Mode

When OUT is inactive (no fault detected) the device operates in NORMAL mode and device is monitoring for voltage and open wire faults.

The OUT pin is inactive and if configured:

- Active high is low.
- Active low is being externally pulled up and is an open drain.

7.4.2 FAULT Mode

FAULT mode is entered if the OUT pin is activated. The OUT pin will either pull high internally, if configured as active high, or will be pulled low internally, if configured as active low. When OUT is deactivated the device returns to NORMAL mode.

7.4.3 Customer Test Mode

Customer Test Mode (CTM) helps to reduce test time for checking the delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least V_{CTM} higher than V5 (see [Figure 7-2](#)). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to a V5 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages ($V_{Cn}-V_{Cn-1}$) and ($V1-VSS$). Stressing the pins beyond the rated limits may cause permanent damage to the device.

[Figure 7-2](#) shows the timing for the Customer Test Mode.

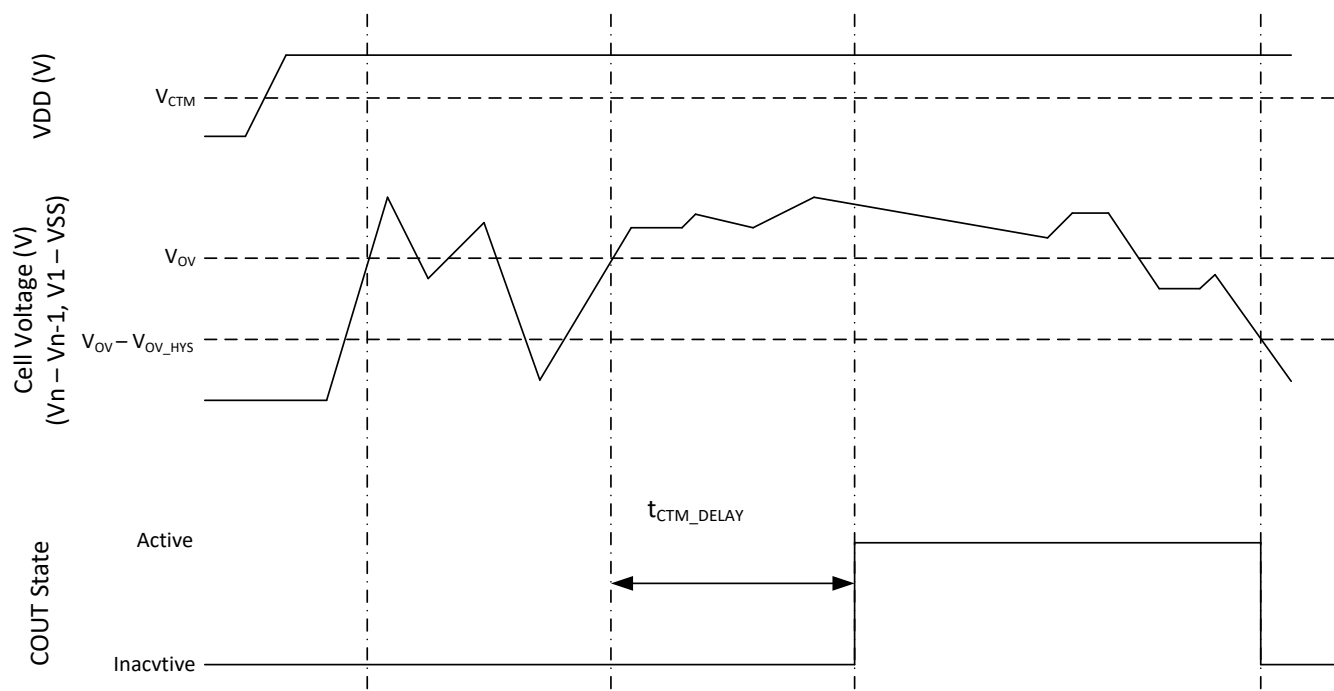


Figure 7-2. Timing for Customer Test Mode

Table 8-1. Parameters (continued)

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Supply voltage filter resistance	R_{VD}	100	300	1K	Ω
Supply voltage filter capacitance	C_{VD}	0.05	0.1	1	μF

Note

The device is calibrated using an R_{IN} value = 1 k Ω . Using a value other than this recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

8.1.2 Detailed Design Procedure

Figure 8-2 shows the measurement for current consumption for the product for both VDD and Vx.

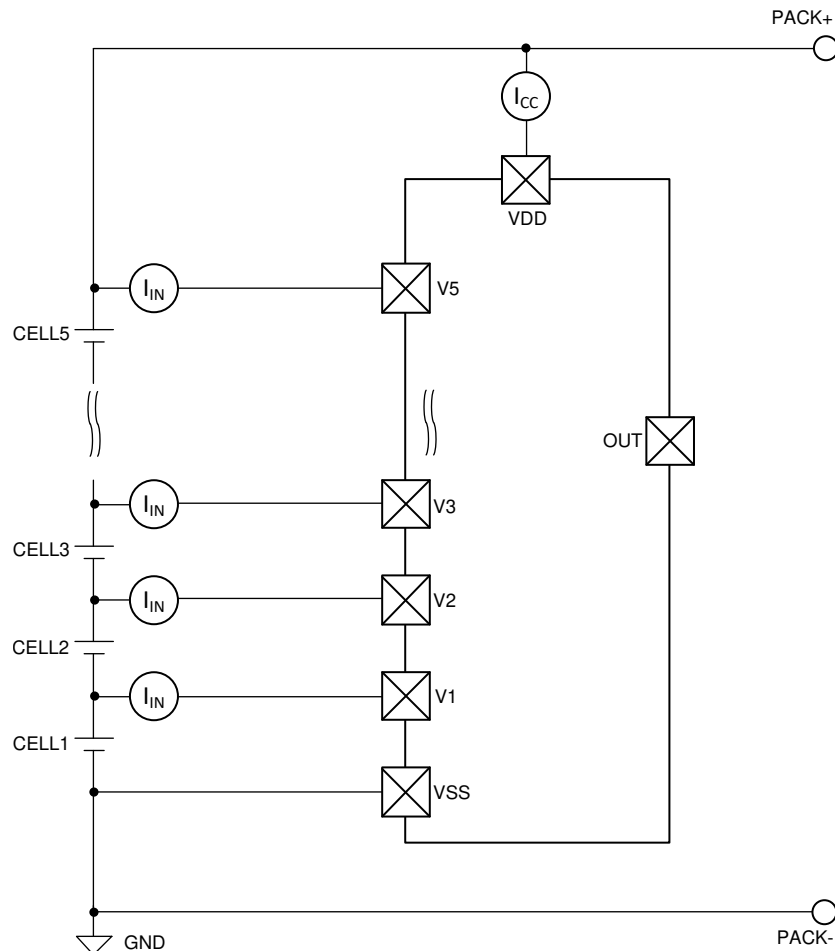


Figure 8-2. Configuration for IC Current Consumption Test

8.1.2.1 Cell Connection Sequence

The BQ77205 device can be connected to the array of cells in any order without damaging the device.

During cell attachment, the device could detect a fault if the cells are not connected within a fault detection delay period. If this occurs, then OUT could transition from inactive to active. OUT can be tied to VSS or VDD to prevent any change in output state during cell attach.

8.2 Systems Example

In this application example, the choice of a FUSE or FETs is required on the OUT pin — configured as an active high drive to 6-V outputs.

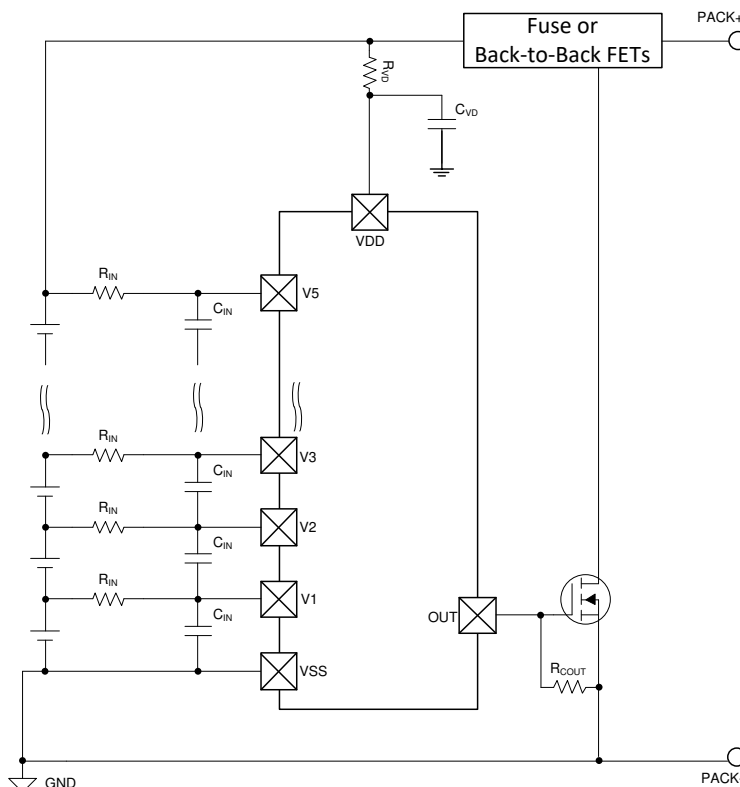


Figure 8-3. 5-Series Cell Configuration with Active High 6-V Option

9 Power Supply Recommendations

The maximum power supply of this device is 30 V on VDD.

10 Layout

10.1 Layout Guidelines

- Verify
 - the RC filters for the Vn and VDD pins are placed as close as possible to the target terminal.
- Route the VSS pin to the CELL– terminal.

10.2 Layout Example

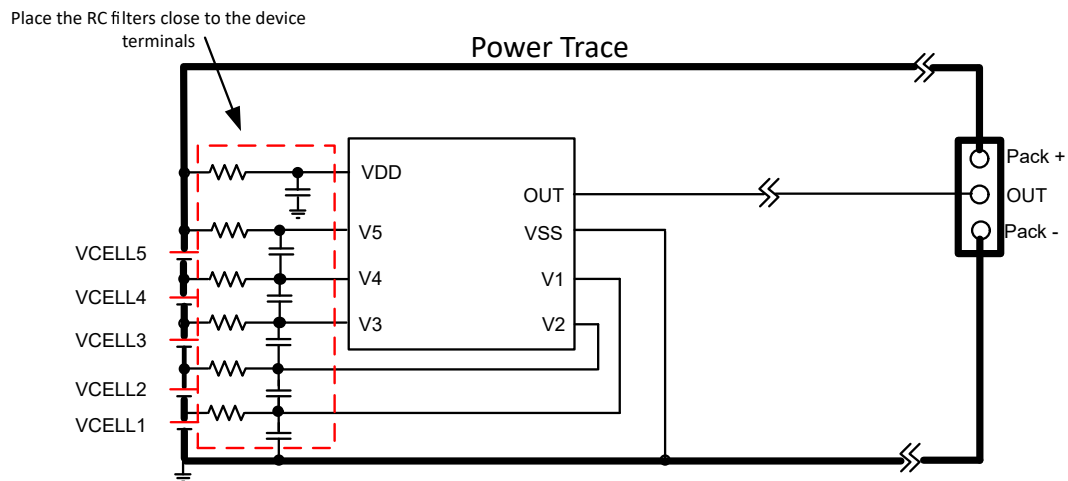


Figure 10-1. Example Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

Changes from Revision * (October 2023) to Revision A (June 2024)	Page
• Updated Device Information Table.....	1
• Updated Device Comparison Table.....	3

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ7720500DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-2-260C-1 YEAR	-40 to 85	2PBS
BQ7720500DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2PBS
BQ7720501DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3IMS
BQ7720501DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3IMS

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ7720500DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
BQ7720501DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

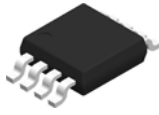
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ7720500DGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
BQ7720501DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0

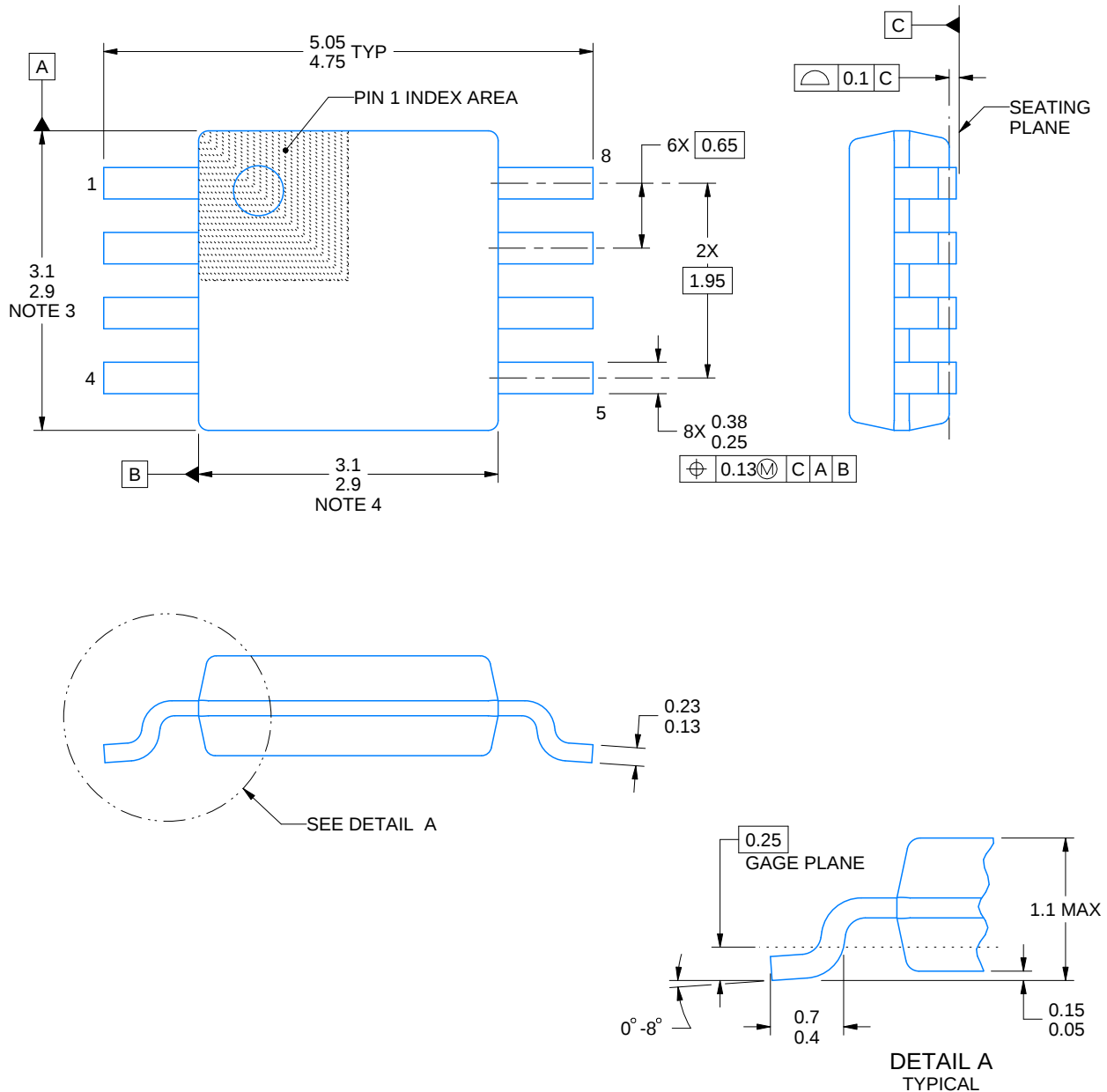
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

PowerPAD is a trademark of Texas Instruments.

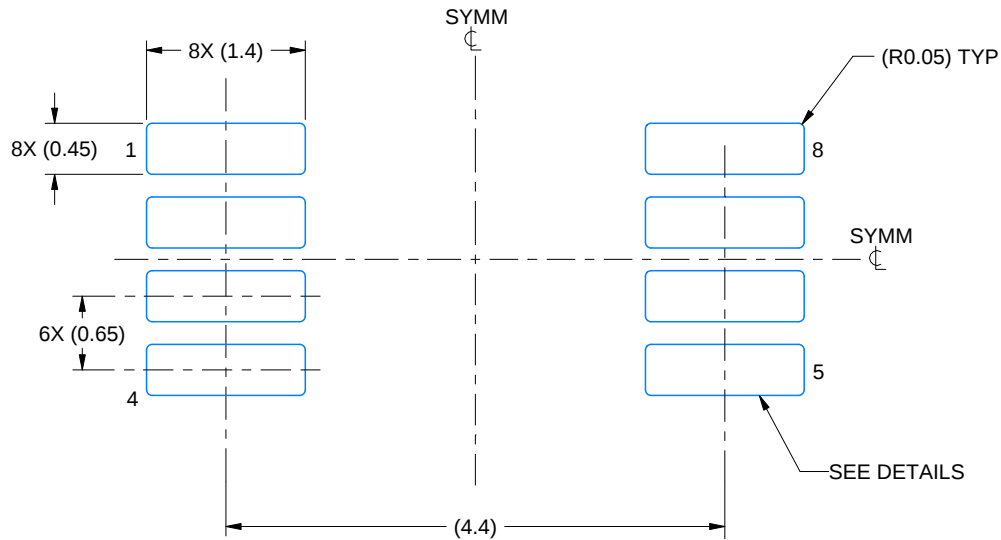
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

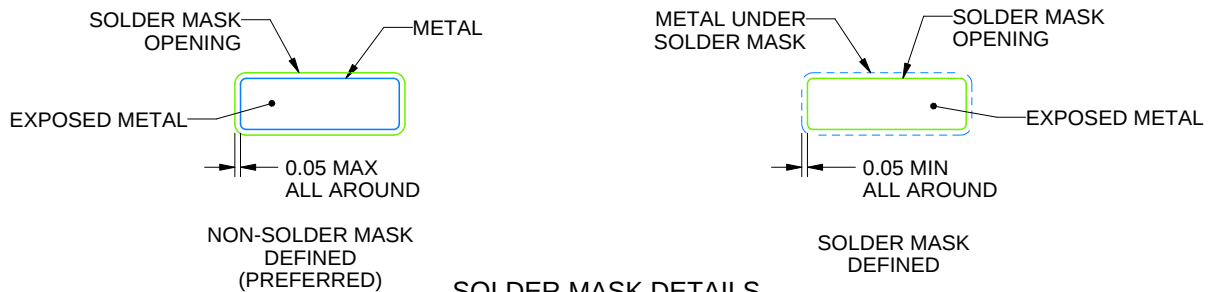
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

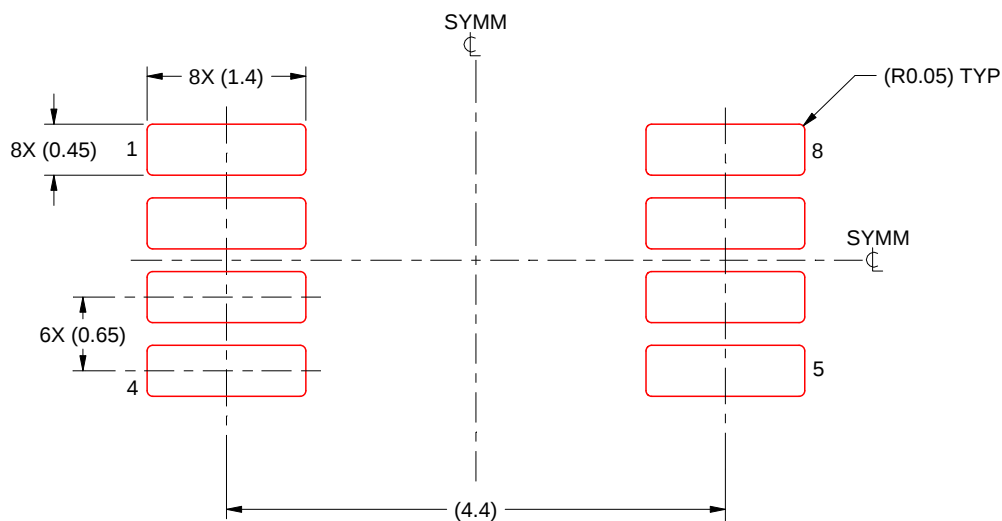
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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