

# SN74CBTD16210

## 20-BIT FET BUS SWITCH

### WITH LEVEL SHIFTING

SCDS049H – MARCH 1998 – REVISED JULY 2002

- Member of Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Designed to Be Used in Level-Shifting Applications

#### description/ordering information

The SN74CBTD16210 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to  $V_{CC}$  is integrated in the circuit to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

The device is organized as a dual 10-bit bus switch with separate output-enable ( $\overline{OE}$ ) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When  $\overline{OE}$  is low, the associated 10-bit bus switch is on, and port A is connected to port B. When  $\overline{OE}$  is high, the switch is open, and the high-impedance state exists between the ports.

#### DGG, DGV, OR DL PACKAGE (TOP VIEW)

|          |    |    |                  |
|----------|----|----|------------------|
| NC       | 1  | 48 | $1\overline{OE}$ |
| 1A1      | 2  | 47 | $2\overline{OE}$ |
| 1A2      | 3  | 46 | 1B1              |
| 1A3      | 4  | 45 | 1B2              |
| 1A4      | 5  | 44 | 1B3              |
| 1A5      | 6  | 43 | 1B4              |
| 1A6      | 7  | 42 | 1B5              |
| GND      | 8  | 41 | GND              |
| 1A7      | 9  | 40 | 1B6              |
| 1A8      | 10 | 39 | 1B7              |
| 1A9      | 11 | 38 | 1B8              |
| 1A10     | 12 | 37 | 1B9              |
| 2A1      | 13 | 36 | 1B10             |
| 2A2      | 14 | 35 | 2B1              |
| $V_{CC}$ | 15 | 34 | 2B2              |
| 2A3      | 16 | 33 | 2B3              |
| GND      | 17 | 32 | GND              |
| 2A4      | 18 | 31 | 2B4              |
| 2A5      | 19 | 30 | 2B5              |
| 2A6      | 20 | 29 | 2B6              |
| 2A7      | 21 | 28 | 2B7              |
| 2A8      | 22 | 27 | 2B8              |
| 2A9      | 23 | 26 | 2B9              |
| 2A10     | 24 | 25 | 2B10             |

NC – No internal connection

#### ORDERING INFORMATION

| $T_A$         | PACKAGE†    |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------|---------------|-----------------------|------------------|
| –40°C to 85°C | SSOP – DL   | Tube          | SN74CBTD16210DL       | CBTD16210        |
|               |             | Tape and reel | SN74CBTD16210DLR      |                  |
|               | TSSOP – DGG | Tape and reel | SN74CBTD16210DGGR     | CBTD16210        |
|               | TVSOP – DGV | Tape and reel | SN74CBTD16210DGV      | CYD210           |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

#### FUNCTION TABLE (each 10-bit bus switch)

| INPUT $\overline{OE}$ | FUNCTION        |
|-----------------------|-----------------|
| L                     | A port = B port |
| H                     | Z               |



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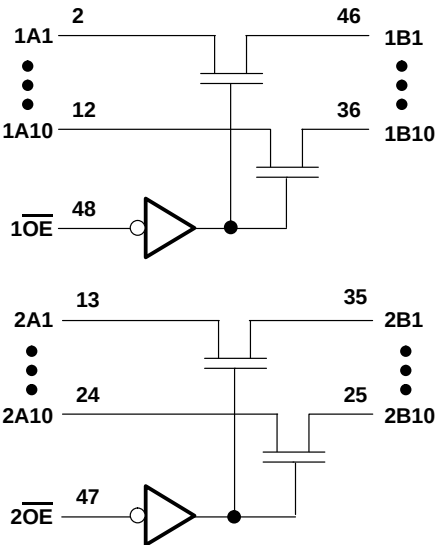
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                        |             |                |
|--------------------------------------------------------|-------------|----------------|
| Supply voltage range, $V_{CC}$                         | .....       | –0.5 V to 7 V  |
| Input voltage range, $V_I$ (see Note 1)                | .....       | –0.5 V to 7 V  |
| Continuous channel current                             | .....       | 128 mA         |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )            | .....       | –50 mA         |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): | DGG package | 70°C/W         |
|                                                        | DGV package | 58°C/W         |
|                                                        | DL package  | 63°C/W         |
| Storage temperature range, $T_{stg}$                   | .....       | –65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

|                                           | MIN | MAX | UNIT |
|-------------------------------------------|-----|-----|------|
| $V_{CC}$ Supply voltage                   | 4.5 | 5.5 | V    |
| $V_{IH}$ High-level control input voltage | 2   |     | V    |
| $V_{IL}$ Low-level control input voltage  |     | 0.8 | V    |
| $T_A$ Operating free-air temperature      | –40 | 85  | °C   |

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**20-BIT FET BUS SWITCH**  
**WITH LEVEL SHIFTING**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                |                | TEST CONDITIONS                                                                      | MIN | TYP <sup>†</sup> | MAX     | UNIT          |
|--------------------------|----------------|--------------------------------------------------------------------------------------|-----|------------------|---------|---------------|
| $V_{IK}$                 |                | $V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$                                      |     |                  | -1.2    | V             |
| $V_{OH}$                 |                | See Figure 2                                                                         |     |                  |         |               |
| $I_I$                    |                | $V_{CC} = 0\text{ V}$ , $V_I = 5.5\text{ V}$                                         |     |                  | 10      | $\mu\text{A}$ |
|                          |                | $V_{CC} = 5.5\text{ V}$ , $V_I = 5.5\text{ V or GND}$                                |     |                  | $\pm 1$ |               |
| $I_{CC}$                 |                | $V_{CC} = 5.5\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$                   |     |                  | 1.5     | mA            |
| $\Delta I_{CC}^\ddagger$ | Control inputs | $V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$ |     |                  | 2.5     | mA            |
| $C_i$                    | Control inputs | $V_I = 3\text{ V or 0}$                                                              |     |                  | 4.5     | pF            |
| $C_{io(OFF)}$            |                | $V_O = 3\text{ V or 0}$ , $\overline{OE} = V_{CC}$                                   |     |                  | 5.5     | pF            |
| $r_{on}^\S$              |                | $V_{CC} = 4.5\text{ V}$ , $V_I = 0$ , $I_I = 64\text{ mA}$                           |     | 5                | 7       | $\Omega$      |
|                          |                | $V_{CC} = 4.5\text{ V}$ , $V_I = 0$ , $I_I = 30\text{ mA}$                           |     | 5                | 7       |               |
|                          |                | $V_{CC} = 4.5\text{ V}$ , $V_I = 2.4\text{ V}$ , $I_I = 15\text{ mA}$                |     | 35               | 50      |               |

<sup>†</sup> All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

<sup>§</sup> Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER            | FROM (INPUT)    | TO (OUTPUT) | MIN | MAX  | UNIT |
|----------------------|-----------------|-------------|-----|------|------|
| $t_{pd}^{\parallel}$ | A or B          | B or A      |     | 0.25 | ns   |
| $t_{en}$             | $\overline{OE}$ | A or B      | 1.5 | 9.8  | ns   |
| $t_{dis}$            | $\overline{OE}$ | A or B      | 1.5 | 8.9  | ns   |

<sup>||</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

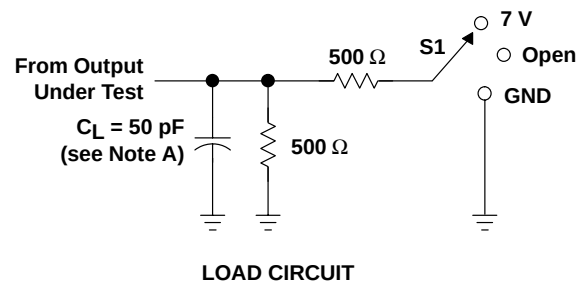
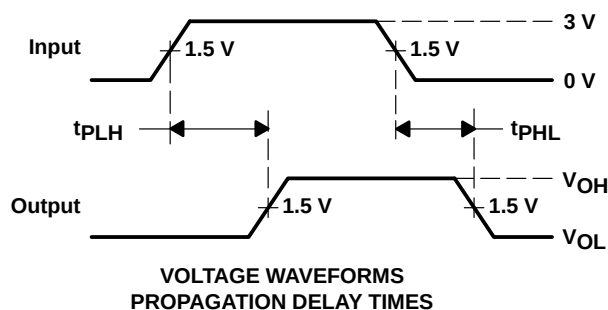
# SN74CBTD16210

## 20-BIT FET BUS SWITCH

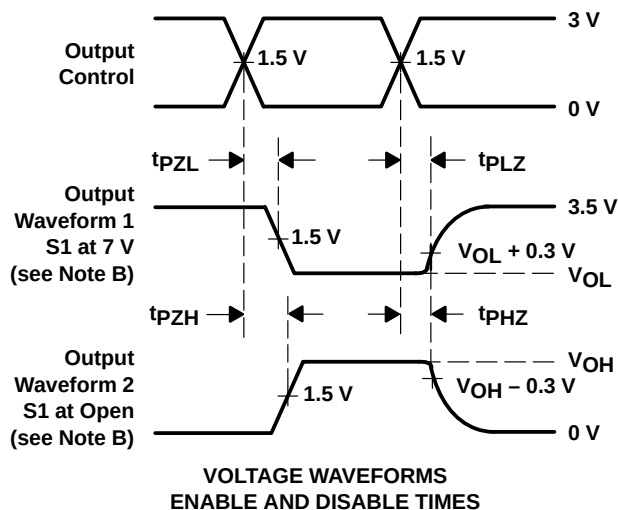
### WITH LEVEL SHIFTING

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#### PARAMETER MEASUREMENT INFORMATION



| TEST              | S1   |
|-------------------|------|
| $t_{pd}$          | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

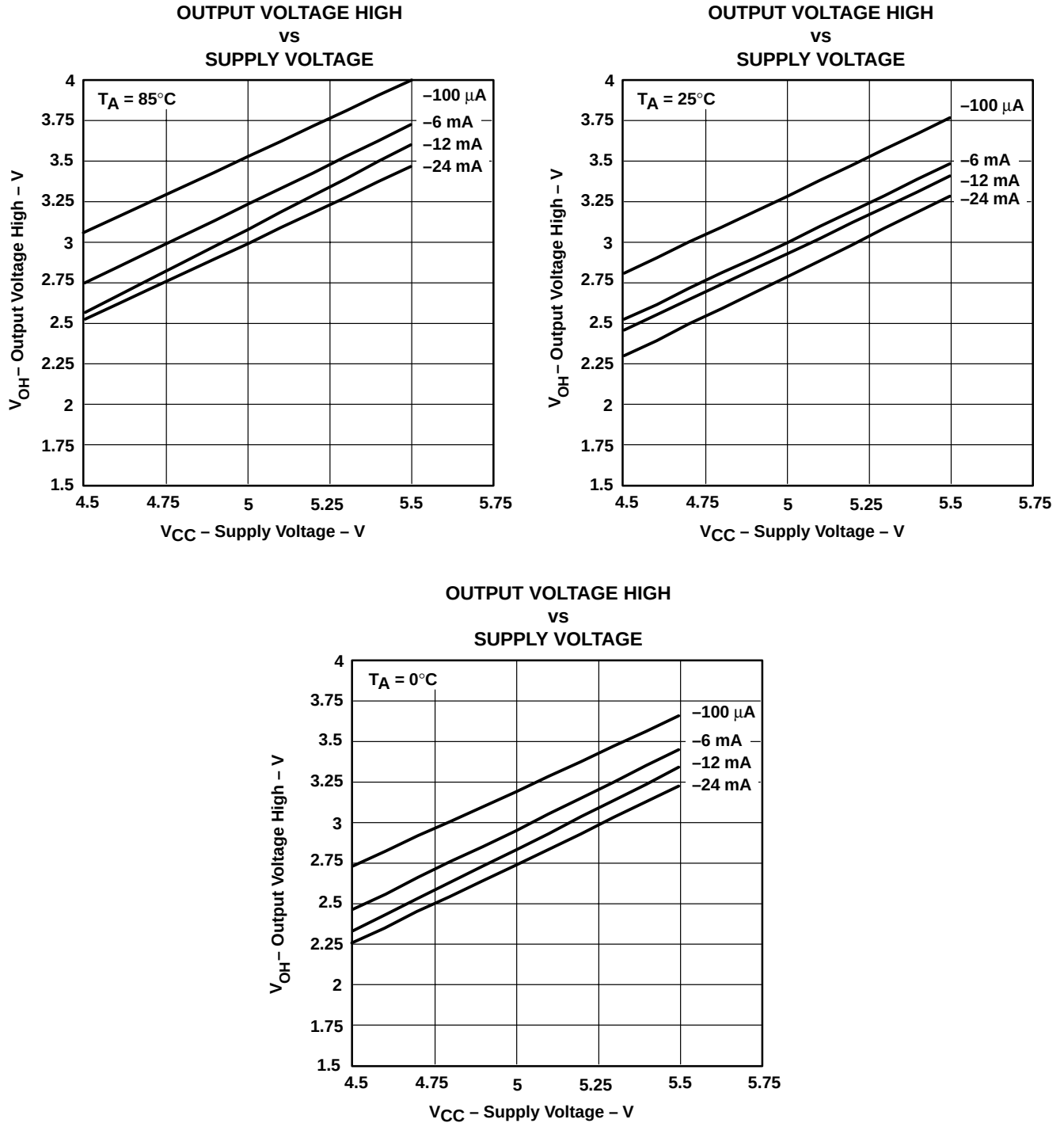


Figure 2. VOH Values

## PACKAGING INFORMATION

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74CBTD16210DGGR</a> | Active        | Production           | TSSOP (DGG)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBTD16210           |
| SN74CBTD16210DGGR.A               | Active        | Production           | TSSOP (DGG)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBTD16210           |
| <a href="#">SN74CBTD16210DGVR</a> | NRND          | Production           | TVSOP (DGV)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CYD210              |
| SN74CBTD16210DGVR.A               | NRND          | Production           | TVSOP (DGV)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CYD210              |
| <a href="#">SN74CBTD16210DL</a>   | NRND          | Production           | SSOP (DL)   48   | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBTD16210           |
| SN74CBTD16210DL.A                 | NRND          | Production           | SSOP (DL)   48   | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBTD16210           |
| <a href="#">SN74CBTD16210DLR</a>  | Active        | Production           | SSOP (DL)   48   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBTD16210           |
| SN74CBTD16210DLR.A                | Active        | Production           | SSOP (DL)   48   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBTD16210           |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

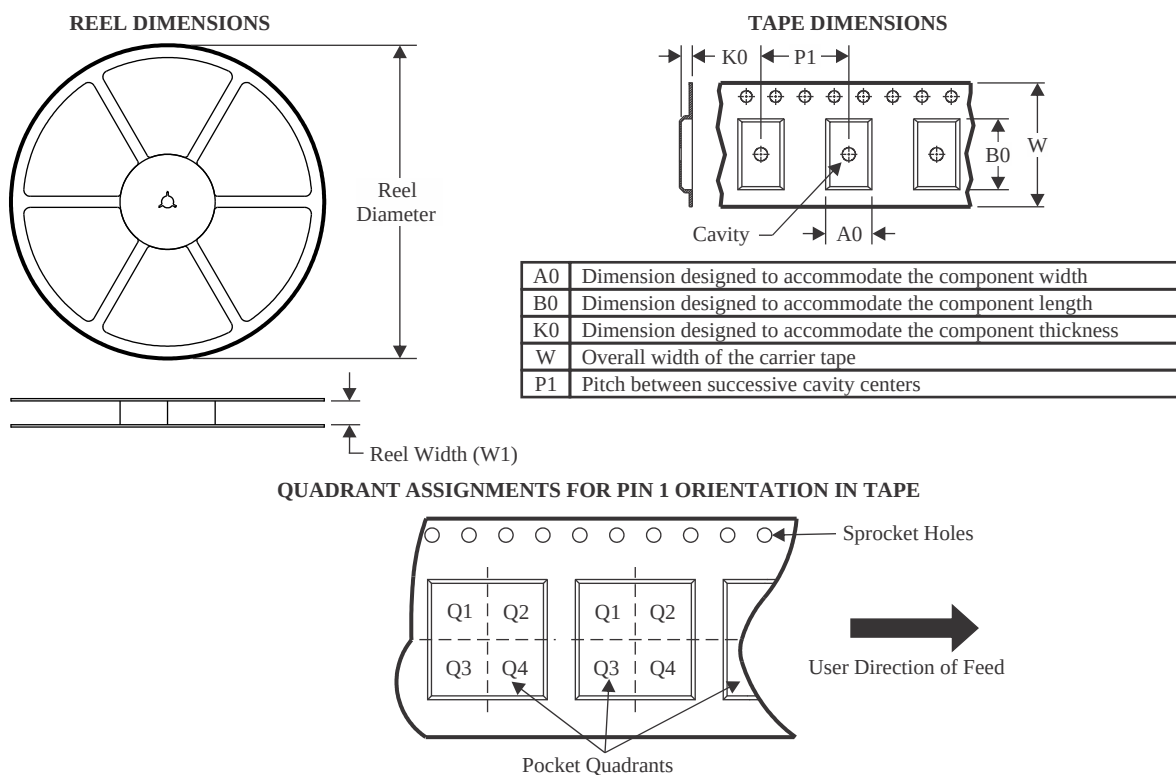
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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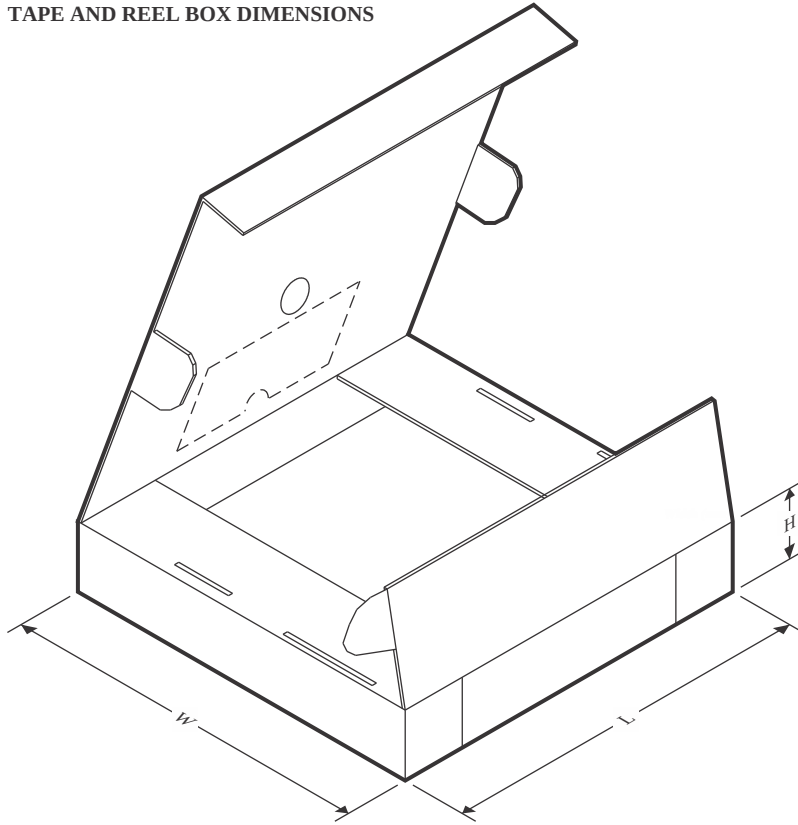
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CBTD16210DGGR | TSSOP        | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| SN74CBTD16210DGVR | TVSOP        | DGV             | 48   | 2000 | 330.0              | 16.4               | 7.1     | 10.2    | 1.6     | 12.0    | 16.0   | Q1            |
| SN74CBTD16210DLR  | SSOP         | DL              | 48   | 1000 | 330.0              | 32.4               | 11.35   | 16.2    | 3.1     | 16.0    | 32.0   | Q1            |

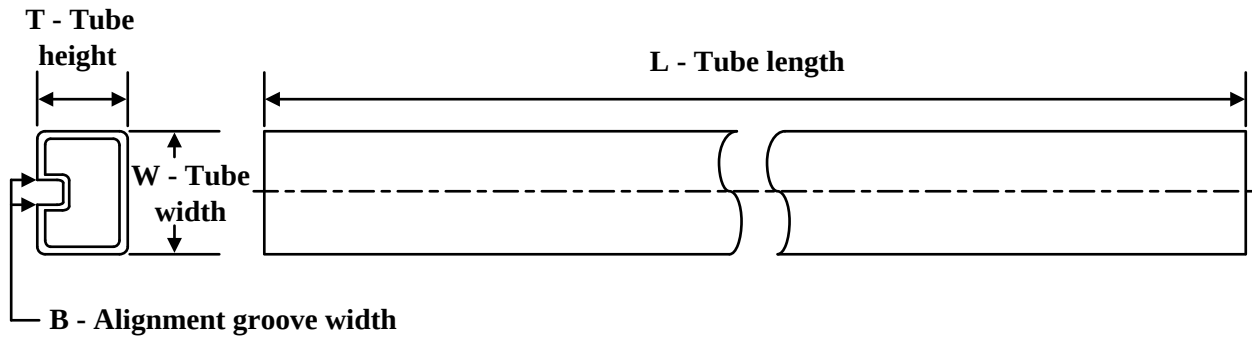
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CBTD16210DGGR | TSSOP        | DGG             | 48   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74CBTD16210DGVR | TVSOP        | DGV             | 48   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74CBTD16210DLR  | SSOP         | DL              | 48   | 1000 | 367.0       | 367.0      | 55.0        |

## TUBE

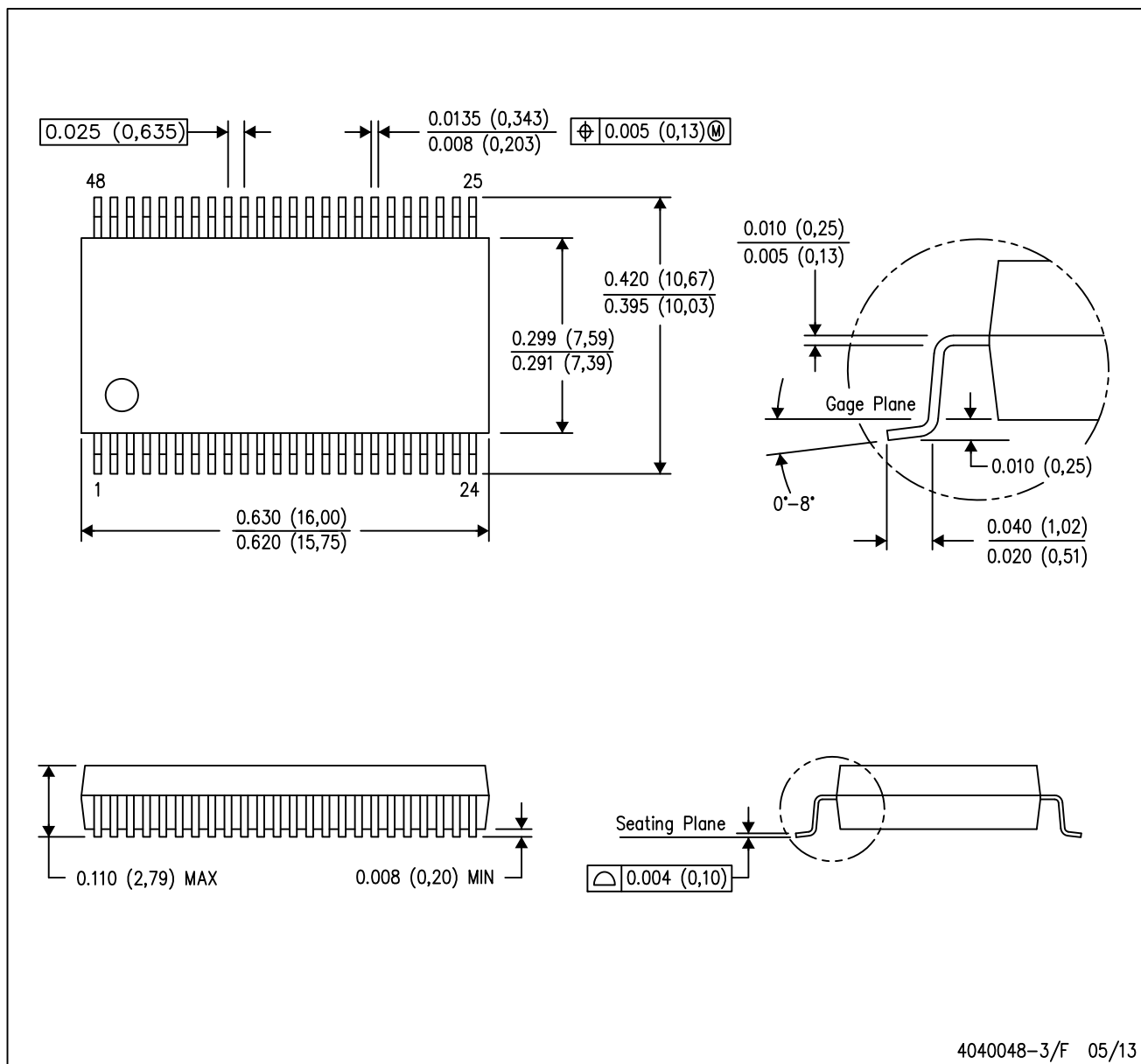


\*All dimensions are nominal

| Device            | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74CBTD16210DL   | DL           | SSOP         | 48   | 25  | 473.7  | 14.24  | 5110   | 7.87   |
| SN74CBTD16210DL.A | DL           | SSOP         | 48   | 25  | 473.7  | 14.24  | 5110   | 7.87   |

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE

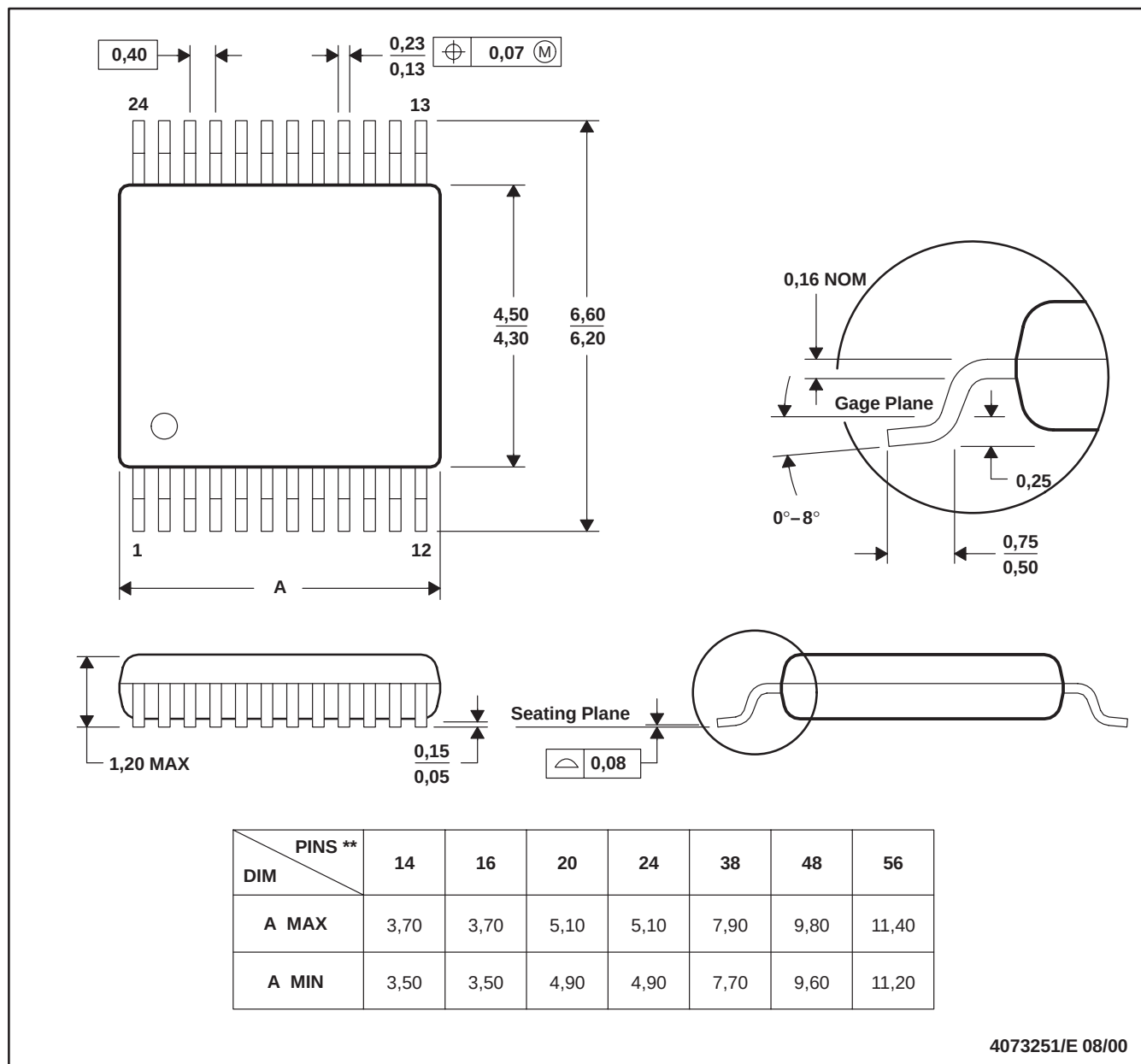


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

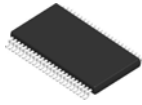
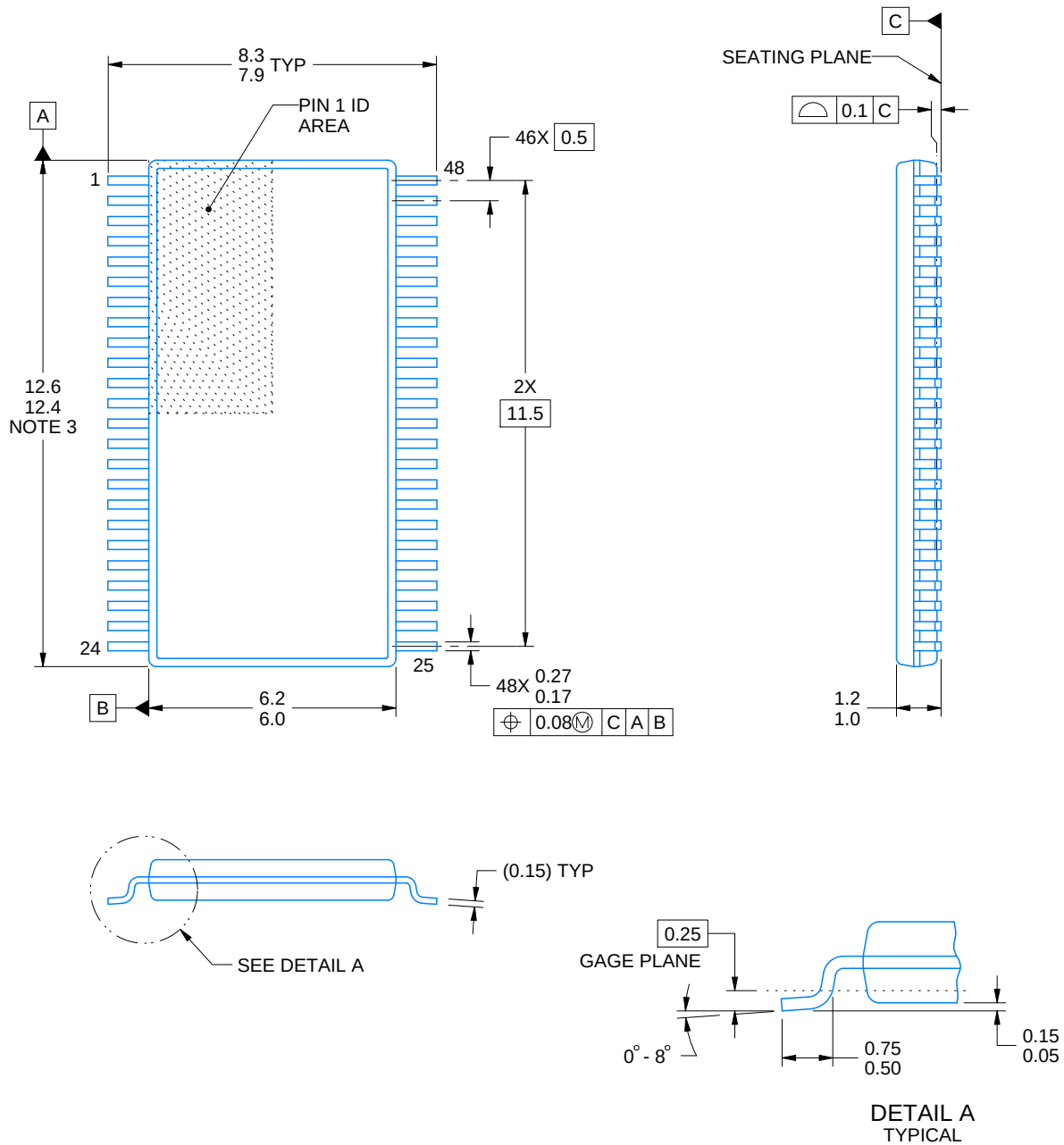
## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



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## NOTES:

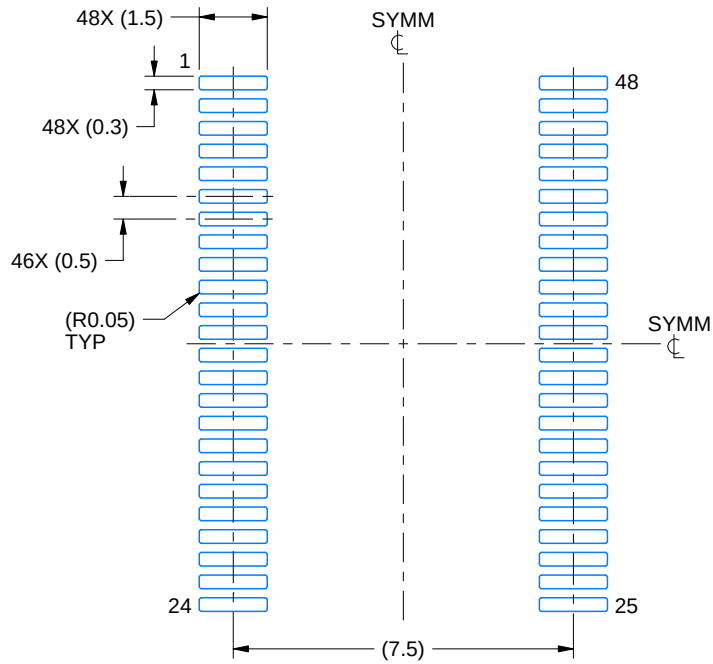
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

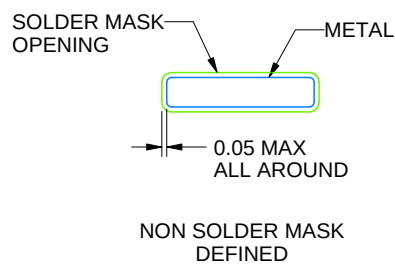
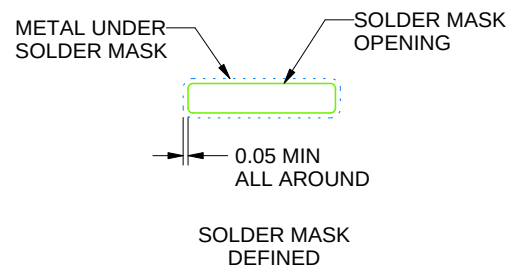
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

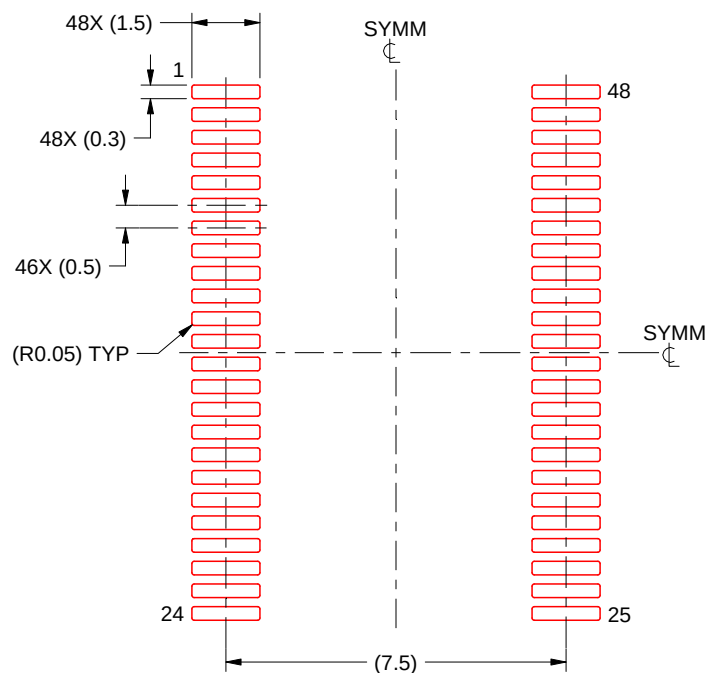
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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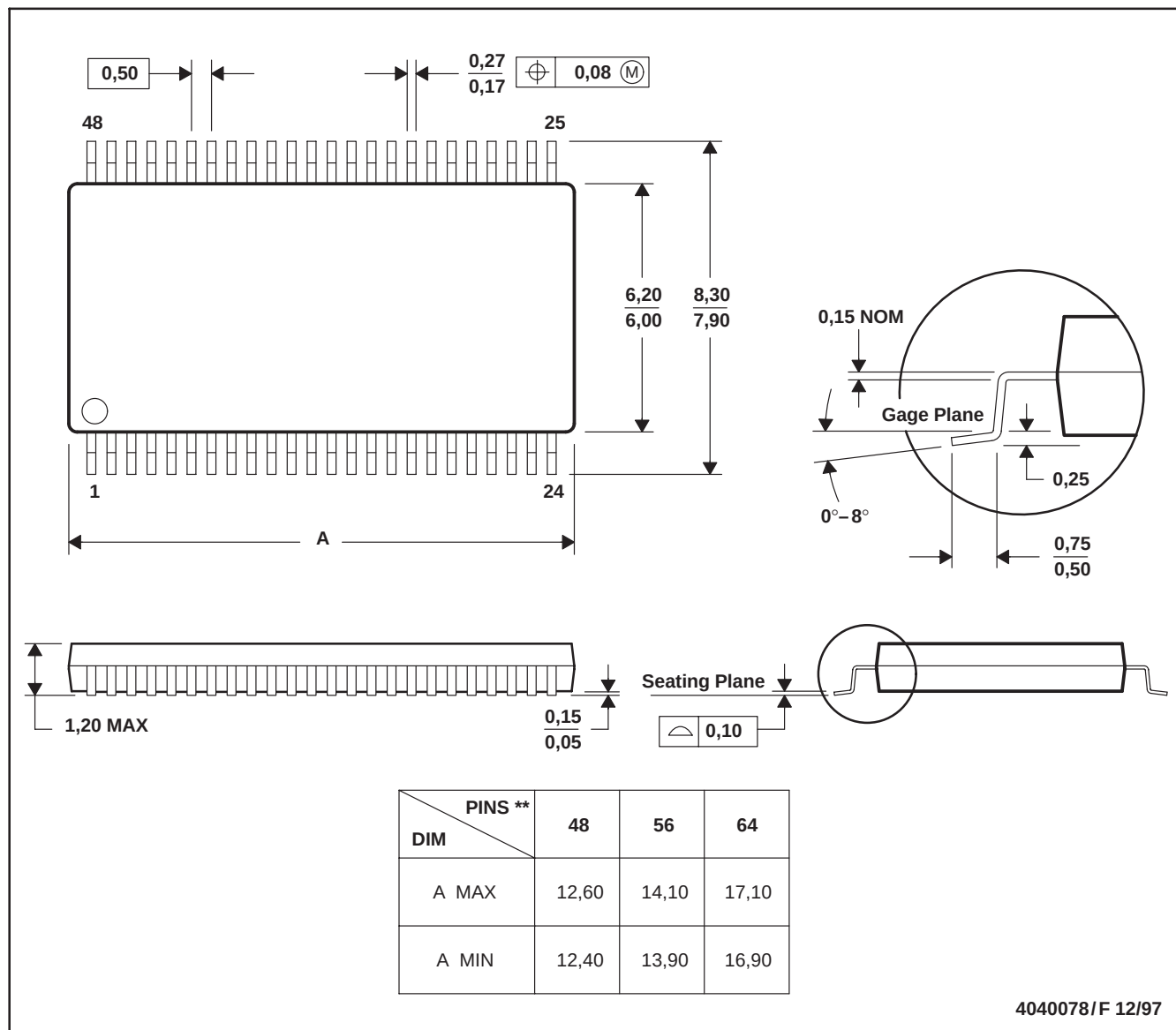
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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