

DS15BA101 1.5 Gbps Differential Buffer with Adjustable Output Voltage

Check for Samples: [DS15BA101](#)

FEATURES

- Data Rates from DC to 1.5+ Gbps
- Differential or Single-ended Input
- Adjustable Output Amplitude
- Single 3.3V Supply
- Industrial -40°C to +85°C Temperature
- Low Power: 150 mW (typ) at 1.5 Gbps
- Space-saving 3 x 3 mm WSON-8 Package

APPLICATIONS

- Cable Extension Applications
- Level Translation
- Signal Buffering and Repeating
- Security Cameras

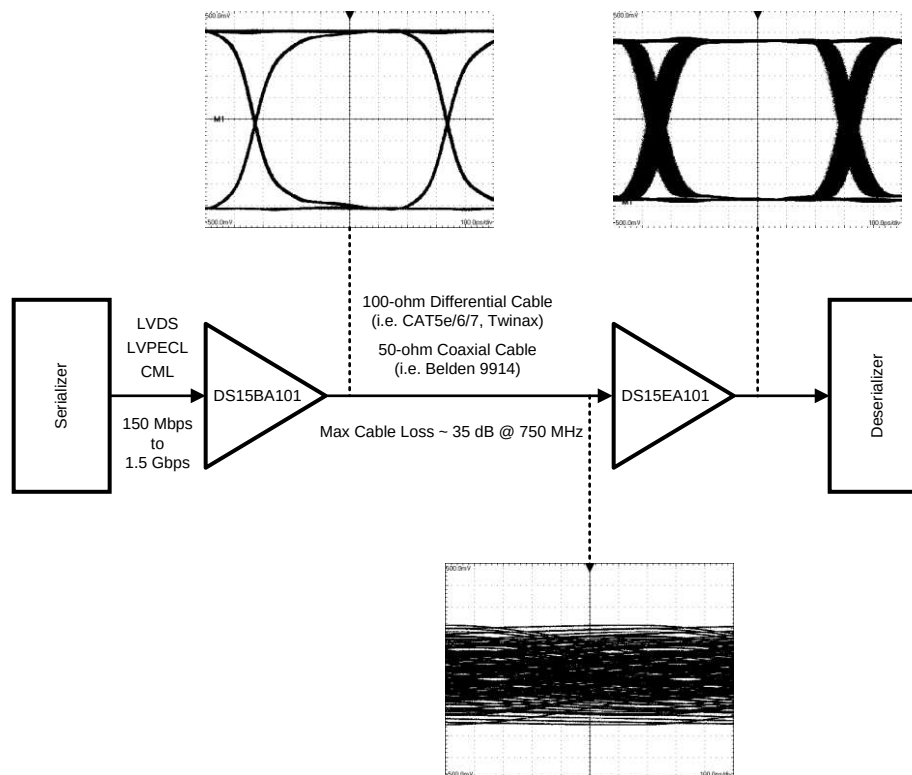
DESCRIPTION

The DS15BA101 is a high-speed differential buffer for cable driving, level translation, signal buffering, and signal repeating applications. Its fully differential signal path ensures exceptional signal integrity and noise immunity and it drives both differential and single-ended transmission lines at data rates in excess of 1.5 Gbps.

Output voltage amplitude is adjustable via a single external resistor for level translation and cable driving applications into 50-ohm single-ended and 100-ohm differential mode impedances.

The DS15BA101 is powered from a single 3.3V supply and consumes 150 mW (typ) at 1.5 Gbps. It operates over the full -40°C to +85°C industrial temperature range and is available in a space saving 3x3 mm WSON-8 package.

Typical Application



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage		-0.5V to 3.6V
Input Voltage (all inputs)		-0.3V to $V_{CC}+0.3V$
Output Current		28 mA
Storage Temperature Range		-65°C to +150°C
Junction Temperature		+150°C
Lead Temperature (Soldering 4 Sec)		+260°C
Package Thermal Resistance	θ_{JA} WSON-8	+90.7°C/W
	θ_{JC} WSON-8	+41.2°C/W
ESD Rating (HBM)		5 kV
ESD Rating (MM)		250V

- (1) "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Recommended Operating Conditions

Supply Voltage ($V_{CC} - GND$):	3.3V $\pm 5\%$
Operating Free Air Temperature (T_A) DS15BA101SD	-40°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{ICM}	Input Common Mode Voltage	See Note ⁽³⁾	IN+, IN-	0.8		$V_{CC} - V_{ID}/2$	V
V_{ID}	Differential Input Voltage Swing			100		2000	mV _{P-P}
V_{OS}	Output Common Mode Voltage		OUT+, OUT-		$V_{CC} - V_{OUT}/2$		V
V_{OUT}	Output Voltage	Single-ended, 25 Ω load $R_{VO} = 953\Omega$ 1%,			400		mV _{P-P}
		Single-ended, 25 Ω load $R_{VO} = 487\Omega$ 1%,			800		mV _{P-P}
I_{CC}	Supply Current	See Note ⁽⁴⁾			45	49	mA

- (1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to GND.
 (2) Typical values are stated for $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.
 (3) Specification is ensured by characterization.
 (4) Maximum I_{CC} is measured at $V_{CC} = +3.465V$ and $T_A = +70^\circ C$.

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified⁽¹⁾.

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DR _{MAX}	Maximum Data Rate	See Note ⁽²⁾	IN+, IN-	1.5	2.0		Gbps
t _{LHT}	Output Low to High Transition Time	20% – 80% ⁽³⁾	OUT+, OUT-		120	220	ps
t _{HLT}	Output High to Low Transition Time				120	220	ps
t _{PLHD}	Propagation Low to High Delay	See Note ⁽²⁾		0.95	1.10	1.35	ns
t _{PHLD}	Propagation High to Low Delay	See Note ⁽²⁾		0.95	1.10	1.35	ns
t _{TJ}	Total Jitter	1.5 Gbps			26		pSp-p

(1) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.

(2) Specification is ensured by characterization.

(3) Specification is ensured by characterization and verified by test.

CONNECTION DIAGRAM

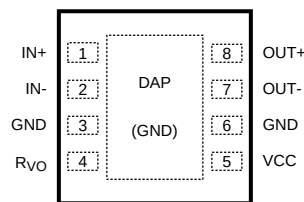


Figure 1. 8-Pad WSON
See NGQ Package

PIN DESCRIPTIONS

Pin #	Name	Description
1	IN+	Non-inverting input pin.
2	IN-	Inverting input pin.
3	GND	Circuit common (ground reference).
4	R _{VO}	Output voltage amplitude control. Connect a resistor to V _{CC} to set output voltage.
5	V _{CC}	Positive power supply (+3.3V).
6	GND	Circuit common (ground reference).
7	OUT-	Inverting output pin.
8	OUT+	Non-inverting output pin.

DEVICE OPERATION

INPUT INTERFACING

The DS15BA101 accepts either differential or single-ended input. The inputs are self-biased, allowing for simple AC or DC coupling. DC-coupled inputs must be kept within the specified common-mode range. The IN+ and IN- pins are self-biased at approximately 2.1V with $V_{CC} = 3.3V$. The following three figures illustrate typical DC-coupled interface to common differential drivers.

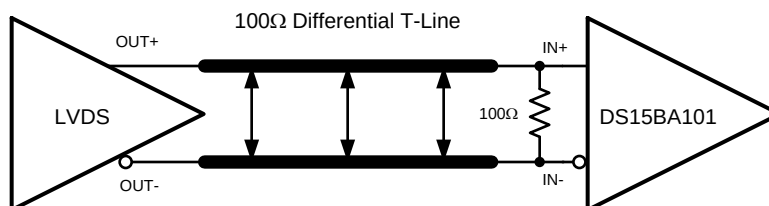


Figure 2. Typical LVDS Driver DC-Coupled Interface to DS15BA101 Input

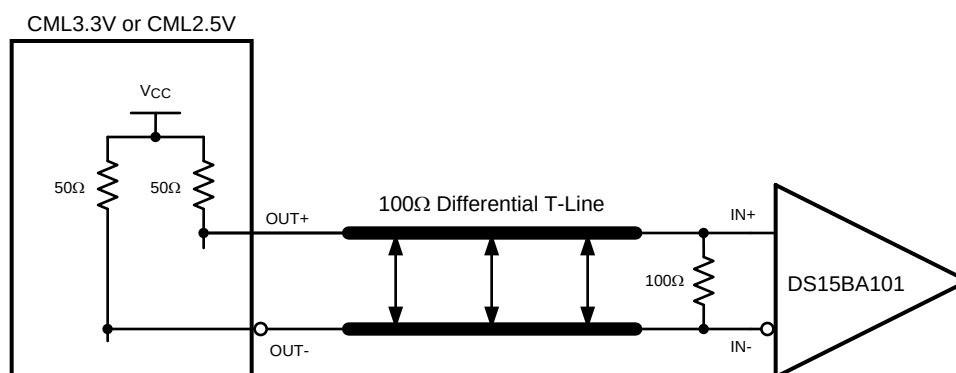


Figure 3. Typical CML Driver DC-Coupled Interface to DS15BA101 Input

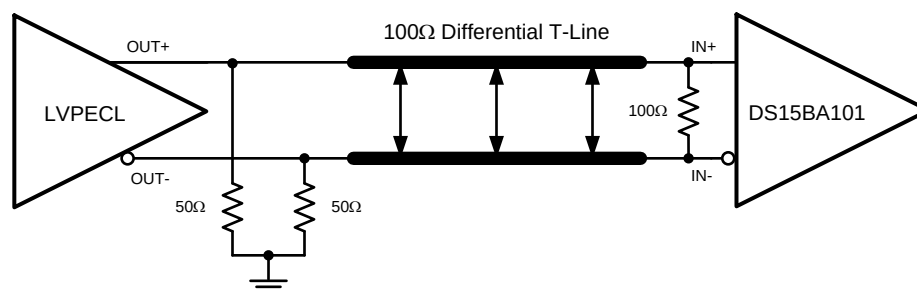


Figure 4. Typical LVPECL Driver DC-Coupled Interface to DS15BA101 Input

OUTPUT INTERFACING

The DS15BA101 uses current mode outputs. Single-ended output levels are 400 mV_{P-P} into AC-coupled 100Ω differential cable (with $R_{VO} = 953\Omega$) or into AC-coupled 50Ω coaxial cable (with $R_{VO} = 487\Omega$). Output level is controlled by the value of the R_{VO} resistor connected between the R_{VO} and V_{CC} .

The R_{VO} resistor should be placed as close as possible to the R_{VO} pin. In addition, the copper in the plane layers below the R_{VO} network should be removed to minimize parasitic capacitance. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most receivers have a common mode input range that can accommodate CML signals, it is recommended to check respective receiver's datasheet prior to implementing the suggested interface implementation.

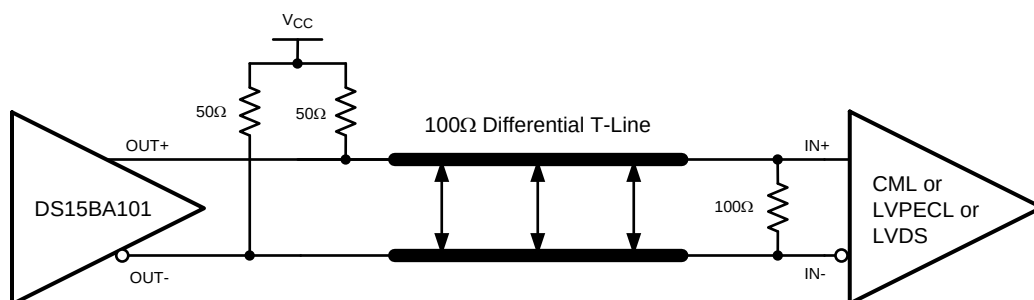


Figure 5. Typical DS15BA101 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

CABLE EXTENDER APPLICATION

The DS15BA101 together with the DS15EA101 form a cable extender chipset optimized for extending serial data streams from serializer/deserializer (SerDes) pairs and field programmable gate arrays (FPGAs) over 100Ω differential (i.e. CAT5e/6/7 and twinax) and 50Ω coaxial cables. Setting correct DS15BA101 output amplitude and proper cable termination are keys for optimal operation. The following two figures show recommended chipset configuration for 100Ω differential and 50Ω coaxial cables.

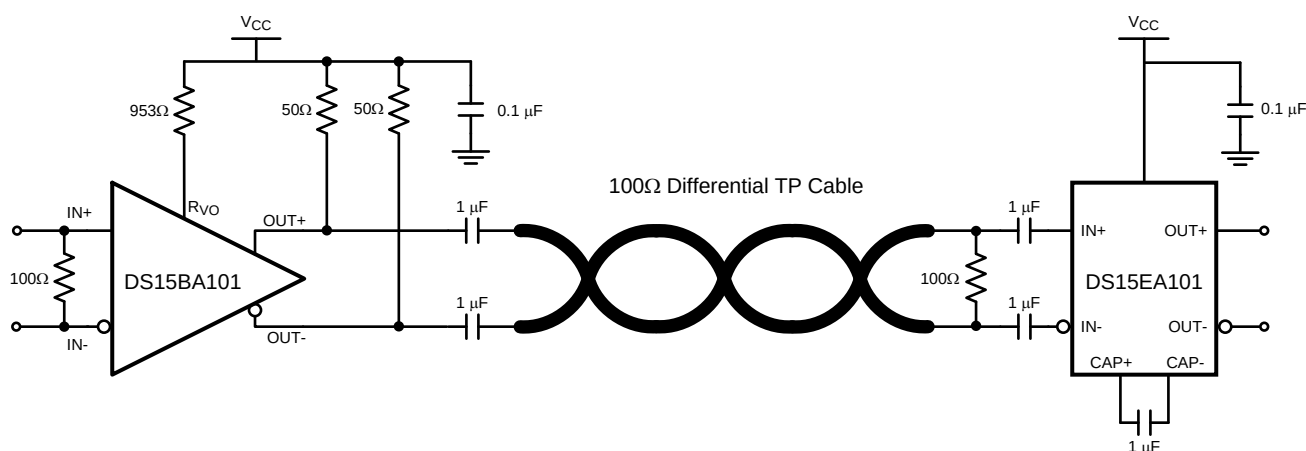


Figure 6. Cable Extender Chipset Connection Diagram for 100Ω Differential Cables

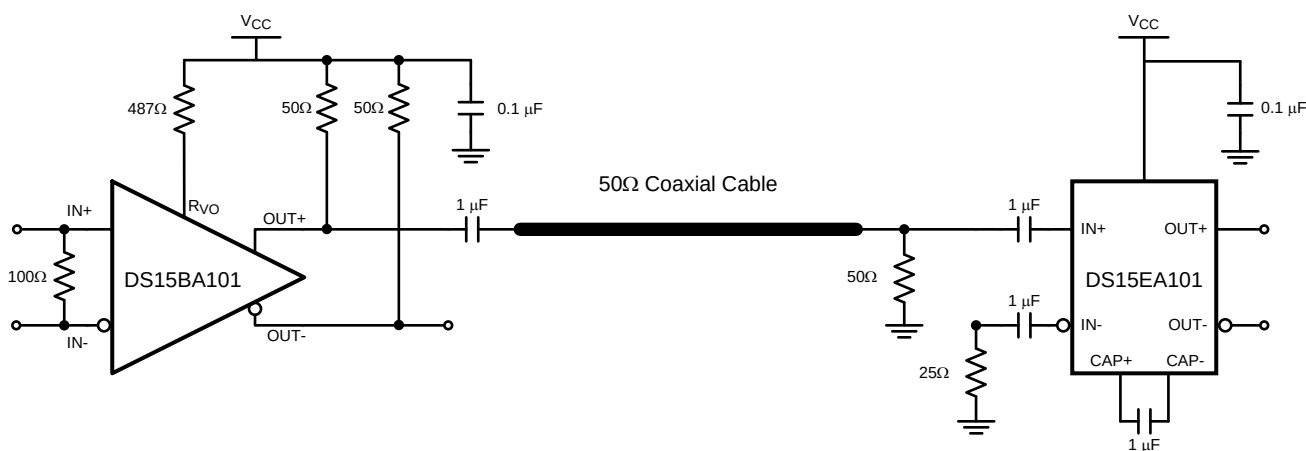


Figure 7. Cable Extender Chipset Connection Diagram for 50Ω Coaxial Cables

REFERENCE DESIGN

There is a complete reference design (P/N: DriveCable02EVK) available for evaluation of the cable extender chipset (DS15BA101 and DS15EA101). For more information, visit <http://www.ti.com/tool/drivecable02evk>.

Typical Performance

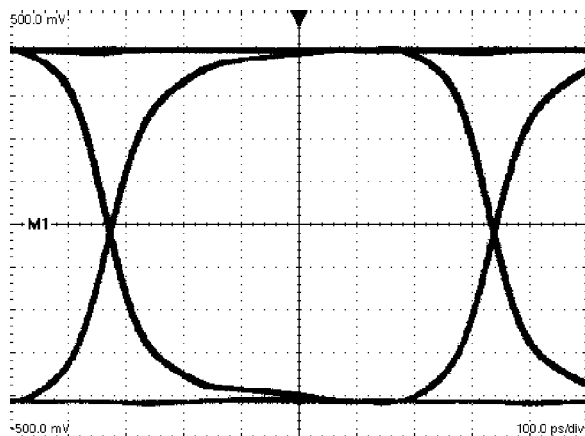


Figure 8. 1.5 Gbps Differential DS15BA101 Output
 $R_{VO} = 953\Omega$, H:100 ps / DIV, V:100 mV / DIV

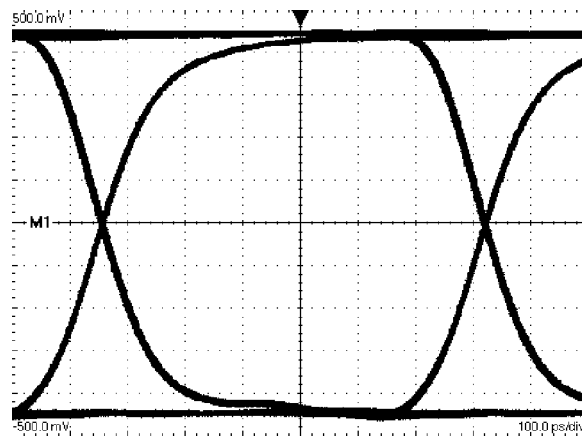


Figure 9. 1.5 Gbps Single-ended DS15BA101 Output
 $R_{VO} = 487\Omega$, H:100 ps / DIV, V:100 mV / DIV

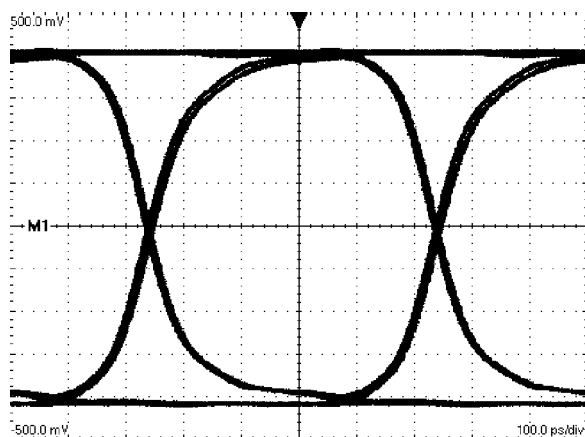


Figure 10. 2.0 Gbps Differential DS15BA101 Output
 $R_{VO} = 953\Omega$, H:100 ps / DIV, V:100 mV / DIV

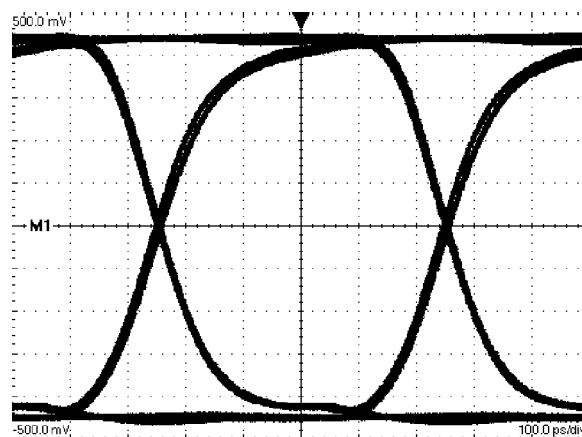


Figure 11. 2.0 Gbps Single-ended DS15BA101 Output
 $R_{VO} = 487\Omega$, H:100 ps / DIV, V:100 mV / DIV

REVISION HISTORY

Changes from Revision I (April 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format	6

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS15BA101SD/NOPB	Active	Production	WSO (NGQ) 8	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	BA101
DS15BA101SD/NOPB.A	Active	Production	WSO (NGQ) 8	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	BA101
DS15BA101SDE/NOPB	Active	Production	WSO (NGQ) 8	250 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	BA101
DS15BA101SDE/NOPB.A	Active	Production	WSO (NGQ) 8	250 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	BA101
DS15BA101SDX/NOPB	Active	Production	WSO (NGQ) 8	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	BA101
DS15BA101SDX/NOPB.A	Active	Production	WSO (NGQ) 8	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	BA101

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

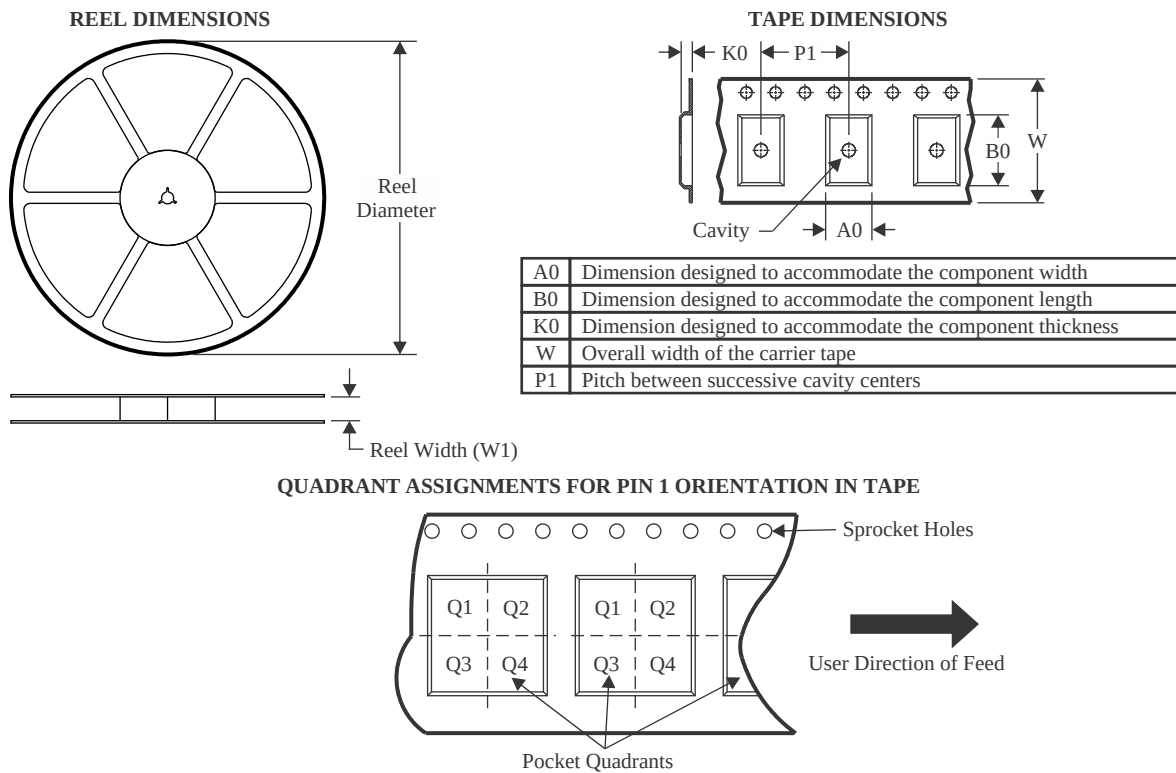
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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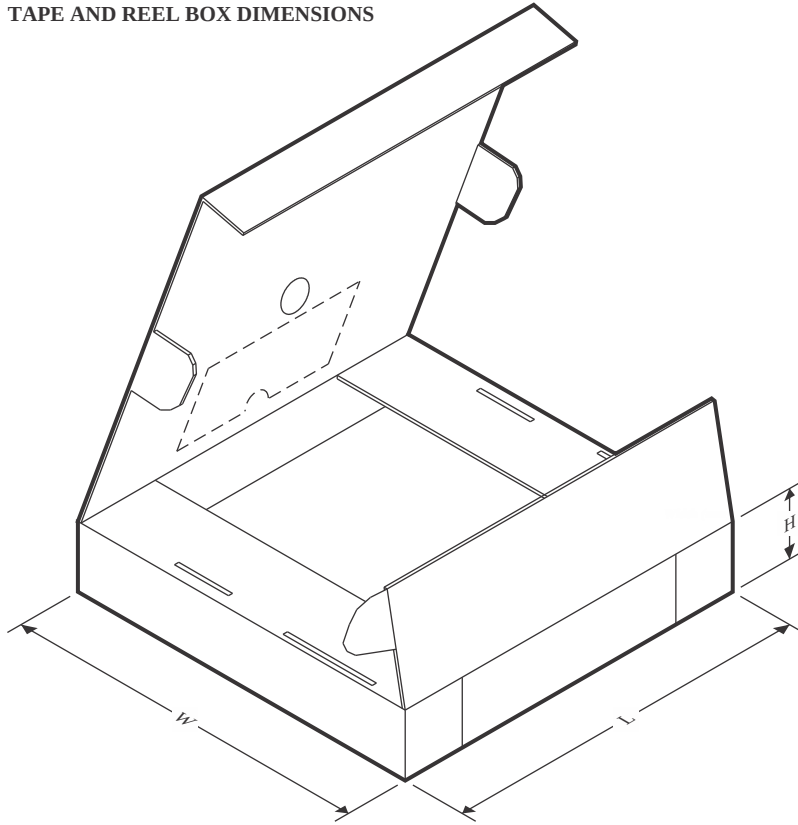
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS15BA101SD/NOPB	WSO	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS15BA101SDE/NOPB	WSO	NGQ	8	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS15BA101SDX/NOPB	WSO	NGQ	8	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

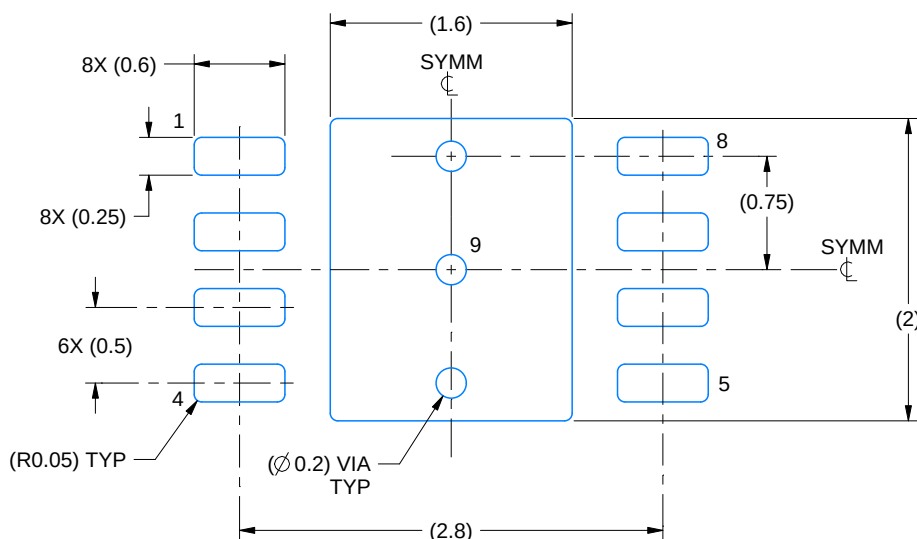
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS15BA101SD/NOPB	WSO	NGQ	8	1000	208.0	191.0	35.0
DS15BA101SDE/NOPB	WSO	NGQ	8	250	208.0	191.0	35.0
DS15BA101SDX/NOPB	WSO	NGQ	8	4500	356.0	356.0	36.0

EXAMPLE BOARD LAYOUT

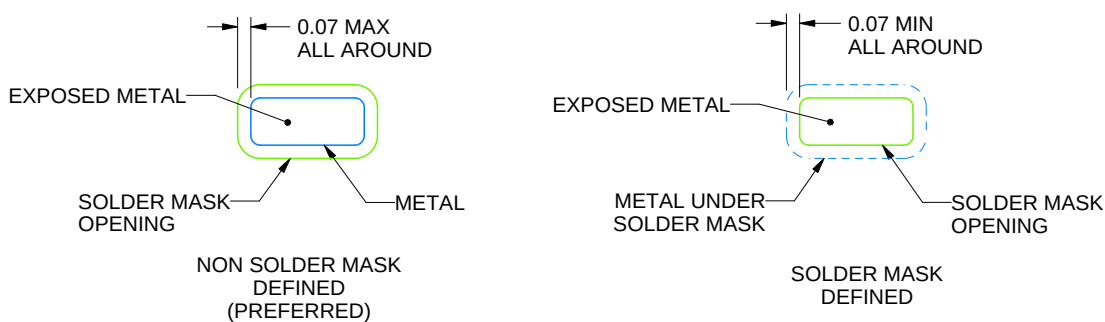
NGQ0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4214922/A 03/2018

NOTES: (continued)

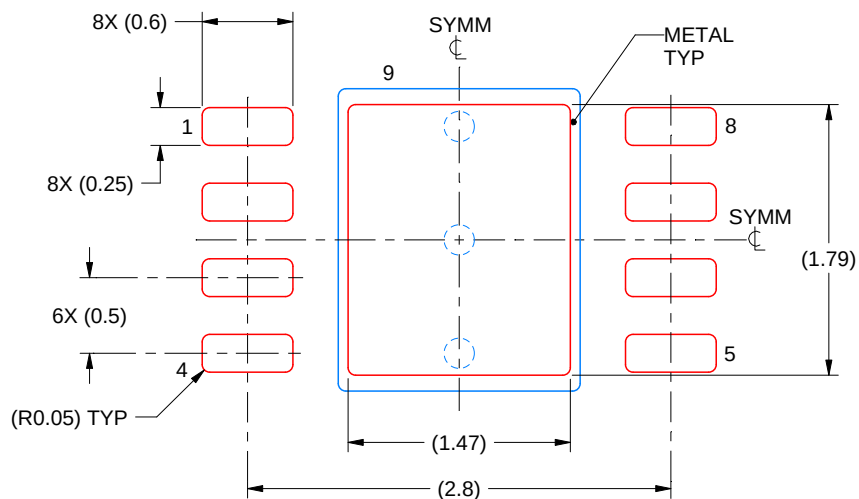
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

NGQ0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214922/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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