DirectPath™, 3-VRMS Line Driver With Adjustable Gain

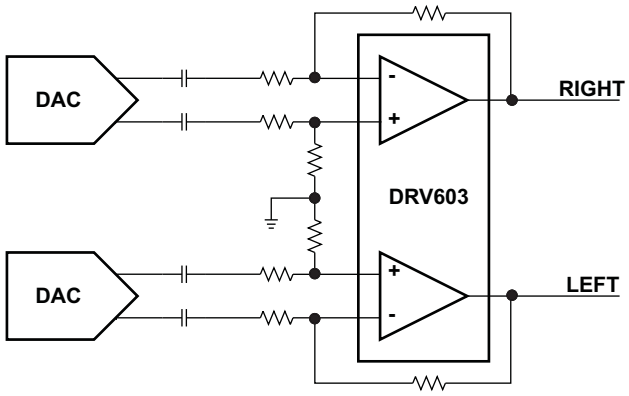
Check for Samples: DRV603

FEATURES

- **DirectPath™**
  - **Eliminates Pop/Clicks**
  - **Eliminates Output DC-Blocking Capacitors**
  - **Provides Flat Frequency Response 20 Hz–20 kHz**
- **Low Noise and THD**
  - **SNR > 109 dB**
  - **Typical Vn < 7 µVms**
  - **THD+N < 0.002%**
- **Output Voltage Into 2.5-kΩ Load**
  - **2 Vrms With 3.3-V Supply Voltage**
  - **3 Vrms With 5-V Supply Voltage**
- **Differential Input**
- **External Undervoltage Mute**

APPLICATIONS

- **PDP / LCD TV**
- **Blu-ray Disc™, DVD Players**
- **Home Theater in a Box**
- **Set-Top Boxes**



DESCRIPTION

The DRV603PW is a 3-V_{RMS} pop-free stereo line driver designed to allow the removal of the output dc-blocking capacitors for reduced component count and cost. The device is ideal for single-supply electronics where size and cost are critical design parameters.

Designed using TI's patented DirectPath™ technology, The DRV603 is capable of driving 3 V_{rms} into a 2.5-kΩ load with 5-V supply voltage. The device has differential inputs and uses external gain-setting resistors to support a gain range of ±1 V/V to ±10 V/V, and line outputs that have ±8 kV IEC ESD protection. The DRV603 (occasionally referred to as the '603) has built-in shutdown control for pop-free on/off control. The DRV603 has an external and internal undervoltage detector that mutes the output.

Using the DRV603 in audio products can reduce component count considerably compared to traditional methods of generating a 3-V_{rms} output. The DRV603 does not require a power supply greater than 5 V to generate its 8.5-V_{pp} output, nor does it require a split-rail power supply. The DRV603 integrates its own charge pump to generate a negative supply rail that provides a clean, pop-free ground biased 3-V_{rms} output.

The DRV603 is available in a 14-pin TSSOP.

If the low noise and trimmed dc-offset and external undervoltage mute function are not beneficial in the application, TI recommends the footprint compatible DRV602.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE	TRANSPORT MEDIA, QUANTITY
–40°C to 85°C	DRV603PW	RAIL, 90
	DRV603PWR	Tape and reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range

			VALUE	UNIT
	Supply voltage, V_{DD} to GND		–0.3 to 5.5	V
V_I	Input voltage		V_{SS} – 0.3 to V_{DD} + 0.3	V
R_L	Minimum load impedance		> 600	Ω
	EN to GND		–0.3 to V_{DD} +0.3	V
T_J	Maximum operating junction temperature range		–40 to 150	°C
T_{stg}	Storage temperature range		–40 to 150	°C
ESD	Electrostatic discharge, IEC ESD	OUTL, OUTR	±8	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JC}$ (°C/W)	$R_{\theta JA}$ (°C/W)	POWER RATING(1) AT $T_A \le 25°C$	POWER RATING(1) AT $T_A \le 70°C$
TSSOP-14 (PW)	35	115(2)	870 mW	348 mW

(1) Power rating is determined with a junction temperature of 125°C. This is the point where performance starts to degrade and long-term reliability starts to be reduced. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and reliability.
(2) These data were taken with the JEDEC high-K test printed circuit board (PCB). For the JEDEC low-K test PCB, the $R_{\theta JA}$ is 185°C/W.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	DC supply voltage	3	3.3	5.5	V
V_{IH}	High-level input voltage	EN		60		% of V_{DD}
V_{IL}	Low-level input voltage	EN		40		% of V_{DD}
T_A	Operating free-air temperature		0		70	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

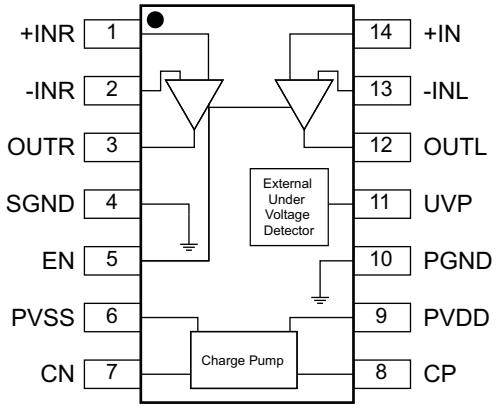
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage	V_{DD} = 3 V to 5 V, input grounded, unity gain			1	mV
PSRR	Power-supply rejection ratio	V_{DD} = 3 V to 5 V		88		dB
V_{OH}	High-level output voltage	V_{DD} = 3.3 V, R_L = 2.5 kΩ	3.1			V
V_{OL}	Low-level output voltage	V_{DD} = 3.3 V, R_L = 2.5 kΩ			–3.05	V
$\|I_{IH}\|$	High-level input current (EN)	V_{DD} = 5 V, V_I = V_{DD}			1	µA
$\|I_{IL}\|$	Low-level input current (EN)	V_{DD} = 5 V, V_I = 0 V			1	µA
I_{DD}	Supply current	V_{DD} = 3.3 V, no load, EN = V_{DD}		11		mA
		V_{DD} = 5 V, no load, EN = V_{DD}		12.5		
		Shutdown mode, V_{DD} = 3 V to 5 V			1	

OPERATING CHARACTERISTICS

V_{DD} = 3.3 V , T_A = 25°C, R_L = 2.5 kΩ, $C_{(PUMP)}$ = $C_{(PVSS)}$ = 1 µF , C_{IN} = 10 µF, R_{IN} = 10 kΩ, R_{fb} = 20 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage (outputs in phase)	THD = 1%, V_{DD} = 3.3 V, f = 1 kHz	2.05			V_{rms}
		THD = 1%, V_{DD} = 5 V, f = 1 kHz	3.01			
		THD = 1%, V_{DD} = 5 V, f = 1 kHz, R_L = 100 kΩ	3.1			
THD+N	Total harmonic distortion plus noise	V_O = 2 V_{rms}, f = 1 kHz		0.001%		
	Crosstalk	V_O = 2 V_{rms}, f = 1 kHz		–100		dB
I_O	Maximum output current	V_{DD} = 3.3 V		20		mA
R_{IN}	Input resistor range		1	10	47	kΩ
R_{fb}	Feedback resistor range		4.7	20	100	kΩ
	Slew rate			4.5		V/µs
	Maximum capacitive load			220		pF
V_N	Noise output voltage	BW = 20 Hz to 22 kHz, A-weighted		6		$µV_{rms}$
SNR	Signal-to-noise ratio	V_O = 3 Vrms, THD+N = 0.1%, BW = 22 kHz, A-weighted		112		dB
G_{BW}	Unity-gain bandwidth			8		MHz
A_{VO}	Open-loop voltage gain			150		dB
V_{uvp}	External undervoltage detection			1.25		V
I_{Hys}	External undervoltage detection hysteresis current			5		µA
f_{cp}	Charge pump frequency		225	450	675	kHz

PW PACKAGE
(TOP VIEW)

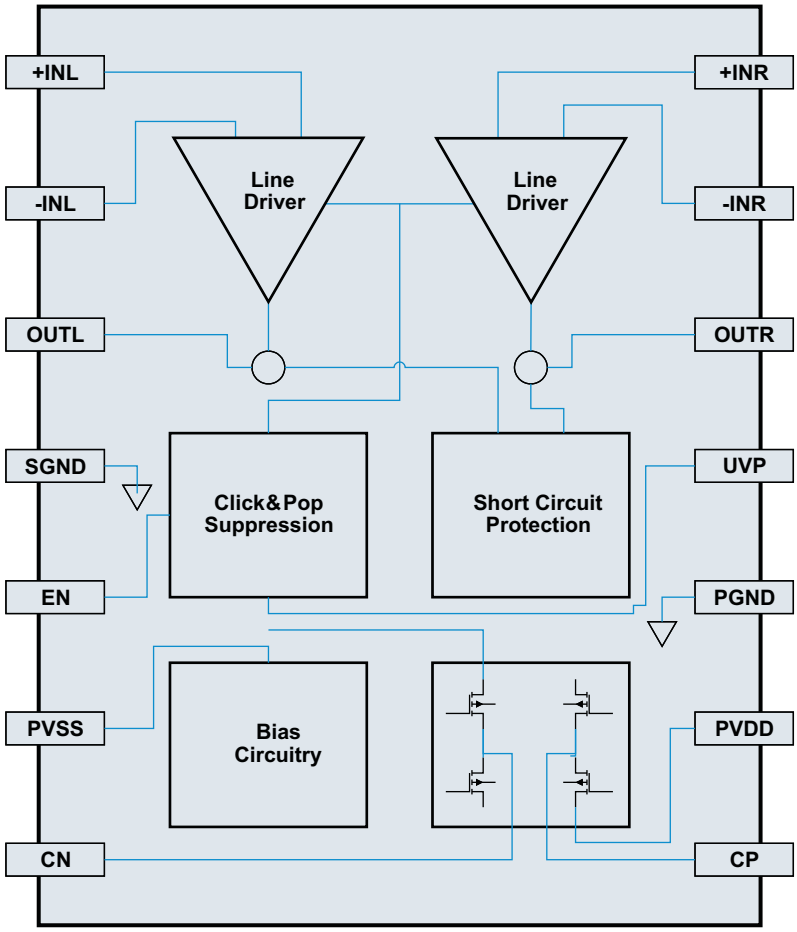


PIN FUNCTIONS

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
+INR	1	I	Right-channel OPAMP positive input
–INR	2	I	Right-channel OPAMP negative input
OUTR	3	O	Right-channel OPAMP output
SGND	4	P	Signal ground
EN	5	I	Enable input, active-high
PVSS	6	P	Supply voltage
CN	7	I/O	Charge-pump flying capacitor negative terminal
CP	8	I/O	Charge-pump flying capacitor positive terminal
PVDD	9	P	Positive supply
PGND	10	P	Power ground
UVP	11	I	Undervoltage protection input
OUTL	12	O	Left-channel OPAMP output
–INL	13	I	Left-channel OPAMP negative input
+INL	14	I	Left-channel OPAMP positive input

(1) I = input, O = output, P = power

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

V_{DD} = 3.3 V , T_A = 25°C, R_L = 2.5 kΩ, $C_{(PUMP)}$ = $C_{(VSS)}$ = 1 µF , C_{IN} = 10 µF, R_{IN} = 10 kΩ, R_{fb} = 20 kΩ (unless otherwise noted)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE V_{DD} = 3.3 V, R_L = 100 kΩ, f = 1 kHz

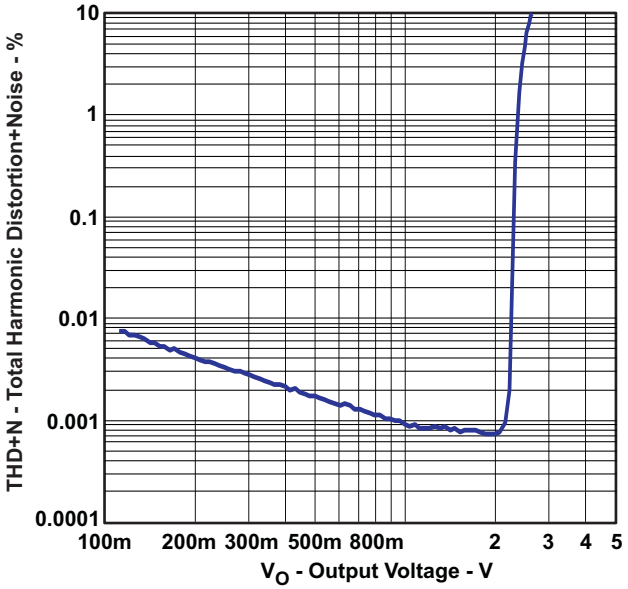


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE V_{DD} = 5 V, R_L = 100 kΩ, f = 1 kHz

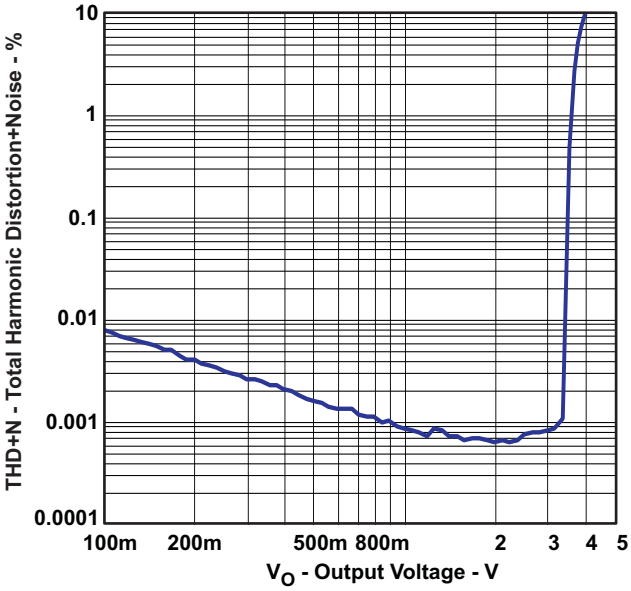


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE V_{DD} = 3.3 V, R_L = 2.5 kΩ, f = 1 kHz

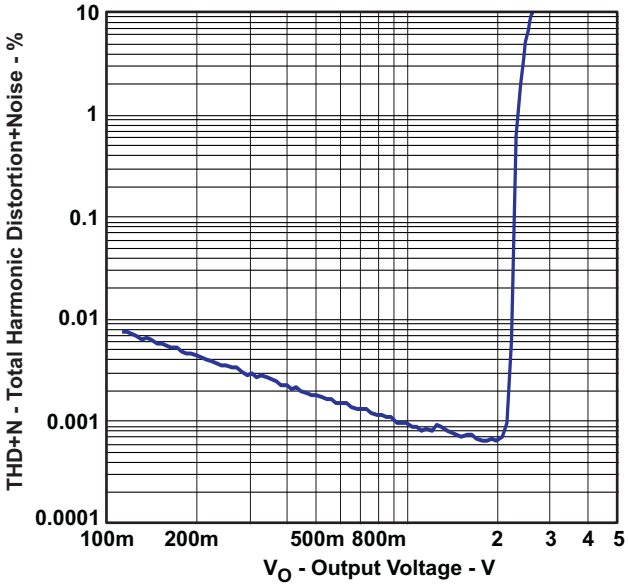


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE V_{DD} = 5 V, R_L = 600 Ω, f = 1 kHz

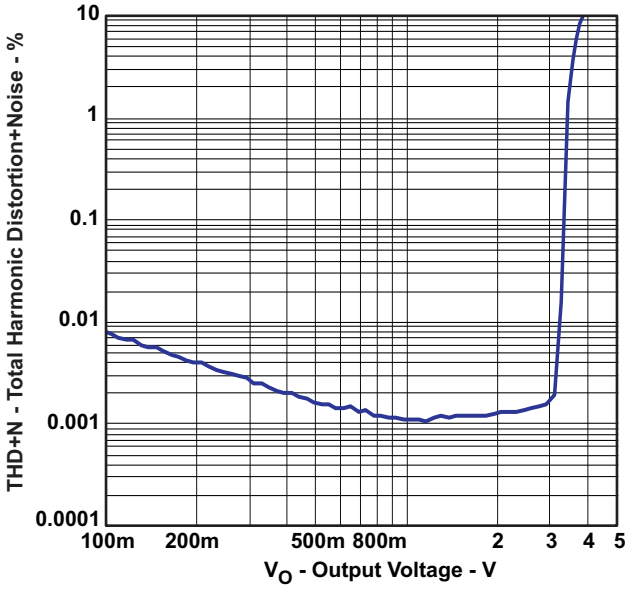


Figure 4.

TYPICAL CHARACTERISTICS (continued)

V_{DD} = 3.3 V , T_A = 25°C, R_L = 2.5 kΩ, $C_{(PUMP)}$ = $C_{(VSS)}$ = 1 µF , C_{IN} = 10 µF, R_{IN} = 10 kΩ, R_{fb} = 20 kΩ (unless otherwise noted)

TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY
V_{DD} = 3.3 V, R_L = 2.5 kΩ, V_O = 2 V_{rms}

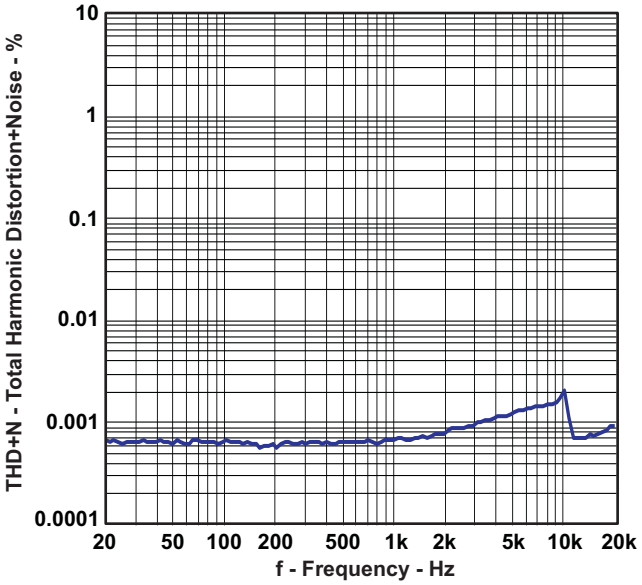


Figure 5.

TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY
V_{DD} = 5 V, R_L = 100 kΩ, V_O = 2 V_{rms}

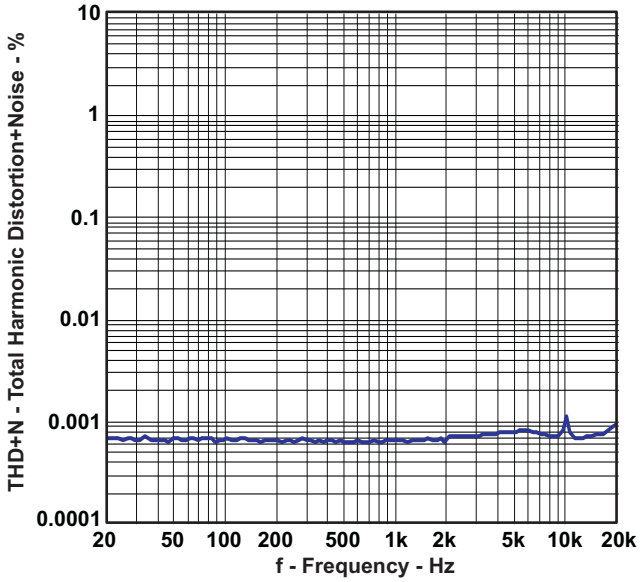


Figure 6.

PHASE vs FREQUENCY
V_{DD} = 5 V, R_L = 100 kΩ, V_O = 2 V_{rms}

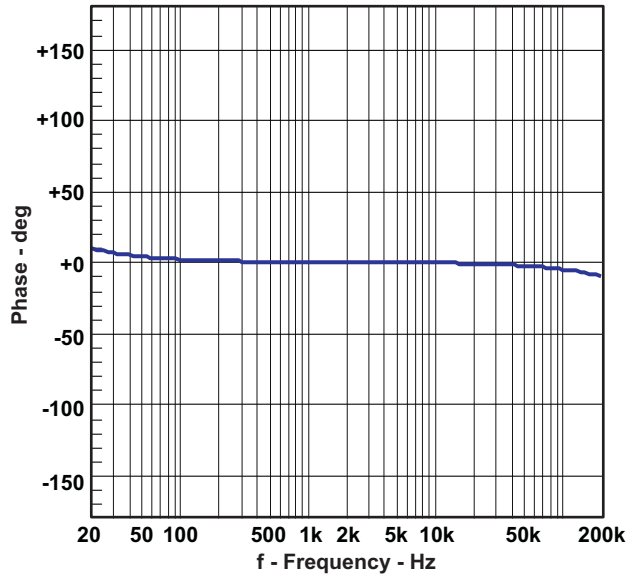


Figure 7.

GAIN vs FREQUENCY
V_{DD} = 5 V, R_L = 100 kΩ, V_O = 2 V_{rms}

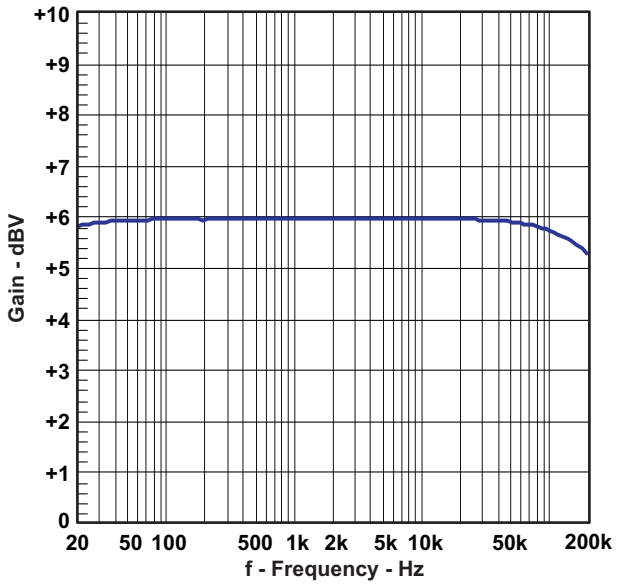


Figure 8.

TYPICAL CHARACTERISTICS (continued)

V_{DD} = 3.3 V , T_A = 25°C, R_L = 2.5 kΩ, $C_{(PUMP)}$ = $C_{(VSS)}$ = 1 µF , C_{IN} = 10 µF, R_{IN} = 10 kΩ, R_{fb} = 20 kΩ (unless otherwise noted)

FFT vs FREQUENCY
V_{DD} = 5 V, R_L = 100 kΩ, V_O = 3 V_{rms} (-60 dB)

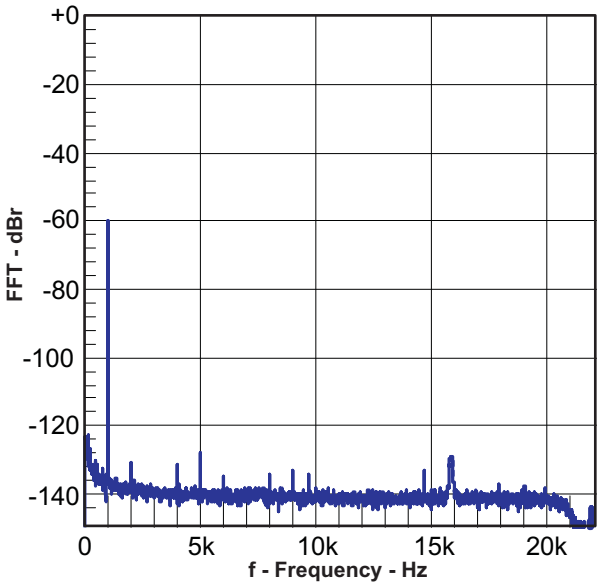


Figure 9.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

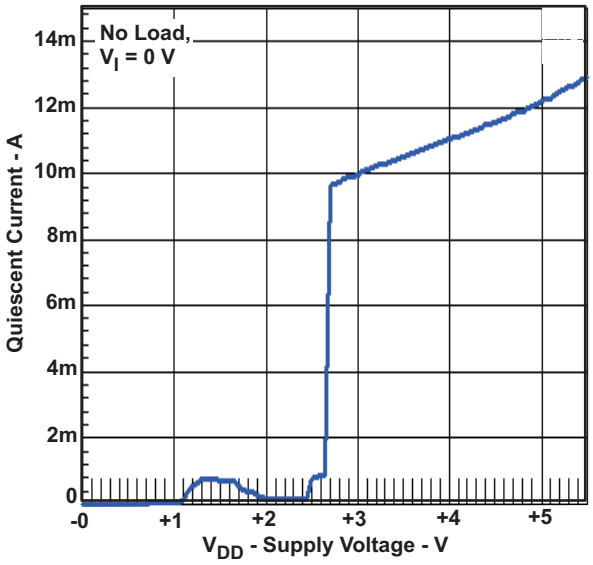


Figure 10.

APPLICATION INFORMATION

LINE DRIVER AMPLIFIERS

Single-supply line-driver amplifiers typically require dc-blocking capacitors. The top drawing in Figure 11 illustrates the conventional line-driver amplifier connection to the load and output signal.

DC blocking capacitors are often large in value, and a mute circuit is needed during power up to minimize click and pop. The output capacitor and mute circuit consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.

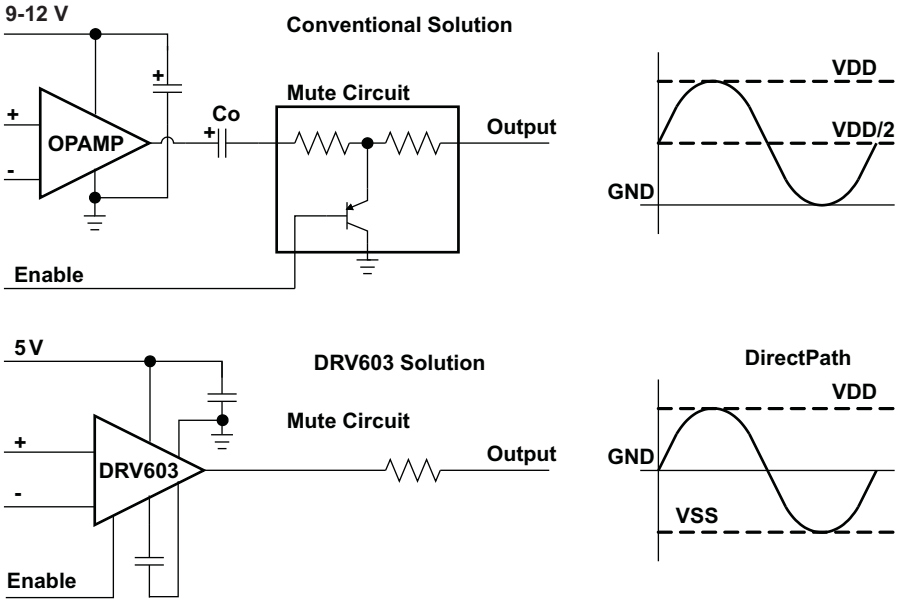


Figure 11. Conventional and DirectPath Line Driver

The DirectPath™ amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail.

Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click and pop reduction circuit, the DirectPath™ amplifier requires no output dc blocking capacitors.

The bottom block diagram and waveform of Figure 11 illustrate the ground-referenced line-driver architecture. This is the architecture of the DRV603.

CHARGE PUMP FLYING CAPACITOR AND PVSS CAPACITOR

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and a value of 1 µF is typical. Capacitor values that are smaller than 1 µF can be used, but the maximum output voltage may be reduced and the device may not operate to specifications.

DECOUPLING CAPACITORS

The DRV603 is a DirectPath™ line-driver amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the DRV603 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

GAIN-SETTING RESISTOR RANGES

The gain-setting resistors, R_{IN} and R_{fb}, must be chosen so that noise, stability, and input capacitor size of the DRV603 are kept within acceptable limits. Voltage gain is defined as R_{fb} divided by R_{IN}.

Selecting values that are too low demands a large input ac-coupling capacitor, C_{IN}. Selecting values that are too high increases the noise of the amplifier. Table 1 lists the recommended resistor values for different gain settings.

Table 1. Recommended Resistor Values

INPUT RESISTOR VALUE, R_{IN}	FEEDBACK RESISTOR VALUE, R_{fb}	DIFFERENTIAL INPUT GAIN	INVERTING INPUT GAIN	NONINVERTING INPUT GAIN
22 kΩ	22 kΩ	1 V/V	–1 V/V	2 V/V
15 kΩ	30 kΩ	1.5 V/V	–1.5 V/V	2.5 V/V
33 kΩ	68 kΩ	2.1 V/V	–2.1 V/V	3.1 V/V
10 kΩ	100 kΩ	10 V/V	–10 V/V	11 V/V

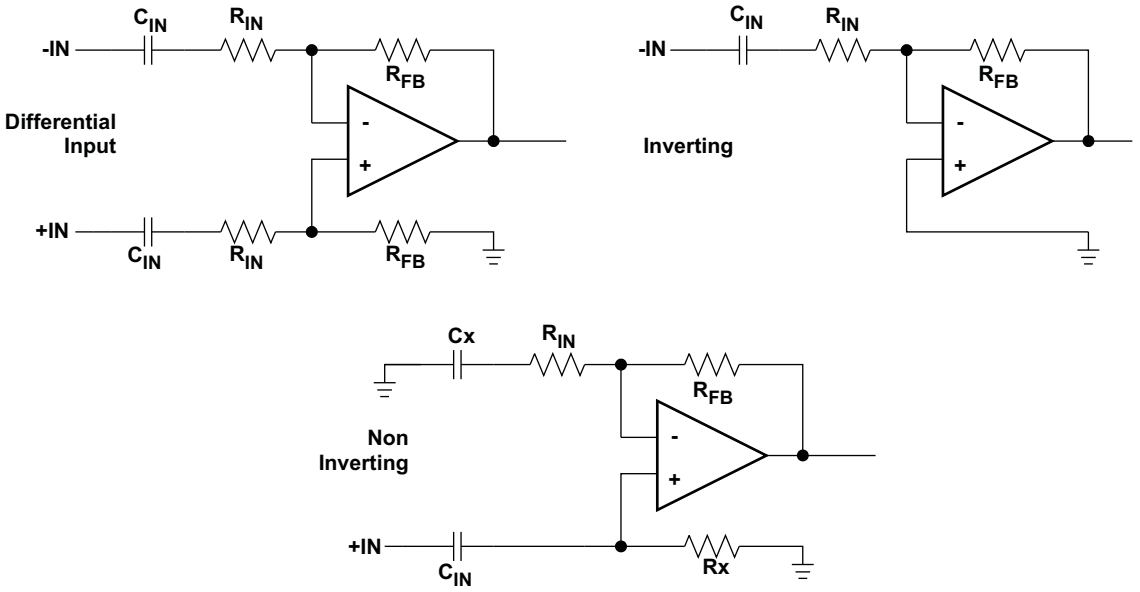


Figure 12. Differential, Inverting and Non-Inverting Gain Configurations

INPUT-BLOCKING CAPACITORS

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DRV603. These capacitors block the dc portion of the audio source and allow the DRV603 inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 1. Then the frequency and/or capacitance can be determined when one of the two values is given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \tag{1}$$

USING THE DRV603 AS A SECOND-ORDER FILTER

Several audio DACs used today require an external low-pass filter to remove out-of-band noise. This is possible with the DRV603, as it can be used like a standard OPAMP. Several filter topologies can be implemented, both single-ended and differential. In Figure 13 , a multi-feedback (MFB) with differential input and single-ended input is shown.

An ac-coupling capacitor to remove dc content from the source is shown; it serves to block any dc content from the source and lowers the dc-gain to 1, helping reducing the output dc-offset to minimum.

The component values can be calculated with the help of the TI FilterPro™ program available on the TI website at:

http://focus.ti.com/docs/toolsw/folders/print/filterpro.html

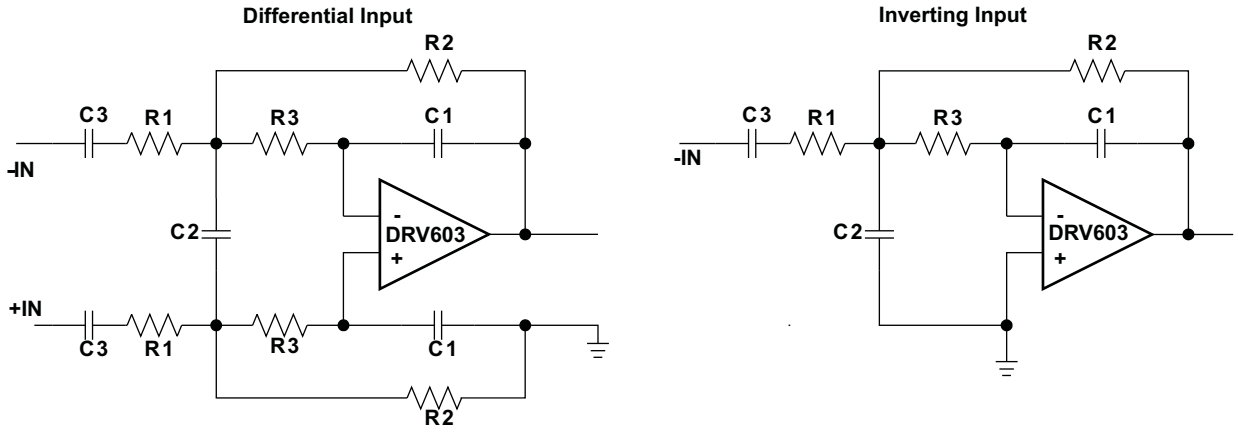


Figure 13. Second-Order Active Low-Pass Filter

The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small size ac-coupling capacitor. Using 5.6 kΩ for the resistors, C1 = 220 pF, and C2 = 470 pF, a DNR of 112 dB can be achieved with a 10-µF input ac-coupling capacitor.

POP-FREE POWER UP

Pop-free power up is ensured by keeping the $\overline{SD}$ (shutdown pin) low during power-supply ramp up and ramp down. The $\overline{SD}$ pin should be kept low until the input ac-coupling capacitors are fully charged before asserting the $\overline{SD}$ pin high to achieve pop-less power up. Figure 14 illustrates the preferred sequence.

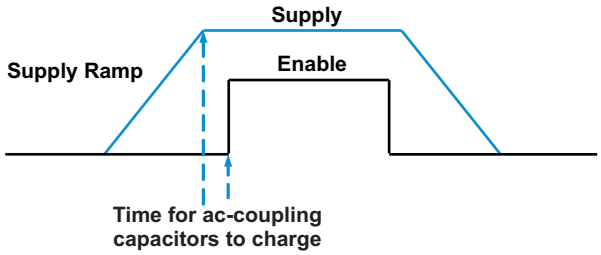


Figure 14. Power-Up Sequence

EXTERNAL UNDERVOLTAGE DETECTION

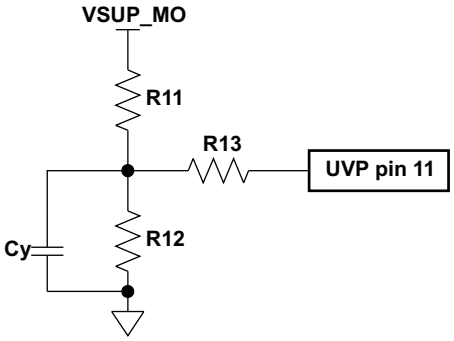
External undervoltage detection can be used to mute/shut down the DRV603 before an input device can generate a pop.

The shutdown threshold at the UVP pin is 1.25 V. The user selects a resistor divider to obtain the shutdown threshold and hysteresis for the specific application. The thresholds can be determined as follows:

V_{UVP} = 1.25 V × (R11 + R12) / R12
Hysteresis = 5 µA × R13 × (R11 + R12) / R12

with the condition R13 >> R11//R12.

For example, to obtain V_{UVP} = 5 V and 1-V hysteresis, R11 = 3 kΩ, R12 = 1 kΩ and R13 = 50 kΩ.



CAPACITIVE LOAD

The DRV603 has the ability to drive a high capacitive load up to 220 pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47 Ω or larger.

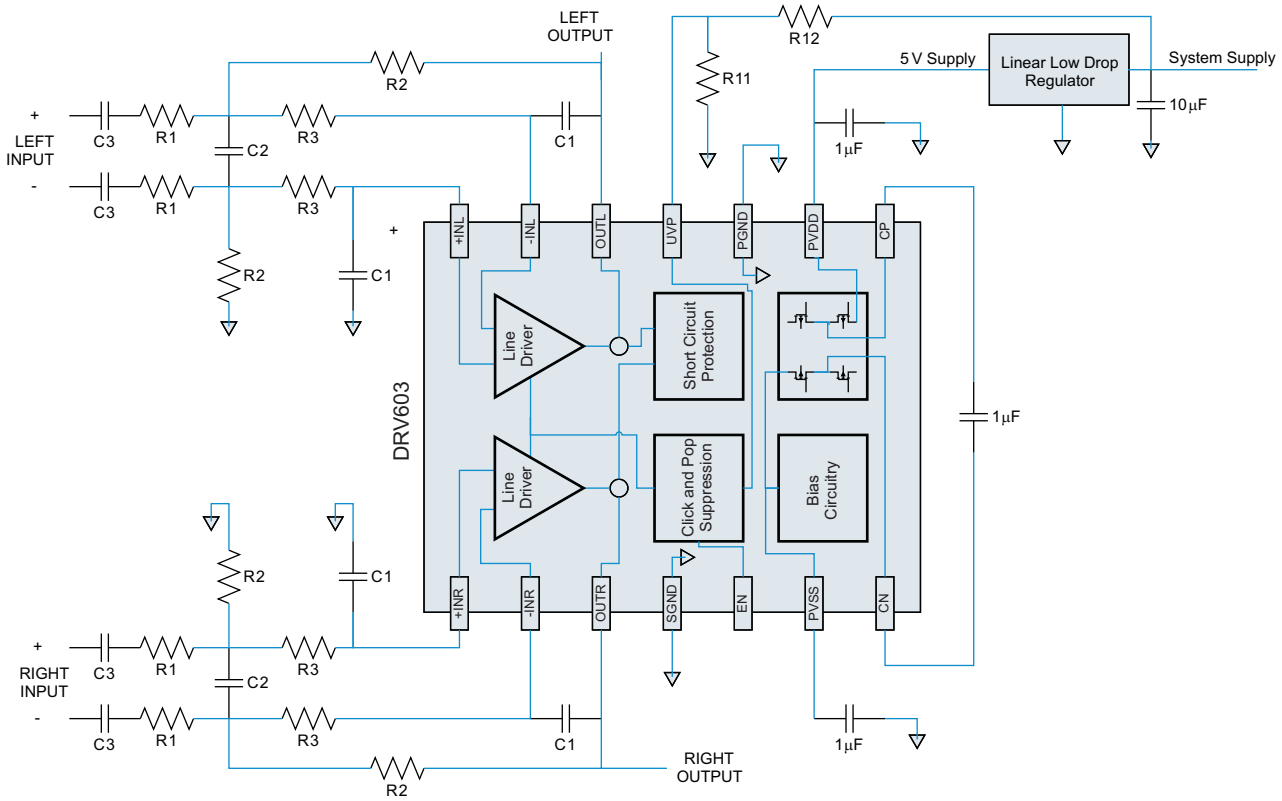
LAYOUT RECOMMENDATIONS

A proposed layout for the DRV603 can be seen in the DRV603EVM User's Guide (SLOU248), and the Gerber files can be downloaded from http://focus.ti.com/docs/toolsw/folders/print/drv603evm.html. To access this information, open the DRV603 product folder and look in the Tools and Software folder.

GAIN-SETTING RESISTORS

The gain-setting resistors, R_{IN} and R_{fb}, must be placed close to the input pins to minimize capacitive loading on these input pins and to ensure maximum stability of the DRV603. For the recommended PCB layout, see the DRV603EVM user's guide (SLOU248).

APPLICATION CIRCUIT



R1 = 5.6 kΩ, R2 = 5.6 kΩ, R3 = 5.6 kΩ, C1 = 220 pF, C2 = 470 pF

Differential-input, single-ended output, second-order filter

REVISION HISTORY

NOTE: Page numbers of current version may differ from previous versions.

Changes from Revision A (February 2009) to Revision B	Page
• Changed Crosstalk spec from –80dB to –100dB	3
• Added missing voltage value (1.25V) to *External Undervoltage Detection* threshold equation.	12

Changes from Revision B (October 2009) to Revision C **Page**

- Changed maximum operating junction temperature 2
- In Dissipation Ratings section, changed θ_{Jx} to $R_{\theta Jx}$ in three places and 185°C to 185°C/W 2
- Corrected reference to Figure 11 9
- Added cross-reference to Figure 13 11

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV603PW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV603
DRV603PW.A	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV603
DRV603PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV603
DRV603PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV603

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

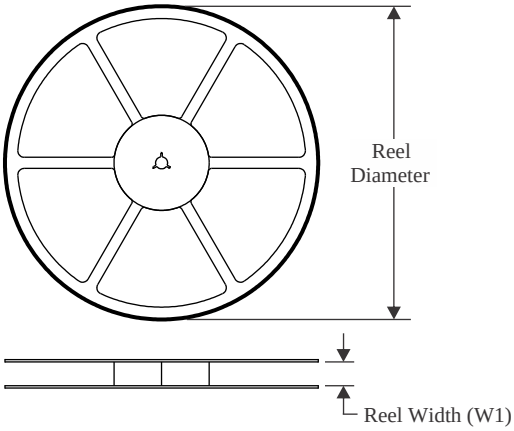
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

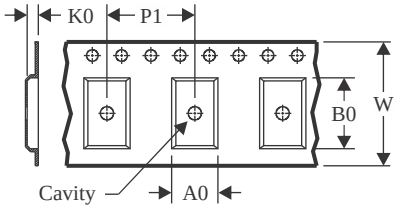
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

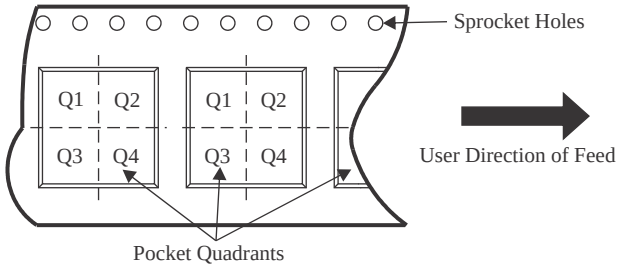


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

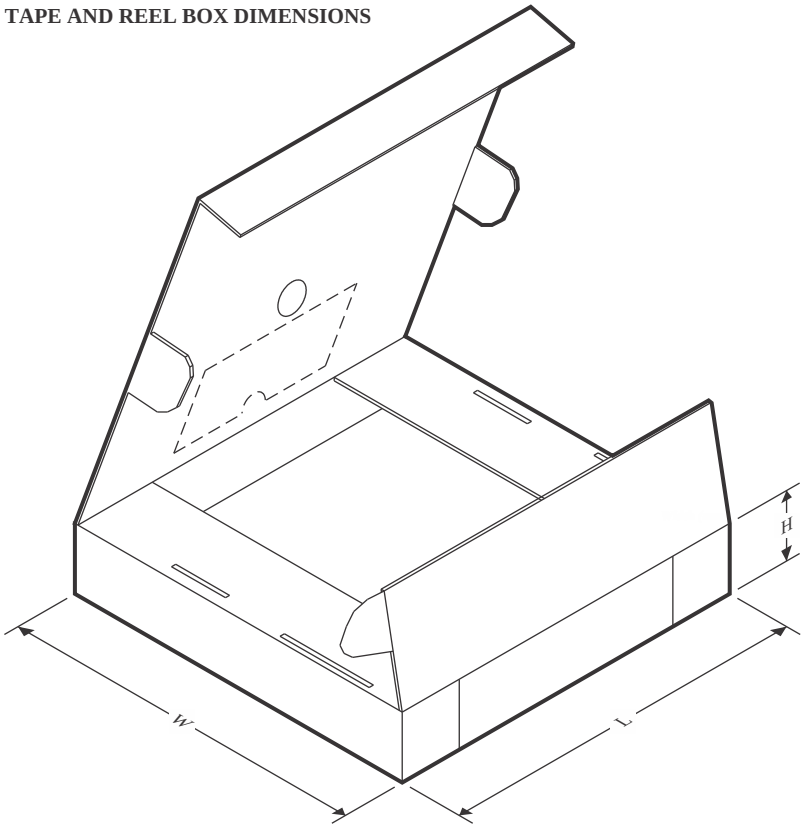
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV603PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

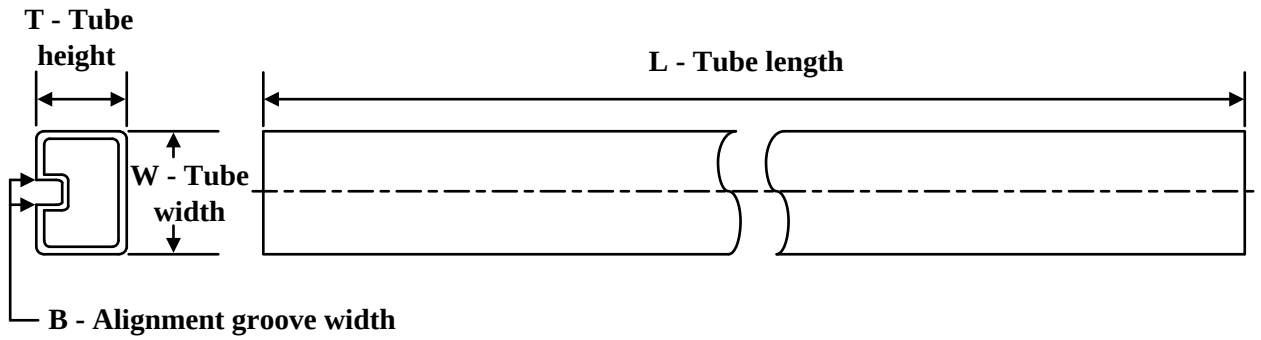
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV603PWR	TSSOP	PW	14	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

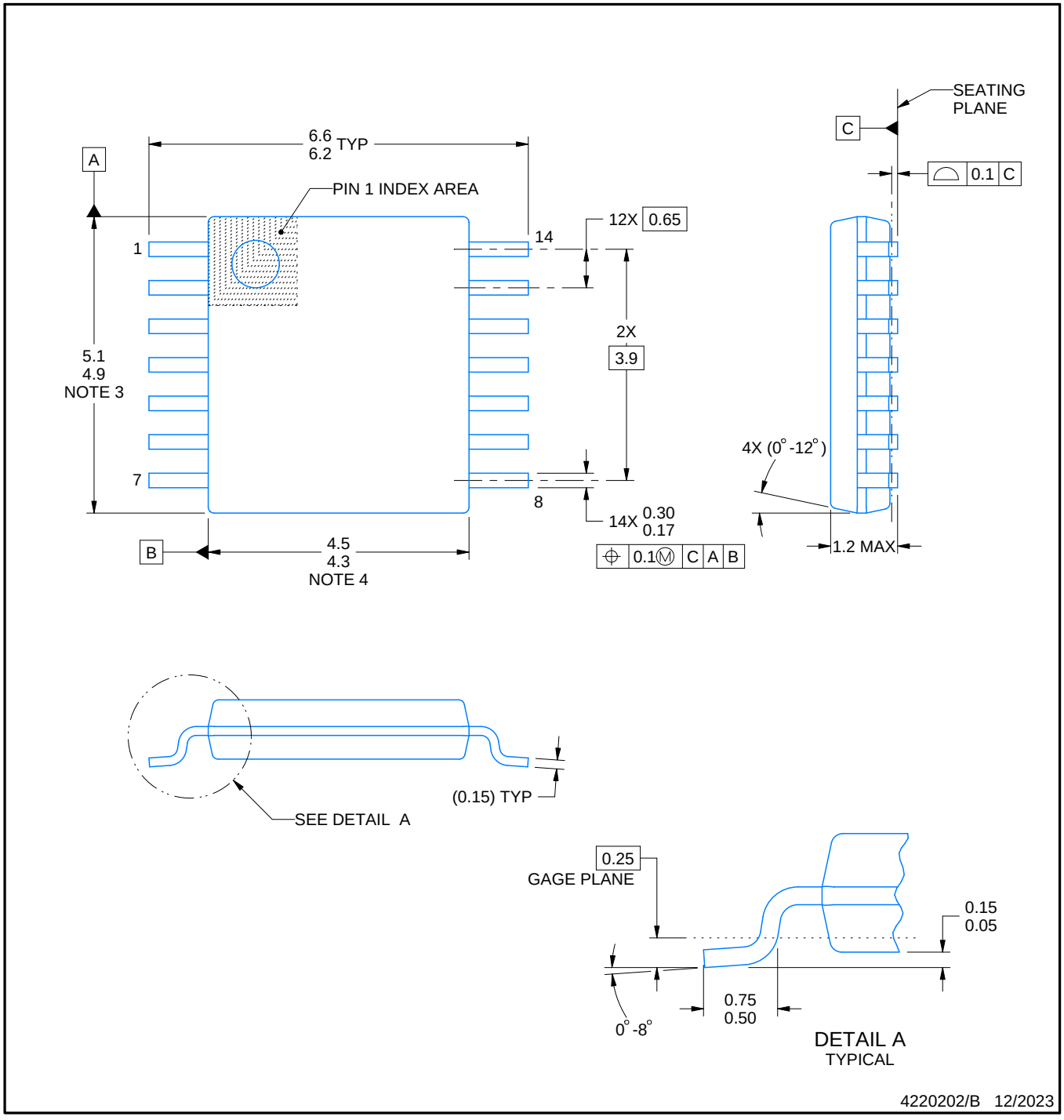
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV603PW	PW	TSSOP	14	90	530	10.2	3600	3.5
DRV603PW.A	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0014A

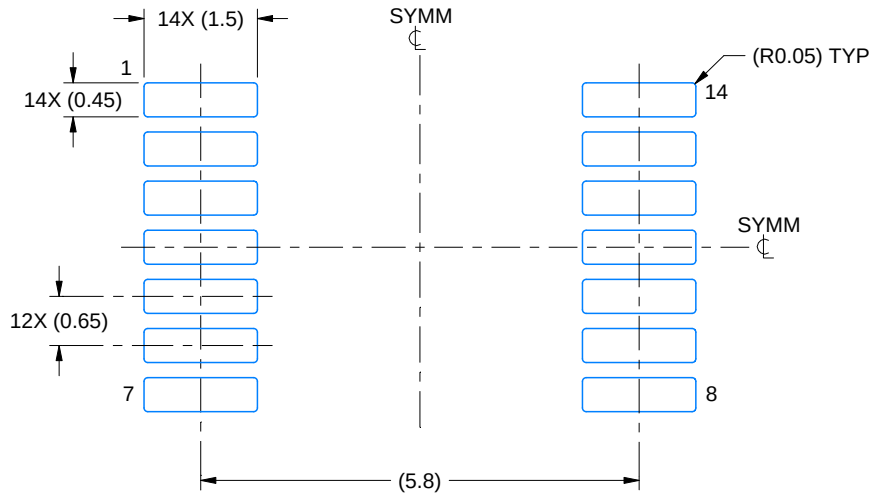
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

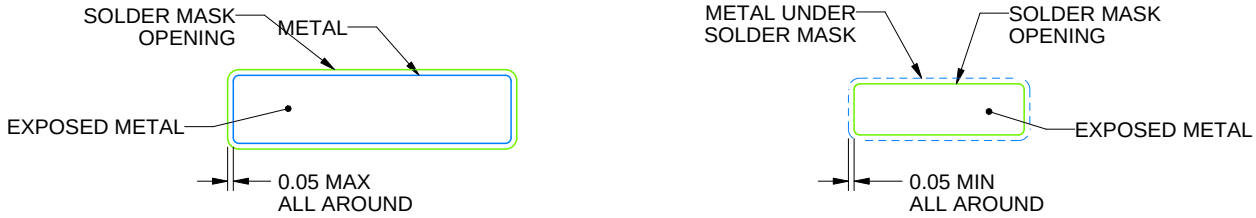


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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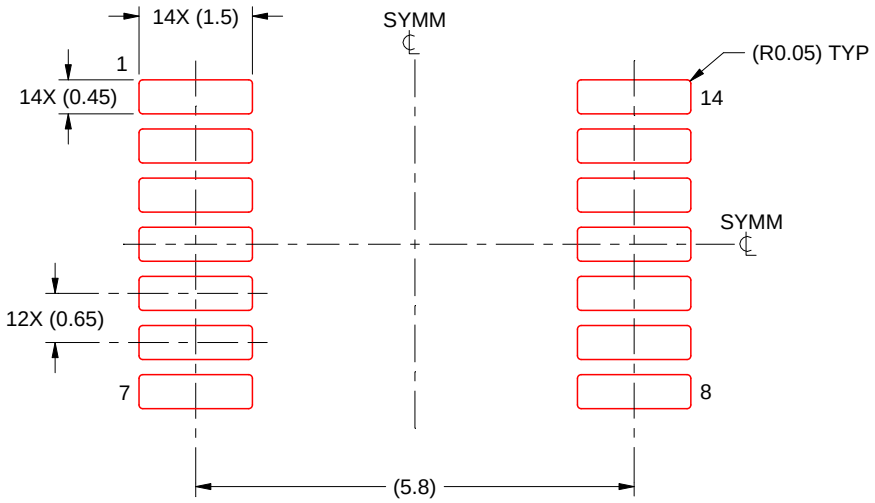
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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