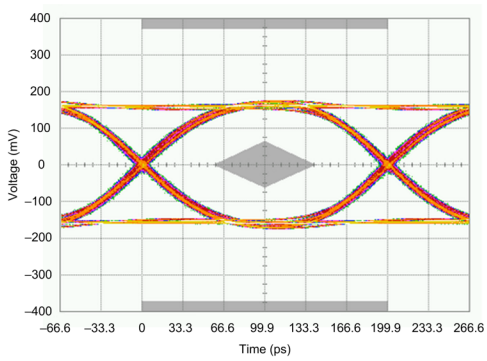
ADC31JB68 Single-channel, 16-bit, 500-MSPS analog-to-digital converter

1 Features

- Single Channel
- 16-Bit Resolution
- Maximum Clock Rate: 500 Msps
- Small 40-Pin QFN Package (6 x 6 mm)
- Input Buffer Input Bandwidth (3 dB): 1300 MHz
- Aperture Jitter: 80 fs
- On Chip Clock Divider: /1, /2, /4
- On Chip Dither
- Consistent Dynamic Performance Using Foreground and Background Calibration
- Input Amplitude and Phase Adjustment
- Input Full Scale: 1.7 Vpp
- Power Supplies: 1.2/1.8/3 V
- JESD204B Interface
  - Subclass 1 Compliant
  - 2 Lanes at 5 Gbps
- Support for Multi-chip Synchronization
- Key Specifications
  - Power Dissipation: 915 mW at 500 Msps
  - Performance at f_{in} = 210 MHz at –1 dBFS
    - SNR: 69.3 dBFS
    - NSD: –153.3 dBFS/Hz
    - SFDR: 80 dBc
    - Non-HD2,HD3: –91 dBFS
  - Performance at fin = 450 MHz at –1 dBFS
    - SNR: 67 dBFS
    - NSD: –151 dBFS/Hz
    - SFDR: 77 dBc HD2,3
    - Non-HD2,HD3: –89 dBFS

Transmitted Eye at Output of 18-Inch, 5-mil. FR4 Microstrip Trace at 5 Gb/s With Optimized De-Emphasis



2 Applications

- High IF Sampling Receivers
- Broadband Wireless
- Microwave Receivers
- Cable CMTS, DOCSIS 3.1 Receivers
- Communications Test Equipment
- Digitizers
- Software Defined Radio (SDR)
- Radar and Antenna Arrays

3 Description

The ADC31JB68 is a low-power, wide-bandwidth, 16-bit, 500-MSPS analog-to-digital converter (ADC). The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. This device is designed to sample input signals of up to 1.3 GHz.

The ADC31JB68 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with very-low power consumption. On-chip dither provides an very-clean noise floor. Embedded foreground and background calibration provides consistent performance over the temperature range, and minimizes part-to-part variation.

This device supports the JESD204B serial interface with data rates up to 5 Gbps on each of two lanes, enabling high system integration density.

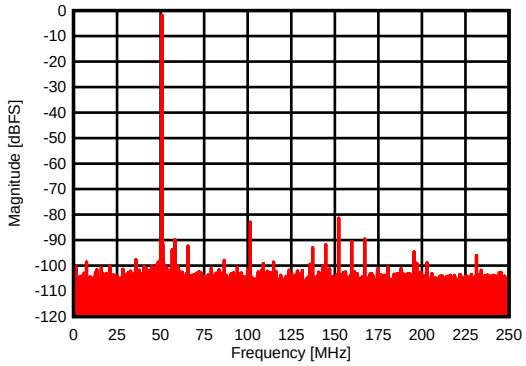
The ADC31JB68 comes in a 6-mm × 6-mm, 40-pin QFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC31JB68	WQFN (40)	6.00 mm × 6.00 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Spectrum With –1-dBFS, 450-MHz Input



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (September 2015) to Revision B — **Page**

- Added new note 2 to clarify power sequence in *Absolute Maximum Ratings* ... 6
- Changed text in last paragraph of *Power Supply Design* section to clarify power up sequence ... 62

Changes from Original (September 2015) to Revision A — **Page**

- Changed From: 1-page Product Preview To: Production datasheet ... 1
- Changed *Features* From: Non-HD2,HD3: TBD dBFS To: Non-HD2,HD3: –91 dBFS ... 1
- Changed *Features* From: Non-HD2,HD3: TBD dBFS To: Non-HD2,HD3: –89 dBFS ... 1

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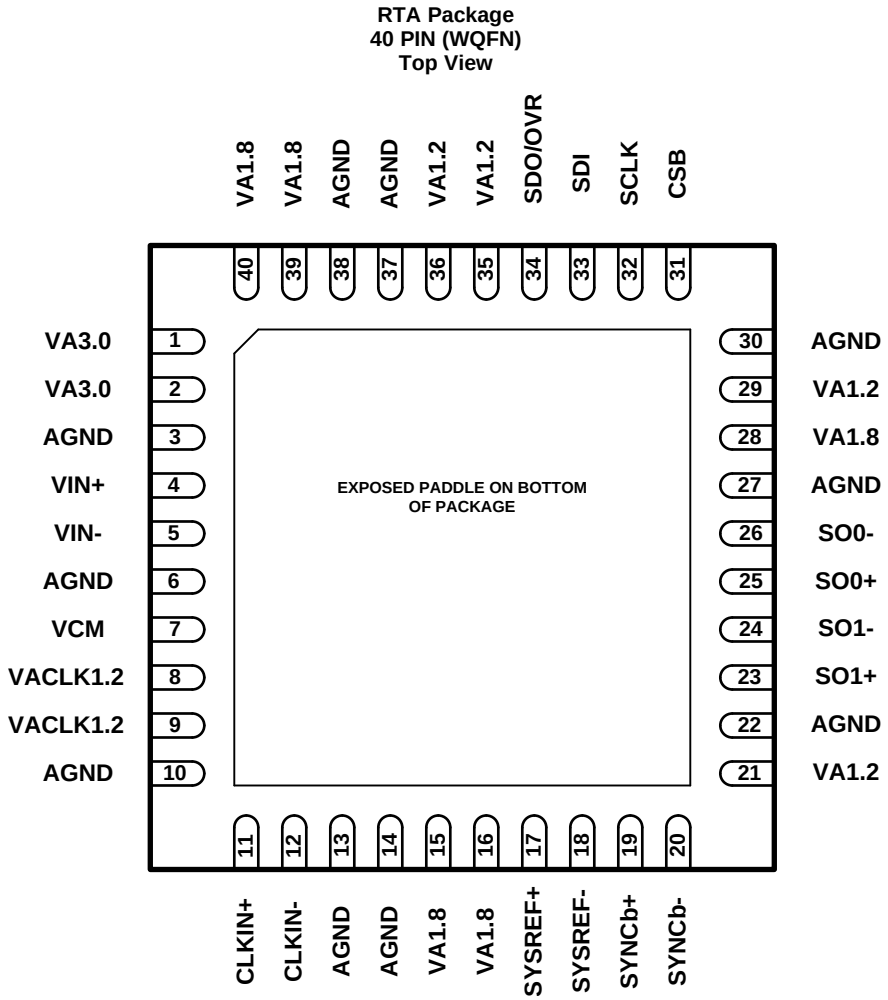
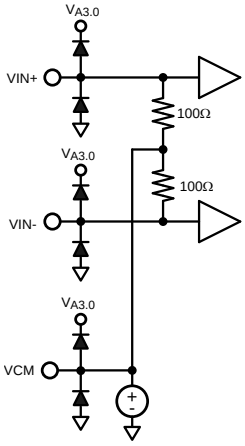
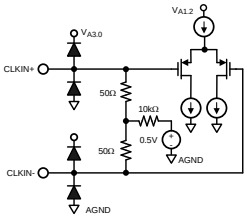
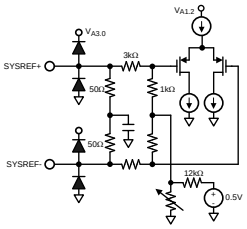
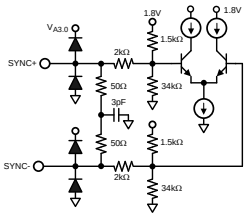
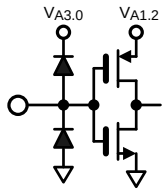
5 Pin Configuration and Functions

The ADC31JB68 is packaged in a 40-pin QFN package (6 x 6 x 0.8, 0.5 mm pin-pitch) with a bottom-side exposed paddle.



Pin Functions

PIN		TYPE or DIAGRAM	DESCRIPTION
NAME	NO.		
INPUT/REFERENCE			
VIN+ VIN–	4, 5		Differential analog input pins. The differential full-scale signal level is 1.7 Vpp. Each input pin is terminated to the internal 1.6V common-mode reference with a 100 Ω resistor for a 200 Ω total differential termination.
VCM	7		Input Interface Common mode voltage. This pin must be bypassed to AGND with a low ESL (equivalent series inductance) 0.1 µF capacitor that is placed as close to the pin as possible to minimize stray inductance. A 10 µF capacitor should also be placed in parallel. It is recommended to use VCM to provide the common mode voltage for the differential analog inputs. The input common-mode bias is provided internally for the ADC input, therefore external use of VCM is recommended but not strictly required. The recommended decoupling is always required.
CLOCK/SYNC			
CLKIN+ CLKIN–	11, 12		Differential device clock input pins. AC coupling is recommended for coupling the clock input to these pins. DC biasing of the clock receiver is provided internally. Each pin is internally terminated to the 500mV DC bias with 50 Ω resistor for a 100 Ω total internal differential termination resistor. Sampling occurs on the falling edge of the differential signal (CLKIN+) − (CLKIN-).
SYSREF+, SYSREF–	17, 18		Differential SYSREF signal input pins. Each pin is internally terminated to the DC bias with a large resistor. An internal 100 Ω differential termination is provided therefore an external termination is not required. Additional resistive components in the input structure give the SYSREF input a wide input common mode range.
SYNCb+ SYNCb–	19, 20		Differential SYNCb signal input pins. DC coupling is required for coupling the SYNCb signal to these pins. Each pin is internally terminated to the DC bias with a large resistor. An internal 100 Ω differential termination is provided therefore an external termination is not required. Additional resistive components in the input structure give the SYNCb input a wide input common mode range. The SYNCb signal is active low and is therefore asserted when the voltage at SYNCb+ is less than at SYNCb–.
SERIAL INTERFACE (SPI)			
SCLK	32		SPI Interface Serial Clock pin. Serial data is shifted into and out of the device synchronous with this clock signal. Compatible with 1.2–3.0V CMOS logic levels.
CSB	31		SPI Interface Chip Select pin. When this signal is asserted, SCLK is used to clock input serial data on the SDI pin or output serial data on the SDO pin. When this signal is de-asserted, the SDO pin is high impedance and the input data is ignored. Active low. A 1kΩ pull-up resistor to the VA1.8 supply is recommended to prevent undesired activation of the SPI bus. Compatible with 1.2–3.0V CMOS logic levels.
SDI	33		SPI Interface Data Input pin. Serial data is shifted into the device on this pin while the CSB signal is asserted. Compatible with 1.2-3.0V CMOS logic levels.

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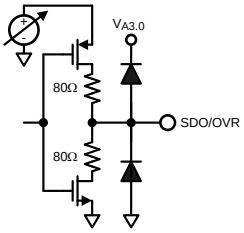
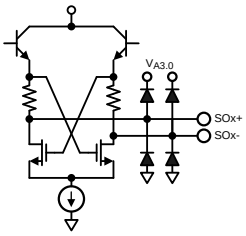
Pin Functions (continued)

PIN		TYPE or DIAGRAM	DESCRIPTION
NAME	NO.		
SDO/OVR	34		SPI Data Output and Over-Range pin. Dual mode pin. When configured as SDO, serial data of the SPI is shifted out of the device on this pin while CSB is asserted. When configured as OVR, the over-range signal is output. Pin mode configurable via the SPI. Output voltage is configurable to 1.2V, 1.8V, or 3.0V CMOS logic levels via the SPI. Default configuration outputs the SDO at a 1.8V logic level.
DIGITAL OUTPUT INTERFACE			
SO0+, SO0–, SO1+, SO1–	25, 26, 23, 24		Differential High Speed Serial Data Lane pins. These pins must be AC coupled to the receiving device. The differential trace routing from these pins must maintain a 100 Ω characteristic impedance.
POWER SUPPLY			
VA3.0	1, 2	Supply Input Pin	3 V Analog Power Supply pin. This pin must be connected to a quiet source and decoupled to AGND with a 0.1 µF capacitor located close to each pin and a second 0.1 µF capacitor on bottom layer.
VA1.8	15, 16, 28, 39, 40	Supply Input Pin	1.8 V Analog Power Supply pins. These pins must be connected to a quiet source and decoupled to AGND with a 0.1 µF capacitor located close to each pin and a second 0.1 µF capacitor on bottom layer.
VA1.2	21, 29, 35, 36	Supply Input Pin	1.2 V Analog Power Supply pins. These pins must be connected to a quiet source and decoupled to AGND with a 0.1 µF capacitor located close to each pin and a second 0.1 µF capacitor on bottom layer.
VACLK1.2	8, 9	Supply Input Pin	1.2 V Analog Power Supply pins for internal clock path. These pins must be connected to a quiet source and decoupled to AGND with a 0.1 µF capacitor located close to each pin and a second 0.1 µF capacitor on bottom layer.
AGND	3, 6, 10, 13, 14, 22, 27, 30, 37, 38	Analog Ground	Analog Ground. Solid ground reference planes under the device are recommended.
Exposed Thermal Pad			Exposed Thermal Pad. The exposed pad must be connected to the AGND ground plane electrically and with good thermal dissipation properties to ensure rated performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
Supply voltage range [2]	VA3.0	–0.3	4.2	V
	VA1.8	–0.3	2.35	V
	VA1.2, VACLK1.2	–0.3	1.55	V
Voltage applied to input pins	VIN+, VIN–	VCM – 0.75	VCM + 0.75	V
	VCM	–0.3	$V_{A3.0}$ + 0.3, not to exceed 4.2 V	V
	CLKIN+, CLKIN–, SYSREF+, SYSREF–	–0.3	1.55	V
	SYNCb+, SYNCb–	–0.3	$V_{A1.8}$ + 0.3	V
	SCLK, SDI, CSb	–0.3	$V_{A3.0}$ + 0.3, not to exceed 4.2 V	V
Temperature	Operating junction temperature range, T_J [3]		125	°C
	Storage temperature, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Power sequence must be followed as stated in the *Power Supply Design* section. Failure to follow the required power sequence may result in unwanted voltage on the VA1.8 pin that can exceed the absolute maximum voltage of 2.35 VDC.
(3) Prolonged use at this temperature may increase the device failure-in-time (FIT) rate.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 [2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

operating conditions specified over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	VA3.0	2.85	3.15	V
	VA1.8	1.7	1.9	V
	VA1.2, VACLK1.2	1.15	1.25	V
CLKIN± duty cycle	CLKDIV = 1	30%	70%	
Operating free-air temperature range, T_A		–40	85	°C
Operating junction temperature range, T_J			105	°C

6.4 Thermal Information

THERMAL METRIC [1]		ADC31JB68 RTA (WQFN) (40) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.4	°C/W

(1) For more information about thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics: Converter Performance

typical values at T_A = 25 °C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, VA3.0 = 3 V; VA1.8 = 1.8 V; VA1.2 = VACLK1.2 = 1.2 V; –1 dBFS differential input; $R_{(term)}$ = 100 Ω (unless otherwise noted)

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
	Resolution	No missing codes			16	Bits
G_{VAR}	Gain variation	Part-to-part variation of input voltage to output code gain between different parts		1		%FSR
TG	Gain temperature drift	Drift of input voltage to output code gain across temperature		100		ppm(FSR)/°C
V_{OFF}	Input voltage offset			0.2		%FSR
TV_{OFF}	Input voltage offset temperature drift			9		ppm(FSR)/°C
DNL	Differential nonlinearity	Sinusoidal histogram, 10-MHz input		±0.23		LSB
INL	Integral nonlinearity	Sinusoidal histogram, 10-MHz input		±7.1		LSB
DYNAMIC AC CHARACTERISTICS						
BW_{3dB}	Analog input bandwidth	See measurement configuration in Figure 64		1300		MHz
SNR	Signal to noise ratio	f_{IN} = 10 MHz, A_{IN} = –40 dBFS		70.6		dBFS
		f_{IN} = 10 MHz		70.3		
		f_{IN} = 100 MHz		70.1		
		f_{IN} = 210 MHz	68.3	69.3		
		f_{IN} = 210 MH, T_A = 25°C	68.4	69.3		
		f_{IN} = 350 MHz		68.1		
		f_{IN} = 450 MHz		67.0		
NSD	Noise spectral density	f_{IN} = 10 MHz, A_{IN} = –40 dBFS		–154.6		dBFS/Hz
		f_{IN} = 10 MHz		–154.3		
		f_{IN} = 100 MHz		–154.1		
		f_{IN} = 210 MHz	–152.3	–153.3		
		f_{IN} = 210 MHz, T_A = 25°C	–152.4	–153.3		
		f_{IN} = 350 MHz		–152.1		
		f_{IN} = 450 MHz		–151.0		
SINAD	Signal to noise and distortion ratio	f_{IN} = 10 MHz		69.9		dBFS
		f_{IN} = 100 MHz		69.5		
		f_{IN} = 210 MHz	67.4	68.9		
		f_{IN} = 210 MHz, T_A = 25ºC	67.8	68.9		
		f_{IN} = 350 MHz		67.6		
		f_{IN} = 450 MHz		66.5		dBFS
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.3		Bits
		f_{IN} = 100 MHz		11.3		
		f_{IN} = 210 MHz	10.9	11.2		
		f_{IN} = 210 MH, T_A = 25°C	11.0	11.2		
		f_{IN} = 350 MHz		10.9		
		f_{IN} = 450 MHz		10.8		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		83		dBc
		f_{IN} = 100 MHz		81		
		f_{IN} = 210 MHz	74	80		
		f_{IN} = 210 MH, T_A = 25°C	75	80		
		f_{IN} = 350 MHz		79		
		f_{IN} = 450 MHz		77		

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Electrical Characteristics: Converter Performance (continued)

typical values at T_A = 25 °C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, VA3.0 = 3 V; VA1.8 = 1.8 V; VA1.2 = VACLK1.2 = 1.2 V; –1 dBFS differential input; $R_{(term)}$ = 100 Ω (unless otherwise noted)

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz		–83		dBc
		f_{IN} = 100 MHz		–81		
		f_{IN} = 210 MHz	–74	–84		
		f_{IN} = 210 MH, T_A = 25°C	–75	–84		
		f_{IN} = 350 MHz		–84		
		f_{IN} = 450 MHz		–77		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz		–92		dBc
		f_{IN} = 100 MHz		–83		
		f_{IN} = 210 MHz	–74	–80		
		f_{IN} = 210 MHz T_A = 25°C	–75	–80		
		f_{IN} = 350 MHz		–79		
		f_{IN} = 450 MHz		–87		
Non-HD2, HD3	Spurious free dynamic range excluding HD2, HD3	f_{IN} = 10 MHz		–93		dBFS
		f_{IN} = 100 MHz		–89		
		f_{IN} = 210 MHz	–83	–91		
		f_{IN} = 210 MH, T_A = 25°C	–83	–91		
		f_{IN} = 350 MHz		–88		
		f_{IN} = 450 MHz		–89		
THD	Total harmonic distortion	f_{IN} = 10 MHz		–81		dBc
		f_{IN} = 100 MHz		–78		
		f_{IN} = 210 MHz	–72	–78		
		f_{IN} = 210 MH, T_A = 25°C	–73	–78		
		f_{IN} = 350 MHz		–73		
		f_{IN} = 450 MHz		–72		
IMD3	Two–tone intermodulation distortion	Worst-case IMD3 spur adjacent to the input tones, f_1 = 200 MHz, f_2 = 210 MHz, A_{IN} = –7-dBFS/tone		–89		dBc

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6.6 Electrical Characteristics: Power Supply

typical values at T_A = 25°C, full temperature range is t_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, VA3.0 = 3 V; VA1.8 = 1.8 V; VA1.2 = VACLK1.2 = 1.2 V; –1 dBFS differential input, and $R_{(term)}$ = 100 Ω (unless otherwise noted)

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
	3-V analog supply (VA3.0)		2.85	3	3.15	V
	1.8-V analog supply (VA1.8)		1.7	1.8	1.9	V
	1.2-V analog supply (VA1.2)		1.15	1.2	1.25	V
	1.2-V analog supply for clock signal path (VACLK1.2)		1.15	1.2	1.25	V
$I_{(A3.0)}$	3-V analog supply current			61		mA
$I_{(A1.8)}$	1.8-V analog supply current			272		mA
$I_{(A1.2)}$	1.2-V analog supply current	Sum of current from VA1.2 and VACLK1.2 supplies		197		mA
P_D	Power dissipation	Total power dissipation; Fin = 10 MHz		915		mW
P_{PD}	Power down power dissipation	Power in power down state, no external clock		17		mW
P_{SL}	Sleep power dissipation	Power in sleep state, no external clock		17		mW
	Sensitivity to supply noise	Power of spectral spur resulting from a 100-mV sinusoidal signal modulating a supply at 500 kHz. Analog input is a –1-dBFS, 210-MHz single tone. In all cases, the spur appears as part of a pair symmetric about the fundamental that scales proportionally with the fundamental amplitude.				dBFS
		VA3.0		–81		
		VA1.8		–55		
		VA1.2 and VACLK1.2		–35		

6.7 Electrical Characteristics: Interface

typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, VA3.0 = 3 V; VA1.8 = 1.8 V; VA1.2 = VACLK1.2 = 1.2 V; –1 dBFS differential input, and $R_{(term)}$ = 100 Ω (unless otherwise noted) (see the *Interface Circuits* section)

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUTS (VIN+, VIN-)						
$V_{(FSR)}$	Full-scale range voltage	Differential peak-to-peak		1.7		V
V_{CM}	Nominal input common-mode voltage			1.6		V
ΔV_{CM}	Maximum input common mode voltage range			V_{CM} ± 0.05		V
R_{IN}	Input termination resistance	Differential resistance at dc		190		Ω
C_{IN}	Input capacitance	Differential		4.6		pF
INPUT COMMON MODE REFERENCE (VCM)						
$V_{(VCM)}$	Common-mode reference voltage output			1.6		V
$I_{(VCM)}$	Maximum VCM pin current load			1		mA
CLOCK INPUT (CLKIN+, CLKIN-)						
V_{ID-MAX}	Maximum input voltage swing (1)	Differential peak voltage			1000	mV
V_{ID-MIN}	Minimum input voltage swing (1)	Differential peak voltage		250		mV
dV_{SS}/dt	Input edge rate at zero crossing (1)	Recommended minimum		5		V/ns
$V_{(IS-BIAS)}$	Input common-mode internal bias voltage (2) (1)			0.5		V
$V_{(IS-IN)}$	Externally applied common-mode voltage (1)	DC-coupled interface		0.5 ± 0.1		V
$Z_{(rdiff)}$	Input termination resistance (2)	Differential resistance at dc		100		Ω
Z_{tt}	Common-mode internal bias source impedance (2)			10		kΩ
C_T	Input capacitance (2)	Differential		2		pF
SYSREF INPUT (SYSREF+, SYSREF-)						
V_{ID-MAX}	Maximum input voltage swing (1)	Differential peak voltage			1000	mV
V_{ID-MIN}	Minimum input voltage swing (1)	Differential peak voltage		250		mV
$V_{(IS-BIAS)}$	Input common-mode internal bias voltage (1)			0.5		V
$V_{(IS-IN)}$	Externally applied common mode voltage (1)	DC-coupled interface, typical value depends on the configuration of the SYS_CM parameter				V
		SYS_CM = 00		0.5 ± 0.1		
		SYS_CM = 01		0.8 ± 0.2		
		SYS_CM = 10		1.25 ± 0.25		
		SYS_CM = 11		1.75 ± 0.25		
$Z_{(rdiff)}$	Input termination resistance (2)	Differential resistance at dc		100		Ω
Ztt	Common-mode internal bias source impedance (2)			14		kΩ
C_T	Input capacitance (2)	Differential		1		pF
SYNCb INPUT (SYNCb+, SYNCb-)						
V_{ID}	Input voltage swing (1)	Differential peak voltage		350		mV
$V_{(IS-IN)}$	Externally applied common-mode voltage (1)	DC-coupled interface		1.25 ± 0.75		V

(1) Specification applies to the electrical level diagram of Figure 26
(2) Specification applies to the electrical circuit diagram of Figure 27

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Electrical Characteristics: Interface (continued)

typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, VA3.0 = 3 V; VA1.8 = 1.8 V; VA1.2 = VACLK1.2 = 1.2 V; –1 dBFS differential input, and $R_{(term)}$ = 100 Ω (unless otherwise noted) (see the *Interface Circuits* section)

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
$Z_{(rdiff)}$	Input termination resistance (2)	Differential resistance at dc		100		Ω
C_T	Input capacitance (2)	Differential		1		pF
SERDES OUTPUT (SO0+/-, SO1+/-) Meets JESD204B LV-OIF-11G-SR Standard						
V_{OD}	Output differential voltage (3)	Differential peak-peak voltage, de-emphasis disabled (DEM = 0)				mV
		VOD = 0		400		
		VOD = 1		470		
		VOD = 2		540		
		VOD = 3		610		
		VOD = 4		670		
		VOD = 5		740		
		VOD = 6		790		
		VOD = 7		840		
$R_{(deepm)}$	Transmitter de-emphasis range	Configurable via SPI, VOD configured to 4				dB
		DEM=0		0.0		
		DEM=1		–0.8		
		DEM=2		–2.4		
		DEM=3		–3.8		
		DEM=4		–4.9		
		DEM=5		–6.3		
		DEM=6		–7.7		
		DEM=7		–10.3		
I_{SC}	Transmitter short circuit current	Transmitter terminals shorted to each other or ground, power on		23		mA
$Z_{(ddiff)}$	Differential output impedance (4)			100		Ω
$R_{L(ddiff)}$	Differential output return loss magnitude	Relative to 100 Ω, for frequencies from 100 MHz to 0.75 × baud rate; default VOD and DEM.		–8.5		dB
SCLK, SDI, CSB INPUT						
V_{IH}	Logical 1 input voltage	Inputs are compatible with 1.2-V up to 3-V logic.	0.9			V
V_{IL}	Logical 0 input voltage				0.3	V
I_{IN0}	Logic low input current			4		nA
I_{IN1}	Logic high input current			–8		nA
C_{IN}	Input capacitance			2		pF
SDO/OVR OUTPUT						
V_{OH}	Logical 1 output voltage (5)	V_{SPI} = 1.2 V, 1.8 V, or 3 V, configurable via SPI	V_{SPI} – 0.2	V_{SPI} (5)		V
V_{OL}	Logical 0 output voltage (5)			0	0.3	V
$+I_{SC}$	Logic high short circuit current	V_{SPI} = 1.8 V		9		mA
$–I_{SC}$	Logic low short circuit current	V_{SPI} = 1.8 V		–14		mA

(3) Specification applies to the electrical level diagram of Figure 28
(4) Specification applies to the electrical circuit diagram of Figure 29
(5) The SPI_CFG register must be changed to a supported output logic level after power up and before a SPI read command is executed. Until that time, the output voltage on SDO/OVR may be as high as the VA3.0 supply during a SPI read command. The SDO/OVR output is high-Z at all times except during a read command.

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6.8 Timing Requirements

typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, VA3.0 = 3 V; VA1.8 = 1.8 V; VA1.2 = VACLK1.2 = 1.2 V; –1 dBFS differential input, and $R_{(term)}$ = 100 Ω (unless otherwise noted) (see Figure 1 and Figure 2 for timing diagrams)

PARAMETER		NOTES	MIN	NOM	MAX	UNIT
ADC SAMPLING INSTANT TIMING CHARACTERISTICS						
F_S	Sampling rate	Equal to F_{CLKIN} / CLKDIV	100		500	MSPS
F_{CLKIN}	Input clock frequency at CLKIN inputs	CLKDIV = 1	100		500	MHz
		CLKDIV = 2	200		1000	
		CLKDIV = 4	400		2000	
DC	Input clock (CLKIN) duty cycle	CLKDIV = 1		50% ± 20%		
		CLKDIV = 2 or CLKDIV = 4		50% ± 5%		
$t_{LAT-ADC}$	ADC core latency	Delay from a reference sampling instant to the boundary of the internal LMFC where the reference sample is the first sample of the next transmitted multi-frame. In this device, the frame clock period is equal to the sampling clock period.		7		Frame clock cycles
t_J	Additive sampling aperture jitter	Depends on input CLKIN differential edge rate at the zero crossing, dV_{SS}/dt, tested with 5 V/ns edge rate.				fs
		CLKDIV = 1		80		
		CLKDIV = 2, 4		90		
OVER-RANGE INTERFACE TIMING CHARACTERISTICS (SDO/OVR(1))						
t_{ODH}	OVR assertion delay	Functional delay between an overrange value sampled and OVR asserted		8		Frame clock cycles
t_{ODL}	OVR de-assertion delay	Functional delay between first underrange value sampled until OVR de-assertion, configurable via SPI				Frame clock cycles
		Configured for minimum delay		t_{ODH}		
		Configured for maximum delay		t_{ODH} + 15		
SYSREF TIMING CHARACTERISTICS						
t_{PH-SYS}	SYSREF assertion duration	Required duration of SYSREF assertion after rising edge event	2			Frame clock cycles
t_{PL-SYS}	SYSREF de-assertion duration	Required duration of SYSREF de-assertion after falling edge event	2			Frame clock cycles
t_{S-SYS}	SYSREF setup time	Relative to CLKIN rising edge			350	ps
t_{H-SYS}	SYSREF hold time	Relative to CLKIN rising edge			0	ps
JESD204B INTERFACE LINK TIMING CHARACTERISTICS						
t_{D-LMFC}	SYSREF to LMFC delay	Functional delay between SYSREF assertion latched and LMFC frame boundary. Depends on CLKDIV setting				
		CLKDIV = 1		4		CLKIN cycles
				4		Frame clock cycles
		CLKDIV = 2		10		CLKIN cycles
				5		Frame clock cycles
		CLKDIV = 4		18		CLKIN cycles
				4.5		Frame clock cycles

(1) The SDO/OVR pin is configured in over-range output mode.

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Timing Requirements (continued)

typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, VA3.0 = 3 V; VA1.8 = 1.8 V; VA1.2 = VACLK1.2 = 1.2 V; –1 dBFS differential input, and $R_{(term)}$ = 100 Ω (unless otherwise noted) (see Figure 1 and Figure 2 for timing diagrams)

PARAMETER		NOTES	MIN	NOM	MAX	UNIT
$t_{D\text{-}K28}$	LMFC to K28.5 delay	Functional delay between the start of the first K28.5 frame during code group synchronization at the serial output and the preceding LMFC frame boundary	5.6	6.6	7.6	Frame clock cycles
$t_{D\text{-}ILA}$	LMFC to ILA delay	Functional delay between the start of the first ILA frame during initial lane synchronization at the serial output and the preceding LMFC frame boundary	5.6	6.6	7.6	
$t_{D\text{-}DATA}$	LMFC to valid data delay	Functional delay between the start of the first valid data frame at the serial output and the preceding LMFC frame boundary	5.6	6.6	7.6	
$t_{S\text{-}SYNCb\text{-}F}$	SYNCb setup time	Required SYNCb setup time-relative to the internal LMFC boundary(2)		3		Frame clock cycles
$t_{H\text{-}SYNCb\text{-}F}$	SYNCb hold time	Required SYNCb hold time relative to the internal LMFC boundary(2)		0		
$t_{H\text{-}SYNCb}$	SYNCb assertion hold time	Required SYNCb hold time after assertion before de-assertion to initiate a link resynchronization		4		
t_{ILA}	ILA duration	Duration of the ILA sequence		4		Multi-frame clock cycles
SERIAL OUTPUT DATA TIMING CHARACTERISTICS						
F_{SR}	Serial bit rate		1		5.0	Gb/s
UI	Unit interval	5.0 Gb/s data rate		200		ps
t_R, t_F	Rise/fall times	5.0 Gb/s data rate, default values for VOD and DEM		43		ps
DJ	Deterministic jitter	Includes periodic jitter (PJ), data dependent jitter (DDJ), duty cycle distortion (DCD), and inter-symbol interference (ISI); 5.0 Gb/s data rate		0.049		p-p UI
				9.82		p-p ps
RJ	Random jitter	Assumes BER of 1e-15 (Q = 15.88); 5.0 Gb/s data rate		0.119		p-p UI
				1.50		rms ps
TJ	Total jitter	Sum of DJ and RJ, assumes BER of 1e-15 (Q = 15.88); 5.0 Gb/s data rate		0.169		p-p UI
				33.6		p-p ps
SPI BUS TIMING CHARACTERISTICS(3)						
f_{SCLK}	Serial clock frequency	$f_{SCLK} = 1 / t_P$			20	MHz
t_{PH}	SCLK pulse width – high		6			ns
t_{PL}	SCLK pulse width – low		7			ns
t_{SSU}	SDI input data setup time		3			ns
t_{SH}	SDI input data hold time		1			ns
t_{ODZ}	SDO output data driven-to-3-state time				10	ns
t_{OZD}	SDO output data 3-state-to-driven time				25	ns
t_{OD}	SDO output data delay time				25	ns
t_{CSS}	CSB setup time		3			ns
t_{CSH}	CSB hold time		1			ns
t_{IAG}	Inter-access gap	Minimum time CSB must be de-asserted between accesses	1			ns

(2) The SYNCb setup and hold times determine the multi-frame after which the ILA is initiated but meeting the setup and hold times are not required to achieve deterministic latency.
(3) All timing specifications for the SPI given for V_{SPI} = 1.8-V logic levels and a 5-pF capacitive load on the SDO pin. Timing specification require larger margins for V_{SPI}= 1.2 V. The serial bit rate of the SPI should be limited to 10 Mb/s or lower for V_{SPI} = 1.2-V logic.

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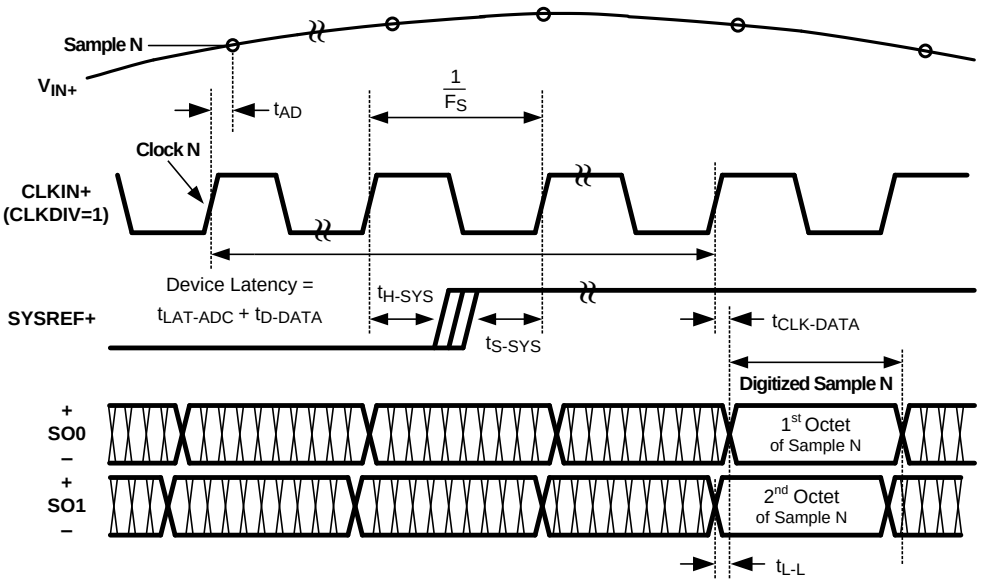

Figure 1. Sample Timing Diagram

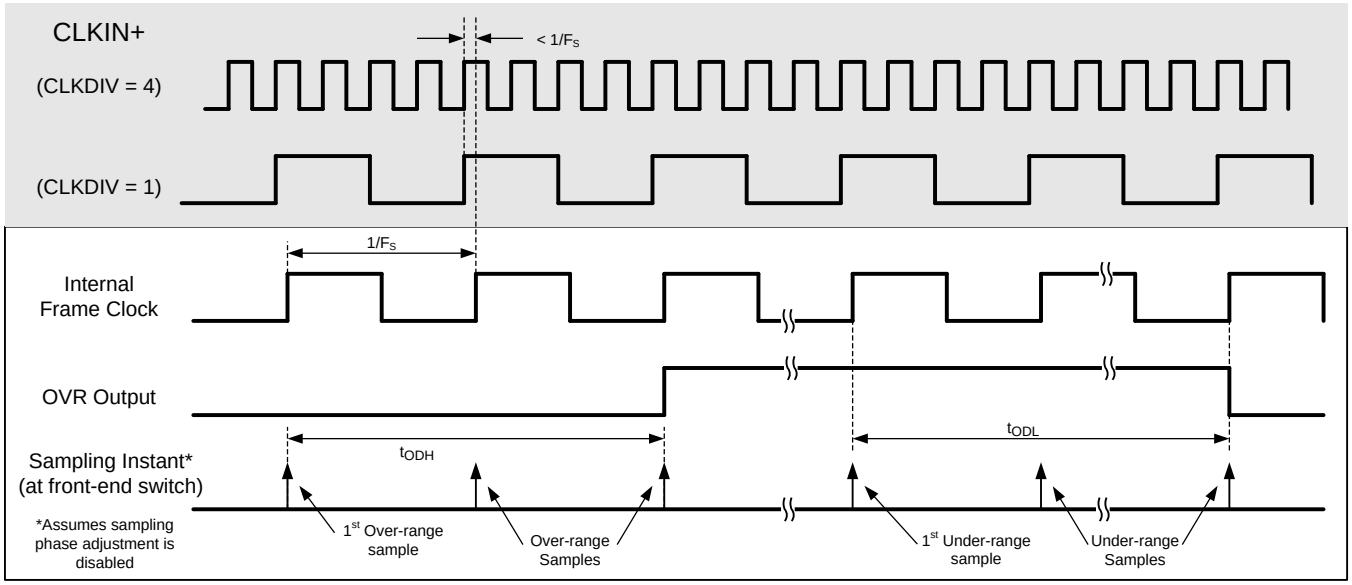

Figure 2. Overrange (OVR) Timing Diagram

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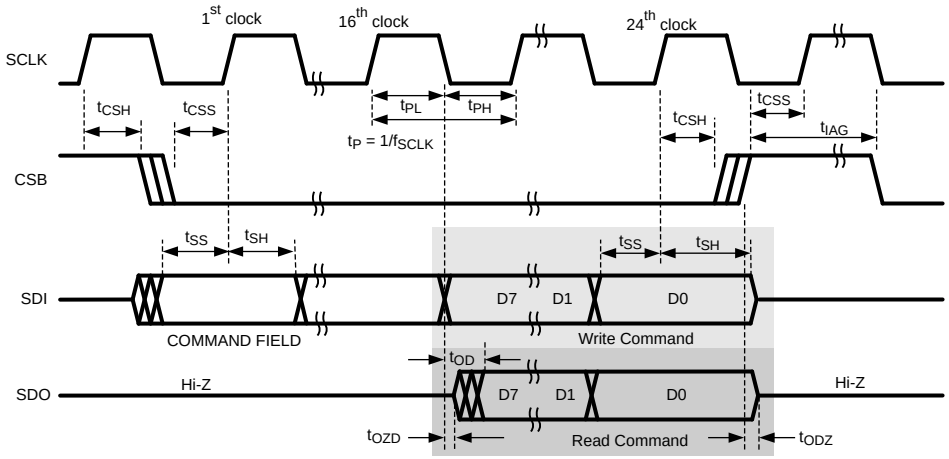

Figure 3. SPI Timing Diagram

6.9 Typical Characteristics

Typical values at T_A = 25 °C, full temperature range is T_{MIN} = –40 °C to T_{MAX} = 85 °C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, $V_{A3.0}$ = 3.0 V, $V_{A1.8}$ = 1.8 V, $V_{A1.2}$ = $V_{ACLK1.2}$ = 1.2 V, –1 dBFS differential input (unless otherwise noted).

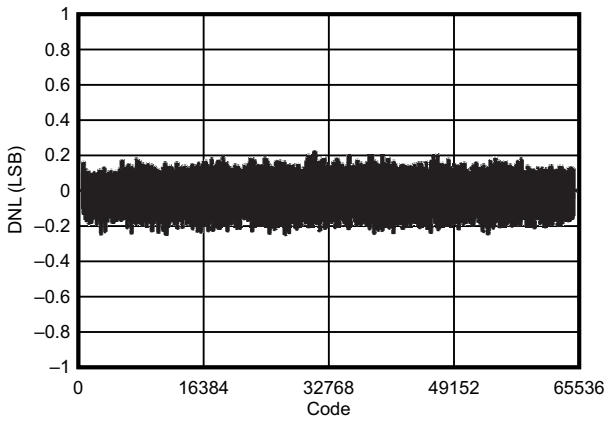

Figure 4. DNL vs Output Code

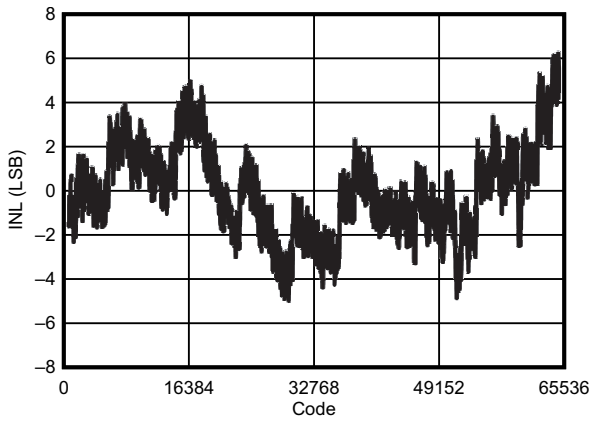

Figure 5. INL vs Output Code

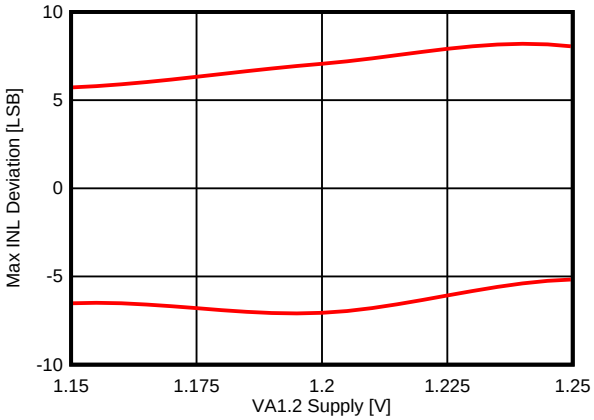

Figure 6. INL vs Supply

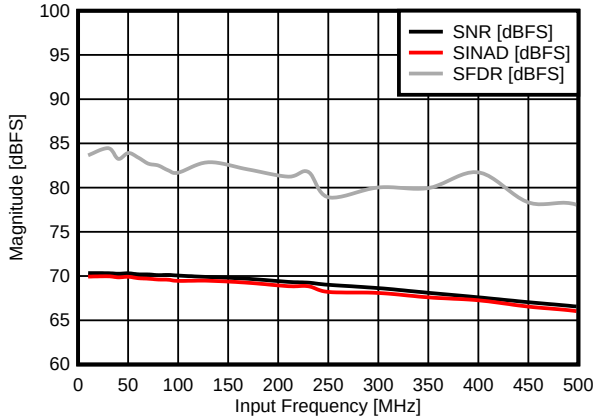

Figure 7. SNR, SINAD, SFDR vs Input Frequency

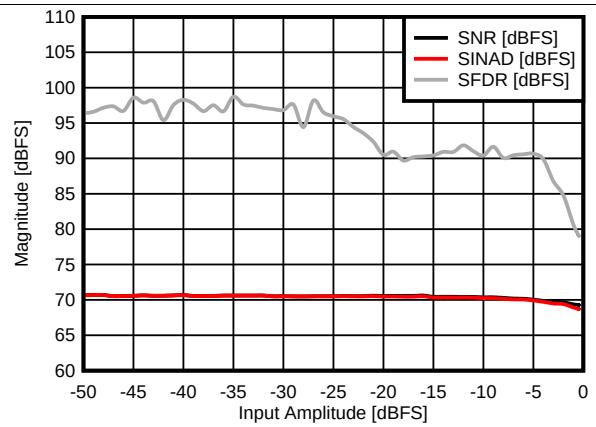

Figure 8. SNR, SINAD, SFDR vs Input Amplitude

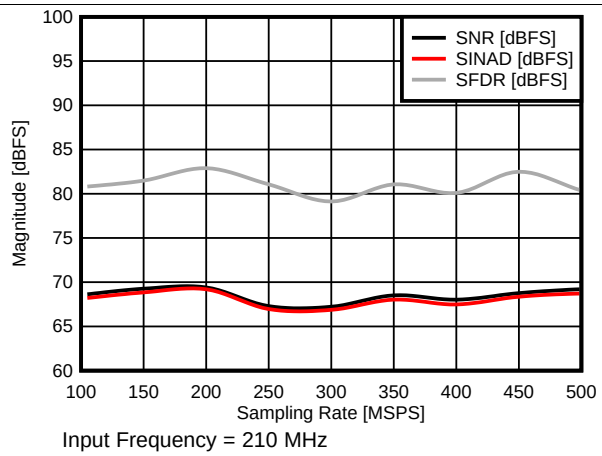

Figure 9. SNR, SINAD, SFDR vs Sampling Rate (F_S)

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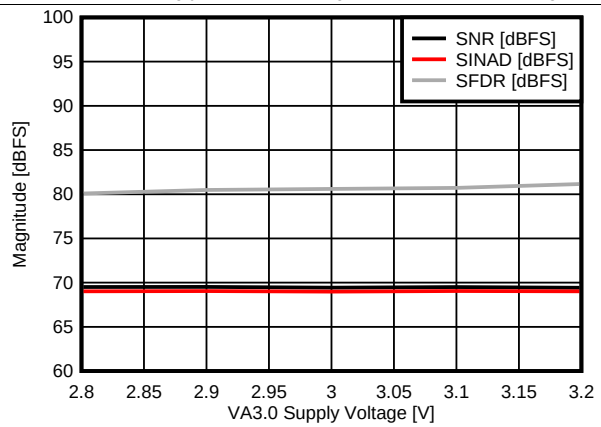
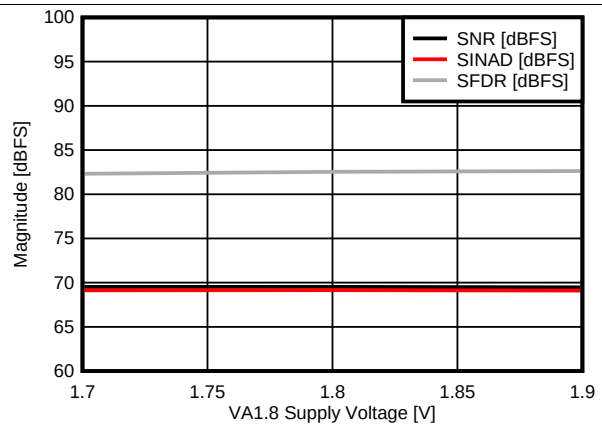
Typical Characteristics (continued)

Typical values at T_A = 25 °C, full temperature range is T_{MIN} = –40 °C to T_{MAX} = 85 °C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, $V_{A3.0}$ = 3.0 V, $V_{A1.8}$ = 1.8 V, $V_{A1.2}$ = $V_{ACLK1.2}$ = 1.2 V, –1 dBFS differential input (unless otherwise noted).



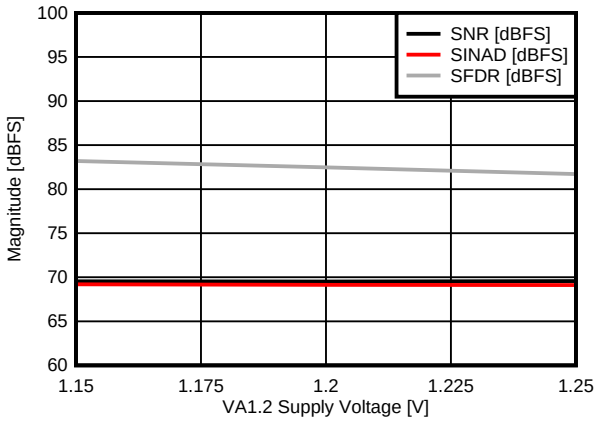
Input Frequency = 210 MHz

Figure 10. SNR, SINAD, SFDR vs VA3.0 Supply



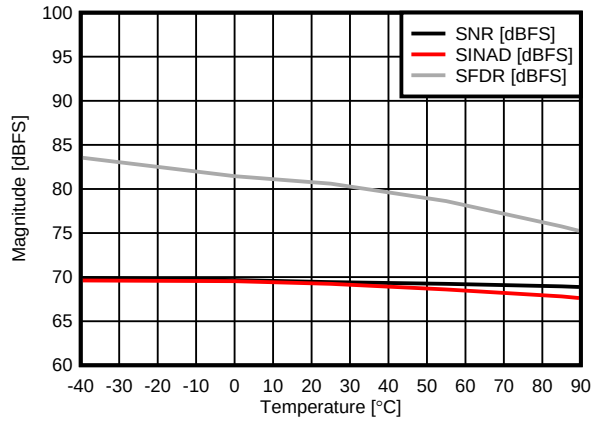
Input Frequency = 210 MHz

Figure 11. SNR, SINAD, SFDR vs VA1.8 Supply



Input Frequency = 210 MHz

Figure 12. SNR, SINAD, SFDR vs VA1.2 Supply



Input Frequency = 210 MHz

Figure 13. SNR, SINAD, SFDR vs Temperature

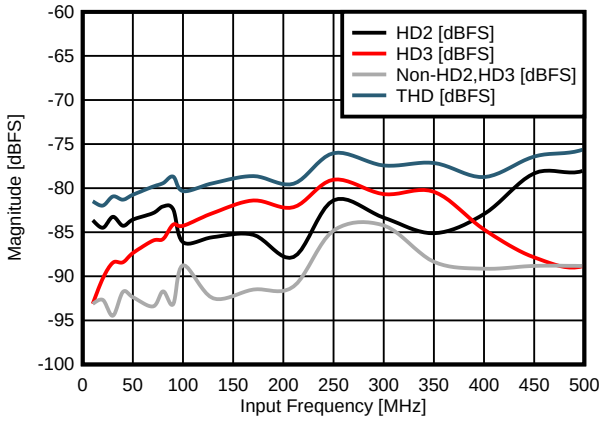
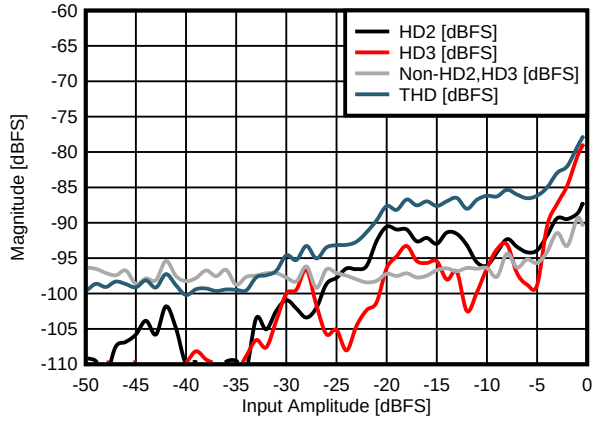


Figure 14. HD2, HD3, SPUR, THD vs Input Frequency

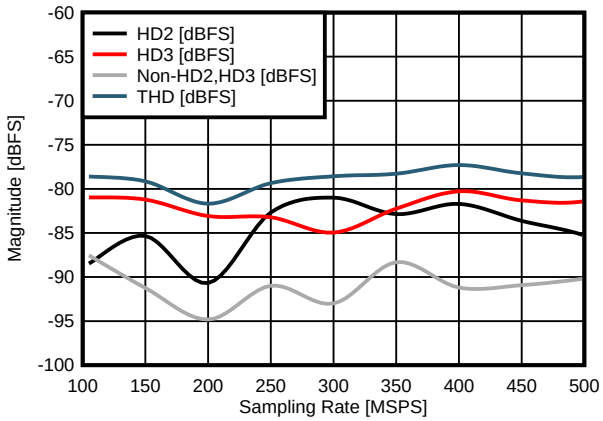


Input Frequency = 210 MHz

Figure 15. HD2, HD3, SPUR, THD vs Input Amplitude

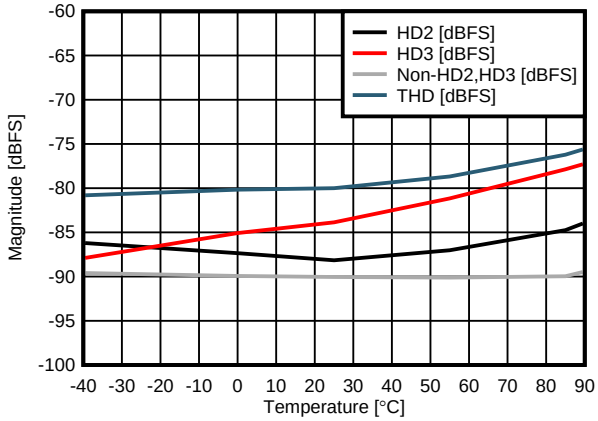
Typical Characteristics (continued)

Typical values at T_A = 25 °C, full temperature range is T_{MIN} = –40 °C to T_{MAX} = 85 °C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, $V_{A3.0}$ = 3.0 V, $V_{A1.8}$ = 1.8 V, $V_{A1.2}$ = $V_{ACLK1.2}$ = 1.2 V, –1 dBFS differential input (unless otherwise noted).



Input Frequency = 210 MHz

Figure 16. HD2, HD3, SPUR, THD vs Sampling Rate



Input Frequency = 210 MHz

Figure 17. HD2, HD3, SPUR, THD vs Temperature

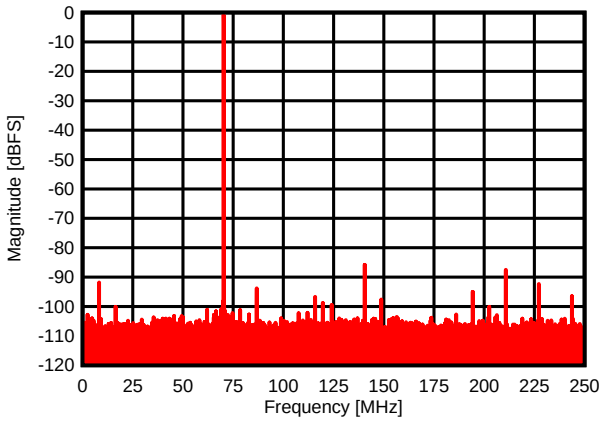


Figure 18. Output Spectrum, 1-Tone Test at 70 MHz

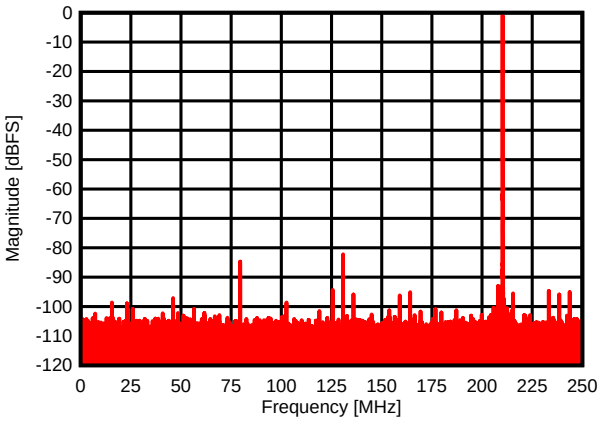


Figure 19. Output Spectrum, 1-Tone Test at 210 MHz

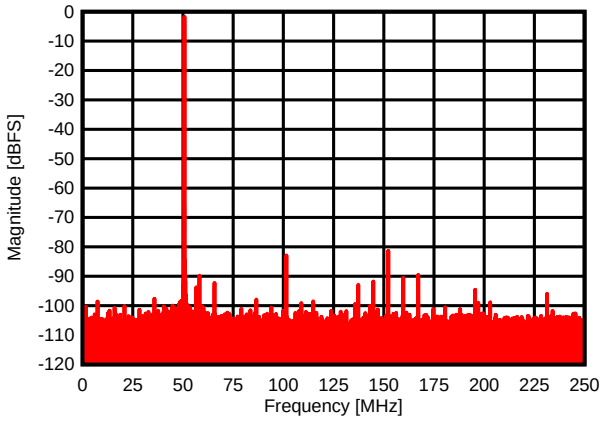
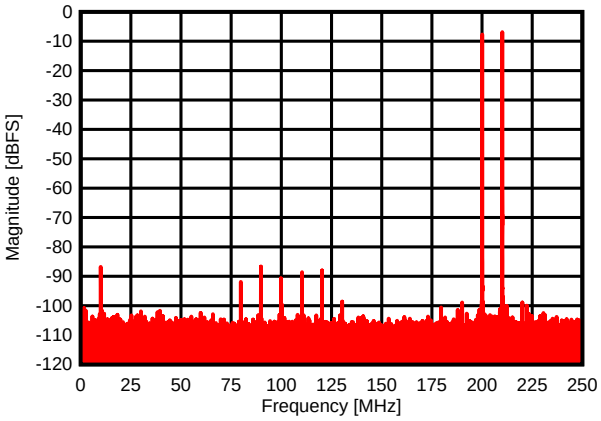


Figure 20. Output Spectrum, 1-Tone Test at 450 MHz



Input Amplitude = –7 dBFS/Tone

Figure 21. Output Spectrum, 2-Tone Test at 200 MHz and 210 MHz

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Typical Characteristics (continued)

Typical values at T_A = 25 °C, full temperature range is T_{MIN} = –40 °C to T_{MAX} = 85 °C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, $V_{A3.0}$ = 3.0 V, $V_{A1.8}$ = 1.8 V, $V_{A1.2}$ = $V_{ACLK1.2}$ = 1.2 V, –1 dBFS differential input (unless otherwise noted).

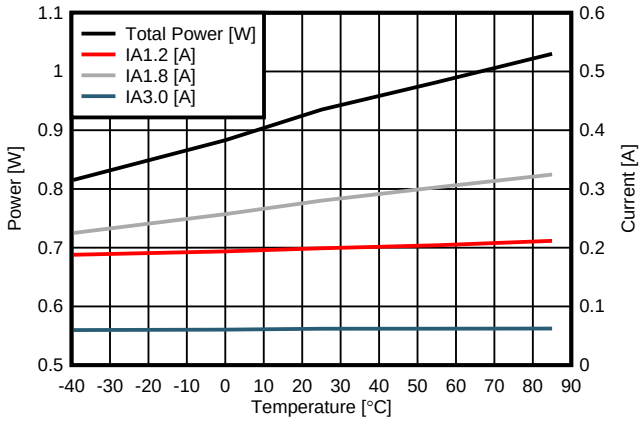


Figure 22. Supply Power and Current vs Temperature

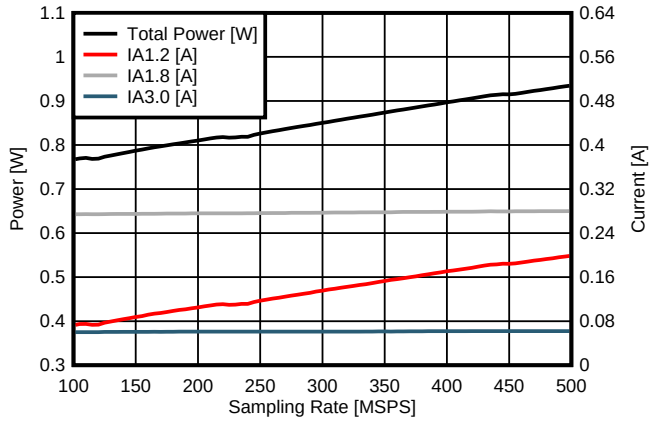
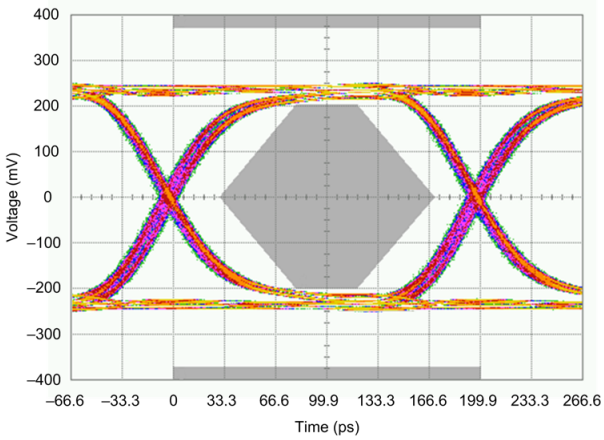
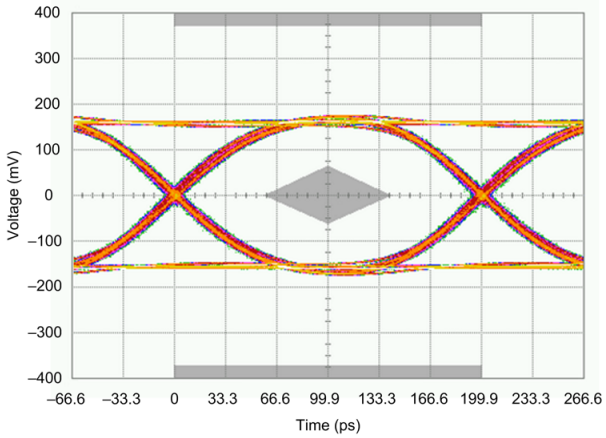


Figure 23. Supply Power and Current vs Sampling Rate



5-mil. FR4 Microstrip Trace at 5 Gb/s with No De-Emphasis

Figure 24. Transmitted Eye at Output of 3-Inch



5-mil. FR4 Microstrip Trace at 5 Gb/s with Optimized De-Emphasis

Figure 25. Transmitted Eye at Output of 18-Inch

7 Parameter Measurement Information

7.1 Interface Circuits

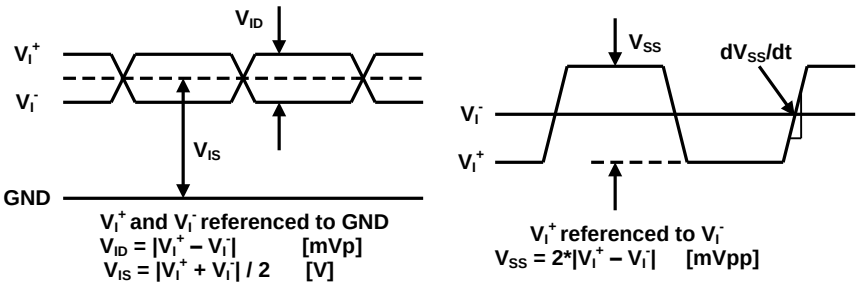


Figure 26. Electrical Level Diagram for Differential Input Signals

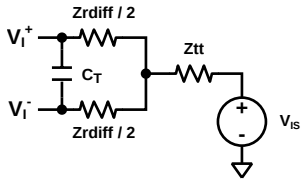


Figure 27. Simplified Electrical Circuit Diagram for Differential Input Signals

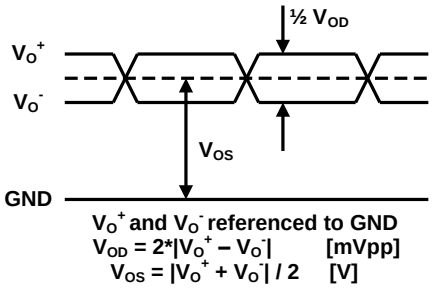


Figure 28. Electrical Level Diagram for Differential Output Signals

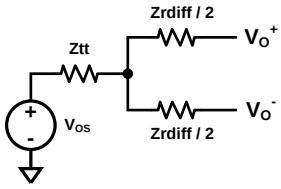


Figure 29. Electrical Circuit Diagram for Differential Output Signals

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8 Detailed Description

8.1 Overview

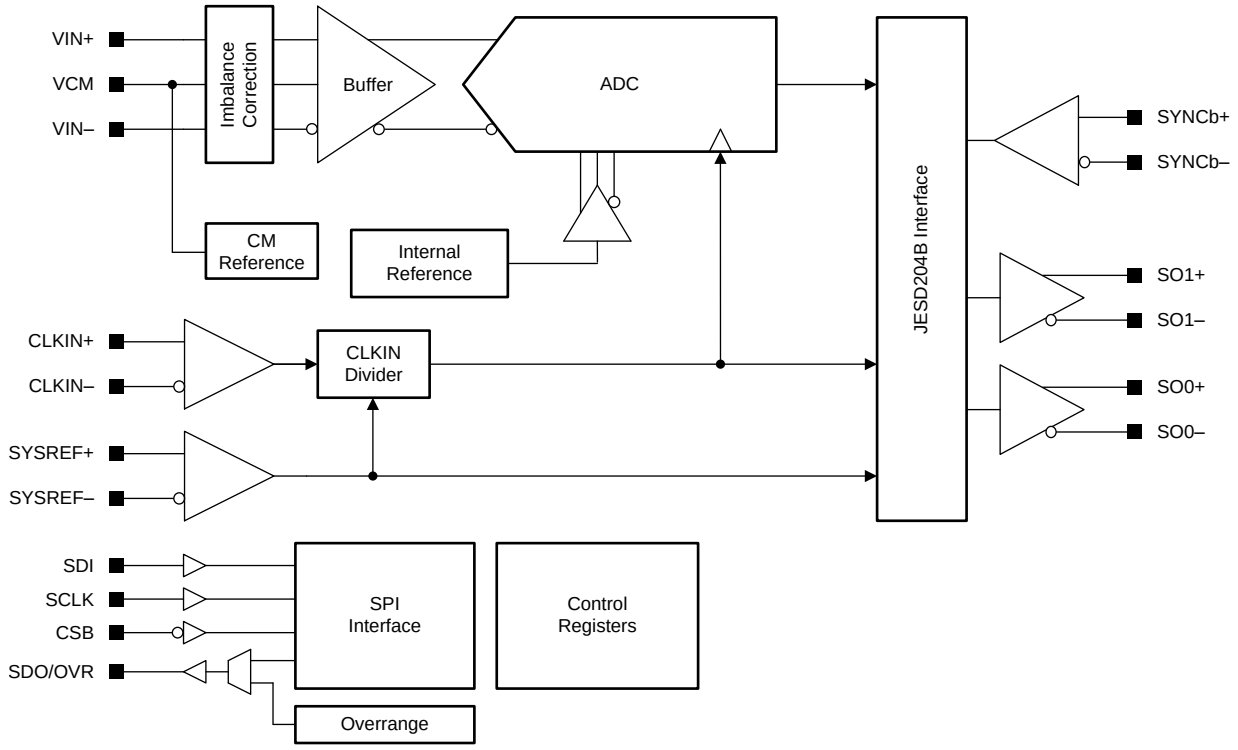
The ADC31JB68 is a low-power, wide-bandwidth, 16-bit, 500-MSPS analog-to-digital converter (ADC). The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. This device is designed for sampling analog input signals of up to 1300 MHz.

The ADC31JB68 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with very low power consumption. On-chip dither provides an exceptionally clean noise floor. Embedded foreground and background calibration ensures consistent dynamic performance over the entire temperature range and minimizes part-to-part variation.

The device outputs its digital data from a JESD204B serial interface with two lanes transferring data at up to 5 Gbps/lane. The interface significantly reduces the number of lanes compared to an LVDS interface, allowing high system integration density. An internal phase locked loop (PLL) transparently generates the necessary clocking for data serialization.

The ADC31JB68 is offered in a 40- pin QFN (6 x 6mm) package and supports the full industrial temperature range.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Inputs and Input Buffer

The ADC31JB68 analog signal inputs are designed to be driven differentially. The analog input pins have an internal analog buffer that drives the sampling circuit. As a result of the analog buffer and internal 200 Ω termination, the input pins present a time-constant impedance load to the external driving source which enables great flexibility in the external analog filter design or direct impedance match to the driver. The buffer also helps to isolate the external driving circuit from the internal switching charge transients of the sampling circuit which results in a more consistent SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to 1.6-V via the internal termination resistors which allows for AC coupling of the input drive network. Each input pin (VIN+, VIN–) must swing symmetrically between (V_{CM} + 0.425 V) and (V_{CM} – 0.425 V), resulting in a 1.7 V_{PP} (default) differential input swing.

8.3.2 Amplitude and Phase Imbalance Correction

The ADC performance can be sensitive to amplitude and phase imbalance of the input differential signal. A front-end balance correction circuit is integrated to optimize the second-order distortion (HD2) performance of the ADC in the presence of an imbalanced input signal. 4-bit control of the phase mismatch and 3-bit control of the amplitude mismatch corrects the input mismatch before the input buffer. A simplified diagram of the amplitude and phase correction circuit at the ADC input is shown in Figure 30.

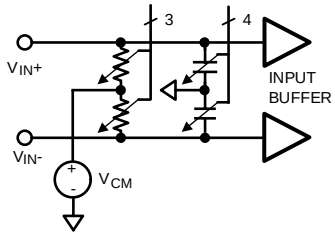


Figure 30. Simplified Input Differential Balance Correction Circuit

Amplitude correction is achieved by varying the single-ended termination resistance of each input while maintaining constant total differential resistance, thereby adjusting the amplitude at each input but leaving the differential swing constant. Phase correction, also considered capacitive balance correction, varies the capacitive load at the ADC input, thereby counter-acting the phase difference between the analog inputs while minimally affecting amplitude. This function is useful for correcting the balance of transformers or filters that drive the ADC analog inputs. Figure 31 shows the measured HD2 resulting from an example 300-MHz imbalanced input signal measured over the available amplitude and phase correction settings. Performance parameters in the Converter Performance Characteristics are characterized with the amplitude and phase correction settings in the default condition (no correction).

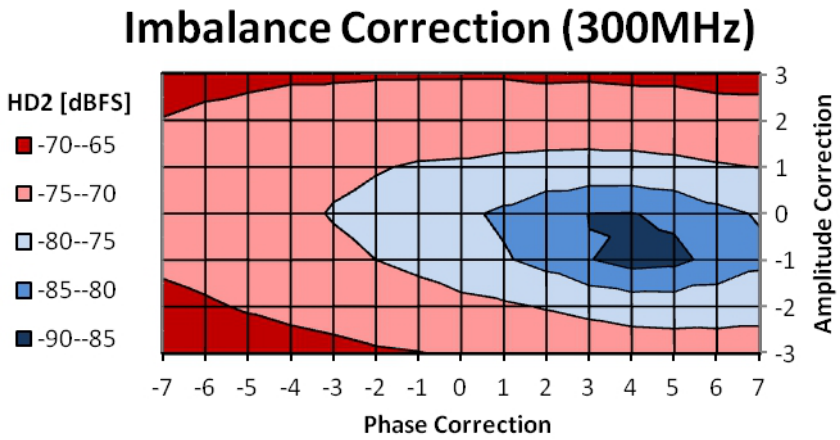


Figure 31. HD2 Optimization at 300 MHz Using Gain and Phase Imbalance Correction

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Feature Description (continued)

8.3.3 Over-Range Detection

Over-range detection is available via the shared SDO/OVR dual-mode pin. Configuration of the SDO/OVR pin into the over-range mode is done through the SPI. By default, the over-range mode is not selected. The SDO/OVR pin asserts (logical high) when an over-range signal is detected at the input. The short delay from when an over-range signal is incident at the input until the SDO/OVR output is asserted allows for almost immediate detection of over-range signals without delay from the internal ADC pipeline latency or serial link latency.

The input power threshold to indicate an over-range event is programmable via the SPI in steps of 128 codes relative to the 16-bit code range of the data at the output of the ADC core.

After an over-range event occurs and the signal at the channel input reduces to a level below full-scale, an internal counter begins counting to provide a hold function. When the counter reaches the hold counter threshold, the over-range signal is de-asserted (logical low). The duration of the hold counter is programmable via the SPI to hold for +3, +7, or +15 frame clock cycles. The counter is disabled (+0 cycles) by default to allow de-assertion without holding.

8.3.4 Input Clock Divider

An input clock divider allows a high frequency clock signal to be distributed throughout the system and locally divided down at the ADC device. The frequency at the CLKIN input may be divided down to the sampling rate of the ADC by factors of 1, 2, or 4. Changing the clock divider setting initiates a JESD204 link re-initialization and requires re-calibration of the ADC if the sampling rate is changed from the rate during the previous calibration (see *ADC Core Calibration*).

8.3.5 SYSREF Detection Gate

When the signal at the SYSREF input is not actively toggling periodically, the SYSREF signal is considered to be in an idle state. The idle state is recommended at any time the ADC31JB68 spurious performance must be maximized. The SYSREF detection gate is provided to prevent transitions of the SYSREF signal in and out of the idle state from impacting the JESD204B core. While the SYSREF signal is In the idle state, the SYSREF detection gate should be used reject noise that may appear on the SYSREF signal.

The detection gate is the AND gate shown in Figure 72. The gate enables or disables propagation of the SYSREF signal through to the internal device logic. If the detection gate is disabled and a false edge appears at the SYSREF input, the signal does not disrupt the internal clock alignment. Note that the SYSREF detection gate is disabled by default; therefore, the device does not respond to a SYSREF edge until the detection gate is enabled.

The SYSREF detection gate features is controlled through the SPI.

8.3.6 Serial Differential Output Drivers

The differential drivers that output the serial JESD204B data are voltage mode drivers with amplitude control and de-emphasis features that may be configured through the SPI for a variety of different channel applications. Eight amplitude control (VOD) and eight de-emphasis control (DEM) settings are available. Both VOD and DEM register fields must be configured to optimize the noise performance of the serial link for a particular lossy channel.

8.3.6.1 De-Emphasis Equalization

De-emphasis of the differential output is provided as a form of continuous-time linear equalization that imposes a high-pass frequency response onto the output signal to compensate for frequency-dependent attenuation as the signal propagates through the channel to the receiver. In the time-domain, the de-emphasis appears as the bit transition transient followed by an immediate reduction in the differential amplitude, as shown in Figure 32. The characteristic appearance of the waveform changes with differential amplitude and the magnitude of de-emphasis applied. The serial lane rate determines the available period of time during which the de-emphasis transient settles. However, the lane rate does not affect the settling behavior of the applied de-emphasis. The de-emphasis value is measured as the ratio (in units of [dB]) between the peak voltage after the signal transition to the settled voltage value in one bit period. The data rate for this measurement is 1 Gb/s to allow settling of the de-emphasis transient.

Feature Description (continued)

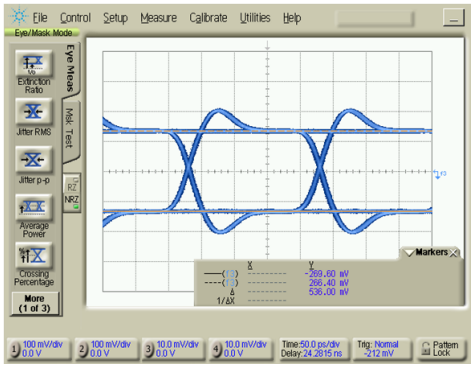

Figure 32. De-emphasis of the Differential Output Signal

8.3.6.2 Serial Lane Inversion

The polarity of the individual serial data lanes can be controlled with the serial lane inversion enable function via the SER_INV register. These controls simplify PCB routing of the serial lanes by allowing the transmitter to be connected to the receiver with either polarity.

8.3.7 ADC Core Calibration

The ADC core of this device requires foreground calibration to be performed after power-up to achieve full performance. Immediately after power-up, the ADC31JB68 device detects that the supplies and clock are valid, waits for a power-up delay, and then performs a foreground calibration of the ADC core automatically. The power-up delay is 9×10^6 sampling clock cycles or 18 ms at a 500-MSPS sampling rate. The calibration requires approximately 1.0×10^6 sampling clock cycles.

If the system requires that the ADC31JB68 input clock divider value (CLKDIV) is set to 2 or 4, then ADC calibration should be performed manually after CLKDIV has been set to the desired value. Manually calibrating the ADC core is performed by changing to power down mode, returning to normal operation, and monitoring the CAL_DONE bit in the JESD_STATUS register until calibration is complete. As an alternative to monitoring CAL_DONE, the system may wait 1.5×10^6 sampling clock cycles until calibration completes.

When the ADC core enters normal conversion, background calibration monitors the performance of the device and automatically adjusts the core to optimally correct for changes in the operating conditions such as supply and temperature. The background calibration settling time is less than 375×10^6 sampling clock cycles.

8.3.8 Data Format

Data may be output in the serial stream as 2's complement format (default) or as offset binary. This selection is chosen via the SPI. The formatting is performed in the data path prior to JESD204B data framing and 8b/10b encoding.

8.3.9 JESD204B Supported Features

The ADC31JB68 device supports a specific feature set of the JESD204B standard targeted to its intended applications but does not implement all the flexibility of the standard. Table 1 summarizes the level of feature support.

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Feature Description (continued)

Table 1. ADC31JB68 Feature Support for the JESD204B Serial Interface

Feature	Supported	Not Supported
Subclass	• Subclass 1	• Subclass 0, 2
Device Clock (CLKIN) and SYSREF	• AC coupled CLKIN • DC coupled CLKIN and SYSREF • Periodic, Pulsed Periodic and One-Shot SYSREF	• AC coupled SYSREF
Latency	• Deterministic latency supported for subclass 1 implementations using standard SYSREF signal	• Deterministic latency not supported for non-standard implementations
Electrical layer features	• LV-OIF-11G-SR interface and performance • AC coupled serial lanes • TX lane polarity inversion	• DC coupled serial lanes
Transport layer features and configuration	• L = 2 lanes • K configuration • Scrambling	• F, S, L, and HD configuration is not independently configurable • M, N, N', CS, CF configuration is not independently configurable • Idle link mode • Short and Long transport layer test patterns
Data link layer features	• 8b/10b encoding • Lane synchronization • D21.5, K28.5, ILA, PRBS7, PRBS15, PRBS23, Ramp test sequences	• RPAT/JSPAT test sequences

8.3.10 JESD204B Interface

The JESD204B transmitter block consists of the transport layer, the data scrambler and the link layer. The transport layer maps the ADC output data into the selected JESD204B frame data format and manages the transmission of ADC output data or test patterns. The link layer performs the 8b/10b data encoding as well as the synchronization and initial lane alignment using the SYNCb input signal. Data from the transport layer can be optionally scrambled.

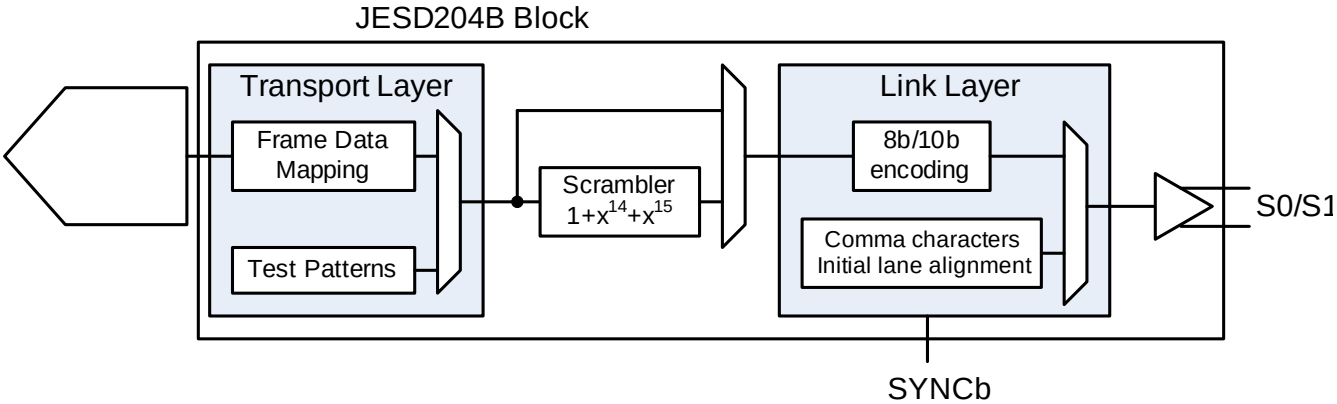

Figure 33. JESD204B Transmitter Block

8.3.11 Transport Layer Configuration

The transport layer features supported by the ADC31JB68 device are a subset of possible features described in the JESD204B standard. The configuration options are intentionally simplified to provide the lowest power and most easy-to-use solution.

8.3.11.1 Lane Configuration

The digital data is output on two serial lanes that support JESD204B. The number of transmission lanes per channel (L) is only 2. The serial data rate is 10 times the sampling rate. A 500 MSPS sampling rate corresponds to a 5.0 Gb/s per lane rate.

8.3.11.2 Frame Format

The lanes per device (L), octets per frame (F), samples per frame (S), and high-density mode (HD) parameters are not independently configurable. The N, N', CS, CF, M, and HD parameters are fixed and not configurable. Table 2 lists the available JESD204B formats and valid ranges for the ADC31JB68. The ranges are limited by the Serdes line rate and the maximum ADC sample frequency. Figure 34 shows the data format.

Table 2. Available JESD204B Formats and Valid Ranges

L	M	F	S	MAX ADC SAMPLING RATE (Msps)	MAX f_{SERDES} (Gbps)
2	1	1	1	500	5.0

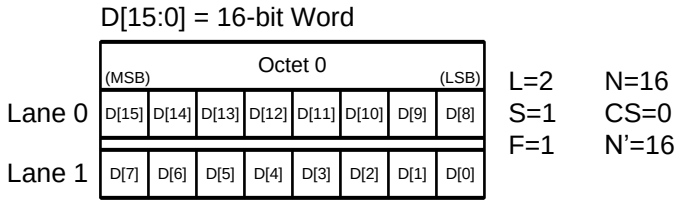

Figure 34. Transport Layer Definitions for the Supported-Lane Configurations

8.3.11.3 ILA Information

Table 3 summarizes the information transmitted during the initial lane alignment (ILA) sequence. Mapping of these parameters into the data stream is described in the JESD204B standard.

Table 3. Configuration of the JESD204B Serial-Data Receiver

Parameter	Description	Logical Value	Encoded Value
ADJCNT	DAC LMFC adjustment	0	0
ADJDIR	DAC LMFC adjustment direction	0	0
BID	Bank ID	0	0
CF	Number of control words per frame clock period per link	0	0
CS	Number of control bits per sample	0	0
DID	Device identification number	0	0
F	Number of octets per frame (per lane)(1)	1	0
HD	High-density format	1	1
JESDV	JESD204 version	1	1
K	Number of frames per multi-frame(1)	Set by register as 17 to 32	16 to 31
L	Number of lanes per link(1)	2	1
LID	Lane identification number	0 (lane 0), 1 (lane 1)	0 or 1
M	Number of converters per device(1)	1	0
N	Converter resolution (1)	16	15
N'	Total number of bits per sample(1)	16	15
PHADJ	Phase adjustment request to DAC	0	0
S	Number of samples per converter per frame cycle(1)	1	0
SCR	Scrambling enabled	Set by register as 0 (disabled) or 1	0 or 1
SUBCLASSV	Device subclass version	1	1
RES1	Reserved field 1	0	0
RES2	Reserved field 2	0	0
FCHK	Checksum(2)	Computed	Computed

(1) These parameters have a binary-value-minus-1 encoding applied before being mapped into the link configuration octets. For example, F = 1 is encoded as 0.
(2) Example: For K=32, lane 0, scrambler disabled, the FCHK value in the ILA will be 0x41 (hex) or 65 (decimal)

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Scrambling of the output serial data is supported and conforms to the JESD204B standard. Scrambling is disabled by default, but may be enabled via the SPI. When scrambling is enabled, the ADC31JB68 device supports the early synchronization option by the receiver during the ILA sequence, although the ILA sequence data is never scrambled.

8.3.12 Test Pattern Sequences

The SPI may enable the following test pattern sequences. Short- and long-transport layer, RPAT, and JSPAT sequences are not supported.

Table 4. Supported Test Pattern Sequences

Test Pattern	Description	Common Purpose
D21.5	Data is transmitted across a normal link but ADC sampled data is replaced with D21.5 symbols, resulting in an alternating 1 and 0 pattern (101010...) on each serial lane. After enabling this pattern, the JESD204B link must be re-initialized.	Jitter or system debug
K28.5	Continuous K28.5 symbols are output on each serial lane. Link initialization is not possible nor required.	System debug
Repeated ILA	ILA repeats indefinitely on each serial lane. After enabling this pattern, the JESD204B link must be reinitialized.	System debug
Ramp	Data is transmitted across a normal link but ADC sampled data is replaced with a ramp pattern. The ramp ascends through a 16-bit range and the step is programmable. After enabling this pattern, the JESD204B link must be reinitialized.	System debug and transport layer verification
PRBS	Standard pseudo-random bit sequences are output on each serial lane. PRBS 7/15/23 Complies with ITU-T O.150 specification and is compatible with J-BERT equipment. Link initialization is not possible nor required.	Jitter and bit error rate testing

8.3.13 JESD204B Link Initialization

A JESD204B link is established via link initialization, which involves the following steps: frame alignment, code group synchronization, and initial lane synchronization. These steps are shown in Figure 35. Link initialization must occur between the transmitting device (ADC) and receiving device before sampled data may be transmitted over the link. The link initialization steps described here are specifically for the ADC31JB68 device, supporting JESD204B subclass 1.

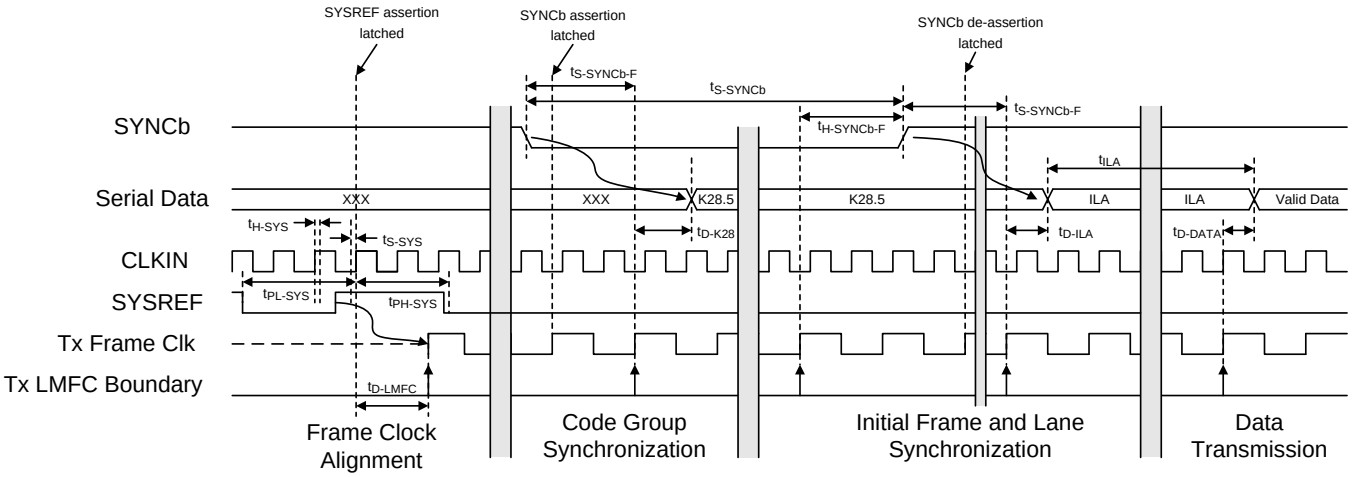

Figure 35. Link-initialization Timing and Flow Diagram

8.3.13.1 Frame Alignment

The Frame Alignment step requires alignment of the frame and local multi-frame clocks within the ADC31JB68 device to an external reference. This is accomplished by providing the device clock and SYSREF clock to the CLKIN and SYSREF inputs, respectively. The ADC31JB68 device aligns its frame clock and LMFC to any SYSREF rising edge event, offset by a SYSREF-to-LMFC propagation delay.

The SYSREF signal must be source synchronous to the device clock; therefore, the SYSREF rising edge must meet setup and hold requirements relative to the signal at the CLKIN input. If these requirements cannot be met, then the alignment of the internal frame and multi-frame clocks cannot be specified. As a result, a link may still be established, but the latency through the link cannot be deterministic. Frame alignment may occur at any time but a re-alignment of the internal frame clock and LMFC will break the link. Note that frame alignment is not required for the ADC31JB68 device to establish a link because the device automatically generates the clocks on power-up with unknown phase alignment.

8.3.13.2 Code Group Synchronization

Code Group Synchronization is initiated when the receiver sends a synchronization request by asserting the SYNCb input of the ADC31JB68 device to a logic low state (SYNCb+ < SYNCb–). After the SYNCb assertion is detected, the ADC31JB68 device outputs K28.5 symbols on all serial lanes. These symbols are used by the receiver to synchronize and time align its clock and data recovery (CDR) block to the known symbols. The SYNCb signal must be asserted for at least 4 frame clock cycles otherwise the event is ignored by the ADC31JB68 device. Code group synchronization is completed when the receiver de-asserts the SYNCb signal to a logic high state.

After the ADC31JB68 detects a de-assertion of its SYNCb input, the *Initial Lane Synchronization* step begins on the following LMFC boundary. The ADC31JB68 device outputs 4 multi-frames of information that compose the ILA sequence. This sequence contains information about the data transmitted on the link. The initial lane synchronization step and link initialization conclude when the ILA is finished and immediately transitions into *Data Transmission*. During data transmission, valid sampled data is transmitted across the link until the link is broken.

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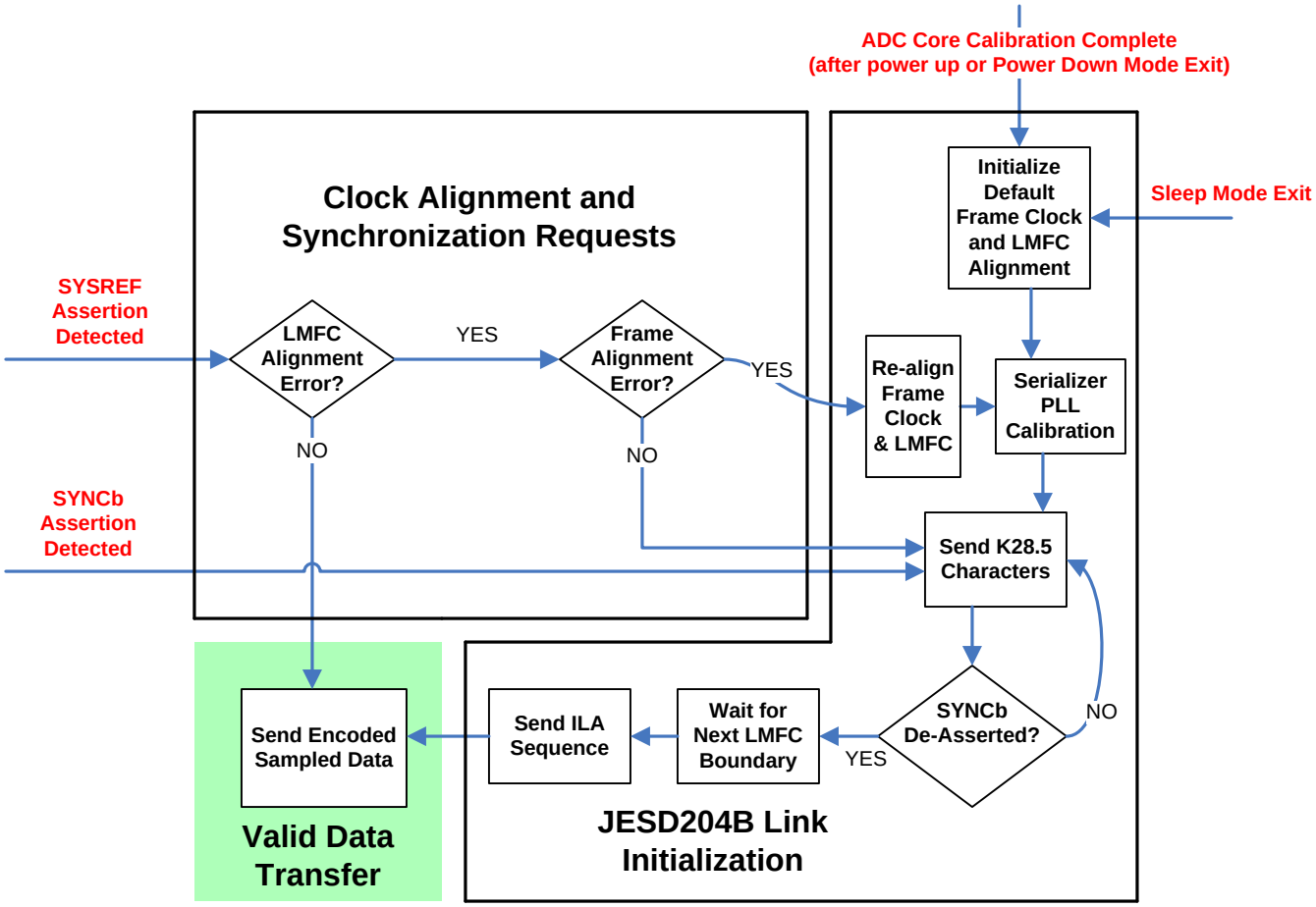

Figure 36. Device Start-Up and JESD204B Link Synchronization Flow Chart

The flowchart in Figure 36 describes how the ADC31JB68 device initializes the JESD204B link and reacts to changes in the link. After the ADC core calibration is finished, the ADC31JB68 device begins with PLL calibration and link initialization using a default frame clock and LMFC alignment by sending K28.5 characters. PLL calibration requires approximately 153×10^3 sampling clock cycles. If SYNCb is not asserted, then the device immediately advances to the ILA sequence at the next LMFC boundary. If SYNCb is asserted, then the device continues to output K28.5 characters until SYNCb is de-asserted.

When a SYSREF rising edge event is detected, then the ADC31JB68 device compares the SYSREF event to the current alignment of the LMFC. If the SYSREF event is aligned to the current LMFC alignment, then no action is taken and the device continues to output data. If misalignment is detected, then the SYSREF event is compared to the frame clock. If misalignment of the frame clock is also detected, then the clocks are re-aligned and the link is reinitialized. If the frame clock is not misaligned, then the frame clock alignment is not updated. In the cases that a SYSREF event causes a link re-initialization, the ADC31JB68 device begins sending K28.5 characters without a SYNCb assertion and immediately transitions to the ILA sequence on the next LMFC boundary unless the SYNCb signal is asserted. Anytime the frame clock and LMFC are re-aligned, the serializer PLL must calibrate before code group synchronization begins. SYSREF events must not occur during ADC31JB68 device power-up, ADC calibration, or PLL calibration. The JESD_STATUS register is available to check the status of the ADC31JB68 device and the JESD204B link.

If a SYNCb assertion is detected for at least 4 frame clock cycles, the ADC31JB68 device immediately breaks the link and sends K28.5 characters until the SYNCb signal is de-asserted.

When exiting sleep mode, the frame clock and LMFC are started with a default (unknown) phase alignment, PLL calibration is performed, and the device immediately transitions into sending K28.5 characters.

8.3.14 SPI

The SPI allows access to the internal configuration registers of the ADC through read and write commands to a specific address. The interface protocol has a 1-bit command, 15-bit address word and 8-bit data word as shown in Figure 37. A read or write command is 24 bits in total, starting with the read or write command bit where 0 indicates a write command and 1 indicates a read command. The read or write command bit is clocked into the device on the first rising edge of SCLK after CSb is asserted to 0. During a write command, the 15-bit address and 8-bit data values follow the read or write bit MSB-first and are latched on the rising edge of SCLK. During a read command, the SDO output is enabled shortly after the 16th rising edge of SCLK and outputs the read value MSB first before the SDO output is returned to a high impedance state. The read or write command is completed on the SCLK rising edge on which the data word's LSB is latched. CSb may be de-asserted to 1 after the LSB is latched into the device.

The SPI allows command streaming where multiple commands are made without de-asserting CSb in-between commands. The commands in the stream must be of similar types, either read or write. Each subsequent command applies to the register address adjacent to the register accessed in the previous command. The address order can be configured as either ascending or descending. Command streaming is accomplished by immediately following a completed command with another set of 8 rising edges of SCLK without de-asserting CSb. During a write command, an 8-bit data word is input on the SDI input for each subsequent set of SCLK edges. During a read command, data is output from SDO for each subsequent set of SCLK edges. Each subsequent command is considered finished after the 8th rising edge of SCLK. De-asserting CSb aborts an incomplete command.

The SDO output is high impedance at all times other than during the final portion of a read command. During the time that the SDO output is active, the logic level is determined by a configuration register. The SPI output logic level must be properly configured after power up and before making a read command to prevent damaging the receiving device or any other device connected to the SPI bus. Until the SPI_CFG register is properly configured, voltages on the SDO output may be as high as the VA3.0 supply during a read command. The SDI, SCLK, and CSB pins are all 1.2-V to 3.0-V compatible.

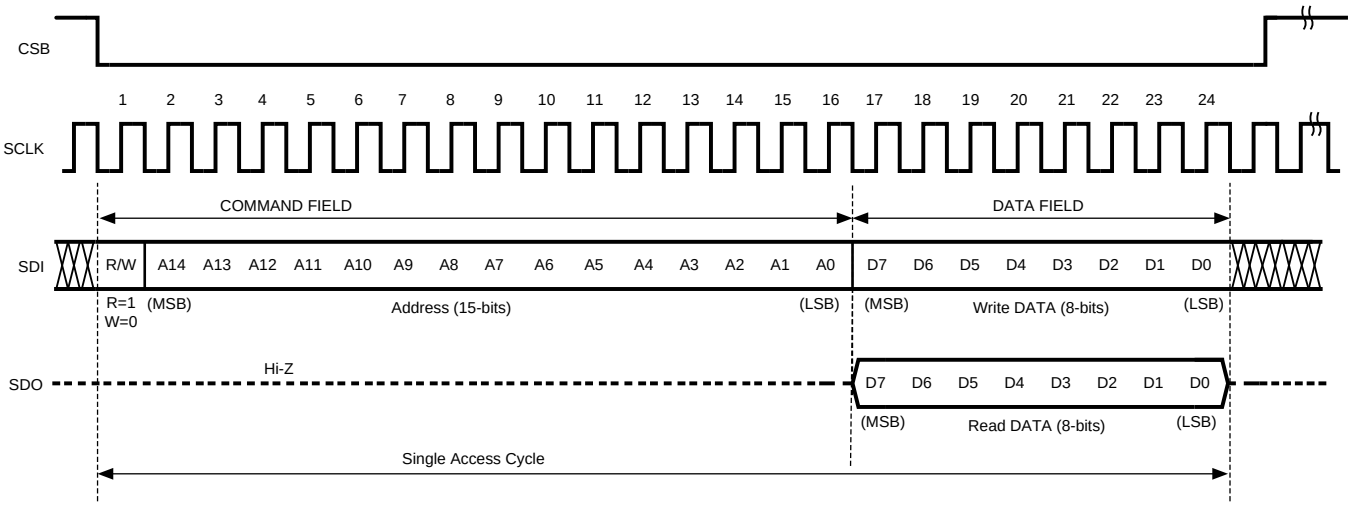

Figure 37. Serial Interface Protocol

8.4 Device Functional Modes

8.4.1 Power-Down and Sleep Modes

Power-down and sleep modes are provided to allow the user to reduce the power consumption of the device without disabling power supplies. Both modes reduce power consumption by the same amount but they differ in the amount of time required to return to normal operation. Upon changing from Power Down back to Normal operation, an ADC calibration routine is performed. Waking from sleep mode does not perform ADC calibration (see *ADC Core Calibration* for more details). Neither power-down mode nor sleep mode resets configuration registers.

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8.5 Register Map

Table 5. ADC31JB68 Register Map

Register	ADDRESS	DFLT	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]
CONFIG_A	0x0000	0x3C	SR	Res (0)	ASCEND	Res (1)	PAL[3:0]			
Address 0x0001 Reserved										
DEVICE _CONFIG	0x0002	0x00	Reserved (000000)						PD_MODE[1:0]	
CHIP_TYPE	0x0003	0x03	Reserved (0000)				CHIP_TYPE[3:0]			
CHIP_ID	0x0004	0x11	CHIP_ID[7:0]							
	0x0005	0x00	CHIP_ID[15:8]							
CHIP _VERSION	0x0006	0x00	CHIP_VERSION[7:0]							
Address 0x0007-0x000B Reserved										
VENDOR_ID	0x000C	0x51	VENDOR_ID[7:0]							
	0x000D	0x04	VENDOR_ID[15:8]							
SPI_CFG	0x0010	0x01	Reserved (000000)						VSPI[1:0]	
OM1	0x0012	0xC1	DF	SYS_CM[1:0]		Res (00)		SYSG _EN	Res(01)	
OM2	0x0013	0x20	Reserved (001000)						CLKDIV [1:0]	
IMB_ADJ	0x0014	0x00	Res (0)	AMPADJ[2:0]			PHADJ[3:0]			
Address 0x0016-0x003A Reserved										
OVR_EN	0x003A	0x00	Reserved (0000000)							OVR_EN
OVR_HOLD	0x003B	0x00	Reserved (000000)						OVR_HOLD[1:0]	
OVR_TH	0x003C	0x00	OVR_TH[7:0]							
DC_MODE	0x003D	0x00	Reserved (00000)					DC_TC[1:0]		DC_EN
Address 0x003E-0x0046 Reserved										
SER_CFG	0x0047	0x00	Res(0)	VOD[2:0]			Res (0)	DEM[2:0]		
Address 0x0048-0x005F Reserved										
JESD_CTRL1	0x0060	0x7F	SCR _EN	K_M1[4:0]					Res (0)	JESD _EN
JESD_CTRL2	0x0061	0x00	Reserved (0000)				JESD_TEST_MODE[3:0]			
JESD_RSTEP	0x0062	0x01	JESD_RSTEP[7:0]							
	0x0063	0x00	JESD_RSTEP[15:8]							
SER_INV	0x0064	0x00	Reserved (0000)				SO1_INV _EN	SO0_IN V _EN	Reserved (00)	
Address 0x0065-0x006B Reserved										
JESD_STATUS	0x006C	N/A	Res (0)	LINK	SYNC	RE ALIGN	ALIGN	PLL _LOCK	CAL _DONE	CLK _RDY
Address 0x006D- Reserved										

8.5.1 Register Descriptions

8.5.1.1 CONFIG_A (address = 0x0000) [reset = 0x3C]

Figure 38. CONFIG_A

7	6	5	4	3	2	1	0
SR	Reserved	ASCEND	Reserved	PAL[3:0]			
R/W	R/W	R/W	R	R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. CONFIG_A

Bit	Field	Type	Reset	Description
7	SR	R/W	0	Setting this soft reset bit causes all registers to be reset to their default state. This bit is self-clearing.
6	Reserved	R/W	0	Reserved and must be written with 0.
5	ASCEND	R/W	1	Order of address change during streaming read or write commands. 0 : Address is decremented during streaming reads or writes. 1 : Address is incremented during streaming reads or writes (default).
4	Reserved	R	1	Reserved and must be written with 1.
3:0	PAL[3:0]	R/W	1100	Palindrome bits are bit 3 = bit 4, bit 2 = bit 5, bit 1 = bit 6, and bit 0 = bit 7. (1)

(1) All writes to this register must be a palindrome (for example, bits [3:0] are a mirror image of bits [7:4]). If the data is not a palindrome, the entire write is ignored.

8.5.1.2 DEVICE CONFIG (address = 0x0002) [reset = 0x00]

Figure 39. DEVICE CONFIG

7	6	5	4	3	2	1	0
Reserved						PD_MODE [1:0]	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. DEVICE CONFIG

Bit	Field	Type	Reset	Description
7:2		R/W	000000	Reserved and must be written with 000000.
1:0	PD_MODE [1:0]	R/W	00	Power-down mode 00 : Normal operation (default) 01 : Reserved 10 : Sleep operation (low power, fastest resume) 11 : Power-down (lowest power)

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8.5.1.3 CHIP_TYPE (address = 0x0003) [reset = 0x03]

Figure 40. CHIP_TYPE

7	6	5	4	3	2	1	0
Reserved				CHIP_TYPE			
R/W				R			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. CHIP_TYPE

Bit	Field	Type	Reset	Description
7:4		R/W	0000	Reserved and must be written with 0000.
3:0	CHIP_TYPE [3:0]	R	0011	Chip type that always returns 0x3, indicating that the part is a high-speed ADC

8.5.1.4 CHIP_ID (address = 0x0005, 0x0004) [reset = 0x00, 0x1B]

Figure 41. CHIP_ID

7	6	5	4	3	2	1	0
CHIP_ID							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. CHIP_ID

Bit	Field	Type	Reset	Description
0x0004[7:0]	CHIP_ID [7:0]	R	0x1B	Chip ID least significant word
0x0005[7:0]	CHIP_ID [15:8]	R	0x00	Chip ID most significant word

8.5.1.5 CHIP_VERSION (address =0x0006) [reset = 0x00]

Figure 42. CHIP_VERSION

7	6	5	4	3	2	1	0
CHIP_VERSION							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. CHIP_VERSION

Bit	Field	Type	Reset	Description
7:0	CHIP_VERSION [7:0]	R	0x00	Chip version

8.5.1.6 VENDOR_ID (address = 0x000D, 0x000C) [reset = 0x04, 0x51]

Figure 43. VENDOR_ID

7	6	5	4	3	2	1	0
VENDOR_ID							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. VENDOR_ID

Bit	Field	Type	Reset	Description
0x000C[7:0]	VENDOR_ID [7:0]	R	0x51	Vendor ID. Texas Instruments vendor ID is 0x0451.
0x000D[7:0]	VENDOR_ID [15:8]	R	0x04	

8.5.1.7 SPI_CFG (address = 0x0010) [reset = 0x01]

Figure 44. SPI_CFG

7	6	5	4	3	2	1	0
Reserved						VSP	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. SPI_CFG

Bit	Field	Type	Reset	Description
7:2	Reserved	R/W	000000	Reserved and must be written with 000000.
1:0	VSPI[1:0]	R/W	01	SPI logic level controls the SDO output logic level. 00 : 1.2 V 01 : 3.0 V (default) 10 : Reserved 11 : 1.8 V This register must be configured (written) before making a read command with a SPI that is not a 3-V logic level. The SPI inputs (SDI, SCLK, and CSb) are compatible with logic levels ranging from 1.2 to 3 V.

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8.5.1.8 OM1 (Operational Mode 1) (address = 0x0012) [reset = 0xC1]

Figure 45. OM1 (Operational Mode 1)

7	6	5	4	3	2	1	0
DF	SYS)CM[1:0]		Reserved		SYSG_EN	Reserved	
R/W	R/W		R/W		R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. OM1 (Operational Mode 1)

Bit	Field	Type	Reset	Description
7	DF	R/W	1	Output data format 0 : Offset binary 1 : Signed 2s complement (default)
6:5	SYS_CM[1:0]	R/W	10	SYSREF Common-Mode Configuration When the SYSREF signal interface is DC coupled, the SYSREF+/- input receiver must be configured to appropriately match the common-mode of the received signal. Set the register field according to the expected common-mode. 00 : 0.4 V - 0.59 V (R_{TAIL} = Open) 01 : 0.6 V - 0.99 V (R_{TAIL} = 4 kΩ) 10 : 1.0 V - 1.49 V (R_{TAIL} = 1 kΩ, default) 11 : 1.5 V - 2.0 V (R_{TAIL} = 0 Ω) • The R_{TAIL} indicates the value of the variable resistor shown in Figure 72
4:3	Reserved	R/W	00	Reserved and must be written with 00.
2	SYSG_EN	R/W	0	SYSREF detection gate enable 0 : SYSREF gate is disabled; (input is ignored, default) 1 : SYSREF gate is enabled
1:0	Reserved	R/W	01	Reserved. Must be written with 01.

8.5.1.9 OM2 (Operational Mode 2) (address = 0x0013) [reset = 0x20]

Figure 46. OM2 (Operational Mode 2)

7	6	5	4	3	2	1	0
Reserved						CLKDIV	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. OM2 (Operational Mode 2)

Bit	Field	Type	Reset	Description
7:2	Reserved	R/W	001000	Reserved and must be written with 001000.
1:0	CLKDIV[1:0]	R/W	00	Clock divider ratio. Sets the value of the clock divide factor, CLKDIV 00 : Divide-by-1, CLKDIV = 1 (default) 01 : Divide-by-2, CLKDIV = 2 10 : Divide-by-4, CLKDIV = 4 11 : Reserved

8.5.1.10 IMB_ADJ (Imbalance Adjust) (address = 0x0014) [reset = 0x00]

Figure 47. IMB_ADJ (Imbalance Adjust)

7	6	5	4	3	2	1	0
Reserved	AMPADJ[2:0]			PHADJ[3:0]			
R/W	R/W			R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. IMB_ADJ (Imbalance Adjust)

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved. Must be written with 0.
6:4	AMPADJ[2:0]	R/W	000	Analog input amplitude imbalance correction 7 = +30 Ω VIN+, –30 Ω VIN– 6 = +20 Ω VIN+, –20 Ω VIN– 5 = +10 Ω VIN+, –10 Ω VIN– 4 = Reserved 3 = –30 Ω VIN+, +30 Ω VIN– 2 = –20 Ω VIN+, +20 Ω VIN– 1 = –10 Ω VIN+, +10 Ω VIN– 0 = +0 Ω VIN+, –0 Ω VIN– (default) Resistance changes indicate variation of the internal single-ended termination
3:0	PHADJ[3:0]	R/W	0000	Analog input phase imbalance correction 15 = +1.68 pF VIN– ... 10 = +0.48 pF VIN– 9 = +0.24 pF VIN– 8 = Reserved 7 = +1.68 pF VIN+ ... 2 = +0.48 pF VIN+ 1 = +0.24 pF VIN+ 0 = +0 pF VIN+, +0 pF VIN– (default) Capacitance changes indicate the addition of internal capacitive load on the given pin.

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8.5.1.11 OVR_EN (Over-Range Enable) (address = 0x003A) [reset = 0x00]

Figure 48. OVR_EN (Over-Range Enable)

7	6	5	4	3	2	1	0
Reserved							OVR_EN
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. OVR_EN (Over-Range Enable)

Bit	Field	Type	Reset	Description
7:1	Reserved	R/W	000000	Reserved and must be written as 000000.
0	OVR_EN	R/W	0	Over-range Enable. 0 : Over-Range function is disabled. (default) 1 : Over-Range function is enabled and output via the SDO pin.

8.5.1.12 OVR_HOLD (Over-Range Hold) (address = 0x003B) [reset = 0x00]

Figure 49. OVR_HOLD (Over-Range Hold)

7	6	5	4	3	2	1	0
Reserved						OVR_HOLD [1:0]	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. OVR_HOLD (Over-Range Hold)

Bit	Field	Type	Reset	Description
7:2	Reserved	R/W	000000	Reserved and must be written as 000000.
1:0	OVR_HOLD [1:0]	R/W	00	Over-range hold function. In the event of an input signal larger than the full-scale range, an over-range event occurs and the over-range indicators are asserted. OVR_HOLD determines the amount of time the over-range indicators remain asserted after the input signal has reduced below full-scale. 00 : OVR indicator extended by +0 clock cycles (default) 01 : OVR indicator extended by +3 clock cycles 10 : OVR indicator extended by +7 clock cycles 11 : OVR indicator extended by +15 clock cycles Note: • The unit of clock cycles corresponds to the period of the internal sampling clock. • The over-range indicators also experience a latency from when the over-range signal is sampled to when the indicator is asserted or de-asserted.

8.5.1.13 OVR_TH (Over-Range Threshold) (address = 0x003C) [reset = 0x00]

Figure 50. OVR_TH (Over-Range Threshold)

7	6	5	4	3	2	1	0
OVR_TH [7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. OVR_TH (Over-Range Threshold)

Bit	Field	Type	Reset	Description
7:0	OVR_TH [7:0]	R/W	00000000	Over-range threshold. This field is an unsigned value from 0 to 255. OVR_TH sets the over-range detection thresholds for the ADC. If the 16-bit signed data exceeds the thresholds, then the over-range bit is set. The 16-bit thresholds are ± OVR_TH × 128 codes from the low and high full-scale codes (32767 and –32768 in signed 2s complement). If OVR_TH is 0, then the default threshold is used (full scale).

OVR_TH	16-bit Threshold		Threshold Relative to Peak Full Scale [dB]
	2 Complement	Offset Binary	
255 (0xFF)	±32640	65408 / 128	–0.03
254 (0xFE)	±32512	65280 / 256	–0.07
128 (0x80)	±16384	49152 / 16,384	–6.02
2 (0x02)	±256	33024 / 32512	–42.14
1 (0x01)	±128	32896 / 32640	–48.16
0 (0x00) (default)	+32767 / –32768	65535 / 0	–0.0

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8.5.1.14 DC_MODE (DC Offset Correction Mode) (address = 0x003D) [reset = 0x00]

Figure 51. DC_MODE (DC Offset Correction Mode)

7	6	5	4	3	2	1	0
Reserved					TC_DC[1:0]		DC_EN
R/W					R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. DC_MODE (DC Offset Correction Mode)

Bit	Field	Type	Reset	Description
7:3	Reserved	R/W	00000	Reserved and must be written as 00000.
2:1	TC_DC[1:0]	R/W	00	DC offset filter time constant. The time constant determines the filter bandwidth of the DC high-pass filter.

TC_TD	Time Constant (F_S = 500 MSPS)	3-dB Bandwidth (F_S = 500 MSPS)	3-dB Bandwidth (Normalized)
00	8.6 µs	18.5 kHz	$37e^{-6}$ × Fs
01	65 µs	2.45 kHz	$4.9e^{-6}$ × Fs
10	526 µs	303 Hz	$605e^{-9}$ × Fs
11	4.2 ms	38 Hz	$76e^{-9}$ × Fs

0	DC_EN	R/W	0	DC offset correction enable 0 : Disable DC offset correction 1 : Enable DC offset correction

8.5.1.15 SER_CFG (Serial Lane Transmitter Configuration) (address = 0x0047) [reset = 0x00]

Figure 52. SER_CFG (Serial Lane Transmitter Configuration)

7	6	5	4	3	2	1	0
Reserved	VOD[2:0]			Reserved	DEM[2:0]		
R/W	R/W			R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. SER_CFG (Serial Lane Transmitter Configuration)

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved. Must be written as 0.
6:4	VOD[2:0]	R/W	000	Serial-lane transmitter driver output differential peak-to-peak voltage amplitude. 000 : 0.400 V (default) 001 : 0.470 V 010 : 0.540 V 011 : 0.610 V 100 : 0.670 V 101 : 0.740 V 110 : 0.790 V 111 : 0.840 V Reported voltage values are nominal values at low-lane rates with de-emphasis disabled.
3	Reserved	R/W	0	Reserved and must be written as 0.
2:0	DEM[2:0]	R/W	000	Serial lane transmitted de-emphasis. 000 : 0 dB 001 : –0.8 dB 010 : –2.4 dB 011 : –3.8 dB 100 : –4.9 dB 101 : –6.3 dB 110 : –7.7 dB 111 : –10.3 dB Reported de-emphasis values are nominal values at low-lane rates with VOD = 4.

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8.5.1.16 JESD_CTRL1 (JESD Configuration Control 1) (address = 0x0060) [reset = 0x7F]

Note: Before altering any parameters in this register, JESD_EN must be set = 0. Changing parameters while JESD_EN = 1 is not supported.

Figure 53. JESD_CTRL1 (JESD Configuration Control 1)

7	6	5	4	3	2	1	0
SCR_EN	K_M1[4:0]					Reserved	JESD_EN
R/W	R/W					R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. JESD_CTRL1 (JESD Configuration Control 1)

Bit	Field	Type	Reset	Description
7	SCR_EN	R/W	0	Scrambler enable. 0 : Disabled (default) 1 : Enabled Note: • JESD_EN must be set to 0 before altering this field.
6:2	K_M1[4:0]	R/W	11111	Number of frames per multi-frame minus 1. The binary values of K_M1 represent the value (K – 1) 00000 : Reserved 00001 : Reserved … 01111 : Reserved 10000 : K = 17 … 11111 : K = 32 (default) Note: • K must be in the range 17 to 32. Values outside this range are either reserved or may produce unexpected results. • JESD_EN must be set to 0 before altering this field.
1	Reserved	R/W	1	Reserved and must be written with 1.
0	JESD_EN	R/W	1	JESD204B link enable. When enabled, the JESD204B link synchronizes and transfers data normally. When the link is disabled, the serial transmitters output a repeating, alternating 01010101 stream. 0 : Disabled 1 : Enabled (default)

8.5.1.17 JESD_CTRL2 (JESD Configuration Control 2) (address = 0x0061) [reset = 0x00]

Figure 54. JESD_CTRL2 (JESD Configuration Control 2)

7	6	5	4	3	2	1	0
Reserved				ESD_TEST_MODES[3:0]			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. JESD_CTRL2 (JESD Configuration Control 2)

Bit	Field	Type	Reset	Description
7:4	Reserved	R/W	0000	Reserved. Must be written as 0000.
3:0	ESD_TEST_MODES[3:0]	R/W	0000	JESD204B test modes. 0000 : Test mode disabled. Normal operation (default) 0001 : PRBS7 test mode 0010 : PRBS15 test mode 0011 : PRBS23 test mode 0100 : Reserved 0101 : ILA test mode 0110 : Ramp test mode 0111 : K28.5 test mode 1000 : D21.5 test mode 1001: Logic low test mode (serial outputs held low) 1010: Logic high test mode (serial outputs held high) 1011 – 1111 : Reserved Note: • JESD_EN must be set to 0 before altering this field.

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8.5.1.18 JESD_RSTEP (JESD Ramp Pattern Step) (address = 0x0063, 0x0062) [reset = 0x00, 0x01]

Figure 55. JESD_RSTEP (JESD Ramp Pattern Step)

7	6	5	4	3	2	1	0
JESD_RSTEP							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. JESD_RSTEP (JESD Ramp Pattern Step)

Bit	Field	Type	Reset	Description
0x0062[7:0]	JESD_RSTEP [7:0]	R/W	0x01	JESD204B ramp test mode step The binary value JESD_RSTEP[15:0] corresponds to the step of the ramp mode step. A value of 0x0000 is not allowed. Note: • JESD_EN must be set to 0 before altering this field.
0x0063[7:0]	JESD_RSTEP [15:8]	R/W	0x00	

8.5.1.19 SER_INV (Serial Lane Inversion Control) (address = 0x0064) [reset = 0x00]

Figure 56. SER_INV (Serial Lane Inversion Control)

7	6	5	4	3	2	1	0
Reserved				SO1_INV_EN	SO0_INV_EN	Reserved	
R/W				R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. SER_INV (Serial Lane Inversion Control)

Bit	Field	Type	Reset	Description
7:4	Reserved	R/W	0000	Reserved. Must be written as 0000.
3	SO1_INV_EN	R/W	0	Serial Lane Inversion enable for SO1 and SO0 Output Drivers 0 : Non-Inverted Polarity (default) 1 : Inverted Polarity Note: • JESD_EN must be set to 0 before altering this field.
2:	SO0_INV_EN	R/W	0	
1:0	Reserved	R/W	00	Reserved. Must be written as 00.

8.5.1.20 JESD_STATUS (JESD Link Status) (address = 0x006C) [reset = N/A]

Figure 57. JESD_STATUS (JESD Link Status)

7	6	5	4	3	2	1	0
Reserved	LINK	SYNC	REALIGN	ALIGN	PLL_LOCK	CAL_DONE	CLK_RDY
R	R	R	R/W	R/W	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. JESD_STATUS (JESD Link Status)

Bit	Field	Type	Reset	Description
7	Reserved	R	N/A	Reserved.
6	LINK	R	N/A	JESD204B link status This bit is set when synchronization is finished, transmission of the ILA sequence is complete, and valid data is being transmitted. 0 : Link not established 1 : Link established and valid data transmitted
5	SYNC	R	N/A	JESD204B link synchronization request status This bit is cleared when a synchronization request is received at the SYNCb input. 0 : Synchronization request received at the SYNCb input and synchronization is in progress 1 : Synchronization not requested Note: • SYNCb must be asserted for at least four local frame clocks before synchronization is initiated. The SYNC status bit reports the status of synchronization, but does not necessarily report the current status of the signal at the SYNCb input.
4	REALIGN	R/W	N/A	SYSREF re-alignment status This bit is set when a SYSREF event causes a shift in the phase of the internal frame or LMFC clocks. Note: • Write a 1 to REALIGN to clear the bit field to a 0 state. • SYSREF events that do not cause a frame or LMFC clock phase adjustment do not set this register bit. • If CLK_RDY becomes low, this bit is cleared.
3	ALIGN	R/W	N/A	SYSREF alignment status This bit is set when the ADC has processed a SYSREF event and indicates that the local frame and multi-frame clocks are now based on a SYSREF event. Note: • Write a 1 to ALIGN to clear the bit field to a 0 state. • Rising-edge SYSREF event sets ALIGN bit. • If CLK_RDY becomes low, this bit is cleared.
2	PLL_LOCK	R	N/A	PLL lock status. This bit is set when the PLL has achieved lock. 0 : PLL unlocked 1 : PLL locked
1	CAL_DONE	R	N/A	ADC calibration status This bit is set when the ADC calibration is complete. 0 : Calibration currently in progress or not yet completed 1 : Calibration complete Note: • Calibration must complete before SYSREF detection (SYS_EN) can be enabled.
0	CLK_RDY	R	N/A	Input clock status This bit is set when the ADC is powered-up and detects an active clock signal at the CLKIN input. 0 : CLKIN not detected 1 : CLKIN detected

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Optimizing Converter Performance

9.1.1.1 Internal Noise Sources

The signal to noise ratio of the ADC is limited by the following noise sources inherent to the device: 1) Quantization Noise, 2) Thermal Noise, 3) Sampling Instant Noise (Aperture Jitter). These sources combine together to limit the noise performance of the converter as described by Equation 1. Noise sources external to the ADC can generally be included in this equation as an RMS summation to determine system performance.

$$SNR_{ADC}[dBc] = -20 \times \log \sqrt{\left(10^{-\frac{SNR_{Quantizatoin\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

Quantization noise is independent of the input signal but does not affect the noise performance of the ADC31JB68 because the SNR limitation of a 16-bit ADC due to quantization noise is 96-dB, well above the SNR of this device. The thermal noise is input independent, spread evenly across the spectrum, and the main limitation for signals with lower frequencies or lower amplitudes.

If quantization and thermal noise is ignored, the fundamental SNR limitation due to aperture jitter can be calculated using Equation 2.

$$SNR_{Jitter}[dBc] = -20 \times \log(2\pi \times f_{in} \times T_{jitter}) \quad (2)$$

Signals with larger amplitudes and higher frequencies introduce signal dependent sampling instant noise due to the Jitter on the sampling clock edge. This noise includes a broadband component that raises the overall noise spectral density as well as a in-close noise component that is spectrally shaped and concentrates around the signal in the spectrum. The differential clock receiver of the ADC31JB68 has a very-low noise floor and wide bandwidth. Minimizing the aperture jitter requires a sampling clock with a steep edge rate at the zero crossing. Lesser edge rates increase the aperture jitter as demonstrated in Figure 58 which shows the SNR limitation due to aperture jitter as a function of clock edge range and input signal frequency.

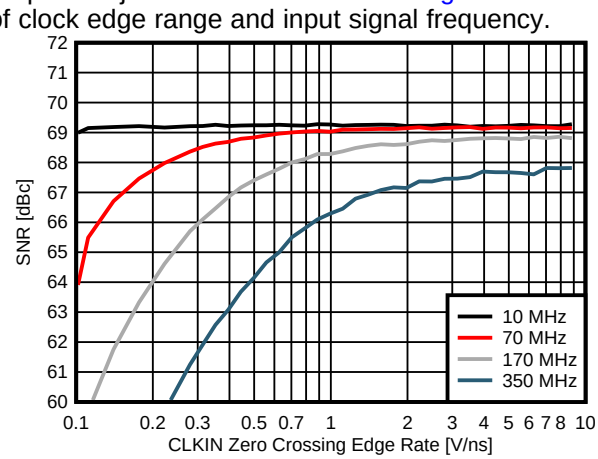

Figure 58. Aperture Jitter vs Input Clock Edge Rate, -1 dBFS Input Signal

Application Information (continued)

9.1.1.2 External Noise Sources

Noise sources external to the ADC device that impact the overall system performance through the ADC include: 1) Analog Input Signal Path noise, 2) Sampling Clock Signal Path Noise, 3) Supply Noise

Analog input signal path noise comes from devices in the signal path prior to the ADC and enters through the analog input (VIN+/-). An anti-aliasing filter must be included in front of the ADC to limit the noise bandwidth and prevent the aliasing of noise into any band of interest. Sampling clock signal path noise enters through the sampling clock input (CLKIN+/-) and adds noise similar to the Aperture Jitter. External clock jitter can be minimized by using high quality clock sources and jitter cleaners (PLLs) as well as bandpass filters at the clock input.

The total clock jitter (T_{Jitter}), including the aperture jitter of the ADC and external clock noise can be calculated with Equation 3 and applied to Equation 1 and Equation 2 to determine the system impact. Figure 59 shows the simulated impact on the SNR of the ADC31JB68 output spectrum for a given total jitter and input signal frequency.

$$T_{Jitter} = \sqrt{\left(T_{Jitter,Ext.Clock_Input}\right)^2 + \left(T_{Aperture_ADC}\right)^2} \quad (3)$$

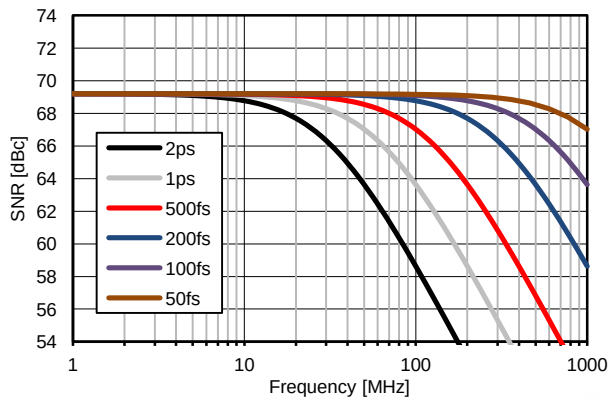

Figure 59. SNR Limit Due to Total Jitter of Sampling Clock With a -1 dBFS Input Signal

Additional noise may couple to the clock path through power supplies. Take care to provide a very-low noise power supply and isolated supply return path to minimize noise added to the supply. Spurious noise added to the clock path results in symmetrical, modulated spurs around large input signals. These spurs have a constant magnitude in units of dB relative to the input signal amplitude or carrier, [dBc].

9.1.2 Analog Input Considerations

9.1.2.1 Differential Analog Inputs and Full Scale Range

The ADC31JB68 device has one channel with a pair of analog signal input pins: VIN+, VIN−. V_{IN}, the input differential signal for a channel, is defined as $V_{IN} = (V_{IN+}) – (V_{IN–})$. Table 26 shows the expected input signal range when the differential signal swings about the input common mode voltage, V_{CM}. The full-scale differential peak-to-peak input range is equal to twice the internal reference voltage, V_{REF}. Nominally, the full scale range is 1.7 Vpp-diff, therefore the maximum peak-to-peak single-ended voltage is 0.85 Vpp at each of the VIN+ and VIN− pins.

The single-ended signals must be opposite in polarity relative to the V_{CM} voltage to provide a purely differential signal, otherwise the common-mode component may be rejected by the ADC input. Table 26 indicates the input to output relationship of the ADC31JB68 device where V_{REF} = 0.85 V.

Differential signals with amplitude or phase imbalances result in lower system performance compared to perfectly balanced signals. Imbalances in signal path circuits lead to differential-to-common-mode signal conversion and differential signal amplitude loss as shown in *Figure 60*. This deviation or imbalance directly causes a reduction in the signal amplitude and may also lead to distortion, particularly even order harmonic distortion, as the signal propagates through the signal path. The Amplitude and Phase Imbalance Correction feature in the ADC31JB68 helps to correct amplitude or phase errors of the signal.

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Application Information (continued)

Table 26. Mapping of the Analog Input Full Scale Range to Digital Codes

VIN+	VIN–	2s Complement Output	Binary Output	Note
$V_{CM} + V_{REF} / 2$	$V_{CM} – V_{REF} / 2$	0111 1111 1111 1111	1111 1111 1111 1111	Positive full-scale
$V_{CM} + V_{REF} / 4$	$V_{CM} – V_{REF} / 4$	0100 0000 0000 0000	1100 0000 0000 0000	
V_{CM}	V_{CM}	0000 0000 0000 0000	1000 0000 0000 0000	Mid-scale
$V_{CM} – V_{REF} / 4$	$V_{CM} + V_{REF} / 4$	1100 0000 0000 0000	0100 0000 0000 0000	
$V_{CM} – V_{REF} / 2$	$V_{CM} + V_{REF} / 2$	1000 0000 0000 0000	0000 0000 0000 0000	Negative full-scale

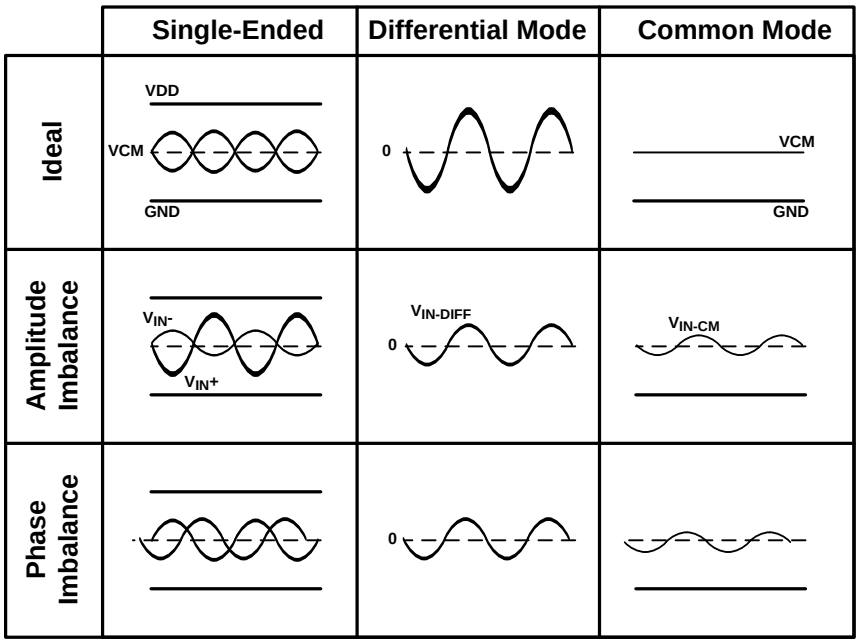

Figure 60. Differential Signal Waveform and Signal Imbalance

9.1.2.2 Analog Input Network Model

Matching the impedance of the driving circuit to the input impedance of the ADC can be important for a flat gain response through the network across frequency. In very broadband applications or lowpass applications, the ADC driving network must have very low impedance with a small termination resistor at the ADC input to maximize the bandwidth and minimize the bandwidth limitation posed by the capacitive load of the ADC input. In bandpass applications, a designer may either design the anti-aliasing filter to match to the complex impedance of the ADC input at the desired intermediate frequency, or consider the resistive part of the ADC input to be part of the resistive termination of the filter and the capacitive part of the ADC input to be part of the filter itself. The capacitive load of the ADC input can be absorbed into most LC bandpass filter designs with a final shunt LC tank stage.

The analog input circuit of the ADC31JB68 device is a buffered input with an internal differential termination. Compared to an ADC with a switched-capacitor input sampling network that has a time-varying input impedance, the ADC31JB68 device provides a time-constant input impedance that simplifies the interface design joining the ADC and ADC driver. A simplified passive model of the ADC input network is shown in Figure 61 that includes the termination resistance, input capacitance, parasitic bond-wire inductance, and routing parastics.

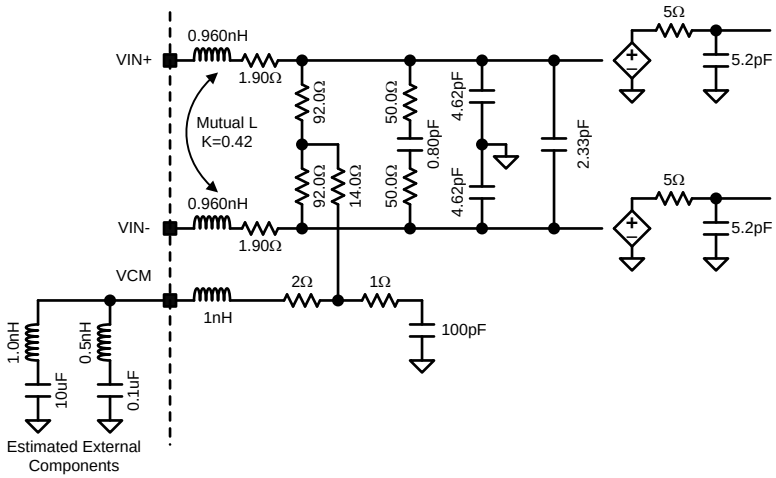

Figure 61. Simplified Analog Input Network Circuit Model

A more accurate load model is described by the measured differential SDD11 (100-Ω) parameter model. A plot of the differential impedance derived from the model is shown on the Smith chart of Figure 62.

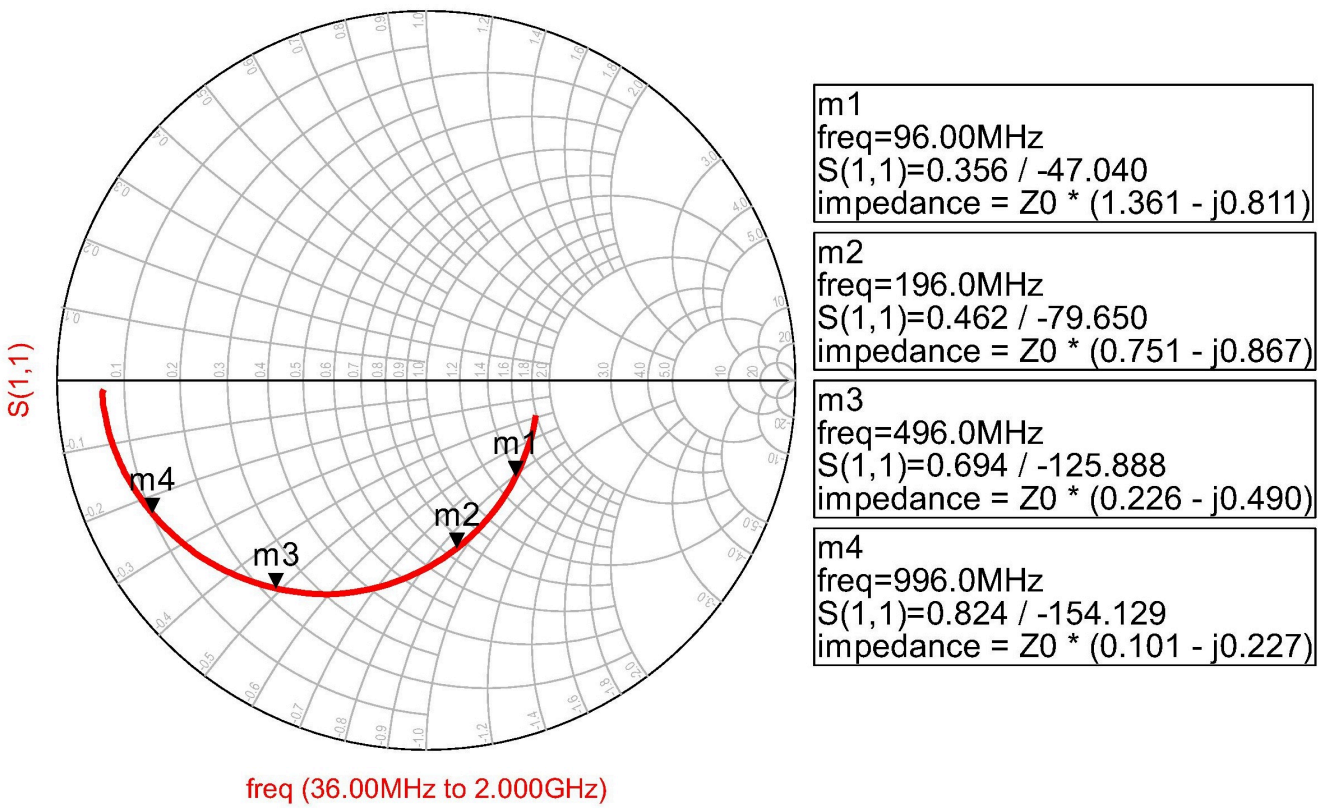

Figure 62. Differential 1-Port S-Parameter Measurement of the ADC Input (Sdd11, Z_0=100 Ω)

9.1.2.3 Input Bandwidth

The input bandwidth response is shown in Figure 63 and depends on the measurement network. The impedance of the driving source or any series resistance in the driving network greatly impacts the measured bandwidth. Three separate measurement methodologies are shown here. The first, shown in Figure 64, is the network used to measure the reported bandwidth in the performance tables. It uses a 50-Ω source, high bandwidth balun, and custom input network.

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Another measurement using the simplified network of Figure 65 demonstrates the bandwidth of the ADC using a low impedance source near the ADC pins. The peaking in the frequency response is caused by the resonance between the package bond wires and input capacitance as well as a parasitic 0.5-nH series trace inductance leading to the device pins. This peaking is typically made insignificant by the anti-aliasing filter that precedes the ADC input.

The third measurement network of Figure 65 also assumes a low impedance voltage source but shows the bandwidth flattening impact of adding 10-Ω in series with the VIN+ and VIN– input pins.

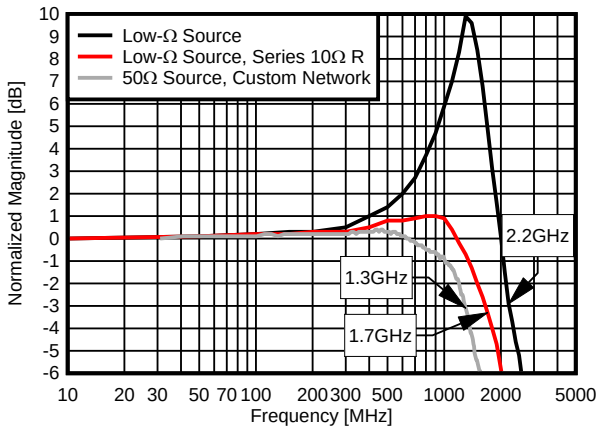

Figure 63. Measured Input Voltage Frequency Response

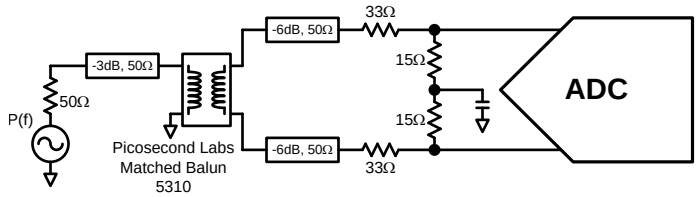

Figure 64. 50-Ω Source, Bandwidth Measurement Network

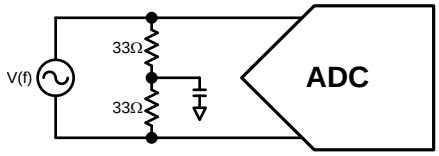

Figure 65. Low-Ω Source Bandwidth Measurement (Simplified)

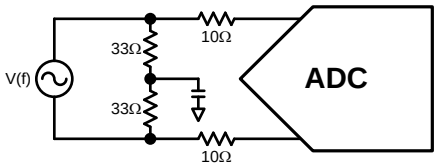

Figure 66. Low-Ω Source, Series 10Ω R, Bandwidth Measurement (Simplified)

9.1.2.4 Driving the Analog Input

The analog input may be driven by a number of network types depending on the end application. The most important design aspects to consider when designing the ADC voltage driver network are signal coupling, impedance matching, differential signal balance, anti-alias filtering, and signal level.

An analog signal is AC or DC coupled to the ADC depending on whether signal frequencies near DC must be sampled without attenuation. DC coupling requires tight control of the output common-mode of the ADC driver to match the input common-mode of the ADC input. In the case of DC coupling, the bias at the VCM pin may be used as a reference to set the driver output common-mode, but the load cannot source or sink more current than the specified value in the electrical parameters. AC coupling does not require strict common-mode control of the driver and is typically achieved using AC coupling capacitors or a flux-coupled transformer. AC coupling capacitors should be chosen to have 0.1-Ω impedance or less over the frequency band of interest. LC filter designs may be customized to achieve either AC or DC coupling.

The internal input network of the ADC31JB68 device has the common-mode voltage bias provided through internal shunt termination resistors. The recommended bias for the external termination resistors is the common-mode reference voltage from the VCM pin.

Impedance matching in high speed signal paths using an ADC is dictated by the characteristic impedance of interconnects and by the design of anti-aliasing filters. Matching the source to the load termination is critical to ensure maximum power transfer to the load and to maintain gain flatness across the desired frequency band. In applications with signal transmission lengths greater than 10% of the smallest signal wavelength (0.1 λ), matching is also desirable to avoid signal reflections and other transmission line effects. Applications that require high order anti-aliasing filters designs, including LC bandpass filters, require an expected source and load termination to ensure the passband bandwidth and ripple of the filter design. The recommended range of the ADC total load termination is from 50- to 200-Ω differential. The ADC31JB68 device has an internal differential load termination, but additional termination resistance may be added at the ADC input pins to adjust the total termination. The load termination at the ADC input presents a system-level design tradeoff. Better 2nd order distortion performance (HD2, IMD2) is achieved by the ADC using a lower load termination resistance, but the ADC driver must have a higher drive strength and linearity to drive the lower impedance. Choosing a 100-Ω total load termination is a reasonable balance between these opposing requirements.

Differential signal balance is important to achieve high distortion performance, particularly even order distortion (HD2, HD4). Circuits such as transformers and filters in the signal path between the signal source and ADC can disrupt the amplitude and phase balance of the differential signal before reaching the ADC input due to component tolerances or parasitic mismatches between the two parallel paths of the differential signal. Driving the ADC31JB68 device with a single-ended signal is not supported due to the tight restriction on the ADC input common-mode to maintain good distortion performance.

Converting a single-ended signal to a differential signal may be performed by an ADC driver or transformer. The advantages of the ADC driver over a transformer include configurable gain, isolation from previous stages of analog signal processing, and superior differential signal balancing. The advantages of using a transformer include no additional power consumption and little additional noise or distortion.

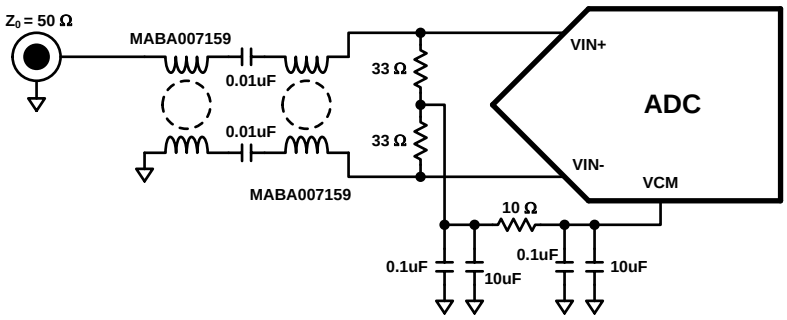

Figure 67. Transformer Input Network

Figure 67 is an example of driving the ADC input with a cascaded transformer configuration. The cascaded transformer configuration provides a high degree of differential signal balancing, the series 0.01-µF capacitors provide AC coupling, and the additional 33-Ω termination resistors provide a total differential load termination of 50 Ω. When additional termination resistors are added to change the ADC load termination, shunt terminations to the VCM reference are recommended to reduce common-mode fluctuations or sources of common-mode interference. A differential termination may be used if these sources of common-mode interference are minimal. In either case, the additional termination components must be placed as close to the ADC pins as possible. The MABA007159 transmission-line transformer from this example is widely available and results in good differential balance. Shunt capacitors at the ADC input, used to suppress the charge kickback of an ADC with switched-capacitor inputs, are not required for this purpose because the buffered input of the ADC31JB68 device does not kick back a significant amount of charge.

The insertion loss between an ADC driver and the ADC input is important because the driver must overcome the insertion loss of the connecting network to drive the ADC to full-scale and achieve the best SNR. Minimizing the loss through the network reduces the output swing and distortion requirements of the driver and usually translates to a system-level power savings in the driver. This can be accomplished by selecting transformers or filter designs with low insertion loss. Some filter designs may employ reduced source terminations or impedance conversions to minimize loss. Many designs require the use of high-Q inductors and capacitors to achieve an expected passband flatness and profile.

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Sampling theory states that if a signal with frequency f_{IN} is sampled at a rate less than 2 × f_{IN}, then it experiences aliasing, causing the signal to fall at a new frequency between 0 and F_S / 2 in the sampled spectrum and become indistinguishable from other signals at that new frequency.

To prevent out-of-band interference from aliasing onto a desired signal at a particular frequency, an anti-aliasing filter is required at the ADC input to attenuate the interference to a level below the level of the desired signal. This is accomplished by a lowpass filter in systems with desired signals from DC to F_S / 2 or with a bandpass filter in systems with desired signals greater than F_S / 2 (under-sampled signals). If an appropriate anti-aliasing filter is not included in the system design, the system may suffer from reduced dynamic range due to additional noise and distortion that aliases into the frequency bandwidth of interest.

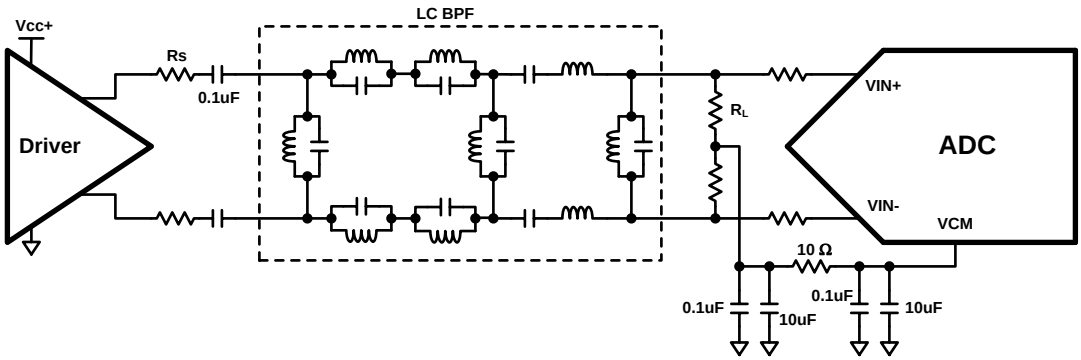

Figure 68. Bandpass Filter Anti-Aliasing Interface

An anti-aliasing filter is required in front of the ADC input in most applications to attenuate noise and distortion at frequencies that alias into any important frequency band of interest during the sampling process. An anti-aliasing filter is typically a LC lowpass or bandpass filter with low insertion loss. The bandwidth of the filter is typically designed to be less than F_S / 2 to allow room for the filter transition bands. Figure 68 is an example architecture of a 9 pole order LC bandpass anti-aliasing filter with added transmission zeros that can achieve a tight filtering profile for second Nyquist zone under-sampling applications.

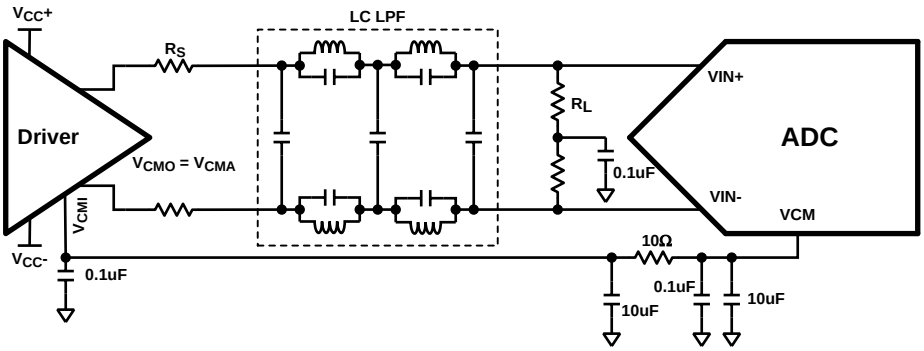

Figure 69. DC Coupled Interface

DC coupling to the analog input is also possible but the input common-mode must be tightly controlled for specified performance. The driver device must have an output common-mode that matches the input common-mode of the ADC31JB68 device and the driver must track the VCM output from the ADC31JB68 device, as shown in the example DC coupled interface of Figure 69, because the input common-mode varies with temperature. The common-mode path from the VCM output, through the driver device, back to the ADC31JB68 device input, and through a common-mode detector inside the ADC31JB68 device forms a closed tracking loop that will correct common-mode offset contributed by the driver device but the loop must be stable to ensure correct performance. The loop requires the large, 10-µF capacitor at the VCM output to establish the dominant pole for stability and the driver device must reliably track the VCM output voltage bias.

9.1.2.5 Clipping and Over-Range

The ADC31JB68 device has two regions of signal clipping: code clipping (over-range) and ESD clipping. When the input signal amplitude exceeds the full-scale reference range, code clipping occurs during which the digital output codes saturate. If the signal amplitude increases beyond the absolute maximum rating of the analog inputs, ESD clipping occurs due to the activation of ESD diodes.

Code clipping may be monitored via the SDO/OVR pin, which can be configured to output an quick detect over-range signal. The over-range threshold is programmable via the SPI. An over-range hold feature is also available to extend the time duration of the indicator longer than the over-range event itself to accommodate the case that a device monitoring the over-range signal cannot process at the rate of the ADC sampling clock.

ESD clipping and activation of the ESD diodes at the analog input should be avoided to prevent damage or shortened life of the device. This clipping may be avoided by selecting an ADC driver with an appropriate saturating output voltage, by placing insertion loss between the driver and ADC, by limiting the maximum amplitude earlier in the signal path at the system level, or by using a dedicated differential signal limiting device such as a clamp. Any signal swing limiting device must be chosen carefully to prevent added distortion to the signal.

9.1.3 CLKIN, SYSREF, and SYNCb Input Considerations

Clocking the ADC31JB68 device shares many common concepts and system design requirements with previously released ADC products that include a JESD204B interface. A SYSREF signal accompanies the device clock to provide phase alignment information for the output data serializer (as well as for the sampling instant when the clock divider is enabled) to ensure that the latency through the JESD204B link is always deterministic, a concept called deterministic latency. To ensure deterministic latency, the SYSREF signal must meet setup and hold requirements relative to CLKIN and the design of the clocking interfaces require close attention. As with other ADCs, the quality of the clock signal also influences the noise and spurious performance of the device.

9.1.3.1 Driving the CLKIN+ and CLKIN– Input

The CLKIN input circuit is composed of a differential receiver and an internal 100-Ω termination to a weakly driven common-mode of 0.5 V. TI recommends AC coupling to the CLKIN input with 0.1-uF external capacitors to maintain the optimal common-mode biasing. Figure 70 shows the CLKIN receiver circuit and an example AC coupled interface.

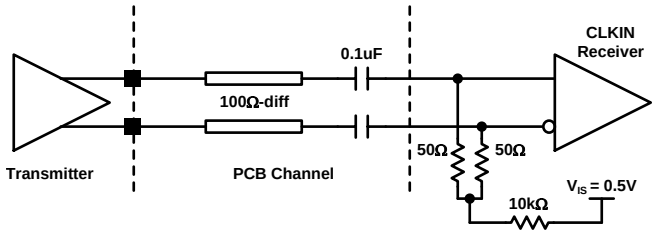

Figure 70. Driving the CLKIN Input With an AC Coupled Interface

DC coupling is allowed as long as the input common-mode range requirements are satisfied. The input common-mode of the CLKIN input is not compatible with many common signaling standards like LVDS and LVPECL. Therefore, the CLKIN signal driver common-mode must be customized at the transmitter or adjusted along the interface. Figure 71 shows an example DC coupled interface that uses a resistor divider network to reduce the common-mode while maintaining a 100-Ω total termination at the load. Design equations are provided with example values to determine the resistor values.

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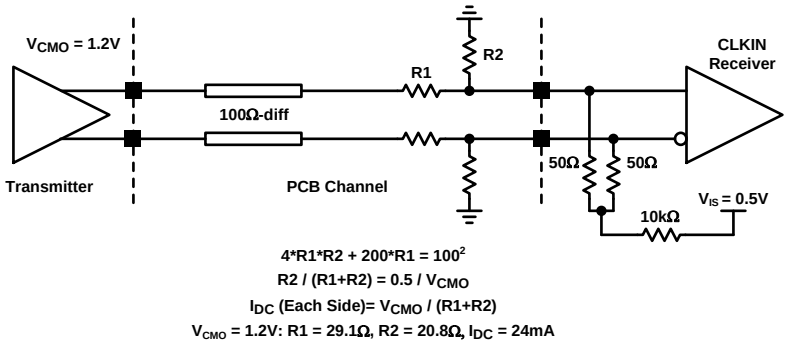

Figure 71. Driving the CLKIN Input With an Example DC Coupled Interface

The CLKIN input supports any type of standard signaling that meets the input signal swing and common-mode range requirements with an appropriate interface. Generic differential sinusoidal or square-wave clock signals are also supported. TI does not recommend driving the CLKIN input single-ended. The differential lane trace on the PCB should be designed to be a controlled 100 Ω and protected from noise sources or other interfering signals.

9.1.3.2 Driving the SYSREF Input

The SYSREF input interface circuit is composed of the differential receiver, internal termination, internal common-mode bias with common-mode control, and SYSREF detection feature.

A 100-Ω differential termination is provided inside the ADC pins. A high impedance reference biases the input common-mode through a resistor network that can be configured to support a wide range of input common modes voltages. Following the receiver, an AND gate provides a method for detecting or ignoring incoming SYSREF events.

The timing relationship between the CLKIN and SYSREF signal is very stringent in a JESD204B system. Therefore, the signal path network of the CLKIN and SYSREF signals must be as similar as possible to ensure that the signal relationship is maintained from the launch of the signal, through their respective channels to the CLKIN and SYSREF input receivers.

DC coupling of the SYSREF signal to the input pins with the simple interface shown in Figure 72 is required. Although the input common-mode range of the receiver itself is limited, a wide input common-mode range is supported using the common-mode control feature which level-shifts the common-mode of the input signal to an appropriate level for the input receiver. The common-mode control feature is configured via the SPI.

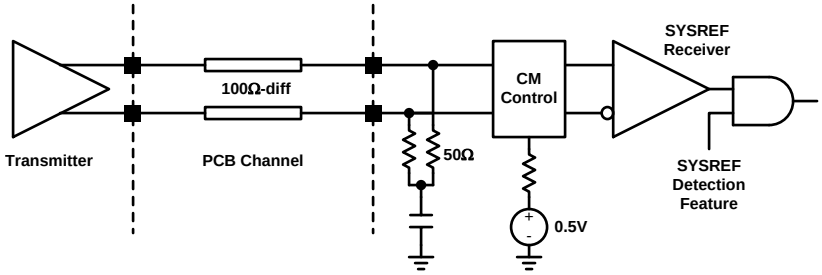

Figure 72. SYSREF Input Receiver and DC Coupled Interface

9.1.3.3 SYSREF Signaling

The SYSREF input may be driven by a number of different types of signals. The supported signal types, shown in Figure 73 (in single-ended form), include periodic, gapped periodic, and one-shot signals. The rising edge of the SYSREF signal is used as a reference to align the internal frame clock and local multi-frame clock (LMFC). To ensure proper alignment of these system clocks, the SYSREF signal must be generated along with the CLKIN signal such that the SYSREF rising edge meets the setup and hold requirements relative to the CLKIN at the ADC31JB68 device inputs.

For each rising clock edge that is detected at the SYSREF input, the ADC31JB68 device compares the current alignment of the internal frame and LMFC with the SYSREF edge and determines if the internal clocks must be re-aligned. In the case that no alignment is needed, the clocks maintain their current alignment and the JESD204B data link is not broken. In the case that re-alignment is needed, the JESD204B data link is broken and the clocks are re-aligned.

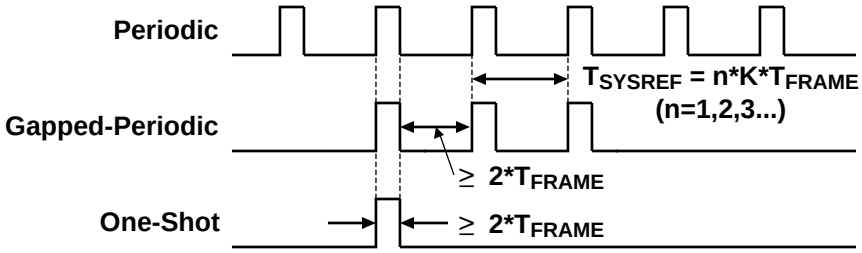

Figure 73. SYSREF Signal Types (Single-Ended Representations)

In the case of a periodic SYSREF signal, the frame and LMFC alignment is established at the first rising edge of SYSREF, and every subsequent rising edge (that properly meets setup and hold requirements) is ignored because the alignment has already been established. A periodic SYSREF must have a period equal to $n \times K / F_S$ where 'F_S' is the sampling rate, 'K' is the JESD204B configuration parameter indicating the number of frames per multi-frame, and 'n' is an integer of one or greater.

Gapped-period signals contain bursts of pulses. The frame and LMFC alignments are established on the first rising edge of the pulse burst. Any rising edge that does not abide by this rule or does not meet the setup and hold requirements forces re-alignment of the clocks.

A one-shot signal contains a single rising edge that establishes the frame and LMFC alignment.

For all types of SYSREF signals, the minimum pulse width is $2 \times T_{FRAME}$.

TI recommends gapped-periodic or one-shot signals for most applications because the SYSREF signal is not active during normal sampling operation. Periodic signals that toggle constantly introduce spurs into the signal spectrum that degrade the dynamic range of the system.

9.1.3.4 SYSREF Timing

The SYSREF timing requirements depend on whether deterministic latency of the JESD204B link is required.

If deterministic latency is required, then the SYSREF signal must meet setup and hold requirements relative to the CLKIN signal. In the case that the internal CLKIN divider is used and a very high-speed signal is provided to the CLKIN input, the SYSREF signal must meet setup and hold requirements relative to the very high-speed signal at the CLKIN input.

If deterministic latency is not required, then the SYSREF signal may be supplied as an asynchronous signal (possibly achieving < ± 2 frame clock cycles latency variation) or not provided at all (resulting in latency variation as large as the multi-frame period).

9.1.3.5 Effectively Using the Detection Gate Feature

TI recommends the use of the SYSREF detection gate for most applications. The gate is enabled when SYSREF is being transmitted and the gate is disabled before the SYSREF transmitter is put in the idle state.

Enabling the SYSREF gate immediately sends a logic signal to a logic block responsible for aligning the internal frame clock and LMFC. If the signal at the SYSREF input is logic high when the gate is enabled, then a "false" rising edge event causes a re-alignment of the internal clocks, despite the fact that the event is not an actual SYSREF rising edge. The SYSREF rising edge following the gate enable then causes a subsequent re-alignment with the desired alignment.

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9.1.3.6 Driving the SYNCb Input

The SYNCb input is part of the JESD204B interface and is used to send synchronization requests from the serial data receiver to the transmitter. The SYNCb signal, quantified as the (SYNCb+ – SYNCb–), is a differential active low signal. In the case of the ADC31JB68 device, a JESD204B subclass 1 device, a SYNCb assertion (logic low) indicates a request for synchronization by the receiver. The SYNCb input is an asynchronous input and does not have sub-clock-cycle setup and hold requirements relative to the CLKIN or any other input to the ADC31JB68 device.

The SYNCb input is a differential receiver as shown in Figure 74. Resistors provide an internal 100-Ω differential termination as well as a voltage divider circuit that gives the SYNCb receiver a wide input common-mode range. The SYNCb signal must be DC coupled from the driver to the SYNCb inputs; therefore, the wide common-mode range allows the use of many different logic standards including LVDS and LVPECL. No additional external components are needed for the SYNCb signal path as shown in the interface circuit of Figure 74, but providing an electrical probing site is recommended for system debug.

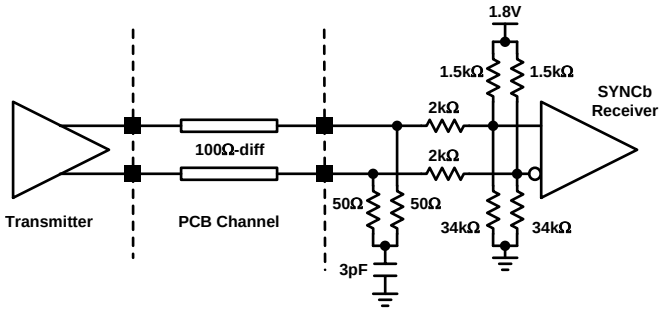

Figure 74. SYNCb Input Receiver and Interface

9.1.4 Output Serial Interface Considerations

9.1.4.1 Output Serial-Lane Interface

The output high speed serial lanes must be AC coupled to the receiving device with 0.01-µF capacitors as shown in Figure 75. DC coupling to the receiving device is not supported. The lane channel on the PCB must be a 100-Ω differential transmission line with dominant coupling recommended between the differential traces instead of to adjacent layers. The lane must terminate at a 100-Ω termination inside the receiving device. Avoid changing the direction of the channel traces abruptly at angles larger than 45°.

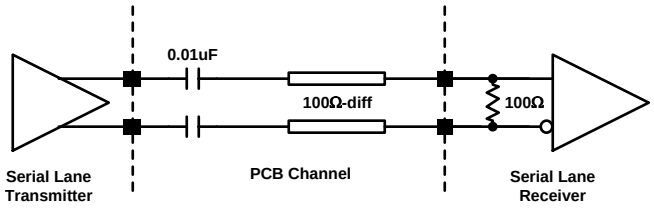

Figure 75. High-Speed Serial-Lane Interface

The recommended spacing between serial lanes is 3× the differential line spacing or greater. High speed serial lanes should be routed on top of or below adjacent, quiet ground planes to provide shielding. TI recommends that other high speed signal traces do not cross the serial lanes on adjacent PCB layers. If absolutely necessary, crossing should occur at a 90° angle with the trajectory of the serial lane to minimize coupling.

The integrity of the data transfer from the transmitter to receiver is limited by the accuracy of the lane impedance and the attenuation as the signal travels down the lane. Inaccurate or varying impedance and frequency dependent attenuation results in increased ISI (part of deterministic jitter) and reduced signal-to-noise ratio, which limits the ability of the receiver to accurately recover the data.

Two features are provided in the ADC31JB68 device serial transmitters to compensate attenuation and ISI caused by the serial lane: voltage swing control (VOD) and de-emphasis (DEM).

9.1.4.2 Voltage Swing and De-Emphasis Optimization

Voltage swing control (VOD) compensates for attenuation across all frequencies through the channel at the expense of power consumption. Increasing the voltage swing increases the power consumption. De-emphasis (DEM) compensates for the frequency dependent attenuation of the channel but results in attenuation at lower frequencies. The voltage swing control and de-emphasis feature may be used together to optimally compensate for attenuation effects of the channel.

The frequency response of the PCB channel is typically lowpass with more attenuation occurring at higher frequencies. The de-emphasis implemented in the ADC31JB68 device is a form of linear, continuous-time equalization that shapes the signal at the transmitter into a high-pass response to counteract the low-pass response of the channel. The de-emphasis setting should be selected such that the equalizer's frequency response is the inverse of the channel's response. Therefore, transferring data at the highest speeds over long channel lengths requires knowledge of the channel characteristics.

Optimization of the de-emphasis and voltage swing settings is only necessary if the ISI and losses caused by the channel are too great for reception at the desired bit rate. Many applications will perform with an adequate BER using the default settings.

9.1.4.3 Minimizing EMI

High data-transfer rates have the potential to emit radiation. EMI may be minimized using the following techniques:

- Use differential stripline channels on inner layer sandwiched between ground layers instead of routing microstrip pairs on the top layer.
- Avoid routing lanes near the edges of boards.
- Enable data scrambling to spread the frequency content of the transmitted data.
- If the serial lane must travel through an interconnect, choose a connector with good differential pair channels and shielding.
- Ensure lanes are designed with an accurate, 100-Ω characteristic impedance and provide accurate 100-Ω terminations inside the receiving device.

9.1.5 JESD204B System Considerations

9.1.5.1 Frame and LMFC Clock Alignment Procedure

Frame and LMFC clocks are generated inside the ADC31JB68 device and are used to properly align the phase of the serial data leaving the device. The phases of the frame and multi-frame clocks are determined by the frame alignment step for JESD204B link initialization as shown in Figure 35. These clocks are not accessible outside the device. The frequencies of the frame and LMFC must be equal to the frame and LMFC of the device receiving the serial data.

When the ADC31JB68 device is powered-up, the internal frame and local multi-frame clocks initially assume a default phase alignment. To ensure determinist latency through the JESD204B link, the frame and LMFC clocks of the ADC31JB68 device must be aligned in the system. Perform the following steps to align the device clocks:

1. Enable the SYSREF signal driver. See *SYSREF Signaling* for more information.
2. Enable detection of the SYSREF signal at the ADC31JB68 device by enabling the SYSREF detection gate. See *Effectively Using the Detection Gate Feature* for more information.
3. Apply the desired SYSREF signal at the ADC31JB68 device SYSREF input.
4. Disable detection of the SYSREF signal by disabling the SYSREF gate.
5. Configure the SYSREF driver into its idle state.

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9.1.5.2 Link Interruption

The internal frame and multi-frame clocks must be stable to maintain the JESD204B link. The ADC31JB68 is designed to maintain the JESD204B link in most conditions but some features interrupt the internal clocks and break the link.

The following actions cause a break in the JESD204B link:

- The ADC31JB68 device is configured into power-down mode or sleep mode
- The ADC31JB68 device CLKIN clock divider setting is changed
- The serial data receiver performs a synchronization request
- The ADC31JB68 device detects a SYSREF assertion that is not aligned with the internal frame or multi-frame clocks
- The CLKIN input is interrupted
- Power to the device is interrupted

The following actions do not cause a change in clock alignment nor break the JESD204B link:

- The ambient temperature or operating voltages are varied across the ranges specified in the normal operating conditions.
- The ADC31JB68 device detects a SYSREF assertion that is aligned with the internal frame and multi-frame clocks.

9.1.5.3 Clock Configuration Examples

The features provided in the ADC31JB68 device allow for a number of clock and JESD204B link configurations. These examples in Table 27 show some common implementations and may be used as a starting point for a more customized implementation.

Table 27. Example ADC31JB68 Clock Configurations

Parameter	Example 1	Example 2	Example 3
CLKIN frequency	500 MHz	1000 MHz	1966.08 MHz
CLKIN divider	1	2	4
Sampling rate	500 MSPS	500 MSPS	491.52 MSPS
K (Frames per multi-frame)	20	32	32
LMFC Frequency	25 MHz	15.625 MHz	15.36 MHz
SYSREF Frequency(1)	25 MHz	11.5625 MHz	7.68 MHz(1)
Serial bit rate for each lane	5.0 Gb/s	5.0 Gb/s	4.9152 Gb/s

(1) The SYSREF frequency for a continuous SYSREF signal can be the indicated frequency f_{LMFC} or integer sub-harmonic such as f_{LMFC} / 2, f_{LMFC} / 3, and so forth. Gapped-periodic SYSREF signals should have pulses spaced by the associated periods 1 / f_{LMFC}, 2 / f_{LMFC}, 3 / f_{LMFC}, and so forth.

9.1.6 SPI

Figure 76 demonstrates a typical circuit to interface the ADC31JB68 device to a SPI master using a shared SPI bus. The 4-wire interface (SCLK, SDI, SDO, CSb) is compatible with 1.2-, 1.8-, or 3.0-V logic. The input pins (SCLK, SDI, CSb) use thick-oxide devices to tolerate 3.0-V logic although the input threshold levels are relative to 1.2-V logic. A low-capacitance protection diode may also be added with the anode connected to the SDO output and the cathode connected to the desired voltage supply to prevent an accidental pre-configured read command from causing damage.

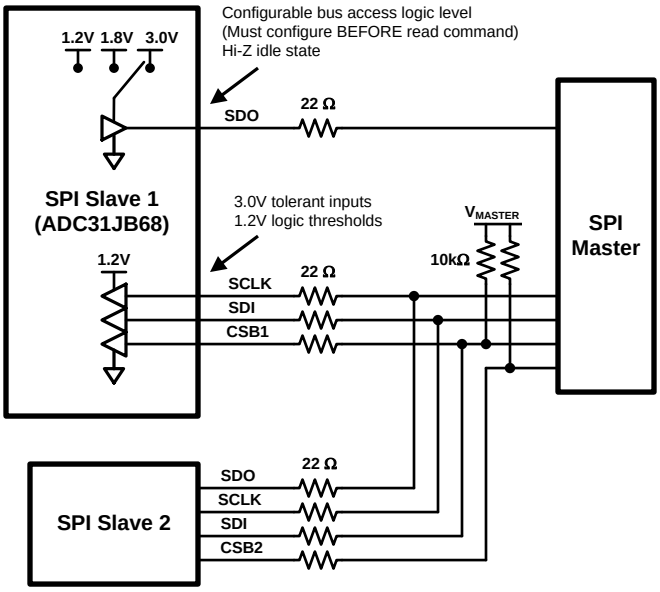

Figure 76. Typical SPI Application

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9.2 Typical Application

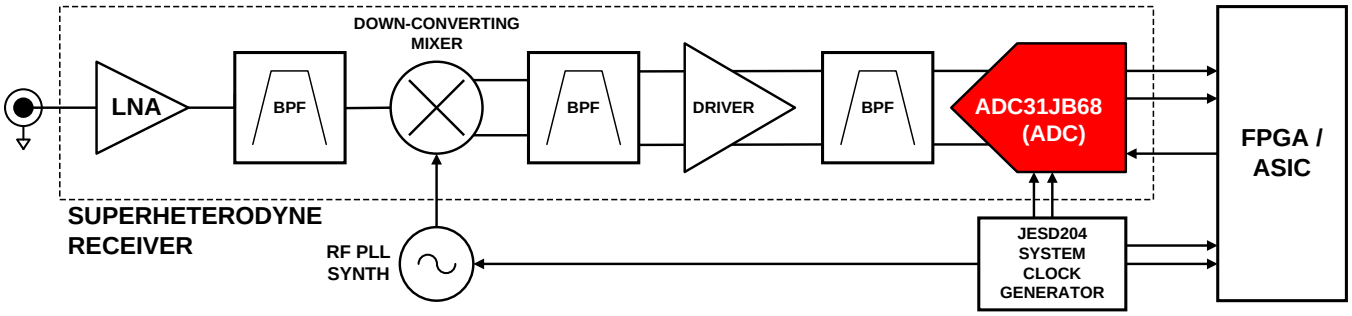

Figure 77. Typical Application Circuit

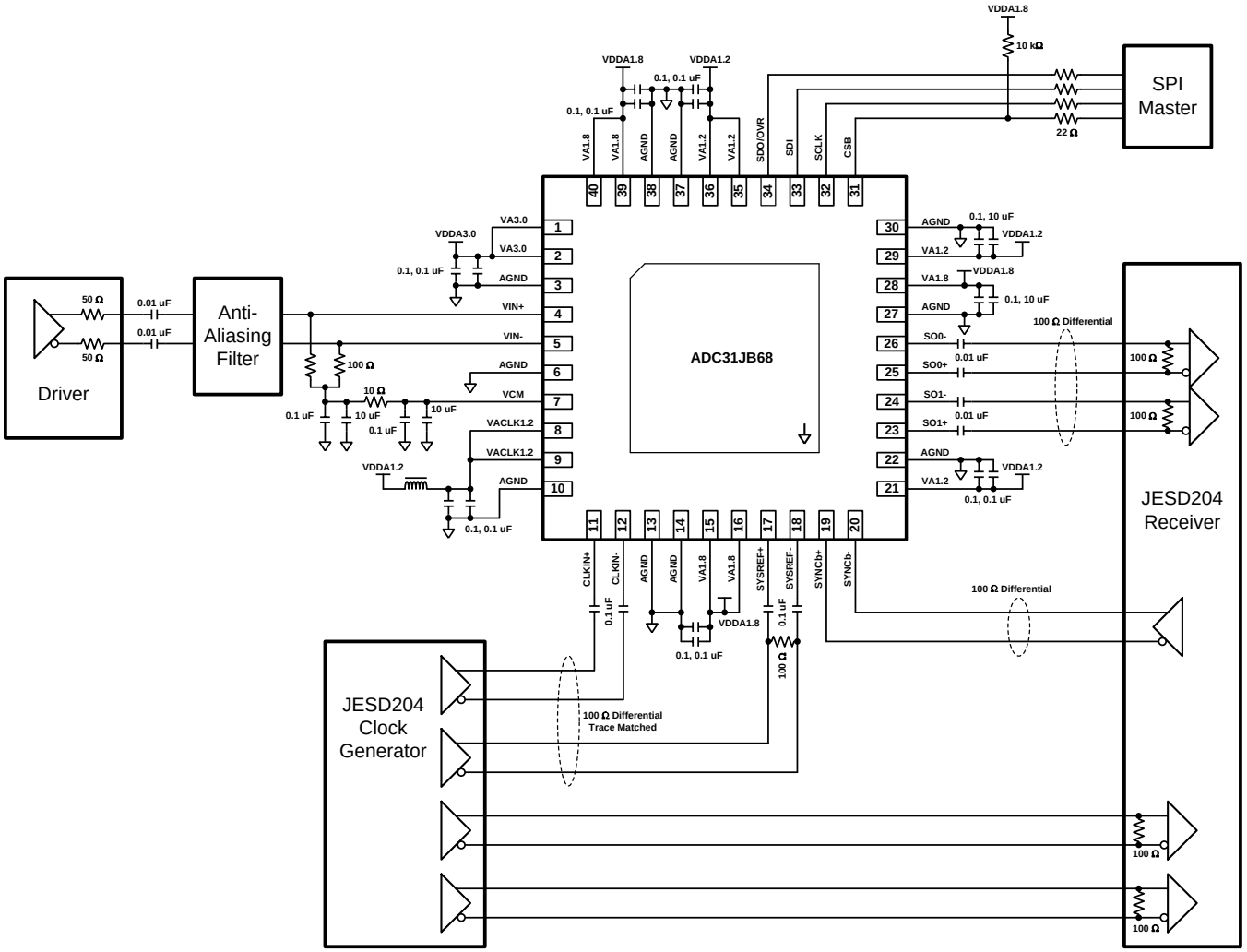

Figure 78. Typical Circuit Implementation

Typical Application (continued)

9.2.1 Design Requirements

The following are example design requirements expected of the ADC in a typical high-IF, 200-MHz bandwidth receiver, and are met by the ADC31JB68 device:

Table 28. Example Design Requirements for a High-IF Application

Specification	Example Design Requirement(1)	ADC31JB68 Capability
Sampling rate	> 450 MSPS to allow 200 MHz unaliased bandwidth	Up to 500 MSPS
Input bandwidth	> 500-MHz, 1 dB flatness	1000 MHz, 1 dB Bandwidth
Full-scale range	< 2 Vpp-diff	1.7 Vpp-diff
Small signal noise spectral density	< –152 dBFS/Hz	–154.5 dBFS/Hz
Large-signal SNR	> 69 dBFS for a –1 dBFS, 210 MHz Input	69.7 dBFS for a –1 dBFS, 210 MHz Input
SFDR	> 75 dBFS for a –1 dBFS, 210 MHz input	79 dBFS for a –1 dBFS, 210 MHz input
HD2, HD3	< –75 dBFS for a –1 dBFS, 210 MHz input	–79 dBFS for a –1 dBFS, 210 MHz input
Next largest SPUR	< –88 dBFS for a –1 dBFS, 210 MHz input	–90 dBFS for a –1 dBFS, 210 MHz input
Over-range detection	Included	Fast over-range detection on SDO/OVR pin
Digital interface	JESD204B interface, 2 lane/channel	JESD204B subclass 1 interface, 2 lane/channel, 5.0 Gb/s bit rate
Configuration interface	SPI configuration, 4-wire, 1.8 V logic, SCLK > 1 MHz	SPI configuration, 4-Wire, 1.8 V Logic, SCLK up to 20 MHz
Package size	< 10 × 10 × 1 mm	6 × 6 × 0.8 mm

(1) These example design requirements do not represent the capabilities of the ADC31JB68, rather the requirements are satisfied by the ADC31JB68.

9.2.2 Design Procedure

The following procedure can be followed to design the ADC31JB68 device into most applications:

- Choose an appropriate ADC driver and analog input interface.
  - Optimize the signal chain gain leading up to the ADC to make use of the full ADC dynamic range.
  - Identify whether DC or AC coupling is required.
  - Determine the desired analog input interface, such as a bandpass filter or a transformer.
  - Use the provided input network models to design and verify the interface.
  - Refer to the interface recommendations in *Analog Input Considerations*.
- Determine the core sampling rate of the ADC.
  - Must satisfy the bandwidth requirements of the application .
  - Must also provide enough margin to prevent aliasing or to accommodate the transitions bands of an anti-aliasing filter.
  - Ensure the application initialization sequence properly handles ADC core calibration as described in *ADC Core Calibration*.
- Determine the system latency requirements.
  - Total allowable latency through the ADC and JESD204B link.
  - Is the system tolerant of latency variation over time or conditions or between power cycles?
- Determine the desired JESD204B link configuration as discussed in *JESD204B Supported Features*.
  - Based on the system latency requirements, determine whether deterministic latency is required across the JESD204B link.
  - Choose the number of frames per multi-frame, K.
  - Choose whether scrambling is desired.
- Choose an appropriate clock generator, CLKIN interface, and SYSREF interface.
  - Determine the system clock distribution scheme and the clock frequencies for the CLKIN and SYSREF inputs.
  - Determine the allowable amount of sampling clock phase noise in the system and then select a CLKIN

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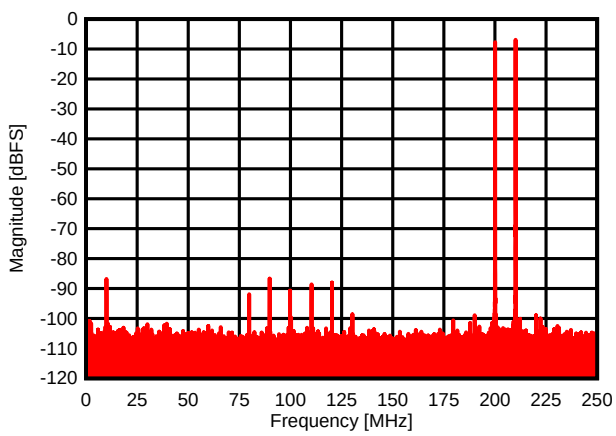
edge rate that satisfies this requirement as discussed in *Internal Noise Sources*.
  - Choose an appropriate CLKIN interface as discussed in *Driving the CLKIN+ and CLKIN– Input*.
  - Based on the latency requirements, determine whether SYSREF must meet setup and hold requirements relative to CLKIN.
  - Choose the SYSREF signal type as discussed in *SYSREF Signaling*.
  - Choose an appropriate SYSREF interface as discussed in *Driving the SYSREF Input*.
  - Choose a CLKIN and SYSREF clock generator based on the above requirements. The signals must come from the same generator in many cases.
- Design the SYNCb interface as discussed in *Driving the SYNCb Input*.
- Choose appropriate configurations for the output serial data interface.
  - Design the serial lane interface according to *Output Serial-Lane Interface*.
  - Choose the required PCB materials, keeping in mind the desired rate of the serial lanes.
  - Characterize the signal lane channels that connect the ADC serial output transmitters to the receiving device either through simulation or bench characterization.
  - Optimize the VOD and DEM parameters to achieve the required signal integrity according to *Voltage Swing and De-Emphasis Optimization*.
- Design the SPI bus interface.
  - Verify the electrical and functional compatibility of the ADC SPI with the SPI controller.
  - Interface the ADC to the SPI bus according to *SPI*.
  - Ensure that the application initialization sequence properly configures the output SDO voltage before the first read command.
- Design the power supply architecture and de-coupling.
  - Choose appropriate power supply and supply filtering devices to provide stable, low-noise supplies as described in *Power Supply Recommendations*.
  - Design the capacitive de-coupling around the ADC, also described in *Power Supply Recommendations*, while paying close attention to placing the capacitors as close to the device as possible.
  - Time the power architecture to satisfy the power sequence requirements described in *Power Supply Design*.
- Ensure that the application initialization sequence satisfies the JESD204B link initialization requirements described in *JESD204B Link Initialization*.
- Refer to Figure 78 for an example hardware design.

9.2.3 Application Curve



f1 = 200 MHz; f2 = 210 MHz, Input Amplitude = –7 dBFS/Tone

Figure 79. Output Spectrum, 2-Tone Test

10 Power Supply Recommendations

10.1 Power Supply Design

The ADC31JB68 device is a very-high dynamic range device, and therefore requires very-low noise power supplies. LDO-type regulators, capacitive decoupling, and series isolation devices like ferrite beads are all recommended.

LDO-type, low-noise regulators should be used to generate the 1.2-V, 1.8-V, and 3.0-V supplies used by the device. To improve power efficiency, a switching-type regulator may precede the LDO to efficiently drop a supply to an intermediate voltage that satisfies the drop-out requirements of the LDO. The recommended supply path includes a switching-type regulator followed by an LDO to provide an efficient and low noise source. Additional ferrite beads and LC filters may be used to further suppress noise. Supplying power to multiple devices in a system from one regulator may result in noise coupling between the multiple devices; therefore, series isolation devices and additional capacitive decoupling is recommended to improve the isolation. VACLK1.2, a sensitive supply that powers the internal clock path, can be sourced by the same regulator as the VA1.2 supply, but the VACLK1.2 supply should be isolated using a ferrite device.

The power supplies must be applied to the ADC31JB68 device in this specific sequence:

1. VA3.0
2. VA1.8 and VA1.2 and VACLK1.2

First, apply the VA3.0 (+3.0 V) to provide the bias for the ESD diodes. Next, within 1 ms after enabling the VA3.0 supply, apply the VA1.8 (+1.8-V) and VA1.2 (+1.2-V) and VACLK1.2 (+1.2-V) supplies. Use the reverse order to turn off the power supplies off.

10.2 Decoupling

Decoupling capacitors must be used at each supply pin to prevent supply or ground noise from degrading the dynamic performance of the ADC and to provide the ADC with a well of charge to minimize voltage ripple caused by current transients. The recommended supply decoupling scheme is to have a ceramic X7R 0201 0.1-μF and a X7R 0402 0.1-μF capacitor at each supply pin. The 0201 capacitor must be placed on the same layer as the device as close to the pin as possible to minimize the AC decoupling path length from the supply pin, through the capacitor, to the nearest adjacent ground pin. The 0402 capacitor should also be close to the pins. TI does not recommend placing all capacitors on the opposite board side. Each voltage supply should also have a single 10-μF decoupling capacitor near the device but the proximity to the supply pins is less critical.

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11 Layout

11.1 Layout Guidelines

The design of the PCB is critical to achieve the full performance of the ADC31JB68 device. Defining the PCB stackup should be the first step in the board design. Experience has shown that at least 6 layers are required to adequately route all required signals to and from the device. Each signal routing layer must have an adjacent solid ground plane to control signal return paths to have minimal loop areas and to achieve controlled impedances for microstrip and stripline routing. Power planes must also have adjacent solid ground planes to control supply return paths. Minimizing the spacing between supply and ground planes improves performance by increasing the distributed decoupling. A recommended stack-up for a 6-layer board design is shown in Figure 80.

Although the ADC31JB68 device consists of both analog and digital circuitry, TI highly recommends solid ground planes that encompass the device and its input and output signal paths. TI does not recommend split ground planes that divide the analog and digital portions of the device. Split ground planes may improve performance if a nearby, noisy, digital device is corrupting the ground reference of the analog signal path. When split ground planes are employed, one must carefully control the supply return paths and keep the paths on top of their respective reference planes.

Quality analog input signal and clock signal path layout is required for full dynamic performance. Symmetry of the differential signal paths and discrete components in the path is mandatory and symmetrical shunt-oriented components should have a common grounding via. The high frequency requirements of the input and clock signal paths necessitate using differential routing with controlled impedances and minimizing signal path stubs (including vias) when possible.

Coupling onto or between the clock and input signal paths must be avoided using any isolation techniques available including distance isolation, orientation planning to prevent field coupling of components like inductors and transformers, and providing well coupled reference planes. Via stitching around the clock signal path and the input analog signal path provides a quiet ground reference for the critical signal paths and reduces noise coupling onto these paths. Sensitive signal traces must not cross other signal traces or power routing on adjacent PCB layers, rather a ground plane should separate the traces. If necessary, the traces should cross at 90° angles to minimize crosstalk.

The substrate dielectric materials of the PCB are largely influenced by the speed and length of the high speed serial lanes. The affordable and common FR4 variety may not offer the consistency or low loss to support the highest speed transmission (5 Gb/s) and long lengths (> 8 inch). Although the VOD and DEM features are available to improve the signal integrity of the serial lanes, some of the highest performing applications may still require special dielectric materials.

Coupling of ambient signals into the signal path is reduced by providing quiet, close reference planes and by maintaining signal path symmetry to ensure the coupled noise is common-mode. Faraday caging may be used in very noisy environments and high dynamic range applications to isolate the signal path.

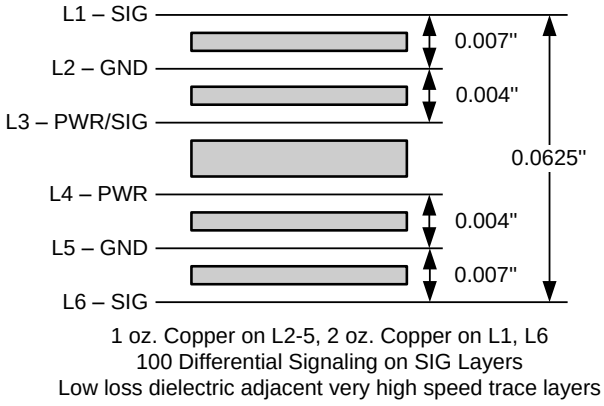

Figure 80. Recommended PCB Layer Stack-Up for a Six-Layer Board

11.2 Layout Example

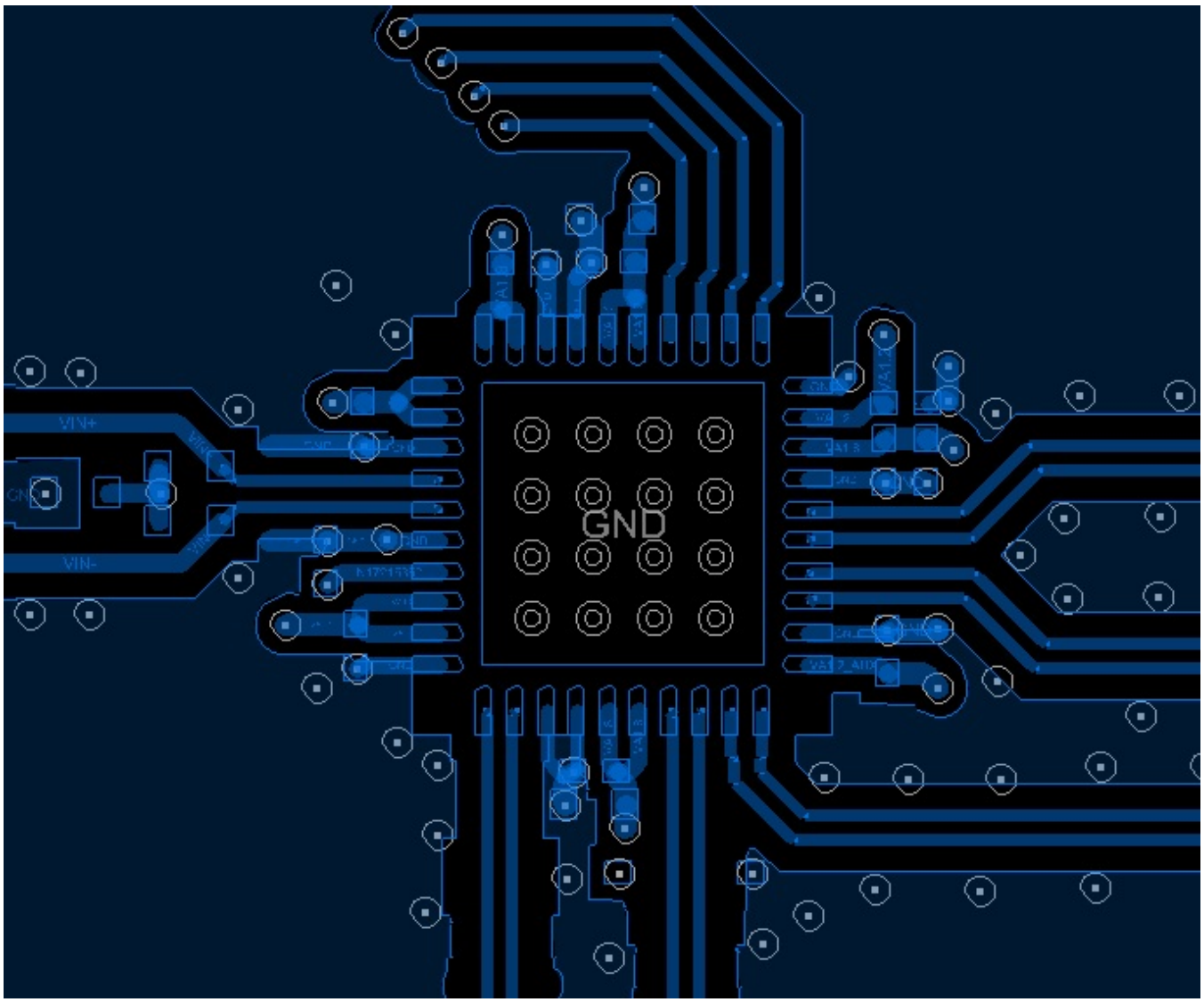

Figure 81. Layout

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12 Device and Documentation Support

12.1 Related Documentation

For related documentation see the following: *ADC31JB68EVM User's Guide*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC31JB68RTAT	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	31JB68
ADC31JB68RTAT.A	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	31JB68

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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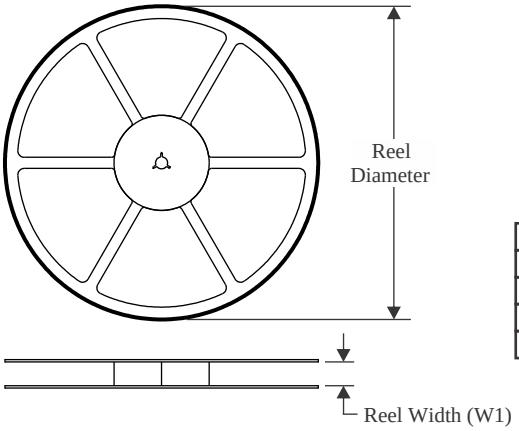
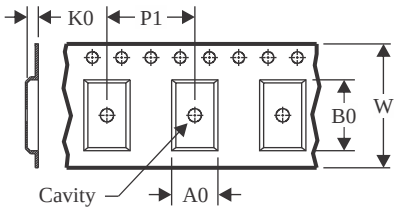
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

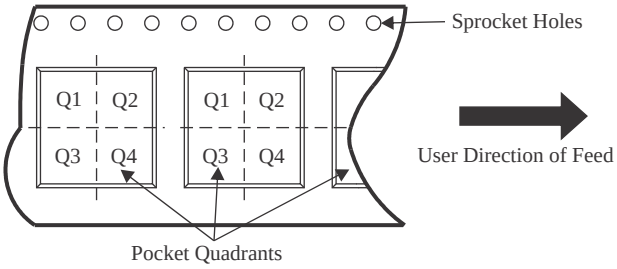


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

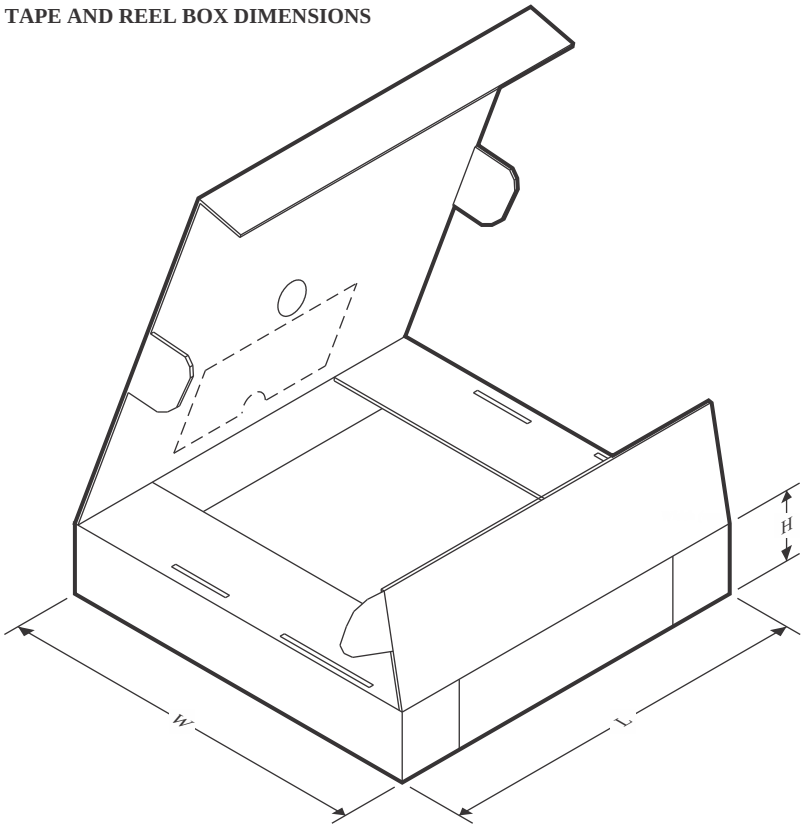
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC31JB68RTAT	WQFN	RTA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

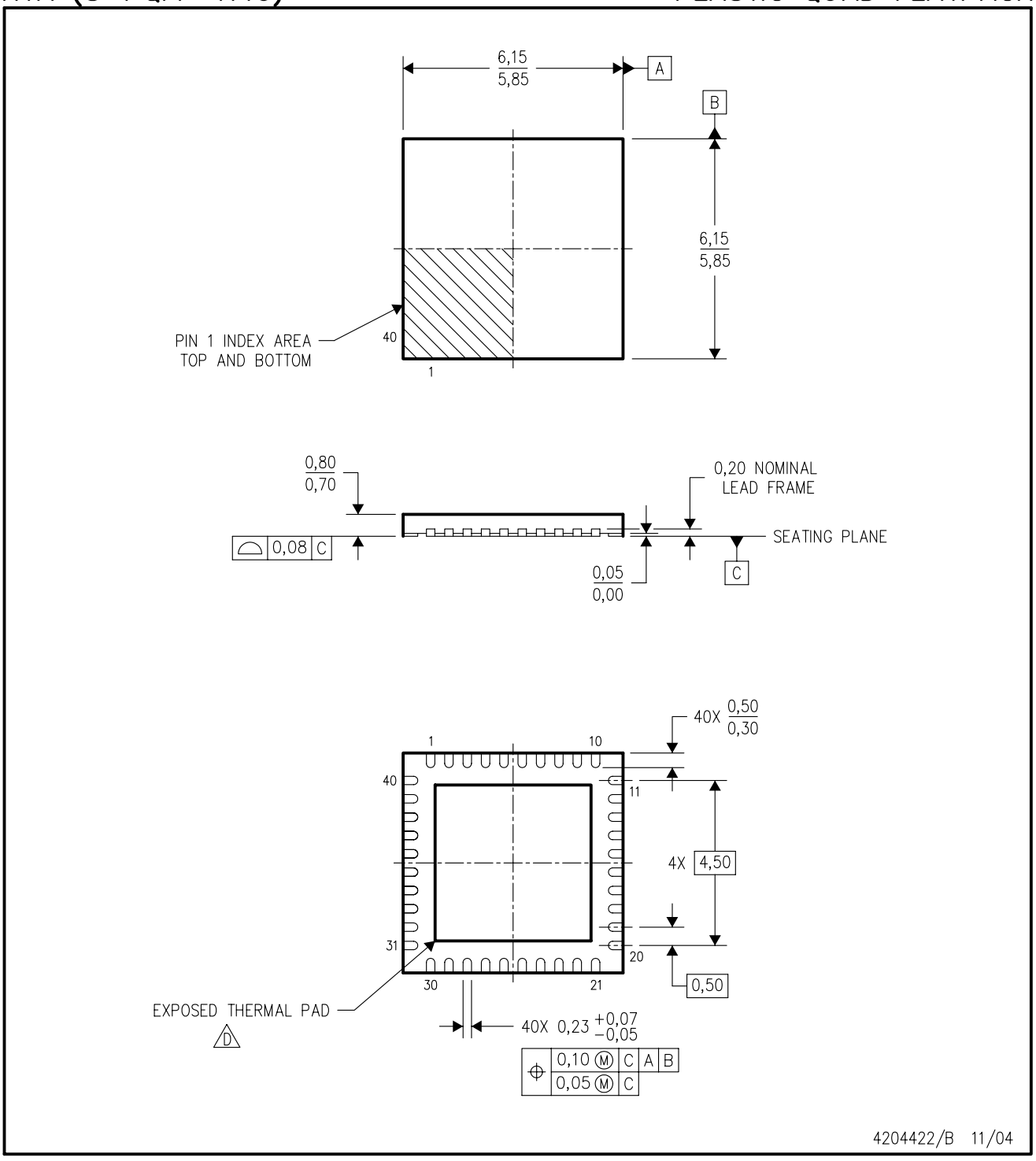
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC31JB68RTAT	WQFN	RTA	40	250	208.0	191.0	35.0

RTA (S–PQFP–N40) PLASTIC QUAD FLATPACK



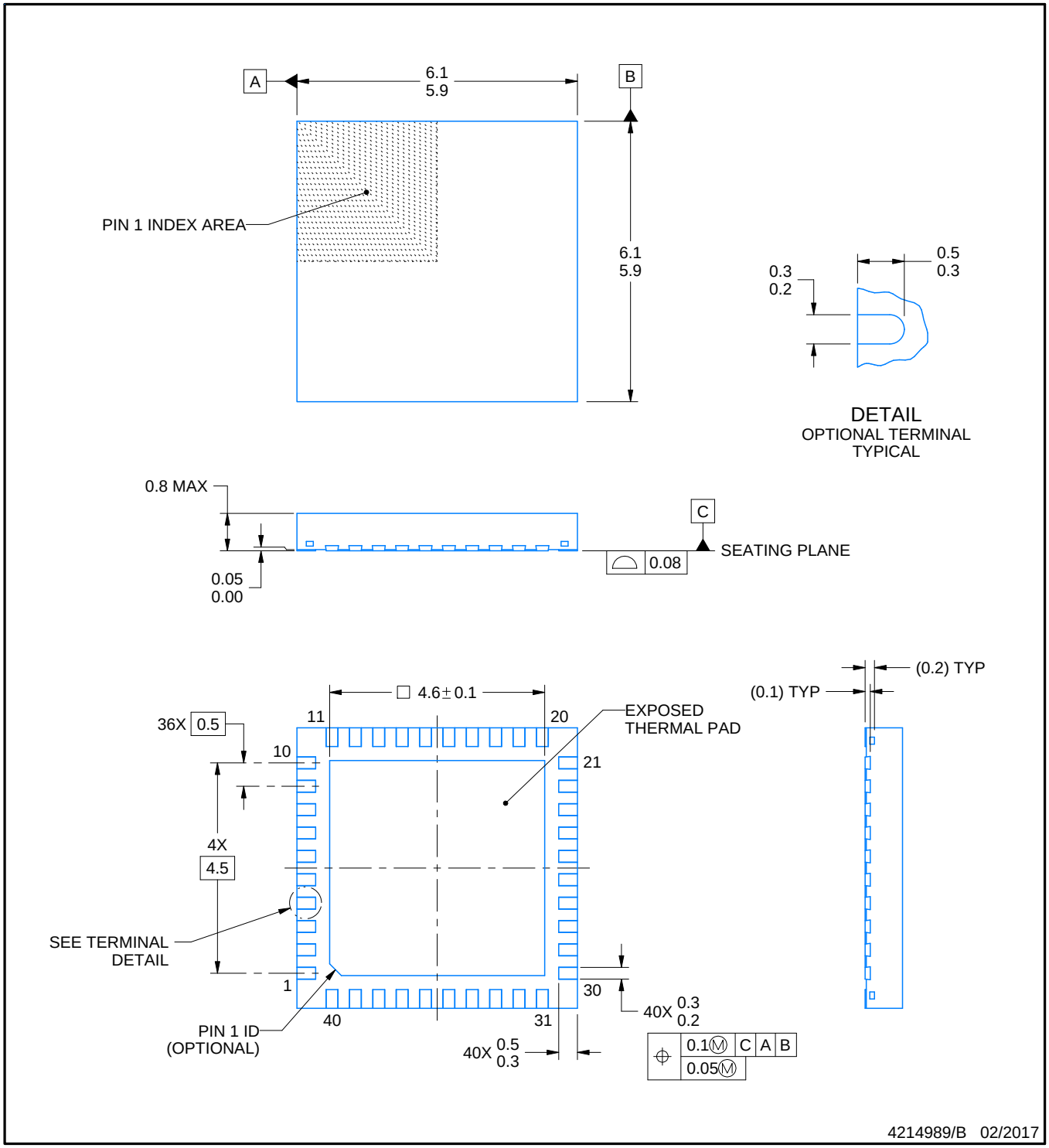
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

PACKAGE OUTLINE

RTA0040A

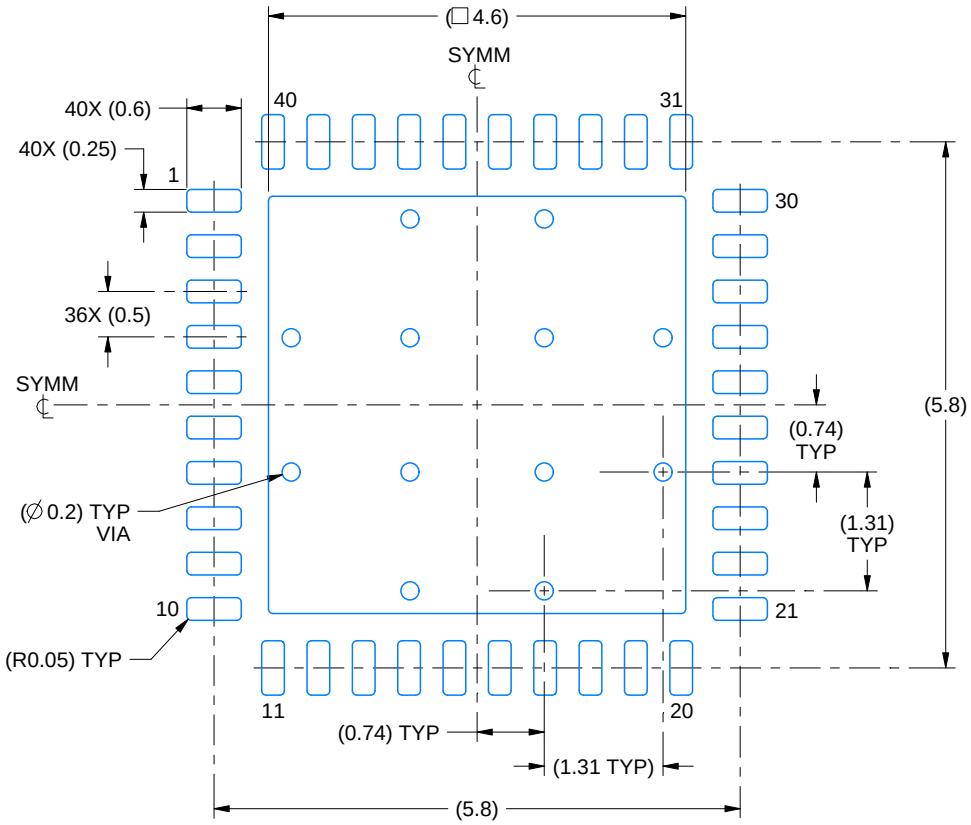
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

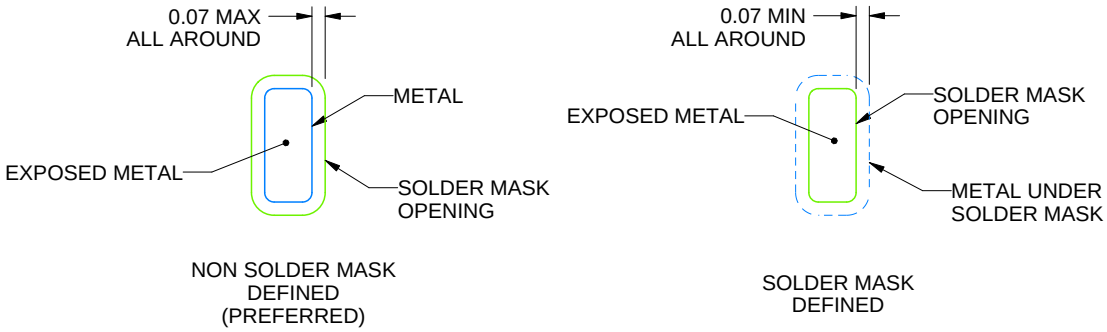


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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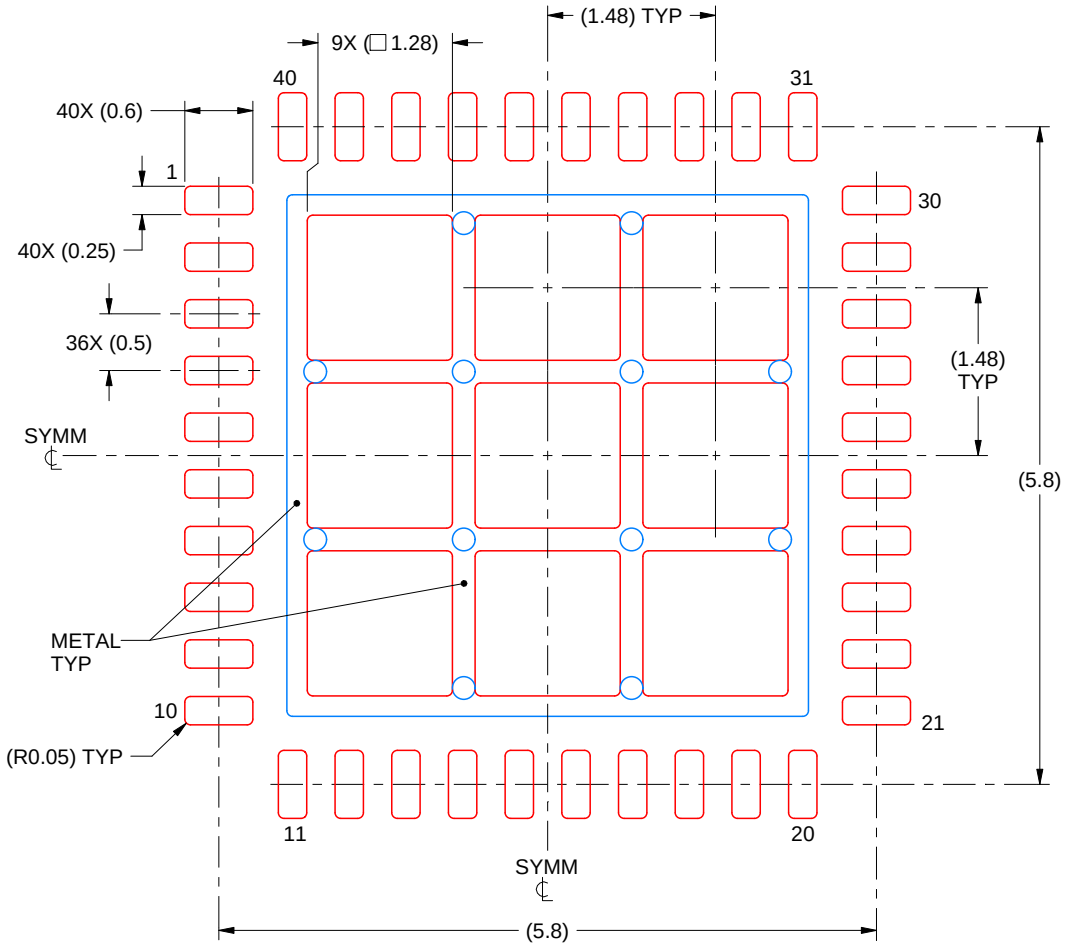
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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