LP8557 High-Efficiency LED Backlight Driver For Tablets

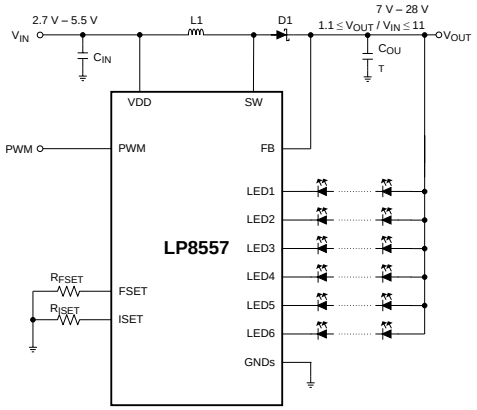
1 Features

- High-Efficiency DC-DC Boost Converter With 28-V Integrated Power MOSFET
- 2.7-V to 5.5-V VDD Range for Supporting Single-Cell Li-Ion Battery Applications
- Six 25-mA High-Precision LED Current Sinks
- Adaptive Boost Voltage and LED Current Sink Headroom Controls for Maximum System Efficiency
- LED String Count Auto-Detect for Maximum Design Flexibility
- Smart Phase Shift PWM Mode for Reduced Audible Noise
- PWM Input Duty Cycle Brightness Control, PWM Output Frequency Selectable Independent of Input Frequency
- Hybrid PWM Plus Current Dimming for Higher LED Drive Optical Efficiency
- Switching Frequency, PWM Output Frequency, and LED Current can be set Through Resistors or I^2C Interface
- Programmable Boost SW Slew Rate Control and Spread Spectrum Scheme for Reduced Switching Noise and Improved EMI Performance
- UVLO, TSD, BST_OVP, BST_OCP, BST_UV, LED OPEN* and LED Short Fault Coverage
- Minimum Number of External Components

2 Applications

Tablet LCD Display LED Backlight

Simplified Schematic With PWM-Only Option



3 Description

The LP8557 and LP8557I are high-efficiency LED drivers each featuring an integrated DC-DC inductive boost converter and six high-precision current sinks. LP8557 is intended for applications that exclusively use a pulse width modulated (PWM) signal for controlling the brightness while LP8557I is intended for applications that can utilize an I^2C master as well.

The boost converter has adaptive output voltage control. This feature minimizes the power consumption by adjusting the voltage to the lowest sufficient level under all conditions.

The adaptive current sink headroom voltage control scales the headroom voltage with the LED current for optimal system efficiency.

The LED string auto-detect function enables use of the same device in systems with 1 to 6 LED strings for the maximum design flexibility.

Proprietary hybrid PWM plus current mode dimming enables additional system power savings. Phase-shift PWM allows reduced audible noise and smaller boost output capacitors.

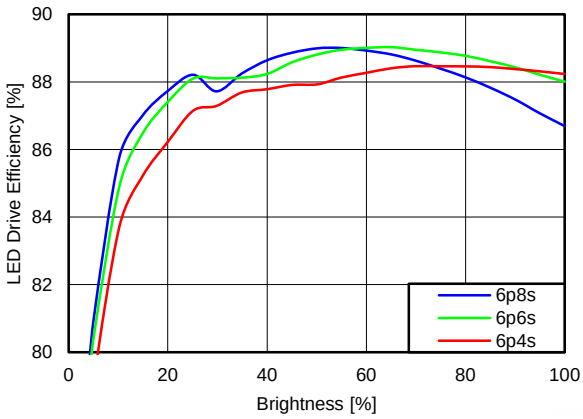
Flexible CABC support combines brightness level selections based on the PWM input and I^2C commands.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LP8557	DSBGA (16)	1.906 mm x 1.64 mm
LP8557I		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

LED Efficiency With 6 LED Strings



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (June 2014) to Revision B — **Page**

- moved storage temperature range to *Abs Max* table ... 4
- Changed *Handling Ratings* table to *ESD Ratings* table ... 4
- Updated *Thermal Information* table ... 4
- Changed word "safety" to "fault detection" ... 11
- Deleted "to 25% of the brightness range" ... 16
- Changed PGEN register table and descriptions ... 28
- Changed fixed typo "2.4.4 kHz" to "24.4 kHz" ... 28
- Added note to beginning of *Application and Implementation* section ... 31
- Added *Community Resources* section ... 43

Changes from Original (December 2013) to Revision A — **Page**

- Changed formatting to match new TI datasheet guidelines; added *Device Information* and *Handling Ratings* table, *Layout*, and *Device and Documentation Support* sections; reformatted *Detailed Description* and *Application and Implementation* sections, fix typographical errors. ... 1
- Changed 6 LED strings to 5 LED Strings to correct typo ... 8
- Added PWM Input Duty Measurement subsection ... 13
- Changed description for "0" BFSET as well as description of register table for BFSET bit ... 29

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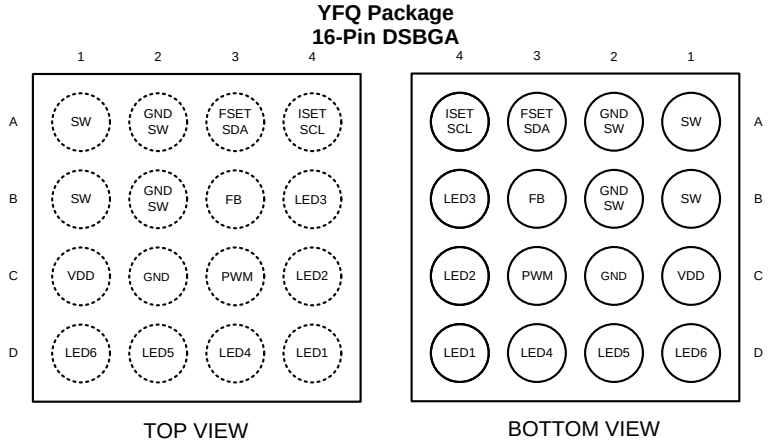
5 Device Comparison Table

ORDERABLE DEVICE	DEVICE OPTION	PACKAGE TOP MARK	PACKAGE TYPE (DRAWING)	PINS	PACKAGE QTY.
LP8557AYFQT	"PWM Only" - Recommended for systems without an I^2C master	D40	DSBGA (YFQ)	16	250
LP8557AYFQR					3000
LP8557IAYFQT	"PWM and I^2C" - Recommended for systems with an I^2C master	D41			250
LP8557IAYFQR					3000

6 Pin Function and Configurations

YFQ Package
16-Pin DSBGA



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
FB	B3	A	Boost feedback pin. The FB and OVP circuitry monitors the voltage on this pin.
FSET/SDA	A3	I/O	Dual function pin. When I^2C is not used (for example, BRTMODE = 00b), this pin can be used to set f_{SW} and/or f_{PWM} by connecting a resistor from this pin to a ground reference. When I^2C is used (for example, BRTMODE = 01, 10 or 11), connect this pin to an SDA line of an I^2C bus. The LP8557 "PWM Only" device option uses this pin as an FSET pin. LP8557I "PWM and I^2C" device option uses this pin as an SDA pin.
GND	C2	G	Ground pin.
ISET/SCL	A4	I	Dual function pin. When I^2C is not used (for example, BRTMODE = 00b), this pin can be used to set the full-scale LED current by connecting a resistor from the pin to a ground reference. When I^2C is used (for example, BRTMODE =01, 10, or 11), connect this pin to an SCL line of an I^2C bus. The LP8557 "PWM Only" device option uses this pin as an ISET pin. LP8557I "PWM and I^2C" device option uses this pin as an SCL pin.
LED1	D4	A	LED driver – current sink terminal. If unused, this pin may be left floating.
LED2	C4	A	LED driver – current sink terminal. If unused, this pin may be left floating.
LED3	B4	A	LED driver – current sink terminal. If unused, this pin may be left floating.
LED4	D3	A	LED driver – current sink terminal. If unused, this pin may be left floating.
LED5	D2	A	LED driver – current sink terminal. If unused, this pin may be left floating.
LED6	D1	A	LED driver – current sink terminal. If unused, this pin may be left floating.
PWM	C3	I	PWM input pin.
SW	A1, B1	A	A connection to the drain terminal of the integrated power MOSFET.
SW_GND	A2, B2	G	A connection to the source terminal of the integrated power MOSFET.
VDD	C1	P	Device power supply pin.

(1) A: Analog Pin, G: Ground Pin, P: Power Pin, I: Digital Input Pin, I/O: Digital Input/Output Pin

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) [(1)(2)]

		MIN	MAX	UNIT
V_{DD}	Voltage range on VDD pin	–0.3	6	V
V_{IO}	Voltage range on digital IO pins	–0.3	6	V
V_O	Voltage range on SW, FB, LED1 to LED6 pins	–0.3	31	V
T_J	Junction temperature	–30	125	°C
T_{sldr}	Maximum lead temperature (soldering)		260	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the potential at the GND pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted) [(1)(2)]

	MIN	MAX	UNIT
V_{DD}	2.7	5.5	V
V (SW, FB, LED1 to LED6)	0	28	V
Ambient temperature, T_A	–30	85	°C
Junction temperature, T_J	–30	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) All voltage values are with respect to the potential at the GND pin.

7.4 Thermal Information

THERMAL METRIC [(1)(2)]		LP8557/LP8557I YFQ (DSBGA) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

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7.5 Electrical Characteristics

Unless otherwise specified: T_A = 25°C, V_{DD} = 3.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input voltage range		2.7		5.5	V
I_{DDQ}	Standby current				1	µA
I_{DD}	Operating current	No current going through LEDs		2.2		mA
f_{OSC}	Internal oscillator frequency accuracy		–4% –7%(1)		4% 7%(1)	
T_{TSD}	Thermal shutdown threshold(2)			150		°C
T_{TSD_hyst}	Thermal shutdown hysteresis(2)			20		

(1) Limits apply over the full operating ambient temperature range –30°C ≤ T_A ≤ 85°C.
(2) Verified by design and not tested in production.

7.6 Boost Converter Electrical Characteristics

Unless otherwise specified: T_A = 25°C, V_{DD} = 3.8 V(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DS_ON}	Switch ON resistance	I_{SW} = 0.5 A		0.2		Ω
V_{BOOST_MIN}	Minimum output voltage		6(2)	7	8(2)	V
V_{BOOST_MAX}	Maximum output voltage		27(2)	28	29(2)	V
I_{SW_CL}	SW pin current limit		2.1	2.4	2.5	A
I_{LOAD_MAX}	Maximum continuous load current (3)	I_{SW_LIM} = 2.4 A V_{IN} = 3 V, V_{OUT} = 24 V		160		mA
f_{SW}	Switching frequency			500 1000		kHz
V_{OVP_TH}	Overvoltage protection voltage threshold			V_{BOOST_MAX} + 1.6		V
V_{UVLO_TH}	UVLO threshold			2.5		
V_{UVLO_hyst}	UVLO hysteresis			50		mV
t_{PULSE}	Switch pulse minimum width (3)	No load		80		ns
$t_{STARTUP}$	Boost start-up time (3)			1		ms

(1) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis.
(2) Limits apply over the full operating ambient temperature range –30°C ≤ T_A ≤ 85°C.
(3) Verified by design and not tested in production.

7.7 LED Driver Electrical Characteristics (LED1 To LED6 Pins)

Unless otherwise specified: T_A = 25°C, V_{DD} = 3.8 V(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LEAKAGE}$	Leakage current	Outputs LED1...LED6, V_{OUT} = 28 V			1	µA
I_{LED_MAX}	Maximum sink current LED1...6			25		mA
I_{LED_ACC}	LED current accuracy(2)	Output current set to 20 mA	–3% –4%(3)		3% 4%(3)	
I_{MATCH}	Channel to Channel Matching (2)	Output current set to 20 mA		0.5		
f_{LED}	LED switching frequency(4)	PFREQ = 000b PFREQ = 111b		4.9 39.1		kHz
V_{SAT}	Saturation voltage(5)	Output current set to 20 mA		200		mV

(1) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis.
(2) The LED current accuracy is defined as 100 × (ILED_AVE – ILED_Target) / ILED_AVE. The channel-to-channel LED current matching is defined as (ILED_MAX – ILED_MIN) / ILED_AVE.
(3) Limits apply over the full operating ambient temperature range –30°C ≤ T_A ≤ 85°C.
(4) Verified by design and not tested in production.
(5) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1 V.

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7.8 PWM Interface Characteristics (PWM Pin)

See [1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PWM}	PWM frequency[2]		75		25000	Hz
t_{MIN_ON}	Minimum pulse ON time[2]			1		µs
t_{MIN_OFF}	Minimum pulse OFF time[2]			1		µs
t_{ON}	Turnon delay from standby to backlight on[2]	PWM pin goes from low to switching.		9		ms
t_{STBY}	Turnoff delay from backlight off to standby[2]	PWM pin goes from switching to low.		52		ms
PWM_{RES}	PWM input resolution[2]	f_{IN} < 2.4 kHz		12		bits
		f_{IN} < 4.8 kHz		11		
		f_{IN} < 9.6 kHz		10		
		f_{IN} < 19.5 kHz		9		
		f_{IN} < 25 kHz		8		

(1) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis.
(2) Verified by design and not tested in production.

7.9 Logic Interface Characteristics (PWM, FSET/SDA, ISET/SCL Pins)

Limits apply over the full operating ambient temperature range –30°C ≤ T_A ≤ 85°C[1].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.44			V
I_I	Input current		–1		1	µA
V_{OL}	Output low level	I_{SDA} = 3 mA			0.5	V
I_O	Output leakage	V_{SDA} = 2.8 V			1	µA

(1) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis.

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7.10 I²C Serial Bus Timing Parameters (SDA, SCL)

See[(1)] and Figure 1.

PARAMETER		MIN	MAX	UNIT
f_{SCL}	Clock Frequency		400	kHz
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time	50		ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20 + 0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15 + 0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load Parameter for Each Bus Line Load of 1 pF corresponds to 1 ns.	10	200	ns
t_{WAIT}	Wait time from V_{DD} = 2.7 V to 1st I²C command	150		µs

(1) Verified by design and not tested in production.

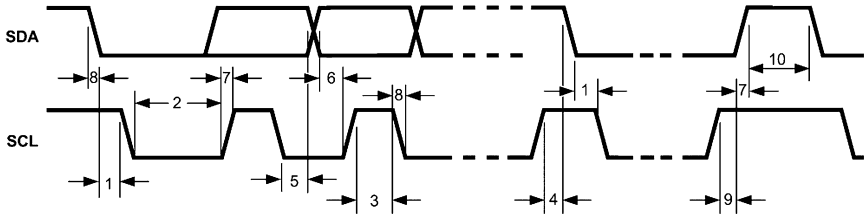

Figure 1. I²C-Compatible Timing

7.11 Typical Characteristics

Unless otherwise specified: $V_{IN} = V_{DD} = 3.8$ V, L = 10 µH Cyntec PIME051E, D = Diodes PD3S130L-7, $C_{OUT} = 2 \times 4.7$ µF, LED $V_f = 2.85$ V (typical), $I_{LED_MAX} = 25$ mA per string.

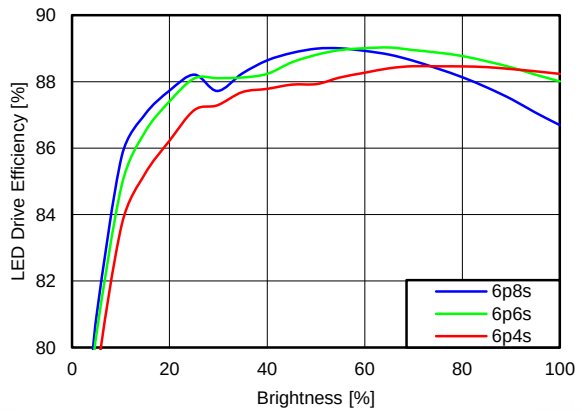

Figure 2. LED Efficiency With 6 LED Strings

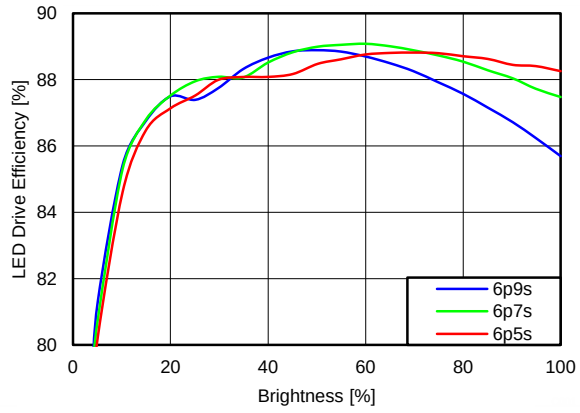

Figure 3. LED Efficiency With 6 LED Strings

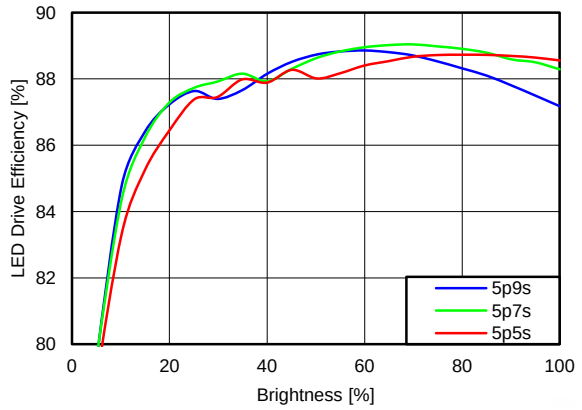

Figure 4. LED Efficiency With 5 LED Strings

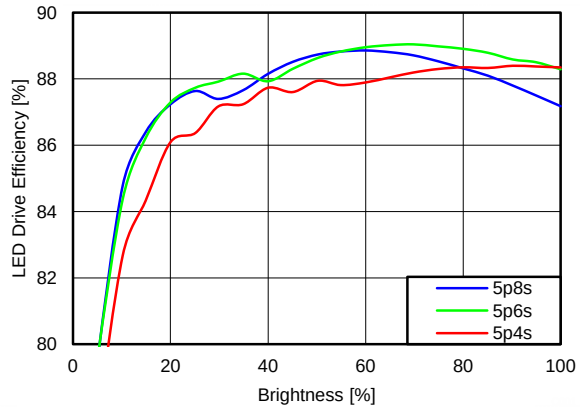

Figure 5. LED Efficiency With 5 LED Strings

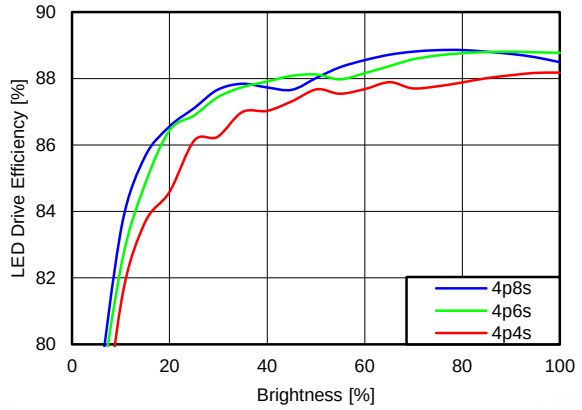

Figure 6. LED Efficiency With 4 LED Strings

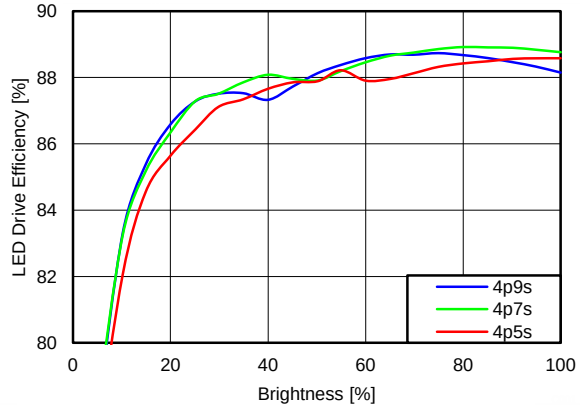

Figure 7. LED Efficiency With 4 LED Strings

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Typical Characteristics (continued)

Unless otherwise specified: $V_{IN} = V_{DD} = 3.8$ V, L = 10 µH Cyntec PIME051E, D = Diodes PD3S130L-7, $C_{OUT} = 2 \times 4.7$ µF, LED $V_f = 2.85$ V (typical), $I_{LED_MAX} = 25$ mA per string.

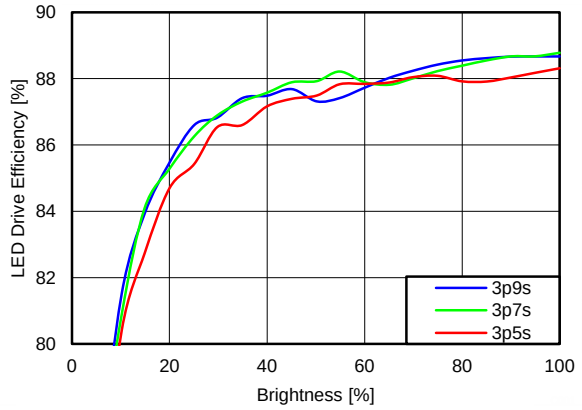


Figure 8. LED Efficiency With 3 LED Strings

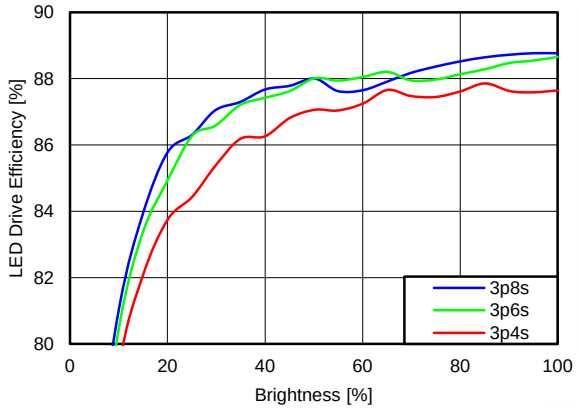


Figure 9. LED Efficiency With 3 LED Strings

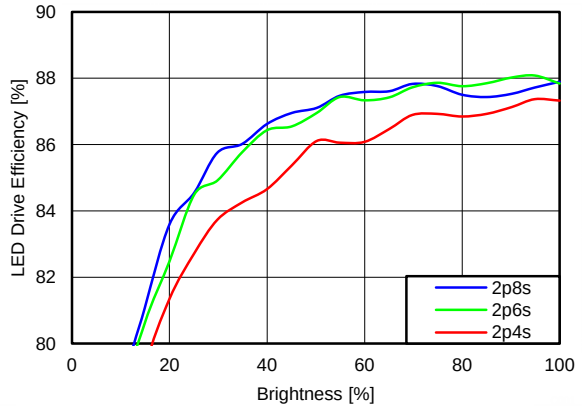


Figure 10. LED Efficiency With 2 LED Strings

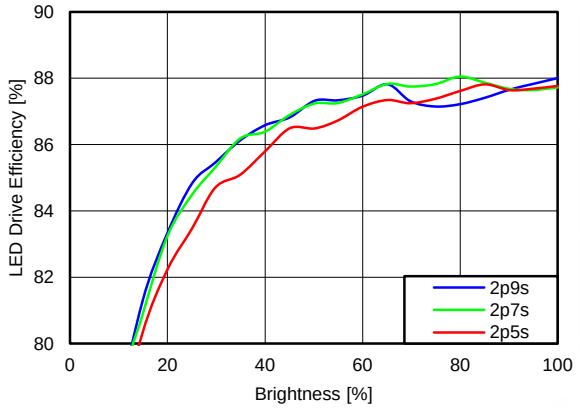


Figure 11. LED Efficiency With 2 LED Strings

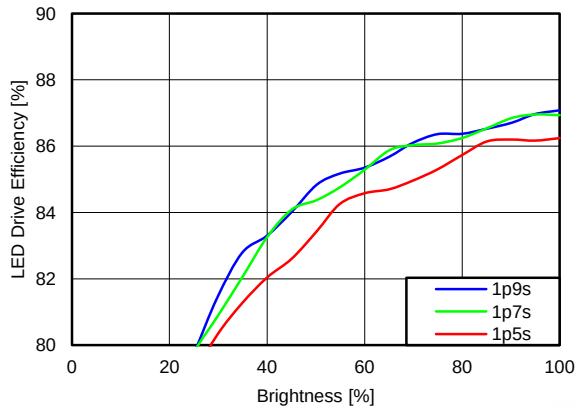


Figure 12. LED Efficiency With 1 LED String

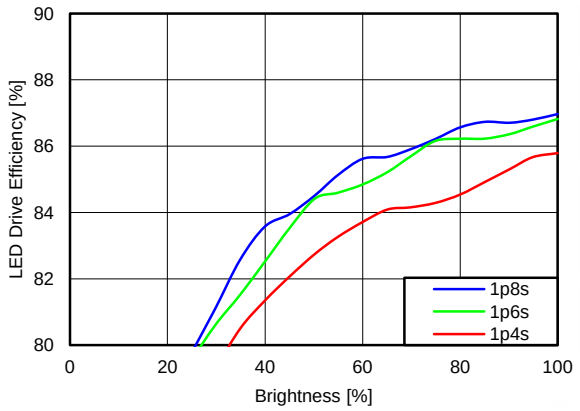
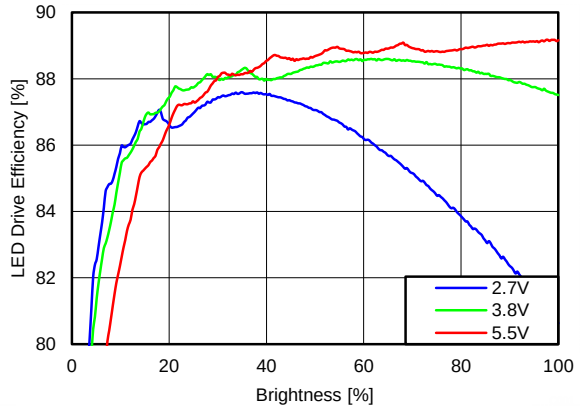


Figure 13. LED Efficiency With 1 LED String

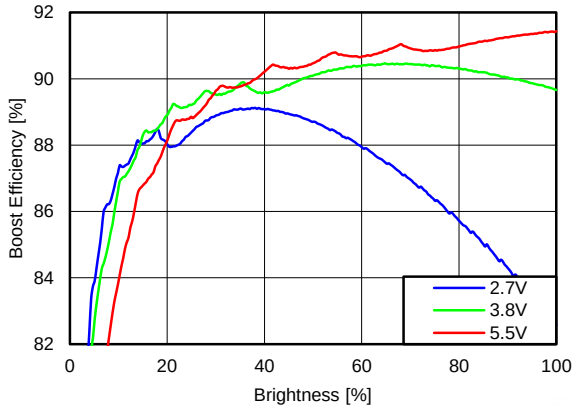
Typical Characteristics (continued)

Unless otherwise specified: $V_{IN} = V_{DD} = 3.8$ V, L = 10 µH Cyntec PIME051E, D = Diodes PD3S130L-7, $C_{OUT} = 2 \times 4.7$ µF, LED $V_f = 2.85$ V (typical), $I_{LED_MAX} = 25$ mA per string.



6p6s Load

Figure 14. LED Efficiency as a Function of VIN/VDD



6p6s Load

Figure 15. Boost Efficiency as a Function of VIN/VDD

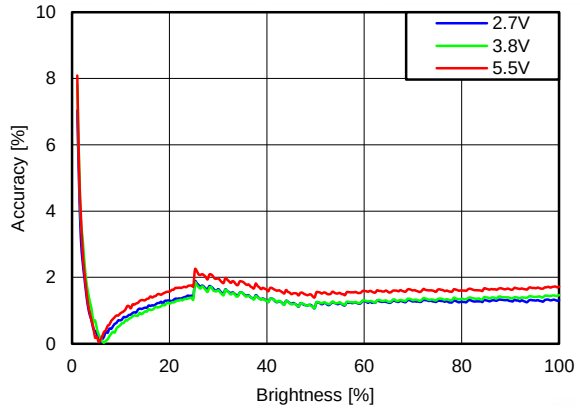


Figure 16. LED Current Accuracy as a Function of VDD

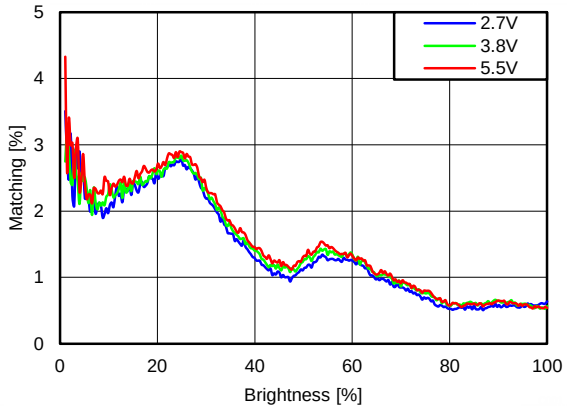


Figure 17. LED Current Channel-Channel Matching as a Function of VDD

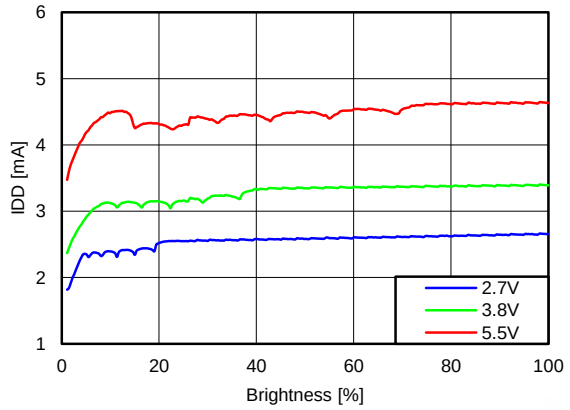


Figure 18. Device Operating Current as a Function of VDD

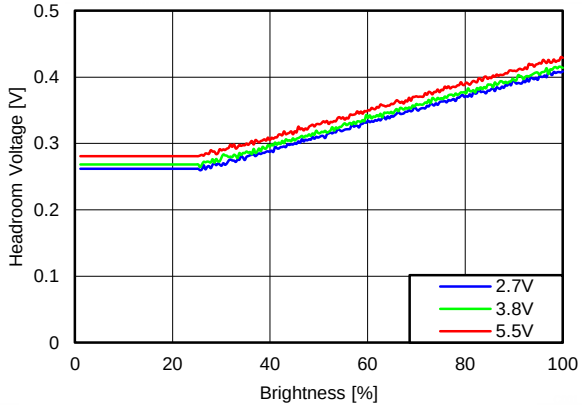


Figure 19. Current Sink Headroom Voltage as a Function of VDD

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8 Detailed Description

8.1 Overview

The LP8557 and LP8557I are high-efficiency LED drivers each featuring an integrated DC-DC inductive boost converter and six high-precision current sinks. LP8557 is intended for applications that exclusively use a pulse width modulated (PWM) signal for controlling the brightness while LP8557I is intended for applications that can utilize an I^2C master as well.

The boost converter has adaptive output voltage control. This feature minimizes the power consumption by adjusting the voltage to the lowest sufficient level under all conditions.

The adaptive current sink headroom voltage control scales the headroom voltage with the LED current for optimal system efficiency.

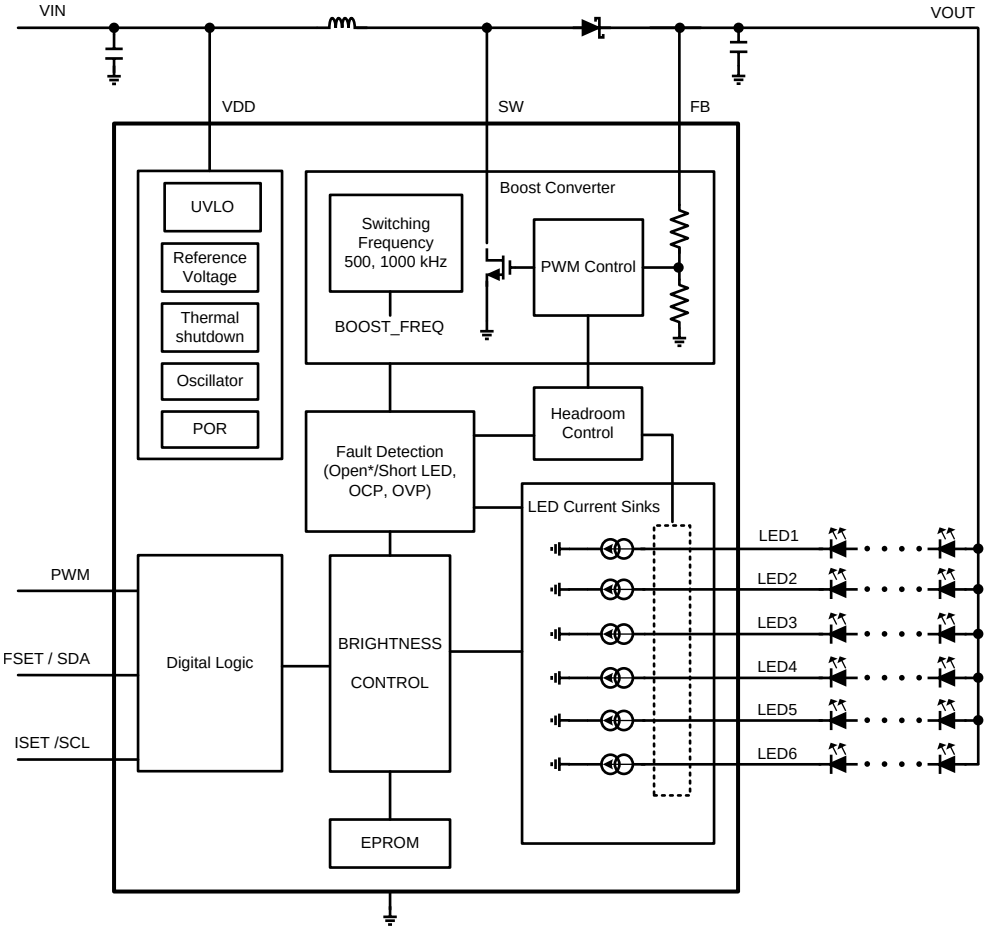
The LED string auto-detect function enables use of the same device in systems with 1 to 6 LED strings for the maximum design flexibility.

Proprietary hybrid PWM plus current mode dimming enables additional system power savings. Phase shift PWM allows reduced audible noise and smaller boost output capacitors.

Flexible CABC support combines brightness level selections based on the PWM input and I^2C commands.

The LP8557 and LP8557I feature a full set of features that ensure robust operation of the device and external components. The set consists of input undervoltage lockout, thermal shutdown, overcurrent protection, overvoltage protection, and LED open and short detection.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Boost Converter Overview

8.3.1.1 Operation

The boost DC-DC converter generates a 7-V to 28-V boost output voltage from a 2.7-V to 5.5-V boost input voltage.

The converter is a magnetic switching PWM mode DC-DC inductive boost converter with a current limit. It uses current programmed mode control, where the inductor current is measured and controlled with the feedback. During start-up, the soft-start function reduces the peak inductor current. Figure 20 shows the boost block diagram.

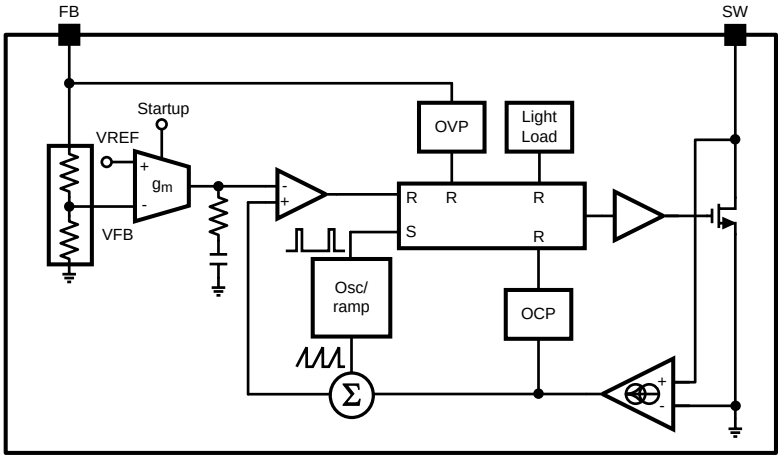


Figure 20. Boost Circuit Block Diagram

8.3.1.2 Adaptive Boost Output Voltage Control

The boost converter operates in adaptive boost control mode. In this mode, the voltage at the LED pins is monitored by the control loop. It raises the boost voltage when the measured voltage of ANY of the LED strings falls below the voltage threshold of its corresponding LOW comparator. If the headrooms of ALL of the LED strings are above the voltage threshold of their corresponding MID comparator, then the boost voltage is lowered.

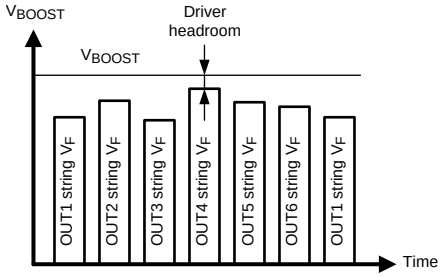


Figure 21. Adaptive Headroom Detail

8.3.2 Brightness Control

The brightness can be controlled using an external PWM signal or the Brightness registers accessible via an I^2C interface or both. Which of these two input sources is selected is set by the BRTMODE bits. The LP8557 operates exclusively in BRTMODE = 00. While the LP8557I, by default, operates in BRTMODE = 11, it can operate in all BRTMODE settings by configuring the bits via the I^2C interface. How the brightness is controlled in each of the four possible modes is described in the following sections.

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Feature Description (continued)

8.3.2.1 PWM Input Duty Measurement

When using PWM input for brightness control the input PWM duty cycle is measured as described in following diagram and the brightness is controlled based on the result. When changing the brightness it must be noted that the measurement cycle is from rising edge to next rising edge and brightness change must be done accordingly (time from rising to rising edge is constant (=cycle time) and falling edge defines the brightness).

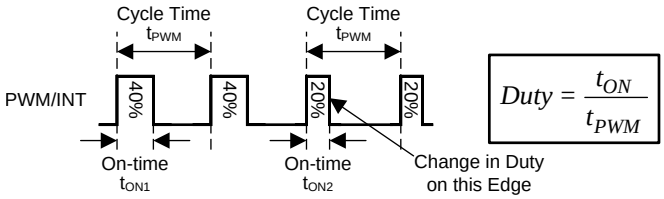

Figure 22. PWM Input Duty Cycle Measurement

8.3.2.2 BRTMODE = 00b

With BRTMODE = 00b, the LED output current is controlled by the PWM input duty cycle. The PWM detector block measures the duty cycle at the PWM pin and uses it to generate a PWM-based brightness code. Before the output is generated, the code goes through the curve shaper block. Then the code goes into the hybrid PWM & I Dimming block which determines the range of the PWM and Current control. The outcome of the hybrid PWM & I dimming block is current and/or up to 6 PWM output signals.

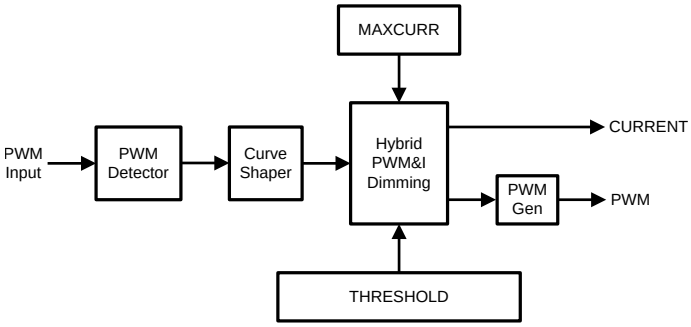

Figure 23. Brightness Data Path for BRTMODE = 00b

Feature Description (continued)

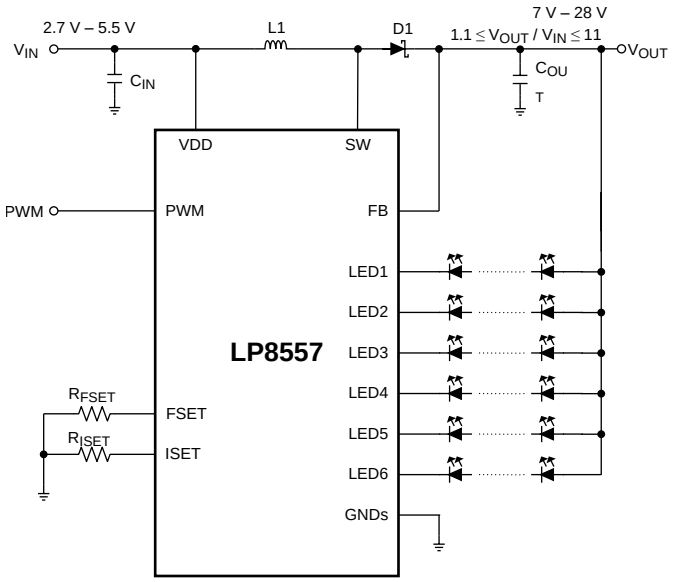

Figure 24. Typical Application Circuit for Devices Configured With BRTMODE = 00

8.3.2.3 BRTMODE = 01b

With BRTMODE = 01b, the LED output current is controlled by the BRTHI/BRTLO registers. Before the output is generated the BRTHI/BRTLO registers-based brightness code goes through the Curve Shaper block. Then the code goes into the hybrid PWM & I dimming block which determines the range of the PWM and current control. The outcome of the Hybrid PWM&I Dimming block is Current and/or up to 6 PWM output signals.

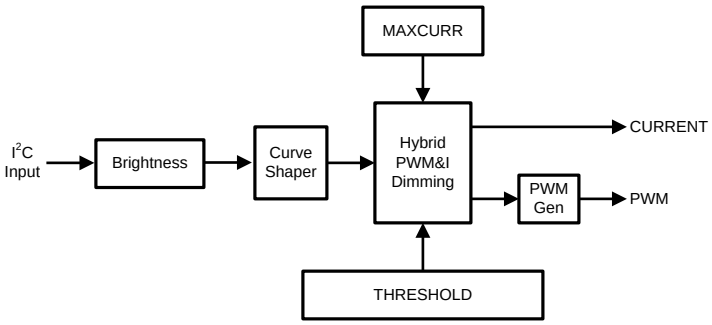

Figure 25. Brightness Data Path for BRTMODE = 01b

8.3.2.4 BRTMODE = 10b

With BRTMODE = 10b, the LED output current is controlled by the PWM input duty cycle and the BRTHI/BRTLO registers. The PWM detector block measures the duty cycle at the PWM pin and uses it to generate PWM-based brightness code. Before the code is multiplied with the BRTHI/BRTLO registers-based brightness code, it goes through the curve shaper block. After the multiplication, the resulting code goes into the hybrid PWM & I dimming block which determines the range of the PWM and Current control. The outcome of the hybrid PWM & I dimming block is current or up to 6 PWM output signals.

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Feature Description (continued)

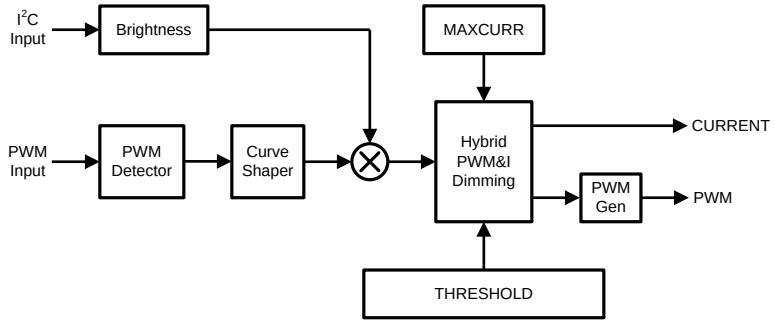

Figure 26. Brightness Data Path for BRTMODE = 10b

8.3.2.5 BRTMODE = 11b

With BRTMODE = 11b, the LED output current is controlled by the PWM input duty cycle and the BRTHI/BRTLO registers. The PWM detector block measures the duty cycle at the PWM pin and uses it to generate PWM-based brightness code. In this mode, the BRTHI/BRTLO registers-based brightness code goes through the curve shaper block before it is multiplied with the PWM input duty cycle-based brightness code. After the multiplication, the resulting code goes into the hybrid PWM & I dimming block which determines the range of the PWM and Current control. The outcome of the hybrid PWM & I dimming block is current and/or up to 6 PWM output signals.

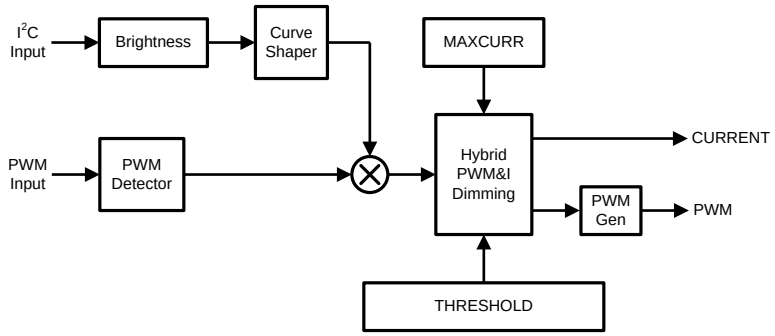

Figure 27. Brightness Data Path for BRTMODE = 11b

Feature Description (continued)

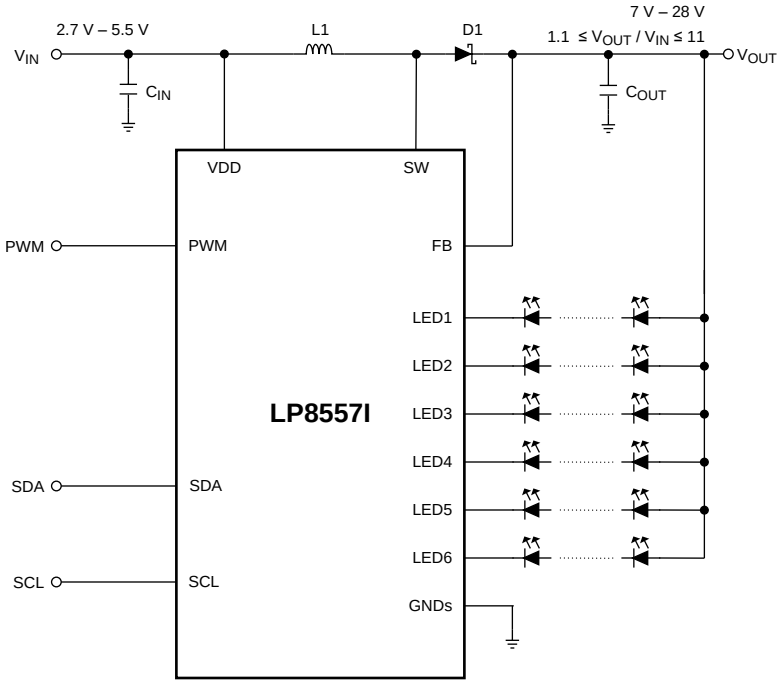

Figure 28. Typical Application Circuit for Devices Configured With BRTMODE = 01, 10, or 11

8.3.2.6 Hybrid PWM & I Dimming Control

Hybrid PWM & I dimming control combines PWM dimming and LED current-dimming control methods. With this dimming control, better optical efficiency is possible from the LEDs compared to pure PWM control while still achieving smooth and accurate control and low brightness levels. The switch point from current-to-PWM control can be set to get the optimal compromise between good matching of the LEDs brightness/white point at low brightness and good optical efficiency.

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Feature Description (continued)

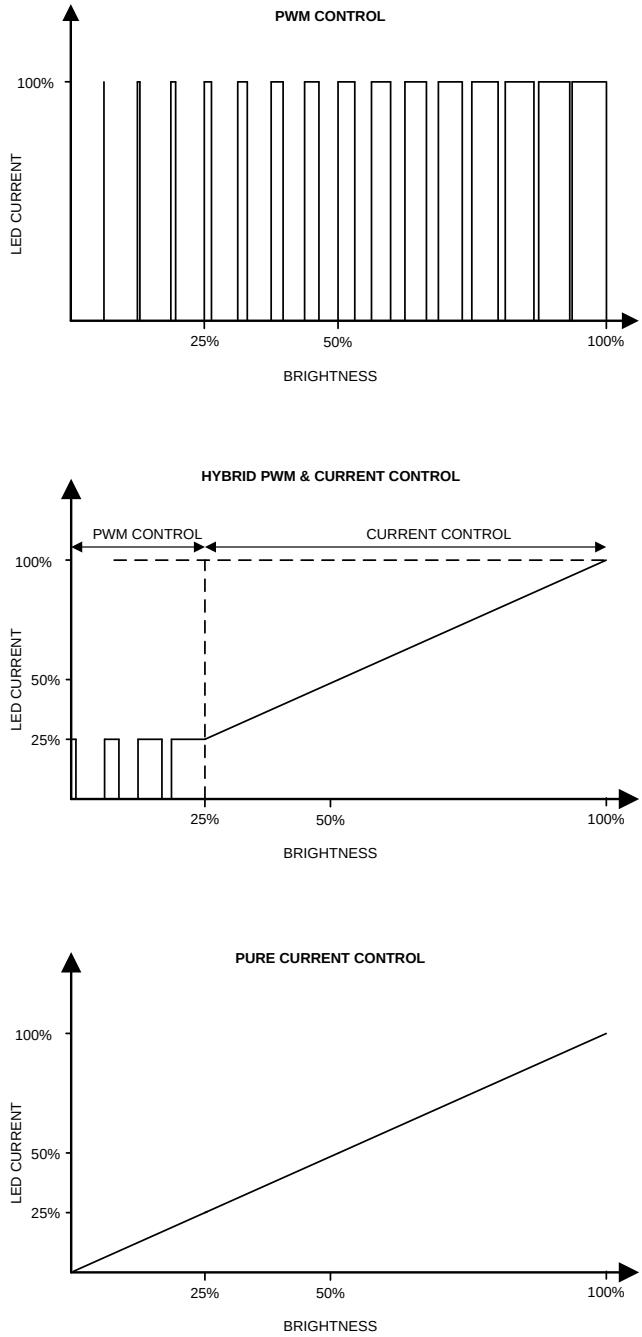

Figure 29. Dimming Methods

8.3.2.7 Phase Shift PWM Scheme

The phase shift PWM (PSPWM) scheme allows delay of the time when each LED current sink is active. When the LED current sinks are not activated simultaneously, the peak load current from the boost output is greatly decreased. This reduces the ripple seen on the boost output and allows smaller output capacitors to be used. Reduced ripple also reduces the output ceramic capacitor audible ringing. The PSPWM scheme also increases the load frequency seen on the boost output by up to six times, therefore transferring the possible audible noise to the frequencies outside the audible range.

The phase difference between each active driver is automatically determined as 360°/number of active drivers.

Feature Description (continued)

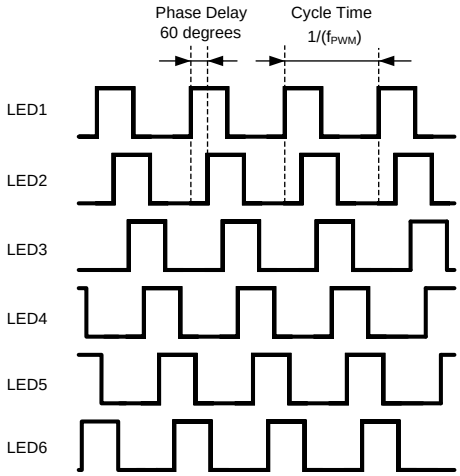

Figure 30. Phase Shift PWM Dimming Scheme Diagram

8.3.3 Slope and Advanced Slope

The transition time between two brightness values can be programmed with the STEP bits from 0 to 200 ms. The same slope time is used for sloping up and down. With advanced slope the brightness changes can be made more pleasing to a human eye. It is implemented with a digital smoothing filter. The filter strength is set with SMOOTH bits.

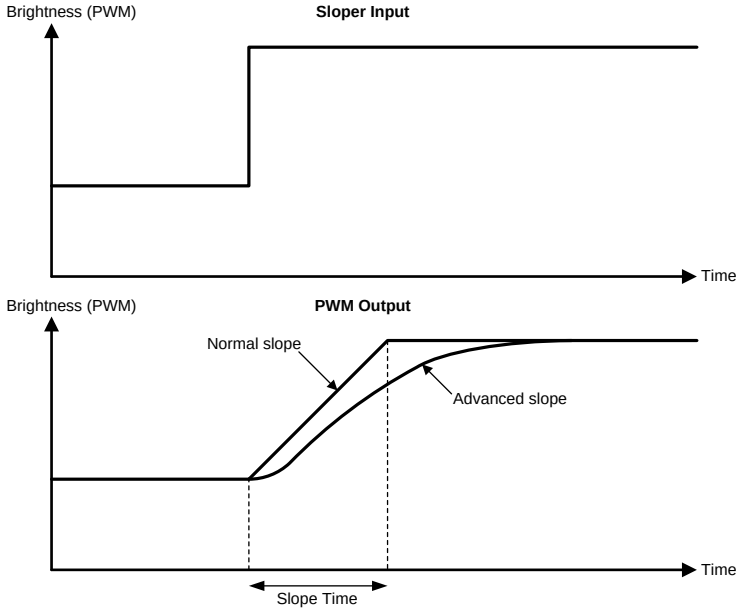

Figure 31. Slope and Advanced Slope

8.3.4 LED String Count Auto Detection

The LP8557 and LP8557I can auto-detect the number of the LED strings attached. During the auto-detect routine, the devices automatically remove the unused current sink(s) and adjust the phasing of the remaining current sinks. The LED OPEN* fault condition is not supported with auto-detect function enabled. On the LP8557I, the user may disable the function by setting CONFIG.AUTO bit to 0 via an I^2C write.

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Feature Description (continued)

8.3.5 EMI Reduction Schemes

LP8557I features two EMI reduction schemes. By default, the schemes are disabled; however, the schemes can be enabled by I^2C writes to SSEN and SREN bits in COMMAND register. The schemes are unavailable on the LP8557.

The first scheme, programmable slew rate control, uses a combination of three drivers for boost switch. Enabling all three drivers allows boost switch on/off transition times to be the shortest. On the other hand, enabling just one driver allows boost switch on/off transition times to be the longest. The longer the transition times, the lower the switching noise on the SW terminal. It should also be noted that the shortest transition times bring the best efficiency as the switching losses are the lowest. This scheme can be enabled by setting SREN=1 with an I^2C write.

The second EMI reduction scheme is the spread spectrum scheme. This scheme deliberately spreads the frequency content of the boost switching waveform, which inherently has a narrow bandwidth, makes the switching waveform's bandwidth wider and ultimately reduces its EMI spectral density. This scheme can be enabled by setting SSEN = 1 with an I^2C write.

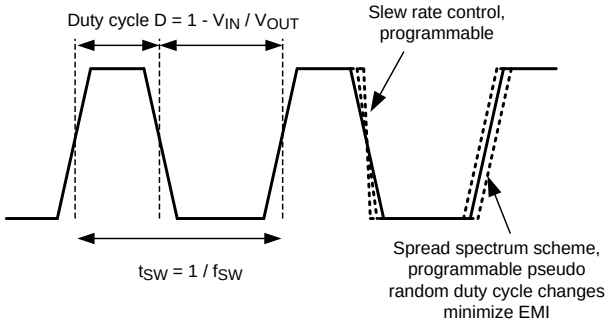

Figure 32. EMI Reduction Schemes

8.3.6 Fault Detection

The LP8557 and LP8557I have fault detection for LED SHORT, UVLO, BST_OVP, BST_OCP, BST_UV, and TSD. Additionally, the LP8557I can support LED OPEN* fault. Faults are recorded in the STATUS register. Each time the STATUS register is read it is automatically cleared.

8.3.6.1 LED Short Detection

Voltages at the individual current sinks are constantly monitored for the LED SHORT fault. This fault may occur when some LEDs in a string are electrically bypassed making that LED string shorter than the other LED strings. The reduced forward voltage causes the current sink attached to that string to have a higher headroom voltage than the other current sinks. When the headroom voltage is higher than the fault comparator threshold (configured with the 0V field in the LEDEN register), that current sink is disabled, and the PWM phasing is automatically adjusted. The fault comparator threshold is at 2 V, typical.

8.3.6.2 LED OPEN Detection*

When the auto-detect function is disabled, each current sink is also monitored for the LED OPEN* condition. The condition is set when the headroom voltage on one or more current sinks is below the LOW comparator threshold, and the boost voltage is at the maximum. This fault condition may be caused by one or more OPEN LED strings or by one or more current sinks shorted to GND. The LP8557I immediately shuts down the backlight whenever an LED OPEN* condition is detected on any enabled LED drivers. The backlight does not turn on again (regardless of the COMMAND.ON bit) until the STATUS register is read.

8.3.6.3 Undervoltage Detection

The device continuously monitors the voltage on the VDD pin. When the VDD voltage drops below 2.5 V the backlight is immediately shut down, and the UVLO bit is set in the STATUS register. The backlight automatically starts again when the voltage has increased above 2.5 V + 50 mV hysteresis. Hysteresis is implemented to avoid continuously triggering undervoltage.

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Feature Description (continued)

8.3.6.4 Thermal Shutdown

If the internal temperature reaches 150°C, the deviceimmediately shuts down the backlight to protect it from damage. The TSD bit is also set in the STATUS register. The device re-activates the backlight again when the internal temperature drops below 130°C.

8.3.6.5 Boost Overcurrent Protection

The device automatically limits boost current to 2.4 A . When the 2.4-A limit is reached the BST_OCP bit is set in the STATUS register. It is normal for the device to trigger the boost current limit during the start-up or sudden brightness changes. The STATUS register can be cleared by reading the bit. If the bit is permanently set, it may indicate an issue in the application.

8.3.6.6 Boost Overvoltage Protection

The device automatically limits boost voltage to VBOOST_MAX + 1.6 V. When the limit is reached the BST_OVP bit is set in the STATUS register. It is normal for the device to trigger the boost OVP limit during the start-up or sudden brightness changes. The status register can be cleared by reading the bit. If the bit is permanently set, it may indicate an issue in the application.

8.3.6.7 Boost Undervoltage Protection

The device can detect when the boost voltage is below VBOOST – 2.5 V for longer than 6 ms. When the threshold is reached the BST_UV bit is set in the STATUS register.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The device is in shutdown mode when the VDD pin is low. Current consumption in this mode from VDD pin is < 1 µA.

8.4.2 Active Mode

In active mode the backlight is enabled either with setting the ON register bit high (LP8557I) or by activating PWM input (LP8557). The power supplying the VDD pin must be present. Brightness is controlled with I^2C writes to brightness registers or by changing PWM input duty cycle (operation without I^2C control). Configuration registers are not accessible in Active mode to prevent damage to the device by accidental writes. Current consumption from VDD terminal in this mode is typically 2.2 mA when LEDs are not drawing any current.

8.5 Programming

8.5.1 I^2C-Compatible Serial Bus Interface

8.5.1.1 Interface Bus Overview

The I^2C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bi-directional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). These lines must be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle.

The default 7-bit I^2C address for the LP8557I slave is 2Ch.

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Programming (continued)

8.5.1.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the I^2C session (see Figure 33). A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I^2C master always generates START and STOP conditions. The I^2C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I^2C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW.

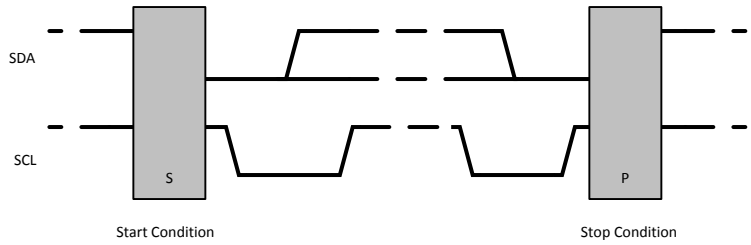

Figure 33. Start And Stop Conditions

After the START condition, the I^2C master sends the 7-bit address followed by an eighth read or write bit (R/W). R/W = 0 indicates a WRITE, and R/W = 1 indicates a READ. The second byte following the chip address selects the register address to which the data is written. The third byte contains the data for the selected register.

8.5.1.3 Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

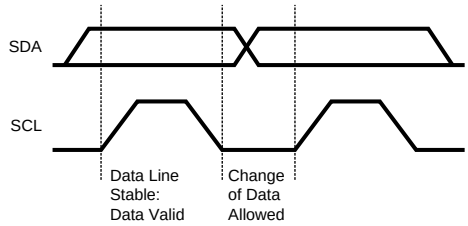

Figure 34. Bit Transfer

Each data transaction is composed of a START Condition, a number of byte transfers (set by the software) and a STOP Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

8.5.1.4 Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

Programming (continued)

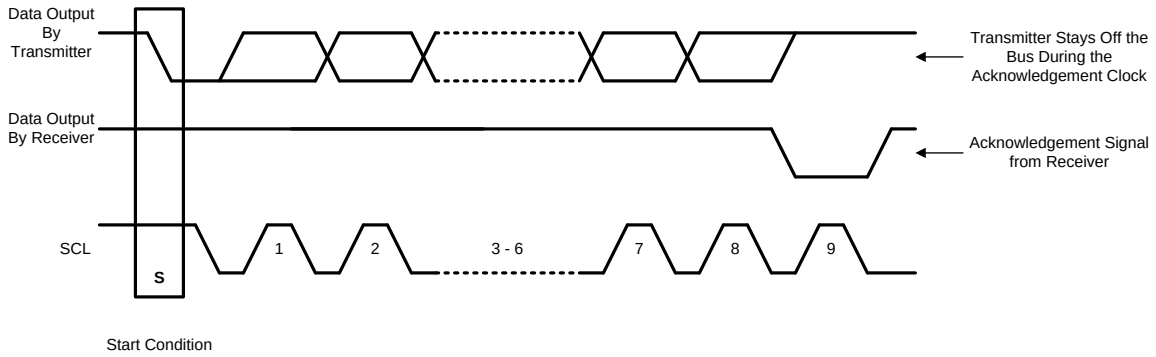

Figure 35. Bus Acknowledge Cycle

8.5.1.5 Acknowledge After Every Byte Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the acknowledge after every byte rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (negative acknowledge) the last byte clocked out of the slave. This negative acknowledge still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

8.5.1.6 Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master sends further data bytes the control register address is incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

8.5.1.7 Control Register Read Cycle

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address is incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

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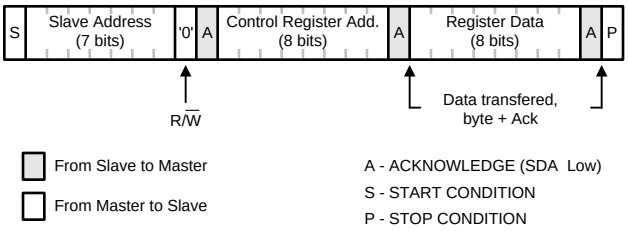
Programming (continued)

Table 1. Data Read and Write Cycles

	ADDRESS MODE
Data Read	<Start Condition>
	<Slave Address><r/w = ‘0’>[Ack]
	<Register Addr.>[Ack]
	<Repeated Start Condition>
	<Slave Address><r/w = ‘1’>[Ack]
	[Register Data]<Ack or Nack>
	… additional reads from subsequent
	register address possible
	<Stop Condition>
Data Write	<Start Condition>
	<Slave Address><r/w=’0’>[Ack]
	<Register Addr.>[Ack]
	<Register Data>[Ack]
	… additional writes to subsequent
	register address possible
	<Stop Condition>

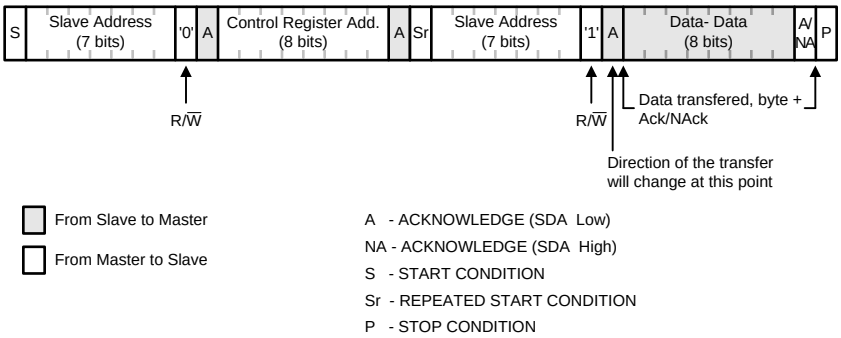
<> Data from master; [] Data from slave

8.5.1.8 Register Read and Write Detail



Register Write Format

Figure 36. Register Write Format



Register Read Format

Figure 37. Register Read Format

8.6 Register Maps

Register	Addr	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND	00h	RESET					SREN	SSEN	ON
STATUS	01h	LED_OPEN*	LED_SHORT		BST_UV	BST_OVP	BST_OCP	TSD	UVLO
BRTLO	03h	BRT[3:0]							
BRTHI	04h	BRT[11:4]							
CONFIG	10h	PWMSB					AUTO	BRTMODE	
CURRENT	11h	ISET					MAXCURR		
PGEN	12h	PFSET					PFREQ		
BOOST	13h	BCSET	BISET					BCOMP	BFREQ
LEDEN	14h			ENABLE					
STEP	15h	SMOOTH						STEP	

The register map is useful for LP8557I users intending to re-configure the register reset values. **If re-configuration is necessary, it has to be done every time the power on VDD pin is recycled.**

There is a restriction on register writes. The COMMAND, BRTLO, and BRTHI registers can be written at any time; however, the remaining registers only accept writes when the COMMAND.ON bit is low. All registers can be read at any time.

Many registers contain empty bit locations. These blank areas are reserved for future use. When writing to a register any empty fields must not be modified; when reading a register, these empty fields should be ignored.

8.6.1 Register Bit Descriptions

8.6.1.1 COMMAND

Address: 0x00h

Reset: 0x00h (LP8557I)

D7	D6	D5	D4	D3	D2	D1	D0
RESET	—				SREN	SSEN	ON

Bits	Field	Type	Default	Description
7	RESET	R/W	0b	Write 1 to reset the device. This bit is self-clearing and is always 0 when read.
6:3	reserved	R/O	0000b	
2	SREN	R/W	0b	Enable the boost slew rate control. **0 = Slew-rate control off (Default)** 1 = Slew-rate control on
1	SSEN	R/W	0b	Enable the spread-spectrum boost clocking. **0 = Spread-spectrum off (Default)** 1 = Spread-spectrum on
0	ON	R/W	See Description	Turn on the backlight. **0 = backlight off (Default)** 1 = backlight on

The COMMAND.ON bit is used to turn on the backlight.

The COMMAND.SSEN and COMMAND.SREN bits may be updated at any time. It is not necessary for the backlight to be off when changing COMMAND.SSEN or COMMAND.SREN.

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8.6.1.2 STATUS

Address: 0x01h

Reset: 0x00h

D7	D6	D5	D4	D3	D2	D1	D0
LED_OPEN*	LED_SHORT	–	BST_UV	BST_OVP	BST_OCP	TSD	UVLO

Bits	Field	Type	Default	Description
7	LED_OPEN*	R/O	0b	An LED_OPEN* condition was detected on one or more strings. The condition is set when the headroom voltage on one or more current sinks is below the LOW comparator threshold, and the boost voltage is at the maximum. This fault condition may be caused by one or more OPEN LED strings or by one or more current sinks shorted to GND. Once set this bit stays set until the STATUS register is read. An LED_OPEN* condition turns off the backlight when CONFIG.AUTO is 0. When CONFIG.AUTO is 1, the condition is never set.
6	LED_SHORT	R/O	0b	An LED SHORT condition was detected on one or more strings. The condition is set when the headroom voltage on one or more current sinks is above the FAULT comparator threshold and at least one driver has the headroom voltage in regulation (between LOW and MID comparator thresholds). This fault condition may be caused by one or more shorted LEDs on one or more (but not all) strings. Once set this bit stays set until the STATUS register is read.
5	reserved	R/O	0b	
4	BST_UV	R/O	0b	A boost output undervoltage condition was detected. The boost voltage is 2.5 V (typical) or more below the target. Once set this bit stays set until the STATUS register is read.
3	BST_OVP	R/O	0b	A boost overvoltage protection condition was detected. The boost voltage is 1.6 V (typical) above the VMAX value. Once set this bit stays set until the STATUS register is read.
2	BST_OCP	R/O	0b	A boost overcurrent protection condition was detected. Once set this bit stays set until the STATUS register is read.
1	TSD	R/O	0b	A thermal shutdown condition was detected. Once set, this bit stays set until the STATUS register is read. A thermal shutdown condition turns off the backlight.
0	UVLO	R/O	0b	An input undervoltage lockout condition was detected. Once set, this bit stays set until the STATUS register is read. An undervoltage lockout condition turns off the backlight.

8.6.1.3 BRTLO

Address: 0x03h

Reset: 0x00h

D7	D6	D5	D4	D3	D2	D1	D0
BRT[3:0]				—			

Bits	Field	Type	Default	Description
7:4	BRT[3:0]	R/W	0000b	Least significant bits of the 12-bit wide brightness level. If controlling the brightness with 8-bit resolution, writing to this register is not needed.
6:0	reserved	R/O	0000b	Reserved.

8.6.1.4 BRTHI

Address: 0x04h

Reset: 0x00h

D7	D6	D5	D4	D3	D2	D1	D0
BRT[11:4]							

Bits	Field	Type	Default	Description
7:0	BRT[11:4]	R/W	00h	Most significant bits of the 12-bit wide brightness level. If controlling the brightness with the 8-bit resolution, writing to this register is all that is needed.

The brightness level can be updated via one (8 bits) or two (16 bits) register writes. The internal brightness level is 12 bits wide and is only updated when the BRTHI register is written. If the BRTHI register is written without a previous write to the BRTLO register, then the lower order bits of the internal brightness is synthesized from the BRTHI register value.

BRTLO	BRTHI	Brightness	Comments
write 0x95	write 0xFC	0xFC9	BRTLO[3:0] is ignored
write 0x10	write 0xDC	0xDC1	set to an exact 12-bit value
no write	write 0x8C	0x8C8	synthesize low order bits
no write	write 0x0C	0x0C0	synthesize low order bits
no write	write 0x00	0x000	0% brightness
no write	write 0xFF	0xFFF	100% brightness

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8.6.1.5 CONFIG

Address: 0x10h

Reset: 0x07h (LP8557I)

D7	D6	D5	D4	D3	D2	D1	D0
PWMSB	—				AUTO	BRTMODE[1:0]	

Bits	Field	Type	Default	Description
7	PWMSB	R/W	0b	Enables PWM standby mode **0 = COMMAND.ON alone turns the backlight on/off (Default)** 1 = turn off the backlight after 52 ms of PWM pin low
6:3	reserved	R/O	0000b	
2	AUTO	R/W	1b	Automatic LED string configuration0 = enable LED strings using just LEDEN.ENABLE **1 = disable all open LED strings (Default)**
1:0	BRTMODE	R/W	11b	Brightness mode 00 = PWM 01 = BRTHI/BRTLO registers 10 = PWM × unshaped BRTHI/BRTLO registers **11 = Unshaped PWM × BRTHI/BRTLO registers**

The AUTO bit is set, and the LED string configuration is done automatically. The LP8557I allows users to disable the auto-detect function by setting AUTO bit to 0b.

8.6.1.6 CURRENT

Address: 0x11h

Reset: 0x07h (LP8557I)

D7	D6	D5	D4	D3	D2	D1	D0
ISET	——				MAXCURR[2:0]		

Bits	Field	Type	Default	Description
7	ISET	R/W	0b	Set full-scale LED current via the ISET pin. **0 = Full-scale current is set with MAXCURR bits. (Default)** 1 = Full-scale current is set with an external, R_{ISET}, resistor.
6:3	reserved	R/O	0000b	
2:0	MAXCURR	R/W	111b	Full-scale current (100% brightness). 000 = 5 mA 001 = 10 mA 010 = 13 mA 011 = 15 mA 100 = 18 mA 101 = 20 mA 110 = 23 mA **111 = 25 mA (Default)**

The ISET bit determines how the maximum LED current is set. On the LP8557I (ISET = 0), the maximum LED current is 25 mA. It may be re-configured via the I^2C interface by overriding MAXCURR bits. Note that re-configuration must be done every time the power on VDD pin is recycled.

8.6.1.7 PGEN

Address: 0x12h

Reset: 0x29h (LP8557I)

D7	D6	D5	D4	D3	D2	D1	D0
PFSET	—	THRESHOLD			PRFEQ[2:0]		

Bits	Field	Type	Default	Description
7	PFSET	R/W	0b	Set PWM output frequency via the FSET pin. **0 = PWM output frequency is set with PRFEQ bits. (Default)** 1 = PWM output frequency is set with an external, R_{FSET}, resistor.
6:3	reserved	R/O	0101b	
5:3	THRESHOLD	R/W	EPROM	Adaptive dimming threshold. PWM dimming is used below threshold, and current dimming is used above threshold. 000 = 100% current diming 001 = PWM below 1.5625% (6-bit PWM) 010 = PWM below 3.125% (7-bit PWM) 011 = PWM below 6.25% (8-bit PWM) 100 = PWM below 12.5% (9-bit PWM) 101 = PWM below 25% (10-bit PWM) 110 = PWM below 50% (11-bit PWM) 111 = 100 %PWM below (12-bit PWM)
2:0	PFREQ	R/W	001b	PWM output frequency 000 = 4.9 kHz **001 = 9.8 kHz (Default)** 010 = 14.6 kHz 011 = 19.5 kHz 100 = 24.4 kHz 101 = 29.3 kHz 110 = 34.2 kHz 111 = 39.1 kHz

The PFSET bit distinguishes how the PWM dimming frequency is set. On the LP8557I (PFSET = 0), the PWM dimming frequency is 9.8 kHz by default. It may be re-configured via I^2C interface by overriding PFREQ bits. Note that re-configuration must be done every time the power on VDD pin is recycled.

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8.6.1.8 BOOST

Address: 0x13h

Reset: 0x02h (LP8557I)

D7	D6	D5	D4	D3	D2	D1	D0
BFSET	BCSET	—				BCOMP	BFREQ

Bits	Field	Type	Default	Description
7	BFSET	R/W	0b	Set boost frequency via the FSET pin. **0 = Boost frequency is set with BFREQ bits. (Default)** 1 = boost frequency is set with an external, R_{FSET}, resistor.
6	BCSET	R/W	0b	Set boost inductor size via ISET pin. **0 = boost inductor and compensation is set with BCOMP bit. (Default)** 1 = boost inductor is set with an external, R_{ISET}, resistor.
5:2	reserved	R/O	0000b	
1	BCOMP	R/W	1b	Boost compensation options. 0 = Boost compensation option 0 **1 = Boost compensation option 1 (Default).**
0	BFREQ	R/W	0b	Boost frequency. **0 = 500 kHz (Default)** 1 = 1 MHz

The BFSET bit distinguishes how the boost switching frequency is set. If BFSET = 0, the boost switching frequency is set by the BFREQ bit. If BFSET = 1, the switching frequency is set with an external resistor. On the LP8557I (BFSET = 0), the boost switching frequency is 500 kHz by default. It may be re-configured via the I^2C interface by overriding the BFREQ bit. Please note the re-configuration must be done every time the power on the VDD pin is recycled.

The BCSET bit distinguishes how the boost inductor and compensation is set. If BCSET = 0, the boost inductor and compensation is set by the BCOMP bit. If BCSET = 1, the boost inductor and compensation is set with an external resistor. On the LP8557I (BCSET = 0), the boost compensation is set to option 1 by default. It may be re-configured via I^2C interface by overriding BCOMP bit. Please note the re-configuration must be done every time the power on the VDD pin is recycled.

8.6.1.9 LEDEN

Address: 0x14h

Reset: 0xBFh (LP8557I)

D7	D6	D5	D4	D3	D2	D1	D0
-		ENABLE[6:1]					

Bits	Field	Type	Default	Description
7:6	reserved	R/W	10b	
5:0	ENABLE	R/W	111111b	LED string enables. 000001 = Only 1 current sink enabled. . . 001111 = Current sinks 1-4 enabled. 011111 = Current sinks 1-5 enabled. **111111 = All 6 current sinks enabled (Default)**

The ENABLE field configures the strings if the AUTO bit is 0. The LP8557I allows re-configuration of the ENABLE bits via I^2C writes. Note that re-configuration must be done every time the power on the VDD pin is recycled.

8.6.1.10 STEP

Address: 0x15h

Reset: 0x00h (LP8557I)

D7	D6	D5	D4	D3	D2	D1	D0
SMOOTH[1:0]		—				STEP[1:0]	

Bits	Field	Type	Default	Description
7:6	SMOOTH	R/W	00b	Filter strength for digital smoothing filter. **00 = no smoothing (Default)** 10 = light smoothing 10 = medium smoothing 11 = heaving smoothing
5:2	reserved	R/W	0000b	
1:0	STEP	R/W	00b	Ramp time for a 0% to 100% current change. **00 = 0 ms (Default)** 01 = 50 ms (12.2 µs/12-bit LSB) 10 = 100 ms (24.4 µs/12-bit LSB) 11 = 200 ms (48.8 µs/12-bit LSB)

On LP8557I, it is possible to enable slope and advanced slope functions by re-configuration of the STEP and SMOOTH bits appropriately via I^2C writes. Note that re-configuration must be done every time power on the VDD pin is recycled.

The STEP field controls the rate of brightness level changes (slope function). Brightness transitions have a fixed step time. The time required to complete a ramp between two levels also depends upon the difference between the starting and ending current levels. For example, when STEP is set to 10b a brightness transition from 0% to 100% takes 100 ms, while a transition from 50% to 100% takes 50 ms.

The SMOOTH field controls the digital smoothing filter (advanced slope function). This filter behaves much like an RC filter. It can be used to remove the overshoot that appears to occur on large brightness changes. The actual amount of smoothing is tailored for the STEP field setting. For example, medium filter strength is higher for 100-ms ramp times than for 50-ms ramp times. This gives 16 possible brightness-level ramping configurations.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Designing With LP8557

The LP8557 is intended for applications without an I^2C master. It can be fully controlled with an external PWM signal. Boost switching frequency, boost compensation, PWM dimming frequency, and the maximum LED current can be set with external resistors.

9.1.1.1 Setting Boost Switching and PWM Dimming Frequencies

Boost switching frequency and PWM dimming frequency are set by connecting a resistor from the FSET pin to GND. Available options are shown in Table 2.

Table 2. Setting Boost Switching and PWM Dimming Frequencies With an External Resistor

RFSET [Ω] (TOLERANCE)	f_{SW} (kHz)	f_{PWM} (kHz)
470k - 1M (±5%)	500	4.9
300k, 330k (±5%)	500	9.8
200k (±5%)	500	14.6
147k, 150k, 154k, 158k (±1%)	500	19.5
121k (±1%)	500	24.4
100k (±1%)	500	29.3
86.6k (±1%)	500	34.2
75.0k (±1%)	500	39.1
63.4k (±1%)	1000	4.9
52.3k, 53.6k (±1%)	1000	9.8
44.2k, 45.3k (±1%)	1000	14.6
39.2k (±1%)	1000	19.5
34.0k (±1%)	1000	24.4
30.1k (±1%)	1000	29.3
26.1k (±1%)	1000	34.2
23.2k (±1%)	1000	39.1
0 (grounded)	500	9.8

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9.1.1.2 Setting Boost Compensation

For stable LP8557 boost operation, appropriate boost compensation must be selected based on the selected boost switching frequency and the boost inductance. Table 3 shows recommended boost compensation options based on the boost switching frequency and selected boost circuit inductance.

Table 3. Recommended Boost Compensation Options Based on the Boost Switching Frequency and Inductance

f_{SW} (kHz)	L (µH)	RECOMMENDED BOOST COMPENSATION OPTION
500	10 15 22	1 1 0
1000	4.7 6.8 10	1 1 0

The LP8557 boost converter compensation is set by placing an external resistor, RISET, from the ISET pin to GND. Note that the ISET pin is shared for setting the full-scale LED current in addition to setting the boost compensation. Setting the boost compensation and the full-scale LED current using an external resistor is shown in Table 4.

9.1.1.3 Setting Full-Scale Led Current

The LP8557 full-scale current is set by placing an external resistor, RISET, from the ISET pin to GND. Note that the ISET pin is shared for setting the boost compensation in addition to the full-scale LED current. Setting the boost compensation and the full-scale LED current using an external resistor is shown in Table 4.

Table 4. Setting Full-Scale LED Current and Boost Compensation Using an External Resistor

RISET [Ω] (TOLERANCE)	BOOST COMPENSATION OPTION	ILED (mA)
470k - 1M (±5%)	1	5
300k, 330k (±5%)	1	10
200k (±5%)	1	13
147k, 150k, 154k, 158k (±1%)	1	15
121k (±1%)	1	18
100k (±1%)	1	20
86.6k (±1%)	1	23
75.0k (±1%)	1	25
63.4k (±1%)	0	5
52.3k, 53.6k (±1%)	0	10
44.2k, 45.3k (±1%)	0	13
39.2k (±1%)	0	15
34.0k (±1%)	0	18
30.1k (±1%)	0	20
26.1k (±1%)	0	23
23.2k (±1%)	0	25
0 (grounded)	1	20

9.1.2 Designing With LP8557I

The LP8557I is intended for applications that can utilize an I^2C master to control the device. Use of an external PWM signal is allowed for controlling the brightness levels; however, I^2C commands are required to turn the backlight on or off. Boost switching frequency, boost compensation, PWM dimming frequency, and the maximum LED current are set to default values. Re-configuration is possible with I^2C writes; however, re-programming has to be done every time power on the VDD pin is recycled.

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9.1.2.1 Setting Boost Switching Frequency

The LP8557I boost converter switching frequency is set to 500 kHz by default. It may be re-programmed by overriding the BFREQ bit with an I²C write. Table 5 shows the boost switching frequency options available.

Table 5. Available Boost Switching Frequencies

BFREQ	f_{SW} [kHz]
0	500
1	1000

9.1.2.2 Setting Boost Compensation

For stable LP8557I boost operation, appropriate boost compensation must be selected based on the selected boost switching frequency and the boost inductance. Table 6 shows recommended boost compensation options based on the boost switching frequency and selected boost circuit inductance.

Table 6. Recommended Boost Compensation Options Based on the Boost Switching Frequency and Inductance

f_{SW} (kHz)	L (µH)	RECOMMENDED BOOST COMPENSATION OPTION
500	10 15 22	1 1 0
1000	4.7 6.8 10	1 1 0

The LP8557I boost converter compensation is set to option 1 by default. It may be re-programmed by overriding the BCOMP bit with an I²C write. Table 7 shows available boost compensation options.

Table 7. Available Boost Compensation Options

BCOMP	BOOST COMPENSATION OPTION
0	0
1	1

9.1.2.3 Setting PWM Dimming Frequency

The LP8557I PWM dimming frequency is set to 9.8 kHz by default. It may be re-programmed by overriding the PFREQ bits with an I²C write. Table 8 summarizes available PWM dimming frequencies.

Table 8. Available PWM Dimming Frequencies

PFREQ	f_{PWM} (kHz)
000	4.9
001	9.8
010	14.6
011	19.5
100	24.4
101	29.3
110	34.2
111	39.1

9.1.2.4 Setting Full-Scale LED Current

The LP8557I full-scale LED current is set to 25 mA by default. It may be re-programmed by overriding MAXCURR bits with an I²C write. Table 9 shows available full-scale LED current levels.

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Table 9. Available Full-Scale LED Currents

MAXCURR	ILED [mA]
000	5
001	10
010	13
011	15
100	18
101	20
110	23
111	25

9.2 Typical Applications

9.2.1 LP8557 PWM-Only Option

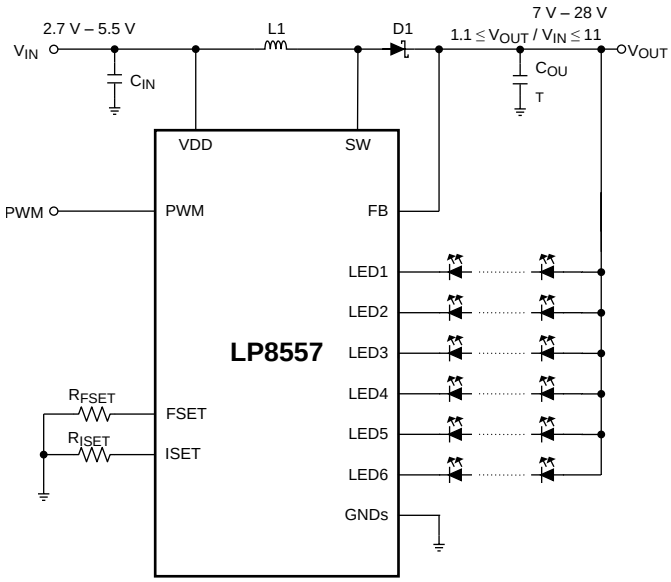

Figure 38. LP8557 PWM-Only Device Option

9.2.1.1 Design Requirements

Table 10. Recommended Inductance

	MIN	TYP	MAX	UNIT
ƒsw = 1 MHz	3.29	4.7 - 10		µH
ƒsw = 500 kHz	7	10 - 22		

Table 11. Recommended Output Capacitance(1)

	MIN	TYP	MAX	UNIT
ƒsw = 1 MHz	2			µF
ƒsw = 500 kHz	2			

(1) The recommended output capacitance is the de-rated capacitance.

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9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Boost Output Capacitor Selection

The LP8557 inductive boost converter typically requires two 4.7-µF output capacitors. The voltage rating of the capacitor must be 35 V or higher as the OVP threshold is at 29.6 V (typ). Pay careful attention to the capacitor tolerance and DC bias response. For proper operation the degradation in capacitance due to tolerance, DC bias, and temperature should stay above 2 µF. This might require placing more than two devices in parallel in order to maintain the required output capacitance over the device operating temperature and output voltage range.

9.2.1.2.2 Schottky Diode Selection

The Schottky diode must have a reverse breakdown voltage greater than the LP8557's maximum output voltage. Additionally, the diode must have an average current rating high enough to handle the LP8557 maximum output current; at the same time the diode's peak current rating must be high enough to handle the peak inductor current. Schottky diodes are required due to their lower forward voltage drop (0.3V to 0.5V) and their fast recovery time.

9.2.1.2.3 Inductor Selection

The chosen inductor must be from 10 to 22 µH (for 500-kHz operation) or 4.7 to 10 µH (for 1-MHz operation) and must have a saturation rating equal to, or greater than, the circuit's peak operating current. I_{PEAK} can be found by the following calculation:

$$I_{PEAK} = \frac{I_{OUT} \times V_{OUT}}{V_{IN} \times \text{efficiency}} + \left[\frac{V_{IN}}{2 \times f_{SW} \times L} \text{x} \left(1 - \frac{V_{IN} \times \text{efficiency}}{V_{OUT}} \right) \right] \tag{1}$$

This assumes the device is operating in continuous conduction mode (CCM) which is typically the case when operating near the peak current. For smaller rated inductors, and when the device is operating in discontinuous conduction mode (DCM), the peak current can be found from:

$$I_{PEAK} = \sqrt{\frac{2 \times I_{OUT}}{f_{SW} \times L \times \text{efficiency}} \times (V_{OUT} - V_{IN} \times \text{efficiency})} \tag{2}$$

The device operates in CCM when the following is true:

$$\frac{I_{OUT} \times V_{OUT}}{V_{IN} \times \text{efficiency}} > \frac{V_{IN}}{f_{SW} \times 2 \times L} \times \left(1 - \frac{V_{IN} \times \text{efficiency}}{V_{OUT}} \right) \tag{3}$$

9.2.1.2.4 Boost Input andVDD Capacitor Selection

The LP8557 VDD pin is typically tied to the same supply as the input of the boost power stage (V_{IN} node). A 10-µF input capacitor is recommended on that node. The voltage rating of the capacitor must be at least 10 V. If a supply powering the VDD pin is different from a supply powering the boost power stage, then 10-µF input capacitors are required on both VDD and VIN nodes.

9.2.1.3 Application Curves

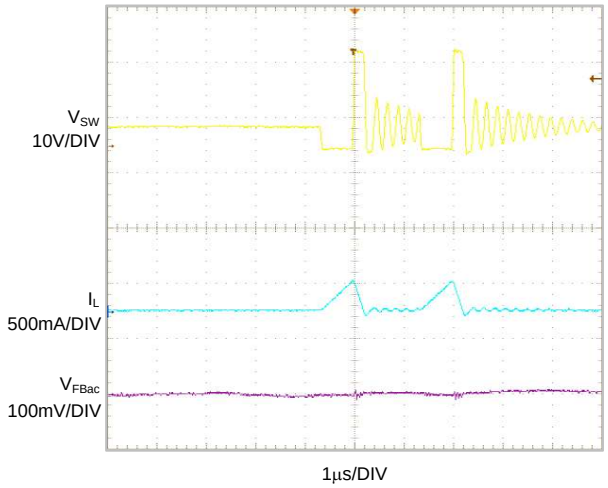

Figure 39. Steady State Operation With Light Load (200 µA/String, 6 Strings)

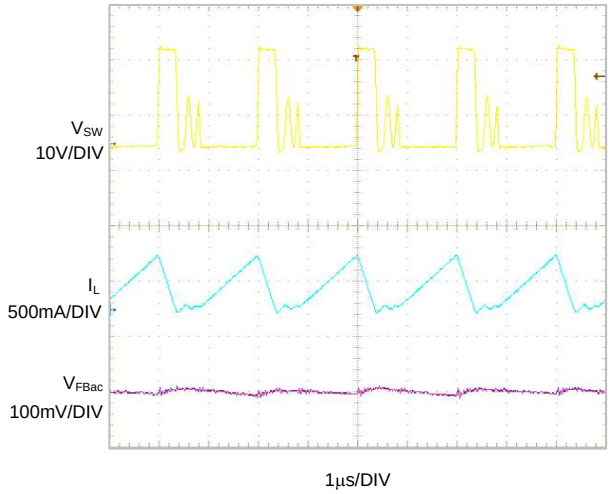

Figure 40. Steady State Operation With Medium Load (5 mA/String, 6 Strings)

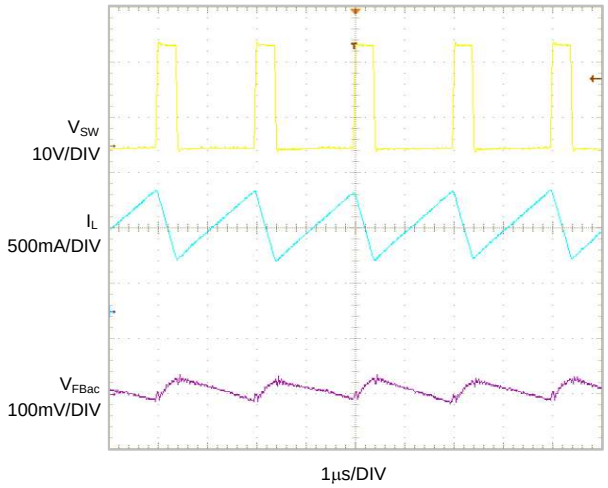

Figure 41. Steady State Operation With Heavy Load (25 mA/String, 6 Strings)

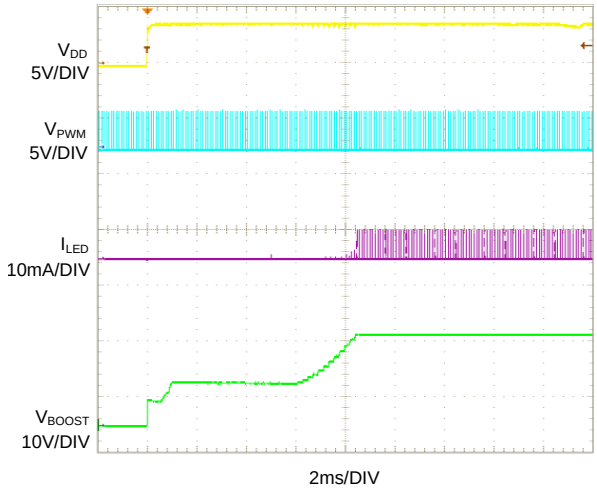

Figure 42. Start-Up With a 1% Input PWM Duty

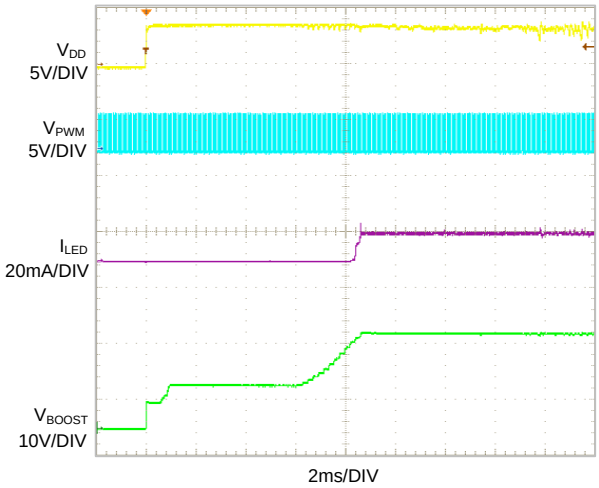

Figure 43. Start-Up With a 50% Input PWM Duty

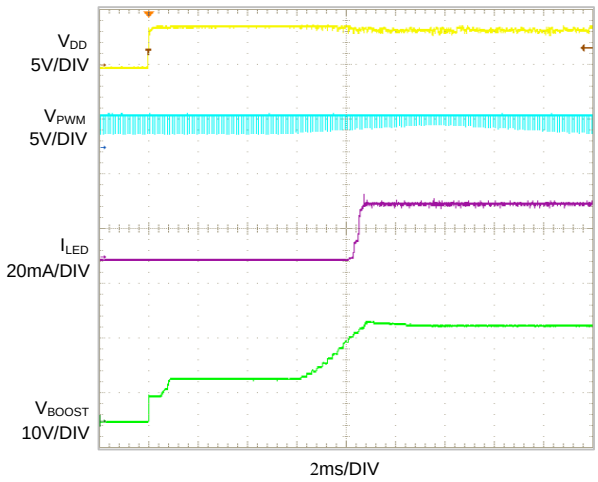

Figure 44. Start-Up With a 99% Input PWM Duty

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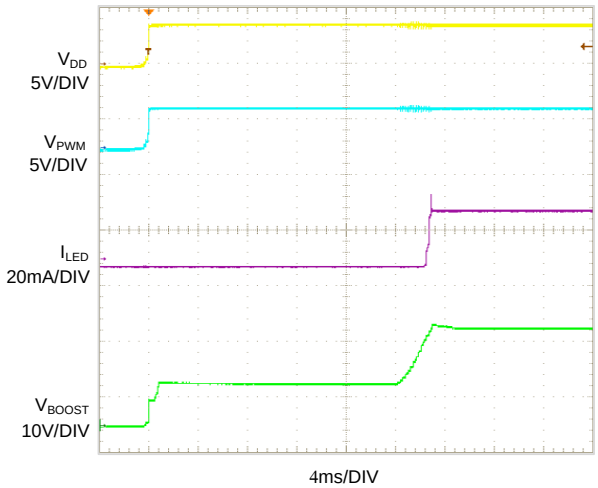

Figure 45. Start-Up With a 100% Input PWM Duty

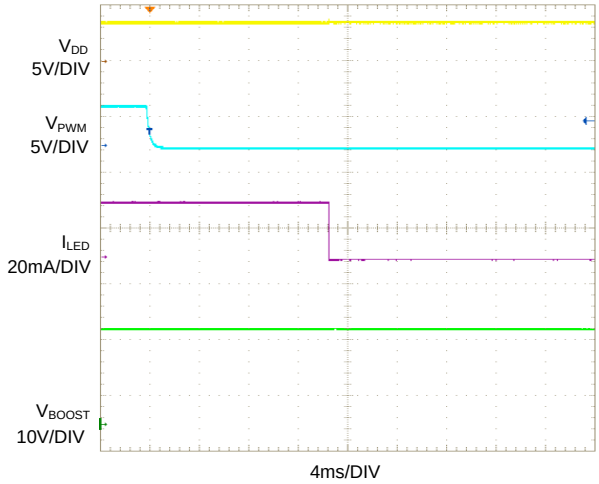

Figure 46. Shutdown Operation

9.2.2 LP8557I PWM and I²C Device Option

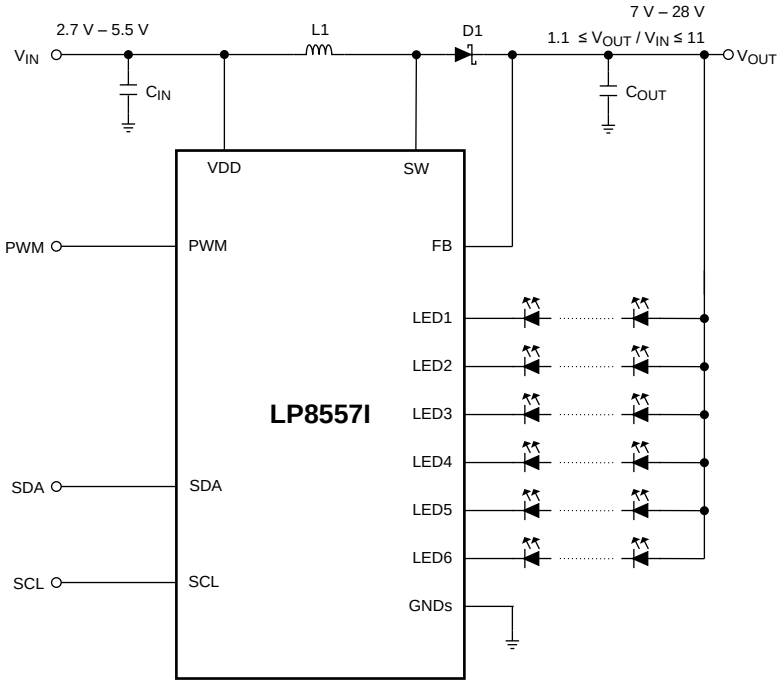

Figure 47. Typical Application With LP8557I PWM and I²C Device Option

9.2.2.1 Design Requirements

See *Design Requirements*.

9.2.2.2 Detailed Design Procedure

See *Detailed Design Procedure*.

9.2.2.3 Application Curves

See *Application Curves*.

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.7 V and 5.5 V. This input supply should be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition (start-up or rapid brightness change). The resistance of the input supply rail should be low enough that the input current transient does not cause drop high enough in the LP8557 supply voltage that can cause false UVLO fault triggering.

If the input supply is located more than a few inches from the LP8557 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. Depending on device EPROM configuration and usage case the boost converter is configured to operate optimally with certain input voltage range. Examples are seen in the *Detailed Design Procedure*. In uncertain cases, TI recommends contacting a TI sales representative for confirmation of the compatibility of the use case, EPROM configuration, and input voltage range.

11 Layout

11.1 Layout Guidelines

Figure 50 shows an example layout which applies the required proper layout guidelines to be used as a guide for laying out the LP8557 circuit.

Table 12. Application Circuit Component List

COMPONENT	MANUFACTURER	VALUE	PART NUMBER	SIZE (mm)	CURRENT/VOLTAGE RATING, RESISTANCE, TEMPERATURE
L	Cyntec	10 µH	PIME051E	5.4 × 5.2 × 1.5	2 A, 0.153 Ω
COUT	Murata	4.7 µF (×2)	GRM188R6YA475KE15D	0603 (1.6 × 0.8 × 0.8)	35 V, X5R
CIN	TDK	10 µF	C1608X5R1A106M080AC	0603 (1.6 × 0.8 × 0.8)	10 V, X5R
Diode	Rohm Semiconductor	Schottky	RB160M-40	SOD-123 (3.5 × 1.6 × 0.8)	V_R = 40 V, V_F = 0.5 V

The following guidelines apply to both LP8557 and LP8557I.

The LP8557 inductive boost converter sees a high switched voltage at the SW pin, and a step current through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling (I = C × dV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW and FB pins due to parasitic inductance in the step current conducting path (V = L × di/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise. Figure 48 highlights these two noise-generating components.

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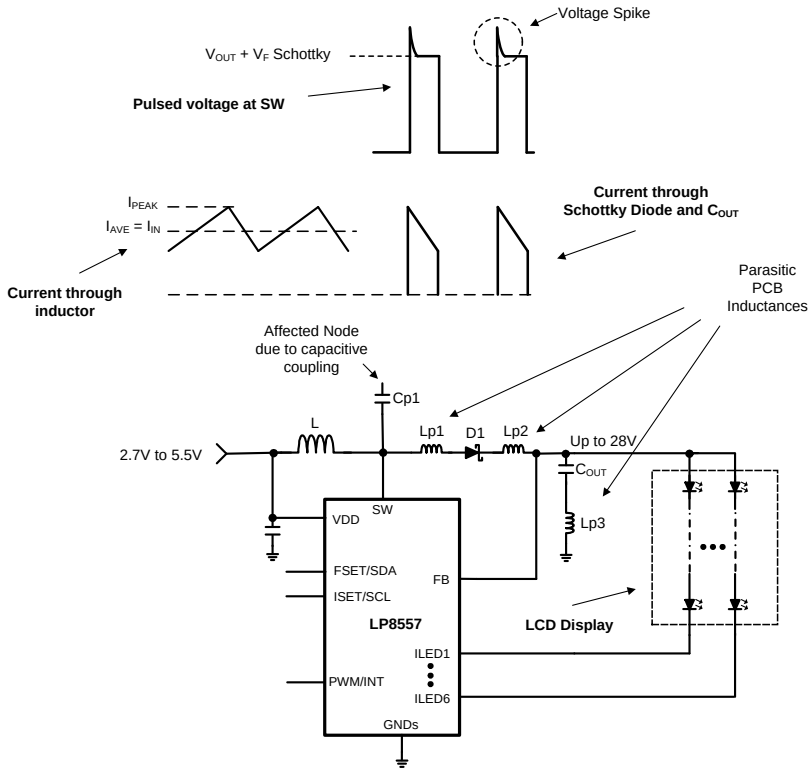

Figure 48. LP8557 Inductive Boost Converter Showing Pulsed Voltage at SW (High dv/dt) And Current Through the Schottky Diode and C_{OUT} (High di/dt)

The following list details the main (layout sensitive) areas of the LP8557's inductive boost converter in order of decreasing importance:

1. **Output Capacitor**
   - COUT+ to Schottky diode cathode connection
   - COUT– to GND bump of the LP8557 connection
2. **Schottky Diode**
   - Schottky diode anode to SW connection
   - Schottky diode cathode to COUT+ connection
3. **Inductor**
   - SW Node PCB capacitance to other traces
4. **Input Capacitor**
   - CIN+ to VDD bump connection
   - CIN– to GND connection

11.1.1 Boost Output Capacitor Placement

Because the output capacitor is in the path of the inductor current discharge path, it detects a high-current step from 0 to I_{PEAK} each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the diodes cathode, through C_{OUT}, and back into the LP8557 GND pin contributes to voltage spikes (V_{SPIKE} = LP_ × dI/dt) at SW and OUT. These spikes can potentially over-voltage the SW and FB pins, or feed through to GND. To avoid this, COUT+ must be connected as close to the cathode of the Schottky diode as possible, and COUT− must be connected as close to the LP8557 GND pins as possible. The best placement for COUT is on the same layer as the LP8557 to avoid any vias that can add excessive series inductance.

11.1.2 Schottky Diode Placement

In the LP8557's boost circuit the Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode sees a high-current step from 0 to I_{PEAK} each time the switch turns off, and the diode turns on. Any inductance in series with the diode can cause a voltage spike (V_{SPIKE} = LP_ × dI/dt) at SW and OUT. This can potentially over-voltage the SW pin, or feed through to VOUT and through the output capacitor, into GND. Connecting the anode of the diode as close to the SW pin as possible, and connecting the cathode of the diode as close to COUT+ as possible, reduces the inductance (LP_) and minimize these voltage spikes.

11.1.3 Inductor Placement

The node where the inductor connects to the LP8557 SW bump has 2 challenges. First, a large switched voltage (0 to (V_{OUT} + $V_{F_SCHOTTKY}$)) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW bump. Any resistance in this path can cause voltage drops that can negatively affect efficiency and reduce the input operating voltage range.

To reduce the capacitive coupling of the signal on SW into nearby traces, the SW bump-to-inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, high-impedance nodes that are more susceptible to electric field coupling need to be routed away from SW and not directly adjacent or beneath. This is especially true for traces such as ISET/SCL, FSET/SDA, and PWM. A GND plane placed directly below SW dramatically reduces the capacitance from SW into nearby traces.

Lastly, limit the trace resistance of the VBATT-to-inductor connection and from the inductor-to-SW connection, by use of short, wide traces.

11.1.4 Boost Input and VDD Capacitor Placement

The LP8557 input capacitor filters the inductor current ripple and the internal MOSFET driver currents. The inductor current ripple can add input voltage ripple due to any series resistance in the input power path. The MOSFET driver currents can add voltage spikes on the input due to the inductance in series with the VIN/VDD and the input capacitor. Close placement of the input capacitor to the VDD pin and to the GND pin is critical because any series inductance between VIN/VDD and CIN+ or CIN– and GND can create voltage spikes that could appear on the VIN/VDD supply line and GND.

Close placement of the input capacitor at the input side of the inductor is also critical. The source impedance (inductance and resistance) from the input supply, along with the input capacitor of the LP8557, forms a series RLC circuit. If the output resistance from the source (R_S, Figure 49) is low enough, the circuit is underdamped and has a resonant frequency (typically the case). Depending on the size of LS, the resonant frequency could occur below, close to, or above the LP8557's switching frequency. This can cause the supply current ripple to be:

1. Approximately equal to the inductor current ripple when the resonant frequency occurs well above the LP8557 switching frequency.
2. Greater than the inductor current ripple when the resonant frequency occurs near the switching frequency.
3. Less than the inductor current ripple when the resonant frequency occurs well below the switching frequency. Figure 49 shows the series RLC circuit formed from the output impedance of the supply and the input capacitor.

The circuit is redrawn for the AC case where the VIN supply is replaced with a short to GND and the LP8557 + Inductor is replaced with a current source (ΔI_L). Equation 1 is the criteria for an under-damped response. Equation 2 is the resonant frequency. Equation 3 is the approximated supply current ripple as a function of L_S, R_S, and C_{IN}.

As an example, consider a 3.8-V supply with 0.1-Ω of series resistance connected to C_{IN} (10 µF) through 50 nH of connecting traces. This results in an under-damped input-filter circuit with a resonant frequency of 225 kHz. Because both the 1-MHz and 500-kHz switching frequency options lie above the resonant frequency of the input filter, the supply current ripple is probably smaller than the inductor current ripple. In this case, using Equation 3, the supply current ripple can be approximated as 0.2 times the inductor current ripple (using a 500-kHz switching frequency) and 0.051 times the inductor current ripple using a 1-MHz switching frequency.

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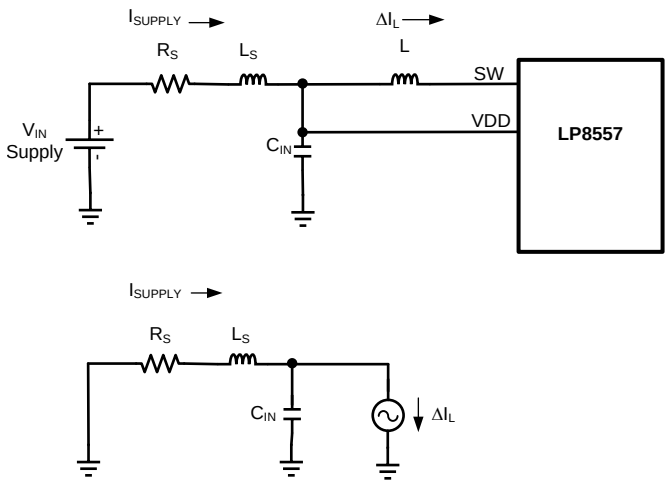

1. $$\frac{1}{L_S \times C_{IN}} > \frac{R_S^2}{4 \times L_S^2}$$

2. $$f_{RESONANT} = \frac{1}{2\pi\sqrt{L_S \times C_{IN}}}$$

3. $$I_{SUPPLYRIPPLE} \approx \Delta I_L \times \frac{\frac{1}{2\pi \times fSW \times C_{IN}}}{\sqrt{R_S^2 + \left(2\pi \times fSW \times L_S - \frac{1}{2\pi \times fSW \times C_{IN}}\right)^2}}$$

Figure 49. Input RLC Network

11.2 Layout Example

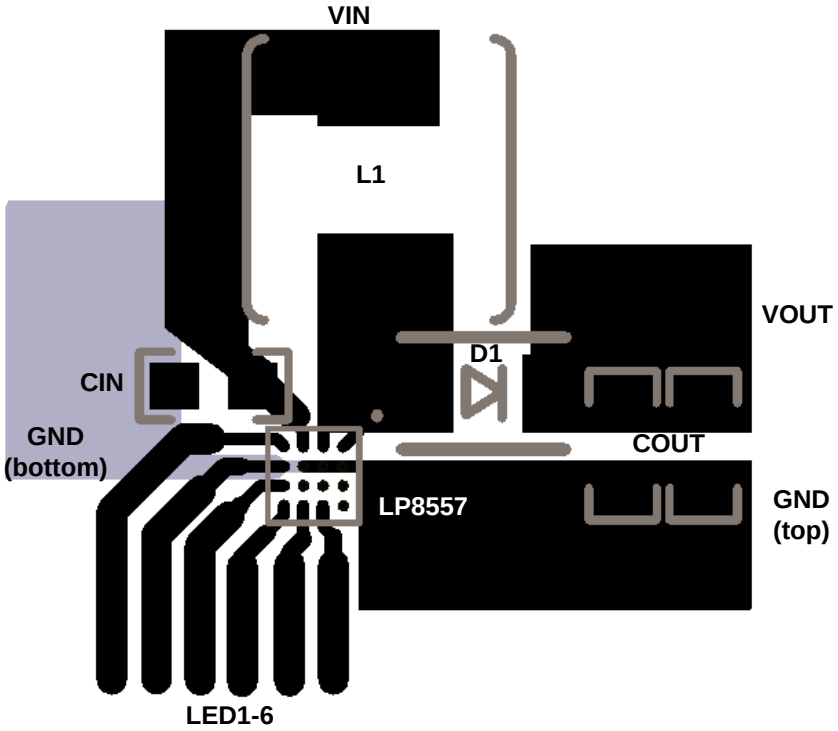

Figure 50. LP8557 and LP8557I Layout Example

Low-pass filter near VDD input pin is recommended for noisy power condition to prevent unstable LED current. 10 Ω plus approximately 2.2 µF to 10 µF can be used as low-pass filter components.

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 13. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LP8557	Click here	Click here	Click here	Click here	Click here
LP85571	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP8557AYFQR	Active	Production	DSBGA (YFQ) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D40
LP8557AYFQR.A	Active	Production	DSBGA (YFQ) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D40
LP8557AYFQR.B	Active	Production	DSBGA (YFQ) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D40
LP8557AYFQT	Active	Production	DSBGA (YFQ) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D40
LP8557AYFQT.A	Active	Production	DSBGA (YFQ) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D40
LP8557AYFQT.B	Active	Production	DSBGA (YFQ) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D40
LP8557IAYFQR	Active	Production	DSBGA (YFQ) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D41
LP8557IAYFQR.A	Active	Production	DSBGA (YFQ) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D41
LP8557IAYFQR.B	Active	Production	DSBGA (YFQ) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D41
LP8557IAYFQT	Active	Production	DSBGA (YFQ) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D41
LP8557IAYFQT.A	Active	Production	DSBGA (YFQ) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D41
LP8557IAYFQT.B	Active	Production	DSBGA (YFQ) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D41

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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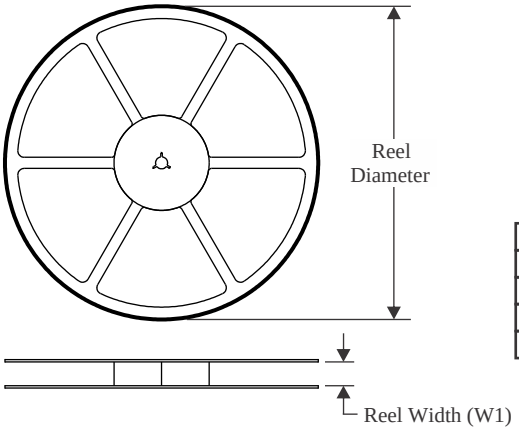
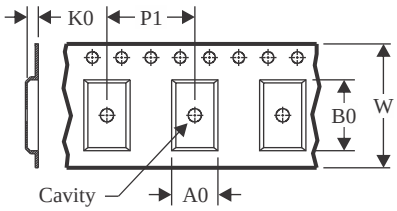
REEL DIMENSIONS

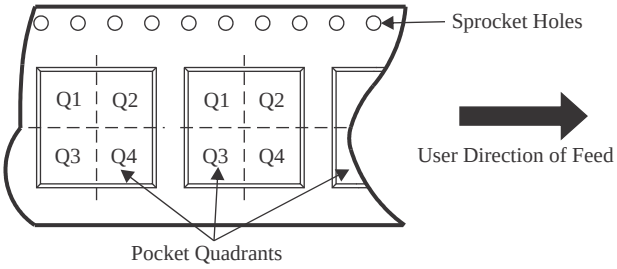


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

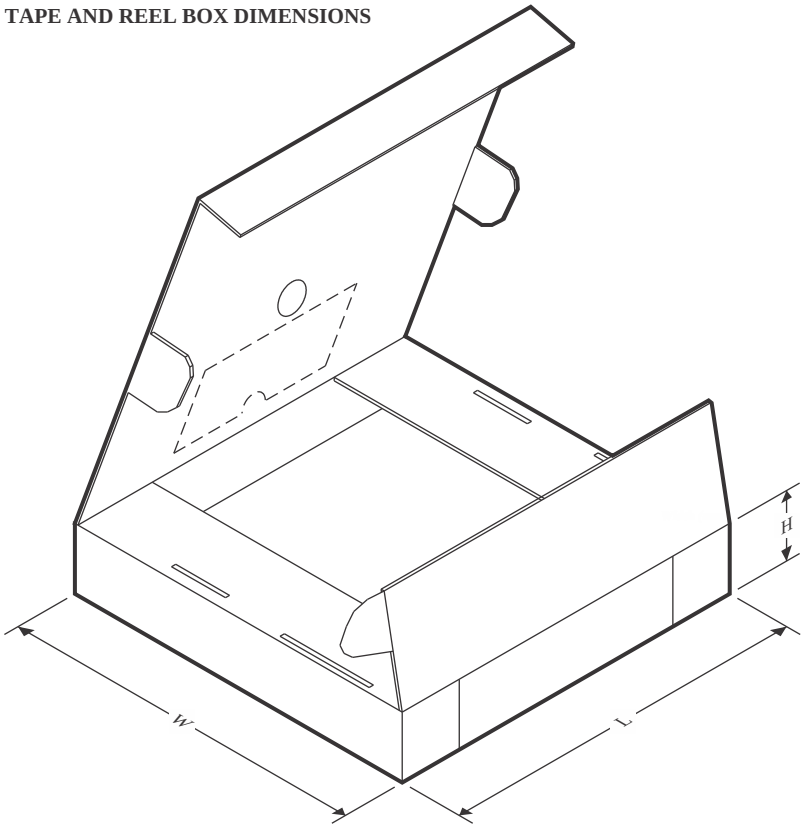
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8557AYFQR	DSBGA	YFQ	16	3000	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1
LP8557AYFQT	DSBGA	YFQ	16	250	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1
LP8557IAYFQR	DSBGA	YFQ	16	3000	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1
LP8557IAYFQT	DSBGA	YFQ	16	250	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1

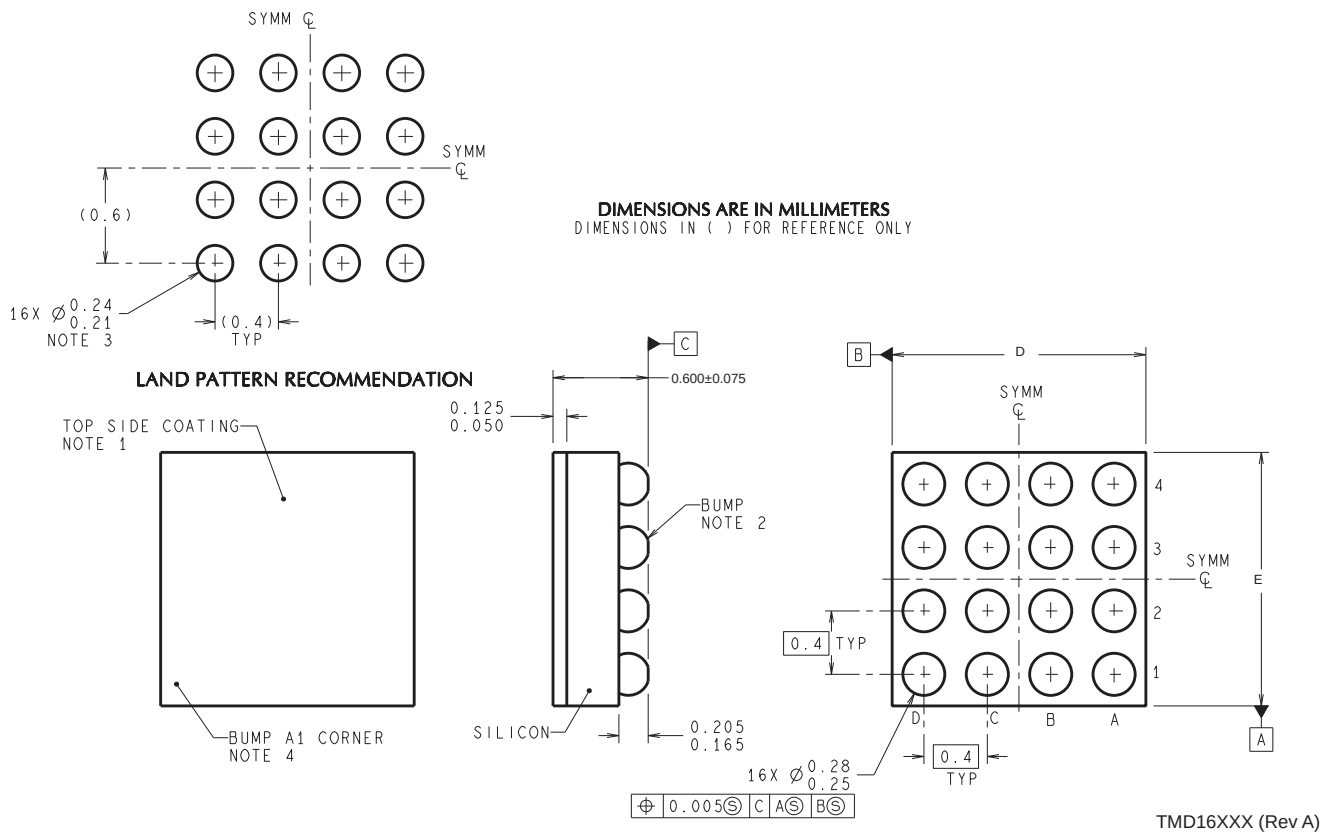
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8557AYFQR	DSBGA	YFQ	16	3000	208.0	191.0	35.0
LP8557AYFQT	DSBGA	YFQ	16	250	208.0	191.0	35.0
LP8557IAYFQR	DSBGA	YFQ	16	3000	208.0	191.0	35.0
LP8557IAYFQT	DSBGA	YFQ	16	250	208.0	191.0	35.0

YFQ0016



D: Max = 1.906 mm, Min =1.846 mm

E: Max = 1.64 mm, Min = 1.58 mm

4215081/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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