



# INA818 35- $\mu$ V Offset, 8-nV/ $\sqrt{\text{Hz}}$ Noise, Low-Power, Precision Instrumentation Amplifier

## 1 Features

- Low offset voltage: 10  $\mu$ V (typ), 35  $\mu$ V (max)
- Gain drift: 5 ppm/ $^{\circ}\text{C}$  ( $G = 1$ ), 35 ppm/ $^{\circ}\text{C}$  ( $G > 1$ ) (max)
- Noise: 8 nV/ $\sqrt{\text{Hz}}$
- Bandwidth: 2 MHz ( $G = 1$ ), 270 kHz ( $G = 100$ )
- Stable with 1-nF capacitive loads
- Inputs protected up to  $\pm 60$  V
- Common-mode rejection: 110 dB,  $G = 10$  (min)
- Power-supply rejection: 100 dB,  $G = 1$  (min)
- Supply current: 385  $\mu$ A (max)
- Supply voltage range:
  - Single supply: 4.5 V to 36 V
  - Dual supply:  $\pm 2.25$  V to  $\pm 18$  V
- Specified temperature:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package: 8-pin SOIC

## 2 Applications

- Industrial monitors
- Flow transmitters
- Battery test equipment
- Multiparameter patient monitors
- Analog input modules
- Semiconductor test equipment
- Portable instrumentation

## 3 Description

The INA818 is a high-precision instrumentation amplifier that offers low power consumption and operates over a very wide single-supply or dual-supply range. A single external resistor sets any gain from 1 to 10000. The device offers high precision as a result of super-beta input transistors, which provide exceptionally low input offset voltage, offset voltage drift, input bias current, input voltage, and current noise. Additional circuitry protects the inputs against overvoltage up to  $\pm 60$  V.

The INA818 is optimized to provide a high common-mode rejection ratio. At  $G = 1$ , the common-mode rejection ratio exceeds 90 dB across the full input common-mode range. The device is designed for low-voltage operation from a 4.5-V single supply, as well as dual supplies up to  $\pm 18$  V.

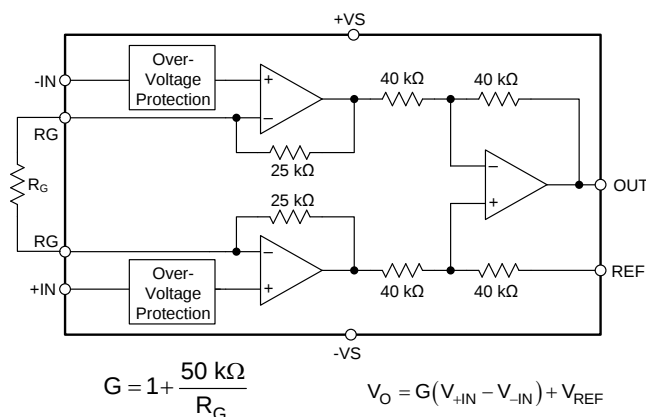
The INA818 is available in an 8-pin SOIC package and is specified over the  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range.

### Device Information<sup>(1)</sup>

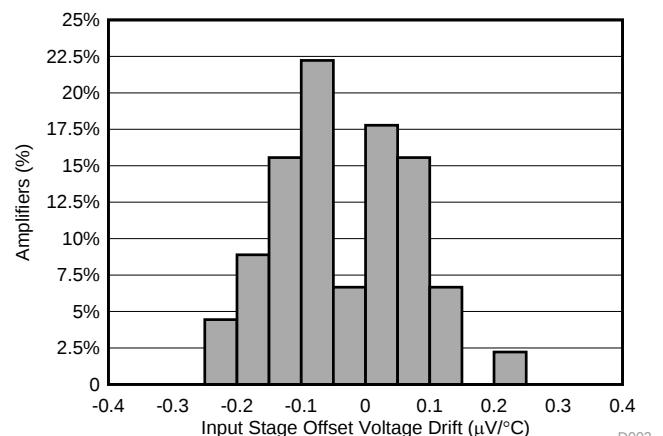
| PART NUMBER | PACKAGE  | BODY SIZE (NOM)          |
|-------------|----------|--------------------------|
| INA818      | SOIC (8) | 4.90 mm $\times$ 3.91 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.

### INA818 Simplified Internal Schematic



### Typical Distribution of Input Stage Offset Voltage Drift



D002



## Table of Contents

|                                                    |           |                                                                  |           |
|----------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                            | <b>1</b>  | 8.3 Feature Description .....                                    | 20        |
| <b>2 Applications</b> .....                        | <b>1</b>  | 8.4 Device Functional Modes .....                                | 26        |
| <b>3 Description</b> .....                         | <b>1</b>  | <b>9 Application and Implementation</b> .....                    | <b>26</b> |
| <b>4 Revision History</b> .....                    | <b>2</b>  | 9.1 Application Information .....                                | 26        |
| <b>5 Device Comparison Table</b> .....             | <b>3</b>  | 9.2 Typical Applications .....                                   | 29        |
| <b>6 Pin Configuration and Functions</b> .....     | <b>4</b>  | <b>10 Power Supply Recommendations</b> .....                     | <b>32</b> |
| <b>7 Specifications</b> .....                      | <b>5</b>  | <b>11 Layout</b> .....                                           | <b>32</b> |
| 7.1 Absolute Maximum Ratings .....                 | 5         | 11.1 Layout Guidelines .....                                     | 32        |
| 7.2 ESD Ratings .....                              | 5         | 11.2 Layout Example .....                                        | 33        |
| 7.3 Recommended Operating Conditions .....         | 5         | <b>12 Device and Documentation Support</b> .....                 | <b>34</b> |
| 7.4 Thermal Information .....                      | 5         | 12.1 Documentation Support .....                                 | 34        |
| 7.5 Electrical Characteristics .....               | 6         | 12.2 Receiving Notification of Documentation Updates .....       | 34        |
| 7.6 Typical Characteristics: Table of Graphs ..... | 8         | 12.3 Community Resources .....                                   | 34        |
| 7.7 Typical Characteristics .....                  | 10        | 12.4 Trademarks .....                                            | 34        |
| <b>8 Detailed Description</b> .....                | <b>19</b> | 12.5 Electrostatic Discharge Caution .....                       | 34        |
| 8.1 Overview .....                                 | 19        | 12.6 Glossary .....                                              | 34        |
| 8.2 Functional Block Diagram .....                 | 19        | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | <b>34</b> |

## 4 Revision History

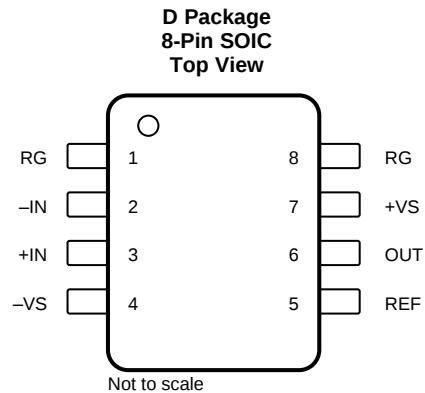
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (April 2019) to Revision A                            | Page     |
|-----------------------------------------------------------------------------|----------|
| • Changed document status from Advance Information to Production Data ..... | <b>1</b> |

## 5 Device Comparison Table

| DEVICE                 | DESCRIPTION                                                                                                               | GAIN EQUATION                        | RG PINS AT PIN |
|------------------------|---------------------------------------------------------------------------------------------------------------------------|--------------------------------------|----------------|
| <a href="#">INA818</a> | 35-μV Offset, 0.4 μV/°C V <sub>OS</sub> Drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier             | $G = 1 + 50 \text{ k}\Omega / R_G$   | 1, 8           |
| <a href="#">INA819</a> | 35-μV Offset, 0.4 μV/°C V <sub>OS</sub> Drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier             | $G = 1 + 50 \text{ k}\Omega / R_G$   | 2, 3           |
| <a href="#">INA821</a> | 35-μV Offset, 0.4 μV/°C V <sub>OS</sub> Drift, 7-nV/√Hz Noise, High-Bandwidth, Precision Instrumentation Amplifier        | $G = 1 + 49.4 \text{ k}\Omega / R_G$ | 2, 3           |
| <a href="#">INA828</a> | 50-μV Offset, 0.5 μV/°C V <sub>OS</sub> Drift, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier             | $G = 1 + 50 \text{ k}\Omega / R_G$   | 1, 8           |
| <a href="#">INA333</a> | 25-μV V <sub>OS</sub> , 0.1 μV/°C V <sub>OS</sub> Drift, 1.8-V to 5-V, RRO, 50-μA I <sub>Q</sub> , Chopper-Stabilized INA | $G = 1 + 100 \text{ k}\Omega / R_G$  | 1, 8           |
| <a href="#">PGA280</a> | 20-mV to ±10-V Programmable Gain IA With 3-V or 5-V Differential Output; Analog Supply up to ±18 V                        | Digital programmable                 | N/A            |
| <a href="#">INA159</a> | G = 0.2 V Differential Amplifier for ±10-V to 3-V and 5-V Conversion                                                      | $G = 0.2 \text{ V/V}$                | N/A            |
| <a href="#">PGA112</a> | Precision Programmable Gain Op Amp With SPI                                                                               | Digital programmable                 | N/A            |

## 6 Pin Configuration and Functions



### Pin Functions

| PIN  |      | I/O | DESCRIPTION                                                         |
|------|------|-----|---------------------------------------------------------------------|
| NAME | NO.  |     |                                                                     |
| -IN  | 2    | I   | Negative (inverting) input                                          |
| +IN  | 3    | I   | Positive (noninverting) input                                       |
| OUT  | 6    | O   | Output                                                              |
| REF  | 5    | I   | Reference input. This pin must be driven by a low-impedance source. |
| RG   | 1, 8 | —   | Gain setting pin. Place a gain resistor between pin 1 and pin 8.    |
| -VS  | 4    | —   | Negative supply                                                     |
| +VS  | 7    | —   | Positive supply                                                     |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                   | MIN              | MAX                 | UNIT |
|---------------------------------------------------|------------------|---------------------|------|
| Supply voltage dual supply, $V_S = (V+) - (V-)$   |                  | ±20                 | V    |
| Supply voltage single supply, $V_S = (V+) - (V-)$ |                  | 40, (single supply) | V    |
| Signal input pins                                 | –60              | 60                  | V    |
| VREF pin                                          | –20              | 20                  | V    |
| Signal output pins maximum voltage                | (– $V_S$ ) – 0.5 | (+ $V_S$ ) + 0.5    | V    |
| Signal output pins maximum current                | –50              | 50                  | mA   |
| Output short-circuit <sup>(2)</sup>               | Continuous       |                     |      |
| Operating Temperature, $T_A$                      | –50              | 150                 | °C   |
| Junction Temperature, $T_J$                       |                  | 175                 |      |
| Storage Temperature, $T_{stg}$                    | –65              | 150                 |      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to  $V_S / 2$ .

### 7.2 ESD Ratings

|             |                         | VALUE                                                                          | UNIT  |
|-------------|-------------------------|--------------------------------------------------------------------------------|-------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±1500 |
|             |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±750  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                       |                       | MIN   | MAX | UNIT |
|-----------------------|-----------------------|-------|-----|------|
| Supply voltage $V_S$  | Single-supply         | 4.5   | 36  | V    |
|                       | Dual-supply           | ±2.25 | ±18 |      |
| Specified temperature | Specified temperature | –40   | 125 | °C   |

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | INA818   | UNIT |
|-------------------------------|----------------------------------------------|----------|------|
|                               |                                              | D (SOIC) |      |
|                               |                                              | 8 PINS   |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 119.6    | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 66.3     | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 61.9     | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 20.5     | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 61.4     | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A      | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{\text{REF}} = 0\text{ V}$ , and  $G = 1$  (unless otherwise noted)

| PARAMETER        |                                               | TEST CONDITIONS                                                           | MIN                                                        | TYP                           | MAX      | UNIT             |
|------------------|-----------------------------------------------|---------------------------------------------------------------------------|------------------------------------------------------------|-------------------------------|----------|------------------|
| INPUT            |                                               |                                                                           |                                                            |                               |          |                  |
| V <sub>OSI</sub> | Input stage offset voltage <sup>(1)(2)</sup>  |                                                                           |                                                            | 10                            | 35       | μV               |
|                  |                                               | T <sub>A</sub> = −40°C to 125°C <sup>(3)</sup>                            |                                                            |                               | 75       | μV               |
|                  |                                               | drift vs temperature, T <sub>A</sub> = −40°C to 125°C                     |                                                            |                               | 0.4      | μV/°C            |
| V <sub>OSO</sub> | Output stage offset voltage <sup>(1)(2)</sup> |                                                                           |                                                            | 50                            | 300      | μV               |
|                  |                                               | T <sub>A</sub> = −40°C to 125°C <sup>(3)</sup>                            |                                                            |                               | 800      | μV               |
|                  |                                               | drift vs temperature, T <sub>A</sub> = −40°C to 125°C                     |                                                            |                               | 5        | μV/°C            |
| PSRR             | Power-supply rejection ratio                  | G = 1, RTI                                                                | 110                                                        | 120                           |          | dB               |
|                  |                                               | G = 10, RTI                                                               | 114                                                        | 130                           |          |                  |
|                  |                                               | G = 100, RTI                                                              | 130                                                        | 135                           |          |                  |
|                  |                                               | G = 1000, RTI                                                             | 136                                                        | 140                           |          |                  |
| Z <sub>id</sub>  | Differential impedance                        |                                                                           |                                                            | 100    1                      |          | GΩ    pF         |
| Z <sub>ic</sub>  | Common-mode impedance                         |                                                                           |                                                            | 100    4                      |          | GΩ    pF         |
|                  | RFI filter, −3-dB frequency                   |                                                                           |                                                            | 32                            |          | MHz              |
| V <sub>CM</sub>  | Operating input range <sup>(4)</sup>          |                                                                           | (V−) + 2                                                   |                               | (V+) − 2 | V                |
|                  |                                               | V <sub>S</sub> = ±2.25 V to ±18 V, T <sub>A</sub> = −40°C to 125°C        | See <a href="#">Figure 51</a> to <a href="#">Figure 54</a> |                               |          |                  |
|                  | Input overvoltage range                       | T <sub>A</sub> = −40°C to 125°C <sup>(3)</sup>                            |                                                            |                               | ±60      | V                |
| CMRR             | Common-mode rejection ratio                   | At DC to 60 Hz, RTI, V <sub>CM</sub> = (V−) + 2 V to (V+) − 2 V, G = 1    | 90                                                         | 105                           |          | dB               |
|                  |                                               | At DC to 60 Hz, RTI, V <sub>CM</sub> = (V−) + 2 V to (V+) − 2 V, G = 10   | 110                                                        | 125                           |          |                  |
|                  |                                               | At DC to 60 Hz, RTI, V <sub>CM</sub> = (V−) + 2 V to (V+) − 2 V, G = 100  | 130                                                        | 145                           |          |                  |
|                  |                                               | At DC to 60 Hz, RTI, V <sub>CM</sub> = (V−) + 2 V to (V+) − 2 V, G = 1000 | 140                                                        | 150                           |          |                  |
| BIAS CURRENT     |                                               |                                                                           |                                                            |                               |          |                  |
| I <sub>B</sub>   | Input bias current                            | V <sub>CM</sub> = V <sub>S</sub> / 2                                      |                                                            | 0.15                          | 0.5      | nA               |
|                  |                                               | T <sub>A</sub> = −40°C to 125°C                                           |                                                            |                               | 2        |                  |
| I <sub>OS</sub>  | Input offset current                          | V <sub>CM</sub> = V <sub>S</sub> / 2                                      |                                                            | 0.15                          | 0.5      | nA               |
|                  |                                               | T <sub>A</sub> = −40°C to 125°C                                           |                                                            |                               | 2        |                  |
| NOISE VOLTAGE    |                                               |                                                                           |                                                            |                               |          |                  |
| e <sub>NI</sub>  | Input stage voltage noise <sup>(5)</sup>      | f = 1 kHz, G = 100, R <sub>S</sub> = 0 Ω                                  |                                                            | 8                             |          | nV/√Hz           |
|                  |                                               | f <sub>B</sub> = 0.1 Hz to 10 Hz, G = 100, R <sub>S</sub> = 0 Ω           |                                                            | 0.19                          |          | μV <sub>PP</sub> |
| e <sub>NO</sub>  | Output stage voltage noise <sup>(5)</sup>     | f = 1 kHz, R <sub>S</sub> = 0 Ω                                           |                                                            | 80                            |          | nV/√Hz           |
|                  |                                               | f <sub>B</sub> = 0.1 Hz to 10 Hz, R <sub>S</sub> = 0 Ω                    |                                                            | 2.6                           |          | μV <sub>PP</sub> |
| I <sub>n</sub>   | Noise current                                 | f = 1 kHz                                                                 |                                                            | 130                           |          | fA/√Hz           |
|                  |                                               | f <sub>B</sub> = 0.1 Hz to 10 Hz, G = 100                                 |                                                            | 4.7                           |          | pA <sub>PP</sub> |
| GAIN             |                                               |                                                                           |                                                            |                               |          |                  |
|                  | Gain equation                                 |                                                                           |                                                            | 1 + (50 kΩ / R <sub>G</sub> ) |          | V/V              |
| G                | Gain                                          |                                                                           | 1                                                          |                               | 1000     | V/V              |
| GE               | Gain error                                    | G = 1, V <sub>O</sub> = ±10 V                                             |                                                            | ±0.005%                       | ±0.025%  |                  |
|                  |                                               | G = 10, V <sub>O</sub> = ±10 V                                            |                                                            | ±0.025%                       | ±0.15%   |                  |
|                  |                                               | G = 100, V <sub>O</sub> = ±10 V                                           |                                                            | ±0.025%                       | ±0.15%   |                  |
|                  |                                               | G = 1000, V <sub>O</sub> = ±10 V                                          |                                                            | ±0.05%                        |          |                  |
|                  | Gain error drift <sup>(6)</sup>               | G = 1, T <sub>A</sub> = −40°C to 125°C, V <sub>O</sub> = ±10 V            |                                                            |                               | ±5       | ppm/°C           |
|                  |                                               | G > 1, T <sub>A</sub> = −40°C to 125°C, V <sub>O</sub> = ±10 V            |                                                            |                               | ±35      |                  |

(1) Total offset, referred-to-input (RTI):  $V_{\text{OS}} = (V_{\text{OSI}}) + (V_{\text{OSO}} / G)$ .

(2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using:  $\Delta V_{\text{OS(RTI)}} = \sqrt{[\Delta V_{\text{OSI}}]^2 + (\Delta V_{\text{OSO}} / G)^2}$

(3) Specified by characterization.

(4) Input voltage range of the INA818 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves Figure 51 through Figure 54 for more information.

(5) Total RTI voltage noise is equal to:  $e_{\text{N(RTI)}} = \sqrt{[e_{\text{NI}}]^2 + (e_{\text{NO}} / G)^2}$

(6) The values specified for  $G > 1$  do not include the effects of the external gain-setting resistor,  $R_{\text{G}}$ .

## Electrical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = 0\text{ V}$ , and  $G = 1$  (unless otherwise noted)

| PARAMETER          |                              | TEST CONDITIONS                                                     | MIN         | TYP         | MAX | UNIT |
|--------------------|------------------------------|---------------------------------------------------------------------|-------------|-------------|-----|------|
|                    | Gain nonlinearity            | G = 1 to 10, V <sub>O</sub> = −10 V to 10 V, R <sub>L</sub> = 10 kΩ |             | 1           | 10  | ppm  |
|                    |                              | G = 100, V <sub>O</sub> = −10 V to 10 V, R <sub>L</sub> = 10 kΩ     |             |             | 15  |      |
|                    |                              | G = 1000, V <sub>O</sub> = −10 V to 10 V, R <sub>L</sub> = 10 kΩ    |             | 10          |     |      |
|                    |                              | G = 1 to 100, V <sub>O</sub> = −10 V to 10 V, R <sub>L</sub> = 2 kΩ |             | 30          |     |      |
| OUTPUT             |                              |                                                                     |             |             |     |      |
|                    | Voltage swing                |                                                                     | (V−) + 0.15 | (V+) − 0.15 |     | V    |
|                    | Load capacitance stability   |                                                                     |             | 1000        |     | pF   |
| Z <sub>O</sub>     | Closed-loop output impedance | f = 10 kHz                                                          |             | 5.0         |     | Ω    |
| I <sub>SC</sub>    | Short-circuit current        | Continuous to V <sub>S</sub> / 2                                    |             | ±20         |     | mA   |
| FREQUENCY RESPONSE |                              |                                                                     |             |             |     |      |
| BW                 | Bandwidth, −3 dB             | G = 1                                                               |             | 2.0         |     | MHz  |
|                    |                              | G = 10                                                              |             | 890         |     | kHz  |
|                    |                              | G = 100                                                             |             | 270         |     |      |
|                    |                              | G = 1000                                                            |             | 30          |     |      |
| SR                 | Slew rate                    | G = 1, V <sub>O</sub> = ±10 V                                       |             | 0.9         |     | V/μs |
| t <sub>S</sub>     | Settling time                | 0.01%, G = 1 to 100, V <sub>STEP</sub> = 10 V                       |             | 12          |     | μs   |
|                    |                              | 0.01%, G = 1000, V <sub>STEP</sub> = 10 V                           |             | 40          |     |      |
|                    |                              | 0.001%, G = 1 to 100, V <sub>STEP</sub> = 10 V                      |             | 16          |     |      |
|                    |                              | 0.001%, G = 1000, V <sub>STEP</sub> = 10 V                          |             | 60          |     |      |
| REFERENCE INPUT    |                              |                                                                     |             |             |     |      |
| R <sub>IN</sub>    | Input impedance              |                                                                     |             | 40          |     | kΩ   |
|                    | Voltage range                |                                                                     | (V−)        | (V+)        |     | V    |
|                    | Gain to output               |                                                                     |             | 1           |     | V/V  |
|                    | Reference gain error         |                                                                     |             | 0.01%       |     |      |
| POWER SUPPLY       |                              |                                                                     |             |             |     |      |
| I <sub>Q</sub>     | Quiescent current            | V <sub>IN</sub> = 0 V                                               |             | 350         | 385 | μA   |
|                    |                              | V <sub>IN</sub> = 0 V, T <sub>A</sub> = −40°C to 125°C              |             |             | 520 |      |

## 7.6 Typical Characteristics: Table of Graphs

**Table 1. Table of Graphs**

| DESCRIPTION                                                           | FIGURE                    |
|-----------------------------------------------------------------------|---------------------------|
| Typical Distribution of Input Stage Offset Voltage                    | <a href="#">Figure 1</a>  |
| Typical Distribution of Input Stage Offset Voltage Drift              | <a href="#">Figure 2</a>  |
| Typical Distribution of Output Stage Offset Voltage                   | <a href="#">Figure 3</a>  |
| Typical Distribution of Output Stage Offset Voltage Drift             | <a href="#">Figure 4</a>  |
| Input Stage Offset Voltage vs Temperature                             | <a href="#">Figure 5</a>  |
| Output Stage Offset Voltage vs Temperature                            | <a href="#">Figure 6</a>  |
| Typical Distribution of Input Bias Current $T_A = 25^{\circ}\text{C}$ | <a href="#">Figure 7</a>  |
| Typical Distribution of Input Bias Current $T_A = 90^{\circ}\text{C}$ | <a href="#">Figure 8</a>  |
| Typical Distribution of Input Offset Current                          | <a href="#">Figure 9</a>  |
| Input Bias Current vs Temperature                                     | <a href="#">Figure 10</a> |
| Input Offset Current vs Temperature                                   | <a href="#">Figure 11</a> |
| Typical CMRR Distribution $G = 1$                                     | <a href="#">Figure 12</a> |
| Typical CMRR Distribution $G = 10$                                    | <a href="#">Figure 13</a> |
| CMRR vs Temperature $G = 1$                                           | <a href="#">Figure 14</a> |
| CMRR vs Temperature $G = 10$                                          | <a href="#">Figure 15</a> |
| Input Current vs Input Overvoltage                                    | <a href="#">Figure 16</a> |
| CMRR vs Frequency (RTI)                                               | <a href="#">Figure 17</a> |
| CMRR vs Frequency (RTI, 1-k $\Omega$ source imbalance)                | <a href="#">Figure 18</a> |
| Positive PSRR vs Frequency (RTI)                                      | <a href="#">Figure 19</a> |
| Negative PSRR vs Frequency (RTI)                                      | <a href="#">Figure 20</a> |
| Gain vs Frequency                                                     | <a href="#">Figure 21</a> |
| Voltage Noise Spectral Density vs Frequency (RTI)                     | <a href="#">Figure 22</a> |
| Current Noise Spectral Density vs Frequency (RTI)                     | <a href="#">Figure 23</a> |
| 0.1-Hz to 10-Hz RTI Voltage Noise $G = 1$                             | <a href="#">Figure 24</a> |
| 0.1-Hz to 10-Hz RTI Voltage Noise $G = 1000$                          | <a href="#">Figure 25</a> |
| 0.1-Hz to 10-Hz RTI Current Noise                                     | <a href="#">Figure 26</a> |
| Typical Distribution of Gain Error $G = 1$                            | <a href="#">Figure 28</a> |
| Typical Distribution of Gain Error $G = 10$                           | <a href="#">Figure 29</a> |
| Input Bias Current vs Common-Mode Voltage                             | <a href="#">Figure 27</a> |
| Gain Error vs Temperature $G = 1$                                     | <a href="#">Figure 30</a> |
| Gain Error vs Temperature $G = 10$                                    | <a href="#">Figure 31</a> |
| Supply Current vs Temperature                                         | <a href="#">Figure 32</a> |
| Gain Nonlinearity $G = 1$                                             | <a href="#">Figure 33</a> |
| Gain Nonlinearity $G = 10$                                            | <a href="#">Figure 34</a> |
| Offset Voltage vs Negative Common-Mode Voltage                        | <a href="#">Figure 35</a> |
| Offset Voltage vs Positive Common-Mode Voltage                        | <a href="#">Figure 36</a> |
| Positive Output Voltage Swing vs Output Current                       | <a href="#">Figure 37</a> |
| Negative Output Voltage Swing vs Output Current                       | <a href="#">Figure 38</a> |
| Short Circuit Current vs Temperature                                  | <a href="#">Figure 39</a> |
| Large-Signal Frequency Response                                       | <a href="#">Figure 40</a> |
| THD+N vs Frequency                                                    | <a href="#">Figure 41</a> |
| Overshoot vs Capacitive Loads                                         | <a href="#">Figure 42</a> |
| Small-Signal Response $G = 1$                                         | <a href="#">Figure 43</a> |
| Small-Signal Response $G = 10$                                        | <a href="#">Figure 44</a> |
| Small-Signal Response $G = 100$                                       | <a href="#">Figure 45</a> |
| Small-Signal Response $G = 1000$                                      | <a href="#">Figure 46</a> |

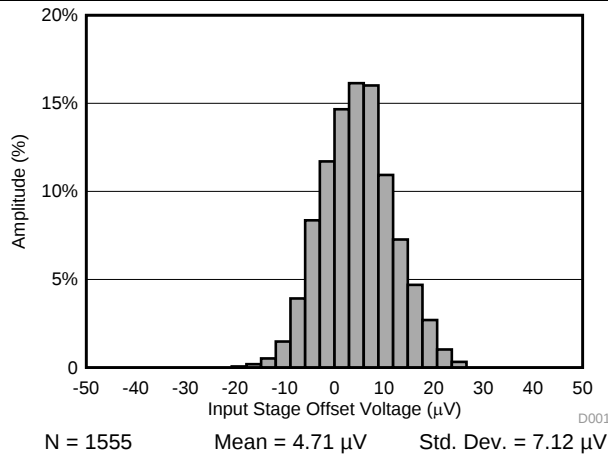
## Typical Characteristics: Table of Graphs (continued)

**Table 1. Table of Graphs (continued)**

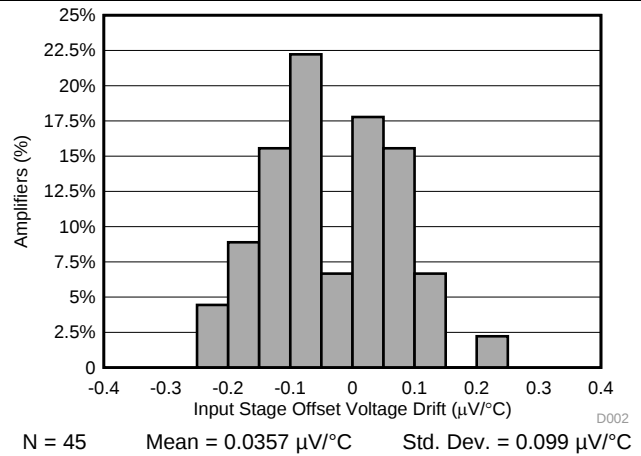
| DESCRIPTION                                                                | FIGURE                    |
|----------------------------------------------------------------------------|---------------------------|
| Large Signal Step Response                                                 | <a href="#">Figure 47</a> |
| Closed-Loop Output Impedance                                               | <a href="#">Figure 48</a> |
| Differential-Mode EMI Rejection Ratio                                      | <a href="#">Figure 49</a> |
| Common-Mode EMI Rejection Ratio                                            | <a href="#">Figure 50</a> |
| Input Common-Mode Voltage vs Output Voltage $G = 1$ , $V_S = 5\text{ V}$   | <a href="#">Figure 51</a> |
| Input Common-Mode Voltage vs Output Voltage $G = 100$ , $V_S = 5\text{ V}$ | <a href="#">Figure 52</a> |
| Input Common-Mode Voltage vs Output Voltage $V_S = \pm 5\text{ V}$         | <a href="#">Figure 53</a> |
| Input Common-Mode Voltage vs Output Voltage $V_S = \pm 15\text{ V}$        | <a href="#">Figure 54</a> |

## 7.7 Typical Characteristics

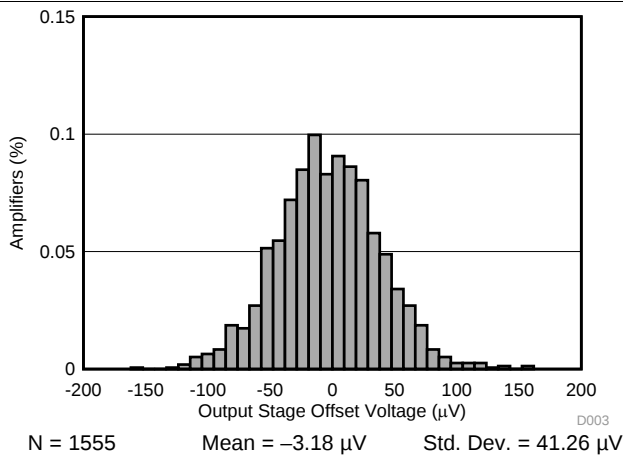
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{\text{REF}} = 0\text{ V}$ , and  $G = 1$  (unless otherwise noted)



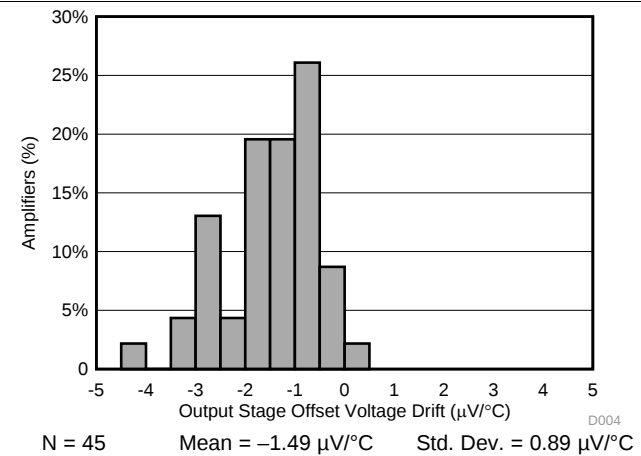
**Figure 1. Typical Distribution of Input Stage Offset Voltage**



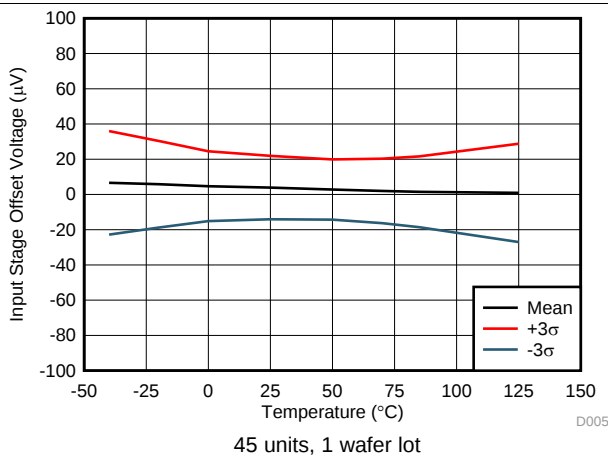
**Figure 2. Typical Distribution of Input Stage Offset Voltage Drift**



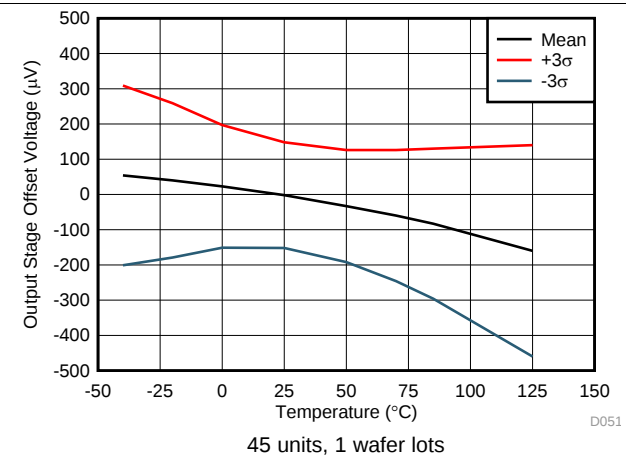
**Figure 3. Typical Distribution of Output Stage Offset Voltage**



**Figure 4. Typical Distribution of Output Stage Offset Voltage Drift**



**Figure 5. Input Stage Offset Voltage vs Temperature**



**Figure 6. Output Stage Offset Voltage vs Temperature**

## Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{\text{REF}} = 0\text{ V}$ , and  $G = 1$  (unless otherwise noted)

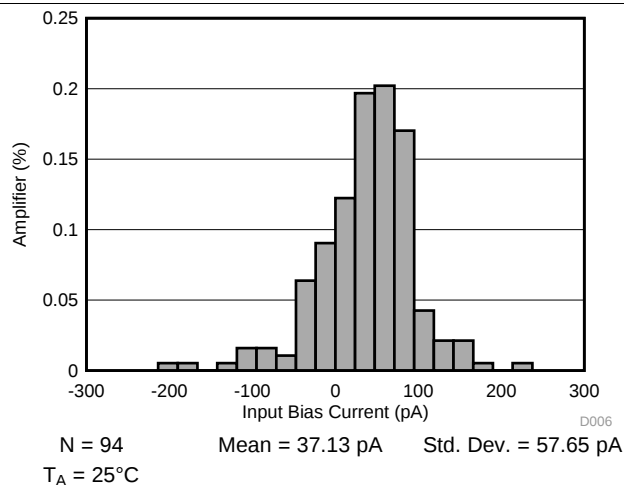


Figure 7. Typical Distribution of Input Bias Current

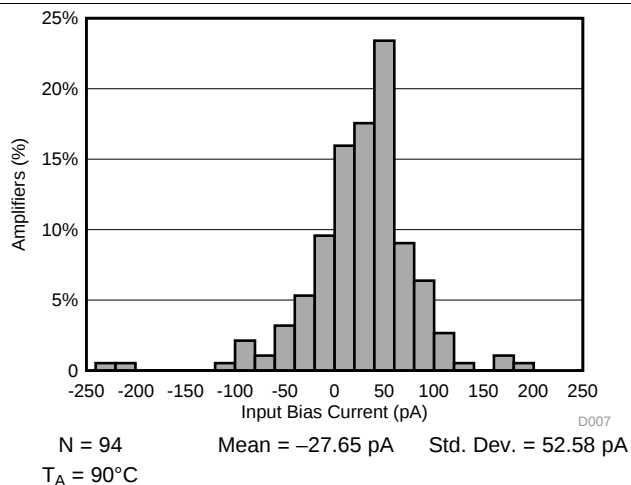


Figure 8. Typical Distribution of Input Bias Current

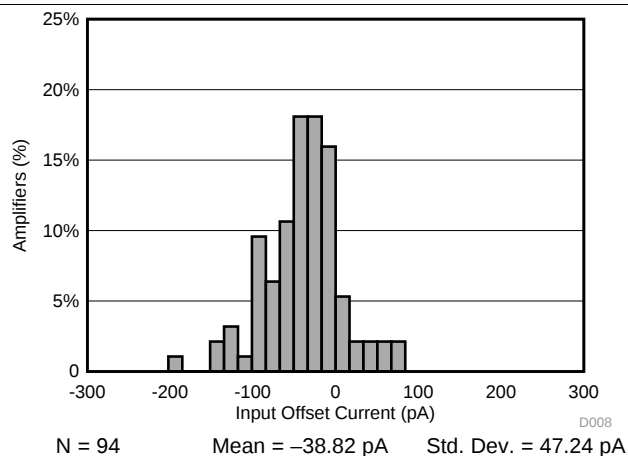


Figure 9. Typical Distribution of Input Offset Current

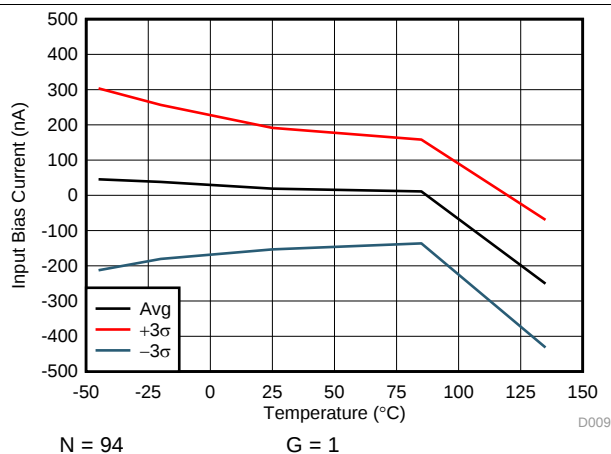


Figure 10. Input Bias Current vs Temperature

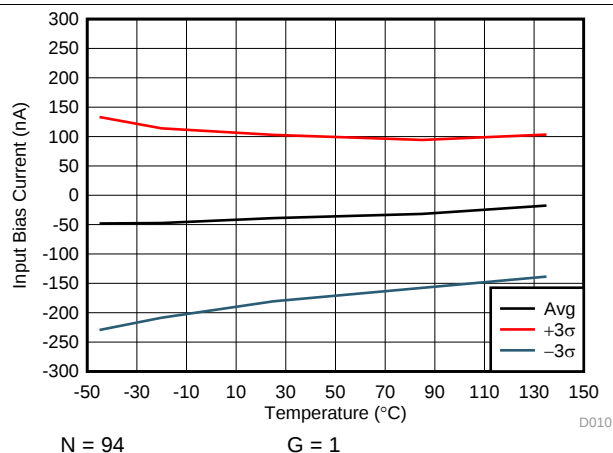


Figure 11. Input Offset Current vs Temperature

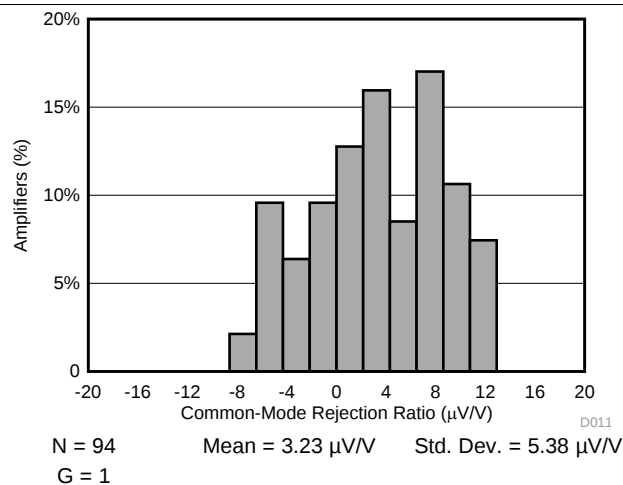


Figure 12. Typical CMRR Distribution

## Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{\text{REF}} = 0\text{ V}$ , and  $G = 1$  (unless otherwise noted)

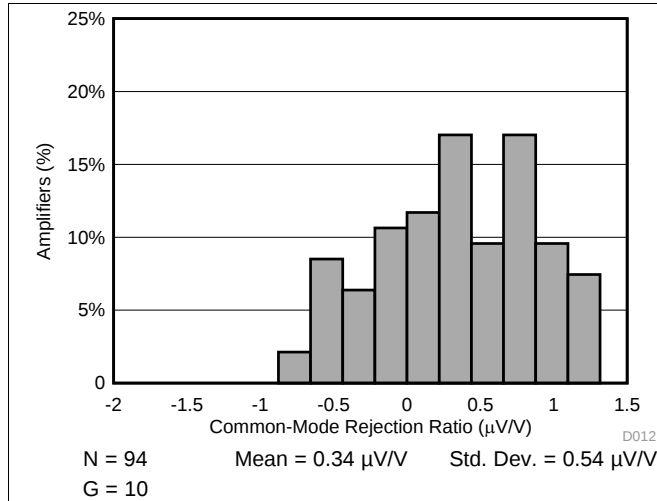


Figure 13. Typical CMRR Distribution

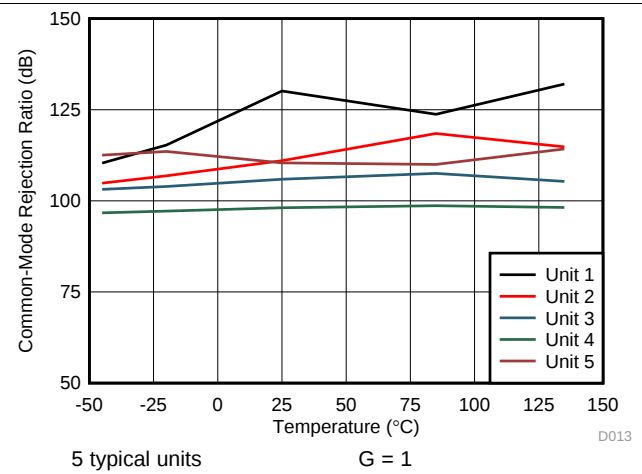


Figure 14. CMRR vs Temperature

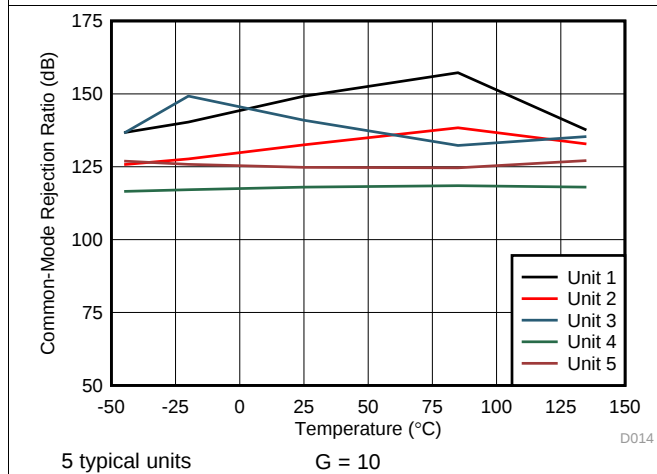


Figure 15. CMRR vs Temperature

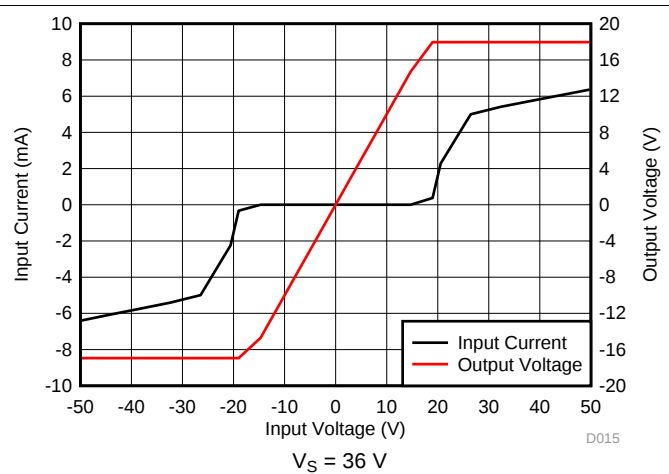


Figure 16. Input Current vs Input Overvoltage

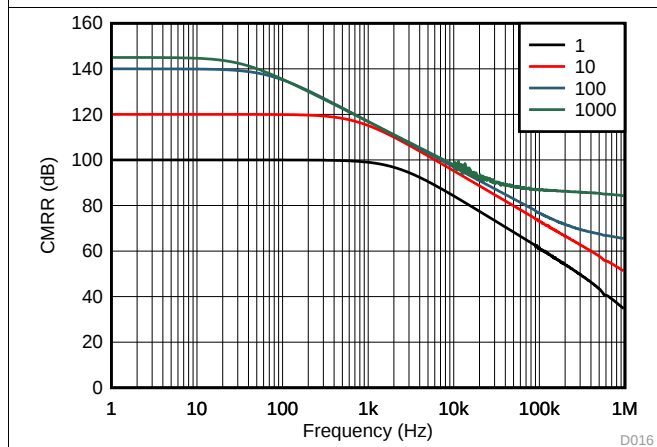


Figure 17. CMRR vs Frequency (RTI)

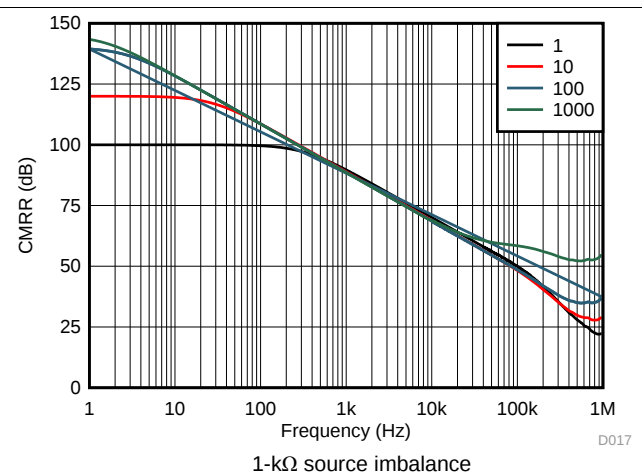
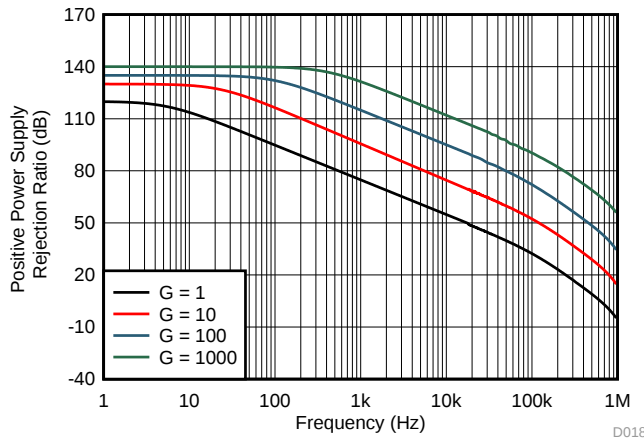


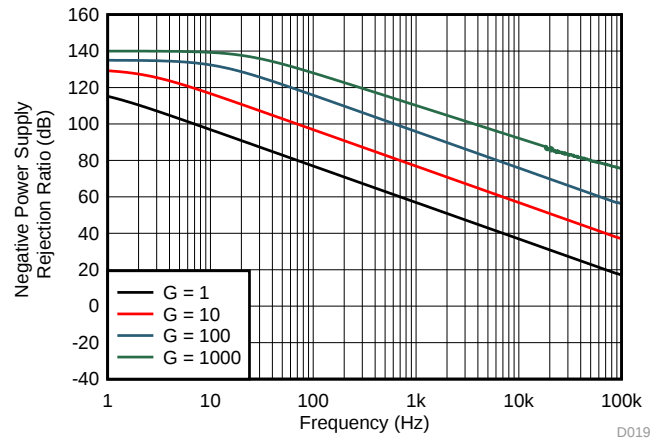
Figure 18. CMRR vs Frequency (RTI)

## Typical Characteristics (continued)

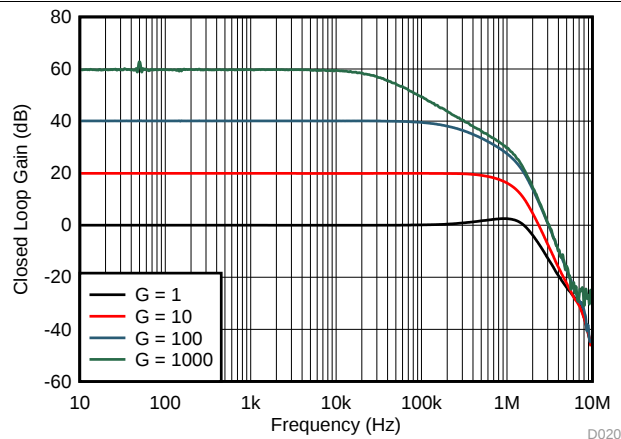
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{\text{REF}} = 0\text{ V}$ , and  $G = 1$  (unless otherwise noted)



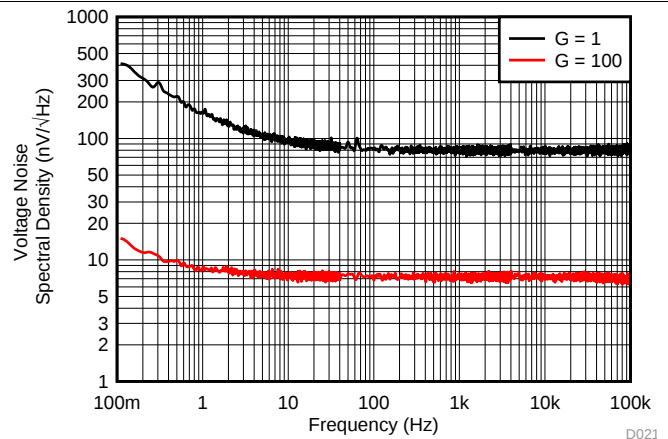
**Figure 19. Positive PSRR vs Frequency (RTI)**



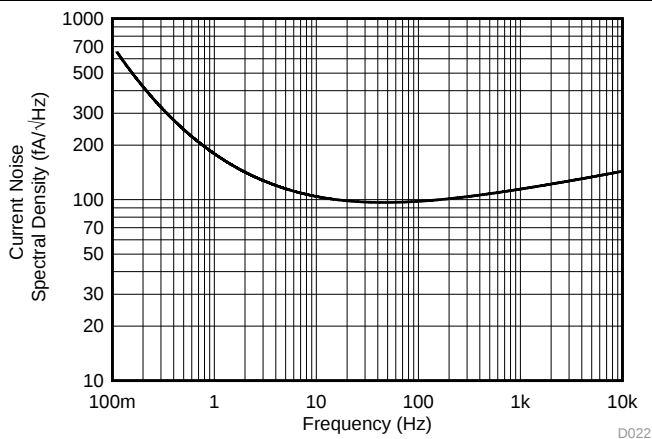
**Figure 20. Negative PSRR vs Frequency (RTI)**



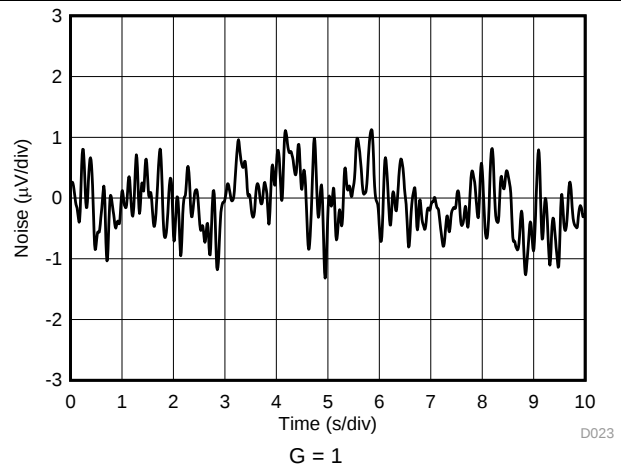
**Figure 21. Gain vs Frequency**



**Figure 22. Voltage Noise Spectral Density vs Frequency (RTI)**



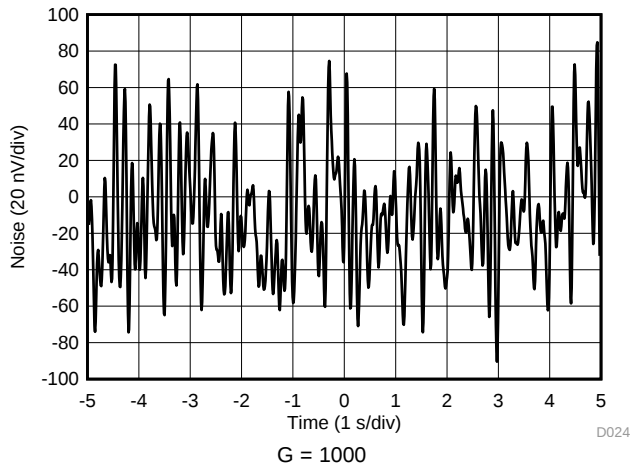
**Figure 23. Current Noise Spectral Density vs Frequency (RTI)**



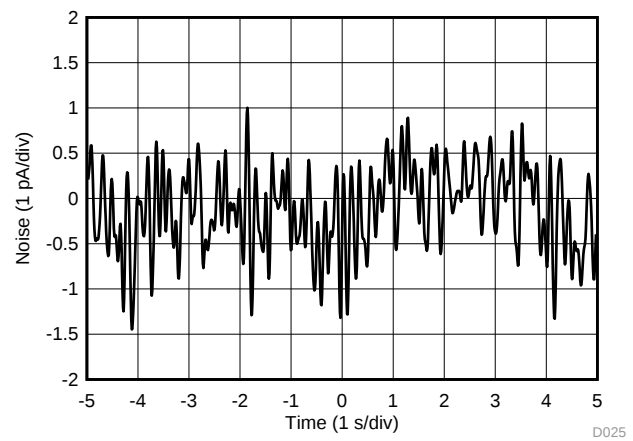
**Figure 24. 0.1-Hz to 10-Hz RTI Voltage Noise**

## Typical Characteristics (continued)

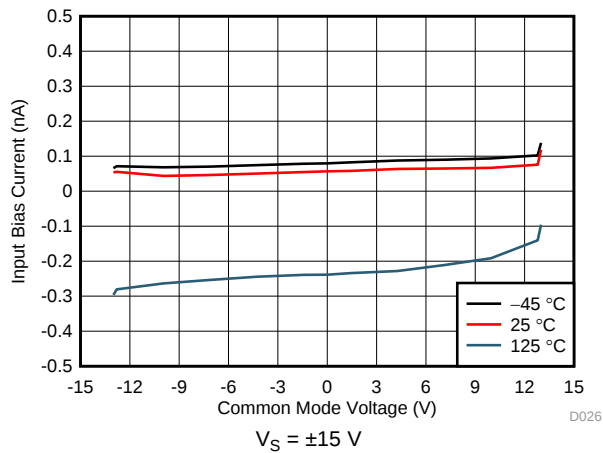
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{\text{REF}} = 0\text{ V}$ , and  $G = 1$  (unless otherwise noted)



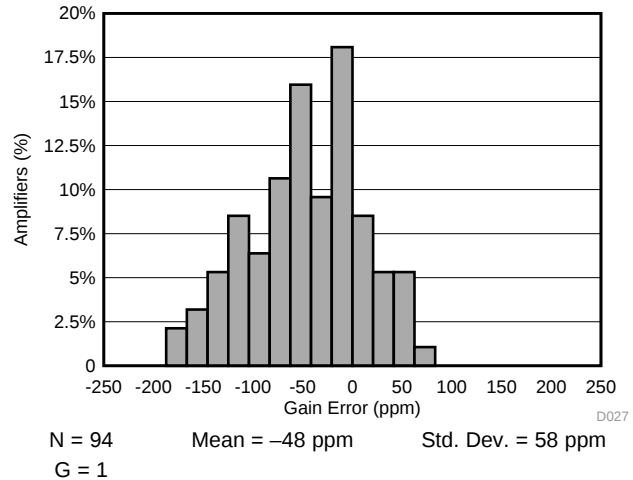
**Figure 25. 0.1-Hz to 10-Hz RTI Voltage Noise**



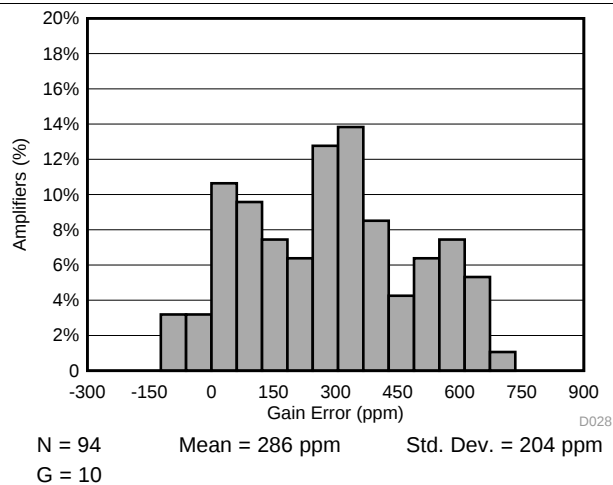
**Figure 26. 0.1-Hz to 10-Hz RTI Current Noise**



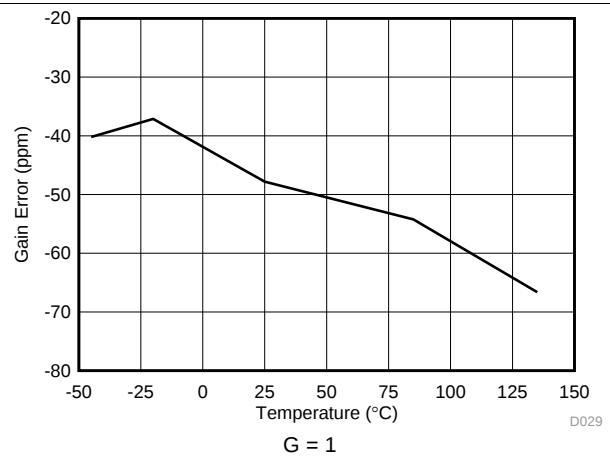
**Figure 27. Input Bias Current vs Common-Mode Voltage**



**Figure 28. Typical Distribution of Gain Error  $G = 1$**



**Figure 29. Typical Distribution of Gain Error  $G = 10$**



**Figure 30. Gain Error vs Temperature**

## Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{\text{REF}} = 0\text{ V}$ , and  $G = 1$  (unless otherwise noted)

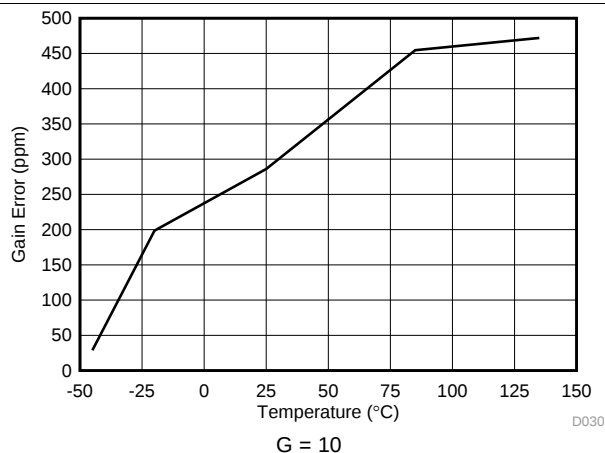


Figure 31. Gain Error vs Temperature

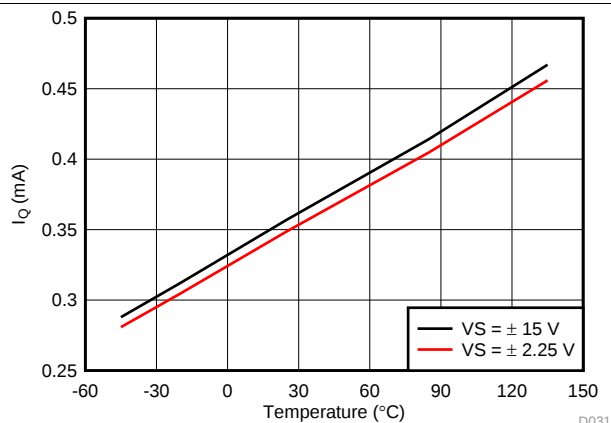


Figure 32. Supply Current vs Temperature

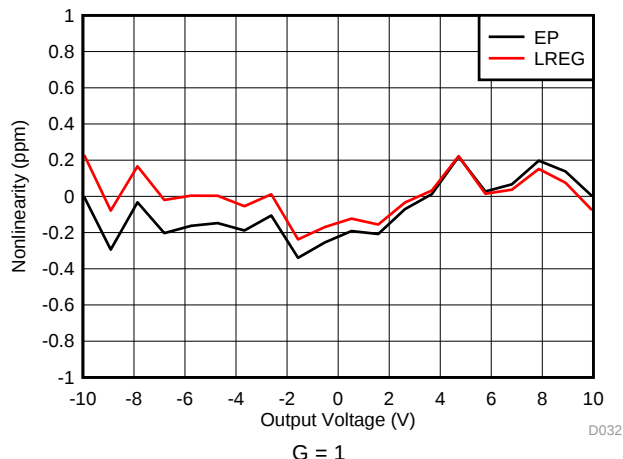


Figure 33. Gain Nonlinearity

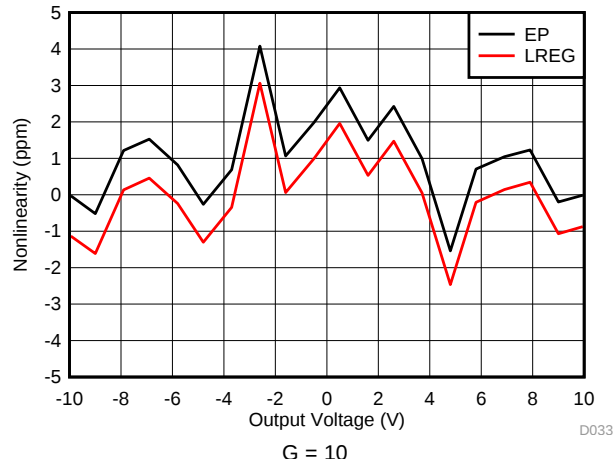


Figure 34. Gain Nonlinearity

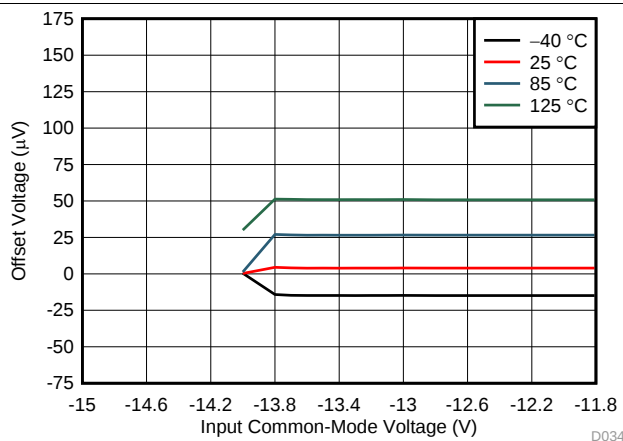


Figure 35. Offset Voltage vs Negative Common-Mode Voltage

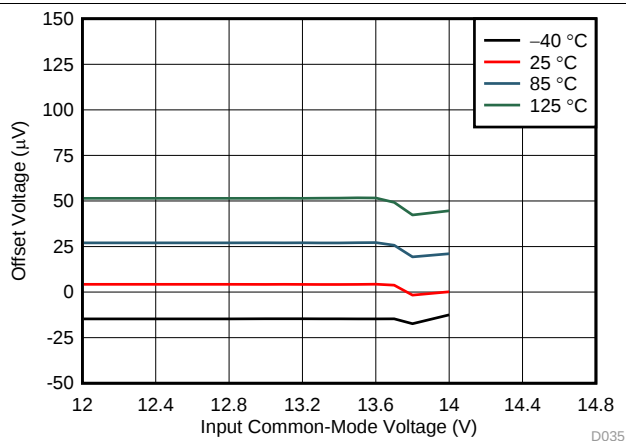
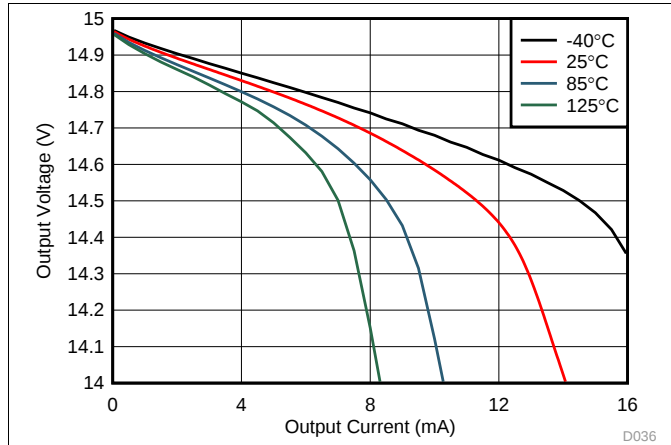


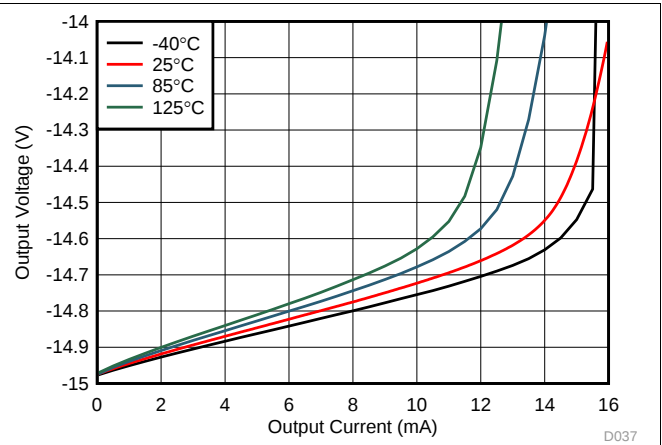
Figure 36. Offset Voltage vs Positive Common-Mode Voltage

## Typical Characteristics (continued)

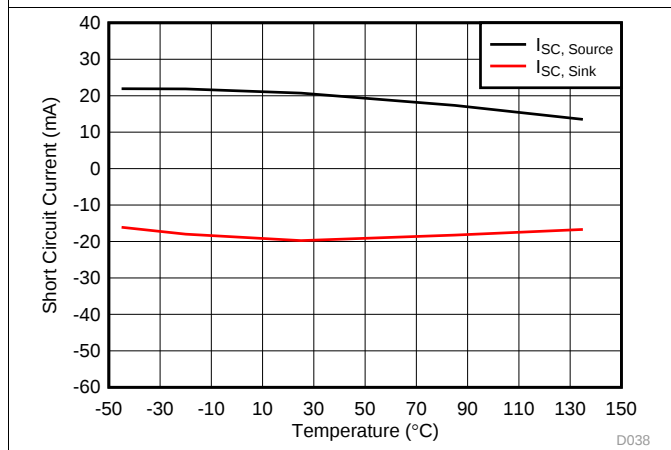
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{\text{REF}} = 0\text{ V}$ , and  $G = 1$  (unless otherwise noted)



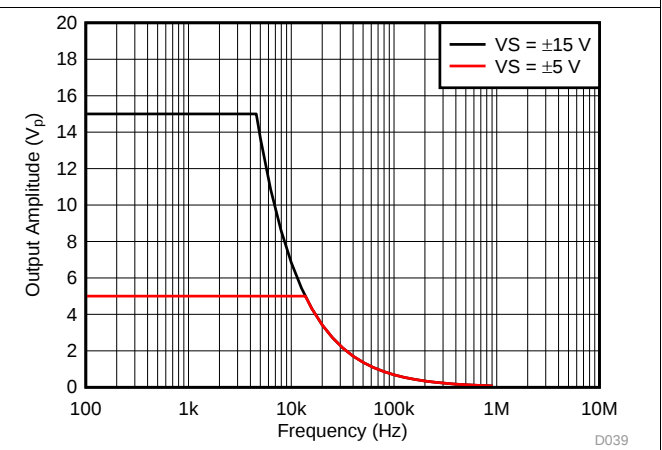
**Figure 37. Positive Output Voltage Swing vs Output Current**



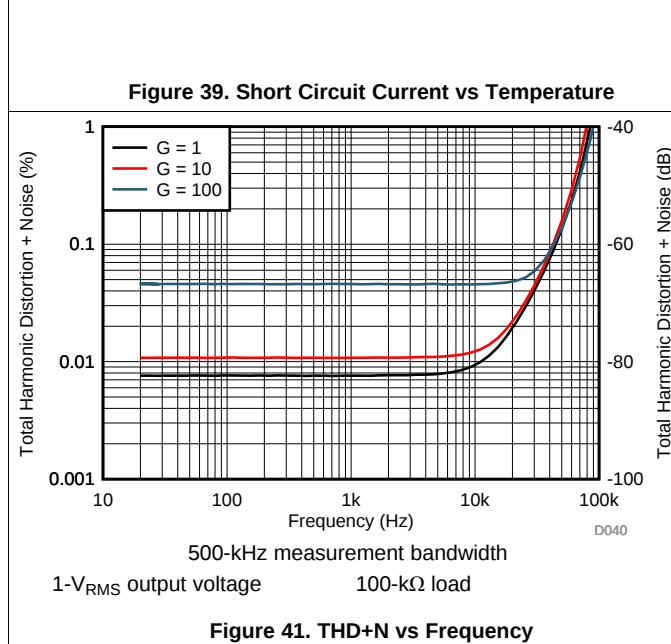
**Figure 38. Negative Output Voltage Swing vs Output Current**



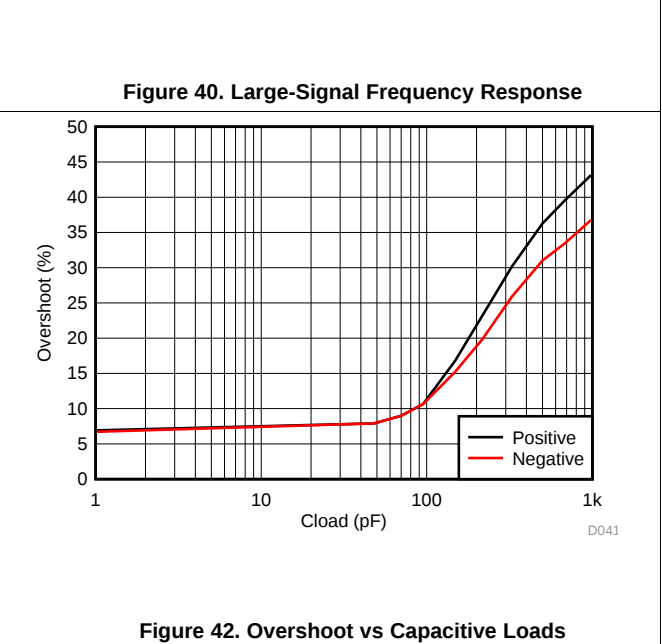
**Figure 39. Short Circuit Current vs Temperature**



**Figure 40. Large-Signal Frequency Response**



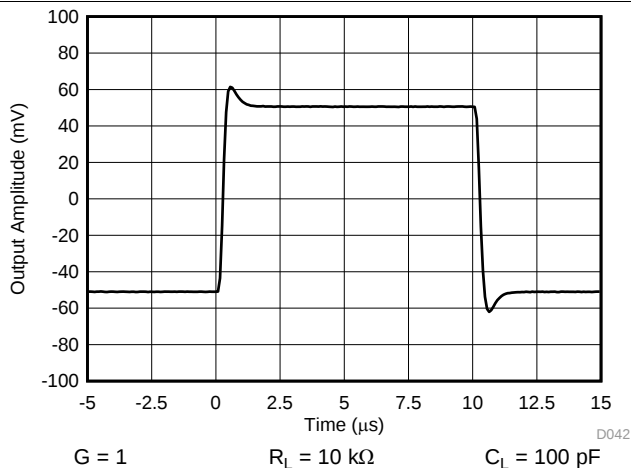
**Figure 41. THD+N vs Frequency**



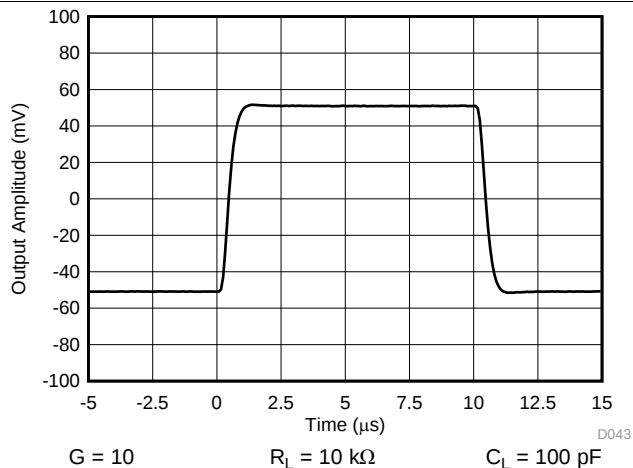
**Figure 42. Overshoot vs Capacitive Loads**

## Typical Characteristics (continued)

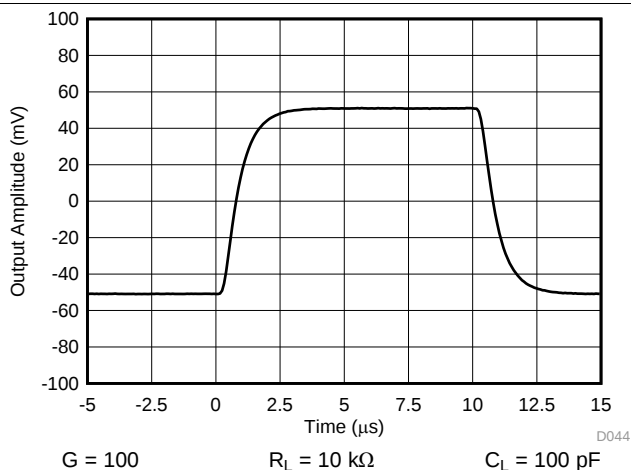
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = 0\text{ V}$ , and  $G = 1$  (unless otherwise noted)



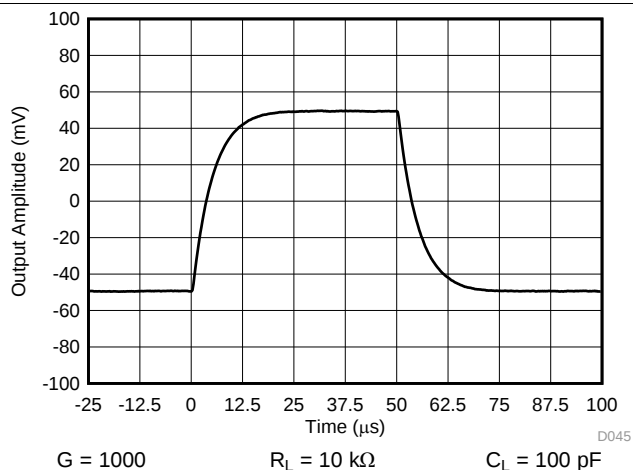
**Figure 43. Small-Signal Response**



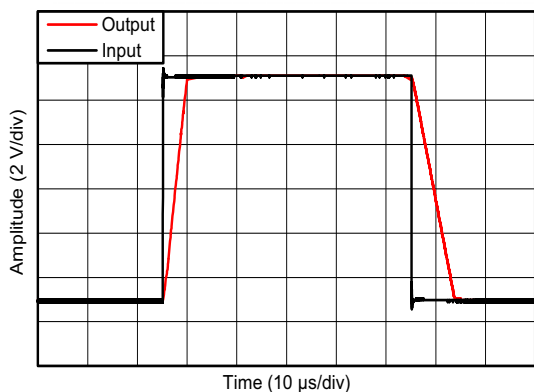
**Figure 44. Small-Signal Response**



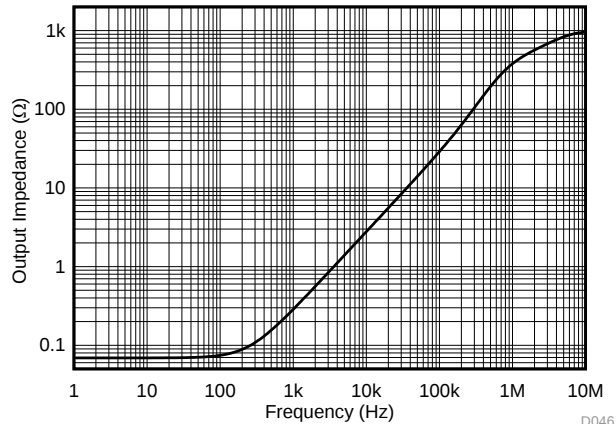
**Figure 45. Small-Signal Response**



**Figure 46. Small-Signal Response**



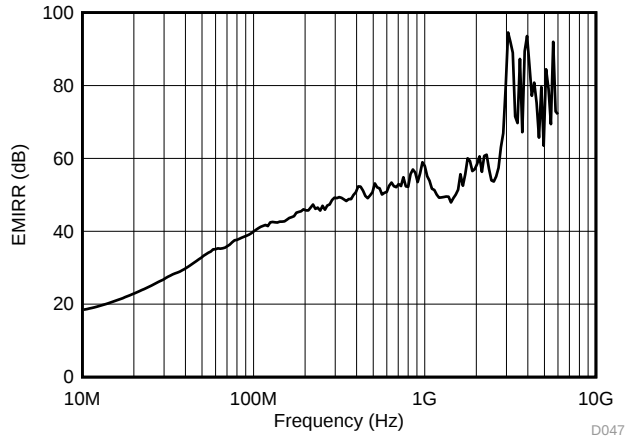
**Figure 47. Large Signal Step Response**



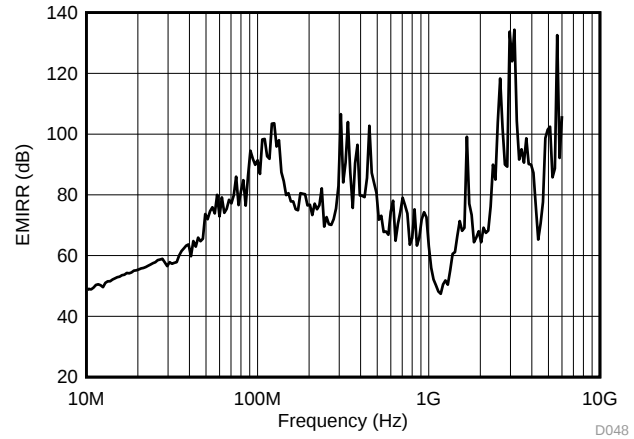
**Figure 48. Closed-Loop Output Impedance**

## Typical Characteristics (continued)

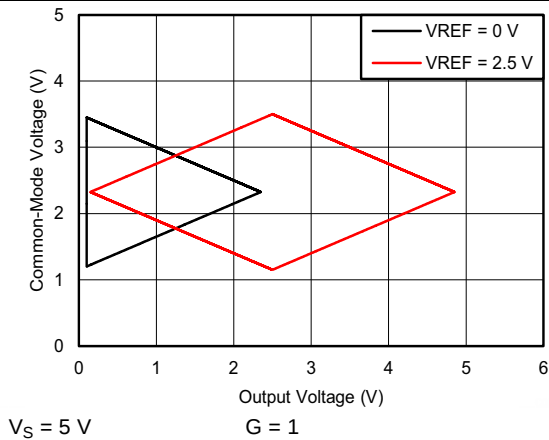
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{\text{REF}} = 0\text{ V}$ , and  $G = 1$  (unless otherwise noted)



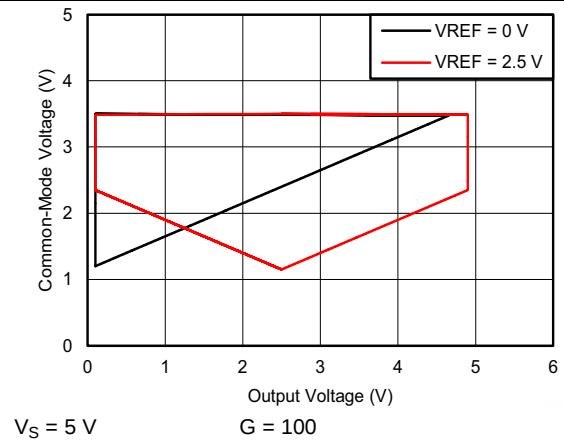
**Figure 49. Differential-Mode EMI Rejection Ratio**



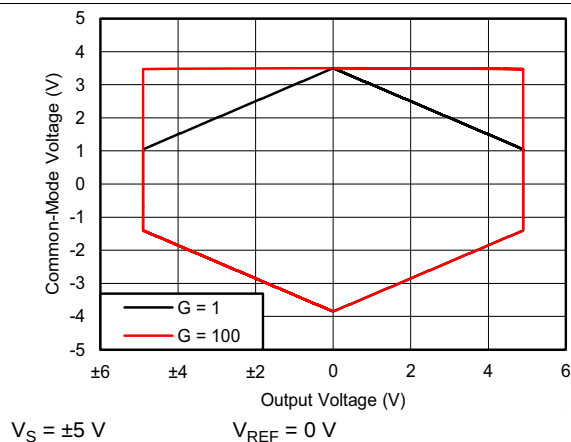
**Figure 50. Common-Mode EMI Rejection Ratio**



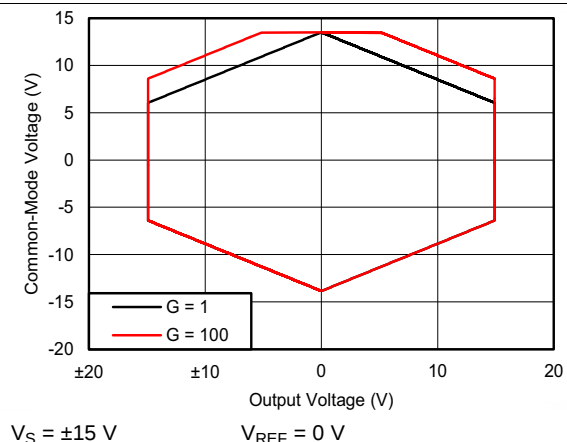
**Figure 51. Input Common-Mode Voltage vs Output Voltage**



**Figure 52. Input Common-Mode Voltage vs Output Voltage**



**Figure 53. Input Common-Mode Voltage vs Output Voltage**



**Figure 54. Input Common-Mode Voltage vs Output Voltage**

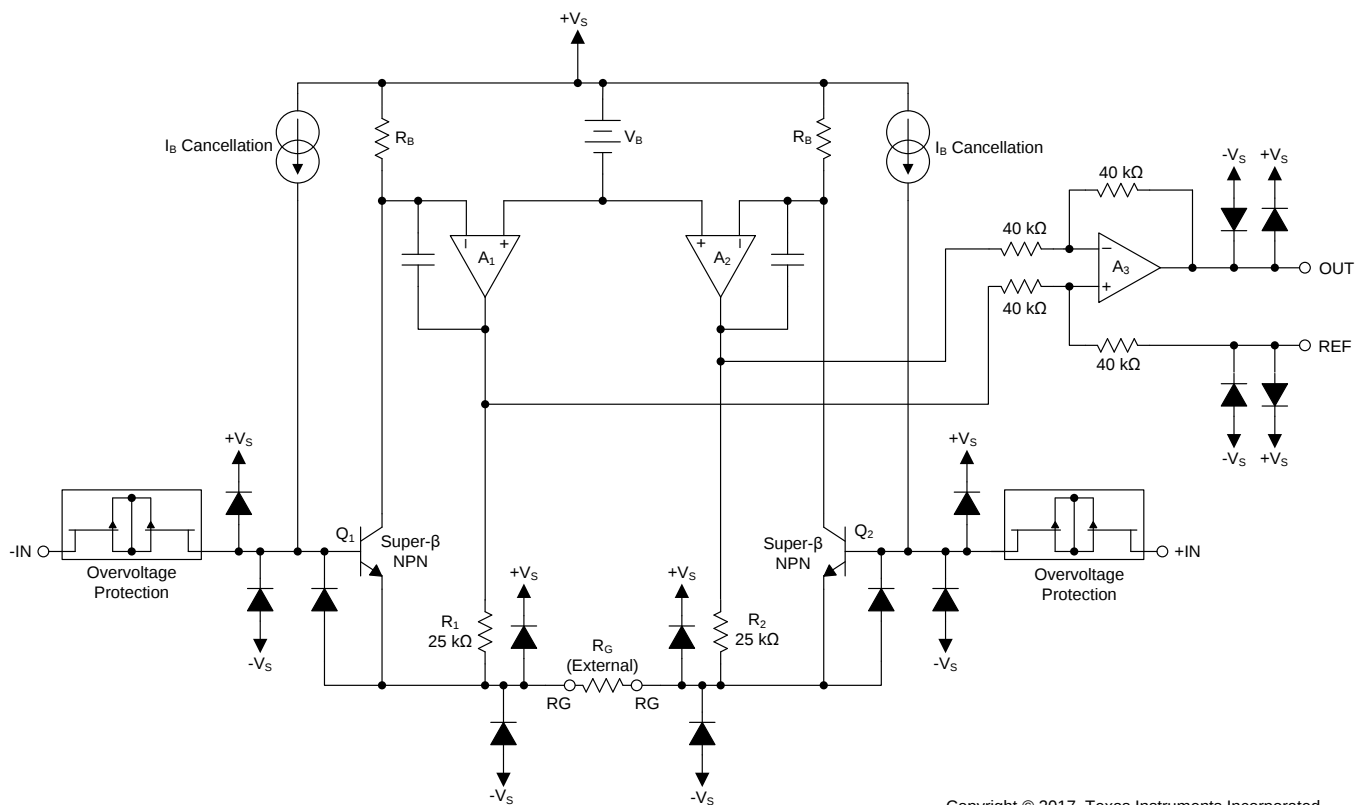
## 8 Detailed Description

### 8.1 Overview

The INA818 is a monolithic, precision instrumentation amplifier incorporating a current-feedback input stage and a four-resistor difference amplifier output stage. The functional block diagram in the next section shows how the differential input voltage is buffered by transistors  $Q_1$  and  $Q_2$  and is forced across resistor  $R_G$ , which causes a signal current to flow through resistors  $R_G$ ,  $R_1$ , and  $R_2$ . The output difference amplifier,  $A_3$ , removes the common-mode component of the input signal and refers the output signal to the REF pin. The  $V_{BE}$  and voltage drop across  $R_1$  and  $R_2$  produce output voltages on  $A_1$  and  $A_2$  that are approximately 0.8 V lower than the input voltages.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

### 8.2 Functional Block Diagram

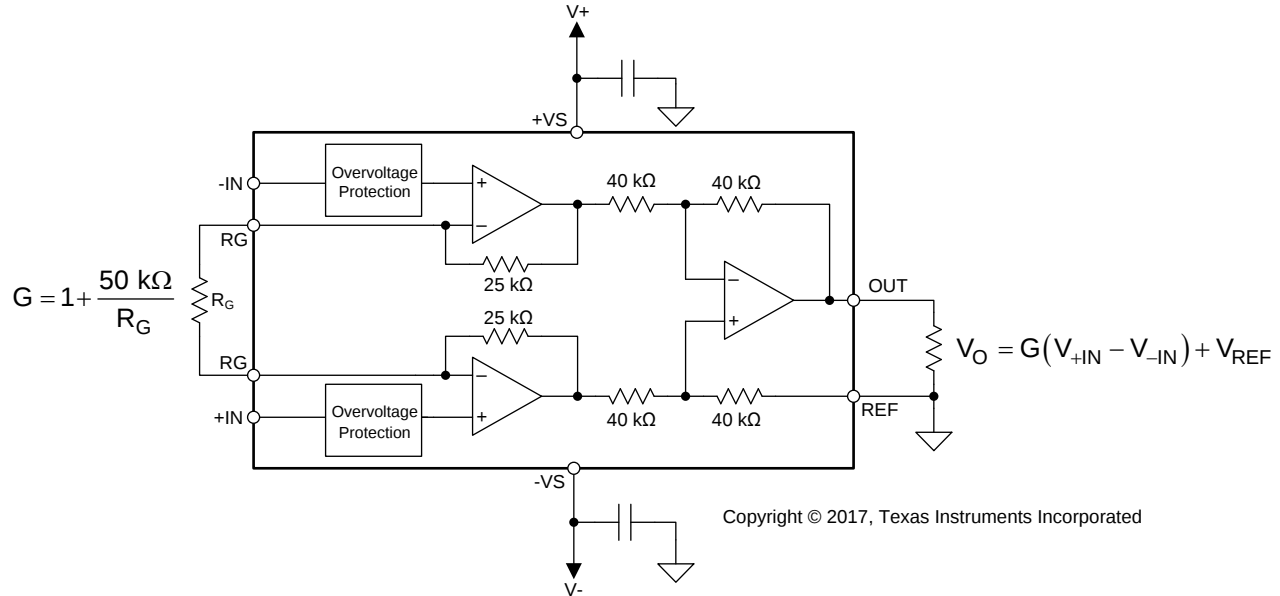


Copyright © 2017, Texas Instruments Incorporated

## 8.3 Feature Description

### 8.3.1 Setting the Gain

Figure 55 shows that the gain of the INA818 is set by a single external resistor ( $R_G$ ) connected between the  $R_G$  pins (pins 1 and 8).



**Figure 55. Simplified Diagram of the INA818 With Gain and Output Equations**

The value of  $R_G$  is selected according to Equation 1:

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G} \quad (1)$$

Table 2 lists several commonly-used gains and resistor values. The 50-k $\Omega$  term in Equation 1 comes from the sum of the two internal 25-k $\Omega$  feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA818. As shown in Figure 55 and explained in more details in the Layout section, make sure to connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground that are placed as close to the device as possible.

**Table 2. Commonly-Used Gains and Resistor Values**

| DESIRED GAIN | $R_G$ ( $\Omega$ ) | NEAREST 1% $R_G$ ( $\Omega$ ) |
|--------------|--------------------|-------------------------------|
| 1            | NC                 | NC                            |
| 2            | 50 k               | 49.9 k                        |
| 5            | 12.5 k             | 12.4 k                        |
| 10           | 5.556 k            | 5.49 k                        |
| 20           | 2.632 k            | 2.61 k                        |
| 50           | 1.02 k             | 1.02 k                        |
| 100          | 505.1              | 511                           |
| 200          | 251.3              | 249                           |
| 500          | 100.2              | 100                           |
| 1000         | 50.05              | 49.9                          |

### 8.3.1.1 Gain Drift

The stability and temperature drift of the external gain setting resistor ( $R_G$ ) also affects gain. The contribution of  $R_G$  to gain accuracy and drift is determined from [Equation 1](#).

The best gain drift of 5 ppm/°C (maximum) is achieved when the INA818 uses  $G = 1$  without  $R_G$  connected. In this case, gain drift is limited by the mismatch of the temperature coefficient of the integrated 40-kΩ resistors in the differential amplifier ( $A_3$ ). At gains greater than 1, gain drift increases as a result of the individual drift of the 25-kΩ resistors in the feedback of  $A_1$  and  $A_2$ , relative to the drift of the external gain resistor ( $R_G$ .) The low temperature coefficient of the internal feedback resistors improves the overall temperature stability of applications using gains greater than 1 V/V over alternate solutions.

Low resistor values required for high gain make wiring resistance an important consideration. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To maintain stability, avoid parasitic capacitance of more than a few picofarads at  $R_G$  connections. Careful matching of any parasitics on the  $R_G$  pins maintains optimal CMRR over frequency.

### 8.3.2 EMI Rejection

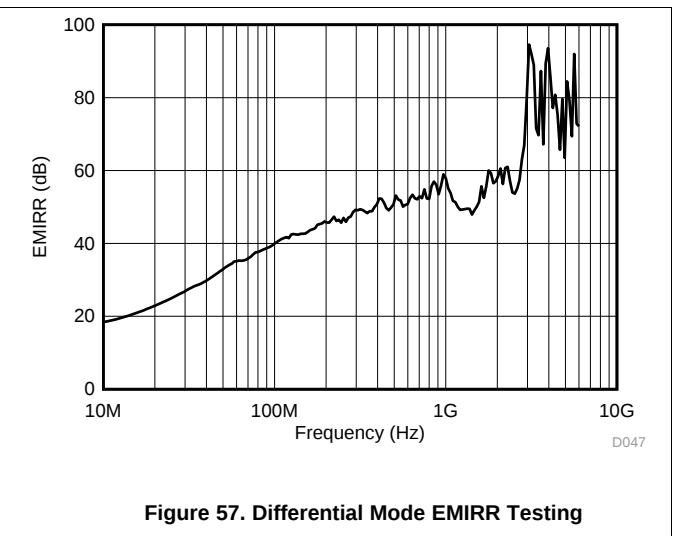
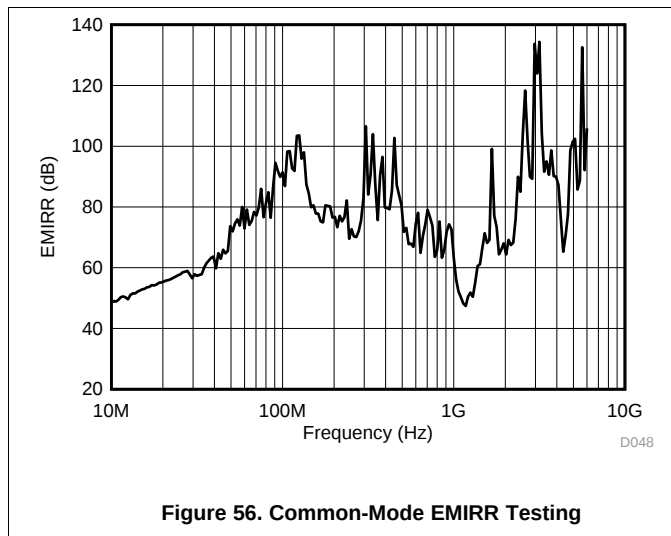
Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the ability of the INA818 to reject EMI. The offset resulting from an input EMI signal is calculated using [Equation 2](#):

$$\Delta V_{OS} = \left( \frac{V_{RF\_PEAK}^2}{100 \text{ mV}_P} \right) \cdot 10^{\left( \frac{EMIRR \text{ (dB)}}{20} \right)}$$

where

- $V_{RF\_PEAK}$  is the peak amplitude of the input EMI signal. (2)

[Figure 56](#) and [Figure 57](#) show the INA818 EMIRR graphs for differential and common-mode EMI rejection across this frequency range. [Table 3](#) lists the EMIRR values for the INA818 at frequencies commonly encountered in real-world applications. Applications listed in [Table 3](#) are centered on or operated near the frequency shown. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system. Incorporating known good practices, such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing may also be required.

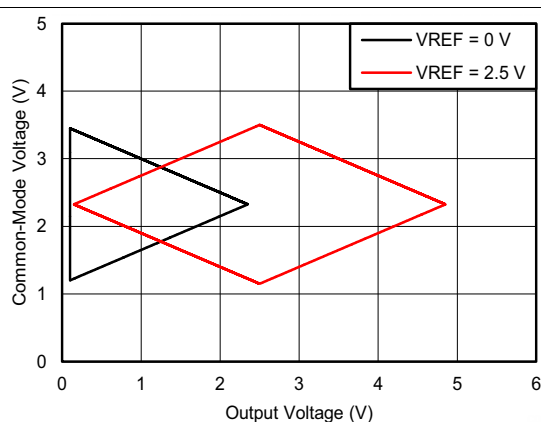
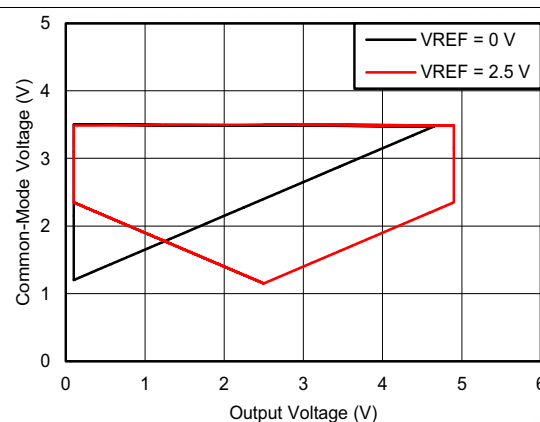
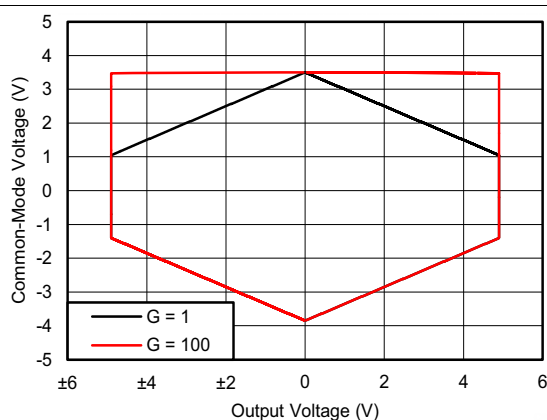
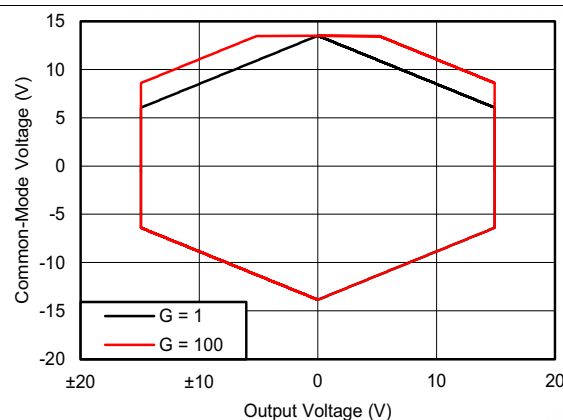


**Table 3. INA818 EMIRR for Frequencies of Interest**

| FREQUENCY | APPLICATION OR ALLOCATION                                                                                                                                                        | DIFFERENTIAL EMIRR | COMMON-MODE EMIRR |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-------------------|
| 400 MHz   | Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications                                                                          | 52 dB              | 80 dB             |
| 900 MHz   | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (up to 1.6 GHz), GSM, aeronautical mobile, UHF applications                     | 55 dB              | 71 dB             |
| 1.8 GHz   | GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)                                                                                  | 58 dB              | 73 dB             |
| 2.4 GHz   | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz) | 59 dB              | 95 dB             |
| 3.6 GHz   | Radiolocation, aero communication and navigation, satellite, mobile, S-band                                                                                                      | 78 dB              | 96 dB             |
| 5 GHz     | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)                                                | 70 dB              | 100 dB            |

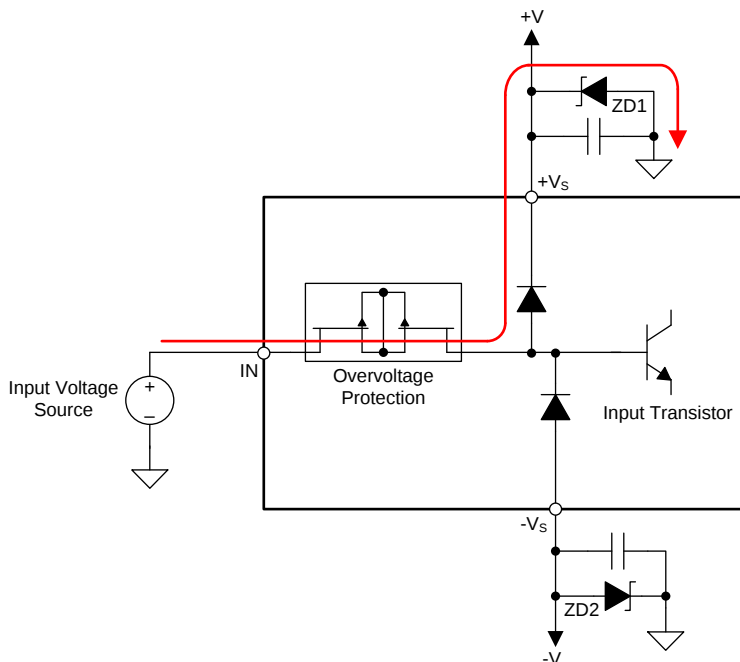
### 8.3.3 Input Common-Mode Range

The linear input voltage range of the INA818 input circuitry extends within 1.5 V (typical) of both power supplies and maintains excellent common-mode rejection throughout this range. The common-mode range for the most common operating conditions are shown in [Figure 58](#), [Figure 53](#), and [Figure 54](#). The common-mode range for other operating conditions is best calculated using the [Common-Mode Input Range Calculator for Instrumentation Amplifiers](#).


 $V_S = 5\text{ V}$ 
 $G = 1$ 
**Figure 58. Input Common-Mode Voltage vs Output Voltage**

 $V_S = 5\text{ V}$ 
 $G = 100$ 
**Figure 59. Input Common-Mode Voltage vs Output Voltage**

 $V_S = \pm 5\text{ V}$ 
 $V_{REF} = 0\text{ V}$ 
**Figure 60. Input Common-Mode Voltage vs Output Voltage**

 $V_S = \pm 15\text{ V}$ 
 $V_{REF} = 0\text{ V}$ 
**Figure 61. Input Common-Mode Voltage vs Output Voltage**

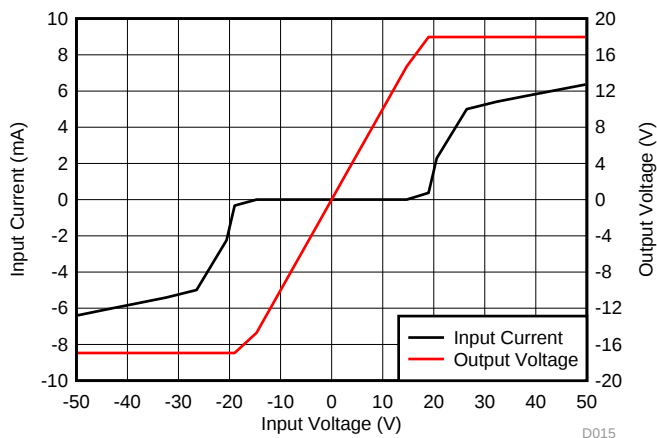
### 8.3.4 Input Protection

The inputs of the INA818 device are individually protected for voltages up to  $\pm 60$  V. For example, a condition of  $-60$  V on one input and  $+60$  V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 8 mA.



**Figure 62. Input Current Path During an Overvoltage Condition**

During an input overvoltage condition, current flows through the input protection diodes into the power supplies; see Figure 62. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2 in Figure 62) must be placed on the power supplies to provide a current pathway to ground. Figure 63 shows the input current for input voltages from  $-50$  V to  $+50$  V when the INA818 is powered by  $\pm 15$ -V supplies.



**Figure 63. Input Current vs Input Overvoltage**

### 8.3.5 Operating Voltage

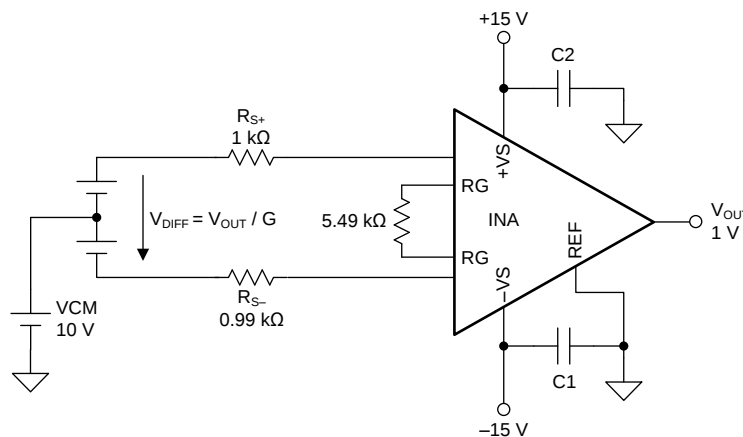
The INA818 operates over a power-supply range of 4.5 V to 36 V ( $\pm 2.25$  V to  $\pm 18$  V).

#### CAUTION

Supply voltages higher than 40 V ( $\pm 20$  V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in *Typical Characteristics*.

### 8.3.6 Error Sources

Most modern signal-conditioning systems calibrate errors at room temperature. However, calibration of errors that result from a change in temperature is normally difficult and costly. Therefore, minimize these errors by choosing high-precision components, such as the INA818, that have improved specifications in critical areas that impact the precision of the overall system. Figure 64 shows an example application.



**Figure 64. Example Application With  $G = 10$  V/V and 1-V Output Voltage**

Resistor-adjustable devices (such as the INA818) show the lowest gain error in  $G = 1$  because of the inherently well-matched drift of the internal resistors of the differential amplifier. At gains greater than 1 (for instance,  $G = 10$  V/V or  $G = 100$  V/V), the gain error becomes a significant error source because of the contribution of the resistor drift of the 25-kΩ feedback resistors in conjunction with the external gain resistor. Except for very high gain applications, the gain drift is by far the largest error contributor compared to other drift errors, such as offset drift.

The INA818 offers excellent gain error over temperature for both  $G > 1$  and  $G = 1$  (no external gain resistor). Table 5 summarizes the major error sources in common INA applications and compares the three cases of  $G = 1$  (no external resistor) and  $G = 10$  (5.49-kΩ external resistor) and  $G = 100$  (511-Ω external resistor). All calculations are assuming an output voltage of  $V_{OUT} = 1$  V. Thus, the input signal  $V_{DIFF}$  (given by  $V_{DIFF} = V_{OUT} / G$ ) exhibits smaller and smaller amplitudes with increasing gain  $G$ .  $V_{DIFF} = 1$  mV at  $G = 1000$  in this example. All calculations refer the error to the input for easy comparison and system evaluation. As Table 5 shows, errors generated by the input stage (such as input offset voltage) are more dominant at higher gain, while the effects of output stage are suppressed because they are divided by the gain when referring them back to the input. The gain error and gain drift error are much more significant for gains greater than 1 because of the contribution of the resistor drift of the 25-kΩ feedback resistors in conjunction with the external gain resistor. In most applications, static errors (absolute accuracy errors) can readily be removed during calibration in production, while the drift errors are the key factors limiting overall system performance.

**Table 4. System Specifications for Error Calculation**

| QUANTITY                      | VALUE | UNIT     |
|-------------------------------|-------|----------|
| $V_{OUT}$                     | 1     | V        |
| VCM                           | 10    | V        |
| VS                            | 1     | V        |
| $R_{S+}$                      | 1000  | $\Omega$ |
| $R_{S-}$                      | 999   | $\Omega$ |
| RG tolerance                  | 0.01  | %        |
| RG drift                      | 10    | ppm/°C   |
| Temperature range upper limit | 105   | °C       |

**Table 5. Error Calculation**

| ERROR SOURCE                                            | ERROR CALCULATION                                                                                             | INA818 VALUES                                  |                  |                         |                           |                            |
|---------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|------------------------------------------------|------------------|-------------------------|---------------------------|----------------------------|
|                                                         |                                                                                                               | SPECIFICATION                                  | UNIT             | G = 1<br>ERROR<br>(ppm) | G = 100<br>ERROR<br>(ppm) | G = 1000<br>ERROR<br>(ppm) |
| ABSOLUTE ACCURACY AT 25°C                               |                                                                                                               |                                                |                  |                         |                           |                            |
| Input offset voltage                                    | V <sub>OSI</sub> / V <sub>DIFF</sub>                                                                          | 35                                             | μV               | 35                      | 350                       | 3500                       |
| Output offset voltage                                   | V <sub>OSO</sub> / (G × V <sub>DIFF</sub> )                                                                   | 300                                            | μV               | 300                     | 300                       | 300                        |
| Input offset current                                    | I <sub>OS</sub> × maximum (R <sub>S+</sub> , R <sub>S-</sub> ) / V <sub>DIFF</sub>                            | 0.5                                            | nA               | 1                       | 5                         | 50                         |
| CMRR (min)                                              | V <sub>CM</sub> / (10 <sup>CMRR/20</sup> × V <sub>DIFF</sub> )                                                | 90 (G = 1),<br>110 (G = 10),<br>130 (G = 100)  | dB               | 316                     | 316                       | 316                        |
| PSRR (min)                                              | (V <sub>CC</sub> -V <sub>S</sub> )/ (10 <sup>PSRR/20</sup> × V <sub>DIFF</sub> )                              | 110 (G = 1),<br>114 (G = 10),<br>130 (G = 100) | dB               | 3                       | 20                        | 32                         |
| Gain error from INA (max)                               | GE(%) × 10 <sup>4</sup>                                                                                       | 0.02 (G = 1),<br>0.15 (G = 10, 100)            | %                | 200                     | 1500                      | 1500                       |
| Gain error from external resistor RG (max)              | GE(%) × 10 <sup>4</sup>                                                                                       | 0.01                                           | %                | 100                     | 100                       | 100                        |
| Total absolute accuracy error (ppm) at 25°C, worst case | sum of all errors                                                                                             | —                                              | —                | 955                     | 2591                      | 5798                       |
| Total absolute accuracy error (ppm) at 25°C, average    | rms sum of all errors                                                                                         | —                                              | —                | 491                     | 1604                      | 3835                       |
| DRIFT TO 105°C                                          |                                                                                                               |                                                |                  |                         |                           |                            |
| Gain drift from INA (max)                               | GTC × (T <sub>A</sub> – 25)                                                                                   | 5 (G = 1),<br>35 (G = 10, 100)                 | ppm/°C           | 400                     | 2800                      | 2800                       |
| Gain drift from external resistor RG (max)              | GTC × (T <sub>A</sub> – 25)                                                                                   | 10                                             | ppm/°C           | 800                     | 800                       | 800                        |
| Input offset voltage drift (max)                        | (V <sub>OSI_TC</sub> / V <sub>DIFF</sub> ) × (T <sub>A</sub> – 25)                                            | 0.4                                            | μV/°C            | 32                      | 320                       | 3200                       |
| Output offset voltage drift                             | [V <sub>OSO_TC</sub> / ( G × V <sub>DIFF</sub> )] × (T <sub>A</sub> – 25)                                     | 5                                              | μV/°C            | 400                     | 400                       | 400                        |
| Offset current drift                                    | I <sub>OS_TC</sub> × maximum (R <sub>S+</sub> , R <sub>S-</sub> ) × (T <sub>A</sub> – 25) / V <sub>DIFF</sub> | 20                                             | pA/°C            | 2                       | 16                        | 160                        |
| Total drift error to 105°C (ppm), worst case            | sum of all errors                                                                                             | —                                              | —                | 1634                    | 4336                      | 7360                       |
| Total drift error to 105°C (ppm), typical               | rms sum of all errors                                                                                         | —                                              | —                | 980                     | 2957                      | 4348                       |
| RESOLUTION                                              |                                                                                                               |                                                |                  |                         |                           |                            |
| Gain nonlinearity                                       |                                                                                                               | 10 (G = 1, 10),<br>15 (G = 100)                | ppm of FS        | 10                      | 10                        | 15                         |
| Voltage noise (at 1 kHz)                                | $\sqrt{BW} \times \sqrt{e_{NI}^2 + \left[\frac{e_{NO}}{G}\right]^2} \times \frac{6}{V_{DIFF}}$                | e <sub>NI</sub> = 8,<br>e <sub>NO</sub> = 90   | μV <sub>PP</sub> | 1204                    | 1070                      | 3941                       |
| Current noise (at 1kHz)                                 | I <sub>N</sub> × maximum (R <sub>S+</sub> , R <sub>S-</sub> ) × √BW / V <sub>DIFF</sub>                       | 0.13                                           | pA/√Hz           | 0.3                     | 2                         | 11                         |
| Total resolution error (ppm), worst case                | sum of all errors                                                                                             | —                                              | —                | 1214                    | 1080                      | 3956                       |
| Total resolution error (ppm), typical                   | rms sum of all errors                                                                                         | —                                              | —                | 1204                    | 1070                      | 3941                       |
| TOTAL ERROR                                             |                                                                                                               |                                                |                  |                         |                           |                            |
| Total error (ppm), worst case                           | sum of all errors                                                                                             | —                                              | —                | 3802                    | 8007                      | 17113                      |
| Total error (ppm), typical                              | rms sum of all errors                                                                                         | —                                              | —                | 1628                    | 3530                      | 7010                       |

## 8.4 Device Functional Modes

The INA818 has a single functional mode and operates when the power-supply voltage is greater than 4.5 V ( $\pm 2.25$  V). The maximum power-supply voltage for the INA818 is 36 V ( $\pm 18$  V.)

## 9 Application and Implementation

### NOTE

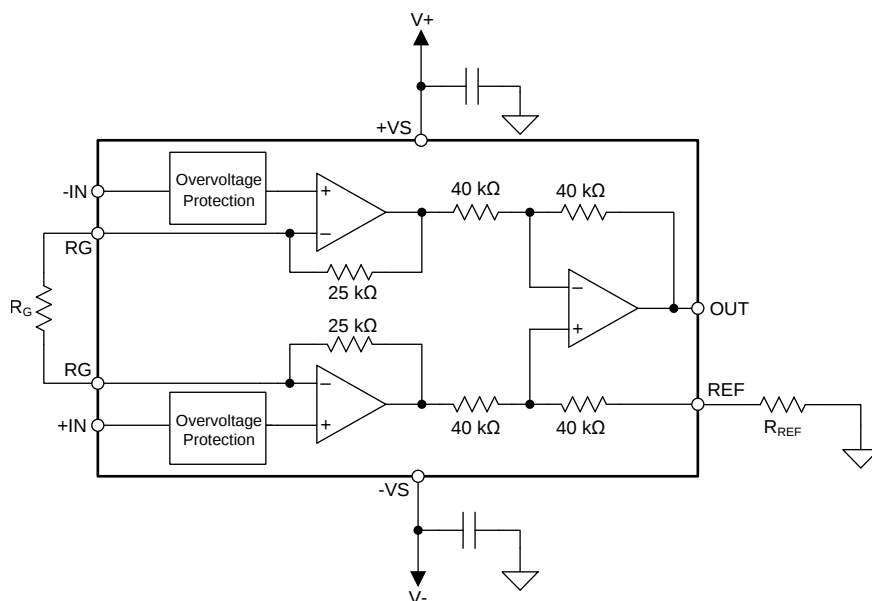
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Reference Pin

The output voltage of the INA818 is developed with respect to the voltage on the reference pin, REF. In dual-supply operation, REF (pin 6) is connected to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise midsupply level is useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA818 drives a single-supply ADC.

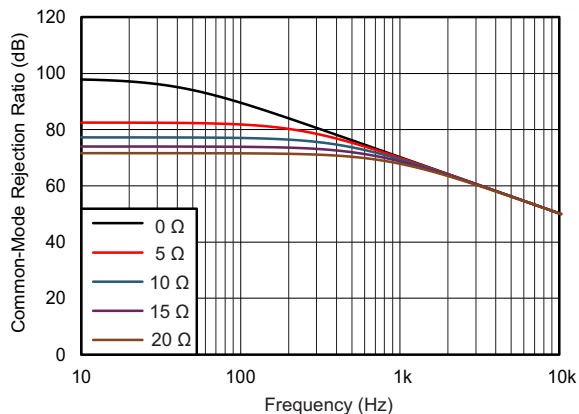
The voltage source applied to the reference pin must have a low output impedance. As shown in Figure 65, any resistance at the reference pin (shown as  $R_{REF}$  in Figure 65) is in series with an internal 40-k $\Omega$  resistor.



**Figure 65. Parasitic Resistance Shown at the Reference Pin**

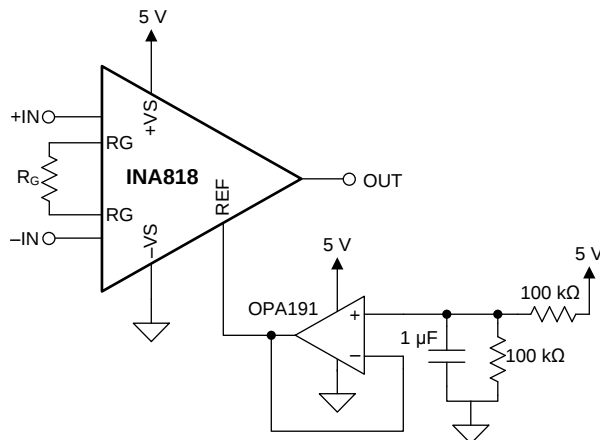
## Application Information (continued)

The parasitic resistance at the reference pin ( $R_{REF}$ ) creates an imbalance in the four resistors of the internal difference amplifier, which degrades the common-mode rejection ratio (CMRR). Figure 66 shows the degradation in CMRR of the INA818 as a result of increased resistance at the reference pin. For the best performance, keep the source impedance to the REF pin ( $R_{REF}$ ) below 5  $\Omega$ .



**Figure 66. The Effect of Increasing Resistance at the Reference Pin**

Voltage-reference devices are a suitable option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider generates a reference voltage, the divider must be buffered by an op amp, as Figure 67 shows, in order to avoid CMRR degradation.



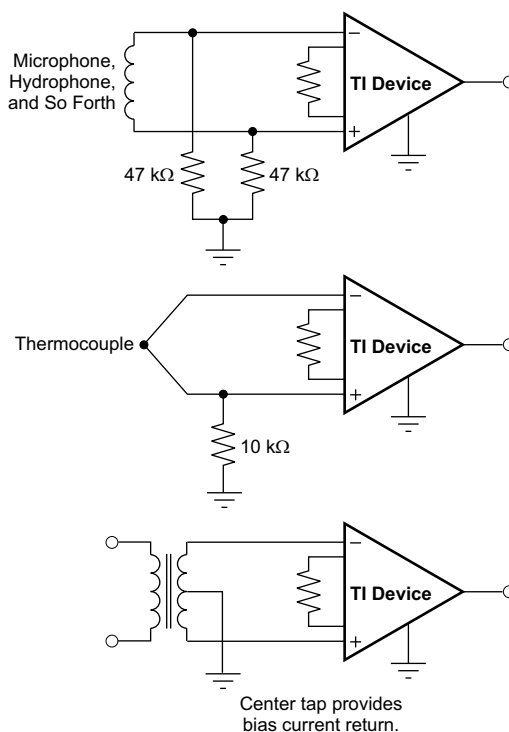
**Figure 67. Using an Op Amp to Buffer Reference Voltages**

## Application Information (continued)

### 9.1.2 Input Bias Current Return Path

The input impedance of the INA818 is extremely high—approximately 100 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 150 pA. High input impedance means that this input bias current changes very little with varying input voltage.

For proper operation, input circuitry must provide a path for input bias current. [Figure 68](#) shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA818, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can connect to one input (as shown in the thermocouple example in [Figure 68](#)). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.



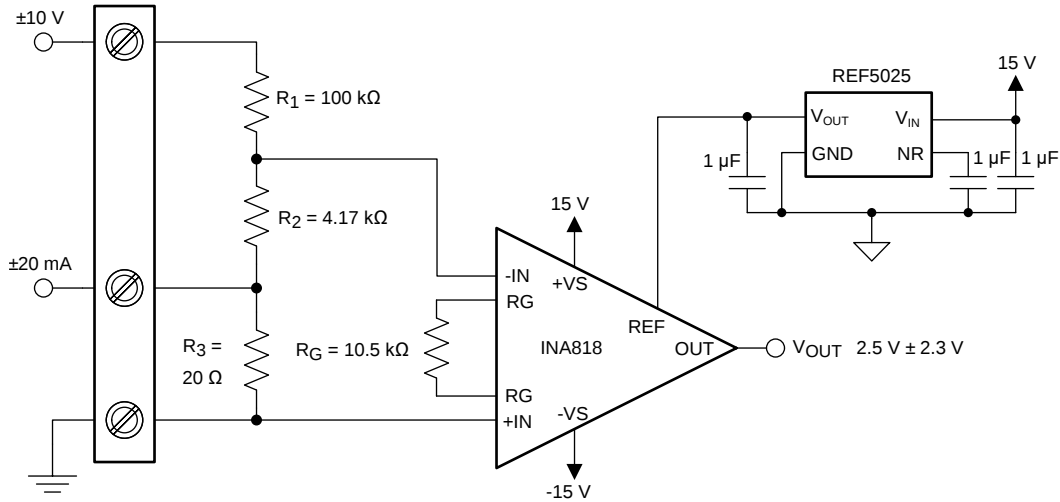
Copyright © 2017, Texas Instruments Incorporated

**Figure 68. Providing an Input Common-Mode Current Path**

## 9.2 Typical Applications

### 9.2.1 Three-Pin Programmable Logic Controller (PLC)

Figure 69 shows a three-pin programmable-logic controller (PLC) design for the INA818. This PLC reference design accepts inputs of  $\pm 10$  V or  $\pm 20$  mA. The output is a single-ended voltage of  $2.5\text{ V} \pm 2.3\text{ V}$  (or 200 mV to 4.8 V). Many PLCs typically have these input and output ranges.



Copyright © 2017, Texas Instruments Incorporated

Figure 69. PLC Input ( $\pm 10$  V, 4 mA to 20 mA)

#### 9.2.1.1 Design Requirements

For this application, the design requirements are as follows:

- 4-mA to 20-mA input with less than 20-Ω burden
- $\pm 20$ -mA input with less than 20-Ω burden
- $\pm 10$ -V input with impedance of approximately 100 kΩ
- Maximum 4-mA to 20-mA or  $\pm 20$ -mA burden voltage equal to  $\pm 0.4$  V
- Output range within 0 V to 5 V

#### 9.2.1.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in Figure 69: current input and voltage input. This design requires  $R_1 \gg R_2 \gg R_3$ . Given this relationship, Equation 3 calculates the current input mode transfer function.

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF}$$

where

- G represents the gain of the instrumentation amplifier
- $V_D$  represents the differential voltage at the INA818 inputs
- $V_{REF}$  is the voltage at the INA818 REF pin
- $I_{IN}$  is the input current

(3)

Equation 4 shows the transfer function for the voltage input mode.

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left[V_{IN} \times \frac{R_2}{R_1 + R_2}\right] \times G + V_{REF}$$

where

- $V_{IN}$  is the input voltage

(4)

## Typical Applications (continued)

$R_1$  sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 k $\Omega$ . 100 k $\Omega$  is selected for  $R_1$  because increasing the  $R_1$  value also increases noise. The value of  $R_3$  must be extremely small compared to  $R_1$  and  $R_2$ . 20  $\Omega$  for  $R_3$  is selected because that resistance value is much smaller than  $R_1$  and yields an input voltage of  $\pm 400$  mV when operated in current mode ( $\pm 20$  mA).

Use Equation 5 to calculate  $R_2$  given  $V_D = \pm 400$  mV,  $V_{IN} = \pm 10$  V, and  $R_1 = 100$  k $\Omega$ .

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167 \text{ k}\Omega \quad (5)$$

The value obtained from Equation 5 is not a standard 0.1% value, so 4.17 k $\Omega$  is selected.  $R_1$  and  $R_2$  also use 0.1% tolerance resistors to minimize error.

Use Equation 6 to calculate the ideal gain of the instrumentation amplifier.

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8 \text{ V} - 2.5 \text{ V}}{400 \text{ mV}} = 5.75 \frac{\text{V}}{\text{V}} \quad (6)$$

Equation 7 calculates the gain-setting resistor value using the INA818 gain equation, Equation 1.

$$R_G = \frac{50 \text{ k}\Omega}{G - 1} = \frac{50 \text{ k}\Omega}{5.75 - 1} = 10.5 \text{ k}\Omega \quad (7)$$

10.5 k $\Omega$  is a standard 0.1% resistor value that can be used in this design.

### 9.2.1.3 Application Curves

Figure 70 and Figure 71 show typical characteristic curves for the circuit in Figure 69.

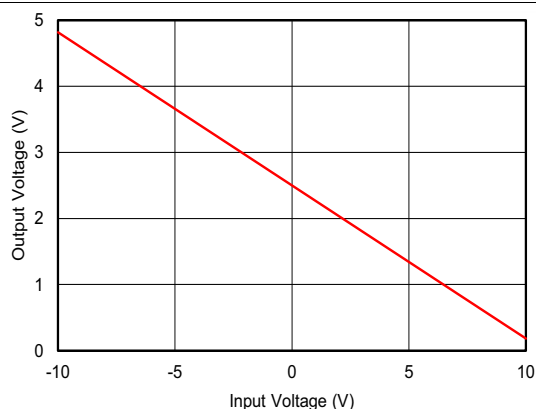


Figure 70. PLC Output Voltage vs Input Voltage

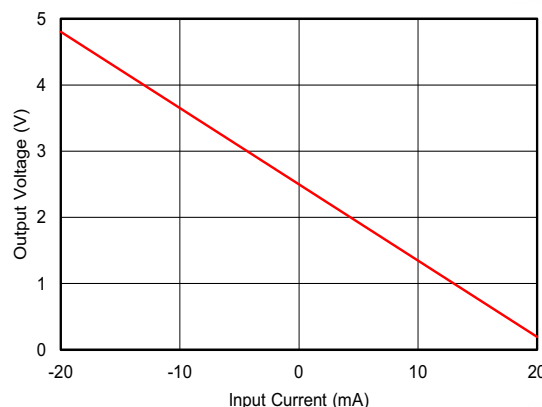
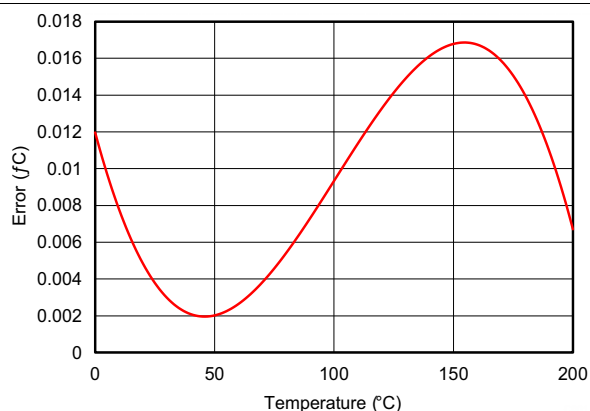
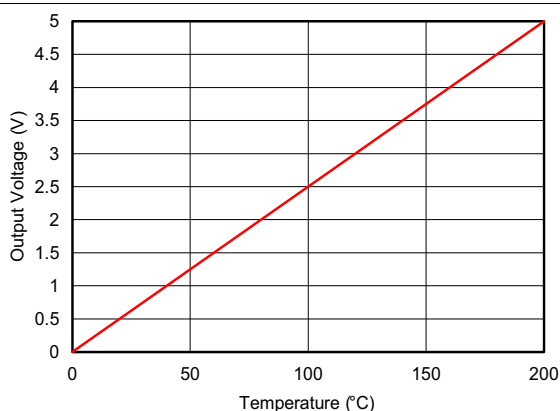
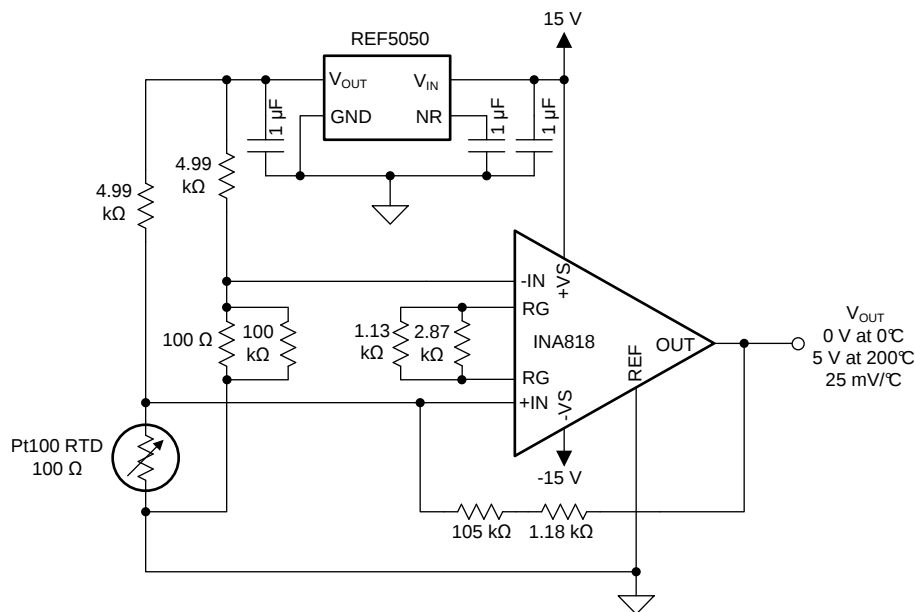


Figure 71. PLC Output Voltage vs Input Current

### 9.2.2 Resistance Temperature Detector Interface



## 10 Power Supply Recommendations

The nominal performance of the INA818 is specified with a supply voltage of  $\pm 15$  V and midsupply reference voltage. The device can also be operated using power supplies from  $\pm 2.25$  V (4.5 V) to  $\pm 18$  V (36 V) and non-midsupply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are shown in the [Typical Characteristics](#) section.

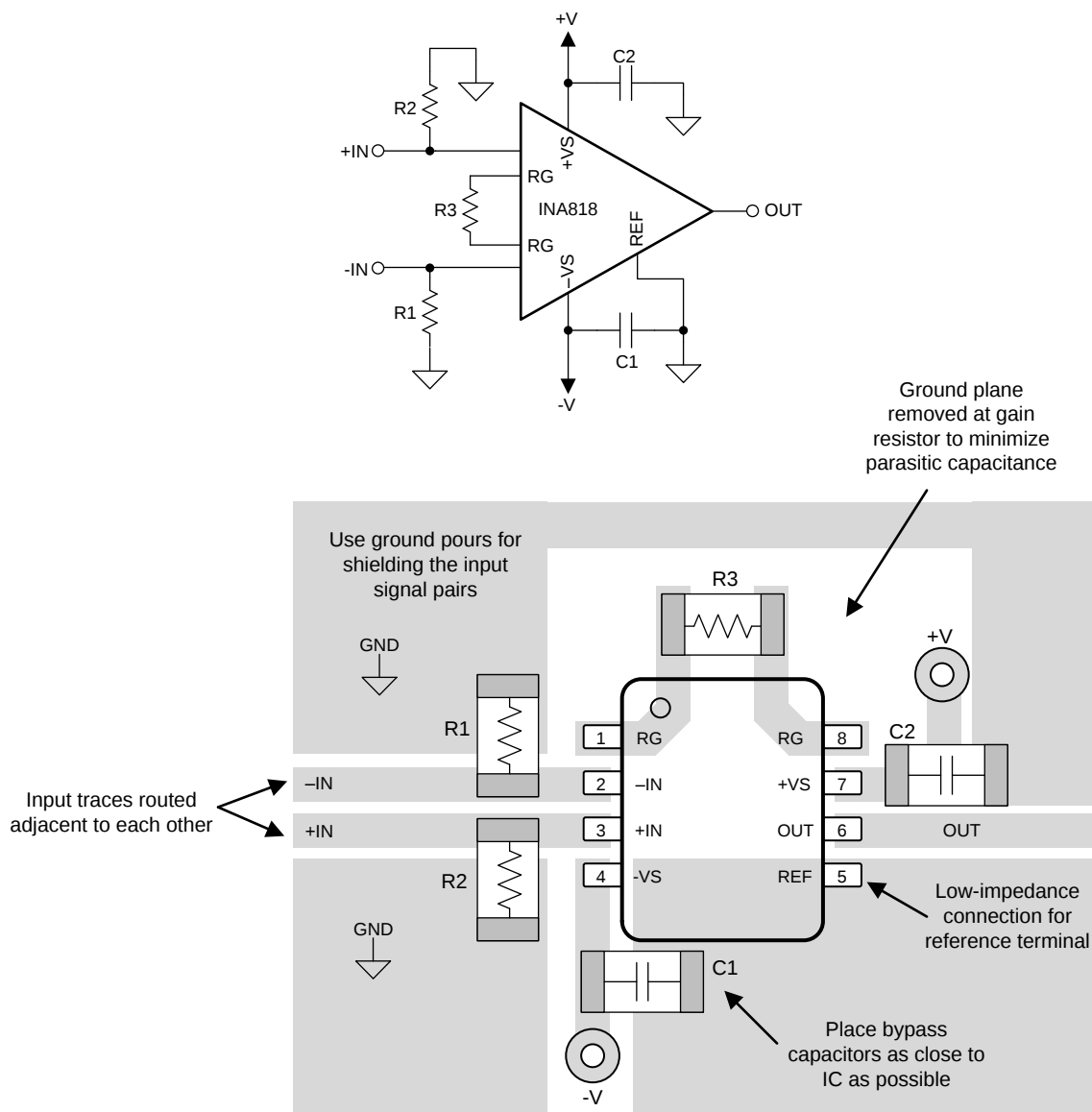
## 11 Layout

### 11.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Take care to make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. Even slight mismatch in parasitic capacitance at the gain setting pins can degrade CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS<sup>®</sup> relays to change the value of  $R_G$ , select the component so that the switch capacitance is as small as possible and most importantly so that capacitance mismatch between the RG pins is minimized.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the device itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 75](#), keeping  $R_G$  close to the pins minimizes parasitic capacitance.
- Keep the traces as short as possible.

## 11.2 Layout Example



Copyright © 2017, Texas Instruments Incorporated

**Figure 75. Example Schematic and Associated PCB Layout**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Universal Instrumentation Amplifier EVM user's guide](#)
- Texas Instruments, [Comprehensive Error Calculation for Instrumentation Amplifiers application note](#)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

Bluetooth is a registered trademark of Bluetooth SIG, Inc.

PhotoMOS is a registered trademark of Panasonic Electric Works Europe AG.

All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number     | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">INA818ID</a>  | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | INA818              |
| INA818ID.B                | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | INA818              |
| <a href="#">INA818IDR</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | INA818              |
| INA818IDR.B               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | INA818              |
| INA818IDRG4               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | INA818              |
| INA818IDRG4.B             | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | INA818              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

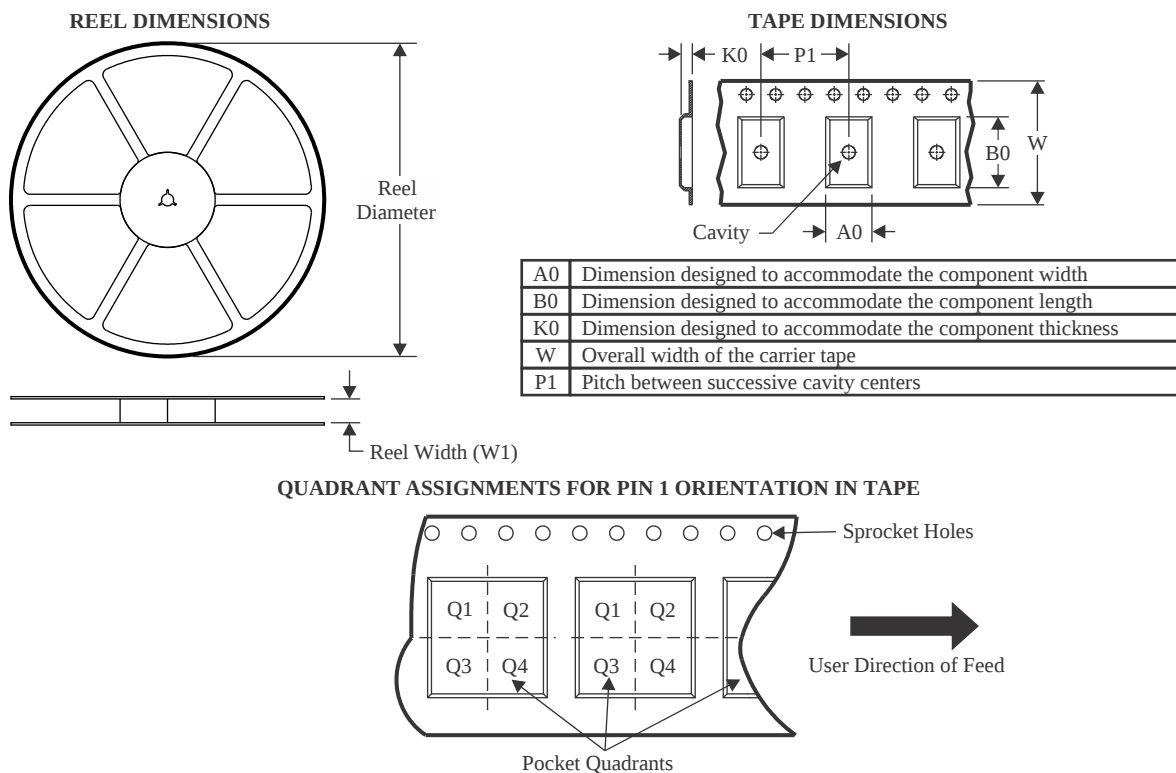
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| INA818IDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| INA818IDRG4 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

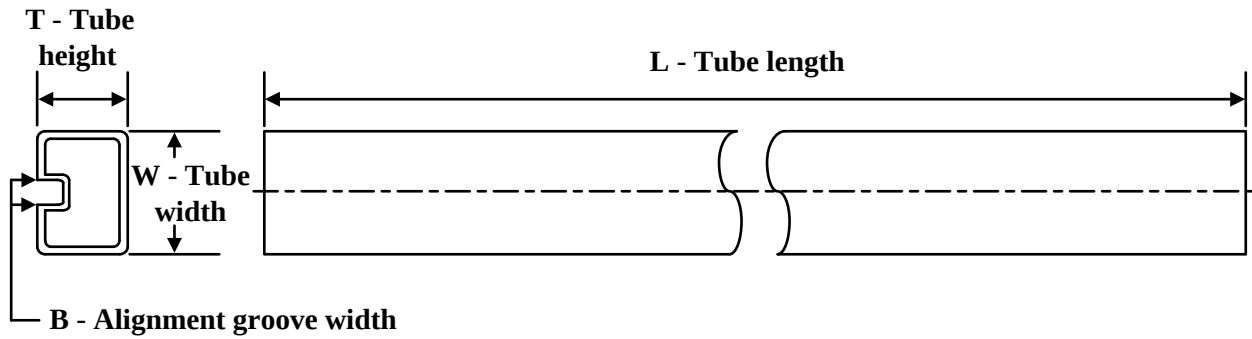
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| INA818IDR   | SOIC         | D               | 8    | 2500 | 356.0       | 356.0      | 35.0        |
| INA818IDRG4 | SOIC         | D               | 8    | 2500 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device     | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| INA818ID   | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| INA818ID.B | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |



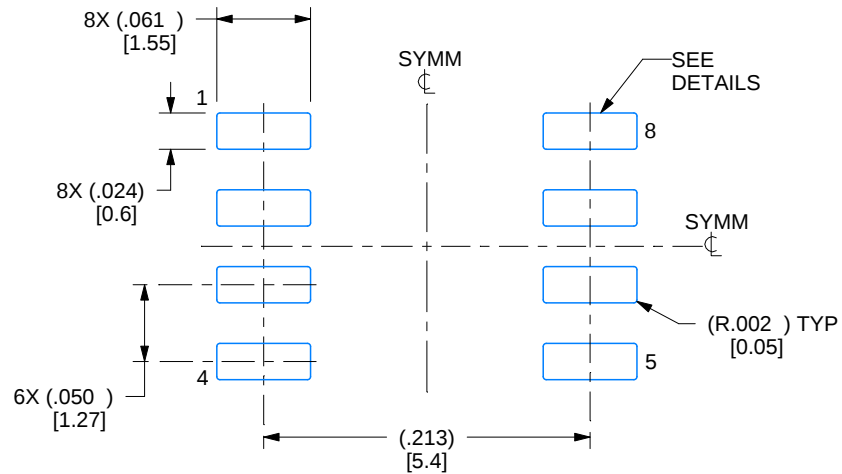
## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

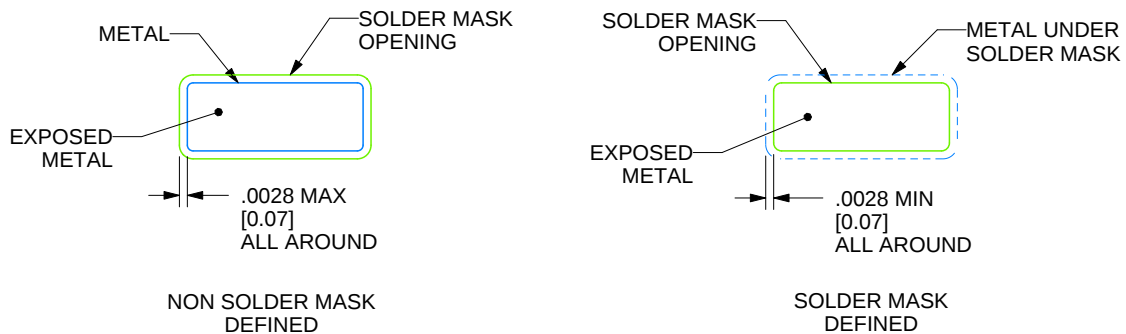
SMALL OUTLINE INTEGRATED CIRCUIT



1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

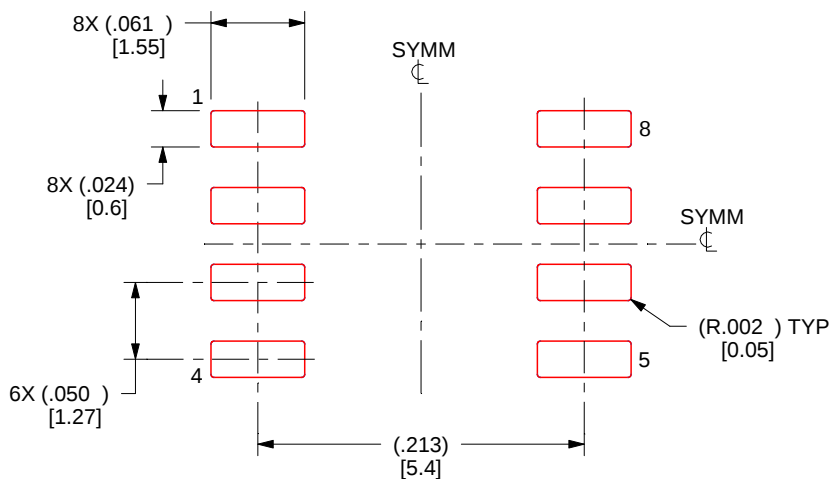
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated