

# TPS7H3302-SP and TPS7H3302-SEP 3-A DDR Radiation Hardened Termination Regulator

## 1 Features

- QMLP TPS7H3302-SP standard microcircuit drawing (SMD) available, [5962R14228](#)
- Space Enhanced Plastic Vendor item drawing available, [VID V62/22615](#)
- Total ionizing dose (TID) characterized
  - Radiation hardness assured (RHA) qualified up to total ionizing dose (TID) 100 krad(Si) or 50 krad(Si)
- Single-Event Effects (SEE) Characterized
  - Single event latch-up (SEL), single event gate rupture (SEGR), single event burnout (SEB) immune up to LET = 70 MeV-cm<sup>2</sup> /mg
  - Single event transient (SET), single event functional interrupt (SEFI), and single event upset (SEU) characterized up to 70 MeVcm<sup>2</sup> /mg
- Supports DDR, DDR2, DDR3, DDR3L, and DDR4 termination applications
- Input voltage: supports a 2.5-V and 3.3-V rail
- Separate low-voltage input (VLDOIN) down to 0.9 V for improved power efficiency
- 3-A sink and source termination regulator
- Enable input and power-good output for power supply sequencing
- VTT termination regulator
  - Output voltage range: 0.5 to 1.75 V
  - 3-A sink and source current
- Integrated precision voltage divider network with sense input
- Remote sensing (VTTSENS)
- VTTREF buffered reference
  - 49% to 51% accuracy with respect to VDDQSNS (±3 mA)
  - ±10 mA sink and source current
- Undervoltage lockout (UVLO) and overcurrent limit (OCL) functionality integrated
- Plastic package

## 2 Applications

- [Satellite electrical power system \(EPS\)](#)
- [Command and data handling \(C&DH\)](#)
- [Optical imaging payload](#)
- [Radar imaging payload](#)

## 3 Description

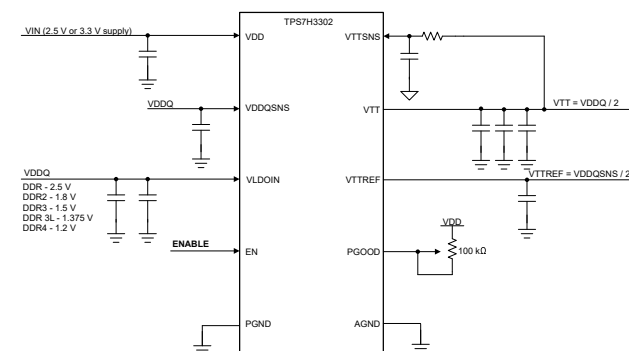
The TPS7H3302 is a radiation-hardened double data rate (DDR) 3-A termination regulator with built-in VTTREF buffer. The regulator is specifically designed to provide a complete, compact, low-noise solution for space DDR termination applications such as single board computers, solid state recorders, and payload processing.

The TPS7H3302 supports DDR VTT termination applications using DDR, DDR2, DDR3, DDR3L, and DDR4. The fast transient response of the TPS7H3302 VTT regulator allows for a very stable supply during read/write conditions. The TPS7H3302 also includes a built-in VTTREF supply that tracks VTT to further reduce the solution size. To enable simple power sequencing, both an enable input and a power-good output (PGOOD) have been integrated into the TPS7H3302. The enable signal can also be used to discharge VTT during suspend to RAM (S3) power down mode.

### Device Information

| PART NUMBER <sup>(1)</sup> | GRADE            | PACKAGE <sup>(2)</sup>                              |
|----------------------------|------------------|-----------------------------------------------------|
| 5962R1422802PYE            | QMLP-RHA         | HTSSOP (32)<br>6.10 mm × 11.00 mm<br>Mass = 0.184 g |
| TPS7H3302MDAPTSEP          | SEP              |                                                     |
| TPS7H3302EVM               | Evaluation Board | EVM                                                 |

- (1) For additional information view the [Device Options](#) table.
- (2) Dimension and mass values are nominal.



Simplified Schematic for DDR Application



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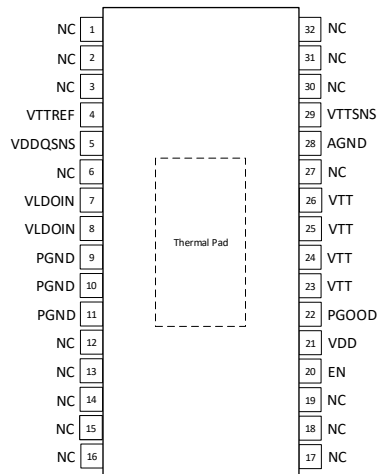
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## 4 Device Options

| GENERIC PART NUMBER | RADIATION RATING <sup>(1)</sup>                                   | GRADE <sup>(2)</sup>   | PACKAGE           | ORDERABLE PART NUMBER |
|---------------------|-------------------------------------------------------------------|------------------------|-------------------|-----------------------|
| TPS7H3302-SP        | TID of 100 krad(Si) RLAT, DSEE free to 70 MeV-cm <sup>2</sup> /mg | QMLP-RHA               | 32-Pin HTSSOP DAP | 5962R1422802PYE       |
| TPS7H3302-SEP       | TID of 50 krad(Si) RLAT, DSEE free to 48 MeV-cm <sup>2</sup> /mg  | Space Enhanced Plastic | 32-Pin HTSSOP DAP | TPS7H3302MDAPTSEP     |
| TPS7H3302EVM        | None                                                              | Evaluation Board       | EVM               | TPS7H3302EVM          |

- (1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
- (2) For additional information about part grade, view [SLYB235](#).

## 5 Pin Configuration and Functions



**Figure 5-1. DAP Package, 32-Pin HTSSOP (Top View)**

### Pin Functions

| PIN         |                          | I/O <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                |
|-------------|--------------------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME        | NO.                      |                    |                                                                                                                                                                                                                            |
| VTTREF      | 4                        | O                  | Reference output. Connect to GND through 0.1-μF ceramic capacitor.                                                                                                                                                         |
| VDDQSNS     | 5                        | I                  | VDDQ sense input. Reference input for VTTREF. <sup>(2)</sup>                                                                                                                                                               |
| VLDOIN      | 7                        | I                  | Supply voltage for the LDO. Connect to VDDQ voltage or an alternate voltage source.                                                                                                                                        |
|             | 8                        |                    |                                                                                                                                                                                                                            |
| PGND        | 9                        | —                  | Power ground. Connect to system ground.                                                                                                                                                                                    |
|             | 10                       |                    |                                                                                                                                                                                                                            |
|             | 11                       |                    |                                                                                                                                                                                                                            |
| EN          | 20                       | I                  | Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device.                                                                                                          |
| VDD         | 21                       | I                  | 2.5- or 3.3-V power supply. A ceramic decoupling capacitor with a value between 1 and 10 μF is required.                                                                                                                   |
| PGOOD       | 22                       | O                  | PGOOD output pin. PGOOD pin is an open drain output to indicate the output voltage is within specification.                                                                                                                |
| VTT         | 23                       | O                  | Power output for VTT LDO.                                                                                                                                                                                                  |
|             | 24                       |                    |                                                                                                                                                                                                                            |
|             | 25                       |                    |                                                                                                                                                                                                                            |
|             | 26                       |                    |                                                                                                                                                                                                                            |
| AGND        | 28                       | —                  | Signal ground. Connect to system ground.                                                                                                                                                                                   |
| VTTSNS      | 29                       | I                  | Voltage sense for VTT. Place capacitor close to pin. Route sense line to VTT near load.                                                                                                                                    |
| NC          | 1-3, 6, 12-19, 27, 30-32 | —                  | No connect. These pins are not internally connected. It is recommended to connect these pins to ground to prevent charge buildup; however, these pins can also be left open or tied to any voltage between ground and VDD. |
| Thermal Pad |                          | —                  | Connect to PGND. This is internally floating.                                                                                                                                                                              |

(1) I = Input, O = Output, — = Other

(2) VDDQSNS shall be connected to the regulated voltage supplying VDDQ. If the VDDQ supply is also used for VLDOIN, an RC filter is recommended to isolate transients from VLDOIN to VDDQ.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating temperature range and all voltages with respect to AGND (unless otherwise noted)<sup>(1)</sup>

|                      |                              | MIN   | MAX | UNIT |
|----------------------|------------------------------|-------|-----|------|
| Input voltage        | VDD, VLDOIN, VTTSNS, VDDQSNS | −0.36 | 3.6 | V    |
|                      | EN                           | −0.3  | 3.6 |      |
|                      | PGND to AGND                 | −0.3  | 0.3 |      |
| Output voltage       | VTT, VTTREF                  | −0.3  | 3.6 | V    |
|                      | PGOOD                        | −0.3  | 3.6 |      |
| Junction temperature | T <sub>J</sub>               | −55   | 150 | °C   |
| Storage temperature  | T <sub>stg</sub>             | −55   | 150 | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

|                    |                         |                                                                                 | VALUE | UNIT |
|--------------------|-------------------------|---------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>     | ±4000 | V    |
|                    |                         | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup> | ±750  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

all voltages with respect to AGND (unless otherwise noted)

|                      |                   | MIN   | NOM | MAX  | UNIT |
|----------------------|-------------------|-------|-----|------|------|
| Input voltage        | VDD               | 2.375 |     | 3.5  | V    |
|                      | VDDQSNS           | 1     |     | 3.5  |      |
|                      | VLDOIN            | 0.9   |     | 3.5  |      |
|                      | EN, VTTSNS, PGOOD | −0.1  |     | 3.5  |      |
|                      | PGND              | −0.1  |     | 0.1  |      |
| Output voltage       | VTT               | −0.1  |     | 3.5  | V    |
|                      | VTTREF            | −0.1  |     | 1.8  |      |
| Input current        | PGOOD             | 0     |     | 4    | mA   |
| Output current       | VTT               | −3    |     | 3    | A    |
|                      | VTTREF            | −0.01 |     | 0.01 |      |
| Junction temperature | T <sub>J</sub>    | −55   |     | 125  | °C   |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TPS7H3302-SEP | UNIT |
|-------------------------------|----------------------------------------------|---------------|------|
|                               |                                              | HTSSOP DAP    |      |
|                               |                                              | 32-PINS       |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 25.9          | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 15.9          | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 7.9           | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 0.2           | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 7.9           | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 1.1           | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

Over  $2.375 \leq VDD \leq 3.5$  V,  $VLDOIN = 1.8$  V,  $VDDQSNS = 1.8$  V,  $EN = VDD$ ,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ; Standard DDR Application; all voltages with respect to AGND, unless otherwise noted

| PARAMETER                 |                             | TEST CONDITIONS               |                                   | MIN   | TYP   | MAX   | UNIT |
|---------------------------|-----------------------------|-------------------------------|-----------------------------------|-------|-------|-------|------|
| SUPPLY CURRENTS           |                             |                               |                                   |       |       |       |      |
| I <sub>VDD</sub>          | Quiescent current           | EN = 3.3 V, no load           |                                   | 18    | 30    |       | mA   |
| I <sub>VDD(SHDN)</sub>    | Shutdown current            | EN = 0 V, no load             | VDDQSNS = 0 V                     | 1.75  | 3     |       | mA   |
|                           |                             |                               | VDDQSNS > 0.78 V                  | 5     | 6     |       |      |
| I <sub>VLDOIN</sub>       | Quiescent current of VLDOIN | EN = 3.3 V, no load           |                                   | 450   | 1200  |       | μA   |
| I <sub>VLDOIN(SHDN)</sub> | Shutdown current of VLDOIN  | EN = 0 V, no load             |                                   | 0.5   | 1     |       | μA   |
| I <sub>VDDQSNS</sub>      | VDDQSNS input current       | EN = 3.3 V                    |                                   | 4     | 6     |       | μA   |
| VTT OUTPUT                |                             |                               |                                   |       |       |       |      |
| VTT <sub>SNS</sub>        | Output DC voltage, VTT      | I <sub>VTT</sub> = 5 mA       | VDDQSNS = VLDOIN = 2.5 V (DDR1)   | 1.24  | 1.25  | 1.26  | V    |
|                           |                             |                               | VDDQSNS = VLDOIN = 1.8V (DDR2)    | 0.89  | 0.9   | 0.91  |      |
|                           |                             |                               | VDDQSNS = VLDOIN = 1.5 V (DDR3)   | 0.745 | 0.752 | 0.759 |      |
|                           |                             |                               | VDDQSNS = VLDOIN = 1.35 V (DDR3L) | 0.67  | 0.677 | 0.684 |      |
|                           |                             |                               | VDDQSNS = VLDOIN = 1.2 V (DDR4)   | 0.596 | 0.602 | 0.608 |      |
|                           |                             | I <sub>VTT</sub> = −5 mA      | VDDQSNS = VLDOIN = 2.5 V (DDR1)   | 1.25  | 1.26  | 1.27  | V    |
|                           |                             |                               | VDDQSNS = VLDOIN = 1.8V (DDR2)    | 0.9   | 0.91  | 0.92  |      |
|                           |                             |                               | VDDQSNS = VLDOIN = 1.5 V (DDR3)   | 0.752 | 0.76  | 0.768 |      |
|                           |                             |                               | VDDQSNS = VLDOIN = 1.35 V (DDR3L) | 0.675 | 0.685 | 0.692 |      |
|                           |                             |                               | VDDQSNS = VLDOIN = 1.2 V (DDR4)   | 0.602 | 0.61  | 0.618 |      |
|                           |                             | −1 A ≤ I <sub>VTT</sub> ≤ 1 A | VDDQSNS = VLDOIN = 2.5 V (DDR1)   | 1.24  | 1.26  | 1.28  | V    |
|                           |                             |                               | VDDQSNS = VLDOIN = 1.8V (DDR2)    | 0.885 | 0.910 | 0.93  |      |
|                           |                             |                               | VDDQSNS = VLDOIN = 1.5 V (DDR3)   | 0.735 | 0.76  | 0.78  |      |
|                           |                             |                               | VDDQSNS = VLDOIN = 1.35 V (DDR3L) | 0.66  | 0.69  | 0.72  |      |
|                           |                             |                               | VDDQSNS = VLDOIN = 1.2 V (DDR4)   | 0.585 | 0.6   | 0.63  |      |

## 6.5 Electrical Characteristics (continued)

Over  $2.375 \leq V_{DD} \leq 3.5$  V,  $V_{LD0IN} = 1.8$  V,  $V_{DDQSNS} = 1.8$  V,  $EN = V_{DD}$ ,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ; Standard DDR

Application; all voltages with respect to AGND, unless otherwise noted

| PARAMETER                     |                                                                                                 | TEST CONDITIONS                                                         |                          | MIN  | TYP         | MAX  | UNIT |
|-------------------------------|-------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|--------------------------|------|-------------|------|------|
| V <sub>DO</sub>               | Dropout voltage,<br>V <sub>DO</sub> = VLDOIN – VTTREF<br>VDO recorded when VTT – VTTREF = 50 mV | VDDQSNS = 2.5 V (DDR1)                                                  | I <sub>VTT</sub> = 0.5 A |      | 5           | 60   | mV   |
|                               |                                                                                                 |                                                                         | I <sub>VTT</sub> = 1 A   |      | 60          | 180  |      |
|                               |                                                                                                 |                                                                         | I <sub>VTT</sub> = 2 A   |      | 190         | 465  |      |
|                               |                                                                                                 | VDDQSNS = 1.8 V (DDR2)                                                  | I <sub>VTT</sub> = 0.5 A |      | 8           | 70   |      |
|                               |                                                                                                 |                                                                         | I <sub>VTT</sub> = 1 A   |      | 65          | 200  |      |
|                               |                                                                                                 |                                                                         | I <sub>VTT</sub> = 2 A   |      | 190         | 475  |      |
|                               |                                                                                                 | VDDQSNS = 1.5 V (DDR3)                                                  | I <sub>VTT</sub> = 0.5 A |      | 5           | 65   |      |
|                               |                                                                                                 |                                                                         | I <sub>VTT</sub> = 1 A   |      | 60          | 180  |      |
|                               |                                                                                                 |                                                                         | I <sub>VTT</sub> = 2 A   |      | 180         | 420  |      |
|                               |                                                                                                 | VDDQSNS = 1.35 V (DDR3L)                                                | I <sub>VTT</sub> = 0.5 A |      | 4           | 60   |      |
|                               |                                                                                                 |                                                                         | I <sub>VTT</sub> = 1 A   |      | 60          | 180  |      |
|                               |                                                                                                 |                                                                         | I <sub>VTT</sub> = 2 A   |      | 175         | 420  |      |
|                               |                                                                                                 | VDDQSNS = 1.2 V (DDR4)                                                  | I <sub>VTT</sub> = 0.5 A |      | 4           | 60   |      |
|                               |                                                                                                 |                                                                         | I <sub>VTT</sub> = 1 A   |      | 60          | 180  |      |
|                               |                                                                                                 |                                                                         | I <sub>VTT</sub> = 2 A   |      | 175         | 420  |      |
| VTT <sub>(TOL)</sub>          | VTT Tolerance to VTTREF (VTT – VTTREF)                                                          | I <sub>VTT</sub> = -3 A                                                 |                          | 1    | 18          | 30   | mV   |
|                               |                                                                                                 | I <sub>VTT</sub> = 3 A                                                  |                          | -30  | -15         | -1   |      |
| I <sub>LIM_SRC_VTT</sub>      | VTT sourcing current limit                                                                      | Ramp output 0 A to 10 A, record current when VTT reaches lowest value   |                          | 5    |             | 9    | A    |
| I <sub>LIM_SNK_VTT</sub>      | VTT sinking current limit                                                                       | Ramp output 0 A to -10 A, record current when VTT reaches highest value |                          | 5    |             | 10   | A    |
| R <sub>DSCHRG</sub>           | VTT discharge resistance                                                                        | VDDQSNS = 0 V, VTT = 0.3 V, EN = 0 V                                    |                          |      | 7           | 25   | Ω    |
| POWER GOOD                    |                                                                                                 |                                                                         |                          |      |             |      |      |
| V <sub>PG(LOW, Falling)</sub> | VTT PGOOD threshold with respect to VTTREF                                                      | PGOOD window lower falling threshold                                    |                          | -21% | -20%        | -18% |      |
| V <sub>PG(LOW, Rising)</sub>  |                                                                                                 | PGOOD window lower rising threshold                                     |                          | -17% | -15%        | -13% |      |
| V <sub>PG(HI, Falling)</sub>  | VTT PGOOD threshold with respect to VTTREF                                                      | PGOOD window High falling threshold                                     |                          | 13%  | 15%         | 17%  |      |
| V <sub>PG(HI, Rising)</sub>   |                                                                                                 | PGOOD window High rising threshold                                      |                          | 18%  | 20%         | 21%  |      |
| V <sub>PG(HYST)</sub>         | VTT PGOOD hysteresis                                                                            |                                                                         |                          |      | 5%          |      |      |
| t <sub>PG(delay)</sub>        | PGOOD startup delay                                                                             | Startup rising edge, VTTSENS within 20% of VTTREF                       |                          |      | 4           |      | ms   |
| t <sub>PG_BAD(delay)</sub>    | PGOOD bad delay                                                                                 | VTTSENS outside of the ±20% PGOOD window                                |                          |      | 1.95        |      | μs   |
| V <sub>PG(OL)</sub>           | Power good output low                                                                           | I <sub>PGOOD(SINK)</sub> = 4 mA                                         |                          |      |             | 0.4  | V    |
| I <sub>PG(LKG)</sub>          | Power good leakage                                                                              | VTTSENS = VTTREF (PGOOD high impedance), PGOOD = VDD + 0.2 V            |                          |      | 0.07        | 1    | μA   |
| VDDQSNS AND VTTREF            |                                                                                                 |                                                                         |                          |      |             |      |      |
| VDDQSNS <sub>UVLO</sub>       | VDDQSNS UVLO turn-on threshold                                                                  | VDDQSNS rising                                                          |                          |      | 750         | 900  | mV   |
| VDDQSNS <sub>UVLO(HYST)</sub> | VDDQSNS UVLO hysteresis                                                                         |                                                                         |                          |      | 75          | 150  |      |
| VTTREF                        | VTTREF voltage                                                                                  |                                                                         |                          |      | VDDQSNS / 2 |      | V    |

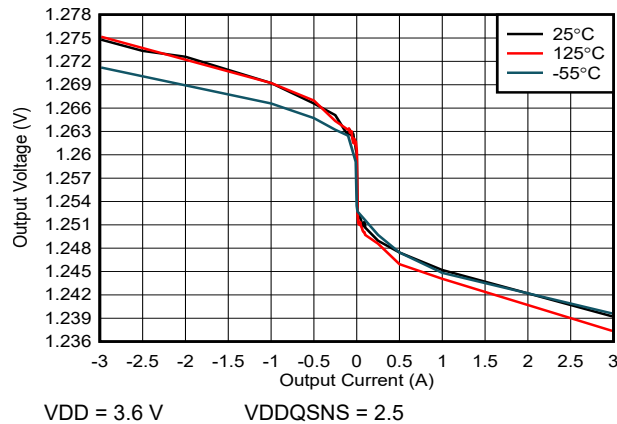
## 6.5 Electrical Characteristics (continued)

Over  $2.375 \leq VDD \leq 3.5$  V,  $VLDOIN = 1.8$  V,  $VDDQSNS = 1.8$  V,  $EN = VDD$ ,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ; Standard DDR Application; all voltages with respect to AGND, unless otherwise noted

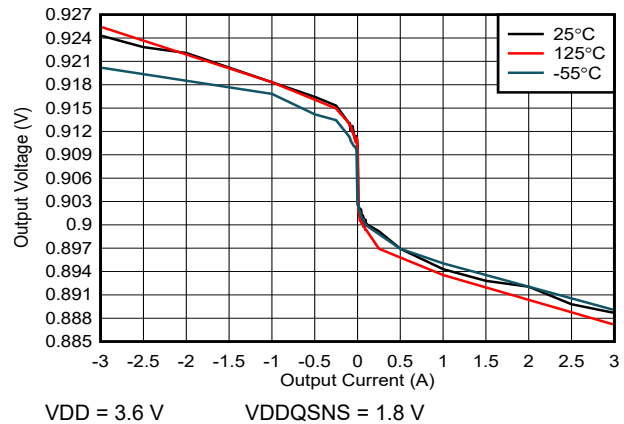
| PARAMETER              |                                           | TEST CONDITIONS                                                                           | MIN              | TYP  | MAX    | UNIT          |
|------------------------|-------------------------------------------|-------------------------------------------------------------------------------------------|------------------|------|--------|---------------|
| VTTREF                 | VTTREF voltage tolerance to VDDQSNS       | $-10 \text{ mA} \leq I_{VTTREF} \leq 10 \text{ mA}$                                       | VDDQSNS = 2.5 V  | 49%  | 51%    |               |
|                        |                                           |                                                                                           | VDDQSNS = 1.8 V  | 49%  | 51%    |               |
|                        |                                           |                                                                                           | VDDQSNS = 1.5 V  | 49%  | 51.25% |               |
|                        |                                           |                                                                                           | VDDQSNS = 1.35 V | 49%  | 51.5%  |               |
|                        |                                           |                                                                                           | VDDQSNS = 1.2 V  | 49%  | 51.5%  |               |
|                        |                                           | $-3 \text{ mA} \leq I_{VTTREF} \leq 3 \text{ mA}$                                         | VDDQSNS = 1.5 V  | 49%  | 51%    |               |
|                        |                                           |                                                                                           | VDDQSNS = 1.35 V | 49%  | 51%    |               |
|                        |                                           |                                                                                           | VDDQSNS = 1.2 V  | 49%  | 51%    |               |
| $I_{LIM\_SRC\_VTTREF}$ | VTTREF sourcing current limit             | Sourcing current ramped from 0 to 55mA. Find when VTTREF drops to half its original value | 35               | 45   |        | mA            |
| $I_{LIM\_SNK\_VTTREF}$ | VTTREF sinking current limit              | Sinking current ramped from 0 to 16.5mA. Find when VTTREF hits peak value                 | 12               | 15   |        |               |
| $I_{VTTREF(dis)}$      | VTTREF discharge current                  | EN = 0 V, VDDQSNS = 0 V, VTTREF = 0.5 V                                                   |                  | 1.3  |        | mA            |
| <b>UVLO AND ENABLE</b> |                                           |                                                                                           |                  |      |        |               |
| $VDD_{UVLO}$           | VDD UVLO turn-on threshold                |                                                                                           |                  | 2.18 | 2.3    | V             |
| $VDD_{UVLO(HYST)}$     | VDD UVLO hysteresis                       |                                                                                           |                  | 40   |        | mV            |
| $V_{IH\_EN}$           | Enable high-level input voltage (turn-on) |                                                                                           |                  |      | 1.7    | V             |
| $V_{IL\_EN}$           | Enable low-level input voltage (turn-off) |                                                                                           | 0.3              |      |        | V             |
| $V_{EN(HYS)}$          | Enable hysteresis voltage                 |                                                                                           |                  | 700  |        | mV            |
| $I_{EN(LKG)}$          | Enable input leakage current              |                                                                                           | -1               |      | 1      | $\mu\text{A}$ |

## 6.6 Typical Characteristics

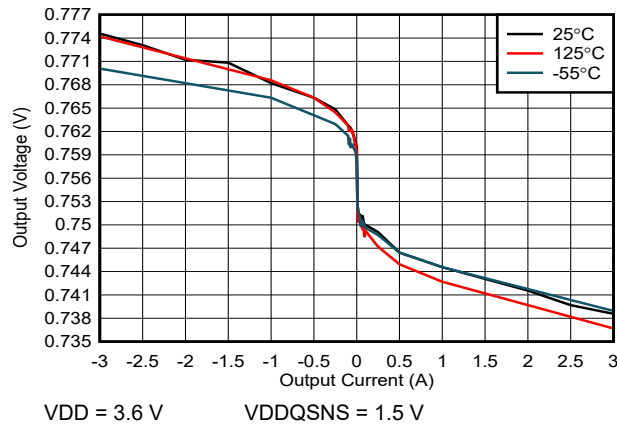
For Figure 6-1 through Figure 6-11, ( $3 \times 150\text{-}\mu\text{F}$  tantalum +  $4 \times 4.7\text{-}\mu\text{F}$  MLCC) or equivalent capacitance/ESR are used on VTT output



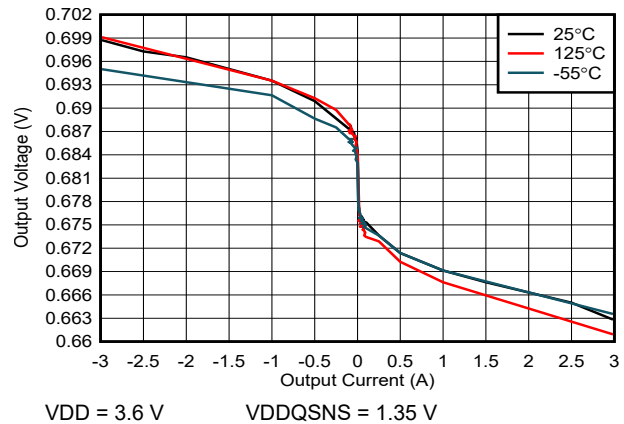
**Figure 6-1. Output Voltage vs Output Current**



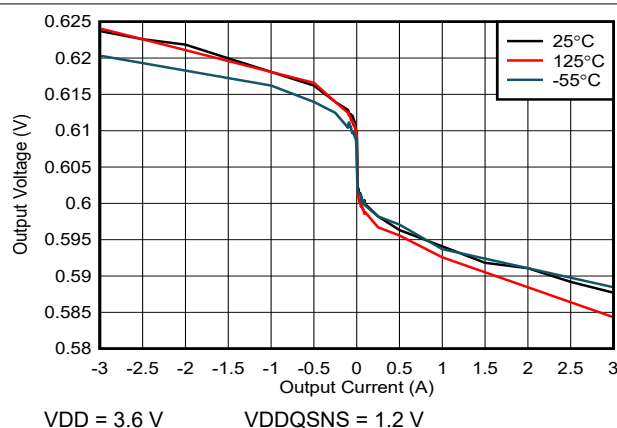
**Figure 6-2. Output Voltage vs Output Current**



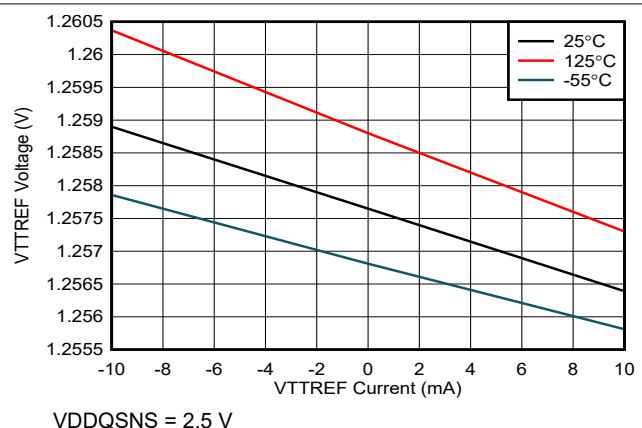
**Figure 6-3. Output Voltage vs Output Current**



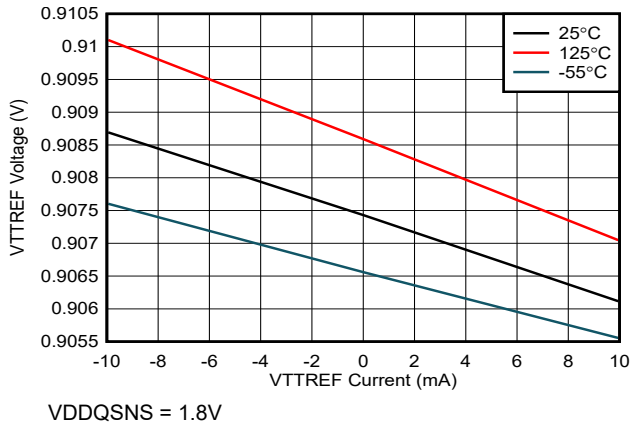
**Figure 6-4. Output Voltage vs Output Current**



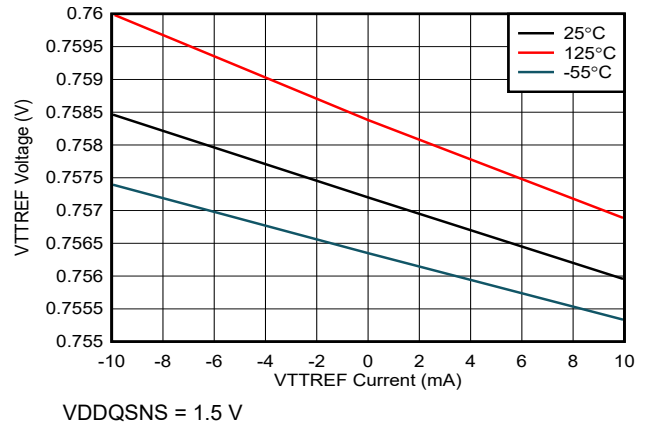
**Figure 6-5. Output Voltage vs Output Current**



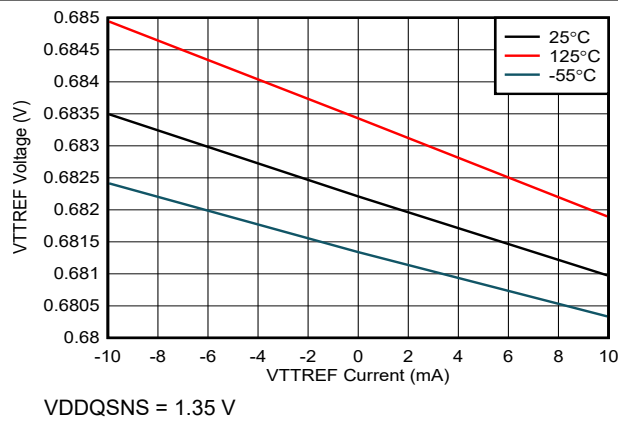
**Figure 6-6. VTTREF Voltage vs VTTREF Current**



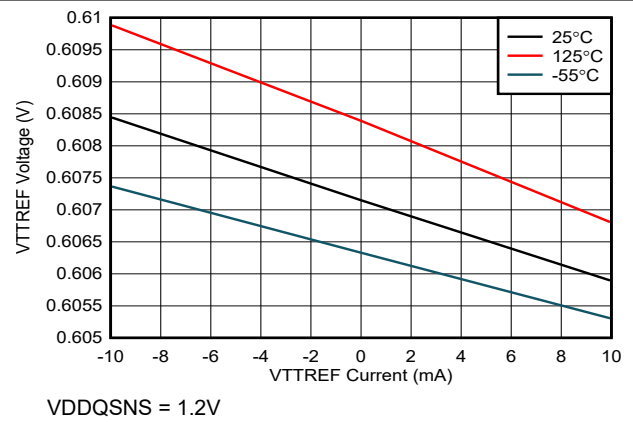
**Figure 6-7. VTTREF Voltage vs VTTREF Current**



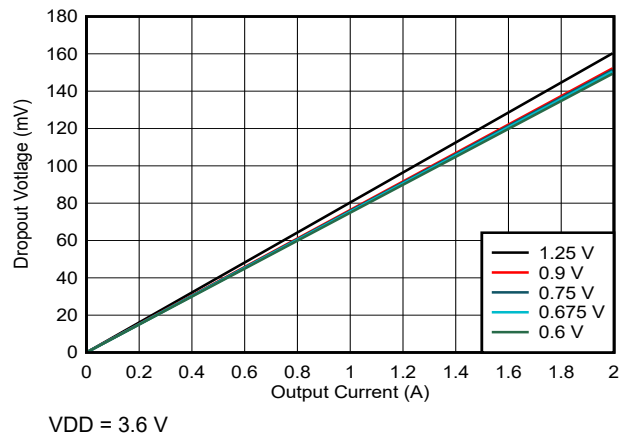
**Figure 6-8. VTTREF Voltage vs VTTREF Current**



**Figure 6-9. VTTREF Voltage vs VTTREF Current**



**Figure 6-10. VTTREF Voltage vs VTTREF Current**



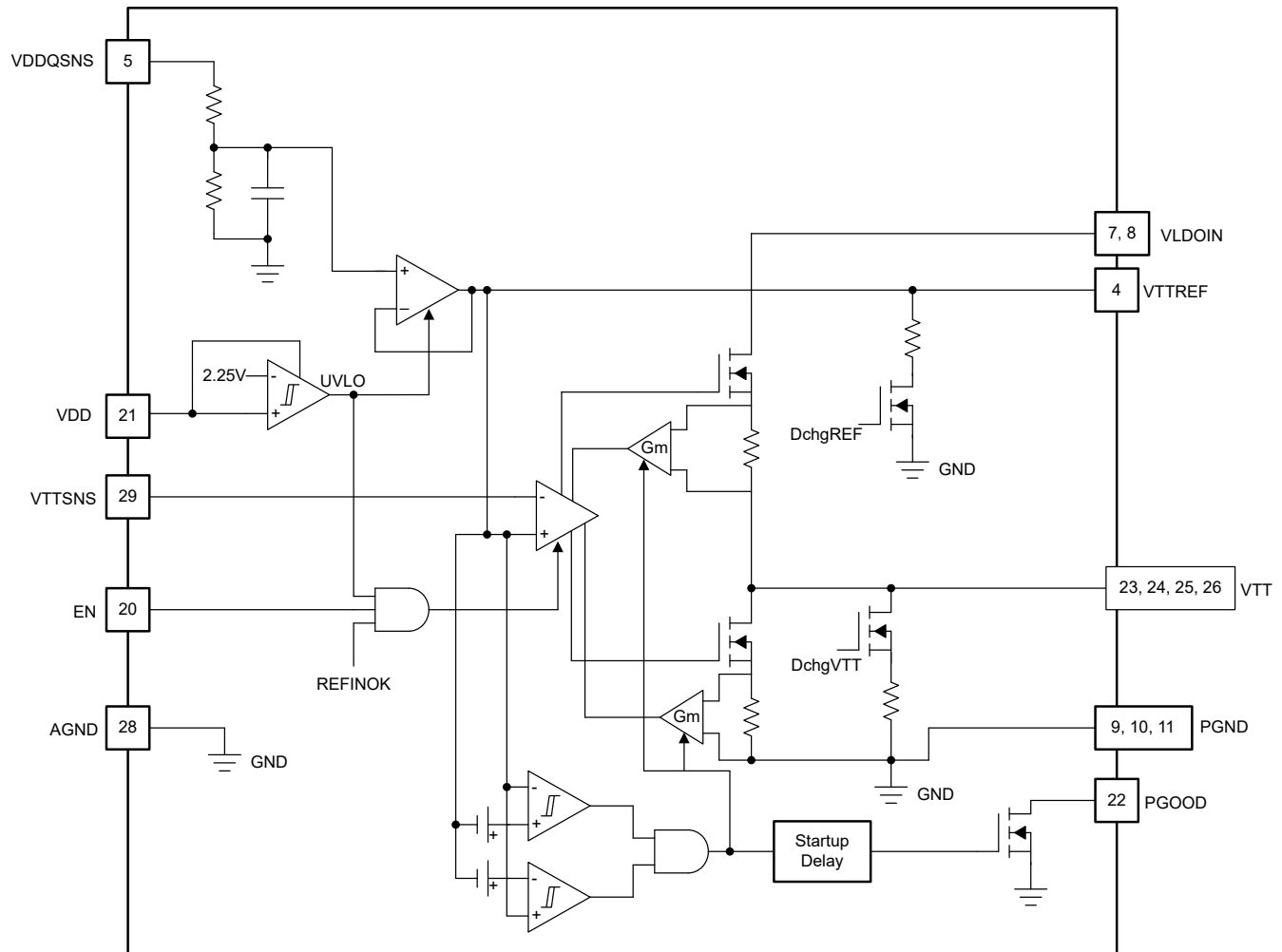
**Figure 6-11. Dropout Voltage vs Output Current**

## 7 Detailed Description

### 7.1 Overview

The TPS7H3302 device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-noise systems where space and mass are a key consideration.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 VTT Sink and Source Regulator

The TPS7H3302 is a 3-A sink and source tracking termination regulator incorporating a high performance, low-dropout (LDO) linear regulator specifically designed for low input voltage, and low external component count systems where board area is a key application parameter. The LDO regulator employs a fast feedback loop so that ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing pin (VTTSENS) should be connected to the positive pin of the output capacitor(s) as a separate trace from the high-current path of VTT.

The TPS7H3302 has a dedicated pin (VLDOIN) for connection to the VTT power supply, in order to minimize the LDO power dissipation. The minimum VLDOIN voltage is highlighted in [Electrical Characteristics](#) : TPS7H3302 (VLDOIN to VTT headroom) for various load conditions.

### 7.3.2 Reference Input (VDDQSNS)

The output voltage, VTT, is regulated to VTTREF. VDDQSNS incorporates an integrated resistor divider network. VDDQSNS should be connected to the memory supply bus (VDDQ). The TPS7H3302 supports VDDQSNS voltage from 1 V to 3.5 V, making it versatile and ideal for many types of low-power LDO applications.

### 7.3.3 Reference Output (VTTREF)

When it is configured for DDR termination applications, VTTREF buffers the DDR VTT reference voltage for the memory application. The VTTREF block consists of an on-chip 1/2 resistor divider and a low-pass filter (LPF). VTTREF tracks 1/2 of VDDQSNS typically within  $\pm 1\%$ . It is typically capable of supporting a  $\pm 10$  mA sink/source load current. VTTREF becomes active when VDDQSNS reaches 0.75V and VDD is above the UVLO threshold. When VTTREF is less than 0.675 V, VTTREF is disabled and subsequently discharges to GND through an internal MOSFET. VTT is also discharged following the discharge of VTTREF. VTTREF is independent of the EN pin state. To meet stability criteria, a ceramic capacitor of 0.1- $\mu$ F minimum must be installed close to VTTREF (pin 4). Capacitor value at VTTREF (pin 4) must not exceed 2.2  $\mu$ F.

### 7.3.4 EN Control (EN)

When EN is driven high, the TPS7H3302 VTT regulator begins normal operation. When EN is driven low, VTT discharges to GND through an internal 18- $\Omega$  (typical) MOSFET. VTTREF remains on when EN is driven low. EN is not tied high internally to prevent power sequencing issues with an external signal that may be controlling the enable. EN is a floating input and not internally tied, thus the user can have complete control over where and when the EN signal is generated. EN feeds directly into power-good (PGOOD). When enable is low, PGOOD is low.

### 7.3.5 Power-Good Function (PGOOD)

The TPS7H3302 provides an open-drain PGOOD output that goes high when the VTT output is within 20% of VTTREF (typ). PGOOD deasserts within 1.95  $\mu$ s after the output exceeds the size of the power-good window. During initial VTT startup, PGOOD asserts high 4 ms (typ) after the VTT enters power-good window. Because PGOOD is an open-drain output, a 100-k $\Omega$  pullup resistor between PGOOD and a stable active supply voltage rail is recommended for proper operation.

### 7.3.6 V<sub>TT</sub> Current Protection

The LDO has a constant overcurrent limit (OCL).

### 7.3.7 V<sub>IN</sub> UVLO Protection

For VDD undervoltage lockout (UVLO) protection, the TPS7H3302 monitors VDD voltage. When the VDD voltage is lower than the UVLO threshold voltage, both the VTT and VTTREF regulators are powered off. This shutdown is a non-latch protection.

### 7.3.8 Thermal Shutdown

The TPS7H3302 includes thermal shutdown circuitry that typically activates at 210°C with a 12°C hysteresis; when engaged the VTT and VTTREF regulators are both shutoff and discharged by the internal discharge MOSFET. This description is only provided in order to provide a complete description of the TPS7H3302; the thermal shutdown feature is not included in the product specification as the plastic package is not designed for use at 210°C.

## 7.4 Device Functional Modes

The TPS7H3302 is a 3-A sink and source LDO provides low output noise to meet system needs. In order to improve efficiency in the LDO, the TPS7H3302 LDO can operate from low VLDOIN voltage rail, thus using dual voltage source one for the VLDOIN that supports high-current and an alternate voltage sources that enables the VDDQSNS pin to track VDDQ.

In some cases VLDOIN and VDDQSNS pins are tied together. In the memory system, VDDQ is a high-current supply that powers the core, the I/O, and the logic of the memory. VTTREF is a low-current, precision reference voltage that provides a threshold between a logic high (one) and a logic low (zero) that adapts to changes in the I/O supply voltage. By providing a precision threshold that adapts to the supply voltage, VTTREF realizes wider noise margins than those possible with a fixed threshold and normal variations in termination and drive impedance. Specifications vary for different DDR technologies. For example DDR3 JEDEC JESD79-3F specifies 0.49 to 0.51 times VDDQ and draws only tens to hundreds of microamps. The TPS7H3302 VTTREF is designed to sink and source up to 10 mA.

## 8 Application and Implementation

### Note

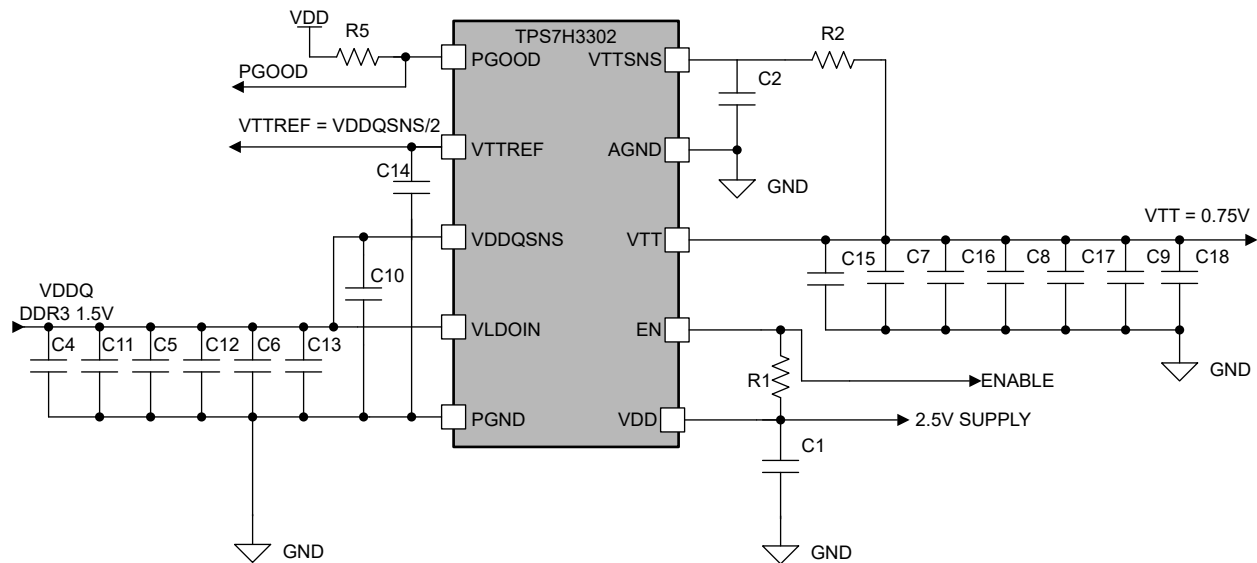
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS7H3302 device is a highly-integrated sink and source LDO. The device is targeted to support VTT voltage for DDR memory applications and is capable of sourcing and sinking 3-A load current. The TPS7H3302EVM user's guide is available on ti.com, [SLVUCK2](#). The guide highlights standard EVM test results, schematic, and bill of materials (BOM) for reference.

### 8.2 Typical Application

The design example describes a 2.5-V  $V_{IN}$ , DDR3 configuration.



**Figure 8-1. Typical Application Schematic**

## 8.2.1 Design Requirements

See the [Section 6.3](#) for recommended limits.

## 8.2.2 Detailed Design Procedure

**Table 8-1. Design Example 1 List of Materials**

| REFERENCE DESIGNATOR      | DESCRIPTION | SPECIFICATION     | PART NUMBER        | MANUFACTURER |
|---------------------------|-------------|-------------------|--------------------|--------------|
| R1, R5                    | Resistor    | 20 k $\Omega$     | RC0603JR-0720KL    | Yageo        |
| R2                        |             | 392 $\Omega$      | RC0603FR-07392RL   | Yageo        |
| C1, C4, C5, C6, C11, C12, | Capacitor   | 10 $\mu$ F, 16 V  | GCM31CR71C106KA64K | Murata       |
| C2                        |             | 1000 pF, 10 V     | CC0603KRX7R7BB102  | Yageo        |
| C7, C8, C9, C18           |             | 4.7 $\mu$ F, 10 V | 1210ZC475KAT2A     | AVX          |
| C10                       |             | 1000 pF, 100 V    | 06031C102KAT2A     | AVX          |
| C13, C15, C16, C17        |             | 150 $\mu$ F, 10 V | T530D157M010ATE005 | Kemet        |
| C14                       |             | 2.2 $\mu$ F, 25 V | 08053C225KAT2A     | AVX          |

### 8.2.2.1 VDD Capacitor

Add a ceramic capacitor, with a value between 1- and 10- $\mu$ F, placed close to the VDD pin to minimize high frequency noise from the supply.

### 8.2.2.2 VLDO Input Capacitor

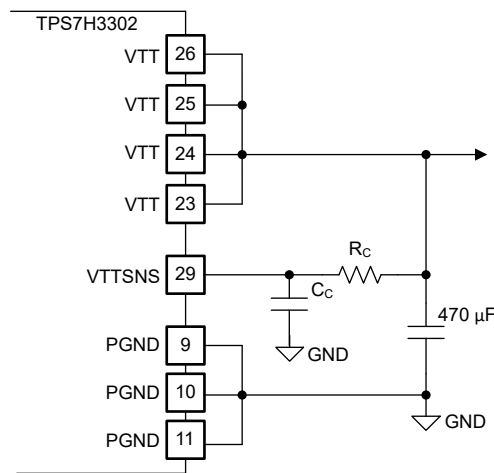
Depending on the trace impedance between the VLDOIN/VDDQ bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN/VDDQ input capacitor. Use a 150- $\mu$ F (or greater) tantalum capacitor in parallel with a 4.7- $\mu$ F ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at VTT.

### 8.2.2.3 VTT Output Capacitor

For stable operation, the total capacitance of the VTT output pin must be greater than 470  $\mu\text{F}$ . Attach three, 3  $\times$  150- $\mu\text{F}$  low-ESR tantalum capacitors in parallel with four 4.7  $\mu\text{F}$  ceramic capacitors to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL). If the total parallel ESR is greater than 2 m $\Omega$ , insert an R-C filter between the output and the VTTSNS input to achieve loop stability. The R-C filter time constant should be almost the same as or slightly lower than the time constant of the output capacitor and its ESR.

### 8.2.2.4 VTTSNS Connection

To achieve tight regulation with minimum effect of trace resistance, a remote sensing pin (VTTSNS) should be connected to the positive pin of the VTT pin output capacitor or capacitors as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSNS pin in case the ESR of the VTT output capacitor or capacitors is larger than 2 m $\Omega$ . The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.



**Figure 8-2. RC Filter for VTTSNS**

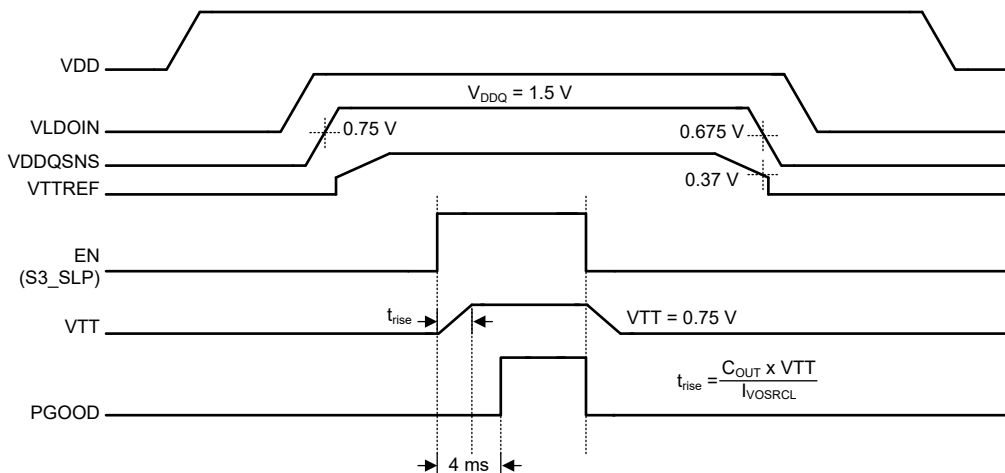
### 8.2.2.5 Low VDD Applications

TPS7H3302 can be used in an application system where either a 2.5-V rail or a 3.3-V rail is available. The TPS7H3302 minimum input voltage requirement is 2.375 V. If a 2.5-V rail is used, ensure that the absolute minimum voltage (both DC and transient) at the device pin is 2.375 V or greater. The voltage tolerance for a 2.5-V rail input is between  $\pm 5\%$  accuracy, or better.

### 8.2.2.6 S3 and Pseudo-S5 Support

The TPS7H3302 provides S3 support by an EN function. The EN pin could be connected to an SLP\_S3 signal in the end application. Both VTTREF and VTT are on when EN = high (S0 state). VTTREF is maintained while VTT is turned off and discharged via an internal discharge MOSFET when EN = low (S3 state). Please notice that the EN signal controls only the output buffer for VTT and therefore, while in S3 state, VDDQSNS is present in order to maintain data in volatile memory. As a result, when EN is set high to exit the S3 state, it is desired to bring VTT into regulation as fast as possible. This causes an output current controlled by the current limit of the device and the output capacitors.

When EN = low and the VDDQSNS voltage is less than 0.75 V (typically), TPS7H3302 enters pseudo-S5 state. Both VTT and VTTREF outputs are turned off and discharged to GND through internal MOSFETs when pseudo-S5 support is engaged (S4/S5 state). [Figure 8-3](#) shows a typical startup and shutdown timing diagram for an application that uses S3 and pseudo-S5 support.

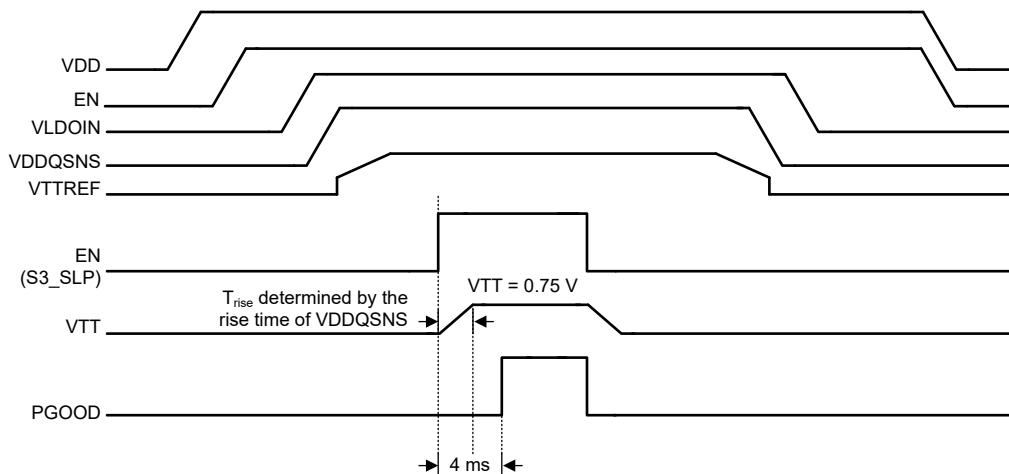


**Figure 8-3. Typical Timing Diagram for S3 and Pseudo-S5 Support**

### 8.2.2.7 Tracking Startup and Shutdown

The TPS7H3302 supports tracking startup of VDDQ and shutdown when EN is tied directly to the system bus and not used to turn on or turn off the device. During tracking startup, VTT follows VTTREF once VDDQSNS voltage is greater than 0.75 V. VDDQSNS incorporates a resistor divider network and a time constant of about 445  $\mu$ s. The rise time of the VTT output is then a function of the rise time of VDDQSNS. If the VDDQSNS rise time is larger than 445  $\mu$ s. Typically PGOOD is asserted 4 ms after VTT is within  $\pm 20\%$  of VTTREF. During tracking shutdown, VTT falls following VTTREF until VTTREF reaches 0.37 V (typically). Once VTTREF falls below 0.37 V, the internal discharge MOSFETs are turned on and quickly discharge both VTTREF and VTT to GND. PGOOD is deasserted once VTT is beyond the  $\pm 20\%$  range of VTTREF. Figure 8-4 shows the typical timing diagram for an application that uses tracking startup and shutdown.

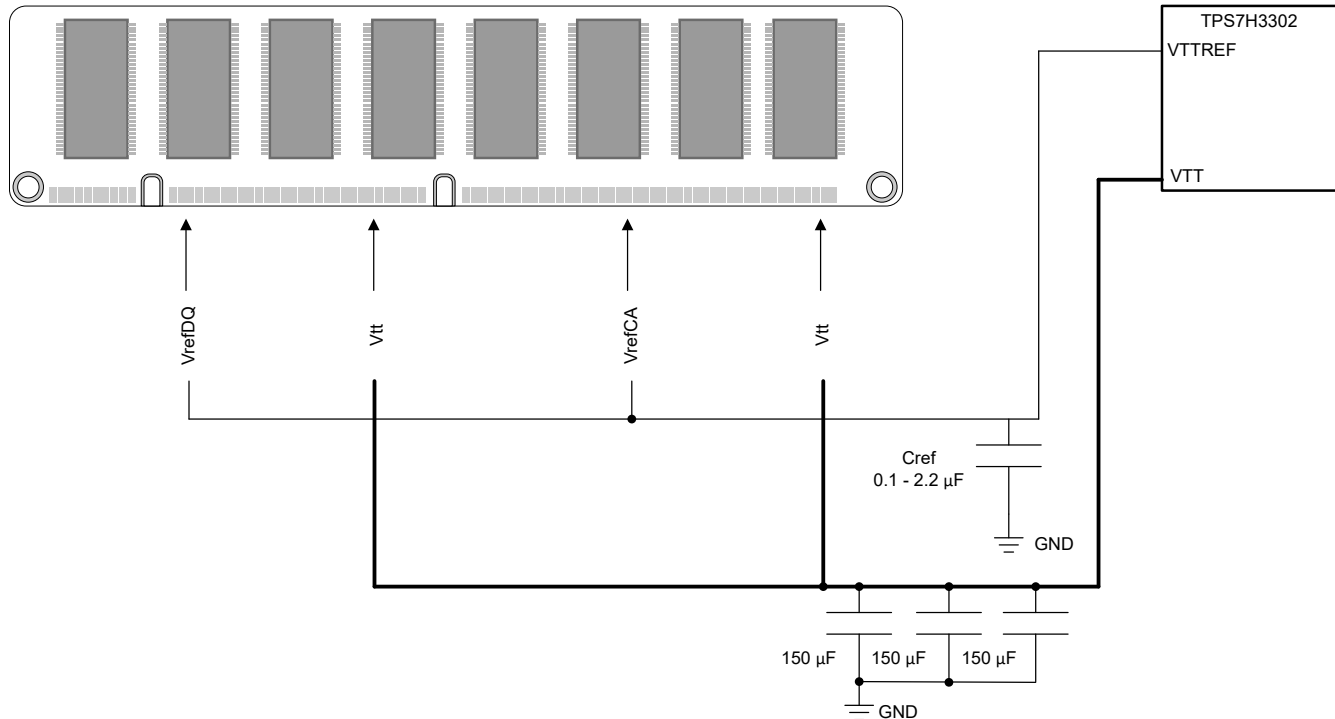
There are no sequencing requirements between VDD and VLDOIN. If VLDOIN is applied first followed by VDD there is no issue. VDD UVLO protection monitors VDD voltage. When VDD is lower than UVLO threshold both VTT and VTTREF regulators are powered off.



**Figure 8-4. Typical Timing Diagram of Tracking Startup and Shutdown**

### 8.2.2.8 Output Tolerance Consideration for VTT DIMM or Module Applications

The TPS7H3302 is specifically designed to power up the memory termination rail (as shown in Figure 8-5). The DDR memory termination structure determines the main characteristics of the VTT rail, which is to be able to sink and source current while maintaining acceptable VTT tolerance. See Figure 8-6 for typical characteristics for a single memory cell.



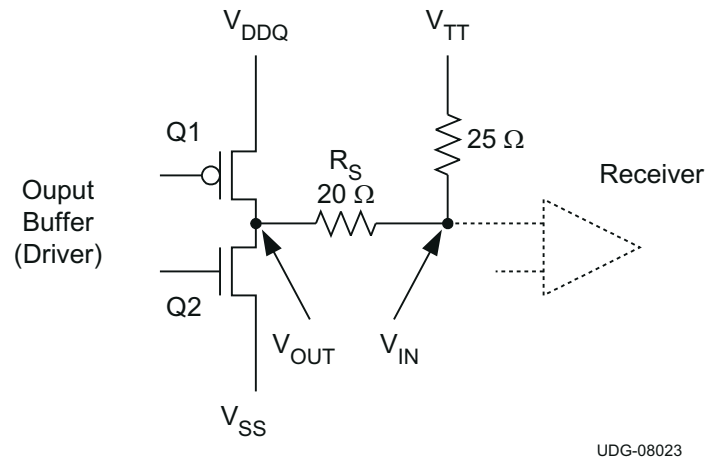
**Figure 8-5. Typical Application Diagram for DDR3 VTT DIMM/Module Using TPS7H3302**

In Figure 8-6, when Q1 is on and Q2 is off:

- Current flows from VDDQ via the termination resistor to VTT.
- VTT sinks current.

In Figure 8-6, when Q2 is on and Q1 is off:

- Current flows from VTT via the termination resistor to GND.
- VTT sources current.



UDG-08023

**Figure 8-6. DDR Physical Signal System SSTL Signaling**

Because VTT accuracy has a direct impact on the memory signal integrity, it is imperative to understand the tolerance requirement on VTT. Based on JEDEC VTT specifications for DDR and DDR2. See [Table 8-2](#) for detailed information and JEDEC relevant specifications.

$V_{TTREF} - 40\text{ mV} < V_{TT} < V_{TTREF} + 40\text{ mV}$ , for both DC and AC conditions

The specification itself indicates that VTT must keep track of VTTREF for proper signal conditioning.

The TPS7H3302 specifies the regulator output voltage to be:

$V_{TTREF} - 30\text{ mV} < V_{TT} < V_{TTREF} + 30\text{ mV}$ , for both DC and AC conditions and  $-3\text{ A} < I_{VTT} < 3\text{ A}$ .

The regulator output voltage is measured at the regulator side, not the load side. The tolerance is applicable to DDR, DDR2, DDR3 and low-power DDR3/DDR4 applications (see [Table 8-2](#) for detailed information). To meet the stability requirement, a minimum output capacitance of 470  $\mu\text{F}$  is needed, combination of both tantalum and ceramic capacitors. Considering the actual tolerance on the MLCC capacitors, four 4.7- $\mu\text{F}$  ceramic capacitors in parallel with 3  $\times$  150- $\mu\text{F}$  low-ESR tantalum capacitor are sufficient to meet the above requirement. Higher ESR tantalum capacitors will require multiple tantalum capacitors in parallel with ceramic capacitors to meet system needs.

**Table 8-2. DDR, DDR2, DDR3, and LP DDR3 Termination Technology and Differences**

|                              | DDR                                                            | DDR2                                                                                                                                                                                        | DDR3                                                                                                                                                                                        | LOW POWER DDR3 (DDR3L)         |
|------------------------------|----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| FSB data rates               | 200, 266, 333 and 400 MHz                                      | 400, 533, 677 and 800 MHz                                                                                                                                                                   | 800, 1066, 1330 and 1600 MHz                                                                                                                                                                | Same as DDR3                   |
| Termination                  | Motherboard termination to VTT for all signals                 | On-die termination for data group. VTT used for termination of address, command and control signals.                                                                                        | On-die termination for data group. VTT used for termination of address, command and control signals.                                                                                        | Same as DDR3                   |
| Termination current demand   | Max sink and source transient currents of up to 2.6 A to 2.9 A | Not as demanding <ul style="list-style-type: none"> <li>Only 34 signals (address, command, control) tied to VTT</li> <li>ODT handles data signals</li> </ul> Less than 1 A of burst current | Not as demanding <ul style="list-style-type: none"> <li>Only 34 signals (address, command, control) tied to VTT</li> <li>ODT handles data signals</li> </ul> Less than 1 A of burst current | Same as DDR3                   |
| Voltage level                | 2.5-V core and I/O 1.25-V VTT                                  | 1.8-V core and I/O 0.9-V VTT                                                                                                                                                                | 1.5-V core and I/O 0.75-V VTT                                                                                                                                                               | 1.35-V core and I/O 0.68-V VTT |
| Relevant JEDEC specification | JESD79F (SSTL_2 JESD8-9B)                                      | DDR2 JESD79-2F (SSTL_18 JESD8-15)                                                                                                                                                           | DDR3 JESD79-3F                                                                                                                                                                              | DDR3L JESD79-3-1A.01           |

The TPS7H3302 is designed as a Gm-driven LDO. The voltage droop between the reference input and the output regulator is determined by the transconductance and output current of the device. The typical Gm is 250 S at 3 A and changes with respect to the load in order to conserve the quiescent current (that is, the Gm is very low at no load condition). The Gm LDO regulator is a single pole system. Its unity gain bandwidth for the voltage loop is only determined by the output capacitance, as a result of the bandwidth nature of the Gm. (See [Equation 1](#))

$$F_{UGBW} = \frac{G_m}{2 \times \pi \times C_{OUT}} \quad (1)$$

where

- $F_{UGBW}$  is the unity gain bandwidth
- $G_m$  is transconductance
- $C_{OUT}$  is the output capacitance

There are two limitations to this type of regulator when it comes to the output bulk capacitor requirement. To maintain stability, the zero location contributed by the ESR of the output capacitors should be greater than the –3-dB point of the current loop. This constraint means that higher ESR capacitors should not be used in the design. In addition, the impedance characteristics of the ceramic capacitor should be well understood in order to prevent the gain peaking effect around the Gm –3-dB point because of the large ESL, the output capacitor, and parasitic inductance of the VTT trace.

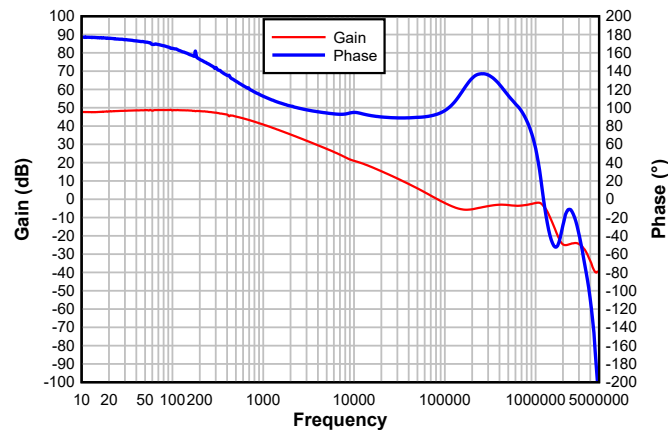
[Figure 8-7](#) shows the bode plot simulation for a typical DDR3 configuration of the TPS7H3302, where:

- $V_{DD} = 2.4 \text{ V}$
- $V_{VLDOIN} = 1.5 \text{ V}$
- $V_{TT} = 0.75 \text{ V}$
- $I_{IO} = 3 \text{ A}$
- $3 \times 150\text{-}\mu\text{F}$  low-ESR tantalum capacitors (T530D157M010ATE005) in parallel with  $4 \times 4.7\text{-}\mu\text{F}$  ceramic capacitor
- $ESR = 1.66 \text{ m}\Omega$
- $ESL = 800 \text{ pH}$

The unity-gain bandwidth is approximately 85 kHz and the phase margin is 92°. The 0-dB level is crossed, the gain peaks because of the ESL effect. However, the peaking is kept well below 0 dB.

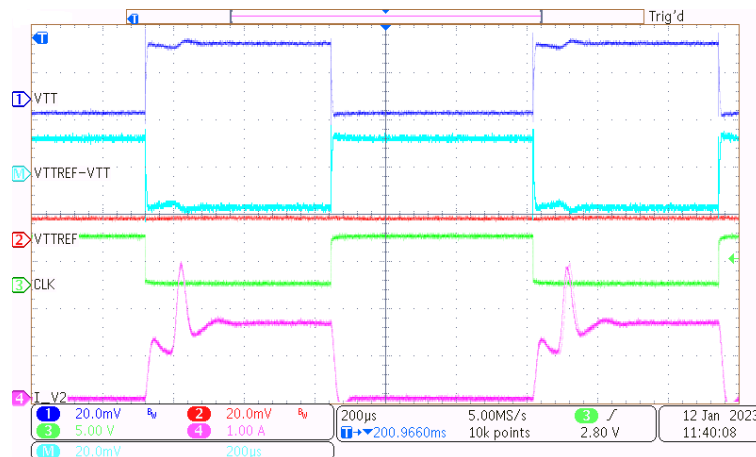
### **Bode Plot for DDR3 VDDQSN5 = 1.5V**

VTT load 3 A



**Figure 8-7. Bode Plot for a Typical DDR3 Configuration**

The figure below shows the Load Regulation and Transient Plot shows the transient response for a typical DDR3 configuration. When the regulator is subjected to a  $\pm 1.875$ -A load step. The current shown only represents the device sourcing 1.875 A due to location of current probe.



**Figure 8-8. Transient Plot**

### 8.2.2.9 LDO Design Guidelines

For TPS7H3302, a minimum of 420 mV ( $V_{LDOINMIN} - V_{TMAX}$ ) is needed in order to support a Gm driven sourcing current of 2 A based on the specified dropout voltage maximum at  $V_{DDQSNS} = 1.5$  V. Because the TPS7H3302 is essentially a Gm-driven LDO, its impedance characteristics are both a function of the  $1/G_m$  and  $R_{DS(on)}$  of the sourcing MOSFET (see [TPS7H3302 Impedance Characteristics](#)). The current inflection point of the design is between 3 A and 4 A. When  $I_{SRC}$  is less than the inflection point, the LDO is considered to be operating in the Gm region; when  $I_{SRC}$  is greater than the inflection point but less than the overcurrent limit point, the LDO is operating in the  $R_{DS(on)}$  region. The typical sourcing  $R_{DS(on)}$  is 154 m $\Omega$  with  $V_{IN} = 3$  V and  $T_J = 125^\circ\text{C}$ .

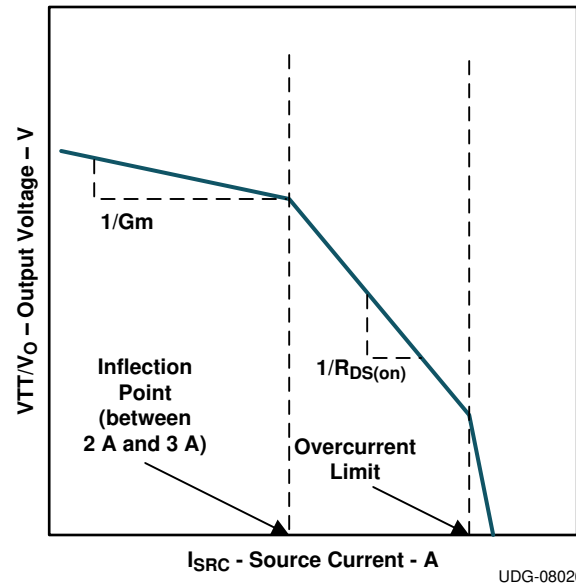


Figure 8-9. TPS7H3302 Impedance Characteristics

### 8.2.3 Application Curve

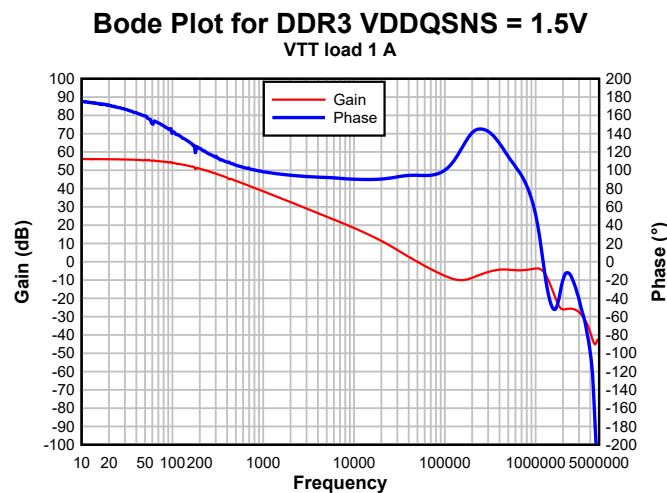


Figure 8-10. DDR2 2-A Load  $V_{DD} = 2.4$  V,  $V_{TT} = 0.9$  V

## 8.3 Power Supply Recommendations

TPS7H3302 is designed to support DDR, DDR2, DDR3, DDR3L, and DDR4 VTT applications. TPS7H3302 VLDOIN supports voltage range from 0.9 V to 3.5 V. The supply must be well regulated. Having a separate VLDOIN supply from DDR VDDQ allows designer to optimize system efficiency. VDD is used to bias the TPS7H3302 IC and its voltage range from 2.375 V to 3.5 V. This supply must be well regulated and bypassed with a ceramic capacitor with a value of 1  $\mu$ F and 10  $\mu$ F. TI recommends that VLDOIN and DDR supply VDDQ be isolated from each other. If this is not possible then an RC filter must be used to isolate VLDOIN and VDDQSNs. However, in so doing the dynamic tracking of VTT and VTTREF will be reduced. See the EVM user's guide [SLVUCK2](#) for additional details.

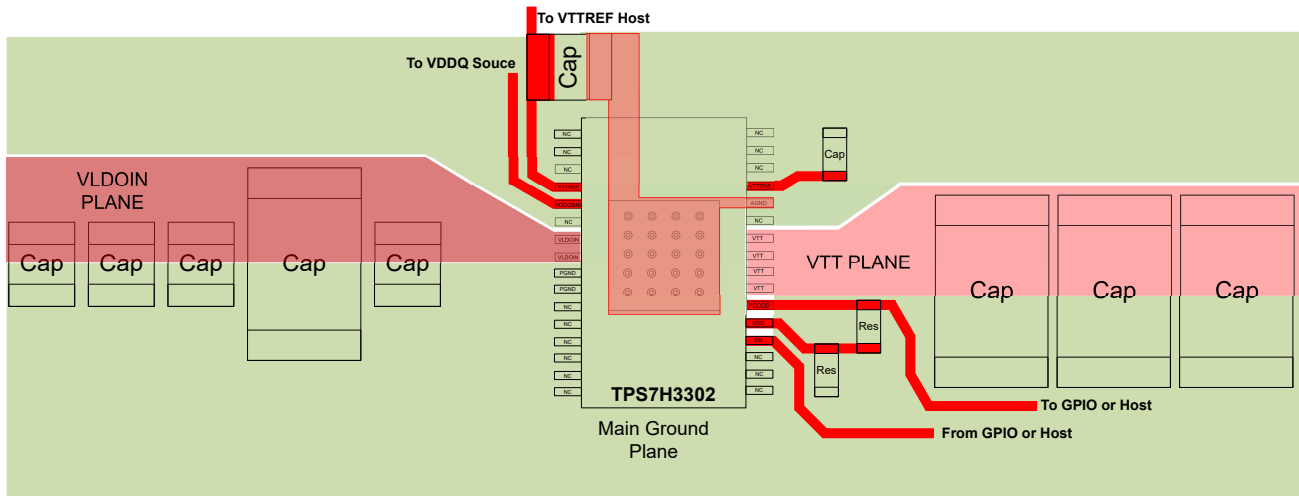
## 8.4 Layout

### 8.4.1 Layout Guidelines

Consider the following points before starting the TPS7H3302 layout design.

- The input bypass capacitor for VLDOIN should be placed as close as possible to the pin with short and wide connections.
- The output capacitor for VTT should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL trace inductance.
- VTTSNS should be connected to the positive node of VTT output capacitors as a separate trace from the high-current power line. This configuration is strongly recommended to avoid additional ESR and/or ESL. If sensing the voltage at the point of the load is required, it is recommended to attach the output capacitor or capacitors at that point. Also, it is recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the output capacitor or capacitors.
- Consider adding low-pass filter at VTTSNS if the ESR of the VTT output capacitor or capacitors is larger than 2 m $\Omega$ .
- VDDQSNs can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise-generating lines.
- The negative node of the VTT output capacitor or capacitors and the VTTREF capacitor should be tied together by avoiding common impedance to the high-current path of the VTT sink and source current.
- The GND and PGND pins should be connected to the thermal land underneath the die pad with multiple vias connecting to the internal system ground planes (for better result, use at least two internal ground planes). Use as many vias as possible to reduce the impedance between PGND/GND and the system ground plane. Also, place bulk caps close to the DIMM/module or memory load point and route the VTTSNS to the DIMM/module load sense point.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package's thermal pad. Numerous vias, 0.33 mm in diameter or smaller, connected from the thermal land to the internal/solder side ground plane or planes should also be used to help dissipation.

## 8.4.2 Layout Example



**Figure 8-11. Layout Example**

## 8.4.3 Thermal Considerations

VTT current can flow in both source and sink directions. As the TPS7H3302 is a linear regulator, power is dissipated internal to the device. When the device is sourcing current, the voltage difference between VLDOIN and VTT times IO ( $I_{IO}$ ) current becomes the power dissipation as shown in Equation 2.

$$P_{DISS\_SRC} = (V_{VLDOIN} - V_{VO}) \times I_{O\_SRC} \quad (2)$$

In this case, if VLDOIN is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, VTT voltage is applied across the internal LDO regulator and the power dissipation ( $P_{DISS\_SNK}$ ) can be calculated by Equation 3.

$$P_{DISS\_SNK} = V_{VO} \times I_{O\_SNK} \quad (3)$$

Because the device does not sink and source current at the same time and the IO current may vary rapidly with time, the actual power dissipation should be the time average of the above dissipations over the thermal relaxation duration of the system. Another source of power consumption is the current used for the internal current control circuitry from the VDD supply and the VLDOIN supply. This can be estimated as 5 mW or less during normal operating conditions. This power must be effectively dissipated from the package.

The thermal performance of an LDO depends on the printed circuit board (PCB) layout.

To further improve the thermal performance of this device, using a larger than recommended thermal land as well as increasing the number of vias helps lower the thermal resistance from junction to heat slug.

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [TPS7H3302-SEP Single-Event Effects Summary radiation report](#) (SLVK132)
- Texas Instruments, [TPS7H3302EVM-CVAL \(HREL022\) user's guide](#) (SLVUCK2)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (May 2023) to Revision B (December 2023)                                                                        | Page |
|-----------------------------------------------------------------------------------------------------------------------------------------|------|
| • Changed TPS7H3302-SP status from "Product Preview" to "Production Data".....                                                          | 1    |
| • Removal of "Product Preview" for TPS7H3302-SP.....                                                                                    | 3    |
| • Removed typical thermal shutdown.....                                                                                                 | 5    |
| • Updated VTTREF accuracy to a percentage difference from VDDQSNs (DDR4, DDR3L, DDR3, DDR2 and DDR) at $\pm 10$ mA and $\pm 3$ mA ..... | 5    |
| • Modified description for Thermal Shutdown.....                                                                                        | 14   |
| • Updated part reference from TPS7H3302-SEP to TPS7H3302 in image.....                                                                  | 17   |
| • Change of part reference in image from TPS7H3302-SEP to TPS7H3302.....                                                                | 20   |
| • Correction of graphical error in Layout Example.....                                                                                  | 27   |

| Changes from Revision * (February 2023) to Revision A (May 2023)                    | Page |
|-------------------------------------------------------------------------------------|------|
| • Changed TPS7H3302-SEP status from "Advance Information" to "Production Data"..... | 1    |
| • Addition of Product Preview for QMLP version TPS7H3302-SP.....                    | 1    |

- 
- Incorporation of TPS7H3302-SP (Product Preview) radiation ratings in Features Section and Device Options Table..... [1](#)
-

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C)             | Part marking<br>(6) |
|-----------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------------------|---------------------|
| <a href="#">5962R1422802PYE</a>   | Active        | Production           | HTSSOP (DAP)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -55 to 125               | R1422802PY          |
| <a href="#">TPS7H3302MDAPTSEP</a> | Active        | Production           | HTSSOP (DAP)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -55 to 125               | TPS7H3302           |
| V62/22615-01XE                    | Active        | Production           | HTSSOP (DAP)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | See<br>TPS7H3302MDAPTSEF | TPS7H3302           |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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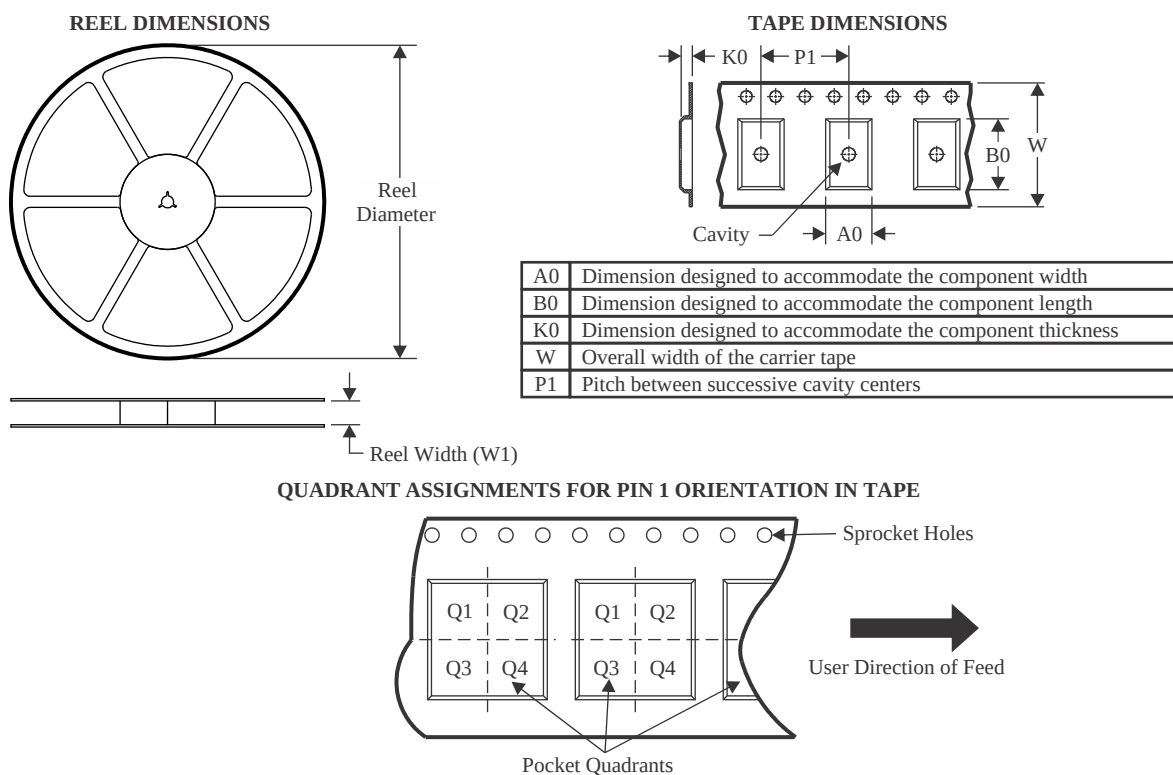
**OTHER QUALIFIED VERSIONS OF TPS7H3302-SEP, TPS7H3302-SP :**

- Catalog : [TPS7H3302-SEP](#)
- Space : [TPS7H3302-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

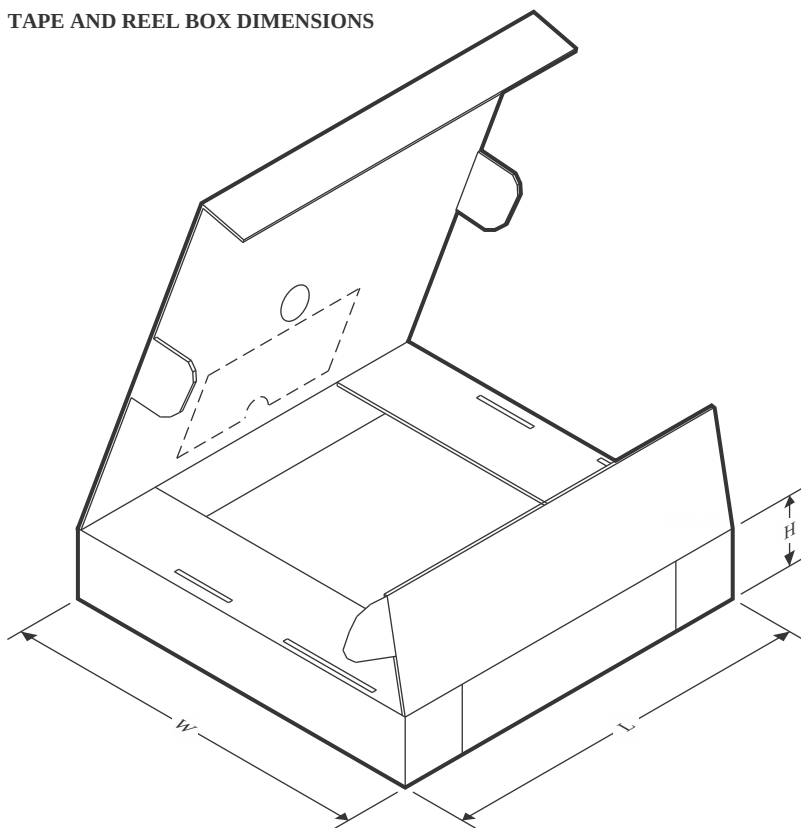
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 5962R1422802PYE   | HTSSOP       | DAP             | 32   | 250 | 178.0              | 24.4               | 8.8     | 11.8    | 1.8     | 12.0    | 24.0   | Q1            |
| TPS7H3302MDAPTSEP | HTSSOP       | DAP             | 32   | 250 | 330.0              | 24.4               | 8.8     | 11.8    | 1.8     | 12.0    | 24.0   | Q1            |
| TPS7H3302MDAPTSEP | HTSSOP       | DAP             | 32   | 250 | 178.0              | 24.4               | 8.8     | 11.8    | 1.8     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| 5962R1422802PYE   | HTSSOP       | DAP             | 32   | 250 | 223.0       | 191.0      | 55.0        |
| TPS7H3302MDAPTSEP | HTSSOP       | DAP             | 32   | 250 | 356.0       | 356.0      | 41.0        |
| TPS7H3302MDAPTSEP | HTSSOP       | DAP             | 32   | 250 | 223.0       | 191.0      | 55.0        |

## GENERIC PACKAGE VIEW

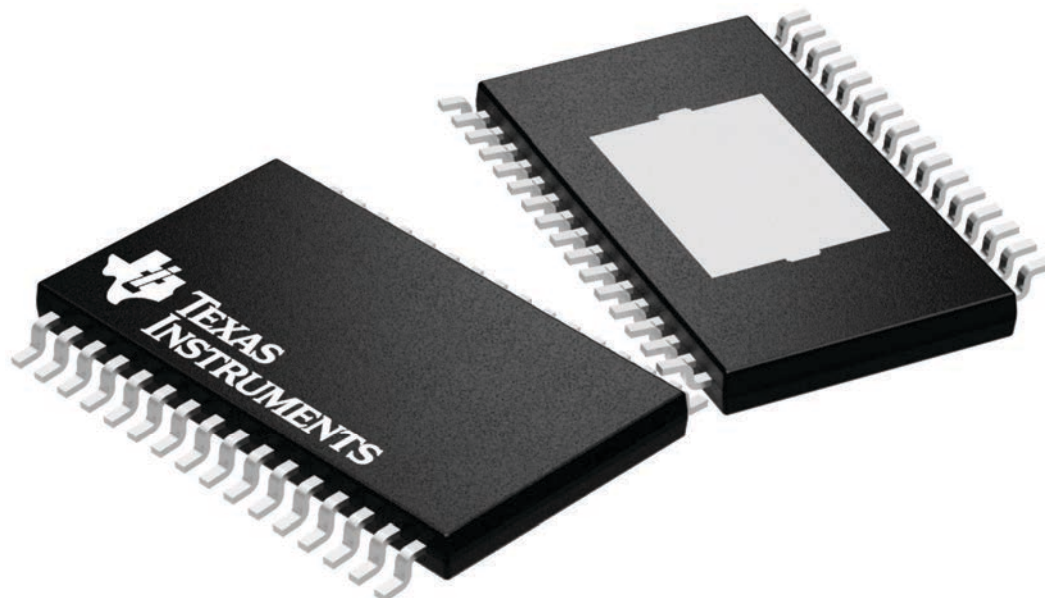
**DAP 32**

**PowerPAD™ TSSOP - 1.2 mm max height**

8.1 x 11, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225303/A



## PowerPAD™ TSSOP - 1.2 mm max height

## PLASTIC SMALL OUTLINE



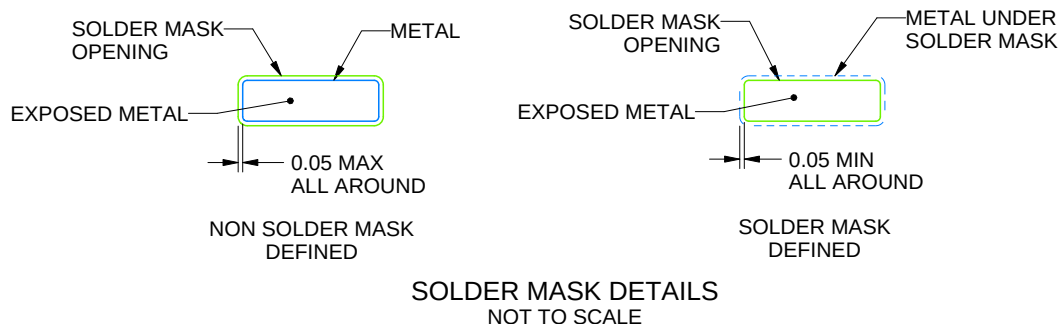
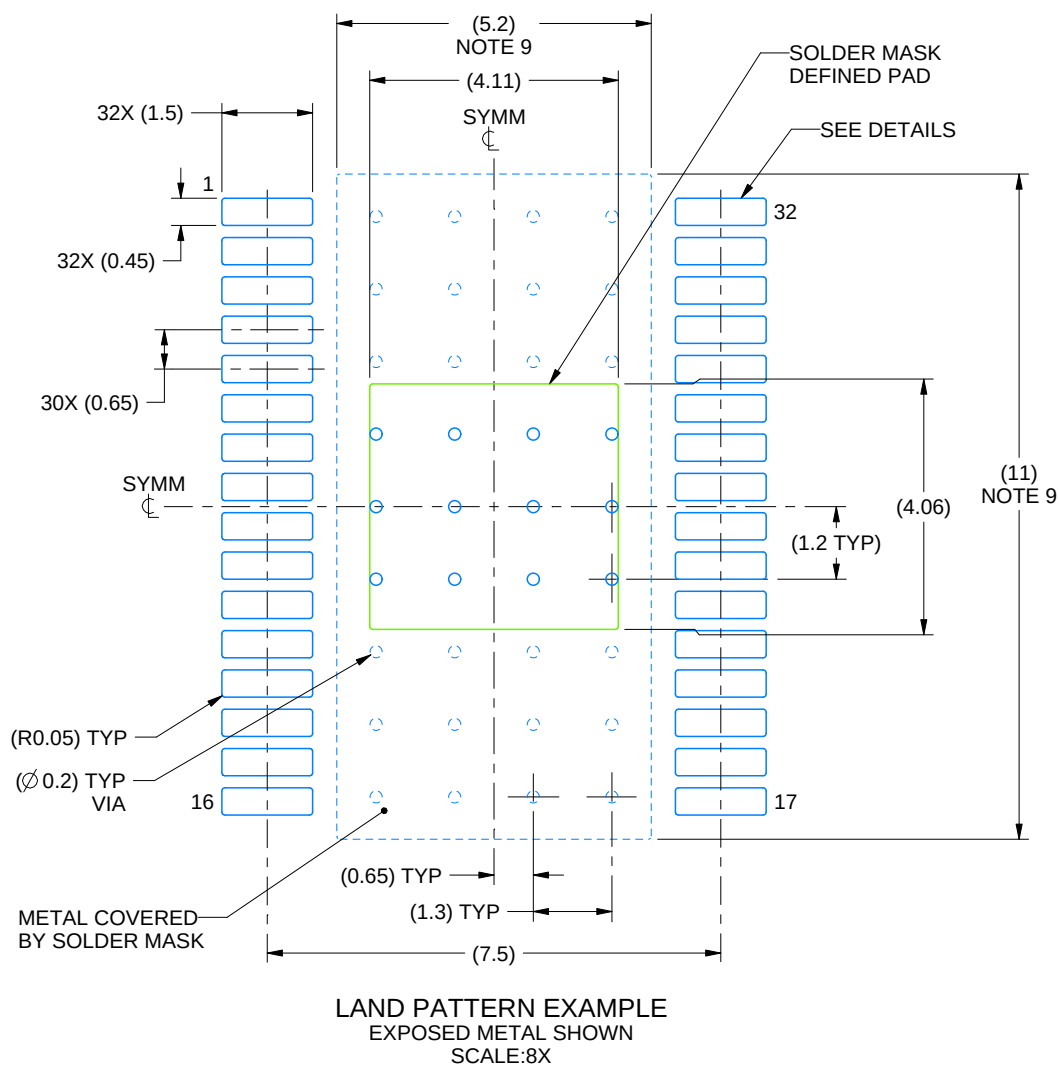
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.

**DAP0032F**

## PowerPAD™ TSSOP - 1.2 mm max height

## PLASTIC SMALL OUTLINE



4226056/A 07/2020

NOTES: (continued)

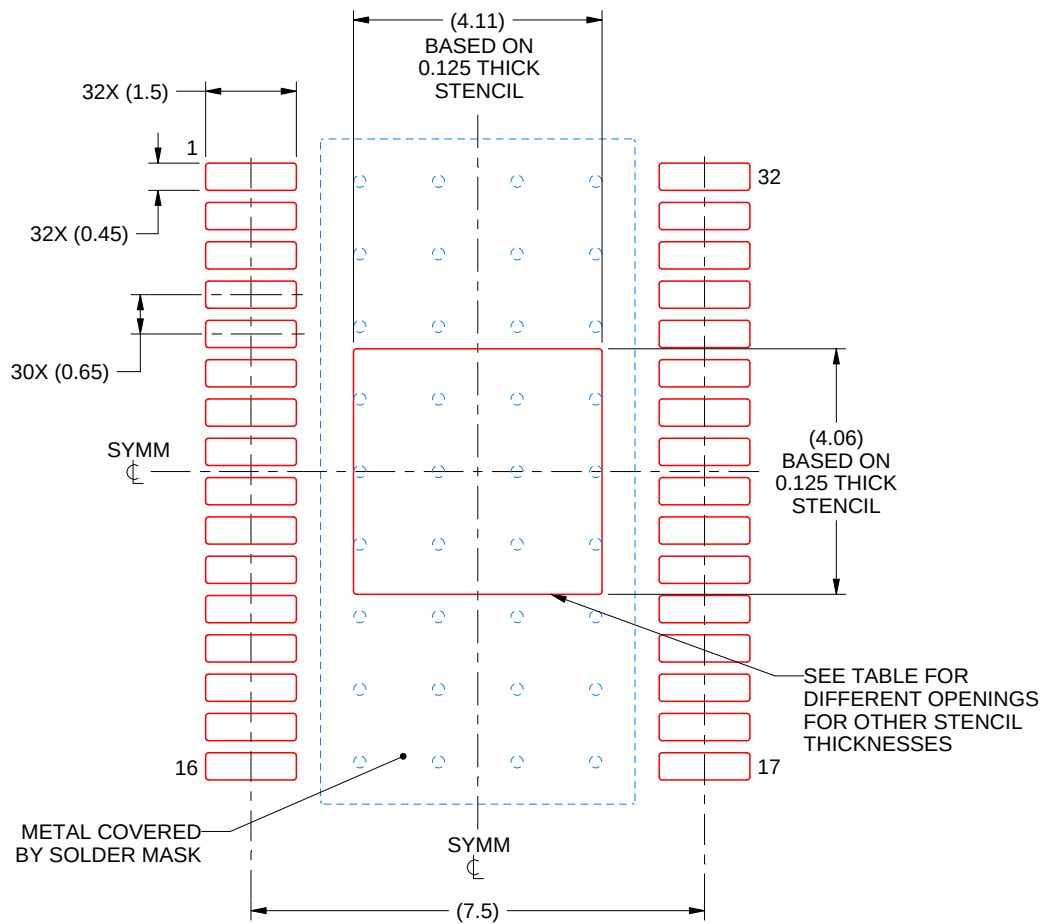
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DAP0032F

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



**SOLDER PASTE EXAMPLE**  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 4.60 X 4.54            |
| 0.125             | 4.11 X 4.06 (SHOWN)    |
| 0.15              | 3.75 X 3.71            |
| 0.175             | 3.47 X 3.43            |

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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