BQ25890H I²C Controlled Single Cell 5-A Fast Charger with MaxCharge™ Technology for High Input Voltage and Adjustable Voltage USB On-the-Go Boost Mode

1 Features

- High Efficiency 5-A, 1.5-MHz Switch Mode Buck Charge
  - 93% Charge Efficiency at 2 A and 91% Charge Efficiency at 3 A Charge Current
  - Optimize for High Voltage Input (9 V / 12 V)
  - Low Power PFM mode for Light Load Operations
- USB On-the-Go (OTG) with Adjustable Output from 4.5 V to 5.5 V
  - Selectable 500-KHz / 1.5-MHz Boost Converter with up-to 2.4 A Output
  - 93% Boost Efficiency at 5 V at 1 A Output
  - Accurate Hiccup Mode Overcurent Protection
  - Support down-to 2.5V Battery
  - Support PWM only or PFM/PWM control for Light Load Efficiency
- Single Input to Support USB Input and Adjustable High Voltage Adapters
  - Support 3.9-V to 14-V Input Voltage Range
  - Input Current Limit (100 mA to 3.25 A with 50-mA resolution) to Support USB2.0, USB3.0 standard and High Voltage Adapters
  - Maximum Power Tracking by Input Voltage Limit up-to 14V for Wide Range of Adapters
  - Auto Detect USB SDP, CDP, DCP, and Non-standard Adapters
- Input Current Optimizer (ICO) to Maximize Input Power without Overloading Adapters
- Resistance Compensation (IRCOMP) from Charger Output to Cell Terminal
- Highest Battery Discharge Efficiency with 11-mΩ Battery Discharge MOSFET up to 9 A
- Integrated ADC for System Monitor (Voltage, Temperature, Charge Current)
- Narrow VDC (NVDC) Power Path Management
  - Instant-on Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- BATFET Control to Support Ship Mode, Wake Up, and Full System Reset
- Flexible Autonomous and I²C Mode for Optimal System Performance
- High Integration includes all MOSFETs, Current Sensing and Loop Compensation
- 12-µA Low Battery Leakage Current to Support Ship Mode
- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±5% Charge Current Regulation
  - ±7.5% Input Current Regulation
- Safety
  - Battery Temperature Sensing for Charge and Boost Mode
  - Thermal Regulation and Thermal Shutdown

2 Applications

- Smart Phone
- Tablet PC
- Portable Internet Devices

3 Description

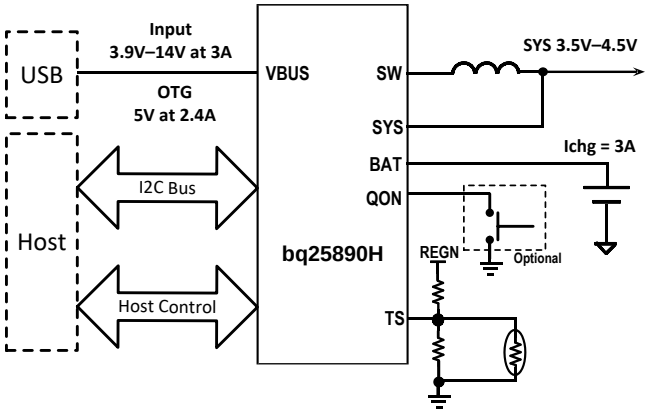
The bq25890H is a highly-integrated 5-A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. The devices support high input voltage fast charging. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq25890H	WQFN (24)	4.00mm x 4.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

Changes from Original (September 2016) to Revision A **Page**

- Added "SW (peak for 10 ns duration)" To the *Absolute Maximum Ratings*(1) ... 6
- Changed V_{SYS} TYP value From: V_{BAT} + 50 mV To: $I_{(SYS)}$ + 150 mV ... 7
- Changed the title of Figure 4 From: Charge Current Accuracy To: I^2C Setting ... 13
- Changed axis title of Figure 8 From: BAT Voltage (V) To: Input Current Limit (mA) ... 13
- Changed V_{VREF} to V_{REGN} in Equation 2 ... 24
- Changed V_{REF} to V_{REGN} in Figure 16 ... 25
- Added sentence to the Battery Monitor secton "In battery only mode, .." ... 25
- Changed the Description values of Table 26 From: mV To: mA ... 49
- Changed the Type values of Bit 7 in Table 28 From: R To: R/W ... 50
- Added V_{REF} system pullup voltage to Table 29 ... 51

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5 Description (continued)

The I^2C Serial interface with charging and system settings makes the device a truly flexible solution.

The bq25890H is a highly-integrated 5-A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. It features fast charging with high input voltage support for a wide range of smartphone, tablet and portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. It also integrates Input Current Optimizer (ICO) and Resistance Compensation (IRCOMP) to deliver maximum charging power to battery. The solution is highly integrated with input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. It also integrates the bootstrap diode for the high-side gate drive and battery monitor for simplified system design. The I^2C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port, and USB compliant adjustable high voltage adapter. To support fast charging using adjustable high voltage adapter, the SN25890H provides support for MaxCharge™ handshake using D+/D- pins and DSEL pin for USB switch control. In addition, the device include interface to support adjustable high voltage adapter using input current pulse protocol. To set the default input current limit, device uses the built-in USB interface, such as USB PHY device. The device is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. In addition, the Input Current Optimizer (ICO) supports the detection of maximum power point detection of the input source without overload. The device also meets USB On-the-Go (OTG) operation power rating specification by supplying 5 V (Adjustable 4.5 V - 5.5 V) on VBUS with current limit up to 2.4 A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This *Supplemental Mode* operation prevents overloading the input source.

The device initiates and completes a charging cycle without software control. It automatically detects the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle.

The charger provides various safety features for battery charging and system operations, including battery temperature negative thermistor monitoring, charging safety timer and overvoltage/overcurrent protections. The thermal regulation reduces charge current when the junction temperature exceeds 120°C (programmable). The STAT output reports the charging status and any fault conditions. The INT immediately notifies host when fault occurs.

The device also provides a 7-bit analog-to-digital converter (ADC) for monitoring charge current and input/battery/system (VBUS, BAT, SYS, TS) voltages. The QON pin provides BATFET enable/reset control to exit low power ship mode or full system reset function.

The device family is available in 24-pin, 4 x 4 mm^2 x 0.75 mm thin WQFN package.

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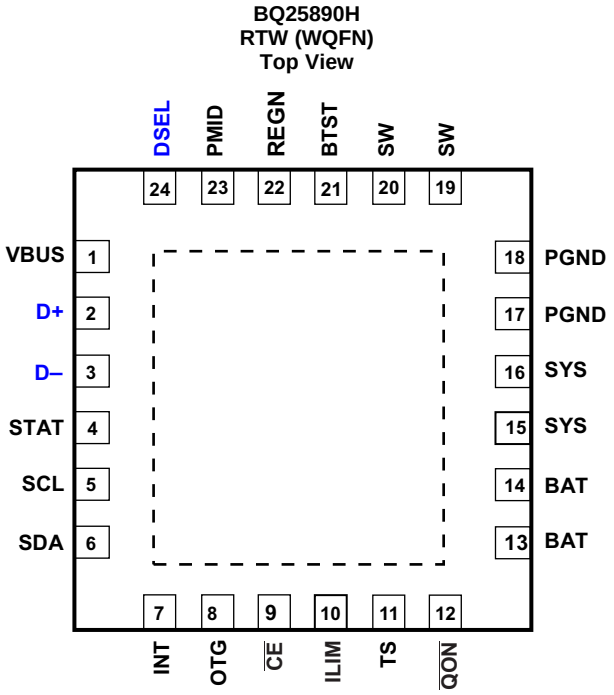
6 Pin Configuration and Functions



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	No.		
VBUS	1	P	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC.
D+	2	AIO	Positive line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter. The pin can be configured as output driver by DP_DAC register bits when input source is plugged-in or during OTG mode.
D–	3	AIO	Negative line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter. The pin can be configured as output driver by DM_DAC register bits when input source is plugged-in or during OTG mode.
STAT	4	DO	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10-kΩ resistor. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin blinks in 1 Hz. The STAT pin function can be disabled when STAT_DIS bit is set.
SCL	5	DI	I^2C Interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	6	DIO	I^2C Interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
INT	7	DO	Open-drain Interrupt Output. Connect the INT to a logic rail via 10-kΩ resistor. The INT pin sends active low, 256-µs pulse to host to report charger device status and fault.
OTG	8	DI	Active high enable pin during boost mode. The boost mode is activated when OTG_CONFIG =1 and OTG pin is high
$\overline{CE}$	9	DI	Active low Charge Enable pin. Battery charging is enabled when CHG_CONFIG = 1 and $\overline{CE}$ pin = Low. $\overline{CE}$ pin must be pulled High or Low.

(1) DI (Digital Input), DO (Digital Output), DIO (Digital Input/Output), AI (Analog Input), AO (Analog Output), AIO (Analog Input/Output)

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Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	No.		
ILIM	10	AI	Input current limit Input. ILIM pin sets the maximum input current and can be used to monitor input current ILIM pin sets the maximum input current limit by regulating the ILIM voltage at 0.8 V. A resistor is connected from ILIM pin to ground to set the maximum limit as $I_{INMAX} = K_{ILIM}/R_{ILIM}$. The actual input current limit is the lower limit set by ILIM pin (when EN_ILIM bit is high) or IIINLIM register bits. Input current limit of less than 500 mA is not support on ILIM pin. ILIM pin can also be used to monitor input current when the voltage is below 0.8V. The input current is proportional to the voltage on ILIM pin and can be calculated by $I_{IN} = (K_{ILIM} \times V_{ILIM}) / (R_{ILIM} \times 0.8)$ The ILIM pin function can be disabled when EN_ILIM bit is 0.
TS	11	AI	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor.
$\overline{QON}$	12	DI	BATFET enable/reset control input. When BATFET is in ship mode, a logic low of $t_{SHIPMODE}$ (typical 1sec) duration turns on BATFET to exit shipping mode. . When VBUS is not plugged-in, a logic low of t_{QON_RST} (typical 15sec) duration resets SYS (system power) by turning BATFET off for t_{BATFET_RST} (typical 0.3sec) and then re-enable BATFET to provide full system power reset. The pin contains an internal pull-up to maintain default high logic
BAT	13,14	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10uF closely to the BAT pin.
SYS	15,16	P	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage. Connect a 20uF closely to the SYS pin.
PGND	17,18	P	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
SW	19,20	P	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047µF bootstrap capacitor from SW to BTST.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the anode of the boost-strap diode. Connect the 0.047 µF bootstrap capacitor from SW to BTST.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost-strap diode. Connect a 4.7 µF (10 V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS pin.
PMID	23	DO	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Given the total input capacitance, put 1µF on VBUS to PGND, and the rest capacitance on PMID to PGND.
DSEL	24	DO	Active high D+/D- multiplexer selection control. Connect a 47-nF (6V rating) ceramic capacitor from DSEL to analog GND. The pin is normally low. During input source type detection, the pin drives high to indicate the device D+/D- detection is in progress and needs to take control of D+, D- signals. When detection is completed, the pin keeps high when DCP, MaxCharge or HVDCP is detected. The pin returns to low when other input source type is detected.
PowerPAD™		P	Exposed pad beneath the IC for heat dissipation. Always solder PowerPAD Pad to the board, and have vias on the PowerPAD plane star-connecting to PGND and ground plane for high-current power converter.

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7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	VALUE
Voltage range (with respect to GND)	VBUS (converter not switching)	–2	22	V
	PMID (converter not switching)	–0.3	22	V
	STAT	–0.3	20	V
	DSEL	–0.3	7	V
	BTST	–0.3	20	V
	SW	–2	16	V
	SW (peak for 10 ns duration)	–3	16	V
	BAT, SYS (converter not switching)	–0.3	6	V
	SDA, SCL, INT, OTG, REGN, TS, $\overline{CE}$, $\overline{QON}$	–0.3	7	V
	D+, D–	–0.3	7	V
	BTST TO SW	–0.3	7	V
	PGND to GND	–0.3	0.3	V
	ILIM	–0.3	5	V
Output sink current	INT, STAT		6	mA
	DSEL		2	mA
Junction temperature		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	3.9		14(1)	V
I_{IN}	Input current (VBUS)			3.25	A
I_{SYS}	Output current (SW)			5	A
V_{BAT}	Battery voltage			4.608	V
I_{BAT}	Fast charging current			5	A
	Discharging current with internal MOSFET			Up to 6 (continuos)	A
				9 (peak) (Up to 1 sec duration)	A
T_A	Operating free-air temperature range	–40		85	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BTST or SW pins. A tight layout minimizes switching noise.

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7.4 Thermal Information

THERMAL METRIC(1)		BQ25890H RTW (WQFN) 24-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.8	°C/W
$R_{\theta JC((op)}$	Junction-to-case (top) thermal resistance	27.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS) in buck mode	V_{BAT} = 4.2 V, $V_{(VBUS)} < V_{(UVLO)}$, leakage between BAT and VBUS			5	µA
		High-Z mode, no VBUS, BATFET disabled (REG09[5]=1), battery monitor disabled, T_J < 85°C		12	23	µA
		High-Z mode, no VBUS, BATFET enabled (REG09[5]=0), battery monitor disabled, T_J < 85°C		32	60	µA
$I_{(VBUS_HIZ)}$	Input supply current (VBUS) in buck mode when High-Z mode is enabled	$V_{(VBUS)}$= 5 V, High-Z mode, no battery, battery monitor disabled		15	35	µA
		$V_{(VBUS)}$= 12 V, High-Z mode, no battery, battery monitor disabled		25	50	µA
$I_{(VBUS)}$	Input supply current (V_{BUS}) in buck mode	$V_{BUS} > V_{(UVLO)}$, $V_{BUS} > V_{BAT}$, converter not switching		1.5	3	mA
		$V_{BUS} > V_{(UVLO)}$, $V_{BUS} > V_{BAT}$, converter switching, V_{BAT} = 3.2 V, I_{SYS} = 0A		3		mA
		$V_{BUS} > V_{(UVLO)}$, $V_{BUS} > V_{BAT}$, converter switching, V_{BAT} = 3.8 V, I_{SYS} = 0 A		3		mA
$I_{(BOOST)}$	Battery discharge current in boost mode	V_{BAT} = 4.2 V, boost mode, $I_{(VBUS)}$= 0 A, converter switching, PFM_OTG_DIS=0		3		mA
		V_{BAT} = 4.2 V, boost mode, $I_{(VBUS)}$= 0 A, converter switching, PFM_OTG_DIS=1		15		mA
VBUS/BAT POWER UP						
$V_{(VBUS_OP)}$	VBUS operating range		3.9		14	V
$V_{(VBUS_UVLOZ)}$	VBUS for active I^2C, no battery		3.6			V
$V_{(SLEEP)}$	Sleep mode falling threshold		25	65	120	mV
$V_{(SLEEPZ)}$	Sleep mode rising threshold		130	250	370	mV
$V_{(ACOV)}$	VBUS over-voltage rising threshold		14		14.6	V
	VBUS over-voltage falling threshold		13.5		14	V
$V_{BAT(UVLOZ)}$	Battery for active I2C, no VBUS		2.3			V
$V_{BAT(DPL)}$	Battery depletion falling threshold		2.15		2.5	V
$V_{BAT(DPLZ)}$	Battery depletion rising threshold		2.35		2.7	V
$V_{(VBUSMIN)}$	Bad adapter detection threshold			3.8		V
$I_{(BADSRC)}$	Bad adapter detection current source			30		mA
POWER-PATH MANAGEMENT						
V_{SYS}	Typical system regulation voltage	$I_{(SYS)}$ = 0 A, $V_{BAT} > V_{SYS(MIN)}$, BATFET Disabled (REG09[5]=1)		V_{BAT}+ 50 mV		V
		$I_{(SYS)}$ = 0 A, $V_{BAT} < V_{SYS(MIN)}$, BATFET Disabled (REG09[5]=1)		$V_{SYS(MIN)}$ + 150 mV		V
$V_{SYS(MIN)}$	Minimum DC system voltage output	$V_{BAT} < V_{SYS(MIN)}$, SYS_MIN = 3.5 V (REG03[3:1]=101), I_{SYS}= 0 A	3.50	3.65		V
$V_{SYS(MAX)}$	Maximum DC system voltage output	V_{BAT} = 4.35 V, SYS_MIN = 3.5V (REG03[3:1]=101), I_{SYS}= 0 A		4.40	4.42	V

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Electrical Characteristics (continued)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{ON(RBFET)}$	Top reverse blocking MOSFET(RBFET) on-resistance between VBUS and PMID	T_J = –40°C to +85°C		27	38	mΩ
		T_J = –40°C to +125°C		27	44	mΩ
$R_{ON(HSFET)}$	Top switching MOSFET (HSFET) on-resistance between PMID and SW	T_J = –40°C to +85°C		27	39	mΩ
		T_J = –40°C to +125°C		27	47	mΩ
$R_{ON(LSFET)}$	Bottom switching MOSFET (LSFET) on-resistance between SW and GND	T_J = –40°C to +85°C		16	24	mΩ
		T_J = –40°C to +125°C		16	28	mΩ
$V_{(FWD)}$	BATFET forward voltage in supplement mode	BAT discharge current 10 mA		30		mV
$V_{BAT(GD)}$	Battery good comparator rising threshold	V_{BAT} rising	3.4	3.55	3.7	V
$V_{BAT(GD_HYST)}$	Battery good comparator falling threshold	V_{BAT} falling		100		mV
BATTERY CHARGER						
$V_{BAT(REG_RANGE)}$	Typical charge voltage range		3.840		4.608	V
$V_{BAT(REG_STEP)}$	Typical charge voltage step			16		mV
$V_{BAT(REG)}$	Charge voltage resolution accuracy	V_{BAT} = 4.208 V (REG06[7:2]=010111) or V_{BAT} = 4.352 V (REG06[7:2]=100000) T_J = –40°C to +85°C	-0.5%		0.5%	
$I_{(CHG_REG_RANGE)}$	Typical fast charge current regulation range		0		5056	mA
$I_{(CHG_REG_STEP)}$	Typical fast charge current regulation step			64		mA
$I_{(CHG_REG_ACC)}$	Fast charge current regulation accuracy	V_{BAT} = 3.1 V or 3.8 V, I_{CHG} = 128 mA T_J = –40°C to +85°C	-20%		20%	
		V_{BAT}= 3.1 V or 3.8 V, I_{CHG} = 256 mA T_J = –40°C to +85°C	-10%		10%	
		V_{BAT}= 3.1 V or 3.8 V, I_{CHG}=1792 mA T_J = –40°C to +85°C	-5%		5%	
$V_{BAT(LOWV)}$	Battery LOWV falling threshold	Fast charge to precharge, BATLOWV (REG06[1]) = 1	2.6	2.8	2.9	V
	Battery LOWV rising threshold	Precharge to fast charge, BATLOWV (REG06[1])=1 (Typical 200-mV hysteresis)	2.8	3	3.1	V
$I_{(PRECHG_RANGE)}$	Precharge current range		64		1024	mA
$I_{(PRECHG_STEP)}$	Typical precharge current step			64		mA
$I_{(PRECHG_ACC)}$	Precharge current accuracy	V_{BAT}=2.6 V, I_{PRECHG} = 256 mA	–10%		+10%	
$I_{(TERM_RANGE)}$	Termination current range		64		1024	mA
$I_{(TERM_STEP)}$	Typical termination current step			64		mA
$I_{(TERM_ACC)}$	Termination current accuracy	I_{TERM} = 256 mA, I_{CHG}<= 1344 mA T_J = –20°C to +85°C	–12%		12%	
		I_{TERM} = 256 mA, I_{CHG}> 1344 mA T_J = –20°C to +85°C	–20%		20%	
$V_{(SHORT)}$	Battery short voltage	VBAT falling		2		V
$V_{(SHORT_HYST)}$	Battery short voltage hysteresis	VBAT rising		200		mV
$I_{(SHORT)}$	Battery short current	VBAT < 2.2 V		100		mA
$V_{(RECHG)}$	Recharge threshold below V_{BATREG}	V_{BAT} falling, VRECHG (REG06[0]=0) = 0		100		mV
		V_{BAT} falling, VRECHG (REG06[0]=0) = 1		200		mV
$I_{SYS(LOAD)}$	System discharge load current	V_{SYS} = 4.2 V	30			mA
$R_{ON(BATFET)}$	SYS-BAT MOSFET (BATFET) on-resistance	T_J = 25°C		11	13	mΩ
		T_J = –40°C to +125°C		11	19	mΩ
INPUT VOLTAGE / CURRENT REGULATION						
$V_{IN(DPM_RANGE)}$	Typical Input voltage regulation range		3.9		15.3	V
$V_{IN(DPM_STEP)}$	Typical Input voltage regulation step			100		mV
$V_{IN(DPM_ACC)}$	Input voltage regulation accuracy	VINDPM = 4.4 V, 9 V, T_J = –40°C to +105°C	3%		3%	
$I_{IN(DPM_RANGE)}$	Typical Input current regulation range		100		3250	mA
$I_{IN(DPM_STEP)}$	Typical Input current regulation step			50		mA
$I_{IN(DPM100_ACC)}$	Input current 100-mA regulation accuracy V_{BAT} = 5 V, current pulled from SW	IINLIM (REG00[5:0]) =100 mA	85	90	100	mA
$I_{IN(DPM_ACC)}$	Input current regulation accuracy V_{BAT} = 5 V, current pulled from SW	USB150, IINLIM (REG00[5:0]) = 150 mA	125	135	150	mA
		USB500, IINLIM (REG00[5:0]) = 500 mA	440	470	500	mA
		USB900, IINLIM (REG00[5:0]) = 900 mA	750	825	900	mA
		Adapter 1.5 A, IINLIM (REG00[5:0]) = 1500 mA	1300	1400	1500	mA

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Electrical Characteristics (continued)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IN(START)}$	Input current regulation during system start up	V_{SYS} = 2.2 V, IINLIM (REG00[5:0])> = 200 mA			200	mA
K_{ILIM}	$I_{INMAX} = K_{ILIM}/R_{ILIM}$	Input current regulation by ILIM pin = 1.5 A	315	350	385	A x Ω
D+/D- DETECTION						
$V_{(0P0_VSRC)}$	D+/D– voltage source (0 V)	I(DP) < 1 mA; DP_DAC=001 or DM_DAC=001	-0.15	0	0.15	V
$V_{(0P6_VSRC)}$	D+/D– voltage source (0.6 V)	I(DP) < 1 mA; DP_DAC=010 or I(DM) < 1 m; ADM_DAC=010	0.5	0.6	0.7	V
$V_{(1P2_VSRC)}$	D+/D– voltage source (1.2 V)	I(DP) < 1 mA; DP_DAC=011 or I(DM) < 1 m; DM_DAC=011	1.075	1.2	1.325	V
$V_{(2P0_VSRC)}$	D+/D– voltage source (2.0 V)	I(DP) < 1 mA; DP_DAC=100 or I(DM) < 1 m; DM_DAC=100	1.875	2.0	2.125	V
$V_{(2P7_VSRC)}$	D+/D– voltage source (2.7 V)	I(DP) < 1 mA; DP_DAC=101 or I(DM) < 1 m; DM_DAC=101	2.575	2.7	2.825	V
$V_{(3P3_VSRC)}$	D+/D– voltage source (3.3 V)	I(DP) < 1 mA; DP_DAC=110 or I(DM) < 1 m; DM_DAC=110	3.15	3.3	3.45	V
$V_{(3p45_VSRC)}$	D+/D– voltage source (3.45 V)		3.3	3.45	3.6	V
$I_{(10UA_ISRC)}$	D+ connection check current source		7	10	14	µA
$I_{(100UA_ISINK)}$	D+/D– current sink (100 µA)		50	100	150	µA
$I_{(DPDM_LKG)}$	D+/D– leakage current	D–, switch open	–1		1	µA
		D+, switch open	–1		1	µA
$I_{(1P6MA_ISINK)}$	D+/D– current sink (1.6 mA)		1.45	1.60	1.75	µA
$V_{(0P4_VTH)}$	D+/D– low comparator threshold		250		400	mV
$V_{(0P8_VTH)}$	D+ low comparator threshold				0.8	V
$V_{(2P7_VTH)}$	D+/D– comparator threshold for non-standard adapter detection (divider 1, 3, or 4)		2.55		2.85	V
$V_{(2P0_VTH)}$	D+/D– comparator threshold for non-standard adapter detection (divider 1, 3)		1.85		2.15	V
$V_{(1P2_VTH)}$	D+/D– comparator threshold for non-standard adapter detection (divider 2)		1.05		1.35	V
$R_{(D-_DWN)}$	D– pulldown for connection check		14.25		24.8	kΩ
BAT OVER-VOLTAGE/CURRENT PROTECTION						
$V_{BAT(OVP)}$	Battery over-voltage threshold	V_{BAT} rising, as percentage of $V_{BAT(REG)}$		104%		
$V_{BAT(OVP_HYST)}$	Battery over-voltage hysteresis	V_{BAT} falling, as percentage of $V_{BAT(REG)}$		2%		
$I_{BAT(FET_OCP)}$	System over-current threshold		9			A
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	REG08[1:0] = 11		120		°C
T_{SHUT}	Thermal shutdown rising temperature	Temperature rising		160		°C
$T_{SHUT(HYS)}$	Thermal shutdown hysteresis	Temperature falling		30		°C
JEITA THERMISTOR COMPARATOR (BUCK MODE)						
$V_{(T1)}$	T1 (0°C) threshold, charge suspended T1 below this temperature.	As percentage to $V_{(REGN)}$	72.75%	73.25%	73.75%	
$V_{(T1_HYS)}$	Charge back to ICHG/2 (REG04[6:0]) and VREG (REG06[7:2]) above this temperature.	As percentage to $V_{(REGN)}$		1.4%		
$V_{(T2)}$	T2 (10°C) threshold, charge back to ICHG/2 (REG04[6:0]) and VREG (REG06[7:2]) below this temperature.	As percentage to $V_{(REGN)}$	67.75%	68.25%	68.75%	
$V_{(T2_HYS)}$	Charge back to ICHG (REG04[6:0]) and VREG (REG06[7:2]) above this temperature.	As percentage to $V_{(REGN)}$		1.4%		
$V_{(T3)}$	T3 (45°C) threshold, charge back to ICHG (REG04[6:0]) and VREG-200 mV (REG06[7:2]) above this temperature.	As percentage to $V_{(REGN)}$	44.25v	44.75%	45.25%	
$V_{(T3_HYS)}$	Charge back to ICHG (REG04[6:0]) and VREG (REG06[7:2]) below this temperature.	As percentage to $V_{(REGN)}$		1%		
$V_{(T5)}$	T5 (60°C) threshold, charge suspended above this temperature.	As percentage to $V_{(REGN)}$	33.875%	34.375%	34.875%	
$V_{(T5_HYS)}$	Charge back to ICHG (REG04[6:0]) and VREG-200 mV (REG06[7:2]) below this temperature.	As percentage to $V_{(REGN)}$		1.25%		
COLD/HOT THERMISTOR COMPARATOR (BOOST MODE)						

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Electrical Characteristics (continued)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BCOLD1)}$	Cold temperature threshold 1, TS pin voltage rising threshold	As percentage to V_{REGN} REG01[5] = 1 (Approximately –20°C w/ 103AT)	79.5%	80%	80.5%	
$V_{(BCOLD1_HYS)}$	Cold temperature threshold 1, TS pin voltage falling threshold	As percentage to V_{REGN} REG01[5] = 1		1%		
$V_{(BHOT2)}$	Hot temperature threshold 2, TS pin voltage falling threshold	As percentage to V_{REGN} REG01[7:6] = 10 (Approx. 65°C w/ 103AT)	30.75%	31.25%	31.75%	
$V_{(BHOT2_HYS)}$	Hot temperature threshold 2, TS pin voltage rising threshold	As percentage to V_{REGN} REG01[7:6] =10		3%		
PWM						
F_{SW}	PWM switching frequency, and digital clock	Oscillator frequency	1.32		1.68	MHz
D_{MAX}	Maximum PWM duty cycle			97%		
BOOST MODE OPERATION						
$V_{(OTG_REG_RANGE)}$	Typical boost mode regulation voltage range		4.55		5.55	V
$V_{(OTG_REG_STEP)}$	Typical boost mode regulation voltage step			64		mV
$V_{(OTG_REG_ACC)}$	Boost mode regulation voltage accuracy	I(VBUS) = 0 A, BOOSTV=4.998V (REG0A[7:4] = 0111)	–3%		3%	
$V_{(OTG_BAT1)}$	Minimum battery voltage to exit boost mode	BAT falling, MIN_VBAT_SEL=0	2.7		2.9	V
$V_{(OTG_BAT2)}$	Minimum battery voltage to exit boost mode	BAT falling, MIN_VBAT_SEL=1	2.4		2.6	V
$V_{(OTG_BAT_EN)}$	Minimum battery voltage to enter boost mode	BAT rising, MIN_VBAT_SEL=0	2.9		3.1	V
		BAT rising, MIN_VBAT_SEL=1	2.7		2.9	V
$I_{(OTG)}$	Typical boost mode output current range		0.5		2.45	A
$I_{(OTG_OCP_ACC)}$	Boost mode RBFET over-current protection accuracy	BOOST_LIM =1.2 A (REG0A[2:0]=010)	1.2		1.65	A
$V_{(OTG_OVP)}$	Boost mode over-voltage threshold	Rising threshold	5.8	6		V

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Electrical Characteristics (continued)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REGN LDO						
$V_{(REGN)}$	REGN LDO output voltage	$V_{(VBUS)}$ = 9 V, $I_{(REGN)}$ = 40 mA	5.6	6	6.4	V
		$V_{(VBUS)}$ = 5 V, $I_{(REGN)}$ = 20 mA	4.7	4.8		V
$I_{(REGN)}$	REGN LDO current limit	$V_{(VBUS)}$ = 9 V, $V_{(REGN)}$ = 3.8 V	50			mA
ANALOG-TO-DIGITAL CONVERTER (ADC)						
RES	Resolution	Rising threshold		7		bits
$V_{BAT(RANGE)}$	Typical battery voltage range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ or OTG mode is enabled	2.304		4.848	V
		$V_{(VBUS)} < V_{BAT} + V_{(SLEEP)}$ and OTG mode is disabled	V_{SYS_MIN}		4.848	V
$V_{(BAT_RES)}$	Typical battery voltage resolution			20		mV
$V_{(SYS_RANGE)}$	Typical system voltage range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ or OTG mode is enabled	2.304		4.848	V
		$V_{(VBUS)} < V_{BAT} + V_{(SLEEP)}$ and OTG mode is disabled	V_{SYS_MIN}		4.848	V
$V_{(SYS_RES)}$	Typical system voltage resolution			20		mV
$V_{(VBUS_RANGE)}$	Typical V_{VBUS} voltage range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ or OTG mode is enabled	2.6		15.3	V
$V_{(VBUS_RES)}$	Typical V_{VBUS} voltage resolution			100		mV
$I_{BAT(RANGE)}$	Typical battery charge current range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ and $V_{BAT} > V_{BAT(SHORT)}$	0		6.4	A
$I_{BAT(RES)}$	Typical battery charge current resolution			50		mA
$V_{(TS_RANGE)}$	Typical TS voltage range		21%		80%	
$V_{(TS_RES)}$	Typical TS voltage resolution			0.47%		
LOGIC I/O PIN (OTG, $\overline{CE}$, $\overline{QON}$)						
V_{IH}	Input high threshold level		1.3			
V_{IL}	Input low threshold level				0.4	V
$I_{IN(BIAS)}$	High Level Leakage Current	Pull-up rail 1.8 V			1	µA
$V_{(QON)}$	Internal /QON pull-up	Battery only mode		BAT		V
		$V_{(VBUS)}$ = 9 V		5.8		V
		$V_{(VBUS)}$ = 5 V		4.3		V
$R_{(QON)}$	Internal /QON pull-up resistance			200		kΩ
LOGIC I/O PIN (DSEL)						
V_{OL}	Output low threshold level	I_{OL} = 2 mA, C_{DSEL}= 47 nF			0.4	V
V_{OH}	Output high threshold level	I_{OH} = 5 mA, C_{DSEL}= 47 nF, non-switching, $I_{(REGN)}$ = 30 mA	4.5			V
LOGIC I/O PIN (INT, STAT)						
V_{OL}	Output low threshold level	Sink current = 5 mA, sink current			0.4	V
I_{OUT_BIAS}	High level leakage current	Pull-up rail 1.8 V			1	µA
I^2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level, SCL and SDA	Pull-up rail 1.8 V	1.3			
V_{IL}	Input low threshold level	Pull-up rail 1.8 V			0.4	V
V_{OL}	Output low threshold level	Sink current = 5 mA, sink current			0.4	V
I_{BIAS}	High level leakage current	Pull-up rail 1.8 V			1	µA

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7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
VBUS/BAT POWER UP						
t_{BADSRC}	Bad Adapter detection duration			30		msec
BAT OVER-VOLTAGE PROTECTION						
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			1		µs
BATTERY CHARGER						
t_{RECHG}	Recharge deglitch time			20		ms
CURRENT PULSE CONTROL						
t_{PUMPX_STOP}	Current pulse control stop pulse		430		570	ms
t_{PUMPX_ON1}	Current pulse control long on pulse		240		360	ms
t_{PUMPX_ON2}	Current pulse control short on pulse		70		130	ms
t_{PUMPX_OFF}	Current pulse control off pulse		70		130	ms
t_{PUMPX_DLY}	Current pulse control stop start delay		80		225	ms
BATTERY MONITOR						
t_{CONV}	Conversion time	CONV_RATE(REG02[6]) = 0		8	1000	ms
$\overline{QON}$ AND SHIPMODE TIMING						
$t_{SHIPMODE}$	$\overline{QON}$ low time to turn on BATFET and exit ship mode	T_J = –10°C to +60°C	0.8		1.3	s
t_{QON_RST}	$\overline{QON}$ low time to enable full system reset	T_J = –10°C to +60°C	15.5		23	s
t_{BATFET_RST}	BATFET off time during full system reset	T_J = –10°C to +60°C	250		400	ms
t_{SM_DLY}	Enter ship mode delay	T_J = –10°C to +60°C	10		15	s
I2C INTERFACE						
f_{SCL}	SCL clock frequency				400	kHz
DIGITAL CLOCK and WATCHDOG TIMER						
f_{LPDIG}	Digital low power clock	REGN LDO disabled	18	30	45	kHz
f_{DIG}	Digital clock	REGN LDO enabled	1320	1500	1680	kHz
t_{WDT}	Watchdog reset time	WATCHDOG (REG07[5:4])=11, REGN LDO disabled	100	160		s
		WATCHDOG (REG07[5:4])=11, REGN LDO enabled	136	160		s

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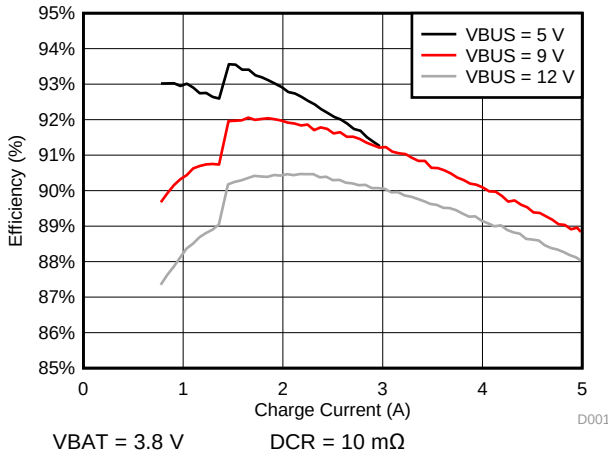
7.7 Typical Characteristics



VBAT = 3.8 V DCR = 10 mΩ

Figure 1. Charge Efficiency vs Charge Current

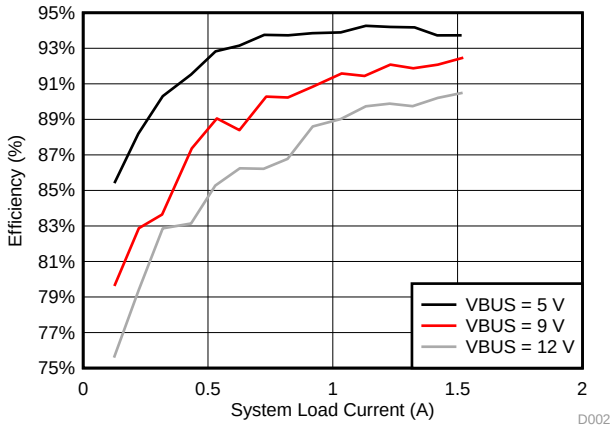


Figure 2. System Light Load Efficiency vs System Light Load Current

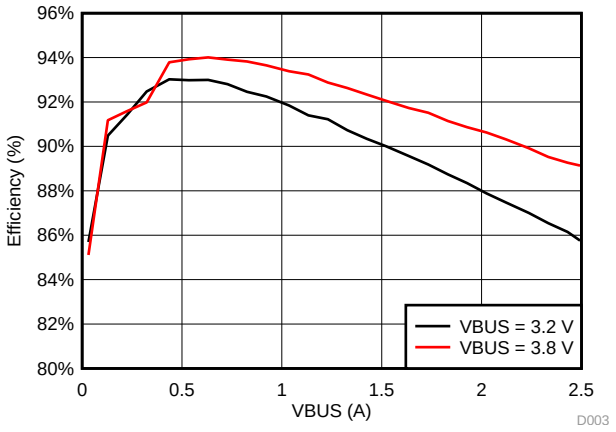
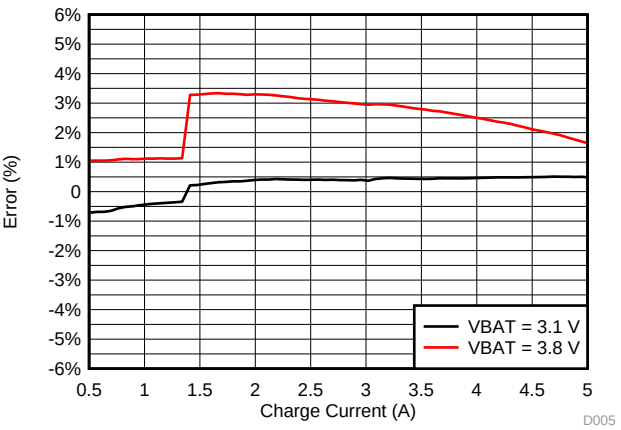
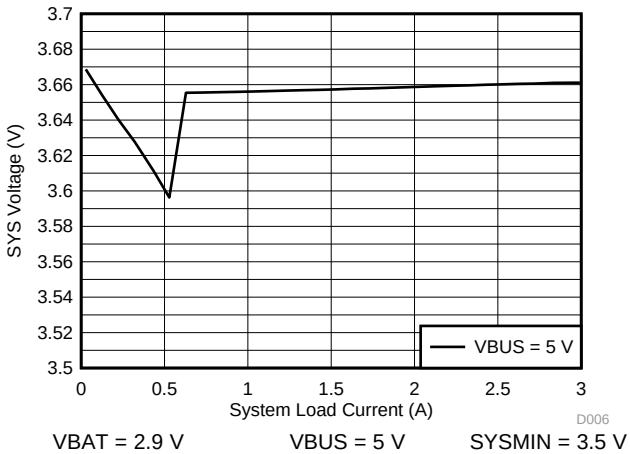


Figure 3. Boost Mode Efficiency vs VBUS Load Current



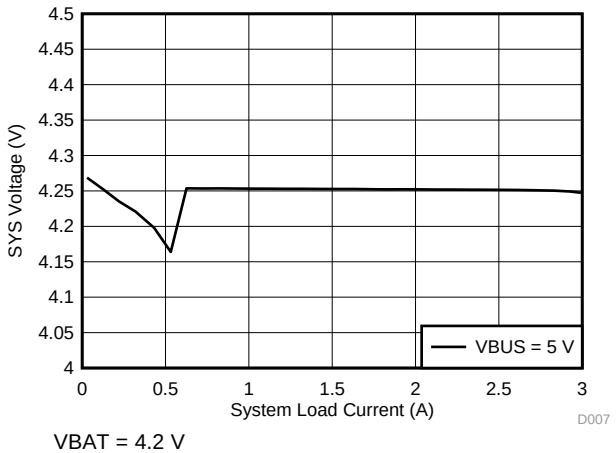
VBUS = 9 V

Figure 4. Charge Current Accuracy vs Charge Current I²C Setting



VBAT = 2.9 V VBUS = 5 V SYSMIN = 3.5 V

Figure 5. SYS Voltage Regulation vs System Load Current



VBAT = 4.2 V

Figure 6. SYS Voltage Regulation vs System Load Current

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Typical Characteristics (continued)

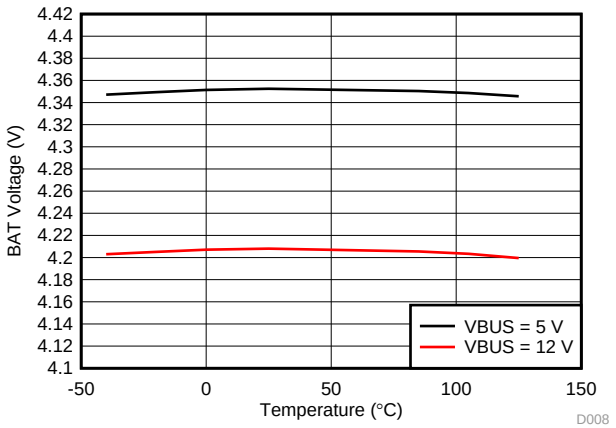

Figure 7. BAT Voltage vs Temperature

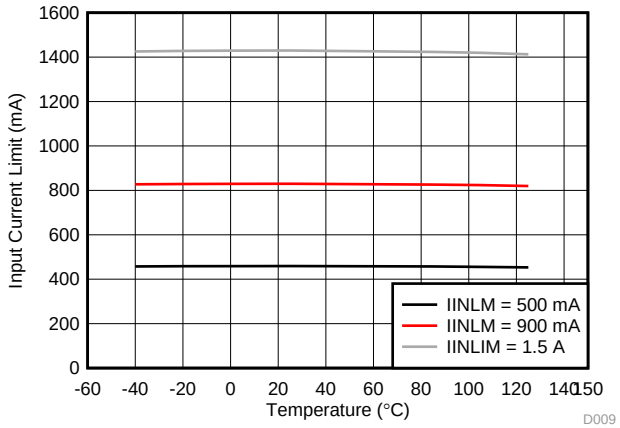

Figure 8. Input Current Limit vs Temperature

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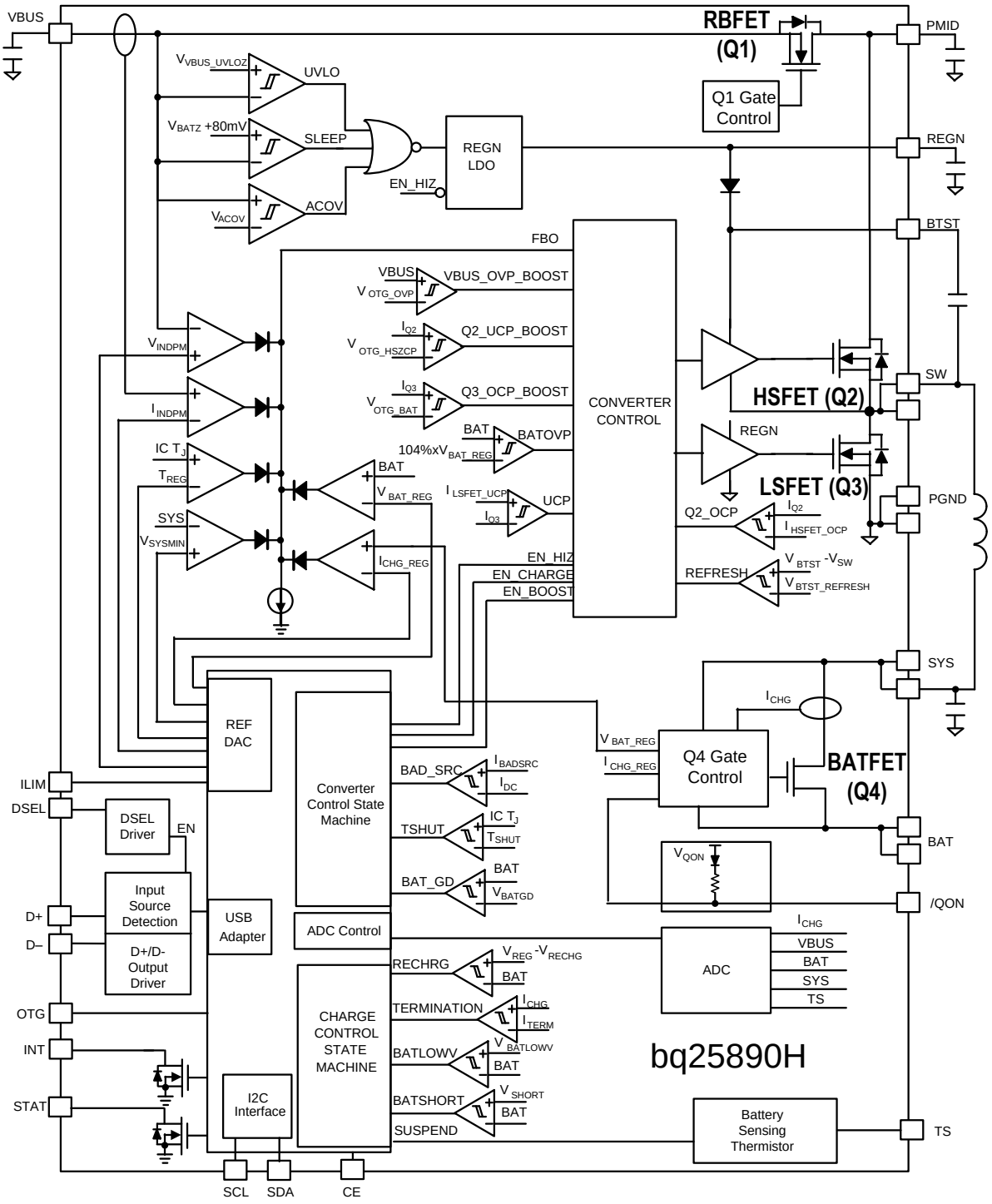
8 Detailed Description

The device is a highly integrated 5-A siwtch-mode battery charger for single cell Li-Ion and Li-polymer battery. It is highly integrated with the input reverse-blocking FET (RBFET, Q1), high-side siwtching FET (HSFET, Q2) , low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4). The device also integrates the boostrap diode for the high-side gate drive.

8.1 Functional Block Diagram



8.2 Feature Description

8.2.1 Device Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage of VBUS and BAT. When VBUS rises above V_{VBUS_UVLOZ} or BAT rises above V_{BAT_UVLOZ} , the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

8.2.2 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold (V_{BAT_DPLZ}), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low $R_{DS(ON)}$ of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharge current through BATFET (*Supplement Mode*). When the system is overloaded or shorted (IBAT > I_{BATFET_OCP}), the device turns off BATFET immediately and set BATFET_DIS bit to indicate BATFET is disabled until the input source plugs in again or one of the methods describe in *BATFET Enable (Exit Shipping Mode)* is applied to re-enable BATFET.

8.2.3 Device Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started when AUTO_DPDM_EN bit is set. The power up sequence from input source is as listed:

1. Power Up REGN LDO
2. Poor Source Qualification
3. *Input Source Type Detection* based on D+/D- to set default Input Current Limit (IINLIM) register and input source type
4. Input Voltage Limit Threshold Setting (VINDPM threshold)
5. Converter Power-up

8.2.3.1 Power Up REGN Regulation (LDO)

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid.

1. VBUS above V_{VBUS_UVLOZ}
2. VBUS above V_{BAT} + V_{SLEEPZ} in buck mode or VBUS below V_{BAT} + V_{SLEEP} in boost mode
3. After 220 ms delay is completed

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than I_{VBUS_HIZ} from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

8.2.3.2 Poor Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to start the buck converter.

1. VBUS voltage below V_{ACOV}
2. VBUS voltage above $V_{VBUSMIN}$ when pulling I_{BADSRC} (typical 30mA)

Once the input source passes all the conditions above, the status register bit VBUS_GD is set high and the INT pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

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Feature Description (continued)

8.2.3.3 Input Source Type Detection

After the VBUS_GD bit is set and REGN LDO is powered, the charger device runs *Input Source Type Detection* when AUTO_DPDM_EN bit is set.

The bq25890H follows the USB Battery Charging Specification 1.2 (BC1.2) and to detect input source (SDP/CDP/DCP) and non-standard adapter through USB D+/D- lines. In addition, when USB DCP is detected, it initiates adjustable high voltage adapter handshake on D+/D-. The device supports MaxCharge™ handshake when MAXC_EN or HVDCP_EN is set.

After input source type detection, an INT pulse is asserted to the host. In addition, the following registers and pin are changed:

1. Input Current Limit (IINLIM) register is changed to set current limit
2. PG_STAT bit is set

The host can over-write IINLIM register to change the input current limit if needed. The charger input current is always limited by the lower of IINLIM register or ILIM pin at all-time regardless of Input Current Optimizer (ICO) is enable or disabled.

When AUTO_DPDM_EN is disabled, the *Input Source Type Detection* is bypassed. The Input Current Limit (IINLIM) register, VBUS_STAT, and SPD_STAT bits are unchanged from previous values.

8.2.3.3.1 D+/D– Detection Sets Input Current Limit

The bq25890H contains a D+/D– based input source detection to set the input current limit automatically. The D+/D- detection includes standard USB BC1.2, non-standard adapter, and adjustable high voltage adapter detections. When input source is plugged-in, the device starts standard USB BC1.2 detections. The USB BC1.2 is capable to identify Standard Downstream Port (SDP), Charging Downstream Port (CDP), and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer of 500ms is expired, the non-standard adapter detection is applied to set the input current limit.

When DCP is detected, the device initates adjustable high voltage adapter handshake including MaxCharge™, etc. The handshake connects combinations of voltage source(s) and/or current sink on D+/D- to signal input source to raise output voltage from 5 V to 9 V / 12 V. The adjustable high voltage adapter handshake can be disabled by clearing MAXC_EN and/or HVDCP_EN bits .

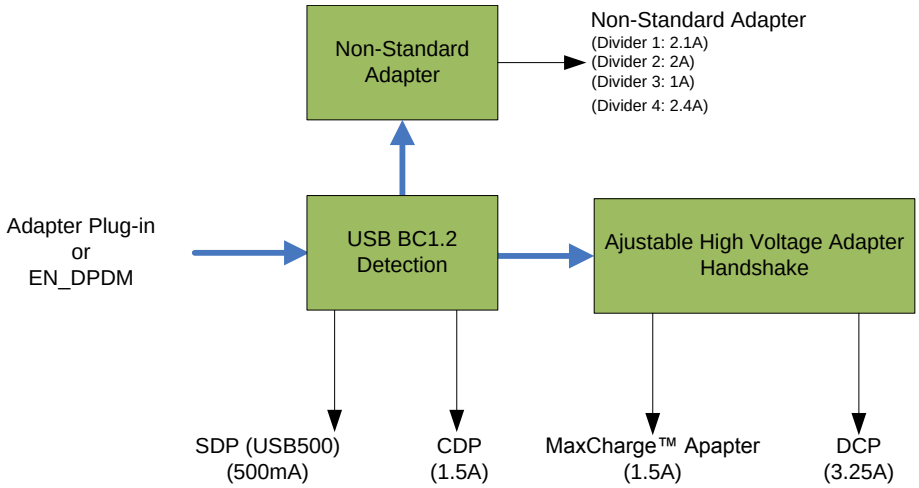

Figure 9. USB D+/D- Detection

Table 1. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D- THRESHOLD	INPUT CURRENT LIMIT
Divider 1	V_{D+} within V_{2P7_VTH}	V_{D-} within V_{2P0_VTH}	2.1A
Divider 2	V_{D+} within V_{1P2_VTH}	V_{D-} within V_{1P2_VTH}	2A
Divider 3	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P7_VTH}	1A
Divider 4	V_{D+} within V_{2P7_VTH}	V_{D-} within V_{2P7_VTH}	2.4A

Table 2. Adjustable High Voltage Adapter D+/D- Output Configurations

ADJUSTABLE HIGH VOLTAGE HANDSHAKE	D+	D-	OUTPUT
MaxCharge (12V)	I_{1P6MA_ISINK}	V_{3p45_VSRC}	12 V
MaxCharge (9V)	V_{3p45_VSRC}	I_{1P6MA_ISINK}	9 V

After the *Input Source Type Detection* is done, an INT pulse is asserted to the host. In addition, the following registers including Input Current Limit register (IINLIM), VBUS_STAT, and SDP_STAT are updated as below:

Table 3. bq25890H Result

D+/D- DETECTION	INPUT CURRENT LIMIT (IINLIM)	SDP_STAT	VBUS_STAT
USB SDP (USB500)	500 mA	1	001
USB CDP	1.5 A	1	010
USB DCP	3.25 A	1	011
Divider 3	1 A	1	110
Divider 1	2.1 A	1	110
Divider 4	2.4 A	1	110
Divider 2	2 A	1	110
MaxCharge	1.5 A	1	100
Unknown Adapter	500 mA	1	101

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8.2.3.3.2 Force Input Current Limit Detection

In host mode, the host can force the device to run by setting FORCE_DPDM bit. After the detection is completed, FORCE_DPDM bit returns to 0 by itself and Input Result is updated.

8.2.3.4 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device supports wide range of input voltage limit (3.9 V – 14 V) for high voltage charging and provides two methods to set Input Voltage Limit (VINDPM) threshold to facilitate autonomous detection.

1. Absolute VINDPM (FORCE_VINDPM=1)

   By setting FORCE_VINDPM bit to 1, the VINDPM threshold setting algorithm is disabled. Register VINDPM is writable and allows host to set the absolute threshold of VINDPM function.
2. Relative VINDPM based on VINDPM_OS registers (FORCE_VINDPM=0) (Default)

When FORCE_VINDPM bit is 0 (default), the VINDPM threshold setting algorithm is enabled. The VINDPM register is read only and the charger controls the register by using VINDPM Threshold setting algorithm. The algorithm allows a wide range of adapter (V_{VBUS_OP}) to be used with flexible VINDPM threshold.

After Input Voltage Limit Threshold is set, an INT pulse is generated to signal to the host.

8.2.3.5 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current limit is forced to the lower of 200 mA or IINLIM register setting. After the system rises above 2.2 V, the device limits input current to the lower value of ILIM pin and IILIM register (ICO_EN = 0) or IDPM_LIM register (ICO_EN = 1).

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the PMID voltage to cancel out any loop gain variation due to a change in input voltage.

In order to improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

8.2.4 Input Current Optimizer (ICO)

The device provides innovative Input Current Optimizer (ICO) to identify maximum power point without overload the input source. The algorithm automatically identify maximum input current limit of power source without entering VINDPM to avoid input source overload.

This feature is enabled by default (ICO_EN=1) and can be disabled by setting ICO_EN bit to 0. After DCP or MaxCharge type input source is detected based on the procedures previously described (*Input Source Type Detection*). The algorithm runs automatically when ICO_EN bit is set. The algorithm can also be forced to execute by setting FORCE_ICO bit regardless of input source type detected.

The actual input current limit used by the *Dynamic Power Management* is reported in IDPM_LIM register while Input Current Optimizer is enabled (ICO_EN = 1) or set by IINLIM register when the algorithm is disabled (ICO_EN = 0). In addition, the current limit is clamped by ILIM pin unless EN_ILIM bit is 0 to disable ILIM pin function.

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8.2.5 Boost Mode Operation from Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 500 mA (BOOST_LIM bits = 000) output requirement. The maximum output current is up to 2.4 A. The boost operation can be enabled if the conditions are valid:

1. BAT above BAT_{LOWV}
2. VBUS less than BAT+V_{SLEEP} (in sleep mode)
3. Boost mode operation is enabled (OTG pin HIGH and OTG_CONFIG bit =1)
4. Voltage at TS (thermistor) pin is within range configured by Boost Mode Temperature Monitor as configured by BHOT and BCOLD bits
5. After 30 ms delay from boost mode enable

In boost mode, the device employs a 500 KHz or 1.5 MHz (selectable using BOOST_FREQ bit) step-up switching regulator based on system requirements. To avoid frequency change during boost mode operations, write to boost frequency configuration bit (BOOST_FREQ) is ignored when OTG_CONFIG is set.

During boost mode, the status register VBUS_STAT bits is set to 111, the VBUS output is 5V by default (selectable via BOOSTV register bits) and the output current can reach up to 2.4 A, selected via I^2C (BOOST_LIM bits). The boost output is maintained when BAT is above V_{OTG_BAT} threshold

8.2.6 Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car battery. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

8.2.6.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS_MIN bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5 V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of BATFET. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

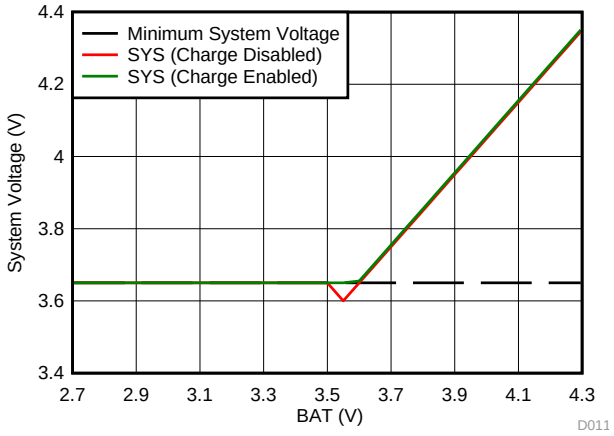

Figure 10. V(SYS) vs V(BAT)

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8.2.6.2 Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IINLIM or IDPM_LIM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the *Supplement Mode* where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VDPM_STAT (VINDPM) and/or IDPM_STAT (IINDPM) is/are set high. Figure 11 shows the DPM response with 9V/1.2A adapter, 3.2-V battery, 2.8-A charge current and 3.4-V minimum system voltage setting.

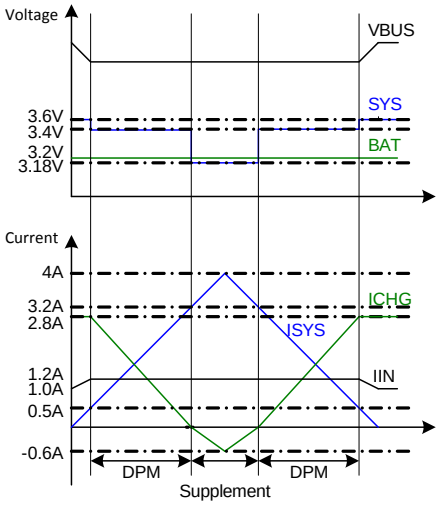

Figure 11. DPM Response

8.2.6.3 Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET VDS stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the *Supplement Mode*. As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce $R_{DS(ON)}$ until the BATFET is in full conduction. At this point onwards, the BATFET VDS linearly increases with discharge current. Figure 12 shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit *Supplement Mode* when the battery is below battery depletion threshold.

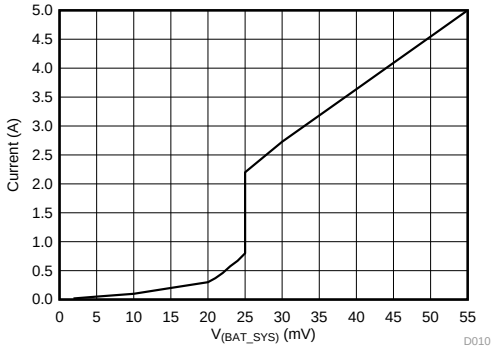

Figure 12. BATFET V-I Curve

8.2.7 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 5-A charge current for high capacity battery. The 11-mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

8.2.7.1 Autonomous Charging Cycle

With battery charging is enabled (CHG_CONFIG bit = 1 and $\overline{CE}$ pin is low), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table 4. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I^2C.

Table 4. Charging Parameter Default Setting

DEFAULT MODE	bq25890	bq25892
Charging Voltage	4.208 V	4.208 V
Charging Current	2.048 A	2.048 A
Pre-charge Current	128 mA	128 mA
Termination Current	256 mA	256 mA
Temperature Profile	JEITA	JEITA
Safety Timer	12 hour	12 hour

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled by setting CHG_CONFIG bit, /CE pin is low and ICHG register is not 0 mA
- No thermistor fault on TS pin
- No safety timer fault
- BATFET is not forced to turn off (BATFET_DIS bit = 0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and device not in DPM mode or thermal regulation. When a full battery voltage is discharged below recharge threshold (threshold selectable via VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, either toggle $\overline{CE}$ pin or CHG_CONFIG bit can initiate a new charging cycle.

The STAT output indicates the charging status of charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting STAT_DIS bit. In addition, the status register (CHRG_STAT) indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is completed, an INT is asserted to notify the host.

8.2.7.2 Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and regulates current / voltage.

Table 5. Charging Current Setting

VBAT	CHARGING CURRENT	REG DEFAULT SETTING	CHRG_STAT
< 2 V	$I_{BATSHORT}$	–	01
2 V – 3 V	I_{PRECHG}	128 mA	01
> 3 V	I_{CHG}	2048 mA	10

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If the charger device is in DPM regulation or thermal regulation during charging, the charging current can be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

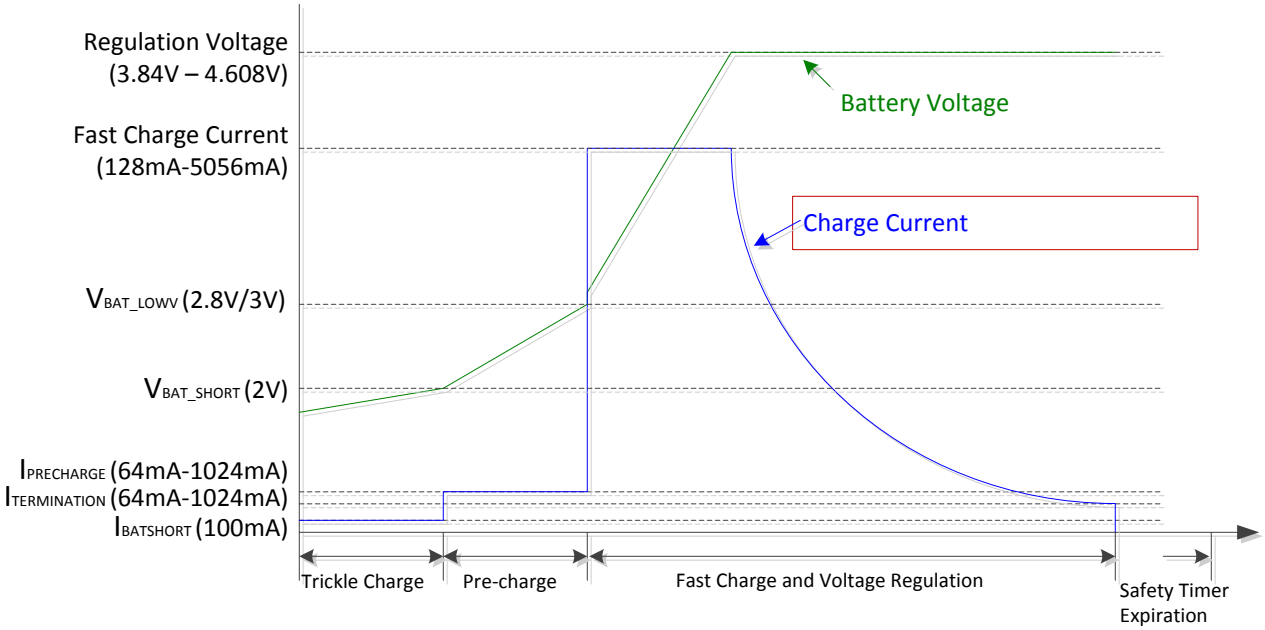

Figure 13. Battery Charging Profile

8.2.7.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage *Supplement Mode*.

When termination occurs, the status register CHRG_STAT is set to 11, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

8.2.7.4 Resistance Compensation (IRCOMP)

For high current charging system, resistance between charger output and battery cell terminal such as board routing, connector, MOSFETs and sense resistor can force the charging process to move from constant current to constant voltage too early and increase charge time. To speed up the charging cycle, the device provides resistance compensation (IRCOMP) feature which can extend the constant current charge time to delivery maximum power to battery.

The device allows the host to compensate for the resistance by increasing the voltage regulation set point based on actual charge current and the resistance as shown below. For safe operation, the host should set the maximum allowed regulation voltage register (V_{CLAMP}) and the minimum resistance compensation (BATCOMP).

$$V_{REG_ACTUAL} = VREG + \min(I_{CHRG_ACTUAL} \times BATCOMP, V_{CLAMP}) \quad (1)$$

8.2.7.5 Thermistor Qualification

8.2.7.5.1 JEITA Guideline Compliance in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

The device continuously monitors battery temperature by measuring the voltage between the TS pins and ground, typically determined by a negative temperature coefficient thermistor (NTC) and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the voltage on TS pin must be within the V_{T1} to V_{T5} thresholds. If TS voltage exceeds the T1–T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range. At cool temperature (T1–T2), JEITA recommends the charge current to be reduced to at least half of the charge current or lower. At warm temperature (T3–T5), JEITA recommends charge voltage below nominal charge voltage.

The device provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3–T5) can be 200 mV below charge voltage (JEITA_VSET=0). The current setting at cool temperature (T1–T2) can be further reduced to 20% or 50% of fast charge current (JEITA_ISET bit).

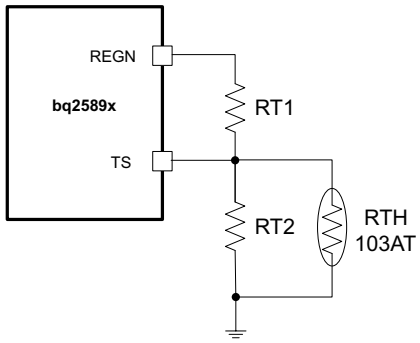

Figure 14. TS Resistor Network

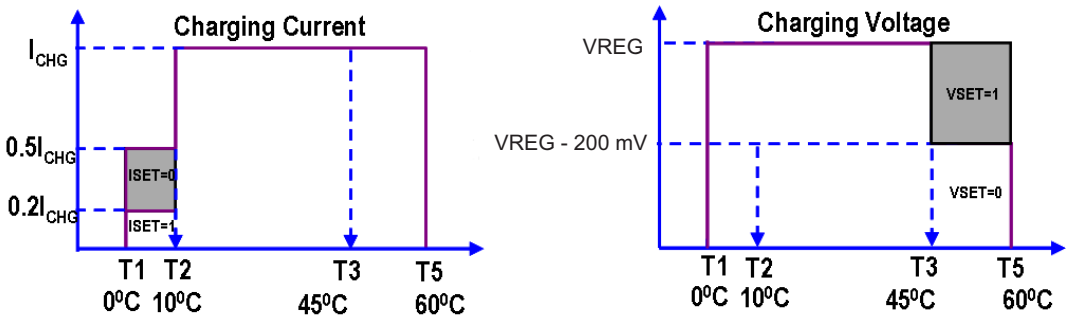

Figure 15. Charging Values

Assuming a 103AT NTC thermistor on the battery pack as shown in Figure 14, the value RT1 and RT2 can be determined by using Equation 2: :

$$RT2 = \frac{V_{REGN} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{V_{REGN}}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{V_{REGN}}{VT1} - 1\right)}$$

$$RT1 = \frac{\frac{V_{REGN}}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (2)$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery,
RTH_{T1} = 27.28 kΩ
RTH_{T5} = 3.02 kΩ
RT1 = 5.24 kΩ

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RT2 = 30.31 kΩ

8.2.7.5.2 Cold/Hot Temperature Window in Boost Mode

For battery protection during boost mode, the device monitors the battery temperature to be within the V_{BCOLDx} to V_{BHOT2} thresholds unless boost mode temperature is disabled by setting BHOT bits to 11. When temperature is outside of the temperature thresholds, the boost mode is suspended. Once temperature is within thresholds, the boost mode is recovered.

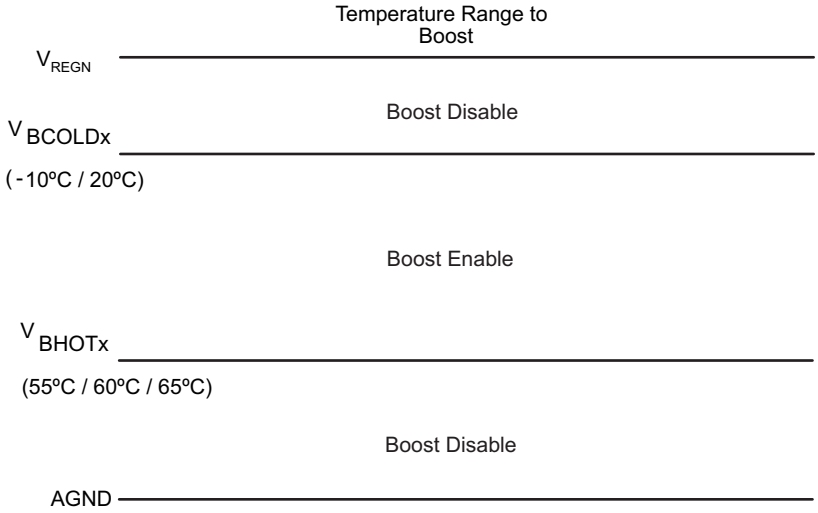

Figure 16. TS Pin Thermistor Sense Thresholds in Boost Mode

8.2.7.6 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 4 hours when the battery is below $V_{BATLOWV}$ threshold. The user can program fast charge safety timer through I^2C (CHG_TIMER bits). When safety timer expires, the fault register CHRG_FAULT bits are set to 11 and an INT is asserted to the host. The safety timer feature can be disabled via I2C by setting EN_TIMER bit.

During input voltage, current or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IDPM_STAT = 1) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This half clock rate feature can be disabled by writing 0 to TMR2X_EN bit.

8.2.8 Battery Monitor

The device includes a battery monitor to provide measurements of VBUS voltage, battery voltage, system voltage, thermistor ratio, and charging current, and charging current based on the device modes of operation. The measurements are reported in Battery Monitor Registers (REG0E-REG12). The battery monitor can be configured as two conversion modes by using CONV_RATE bit: one-shot conversion (default) and 1 second continuous conversion.

For one-shot conversion (CONV_RATE = 0), the CONV_START bit can be set to start the conversion. During the conversion, the CONV_START is set and it is cleared by the device when conversion is completed. The conversion result is ready after t_{CONV} (maximum 1 second).

For continuous conversion (CONV_RATE = 1), the CONV_RATE bit can be set to initiate the conversion. During active conversion, the CONV_START is set to indicate conversion is in progress. The battery monitor provides conversion result every 1 second automatically. The battery monitor exits continuous conversion mode when CONV_RATE is cleared.

When battery monitor is active, the REGN power is enabled and can increase device quiescent current. In battery only mode, the battery monitor is only active when $V_{(BAT)}$ > SYS_MIN setting in REG03.

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Table 6. Battery Monitor Modes of Operation

PARAMETER	REGISTER	MODES OF OPERATION			
		CHARGE MODE	BOOST MODE	DISABLE CHARGE MODE	BATTERY ONLY MODE
Battery Voltage (V_{BAT})	REG0E	Yes	Yes	Yes	Yes
System Voltage (V_{SYS})	REG0F	Yes	Yes	Yes	Yes
Temperature (TS) Voltage (V_{TS})	REG10	Yes	Yes	Yes	Yes
VBUS Voltage (V_{VBUS})	REG11	Yes	Yes	Yes	NA
Charge Current (I_{BAT})	REG12	Yes	NA	NA	NA

8.2.9 Status/Control Outputs (STAT, INT and DSEL)

8.2.9.1 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED as shown in Figure 47. The STAT pin function can be disable by setting STAT_DIS bit.

Table 7. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input overvoltage, TS fault, timer fault, input or system overvoltage). Boost Mode suspend (due to TS Fault)	blinking at 1 Hz

8.2.9.2 Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate 256-µs INT pulse.

- USB/adapter source identified (through PSEL or DPDM detection, with OTG pin)
- Good input source detected
  - VBUS above battery (not in sleep)
  - VBUS below V_{ACOV} threshold
  - VBUS above $V_{VBUSMIN}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Input removed
- Charge Complete
- Any FAULT event in REG0C

When a fault occurs, the charger device sends out INT and keeps the fault state in REG0C until the host reads the fault register. Before the host reads REG0C and all the faults are cleared, the charger device would not send any INT upon new faults. To read the current fault status, the host has to read REG0C two times consecutively. The 1st read reports the pre-existing fault register status and the 2nd read reports the current fault register status.

8.2.9.3 D+/D- Multiplexer Selection Control

The DSEL pin is normally grounded and pulled-up by internally to 5V during input source type detection (when AUTO_DPDM_EN=1 or FORCE_DPDM=1). The pin is normally low and drives high to indicate the D+/D- detection is in progress. When detection is completed, the pin maintains high logic when DCP, MaxCharge or HVDCP is detected. The pin returns to logic low when other input source type is detected. In addition, while input source is plugged in or during OTG mode, the FORCE_DSEL bit can be set to force the DSEL pin to change from low to high regardless of input source type detected. When in battery discharge mode (not in OTG), the DSEL pin is always low.

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8.2.10 BATET (Q4) Control

8.2.10.1 BATFET Disable Mode (Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host set BATFET_DIS bit, the charger can turn off BATFET immediately or delay by t_{SM_DLY} as configurated by BATFET_DLY bit.

8.2.10.2 BATFET Enable (Exit Shipping Mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET_DIS, one of the following events can enable BATFET to restore system power:

1. Plug in adapter
2. Clear BATFET_DIS bit
3. Set REG_RST bit to reset all registers including BATFET_DIS bit to default (0)
4. A logic high to low transition on $\overline{QON}$ pin with $t_{SHIPMODE}$ deglitch time to enable BATFET to exit shipping mode

8.2.10.3 BATFET Full System Reset

The BATFET functions as a load switch between battery and system when input source is not plugged-in. By changing the state of BATFET from off to on, system connects to SYS can be effectively have a power-on-reset. The $\overline{QON}$ pin supports push-button interface to reset system power without host by change the state of BATFET.

When the $\overline{QON}$ pin is driven to logic low for t_{QON_RST} (typical 15 seconds) while input source is not plugged in and BATFET is enabled (BATFET_DIS=0), the BATFET is turned off for t_{BATFET_RST} and then it is re-enabled to reset system power. This function can be disabled by setting BATFET_RST_EN bit to 0.

8.2.11 Current Pulse Control Protocol

The device provides the control to generate the VBUS current pulse protocol to communicate with adjustable high voltage adapter in order to signal adapter to increase or decrease output voltage. To enable the interface, the EN_PUMPX bit must be set. Then the host can select the increase/decrease voltage pulse by setting one of the PUMPX_UP or PUMPX_DN bit (but not both) to start the VBUS current pulse sequence. During the current pulse sequence, the PUMPX_UP and PUMPX_DN bits are set to indicate pulse sequence is in progress and the device pulses the input current limit between current limit set forth by IINLIM or IDPM_LIM register and the 100mA current limit ($I_{INDPM100_ACC}$). When the pulse sequence is completed, the input current limit is returned to value set by IINLIM or IDPM_LIM register and the PUMPX_UP or PUMPX_DN bit is cleared. In addition, the EN_PUMPX can be cleared during the current pulse sequence to terminate the sequence and force charger to return to input current limit as set forth by the IINLIM or IDPM_LIM register immediately. When EN_PUMPX bit is low, write to PUMPX_UP and PUMPX_DN bit would be ignored and have no effect on VBUS current limit.

8.2.12 D+/D- Output Driver

The device provides independent controlled voltage output drivers on D+ and D- pins to interface or emulate non-standard adapters when input source is plugged-in or OTG mode is enabled. The D+/D- drivers are disabled in high impedance mode (HiZ) by default or when DP_DAC or DM_DAC bits are set to 000. The drivers are enabled and controlled independently with predefined voltage threshold when DP_DAC and DM_DAC bits are set to values between 001 to 110.

When input source is plugged-in, the output drivers control (DP_DAC and DM_DAC) are reset to HiZ (000) to execute USB BC1.2 and built-in handshake during the input source type detection. The host is recommended to change DP_DAC and DM_DAC settings after input source type detection when VBUS_STAT/PG_STAT bits are updated.

When OTG mode is enabled, the drivers can be enabled to provide electrical signature on D+/D- to emulate USB non-standard adapters (Divider 1-4) as shown in Table 1.

8.2.13 Input Current Limit on ILIM

For safe operation, the device has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

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$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (3)$$

The actual input current limit is the lower value between ILIM setting and register setting (IINLIM). For example, if the register setting is 111111 for 3.25 A, and ILIM has a 260-Ω resistor (KILIM = 390 max.) to ground for 1.5 A, the input current limit is 1.5 A. ILIM pin can be used to set the input current limit rather than the register settings when EN_ILIM bit is set. The device regulates ILIM pin at 0.8 V. If ILIM voltage exceeds 0.8 V, the device enters input current regulation (Refer to *Dynamic Power Management* section).

The ILIM pin can also be used to monitor input current when EN_ILIM is enabled. The voltage on ILIM pin is proportional to the input current. ILIM pin can be used to monitor the input current following Equation 4:

$$I_{IN} = \frac{K_{ILIM} \times V_{ILIM}}{R_{ILIM} \times 0.8\ V} \quad (4)$$

For example, if ILIM pin is set with 260-Ω resistor, and the ILIM voltage is 0.4 V, the actual input current 0.615 A - 0.75 A (based on KILM specified). If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 0.8 V. If ILIM pin is short, the input current limit is set by the register.

The ILIM pin function can be disabled by setting EN_ILIM bit to 0. When the pin is disabled, both input current limit function and monitoring function are not available.

8.2.14 Thermal Regulation and Thermal Shutdown

8.2.14.1 Thermal Protection in Buck Mode

The device monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds the preset thermal regulation limit (TREG bits), the device lowers down the charge current. The wide thermal regulation range from 60ºC to 120ºC allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds T_{SHUT}. The fault register CHRG_FAULT is set to 10 and an INT is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is below T_{SHUT_HYS}.

8.2.14.2 Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC surface temperature exceeds T_{SHUT}, the boost mode is disabled (converter is turned off) by setting OTG_CONFIG bit low and BATFET is turned off. When IC surface temperature is below T_{SHUT_HYS}, the BATFET is enabled automatically to allow system to restore and the host can re-enable OTG_CONFIG bit to recover.

8.2.15 Voltage and Current Monitoring in Buck and Boost Mode

8.2.15.1 Voltage and Current Monitoring in Buck Mode

The device closely monitors the input and system voltage, as well as HSFET current for safe buck and boost mode operations.

8.2.15.1.1 Input Overvoltage (ACOV)

The input voltage for buck mode operation is V_{VBUS_OP}. If VBUS voltage exceeds V_{ACOV}, the device stops switching immediately. During input over voltage (ACOV), the fault register CHRG_FAULT bits sets to 01. An INT is asserted to the host..

8.2.15.1.2 System Overvoltage Protection (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. When SYSOVP is detected, the converter stops immediately to clamp the overshoot.

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8.2.15.2 Voltage and Current Monitoring in Boost Mode

The device closely monitors the VBUS voltage, as well as RBFET and LSFET current to ensure safe boost mode operation.

8.2.15.2.1 VBUS Overcurrent Protection

The charger device closely monitors the RBFET (Q1), and LSFET (Q3) current to ensure safe boost ode operation. During overcurrent condition when output current exceed (I_{OTG_OCP}) the device operates in hiccup mode for protection. While in hiccup mode cycle, the device turns off RBFET for $t_{OTG_OCP_OFF}$ (30 ms typical) and turns on RBFET for $t_{OTG_OCP_ON}$ (250 µs typical) in an attempt to restart. If the overcurrent condition is removed, the boost converter returns to normal operation. When overcurrent condition continues to exist, the device repeats the hiccup cycle until overcurrent condition is removed. When overcurrent condition is detected the fault register bit BOOST_FAULT is set high to indicate fault in boost operation. An INT is also asserted to the host.

8.2.15.2.2 Boost Mode Overvoltage Protection

When the VBUS voltage rises above regulation target and exceeds V_{OTG_OVP}, the device enters overvoltage protection which stops switching, clears OTG_CONFIG bit and exits boost mode. During the overvoltage duration, the fault register bit (BOOST_FAULT) is set high to indicate fault in boost operation. An INT is also asserted to the host.

8.2.16 Battery Protection

8.2.16.1 Battery Overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register BAT_FAULT bit goes high and an INT is asserted to the host.

8.2.16.2 Battery Over-Discharge Protection

When battery is discharged below V_{BAT_DPL}, the BATFET is turned off to protect battery from over discharge. To recover from over-discharge, an input source is required at VBUS. When an input source is plugged in, the BATFET turns on. Thy is charged with $I_{BATSHORT}$ (typically 100 mA) current when the VBAT < V_{SHORT}, or precharge current as set in IPRECHG register when the battery voltage is between V_{SHORT} and $V_{BATLOWV}$.

8.2.16.3 System Overcurrent Protection

When the system is shorted or significantly overloaded (I_{BAT} > I_{BATOP}) so that its current exceeds the overcurrent limit, the device latches off BATFET. Section *BATFET Enable (Exit Shipping Mode)* can reset the latch-off condition and turn on BATFET

8.2.17 Serial Interface

The device uses I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6AH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG14. Register read beyond REG14 (0x14) returns 0xFF. The I^2C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

8.2.17.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

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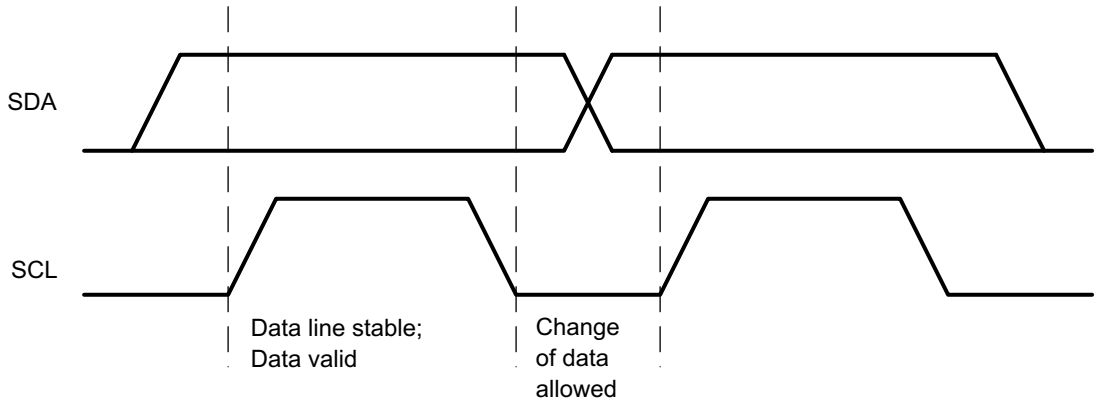

Figure 17. Bit Transfer on the I²C Bus

8.2.17.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

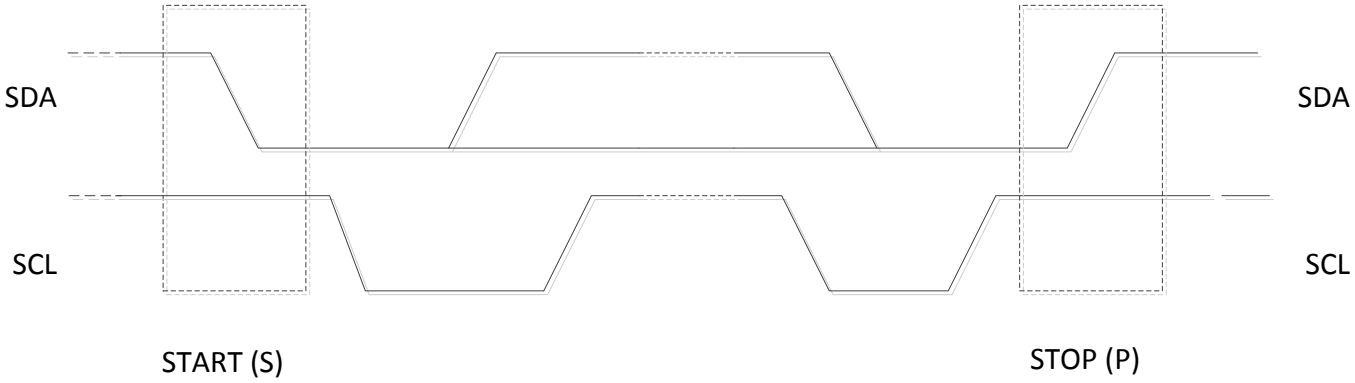

Figure 18. START and STOP conditions

8.2.17.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

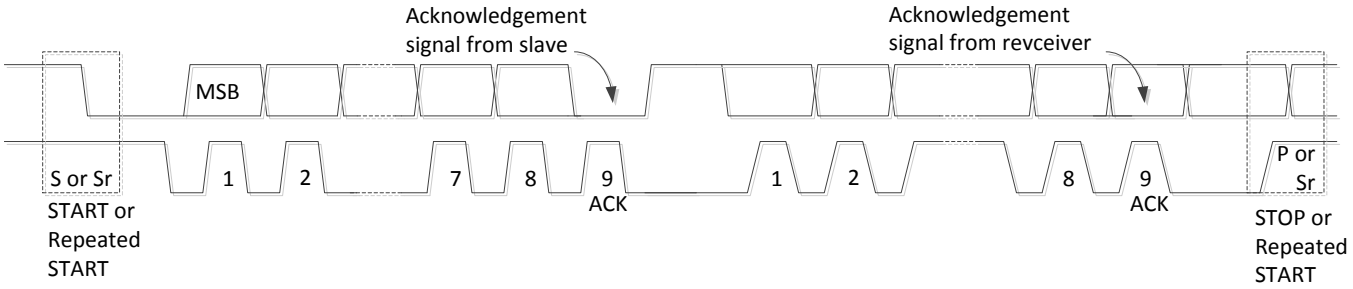

Figure 19. Data Transfer on the I²C Bus

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8.2.17.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

8.2.17.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

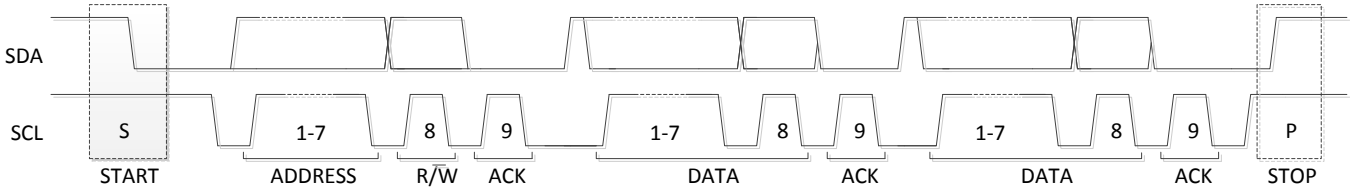

Figure 20. Complete Data Transfer

8.2.17.6 Single Read and Write

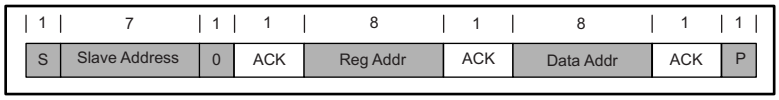

Figure 21. Single Write

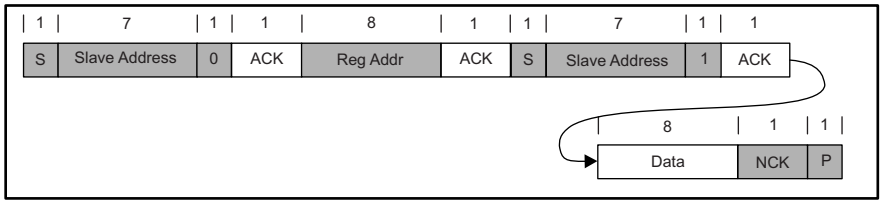

Figure 22. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

8.2.17.7 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG14 except REG0C.

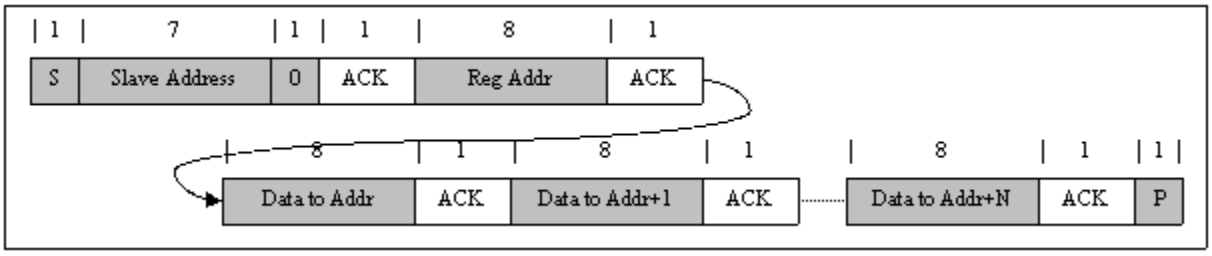

Figure 23. Multi-Write

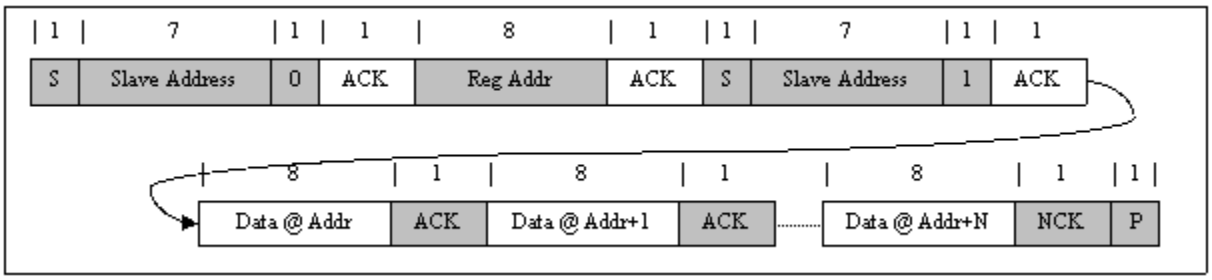

Figure 24. Multi-Read

REG0C is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG0C reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REG0C for the second time. The only exception is NTC_FAULT which always reports the actual condition on the TS pin. In addition, REG0C does not support multi-read and multi-write.

8.3 Device Functional Modes

8.3.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WATCHDOG_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG_FAULT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings.

In default mode, the device keeps charging the battery with 12-hour fast charging safety timer. At the end of the 12-hour, the charging is stopped and the buck converter continues to operate to supply system load. Any write command to device transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits=00.

When the watchdog timer (WATCHDOG_FAULT bit = 1) is expired, the device returns to default mode and all registers are reset to default values except IINLIM, VINDPM, VINDPM_OS, BATFET_RST_EN, BATFET_DLY, and BATFET_DIS bits.

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Device Functional Modes (continued)

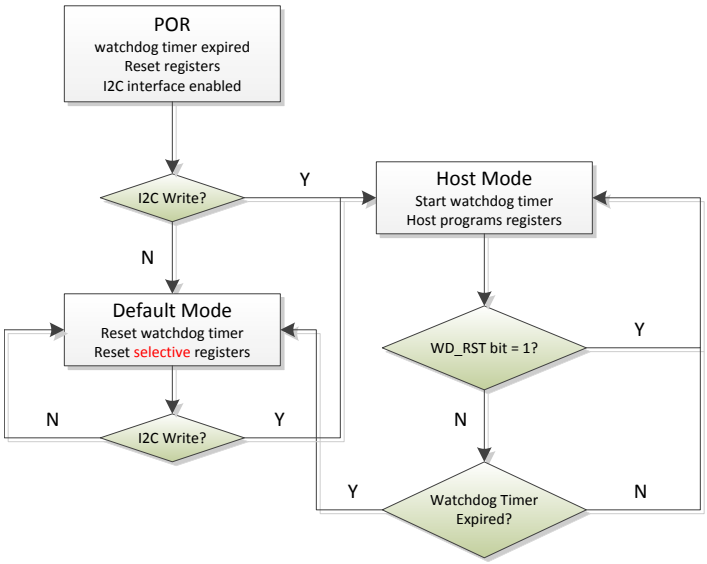

Figure 25. Watchdog Timer Flow Chart

8.4 Register Maps

I2C Slave Address: 6AH (1101010B + R/$\overline{W}$)

8.4.1 REG00

Figure 26. REG00

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. REG00

Bit	Field	Type	Reset	Description	
7	EN_HIZ	R/W	by REG_RST by Watchdog	Enable HIZ Mode 0 – Disable (default) 1 – Enable	
6	EN_ILIM	R/W	by REG_RST by Watchdog	Enable ILIM Pin 0 – Disable 1 – Enable (default: Enable ILIM pin (1))	
5	IINLIM[5]	R/W	by REG_RST	1600mA	Input Current Limit Offset: 100mA Range: 100mA (000000) – 3.25A (111111) Default:0001000 (500mA) (Actual input current limit is the lower of I2C or ILIM pin) IINLIM bits are changed automaticallly after input source type detection is completed USB Host SDP = 500mA USB CDP = 1.5A USB DCP = 3.25A Adjustable High Voltage (MaxCharge) DCP = 1.5A Unknown Adapter = 500mA Non-Standard Adapter = 1A/2A/2.1A/2.4A
4	IINLIM[4]	R/W	by REG_RST	800mA	
3	IINLIM[3]	R/W	by REG_RST	400mA	
2	IINLIM[2]	R/W	by REG_RST	200mA	
1	IINLIM[1]	R/W	by REG_RST	100mA	
0	IINLIM[0]	R/W	by REG_RST	50mA	

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8.4.2 REG01

Figure 27. REG01

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. REG01

Bit	Field	Type	Reset	Description
7	DP_DAC[2]	R/W	by REG_RST	D+ Pin Output Driver 000 – HiZ mode (Default) 001 – 0V (V_{0P0_VSRC}) 010 – 0.6V (V_{0P6_VSRC}) 011 – 1.2V (V_{1P2_VSRC}) 100 – 2.0V (V_{2P0_VSRC}) 101 – 2.7V (V_{2P7_VSRC}) 110 – 3.3V (V_{3P3_VSRC}) 111 – Reserved Register bits are reset to default value when input source is plugged-in and can be changed after D+/D- detection is completed.
6	DP_DAC[1]	R/W	by REG_RST	
5	DP_DAC[0]	R/W	by REG_RST	
4	DM_DAC[2]	R/W	by REG_RST	D- Pin Output Driver 000 – HiZ mode (Default) 001 – 0V (V_{0P0_VSRC}) 010 – 0.6V (V_{0P6_VSRC}) 011 – 1.2V (V_{1P2_VSRC}) 100 – 2.0V (V_{2P0_VSRC}) 101 – 2.7V (V_{2P7_VSRC}) 110 – 3.3V (V_{3P3_VSRC}) 111 – Reserved Register bits are reset to default value when input source is plugged-in and can be changed after D+/D- detection is completed.
3	DM_DAC[1]	R/W	by REG_RST	
2	DM_DAC[0]	R/W	by REG_RST	
1	EN_12V	R/W	by REG_RST	Enable 12V detection for MaxCharge and HVDCP 0 – Disable 12V Detection (default) 1 – Enable 12V Detection
0	VINDPM_OS	R/W	by REG_RST	Input Voltage Limit Offset 0 – 400mV 1 – 600mV (default)

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8.4.3 REG02

Figure 28. REG02

7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. REG02

Bit	Field	Type	Reset	Description
7	CONV_START	R/W	by REG_RST by Watchdog	ADC Conversion Start Control 0 – ADC conversion not active (default). 1 – Start ADC Conversion This bit is read-only when CONV_RATE = 1. The bit stays high during ADC conversion and during input source detection.
6	CONV_RATE	R/W	by REG_RST by Watchdog	ADC Conversion Rate Selection 0 – One shot ADC conversion (default) 1 – Start 1s Continuous Conversion
5	BOOST_FREQ	R/W	by REG_RST by Watchdog	Boost Mode Frequency Selection 0 – 1.5MHz 1 – 500KHz Note: Write to this bit is ignored when OTG_CONFIG is enabled.
4	ICO_EN	R/W	by REG_RST	Input Current Optimizer (ICO) Enable 0 – Disable ICO Algorithm 1 – Enable ICO Algorithm (default)
3	HVDCP_EN	R/W	by REG_RST	High Voltage DCP Enable 0 – Disable HVDCP handshake 1 – Enable HVDCP handshake (default)
2	MAXC_EN	R/W	by REG_RST	MaxCharge Adapter Enable 0 – Disable MaxCharge handshake 1 – Enable MaxCharge handshake (default)
1	FORCE_DPDM	R/W	by REG_RST by Watchdog	Force D+/D- Detection 0 – Not in D+/D- or PSEL detection (default) 1 – Force D+/D- detection
0	AUTO_DPDM_EN	R/W	by REG_RST	Automatic D+/D- Detection Enable 0 –Disable D+/D- or PSEL detection when VBUS is plugged-in 1 –Enable D+/D- or PEL detection when VBUS is plugged-in (default)

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8.4.4 REG03

Figure 29. REG03

7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. REG03

Bit	Field	Type	Reset	Description	
7	FORCE_DSEL	R/W	by REG_RST	DSEL Pin Control 0 – Allow DSEL pin output to drive low (default) 1 – Force DSEL pin output to drive high	
6	WD_RST	R/W	by REG_RST by Watchdog	I2C Watchdog Timer Reset 0 – Normal (default) 1 – Reset (Back to 0 after timer reset)	
5	OTG_CONFIG	R/W	by REG_RST by Watchdog	Boost (OTG) Mode Configuration 0 – OTG Disable (default) 1 – OTG Enable	
4	CHG_CONFIG	R/W	by REG_RST by Watchdog	Charge Enable Configuration 0 - Charge Disable 1- Charge Enable (default)	
3	SYS_MIN[2]	R/W	by REG_RST	0.4V	Minimum System Voltage Limit Offset: 3.0V Range 3.0V-3.7V Default: 3.5V (101)
2	SYS_MIN[1]	R/W	by REG_RST	0.2V	
1	SYS_MIN[02]	R/W	by REG_RST	0.1V	
0	MIN_VBAT_SEL	R/W	by REG_RST by Watchdog	Minimum Battery Voltage (falling) to exit boost mode 0 - 2.9V (default) 1- 2.5V	

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8.4.5 REG04

Figure 30. REG04

7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. REG04

Bit	Field	Type	Reset	Description	
7	EN_PUMPX	R/W	by Softwareby by Watchdog	Current pulse control Enable 0 - Disable Current pulse control (default) 1- Enable Current pulse control (PUMPX_UP and PUMPX_DN)	
6	ICHG[6]	R/W	by Softwareby by Watchdog	4096mA	Fast Charge Current Limit Offset: 0mA Range: 0mA (0000000) – 5056mA (1001111) Default: 2048mA (0100000) Note: ICHG=000000 (0mA) disables charge ICHG > 1001111 (5056mA) is clamped to register value 1001111 (5056mA)
5	ICHG[5]	R/W	by Softwareby by Watchdog	2048mA	
4	ICHG[4]	R/W	by Softwareby by Watchdog	1024mA	
3	ICHG[3]	R/W	by Softwareby by Watchdog	512mA	
2	ICHG[2]	R/W	by Softwareby by Watchdog	256mA	
1	ICHG[1]	R/W	by Softwareby by Watchdog	128mA	
0	ICHG[0]	R/W	by Softwareby by Watchdog	64mA	

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8.4.6 REG05

Figure 31. REG05

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. REG05

Bit	Field	Type	Reset	Description	
7	IPRECHG[3]	R/W	by Softwareby by Watchdog	512mA	Precharge Current Limit Offset: 64mA Range: 64mA – 1024mA Default: 128mA (0001)
6	IPRECHG[2]	R/W	by Softwareby by Watchdog	256mA	
5	IPRECHG[1]	R/W	by Softwareby by Watchdog	128mA	
4	IPRECHG[0]	R/W	by Softwareby by Watchdog	64mA	
3	ITERM[3]	R/W	by Softwareby by Watchdog	512mA	Termination Current Limit Offset: 64mA Range: 64mA – 1024mA Default: 256mA (0011)
2	ITERM[2]	R/W	by Softwareby by Watchdog	256mA	
1	ITERM[1]	R/W	by Softwareby by Watchdog	128mA	
0	ITERM[0]	R/W	by Softwareby by Watchdog	64mA	

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8.4.7 REG06

Figure 32. REG06

7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. REG06

Bit	Field	Type	Reset	Description	
7	VREG[5]	R/W	by Softwareby by Watchdog	512mV	Charge Voltage Limit Offset: 3.840V Range: 3.840V – 4.608V (110000) Default: 4.208V (010111) Note: VREG > 110000 (4.608V) is clamped to register value 110000 (4.608V)
6	VREG[4]	R/W	by Softwareby by Watchdog	256mV	
5	VREG[3]	R/W	by Softwareby by Watchdog	128mV	
4	VREG[2]	R/W	by Softwareby by Watchdog	64mV	
3	VREG[1]	R/W	by Softwareby by Watchdog	32mV	
2	VREG[0]	R/W	by Softwareby by Watchdog	16mV	
1	BATLOWV	R/W	by Softwareby by Watchdog	Battery Precharge to Fast Charge Threshold 0 – 2.8V 1 – 3.0V (default)	
0	VRECHG	R/W	by Softwareby by Watchdog	Battery Recharge Threshold Offset (below Charge Voltage Limit) 0 – 100mV (V_{RECHG}) below VREG (REG06[7:2]) (default) 1 – 200mV (V_{RECHG}) below VREG (REG06[7:2])	

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8.4.8 REG07

Figure 33. REG07

7	6	5	4	3	2	1	0
1	0	0	1	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. REG07

Bit	Field	Type	Reset	Description
7	EN_TERM	R/W	by Softwareby Watchdog	Charging Termination Enable 0 – Disable 1 – Enable (default)
6	STAT_DIS	R/W	by Softwareby Watchdog	STAT Pin Disable 0 – Enable STAT pin function (default) 1 – Disable STAT pin function
5	WATCHDOG[1]	R/W	by Softwareby Watchdog	I2C Watchdog Timer Setting 00 – Disable watchdog timer 01 – 40s (default) 10 – 80s 11 – 160s
4	WATCHDOG[0]	R/W	by Softwareby Watchdog	
3	EN_TIMER	R/W	by Softwareby Watchdog	Charging Safety Timer Enable 0 – Disable 1 – Enable (default)
2	CHG_TIMER[1]	R/W	by Softwareby Watchdog	Fast Charge Timer Setting 00 – 5 hrs 01 – 8 hrs 10 – 12 hrs (default) 11 – 20 hrs
1	CHG_TIMER[0]	R/W	by Softwareby Watchdog	
0	JEITA_ISET (0C-10C)	R/W	by Softwareby Watchdog	JEITA Low Temperature Current Setting 0 – 50% of ICHG (REG04[6:0]) 1 – 20% of ICHG (REG04[6:0]) (default)

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8.4.9 REG08

Figure 34. REG08

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. REG08

Bit	Field	Type	Reset	Description	
7	BAT_COMP[2]	R/W	by Softwareby by Watchdog	80mΩ	IR Compensation Resistor Setting Range: 0 – 140mΩ Default: 0Ω (000) (i.e. Disable IRComp)
6	BAT_COMP[1]	R/W	by Softwareby by Watchdog	40mΩ	
5	BAT_COMP[0]	R/W	by Softwareby by Watchdog	20mΩ	
4	VCLAMP[2]	R/W	by Softwareby by Watchdog	128mV	IR Compensation Voltage Clamp above VREG (REG06[7:2]) Offset: 0mV Range: 0-224mV Default: 0mV (000)
3	VCLAMP[1]	R/W	by Softwareby by Watchdog	64mV	
2	VCLAMP[0]	R/W	by Softwareby by Watchdog	32mV	
1	TREG[1]	R/W	by Softwareby by Watchdog	Thermal Regulation Threshold 00 – 60°C 01 – 80°C 10 – 100°C 11 – 120°C (default)	
0	TREG[0]	R/W	by Softwareby by Watchdog		

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8.4.10 REG09

Figure 35. REG09

7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. REG09

Bit	Field	Type	Reset	Description
7	FORCE_ICO	R/W	by Softwareby by Watchdog	Force Start Input Current Optimizer (ICO) 0 – Do not force ICO (default) 1 – Force ICO Note: This bit is can only be set only and always returns to 0 after ICO starts
6	TMR2X_EN	R/W	by Softwareby by Watchdog	Safety Timer Setting during DPM or Thermal Regulation 0 – Safety timer not slowed by 2X during input DPM or thermal regulation 1 – Safety timer slowed by 2X during input DPM or thermal regulation (default)
5	BATFET_DIS	R/W	by Softwareby	Force BATFET off to enable ship mode 0 – Allow BATFET turn on (default) 1 – Force BATFET off
4	JEITA_VSET (45C-60C)	R/W	by Software by Watchdog	JEITA High Temperature Voltage Setting 0 – Set Charge Voltage to VREG-200mV during JEITA hig temperature (default) 1 – Set Charge Voltage to VREG during JEITA high temperature
3	BATFET_DLY	R/W	by Softwareby	BATFET turn off delay control 0 – BATFET turn off immediately when BATFET_DIS bit is set (default) 1 – BATFET turn off delay by t_{SM_DLY} when BATFET_DIS bit is set
2	BATFET_RST_EN	R/W	by Softwareby	BATFET full system reset enable 0 – Disable BATFET full system reset 1 – Enable BATFET full system reset (default)
1	PUMPX_UP	R/W	by Softwareby by Watchdog	Current pulse control voltage up enable 0 – Disable (default) 1 – Enable Note: This bit is can only be set when EN_PUMPX bit is set and returns to 0 after current pulse control sequence is completed
0	PUMPX_DN	R/W	by Softwareby by Watchdog	Current pulse control voltage down enable 0 – Disable (default) 1 – Enable Note: This bit is can only be set when EN_PUMPX bit is set and returns to 0 after current pulse control sequence is completed

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8.4.11 REG0A

Figure 36. REG0A

7	6	5	4	3	2	1	0
0	1	1	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. REG0A

Bit	Field	Type	Reset	Description	
7	BOOSTV[3]	R/W	by Softwareby by Watchdog	512mV	Boost Mode Voltage Regulation Offset: 4.55V Range: 4.55V – 5.51V Default:4.998V(0111)
6	BOOSTV[2]	R/W	by Softwareby by Watchdog	256mV	
5	BOOSTV[1]	R/W	by Softwareby	128mV	
4	BOOSTV[0]	R/W	by Softwareby by Watchdog	64mV	
3	PFM_OTG_DIS	R/W	by Software	PFM mode allowed in boost mode 0 – Allow PFM in boost mode (default) 1 – Disable PFM in boost mode	
2	BOOST_LIM[2]	R/W	by Software by Watchdog	000: 0.5A 001: 0.75A 010: 1.2A 011: 1.4A 100: 1.65A 101: 1.875A 110: 2.15A 111: 2.45A	Boost Mode Current Limit Default: 1.4A (011)
1	BOOST_LIM[1]	R/W	by Software by Watchdog		
0	BOOST_LIM[0]	R/W	by Software by Watchdog		

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8.4.12 REG0B

Figure 37. REG0B

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. REG0B

Bit	Field	Type	Reset	Description
7	VBUS_STAT[2]	R	N/A	VBUS Status register 000: No Input 001: USB Host SDP 010: USB CDP (1.5A) 011: USB DCP (3.25A) 100: Adjustable High Voltage DCP (MaxCharge) (1.5A) 101: Unknown Adapter (500mA) 110: Non-Standard Adapter (1A/2A/2.1A/2.4A) 111: OTG Note: Software current limit is reported in IINLIM register
6	VBUS_STAT[1]	R	N/A	
5	VBUS_STAT[0]	R	N/A	
4	CHRG_STAT[1]	R	N/A	Charging Status 00 – Not Charging 01 – Pre-charge (< $V_{BATLOWV}$) 10 – Fast Charging 11 – Charge Termination Done
3	CHRG_STAT[0]	R	N/A	
2	PG_STAT	R	N/A	Power Good Status 0 – Not Power Good 1 – Power Good
1	Reserved			Reserved: Always reads 0
0	VSYS_STAT	R	N/A	VSYS Regulation Status 0 – Not in VSYSMIN regulation (BAT > VSYSMIN) 1 – In VSYSMIN regulation (BAT < VSYSMIN)

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8.4.13 REG0C

Figure 38. REG0C

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. REG0C

Bit	Field	Type	Reset	Description
7	WATCHDOG_FAULT	R	N/A	Watchdog Fault Status Status 0 – Normal 1- Watchdog timer expiration
6	BOOST_FAULT	R	N/A	Boost Mode Fault Status 0 – Normal 1 – VBUS overloaded in OTG, or VBUS OVP, or battery is too low in boost mode
5	CHRG_FAULT[1]	R	N/A	Charge Fault Status 00 – Normal 01 – Input fault (VBUS > V_{ACOV} or VBAT < VBUS < $V_{VBUSMIN}$(typical 3.8V)) 10 - Thermal shutdown 11 – Charge Safety Timer Expiration
4	CHRG_FAULT[0]	R	N/A	
3	BAT_FAULT	R	N/A	Battery Fault Status 0 – Normal 1 – BATOVP (VBAT > V_{BATOVP})
2	NTC_FAULT[2]	R	N/A	NTC Fault Status Buck Mode: 000 – Normal 010 – TS Warm 011 – TS Cool 101 – TS Cold 110 – TS Hot Boost Mode: 000 – Normal 101 – TS Cold 110 – TS Hot
1	NTC_FAULT[1]	R	N/A	
0	NTC_FAULT[0]	R	N/A	

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8.4.14 REG0D

Figure 39. REG0D

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. REG0D

Bit	Field	Type	Reset	Description	
7	FORCE_VINDPM	R/W	by Softwareby	VINDPM Threshold Setting Method 0 – Run Relative VINDPM Threshold (default) 1 – Run Absolute VINDPM Threshold Note: Register is reset to default value when input source is plugged-in	
6	VINDPM[6]	R/W	by Softwareby	6400mV	Absolute VINDPM Threshold Offset: 2.6V Range: 3.9V (0001101) – 15.3V (1111111) Default: 4.4V (0010010) Note: Value < 0001101 is clamped to 3.9V (0001101) Register is read only when FORCE_VINDPM=0 and can be written by internal control based on relative VINDPM threshold setting Register can be read/write when FORCE_VINDPM = 1 Note: Register is reset to default value when input source is plugged-in
5	VINDPM[5]	R/W	by Softwareby	3200mV	
4	VINDPM[4]	R/W	by Softwareby	1600mV	
3	VINDPM[3]	R/W	by Softwareby	800mV	
2	VINDPM[2]	R/W	by Softwareby	400mV	
1	VINDPM[1]	R/W	by Softwareby	200mV	
0	VINDPM[0]	R/W	by Softwareby	100mV	

8.4.15 REG0E

Figure 40. REG0E

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. REG0E

Bit	Field	Type	Reset	Description	
7	THERM_STAT	R	N/A	Thermal Regulation Status 0 – Normal 1 – In Thermal Regulation	
6	BATV[6]	R	N/A	1280mV	ADC conversion of Battery Voltage (V_{BAT}) Offset: 2.304V Range: 2.304V (0000000) – 4.848V (1111111) Default: 2.304V (0000000)
5	BATV[5]	R	N/A	640mV	
4	BATV[4]	R	N/A	320mV	
3	BATV[3]	R	N/A	160mV	
2	BATV[2]	R	N/A	80mV	
1	BATV[1]	R	N/A	40mV	
0	BATV[0]	R	N/A	20mV	

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8.4.16 REG0F

Figure 41. REG0F

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. REG0F

Bit	Field	Type	Reset	Description	
7	Reserved	R	N/A	Reserved: Always reads 0	
6	SYSV[6]	R	N/A	1280mV	ADDC conversion of System Voltage (V_{SYS}) Offset: 2.304V Range: 2.304V (0000000) – 4.848V (1111111) Default: 2.304V (0000000)
5	SYSV[5]	R	N/A	640mV	
4	SYSV[4]	R	N/A	320mV	
3	SYSV[3]	R	N/A	160mV	
2	SYSV[2]	R	N/A	80mV	
1	SYSV[1]	R	N/A	40mV	
0	SYSV[0]	R	N/A	20mV	

8.4.17 REG10

Figure 42. REG10

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. REG10

Bit	Field	Type	Reset	Description	
7	Reserved	R	N/A	Reserved: Always reads 0	
6	TSPCT[6]	R	N/A	29.76%	ADC conversion of TS Voltage (TS) as percentage of REGN Offset: 21% Range 21% (0000000) – 80% (1111111) Default: 21% (0000000)
5	TSPCT[5]	R	N/A	14.88%	
4	TSPCT[4]	R	N/A	7.44%	
3	TSPCT[3]	R	N/A	3.72%	
2	TSPCT[2]	R	N/A	1.86%	
1	TSPCT[1]	R	N/A	0.93%	
0	TSPCT[0]	R	N/A	0.465%	

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8.4.18 REG11

Figure 43. REG11

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. REG11

Bit	Field	Type	Reset	Description	
7	VBUS_GD	R	N/A	VBUS Good Status 0 – Not VBUS attached 1 – VBUS Attached	
6	VBUSV[6]	R	N/A	6400mV	ADC conversion of VBUS voltage (V_{BUS}) Offset: 2.6V Range 2.6V (0000000) – 15.3V (1111111) Default: 2.6V (0000000)
5	VBUSV[5]	R	N/A	3200mV	
4	VBUSV[4]	R	N/A	1600mV	
3	VBUSV[3]	R	N/A	800mV	
2	VBUSV[2]	R	N/A	400mV	
1	VBUSV[1]	R	N/A	200mV	
0	VBUSV[0]	R	N/A	100mV	

8.4.19 REG12

Figure 44. REG12

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. REG12

Bit	Field	Type	Reset	Description	
7	Unused	R	N/A	Always reads 0	
6	ICHGR[6]	R	N/A	3200mA	ADC conversion of Charge Current (I_{BAT}) when V_{BAT} > $V_{BATSHORT}$ Offset: 0mA Range 0mA (0000000) – 6350mA (1111111) Default: 0mA (0000000) Note: This register returns 0000000 for V_{BAT} < $V_{BATSHORT}$
5	ICHGR[5]	R	N/A	1600mA	
4	ICHGR[4]	R	N/A	800mA	
3	ICHGR[3]	R	N/A	400mA	
2	ICHGR[2]	R	N/A	200mA	
1	ICHGR[1]	R	N/A	100mA	
0	ICHGR[0]	R	N/A	50mA	

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8.4.20 REG13

Figure 45. REG13

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. REG13

Bit	Field	Type	Reset	Description	
7	VDPM_STAT	R	N/A	VINDPM Status 0 – Not in VINDPM 1 – VINDPM	
6	IDPM_STAT	R	N/A	IINDPM Status 0 – Not in IINDPM 1 – IINDPM	
5	IDPM_LIM[5]	R	N/A	1600mA	Input Current Limit in effect while Input Current Optimizer (ICO) is enabled Offset: 100mA (default) Range 100mA (0000000) – 3.25mA (1111111)
4	IDPM_LIM[4]	R	N/A	800mA	
3	IDPM_LIM[3]	R	N/A	400mA	
2	IDPM_LIM[2]	R	N/A	200mA	
1	IDPM_LIM[1]	R	N/A	100mA	
0	IDPM_LIM[0]	R	N/A	50mA	

8.4.21 REG14

Figure 46. REG14

7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	1
R/W	R/W	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. REG14

Bit	Field	Type	Reset	Description
7	REG_RST	R/W	N/A	Register Reset 0 – Keep current register setting (default) 1 – Reset to default register value and reset safety timer Note: Reset to 0 after register reset is completed
6	ICO_OPTIMIZED	R	N/A	Input Current Optimizer (ICO) Status 0 – Optimization is in progress 1 – Maximum Input Current Detected
5	PN[2]	R	N/A	Device Configuration 011: bq25890H
4	PN[1]	R	N/A	
3	PN[0]	R	N/A	
2	TS_PROFILE	R	N/A	Temperature Profile 1- JEITA
1	DEV_REV[1]	R	N/A	Device Revision: 11
0	DEV_REV[0]	R	N/A	

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9 Application and Implementation

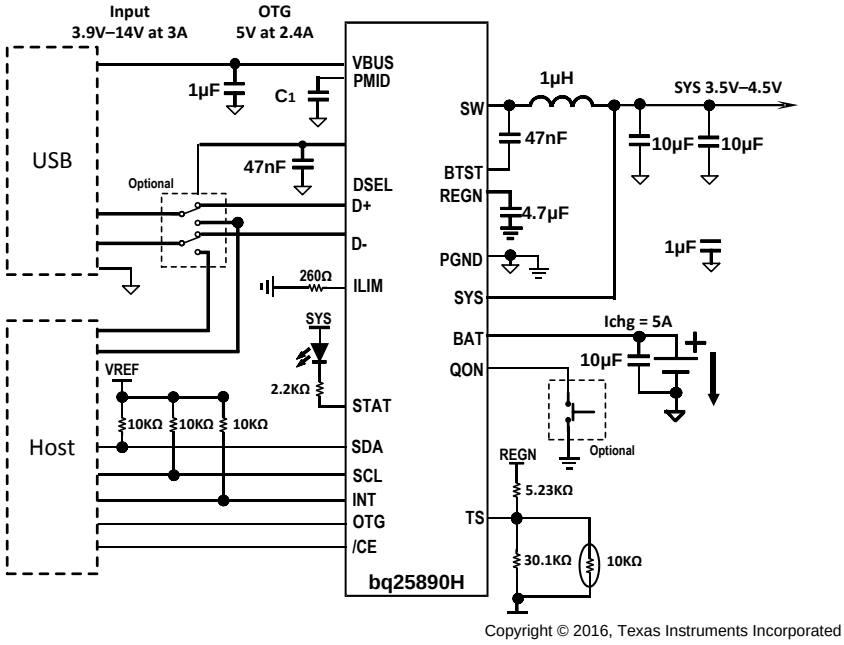
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application consists of the device configured as an I^2C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphones and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

9.2 Typical Application



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Recommended C1 = 8.2 µF (OTG ≤ 1.8 A) or 20 µF (OTG ≤ 2.4 A)

Figure 47. bq25890 with D+/D- Interface and USB On-The-Go (OTG)

9.2.1 Design Requirements

For this design example, use the parameters shown in Table 29.

Table 29. Design Parameter

PARAMETERS	VALUES
Input voltage range	3.9 V to 14 V
Input current limit	1.5 A
Fast charge current	5000 mA
Output voltage	4.352 V
V_{REF} system pullup voltage	1.8 V - 3.3 V

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The device has 1.5 MHz switching frequency to allow the use of small inductor and capacitor values. The Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{BAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (5)$$

The inductor ripple current depends on input voltage (V_{BUS}), duty cycle ($D = V_{BAT}/V_{VBUS}$), switching frequency (fs) and inductance (L):

$$I_{RIPPLE} = \frac{V_{BUS} \times D \times (1-D)}{fs \times L} \quad (6)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of (20–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

9.2.2.2 Buck Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{PMID} occurs where the duty cycle is closest to 50% and can be estimated by Equation 7:

$$I_{PMID} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (7)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25 V rating or higher capacitor is preferred for up to 14-V input voltage. 8.2-μF capacitance is suggested for typical of 3 A – 5 A charging current.

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9.2.2.3 System Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{CSYS} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (8)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{SYS}}{8 \, LC_{SYS} f s^2} \left(1 - \frac{V_{SYS}}{V_{BUS}}\right) \quad (9)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC. The charger device has internal loop compensator. To get good loop stability, 1-µH and minimum of 20-µF output capacitor is recommended. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R.

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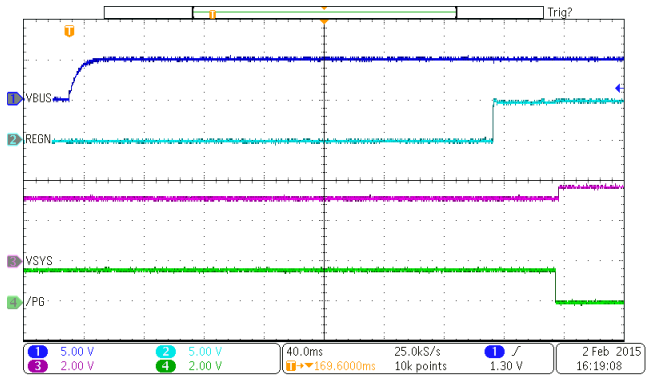
9.2.3 Application Curves



VBAT = 3.2 V

Figure 48. Power Up with Charge Disabled

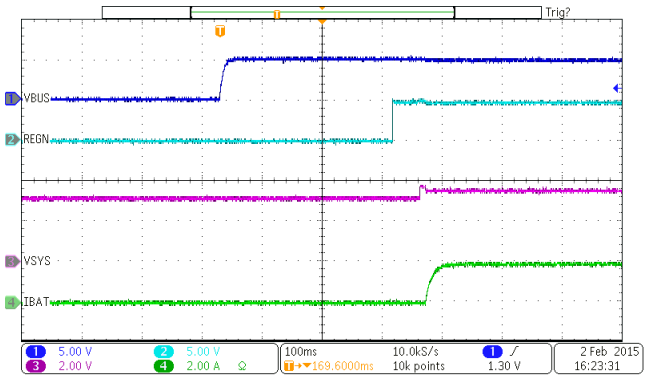
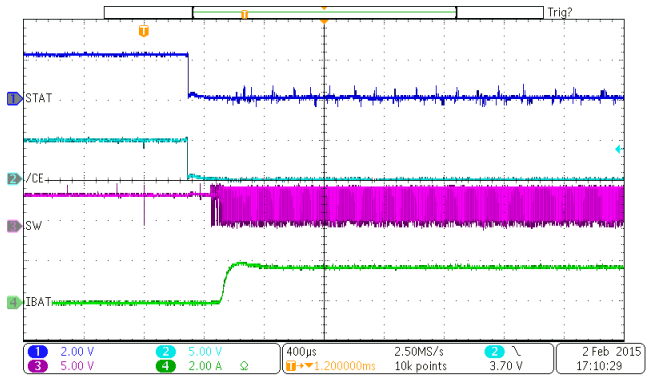
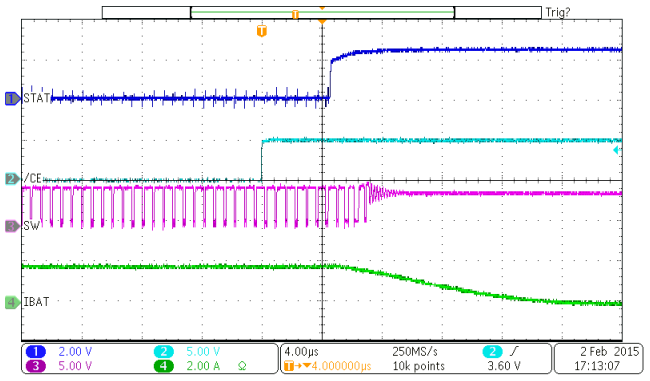


Figure 49. Power Up with Charge Enabled



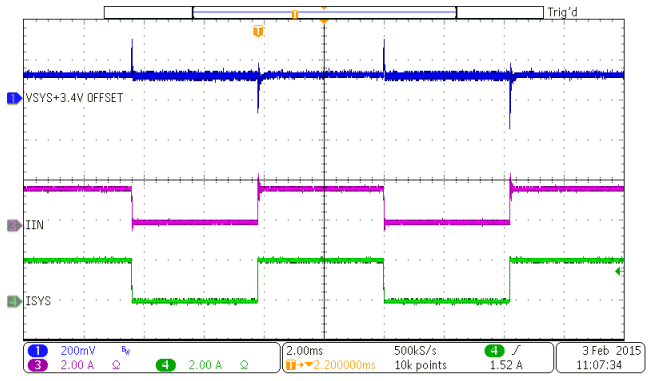
VBUS = 5 V

Figure 50. Charge Enable



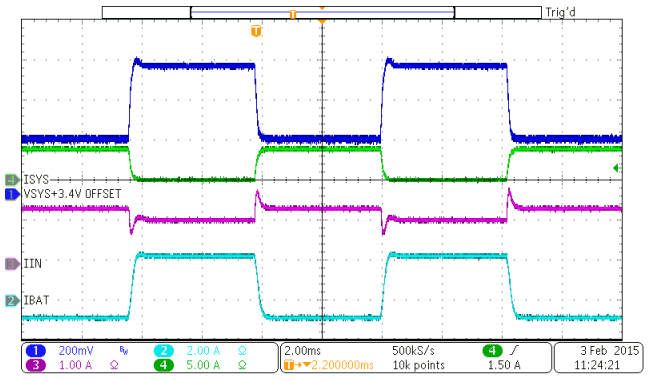
VBUS = 12 V

Figure 51. Charge Disable



VBUS = 5 V I_{IN} = 3 A Charge Disable

Figure 52. Input Current DPM Response without Battery



VBUS = 9 V I_{IN} = 1.5 A VBAT = 3.8 V
I_{CHG} = 2 A I_{SYS} = 0 A - 4 A

Figure 53. Load Transient During Supplement Mode

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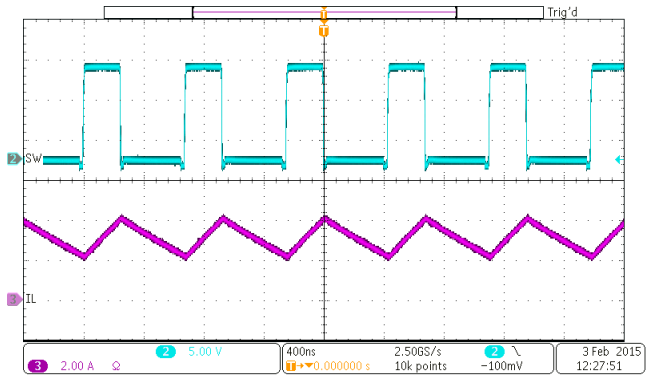
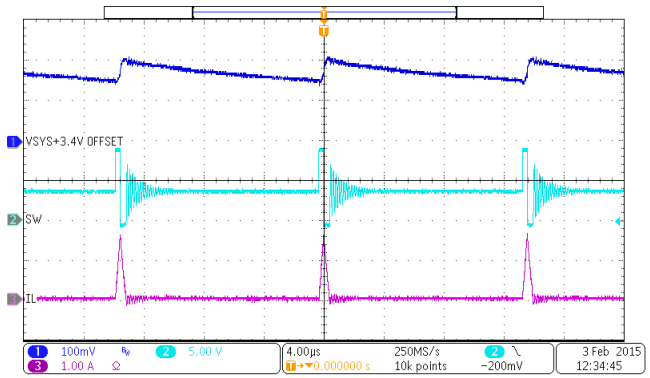


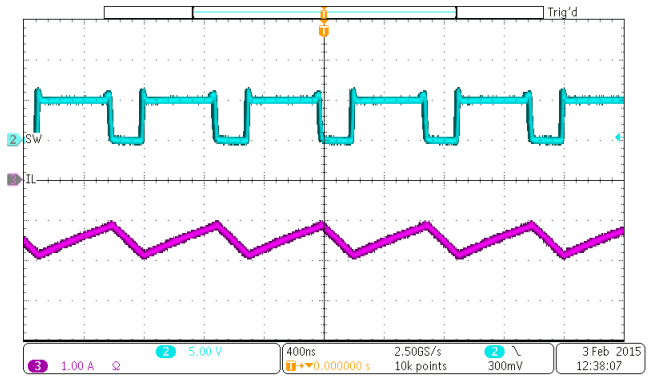
VBUS = 12 V VBAT = 3.8 V ICHG = 3 A

Figure 54. PWM Switching Waveform



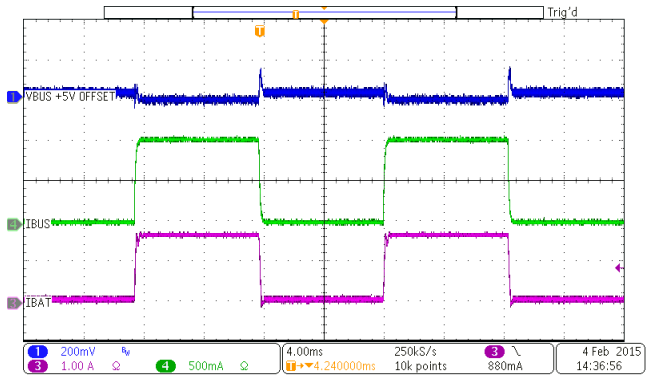
VBUS = 9V I_{SYS} = 10 mA, Charge Disable
No Battery

Figure 55. PFM Switching Waveform



VBAT = 3.8 V I_{LOAD} = 1 A

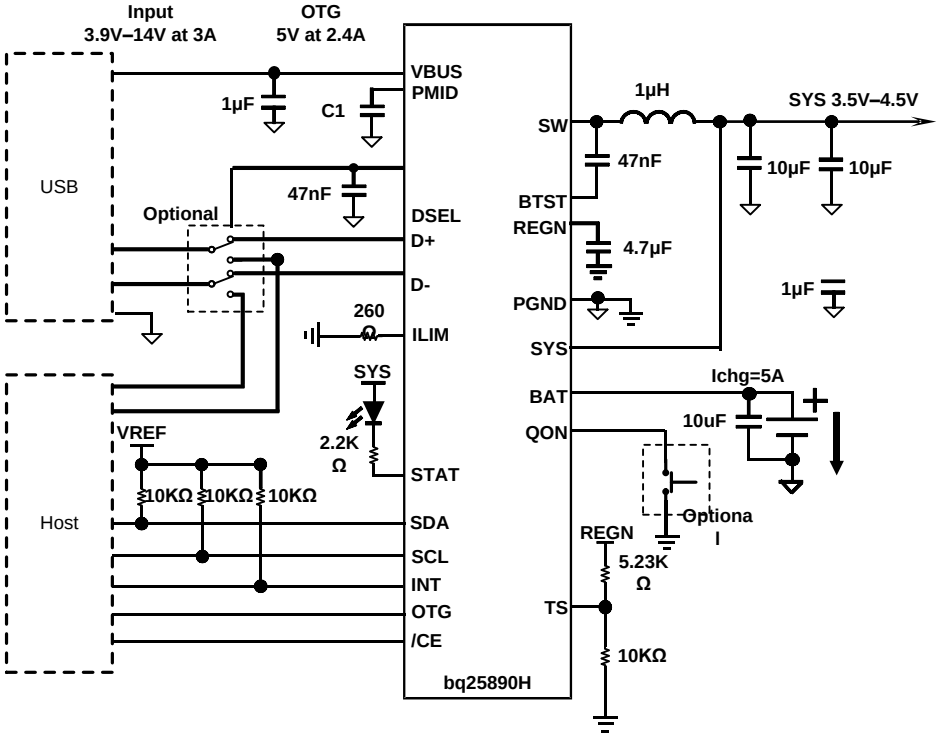
Figure 56. Boost Mode Switching Waveform



VBAT = 3.8 V I_{LOAD} = 0 A - 1 A

Figure 57. Boost Mode Load Transient

9.3 System Examples



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Recommended C1 = 8.2 µF (OTG ≤ 1.8 A) or 20 µF (OTG ≤ 2.4 A)

Figure 58. bq25890H with D+/D- Interface, USB On-The-Go (OTG) and no Thermistor Connections

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10 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9 V and 14 V input with at least 100-mA current rating connected to VBUS or a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 59) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the VQFN information, refer to SCBA017 and SLUA271.

11.2 Layout Example

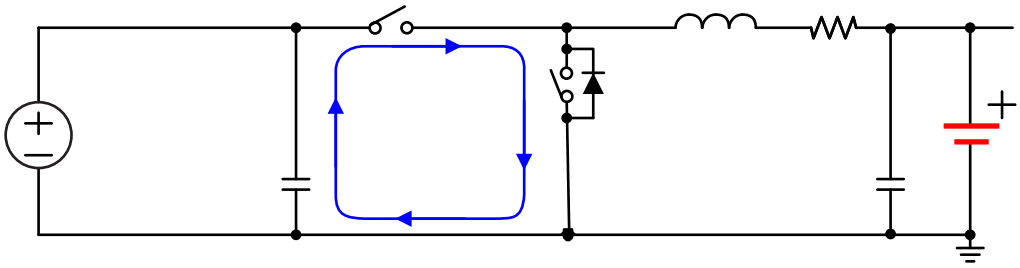

Figure 59. High Frequency Current Path

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

Quad Flatpack No-Lead Logic Packages Application Report SCBA017

QFN/SON PCB Attachment Application Report SLUA271

Semiconductor and IC Package Thermal Metrics Application Report SPRA953

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on A*lert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25890HRTWR	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 25890H
BQ25890HRTWR.A	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 25890H
BQ25890HRTWR.B	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 25890H
BQ25890HRTWT	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 25890H
BQ25890HRTWT.A	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 25890H
BQ25890HRTWT.B	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 25890H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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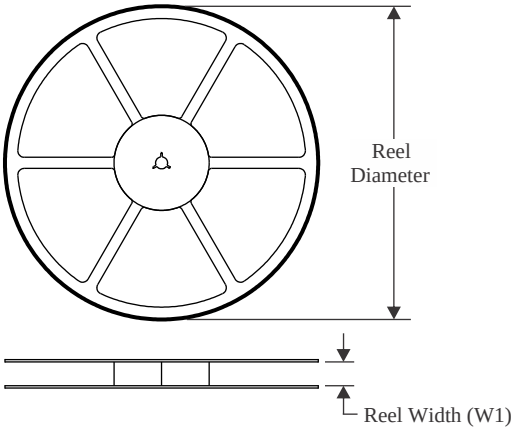
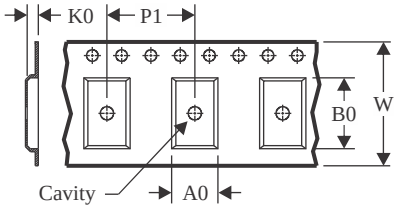
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

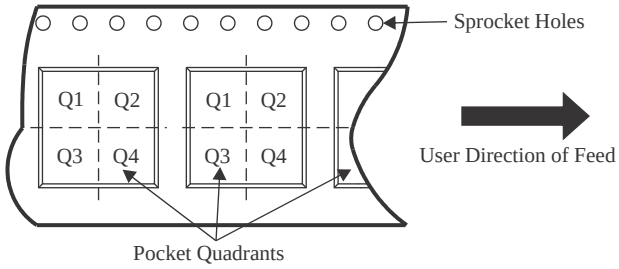


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

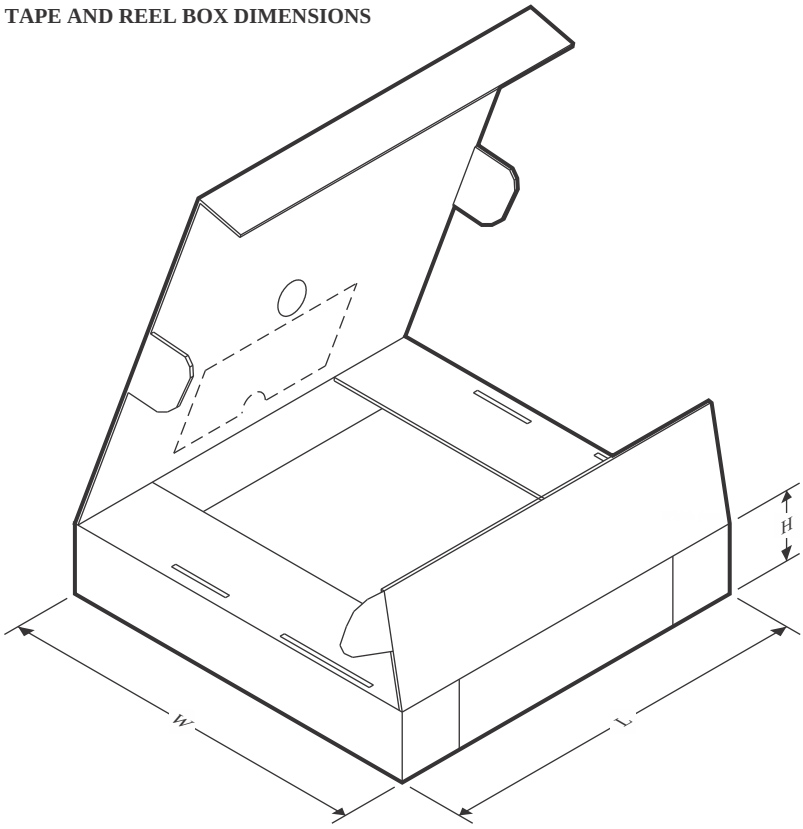
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25890HRTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25890HRTWT	WQFN	RTW	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25890HRTWR	WQFN	RTW	24	3000	346.0	346.0	33.0
BQ25890HRTWT	WQFN	RTW	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

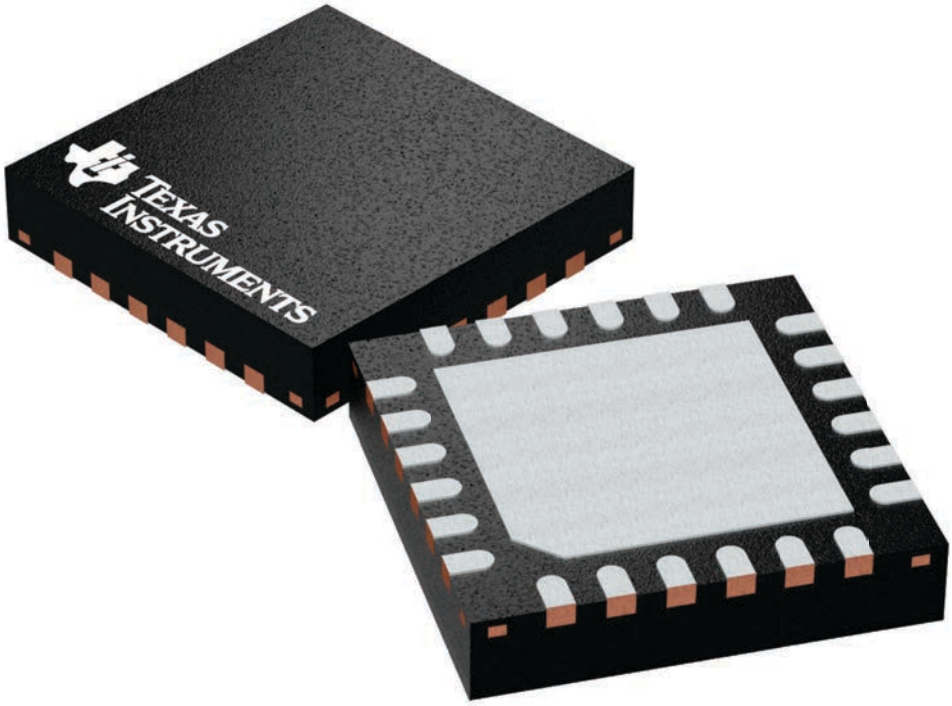
RTW 24

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

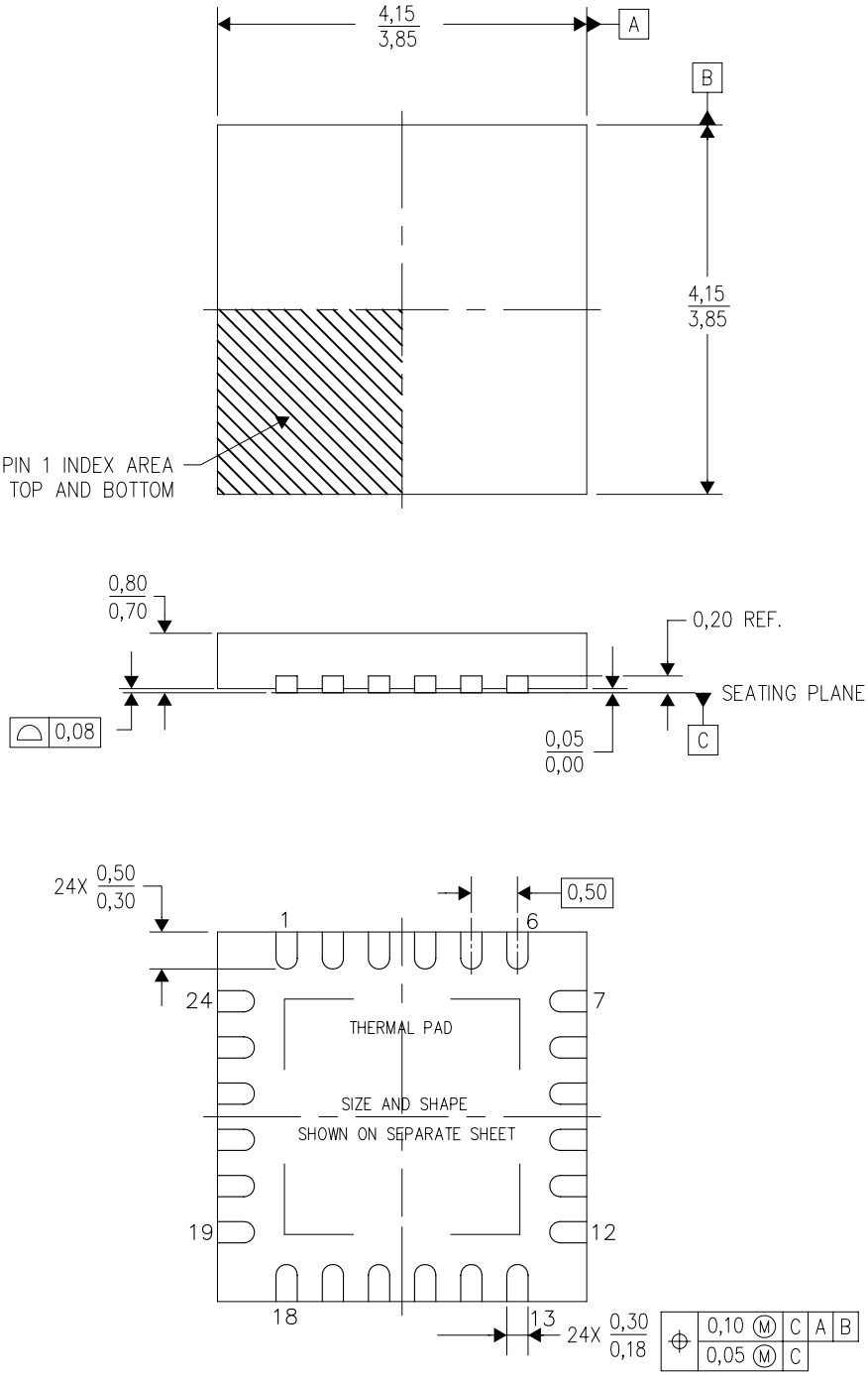
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224801/A

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

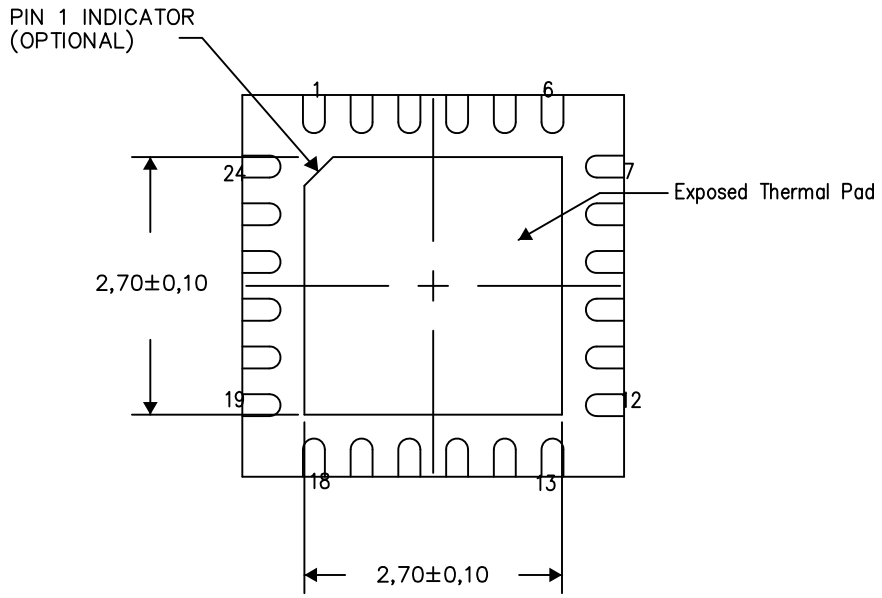
RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



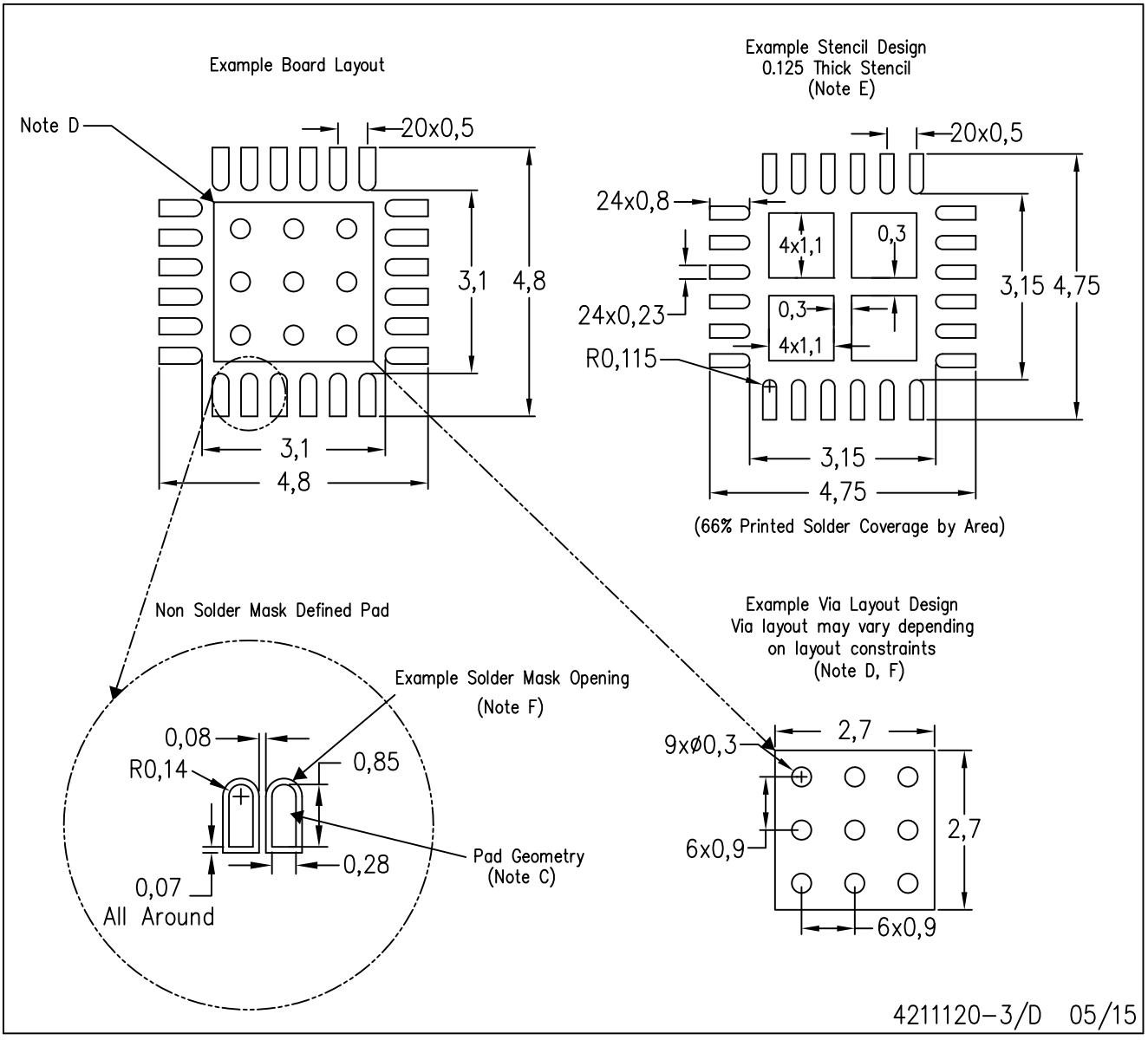
Bottom View

Exposed Thermal Pad Dimensions

4206249–5/P 05/15

NOTES: A. All linear dimensions are in millimeters

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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