LED Driver with Dynamic Headroom Control and Thermal Control Interfaces

Check for Samples: LM3464, LM3464A

FEATURES

- **Wide Input Voltage Range**
  - **12V-80V (LM3464)**
  - **12V-95V (LM3464A)**
- **Dynamic Headroom Control Ensures Maximum Efficiency**
- **4 Output Channels With Individual Current Regulation**
- **High Channel to Channel Accuracy**
- **Digital PWM/Analog Dimming Control Interface**
- **Resistor Programmable Dimming Frequency and Minimum Duty Cycle (Analog Dimming Mode)**
- **Direct Interface to Thermal Sensor**
- **Fault Detection**
- **Over Temperature Protection**
- **Thermal Shutdown**
- **Under Voltage Lockout**
- **Thermal Enhanced TSSOP-28 Package**

APPLICATIONS

- **Streetlights**
- **Solid State Lighting Solutions**

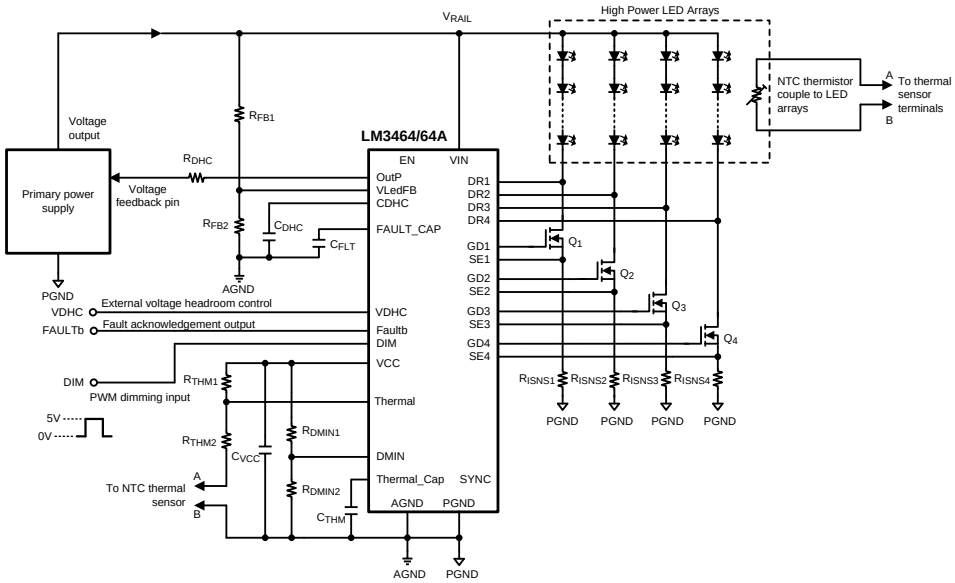
DESCRIPTION

The LM3464/64A is a 4-channel high voltage current regulator that provides a simple solution for LED lighting applications. The LM3464/64A provides four individual current regulator channels and works in conjunction with external N-channel MOSFETs and sense resistors to give accurate driving current for every LED string. Additionally, the Dynamic Headroom Control (DHC) output can be interfaced to the external power supply to adjust the LED supply voltage to the lowest level that is adequate to maintain all the string currents in regulation, yielding the optimal overall efficiency.

Digital PWM or analog voltage signals can be used to control the duty cycle of the all the channels. When analog control is used, the dimming frequency can be programmed via an external capacitor. A minimum duty cycle control is provided in the conditions that the analog dimming is configured as thermal feedback.

Protection features include VIN under-voltage lock-out, LED open/short circuit and over-temperature fault signaling to the system controller.

Typical Application



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Connection Diagram

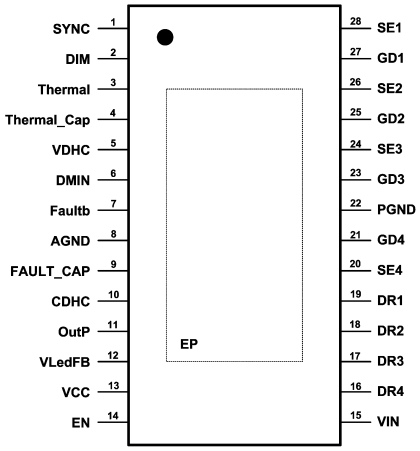

Figure 1. Top View
28-Lead TSSOP-28
Package Number PWP

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	SYNC	Synchronization signal output for cascade operation (Master-Slave configuration)	Connect this pin to the DIM pin of other LM3464/64A to enable cascade operation (multiple device). This pin should leave open for single device operation.
2	DIM	PWM dimming control	Apply logic level PWM signal to this pin controls the average brightness of the LED string. (<1.25V disable output).
3	Thermal	Thermal sensor input	Connect thermal sensor to this pin with bias accordingly to facilitate thermal foldback and control the brightness of the LED array.
4	Thermal_Cap	Thermal dimming ramp capacitor	Connect a capacitor across this pin and GND to define the thermal dimming frequency.
5	VDHC	Head room control	Apply external voltage across this pin and ground to define the minimum drain voltage. This pin is internal biased at 0.9V.
6	DMIN	Minimum thermal dimming duty control	The voltage across this pin and GND defines the minimum thermal dimming duty cycle.
7	Faultb	Fault signal output	Open Drain output, pull-down when FAULT condition occurred.
8	AGND	Signal ground	Analog ground connection for internal circuitry. Must be connected to PGND external to the package.
9	FAULT_CAP	Fault delay capacitor	Connect to an external capacitor to program the fault response time.
10	CDHC	DHC time constant capacitor	An external capacitor to ground programs the Dynamic Headroom Control loop response time
11	OutP	DHC Output	Connect this pin to the voltage feedback input of primary power supply to facilitate dynamic headroom control.
12	VLedFB	Output voltage sense input	This pin senses the output voltage of the primary power supply.
13	VCC	Internal regulator output	This pin is the output terminal of the internal voltage regulator and should be bypassed by a high quality 1uF ceramic capacitor.
14	EN	Enable input	This pin serves as device enable input when logic level signal is applied. (Active high with internal pull-up)
15	VIN	Supply voltage	The input voltage should be in the range of 12V to 80V for LM3464, 12–95V for LM3464A
16	DR4	Channel 4 drain sense input	This pin senses the drain voltage of the external MOSFET of channel 4 to facilitate DHC operation and fault detection.
17	DR3	Channel 3 drain sense input	This pin senses the drain voltage of the external MOSFET of channel 3 to facilitate DHC operation and fault detection.
18	DR2	Channel 2 drain sense input	This pin senses the drain voltage of the external MOSFET of channel 2 to facilitate DHC operation and fault detection.

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PIN DESCRIPTIONS (continued)

Pin	Name	Description	Application Information
19	DR1	Channel 1 drain sense input	This pin senses the drain voltage of the external MOSFET of channel 1 to facilitate DHC operation and fault detection.
20	SE4	Channel 4 sense input	Connect to an external sense resistor to define the Channel 4 LED current.
21	GD4	Channel 4 gate driver output	Connect to the gate of external NMOS to control the channel 4 LED current.
22	PGND	Power Ground	Ground for power circuitry. Reference point for all stated voltages. Must be externally connected to EP and AGND
23	GD3	Channel 3 gate driver output	Connect to the gate of external NMOS to control the channel 3 LED current.
24	SE3	Channel 3 sense input	Connect to an external sense resistor to define the Channel 3 LED current.
25	GD2	Channel 2 gate driver output	Connect to the gate of external NMOS to control the channel 2 LED current.
26	SE2	Channel 2 sense input	Connect to an external sense resistor to define the Channel 2 LED current.
27	GD1	Channel 1 gate driver output	Connect to the gate of external NMOS to control the channel 1 LED current.
28	SE1	Channel 1 sense input	Connect to an external sense resistor to define the Channel 1 LED current.
EP	EP	Thermal Pad (Power Ground)	Used to dissipate heat from the package during operation. Must be electrically connected to PGND external to the package.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (LM3464/LM3464A) (1)(2)

V_{IN} to GND	-0.3V to 100V
DR1, DR2, DR3, DR4 to GND	-0.3V to 100V
EN to GND	-0.3V to 5.5V
All other inputs to GND	-0.3V to 7V
ESD Rating (3), Human Body Model	±2 kV
Storage Temperature Range	−65°C to + 150°C
Junction Temperature (T_J)	+ 150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Operating Ratings (LM3464)

Supply Voltage Range (VIN)	12V to 80V
Junction Temperature Range (T_J)	−40°C to + 125°C
Thermal Resistance (θ_{JA}) (1)	33.5°C/W
Thermal Resistance (θ_{JC}) (1)	6°C/W

(1) Measurements are performed on a 4 layer JEDEC board with 10 vias provided under the exposed pad. See JESD51-1 to JESD51-11. The value of θ_{JA} is specifically dependent on the PCB trace area, trace material and the number of layers and thermal vias.

Operating Ratings (LM3464A)

Supply Voltage Range (VIN)	12V to 95V
Junction Temperature Range (T_J)	−40°C to + 125°C
Thermal Resistance (θ_{JA}) (1)	33.5°C/W
Thermal Resistance (θ_{JC}) (1)	6°C/W

(1) Measurements are performed on a 4 layer JEDEC board with 10 vias provided under the exposed pad. See JESD51-1 to JESD51-11. The value of θ_{JA} is specifically dependent on the PCB trace area, trace material and the number of layers and thermal vias.

Electrical Characteristics (LM3464/LM3464A)

Specification with standard type are for $T_A = T_J = +25°C$ only; limits in **boldface** type apply over the full Operating Junction Temperature (T_J) range. Minimum and Maximum are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = +25°C$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 48V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vcc Regulator (1)						
$V_{IN-UVLO}$	Vin under voltage lockout	V_{IN} increasing		8.5		V
$V_{IN-UVLO-HYS}$	Vin UVLO hysteresis	V_{IN} decreasing		95		mV
V_{CC}	VCC output voltage	C_{VCC} = 0.68 µF No load	**6.15**	6.3	**6.51**	V
$V_{CC-UVLO}$	VCC under-voltage lockout threshold (UVLO)	V_{CC} increasing	**4.98**		**5.28**	V
$V_{CC-UVLO-HYS}$	VCC UVLO hysteresis	V_{CC} decreasing		250		mV
I_{IN}	Quiescent Current from VIN	C_{VCC} = 0.68 µF No load	**1.65**	2.3	**3**	mA
I_{VCC}	VCC Current limit	V_{CC} = 0V	**18**			mA
Device Enable						
$V_{EN-DISABLE}$	Device disable voltage threshold	V_{EN} Decreasing	**2.1**	2.55	**3**	V

(1) V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

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Electrical Characteristics (LM3464/LM3464A) (continued)

Specification with standard type are for $T_A = T_J = +25°C$ only; limits in **boldface** type apply over the full Operating Junction Temperature (T_J) range. Minimum and Maximum are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = +25°C$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 48V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{EN-MAX}	EN pin internal pull current	$V_{EN} = 0V$	**7.2**	11	**14.7**	uA
Analog Dimming Control Interface						
$V_{CTHM-MAX}$	Sawtooth max. voltage threshold at Thermal_Cap pin 100% output duty cycle		**2.95**	3.25	**3.3**	V
$V_{CTHM-MIN}$	Sawtooth min. voltage threshold at Thermal_Cap pin 0% output duty cycle		**0.325**	0.4	**0.493**	V
I_{CTHM}	Thermal_Cap pin output current		**38.9**	50	**61**	uA
PWM Dimming Control Interface						
$V_{DIM-LED-ON}$	DIM pin voltage threshold at LED ON	$V_{DMIN} = 0V$ $V_{THERMAL} = V_{CC}$	**1.19**			V
$V_{DIM-LED-OFF}$	DIM pin voltage threshold at LED OFF	$V_{DMIN} = 0V$ $V_{THERMAL} = V_{CC}$			**1.3**	V
Dynamic Headroom Control Output						
$V_{OutP-MAX}$	OutP pin max. output voltage			V_{CC}-0.5		V
$V_{OutP-MIN}$	OutP pin min. output voltage	IoutP = 1 mA current sink		0.3		V
$V_{LEDFB-LED-ON}$	VLedFB pin voltage threshold at LED ON		**2.4**	2.5	**2.58**	V
$V_{LEDFB-SYS-RST}$	System restart VLedFB pin voltage threshold for system restart	Measure at VLedFB pin		1.2		V
LED Current Regulator						
$V_{GDx-MAX}$	GDx gate driver max. output voltage		4.73	V_{CC}–1		V
$V_{GDx-MIN}$	GDx gate driver min. output voltage			0.115	0.127	V
$I_{GDx-MAX}$	GDx gate driver short circuit current	GDx short to GND			8	mA
I_{DRx}	DRx pin input current	$V_{DRx} = 10V$		25	**29**	µA
		$V_{DRx} = 100V$		55	**70**	µA
Fault Detection and Handling						
V_{OVP-TH}	DRx Pin over-voltage protection threshold	Measure at DRx pin	**18**	19	**21**	V
$V_{SHORTFAULT}$	DRx short fault threshold	Any $V_{DRx} < 2.5V$	**8.35**	8.4	**9.75**	V
$V_{OPENFAULT}$	SEx open fault threshold	Measure at SEx pin	30			mV
$I_{FAULT-CAP}$	FAULT_CAP pin output current	All $V_{DRx} < V_{OVP-TH}$		25		uA
$I_{FAULT-CAP-OVP}$	FAULT_CAP pin output current at DRx over-voltage	Any $V_{DRx} \geq V_{OVP-TH}$		105		uA
$V_{FAULT-CAP}$	FAULT-CAP pin voltage threshold at fault timer expire	$V_{FAULT-CAP}$ rising		3.6		V
R_{Faultb}	Faultb pin to GND resistance	LED fault = TRUE		110		Ω
Thermal Protection						
T_{OTM-TH}	Over Temperature Monitor Threshold			125		°C
$T_{OTM-HYS}$	Over Temperature Monitor Hysteresis			20		°C
T_{SD}	Thermal shutdown temperature	T_J rising		165		°C
T_{SD-HYS}	Thermal shutdown temperature hysteresis	T_J falling		20		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient (2)	TSSOP-28 Package		33.5		°C/W
θ_{JC}	Junction to Case (2)			6		°C/W

(2) Measurements are performed on a 4 layer JEDEC board with 10 vias provided under the exposed pad. See JESD51-1 to JESD51-11. The value of θ_{JA} is specifically dependent on the PCB trace area, trace material and the number of layers and thermal vias.

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Typical Performance Characteristics

All curves taken at VIN = 48V with configuration in typical application for driving twelve power LEDs with four output channels active and output current per channel = 350 mA. T_A = 25°C, unless otherwise specified.

Channel 1 Current Sense Voltage (V_{SE1})

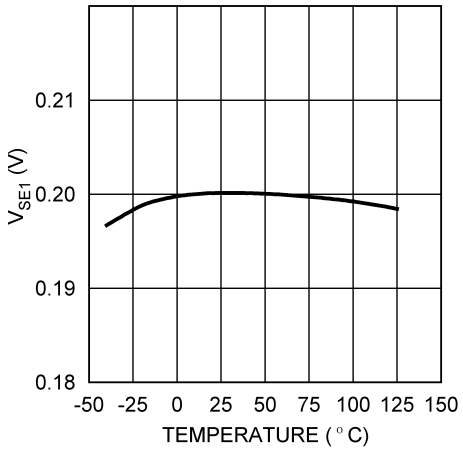

Figure 2.

Effifciency (%)

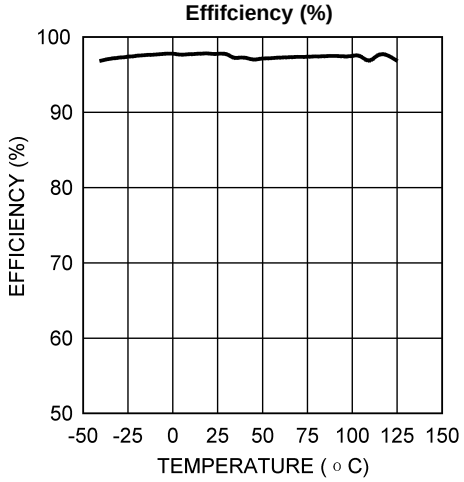

Figure 3.

Thermal_Cap Pin Output Current

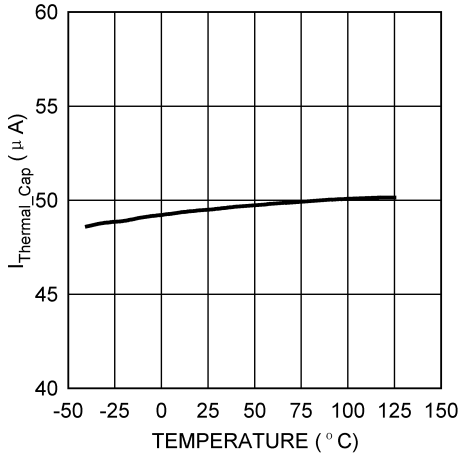

Figure 4.

VCC Variation (%)

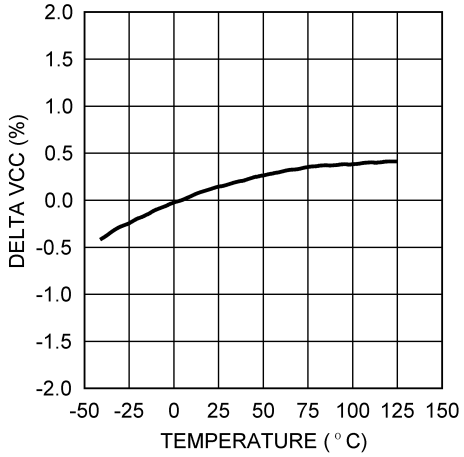

Figure 5.

Operating Current (EN pin floating)

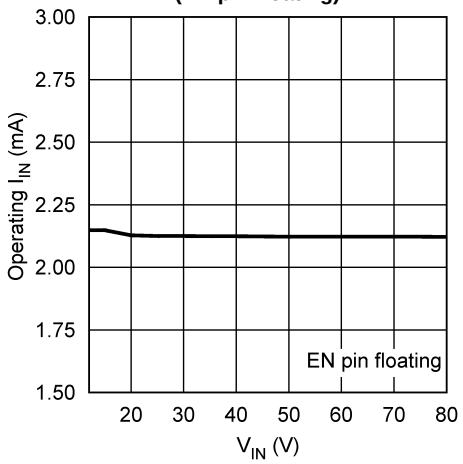

Figure 6.

Shutdown Current (EN pin = 0V)

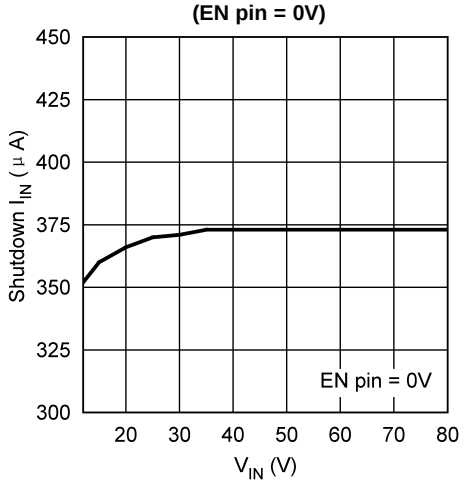

Figure 7.

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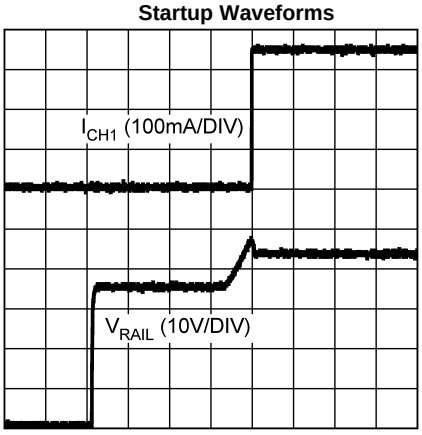
Typical Performance Characteristics (continued)

All curves taken at VIN = 48V with configuration in typical application for driving twelve power LEDs with four output channels active and output current per channel = 350 mA. T_A = 25°C, unless otherwise specified.

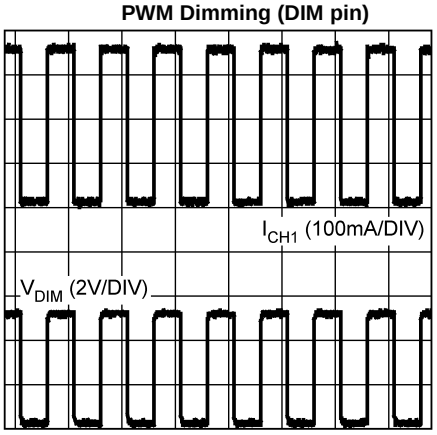
Startup Waveforms



200ms/DIV

Figure 8.

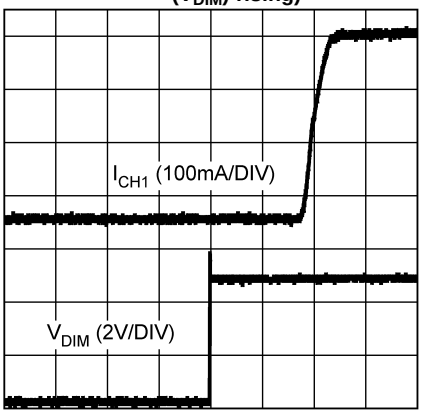
PWM Dimming (DIM pin)



4ms/DIV

Figure 9.

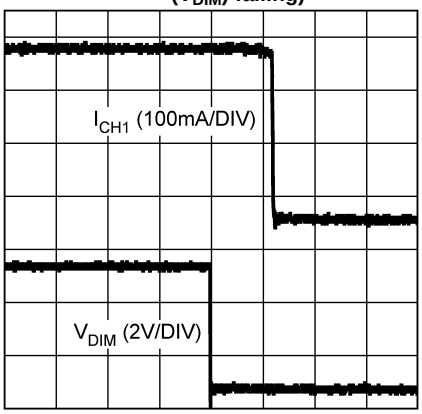
PWM Dimming Delay Time (V_{DIM}) rising)



1us/DIV

Figure 10.

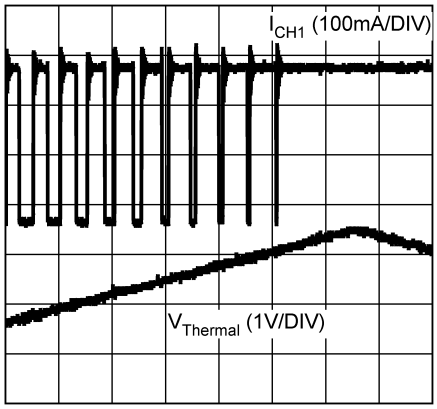
PWM Dimming Delay Time (V_{DIM}) falling)



1us/DIV

Figure 11.

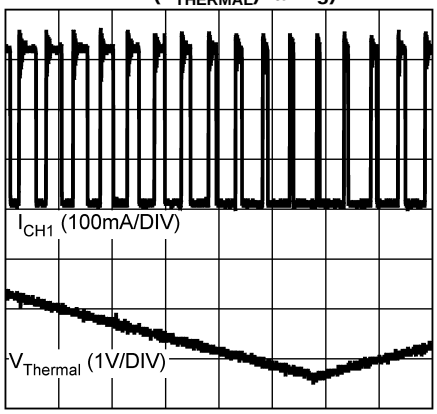
Thermal Foldback Dimming ($V_{THERMAL}$) rising)



400us/DIV

Figure 12.

Thermal Foldback Dimming ($V_{THERMAL}$) falling)



400us/DIV

Figure 13.

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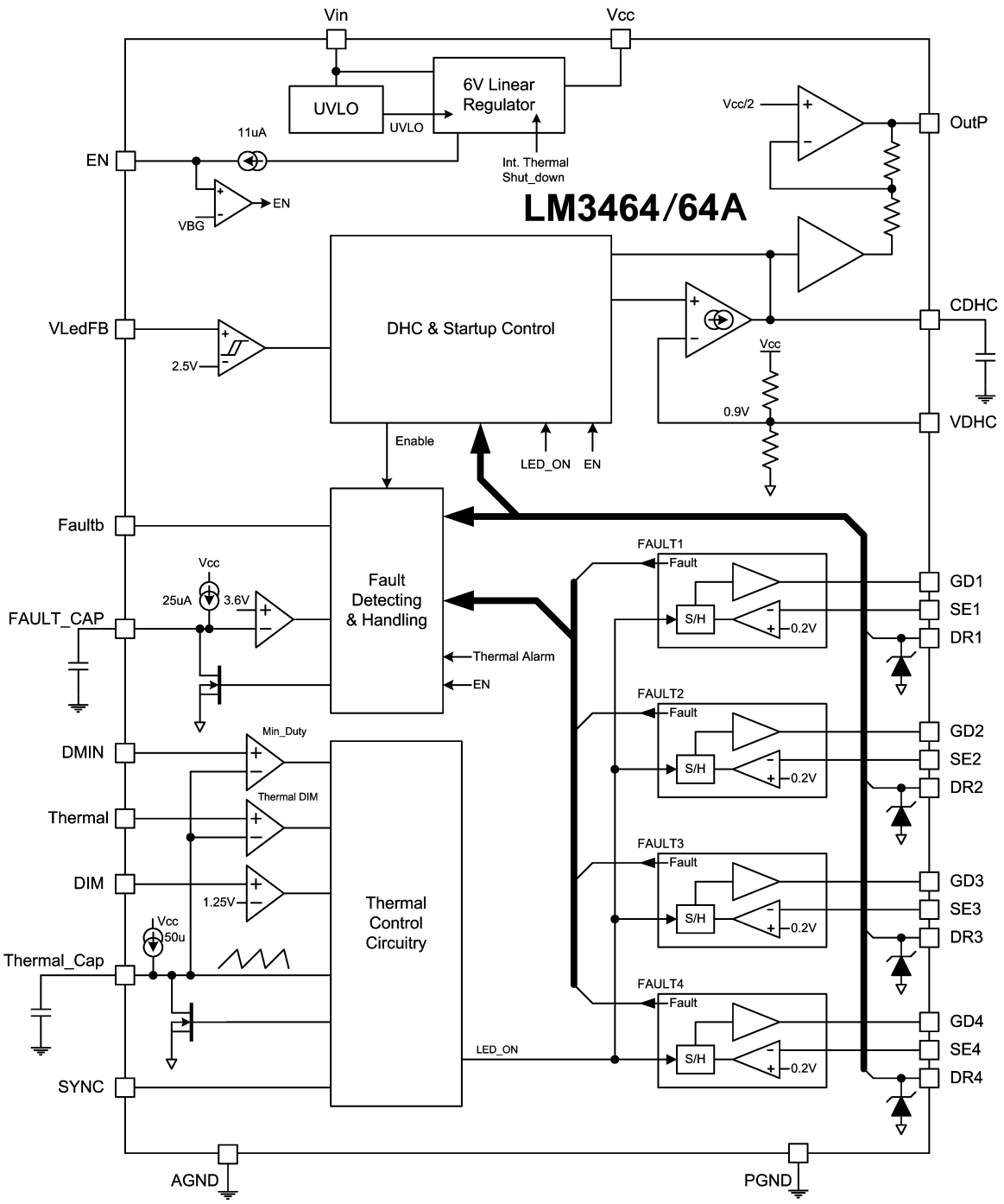
BLOCK DIAGRAM



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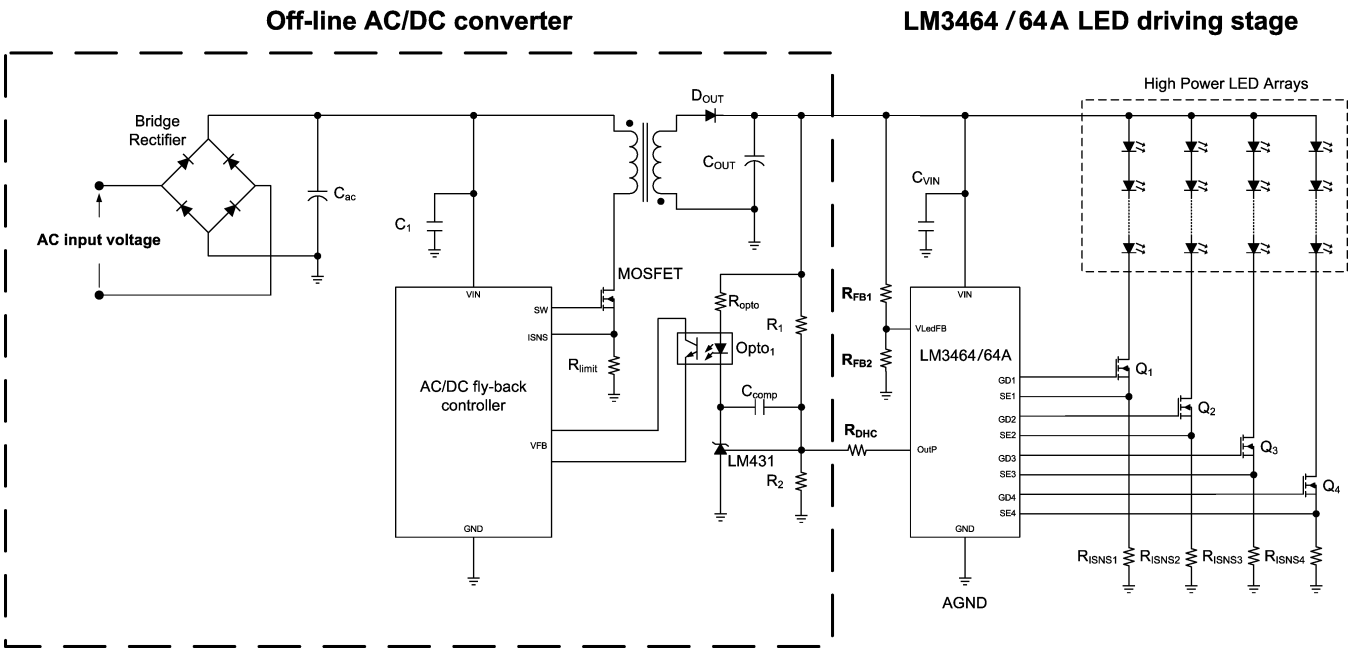

Figure 14. Typical Application Circuit with Fly-Back AC/DC Converter

OVERVIEW

The LM3464/64A is a four channel linear current regulator designed for LED lighting systems with wide input voltage range, high speed PWM and thermal foldback dimming control interface. The LM3464/64A incorporates a Dynamic Headroom Control (DHC) technology which maximizes overall efficiency of the lighting system by adjusting the output voltage of the primary power source dynamically. Linear current regulation secures high accuracy output current, LED and system reliability. High speed PWM dimming provides the flexibility of brightness control while maintaining constant color temperature of the light. The thermal foldback feature enables the LM3464/64A to manage the temperature of the LED heat sink or system chassis with a simple NTC/PTC temperature sensor. The thermal foldback input can also be used as an analog dimming control input to adapt to other sensors easily, such as ambient light sensor.

Dynamic Headroom Control (DHC)

Operation Principles of DHC

Dynamic Headroom Control is a technology that aims at maximizing the overall system efficiency by altering the supply voltage to the LED(s) dynamically in respect to the characteristics of the LED(s). In the LM3464/64A, DHC is facilitated by connecting a resistor in between the OutP pin of the LM3464/64A and the voltage feedback node of the primary power supply (AC/DC) as shown in Figure 15.

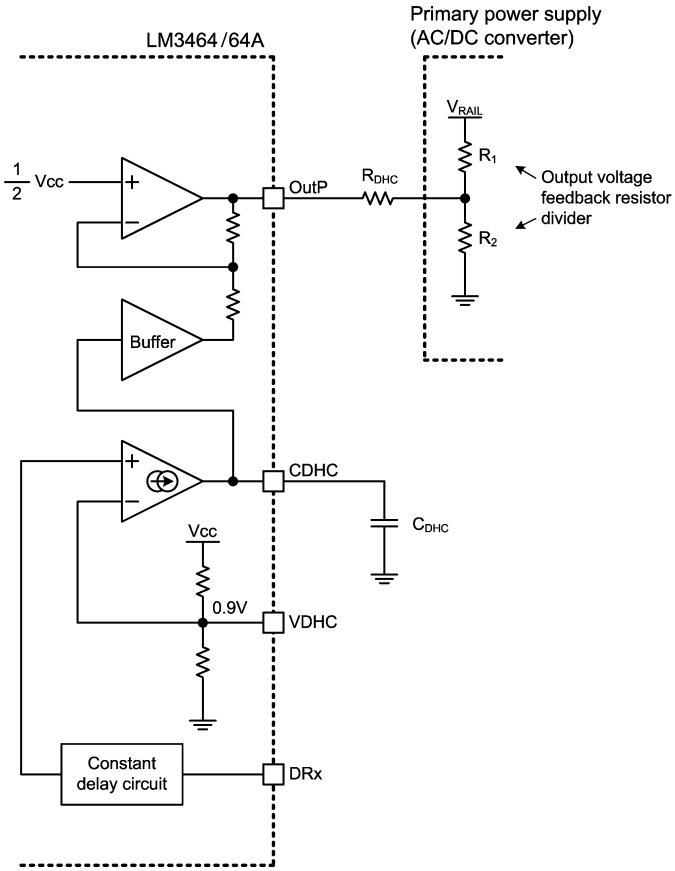

Figure 15. Circuitry of the DHC Mechanism

For example, in steady state, when all the output channels are in regulation and the forward voltage of any LED string decreases due to temperature raise, the drain voltage of the corresponding channel (DRx) increases to exceed the default 0.9V typical headroom voltage in order to maintain constant output current. As the drain voltage increases, the voltage of CDHC increases and the current sink into the OutP pin decreases. This will finally result in decrease of rail voltage (V_{RAIL}) until the corresponding DRx voltage returns to minimum level.

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System Operation

In order to provide failure protection to the LEDs, the rail voltage is pulled up by the LM3464/64A from a relatively low voltage level at system startup until the rail voltage reaches certain preset level. Figure 16 shows the change of the rail voltage of the LM3464/64A LED lighting system upon the primary power source is powered.

The Lm3464/64A can be interfaced to an off-the-shelf converter to form a LED lighting system with simple connections. Figure 14 shows the typical application circuit of a lighting system using the LM3464/64A with a fly-back AC/DC converter. In this application, the output voltage of the AC/DC converter is mainly governed by a voltage reference IC, LM431 and a voltage divider consists of R_1 and R_2. The LM3464/64A influences the output voltage of the AC/DC converter by sinking current from the junction of the voltage divider (R_1 and R_2) to realize dynamic headroom control.

The operation of the LM3464/64A upon startup can be divided into several phases according to the changes of the rail voltage as shown in Figure 16. When the AC/DC converter is powered, the rail voltage increases and stays steady when its native nominal output voltage, $V_{RAIL(nom)}$ is reached. This voltage is defined by the output voltage feedback resistor divider of the AC/DC converter. At this voltage level, the LM3464/64A is powered already. After certain delay defined by C_{DHC}, the LM3464/64A starts to push the rail voltage up by sinking current into the OutP pin from the voltage feedback node of the AC/DC converter until the rail voltage reaches V_{DHC_READY}. V_{DHC_READY} is the highest rail voltage in normal operation and should be enough to turn on all the LED strings with current regulation (defined by R_{SNSx}). As V_{RAIL} reaches V_{DHC_READY}, the LM3464/64A turns on all the output channels. This discharges the output capacitor of the primary power supply and causes the rail voltage to decrease to certain level that system efficiency is maximized (V_{LED}).

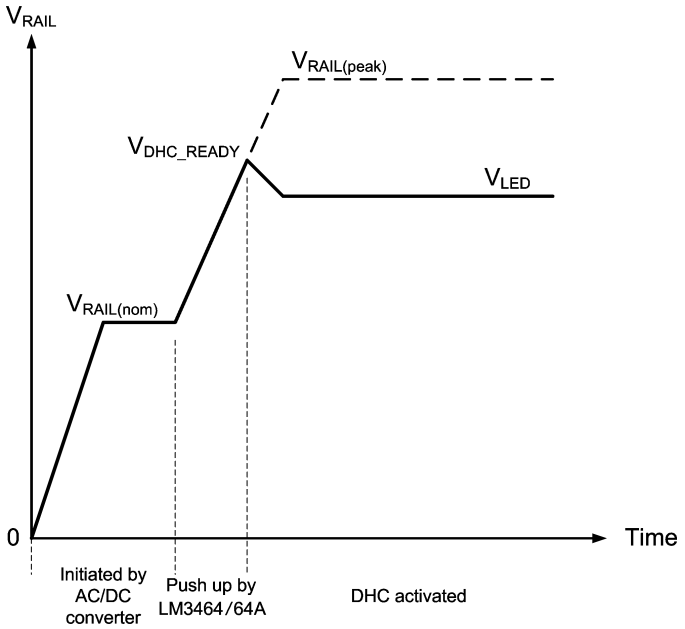

Figure 16. Changes of Rail Voltage Upon Power Up

APPLICATION INFORMATION

SETTING ($V_{RAIL(nom)}$)

The nominal rail voltage $V_{RAIL(nom)}$ is the nominal output voltage of the primary power supply (AC/DC) prior to DHC begins. The selection of $V_{RAIL(nom)}$ is primarily depend on the forward voltages of the LED arrays and should follow the equation shows below:

$$V_{RAIL(nom)} \le V_{f(all_temp)} + V_{VDHC} \quad (1)$$

In the equation, $V_{f(all_temp)}$ is the lowest forward voltage among all the LED strings under all possible temperature. And V_{VDHC} is the voltage headroom which equals to the voltage at the VDHC pin. Normally, the forward voltage of an LED drops as the ambient temperature increases. This could create large variation of total forward voltage of a LED sting under different temperature. In order to ensure proper system startup, the variation of LED forward voltage against temperature must be considered in calculations.

SETTING V_{DHC_READY} AND $V_{RAIL(peak)}$

DHC begins when the voltage at VLedFB pin reaches 2.5V, which is defined by the values of R_{FB1} and R_{FB2}:

$$2.5V = V_{DHC_READY} \times \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \quad (2)$$

Where

$$V_{DHC_READY} < V_{RAIL(peak)} \quad (3)$$

At this stage, the current of the LED strings are regulated and the rail voltage decreases in order to maintain minimum voltage drop and power dissipation on the MOSFETs.

In case the OutP pin is accidentally shorten to ground, the rail voltage will increase and end up exceeds V_{DHC_READY}. To avoid damaging the AC/DC converter, the possible peak output voltage, $V_{RAIL(peak)}$ can be roughly defined by the forward voltage of the LED strings and must set below the rated voltage of the components at the output of the AC/DC converter. In order to limit the power dissipation on the external MOSFETs, $V_{RAIL(peak)}$ is set to to no more than 10VDC higher than the forward voltage of the LED string. The following equations define the maximum output voltage of the AC/DC converter that can be pushed up by the LM3464/64A:

$$V_{RAIL(peak)} = V_{R1} + V_{REF(AC/DC)} = (R_1 \times I_{R1}) + V_{REF(AC/DC)} \quad (4)$$

for $V_{REF(AC/DC)} = 2.5V$

$$I_{R1} = \frac{V_{RAIL(peak)} - 2.5V}{R_1} \quad (5)$$

also since

$$I_{R1} = \frac{V_{REF(AC/DC)}}{R_{D2}} + \frac{V_{REF(AC/DC)} - V_{D1} - V_{outP(min)}}{R_{DHC}}$$

$$= \frac{2.5V}{R_{D2}} + \frac{2.5V - 0.5V - 0.3V}{R_{DHC}} \quad (6)$$

$$R_{DHC} = \frac{1.7V}{\left(I_{R1} - \frac{2.5V}{R_2}\right)} \quad (7)$$

As the system enters steady state, the rail voltage V_{RAIL} decreases and finally settles to an optimal level that maintains the maximum power efficiency of the system. The voltage level of V_{RAIL} under steady state can be calculated following this equation:

$$V_{RAIL} = V_{f(highest)} + V_{VDHC} \quad (8)$$

In the equation, V_{RAIL} is the rail voltage in steady state and $V_{f(highest)}$ is the total forward voltage of the LED string which carry the highest forward voltage among the LED stings.

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V_{VDHC} is the voltage at the VDHC pin. This voltage decides the headroom voltage for the LM3464/64A driver stage and equals to the minimum V_{DRx} among the drain voltages of the MOSFETs under steady state. The VDHC pin is internally biased to 0.9V which also set the default voltage headroom to 0.9V. In applications that the output of the AC/DC converter contains more than 0.9V peak-to-peak ripple voltage, the voltage headroom can be increased by applying external bias to the VDHC pin.

DEFINING VOLTAGE HEADROOM

The voltage headroom is the rail voltage margin that reserve for precision linear current regulation under steady state. Under steady state, the voltage headroom is always minimized by the LM3464/64A to reduce power losses on the MOSFETs till one of the drain voltage (V_{DRx}) of the MOSFETs equals the voltage on VDHC pin (0.9V typical).

With external bias, the voltage of the VDHC pin can be adjusted up or down to adapt to different types of primary power supply. Figure 17 shows a simple resistor based biasing circuit that derives biasing voltage from the output of the internal voltage regulator, the VCC pin.

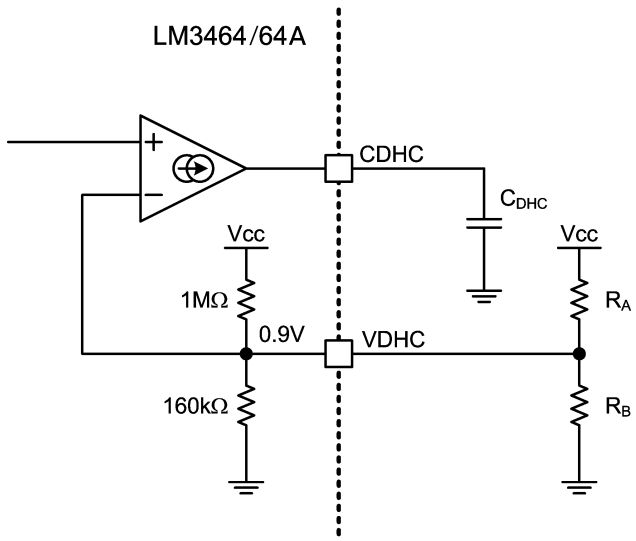

Figure 17. Adjusting Voltage Headroom with Resistors

With the additional resistors, the VDHC pin voltage is adjustable in between 0.8V and 2V. The values of R_A and R_B should be at least 10 times lower than the typical values of the internal resistor divider of the VDHC pin (see Figure 17). However, it is recommended not to set the voltage headroom too low because the ripple voltage of the primary power supply output may cause visible flicker due to insufficient voltage headroom. Thus the voltage headroom follows this equation:

$$V_{DHC} = \frac{160\ k\Omega\ //\ R_B}{160\ k\Omega\ //\ R_B + 1\ M\Omega\ //R_A} \times V_{CC}$$

where

- $0.8V < V_{VDHC} < 2V$ (9)

SETTING LED CURRENT

The LED current regulating mechanism of the LM3464/64A driver stage contains four individual LED current regulators. Every LED current regulator is composed of an external MOSFET (Q_1-Q_4), a current sensing resistor (R_{ISNS1}-R_{ISNS4}) and an amplifier inside the LM3464/64A that monitors the feedback voltage from the current sensing resistor. The integrated amplifier compares the voltage across current sensing resistors (R_{ISNS1}-R_{ISNS4}) to a 200mV typical reference voltage and controls the gate voltage of the MOSFETs (Q_1-Q_4) to realize linear current regulations. Figure 18 shows the simplified circuit of the linear LED current regulators.

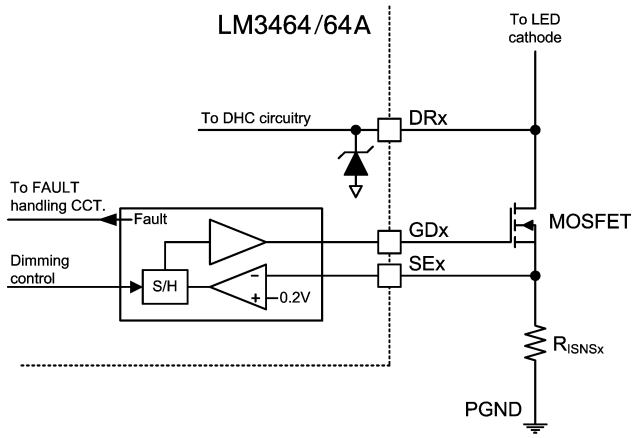

Figure 18. Linear LED Current Regulator

The driving currents of the LED strings are defined by the values of R_{ISNS1} to R_{ISNS4} individually. The LED current and the value of R_{ISNSx} are related by the following equation:

$$I_{LED} = \frac{200}{R_{ISNSx}} \text{ mA} \tag{10}$$

Since the accuracy of the LED currents are dependent on the tolerance of R_{ISNSx}, the R_{ISNSx} to recommended to be thick carbon file resistors with no more than 1% tolerance and adequate rated power to the desired LED current.

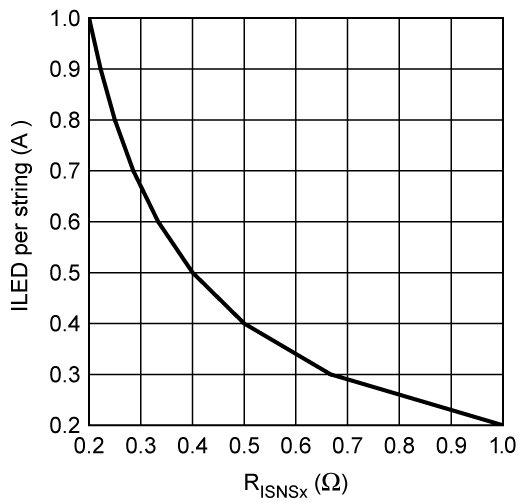

Figure 19. LED Current vs R_{ISNSx}

RESPONSE OF THE LM3464/64A DRIVER STAGE

In order to ensure good operation stability of the entire system, the response of the LM3464/64A circuitry must be set slower than the primary power supply. The response of the LM3464/64A is decided by the value of the capacitor, C_{DHC}. In general, a higher capacitance C_{DHC} will result in slower response of the LM3464/64A driver stage.

Generally, a first order integrator that consists of C_{DHC} and a transconductance amplifier with g_m = 76umho and +/– 15uA current limit as shown in Figure 20 defines the frequency response of the LM3464/64A driver stage.

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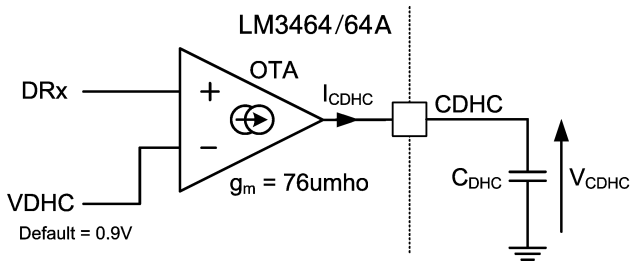

Figure 20. Simplified Circuit of the Frequency Response Setting Mechanism

The transconductance amplifier serves as a voltage to current converter that charges C_{DHC} with a current proportional to the difference in voltage between the DRx and VDHC pins.

As the voltage of the OutP pin is equal to $V_{CC} – V_{CDHC}$, the capacitance of C_{DHC}decide the rate of change of the OutP pin voltage and eventually limits the frequency response of the whole system . The higher capacitance the C_{DHC} has, the longer time the OutP pins takes for certain voltage change. Thus the value of C_{DHC} decides the response of the LM3464/64A driver stage.

If the response of the LM3464/64A driver stage is set faster than that of the primary power supply, the entire system will suffer from unstable operation. However, setting the response of the LM3464/64A driver stage unnecessarily slow will worsen transient performance of the system and false trigger the fault detection mechanism of the LM3464/64A. Practically, the minimum value of the C_{DHC} can be found out by means of 'try and error'. In most cases, a 1uF 16V ceramic capacitor is a good starting point that sets the response of the LM3464/64A driver stage slow enough for initial trial.

The value of the C_{DHC} capacitor can be reduced to speed up the response of the LM3464/64A driver stage. Otherwise, in case the system is unstable with 1uF C_{DHC}, the capacitance of the C_{DHC} capacitor should be increased until the entire system get into stable operation.

This approach is effectively setting the cut-off frequency of the LM3464/64A driver stage lower than that of the primary power supply. Usually, setting the cut-off frequencies of the two stages apart can help avoiding unstable operation. The cut-off frequency of the LM3464/64A driver stage is governed by the follow equation:

$$f_{LM3464(-3\ dB)} = \frac{1}{2\pi(1.2 \times 10^6) \times C_{DHC}} \tag{11}$$

THERMAL FOLDBACK INTERFACE

The thermal foldback function of the LM3464/64A helps in reducing the average LED currents and prolonging the LED lifetime under high temperature. By applying a DC voltage to the Thermal pin, the average output current is adjustable from 100% down to a minimum value limited by the discharge time of the C_{THM}. The Thermal pin of the LM3464/64A is an analog input for thermal foldback control that accepts a DC voltage in the range of 0V to V_{CC}. The thermal foldback control circuitry reduces the average LED currents by means of PWM dimming as shown in Figure 21:

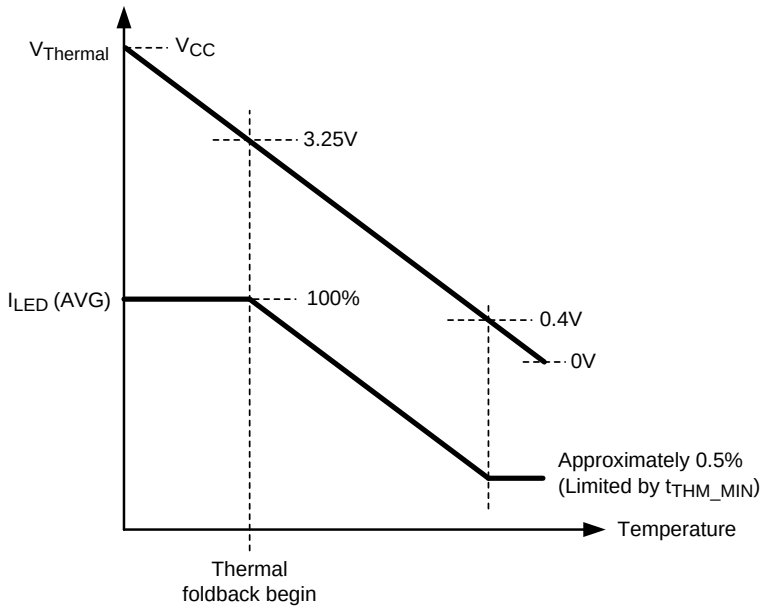

Figure 21. Average LED Current Reduces According to $V_{Thermal}$

The dimming frequency is defined by a sawtooth waveform that generated by charging and discharging the capacitor C_{THM} which connects across the Thermal_Cap pin and GND. The LM3464/64A charges the C_{THM} up to 3.25V with 50uA constant current and discharge the C_{THM} by pulling the Thermal_Cap pin to ground through a 125Ω (typ.) resistor until the pin voltage reaches 0.4V ($V_{CTHM\text{-}MIN}$). When the voltages of the Thermal and DMIN pins are both below 0.4V, the minimum dimming on time equals the discharge time of the C_{THM} following the equation:

$$t_{THM_MIN} = 262 \times C_{THM} \text{ in second} \tag{12}$$

Thus the minimum dimming duty cycle for thermal foldback that being restricted by the discharge time of C_{THM} is approximately 0.5%:

$$D_{THM_MIN} = (t_{THM_MIN} \times f_{Thermal_foldback}) \times 100\%$$

$$\text{Approximately equal to } 0.5\% \tag{13}$$

By comparing the voltage at the Thermal pin to the sawtooth voltage being generated at the Thermal_Cap pin of the LM3464/64A, a PWM dimming signal for thermal foldback is generated as shown in Figure 22:

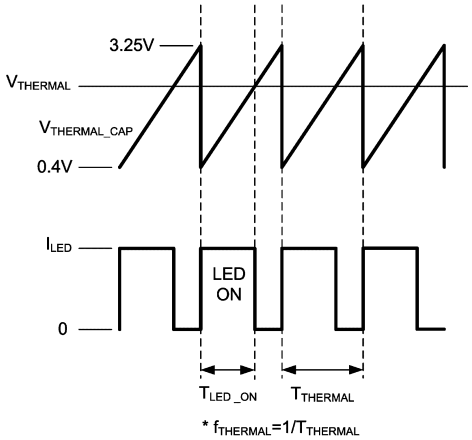

Figure 22. Signals Facilitating Thermal Foldback Control

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If the voltage at the Thermal pin is driven to exceed 3.25V, all output channels will be enabled with 100% thermal dimming duty cycle. If the Thermal pin voltage is set below 0.4V, all output channels will be disabled with 0% thermal dimming duty cycle. The dimming frequency and duty cycle with thermal foldback control are governed by the following equations:

$$\text{hermal-foldback} = \frac{50\ \mu A}{(3.25 - 0.4) \times C_{THM}} \quad (14)$$

$$D_{Thermal\text{-}foldback} = (T_{LED_ON} \times f_{Thermal\text{-}foldback}) \times 100\% \quad (15)$$

$$= [(V_{THERMAL} - 0.4) \times 35]\% \quad (16)$$

$$\text{for } 0.4 \le V_{THERMAL} \le 3.25V \quad (17)$$

SETTING MINIMUM THERMAL DIMMING DUTY CYCLE

In applications that need to ensure minimum illumines under high temperature environments, the minimum dimming duty cycle for thermal foldback may need to be limited. Such limit is defined by the voltage at the DMIN pin. When the Thermal pin voltage falls below the voltage at the DMIN pin, the thermal foldback dimming duty cycle will maintain at the level which set by the voltage of the DMIN pin (V_{DMIN}), as shown in Figure 23.

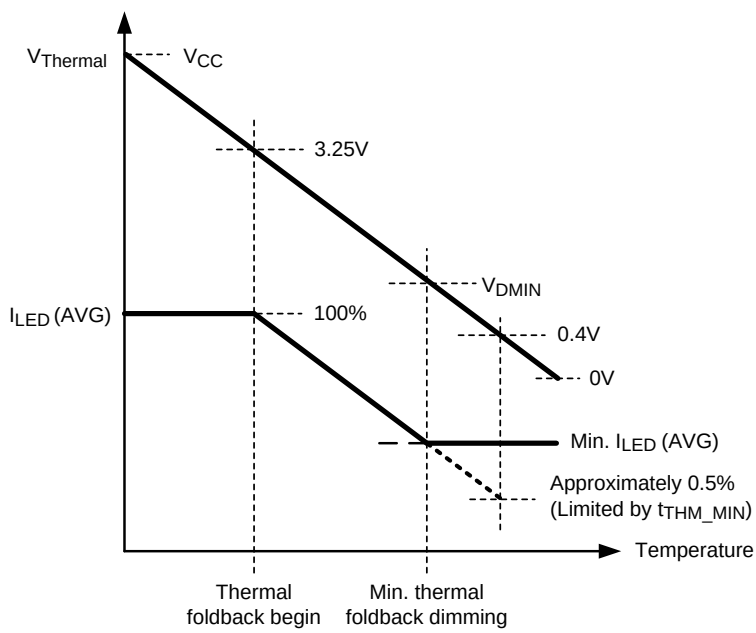

Figure 23. Thermal Foldback Control with Minimum Dimming Duty Cycle Limit

To define the minimum thermal dimming duty cycle, V_{DMIN} should be set in between 0.4V to 3.25V. The minimum duty cycle is governed by the following equation:

$$D_{MINIMUM} = [(V_{DMIN} - 0.4) \times 35]\% \quad (18)$$

$$\text{for } 0.4 \le V_{DMIN} \le 3.25V \quad (19)$$

When V_{DMIN} is below 0.4V (e.g. connect to GND), the minimum thermal dimming duty cycle limit is disabled. In applications that thermal foldback control is not required, the DMIN pin can be tied to GND to reduce power consumption.

PWM DIMMING

The LM3464/64A provides a DIM pin that accepts TTL logic level signal for PWM dimming. When the DIM pin is pulled low, all LED current regulators will turn off while maintaining V_{CC} regulator and part of the internal circuitries operating. External pull up resistor is required if the DIM pin is driven by an open collector / drain driver. PWM dimming ensures uniform color temperature of the light throughout the entire dimming range. The average current of every output channel is decided by the dimming duty cycle and follows the equation below:

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$$I_{LED(AVG)} = D_{PWM} \times I_{LED} \quad (20)$$

PWM DIMMING CONTROL WITH THERMAL FOLDBACK

The PWM dimming control can coexist with thermal foldback by applying PWM dimming control signal and thermal control signal to the DIM and Thermal pins concurrently. Normally, the dimming frequency for thermal foldback control should be much higher than the frequency of the PWM dimming control signal. Figure 24 presents the relationship among $V_{Thermal}$, $V_{Thermal_Cap}$, V_{DIM} and I_{LED}. As shown in the figure, when thermal foldback is functioning, the average output current can be further decreased linearly according to the duty cycle of the PWM dimming signal being applied to the DIM pin. In order to synchronize the dimming signals, the C_{THM} is discharged on every rising edge of the PWM dimming signal on DIM pin, notice as t_1, t_2 and t_3 in Figure 24.

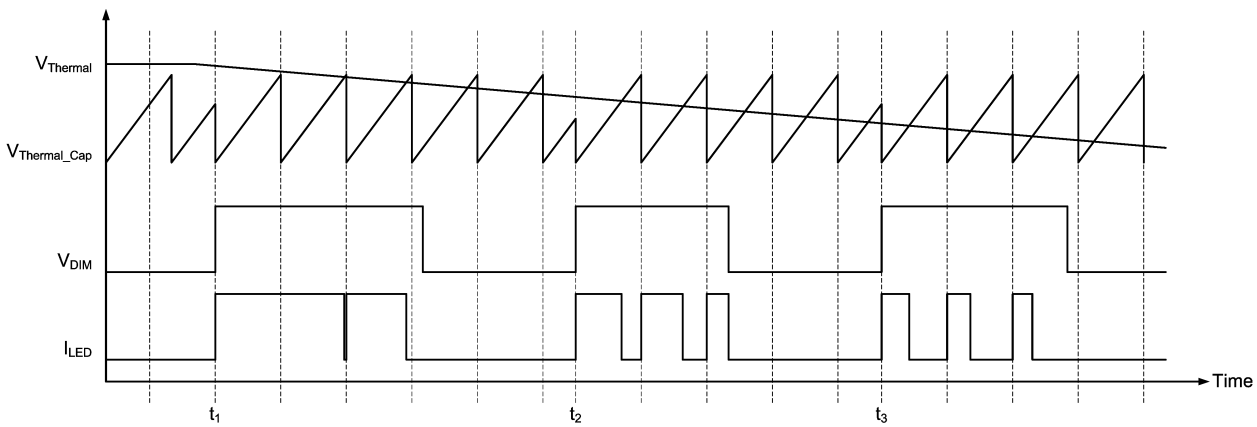

Figure 24. Thermal Foldback + PWM Dimming Control

LOW POWER STANDBY

The LM3464/64A will enter low power standby mode when the EN pin is pulled to GND. The EN pin is internally biased thus no external pull-up resistor or bias is required. Under standby mode, all the output channels are cut-off and part of the internal circuitries are disabled to maintain low power consumption. Upon the EN pin is pulled low, the OutP pin stopa sinking current from the feedback node of the primary power stage. This causes the rail voltage fall back to $V_{RAIL(nom)}$ slowly as the output capacitors of the primary power supply are being discharged by the LEDs. Pulling the EN pin low will not disable the V_{CC} regulator. When the EN pin is released (floating), the LM3464/64A exits low power standby mode and the startup sequence begins as described in Figure 16.

FAULT HANDLING and INDICATION

The LM3464/64A features a complete mechanism for fault handling and indication. The LM3464/64A detects LED failures and raises fault indication signal at the Faultb pin upon open or short circuits of LED strings, insufficient supply voltage and so on. In order to avoid false triggering the fault detection circuitry, the LM3464/64A features a timer for fault recognition. When a fault condition arises and sustains longer than the time constant preset by the capacitor , C_{FLT}, a fault is confirmed. The Faultb pin is then pulled low as an indication. The time constant for fault detection is defined by the value of the capacitor connects across the FAULT_CAP pin and GND, C_{FLT}. Normally, a 2.2 nF C_{FLT} that set a 264 us delay time is suitable for most application. For those applications with slow response primary power supply, the value of C_{FLT} may need to increase accordingly. The time delay for fault detection is governed by the following equation:

$$T_{FAULT} = \frac{C_{FLT} \times 3.0V}{25\ \mu A} \quad (21)$$

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OPEN CIRCUIT OF LED STRINGS

Detection of LED open circuit is achieved by detecting the voltages of the SEx pin and the internal gate control signal being fed to the internal MOSFET gate driver. When a LED string is open circuit, the V_{SEx} pin is pulled down to below 30mV by the current sensing resistor. As V_{SEx} falls below its regulated level, the LM3464/64A increases the gate voltage of the corresponding MOSFET (V_{GDx}) in order to maintain current regulation. Thus, the requirement for LED open circuit is V_{SEx} below 30mV and internal gate voltage reaches its maximum (at V_{GDx} about 5V). When the requirement of LED open fault is fulfilled, the LM3464/64A begins to charge up the C_{FLT}. When the voltage of the FAULT_CAP reaches 3V, and the condition of open fault retains, an open fault is confirmed.

After an open fault is confirmed, the failed channel(s) will be disabled and excluded from DHC loop. To reactivate the disabled channel(s), the EN pin can be pulled to GND for a soft reset or re-power the primary power supply for a system reset. Either reset methods results in a system restart with startup sequence shows in Figure 16.

SHORT CIRCUIT OF LED STRINGS

If any LED string experiences partially short circuit after normal system startup, the drain voltage (DRx) of the corresponding channel(s) will increase so as to maintain correct current regulation. When drain voltage increases up to 8.4V higher than the drain voltages of any other channels, the shortened channel will be latched off and excluded from the DHC loop to avoid further damages. Once a short fault is confirmed, the Faultb pin will be pulled low no matter it is due to failure of the power source or shortening of LED strings. When a short circuit of LED sting is confirmed, the failed channel(s) will be disabled and excluded from DHC loop. The disabled channels can be reactivated by either pulling the EN pin to GND or system re-powering.

DRx PIN OVER-VOLTAGE PROTECTION

The LM3464/64A features a over-voltage protection function that prevents damaging of the external MOSFETs due to short circuit of LED string(s). When the voltage of any DRx pin reaches 19V typical, the fault detection timer is triggered with the output current of the FAULT_CAP pin increases by 4 times ($I_{FAULT-CAP-OVP}$) and results in fault detection time 4 times shorter. If a over-voltage of any DRx pin is confirmed, the particular channel will be latched off and excluded from DHC loop until the EN pin is pulled low (soft reset) or system re-powering is undertaken.

DRIVING LESS THAN FOUR LED STRINGS

The LM3464/64A allows users to disable the unused output channels. Any output channel without a LED string connected or with DRx and SEx pins floating will be disabled at system startup. A disabled channel will be excluded from the DHC loop and will not contribute headroom control signal to the LM3464/64A. This function is applicable to both single LM3464/64A and cascade operation modes.

EXPANDING NUMBER OF OUTPUT CHANNEL

The LM3464/64A can be cascaded to expand the number of output channel. Bases on the master-slave architecture, one of the LM3464/64A in the system must be set to master mode and the rest must be set to slave mode. Figure 27 shows an example application circuit that provides eight output channels.

To enable cascade operation, the SYNC pin of the master LM3464/64A should connect to the DIM pin of the first slave device and similarly the SYNC pin of such slave device should connect to its down stream slave device for startup synchronization. In addition, the OutP pins of all the LM3464/64A have to tie up though a diode and resistor R_{DHC} to the voltage feedback node of the primary power supply to accomplish dynamic headroom control, as shown in Figure 27.

The slave devices can only be commanded by the master LM3464/64A. With the master and slave devices linked up, the information of startup synchronization, thermal foldback and PWM dimming controls are gathered by the master device and distribute stage by stage through the SYNC pin.

To set a LM3464/64A in master mode, the voltage of the VLedFB pin must be set below 3.25V. When the VLedFB pin is connected to VCC, the device is in slave mode. In slave mode, local thermal foldback and PWM controls are overridden by the packaged synchronization signal delivered from the master.

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CONNECTION TO LED ARRAYS

When LEDs are connected to the LM3464/64A driver stage through long cables, the parasitic components of the cable harness and external MOSFETs may resonant and eventually lead to unstable system operation. In applications that the cables between the LM3464/64A driver circuit and LED light engine are longer than 1 meter, a 4.7kΩ resistor should be added across the GDx pins to GND as shown in Figure 25.

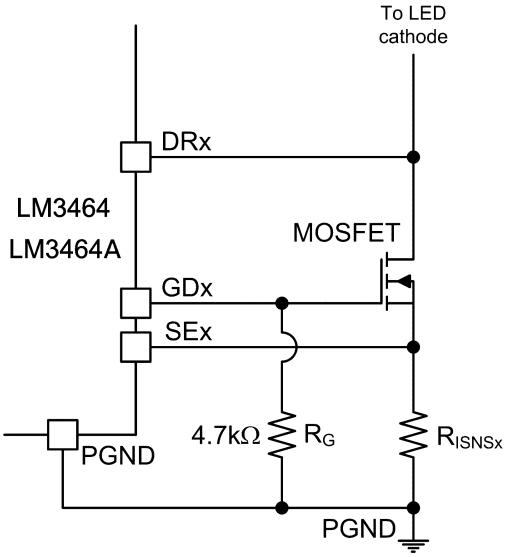

Figure 25. Additional Resistor Across GDx and SEx for Cable Harness Over 1m Long

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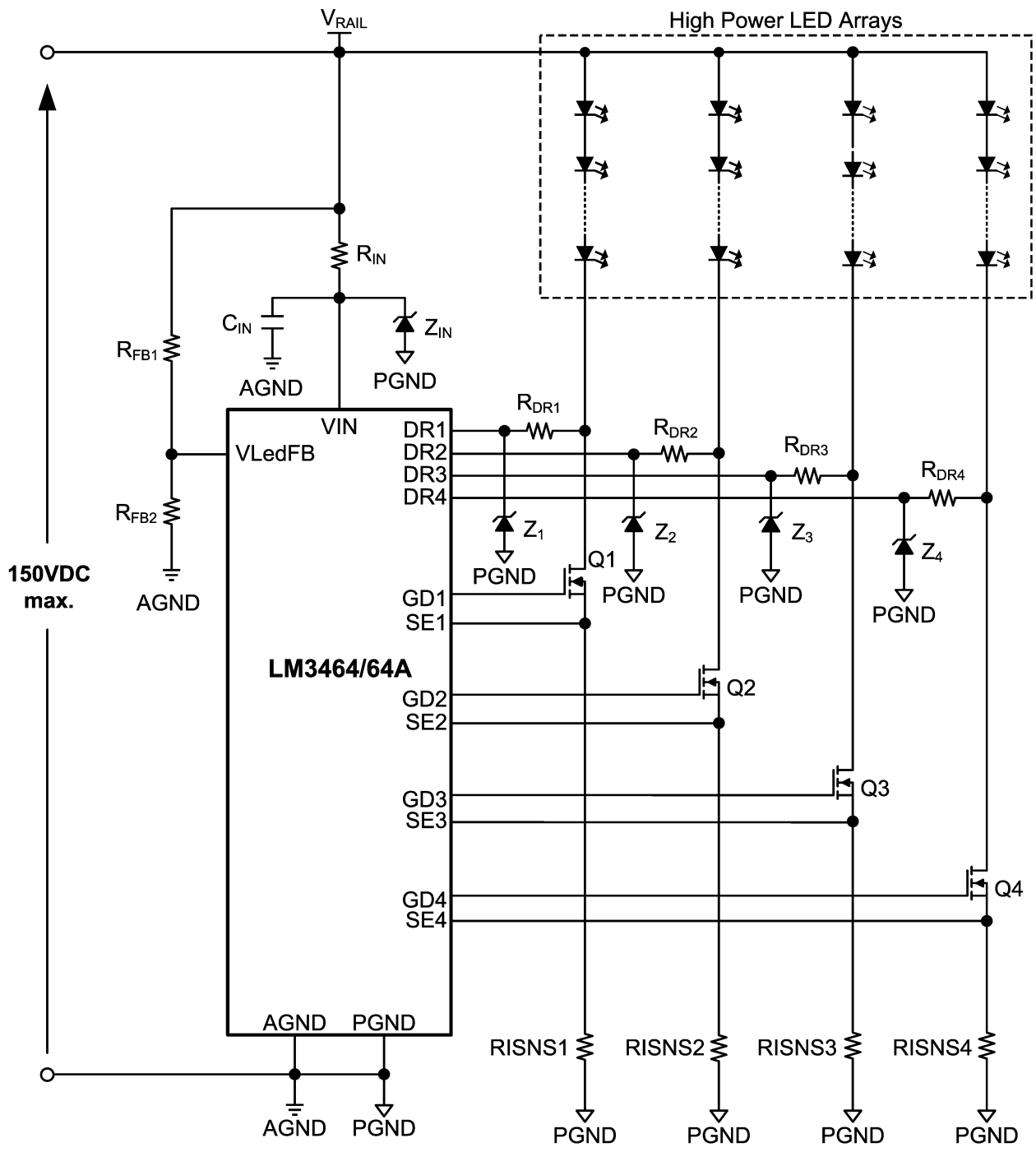

Figure 26. Additional Voltage Clamping Circuits for $V_{RAIL(peak)}$ > 80V/95V (LM3464/64A)

APPLICATIONS WITH HIGH RAIL VOLTAGE

The normal operation voltage of the LM3464 and LM3464A are rated to 80V and 95V respectively, applying voltage over the operation voltage limit to the LM3464/64A can damage the device permanently. In applications that the rail voltage is higher than the operation voltage limited of the device (80V for LM3464, 95V for LM3464A), voltage clamping circuits must be added externally to ensure the voltage limits of all the pins of the LM3464/64A are not violated. Figure 26 shows a typical application circuit with 150V peak rail voltage.

In Figure 26, Z_1, Z_2, Z_3, Z_4 and Z_{IN} are zener diodes for clamping the DRx pin voltage and input voltage (VIN pin) of the LM3464/64A. The reverse voltage of the zener diodes must be below 80V for LM3464 and 95V for LM3464A. The resistors R_{DR1}, R_{DR2}, R_{DR3}, R_{DR4} and R_{IN} are resistors for absorbing the voltage difference between the clamping voltage of the zener diodes and the rail voltage.

Calculating the Values of Z_x and R_{DRx}:

The resistance of the R_{DRx} must be properly selected according to the reverse current of the zener diode and input current of the DRx pins of the LM3464/64A to secure the allowable pin voltages are not violated. For instant, the DRx pins are required to clamp at 75V and a 500mW/75V zener diode CMHZ5267B from Central Semiconductor is used. The reverse current of the CMHZ5267B is specified 1.7mA at 75V zener voltage. The maximum allowable reverse current is 6.67mA as the power rating of the CMHZ5276B is 500mW.

Given that the input current of the DRx pins of the LM3464/64A at 100V is 63uA maximum, if the DRx pin voltage is below 100V the current flows into the DRx pin (I_{DRx}) is below 63uA. In order to reserve operation margin for component variations, I_{DRx} is assumed equal to 63uA in the following calculations.

Because $V_{RAIL(peak)}$ is the possible highest voltage at the DRx pins, the maximum resistance of R_{DRx} can be obtained following this equation:

$$R_{DRX} = \frac{V_{RAIL(peak)} - V_Z}{I_{DRX} + I_Z} \tag{22}$$

Where V_Z and I_Z are the reverse voltage and current of the zener diode Zx respectively.

For $V_{RAIL(peak)}$ = 150V, the maximum value of R_{DRx} is:

$$R_{DRX(max)} = \frac{150V - 75V}{63\mu A + 1.7mA} = 42.5k\Omega \tag{23}$$

And the minimum value of R_{DRx} is:

$$R_{DRX(min)} = \frac{150V - 75V}{63\mu A + 6.67mA} = 11.14k\Omega \tag{24}$$

Thus, the value of R_{DRx} must be selected in the range:

$$11.14k\Omega \le R_{DRX} \le 42.5k\Omega \tag{25}$$

To minimize power dissipation on the zener diodes, a standard 42.2kΩ resistor can be used for the R_{DRx}. Because the resistors, R_{DRx} are used to absorb the power being introduced by the voltage difference between V_{RAIL} and V_{Zx}, the maximum power dissipation on every R_{DRx} equals to:

$$P_{RDRX(max)} = \frac{(V_{RAIL(peak)} - V_Z)^2}{R_{DRX}} = \frac{(150V - 75V)^2}{42.2k\Omega} = 133mW \tag{26}$$

Thus, a standard 42.2kΩ resistor with 0.25W power rating (1206 package) and 1% tolerance can be used.

Calculating the Values of Z_{IN} and R_{IN}:

Similar to the requirements of selecting the Zx and R_{DRx}, the voltage at the VIN pin of the LM3464/64A is clamped to 75V by a voltage clamping circuit consists of Z_{IN} and R_{IN}. Because the maximum operating and shut-down current (V_{EN} < 2.1V) are 3mA and 700uA respectively, in order to ensure the voltage of the VIN pin is clamped close to 75V even when the LM3464/64A is disabled, a 1.5W/75V zener diode CMZ5946B from Central Semiconductor is used to ensure adequate conduction current for Z_{IN}. The reverse current of the CMZ5946B is specified 5mA at 75V, so the allowable current flows through Z_{IN} is in between 5mA to 20mA.

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The value of R_{IN} is governed by the following equations:

$$R_{IN} = \frac{V_{RAIL(peak)} - V_{ZIN}}{I_{IN} + I_{ZIN}} \tag{27}$$

Maximum value of R_{IN}:

$$R_{IN(max)} = \frac{150V - 75V}{3mA + 5mA} = 9.375k\Omega \tag{28}$$

Minimum value of R_{IN}:

$$R_{IN(min)} = \frac{150V - 75V}{3mA + 20mA} = 3.26k\Omega \tag{29}$$

So the value of R_{IN} must be in the range:

$$3.26k\Omega \le R_{DRX} \le 9.38k\Omega \tag{30}$$

To minimize power dissipations on both the Z_{IN} and R_{IN}, a standard 9.31kΩ resistor can be selected for the R_{IN}. Then the maximum power dissipation on R_{IN} is:

$$P_{RIN(max)} = \frac{(V_{RAIL(peak)} - V_{ZIN})^2}{R_{IN}} = \frac{(150V - 75)^2}{9.38k\Omega} = 600mW \tag{31}$$

Thus, a standard 9.38kΩ resistor with 2512 package (1W) and 1% tolerance can be used.

Additional Application Circuit

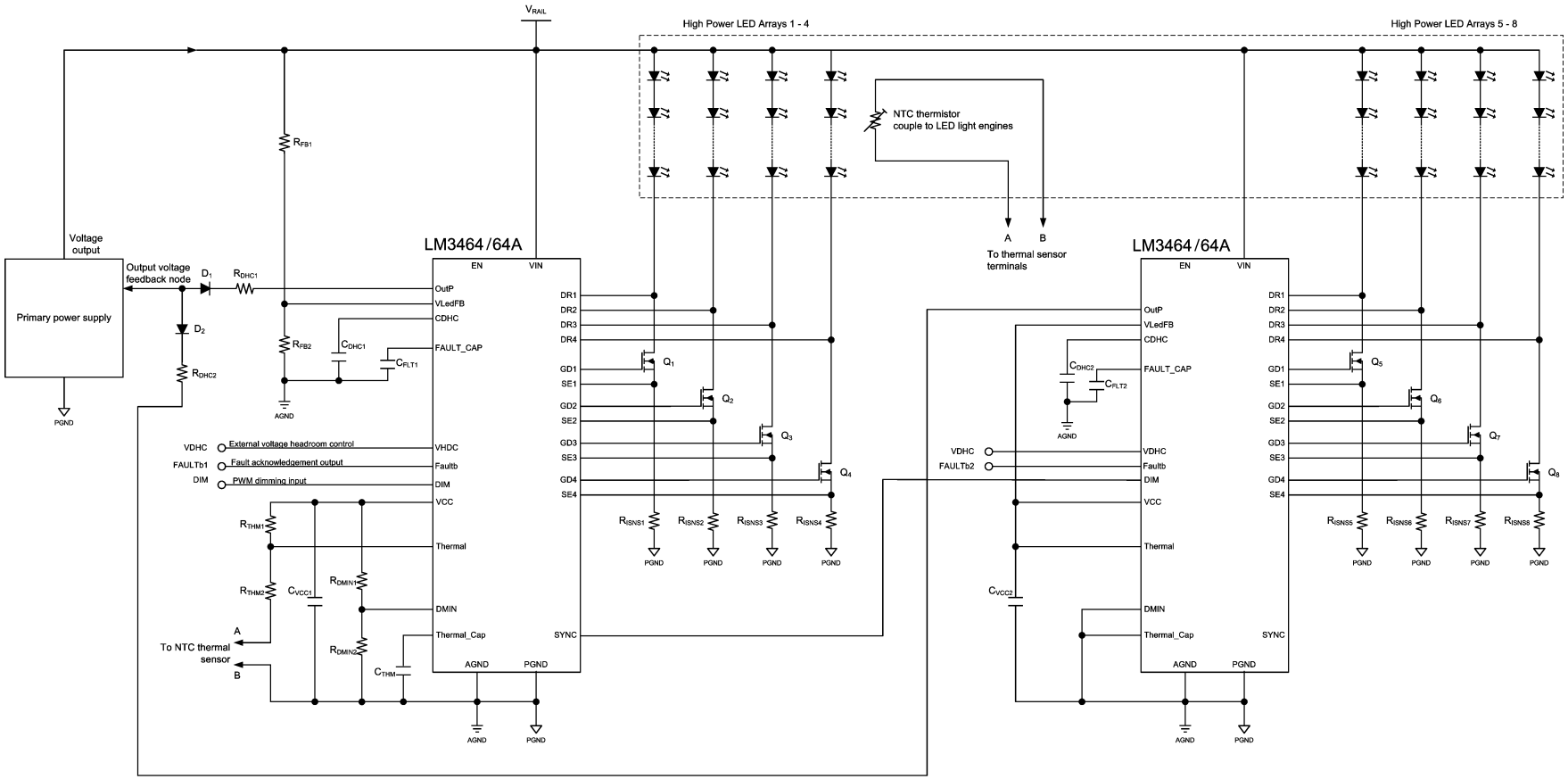

Figure 27. Cascade Operation with Thermal Foldback Control

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REVISION HISTORY

Changes from Revision E (May 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	24

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3464AMH/NOPB	Active	Production	HTSSOP (PWP) | 28	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3464AMH
LM3464AMH/NOPB.A	Active	Production	HTSSOP (PWP) | 28	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3464AMH
LM3464AMHX/NOPB	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3464AMH
LM3464AMHX/NOPB.A	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3464AMH
LM3464MH/NOPB	Active	Production	HTSSOP (PWP) | 28	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3464MH
LM3464MH/NOPB.A	Active	Production	HTSSOP (PWP) | 28	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3464MH
LM3464MHX/NOPB	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3464MH
LM3464MHX/NOPB.A	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3464MH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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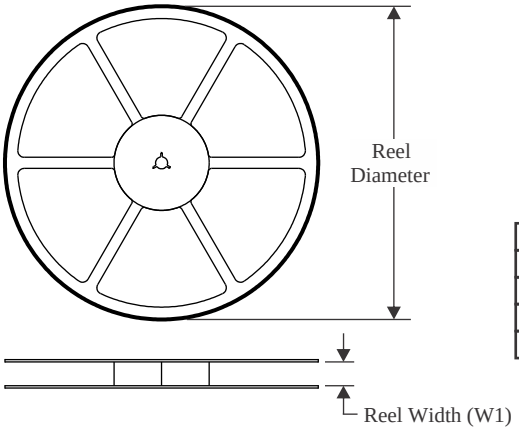
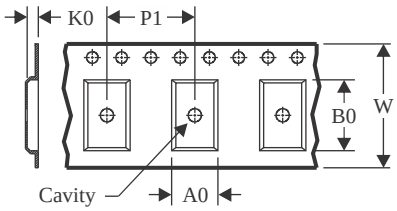
TAPE AND REEL INFORMATION

REEL DIMENSIONS

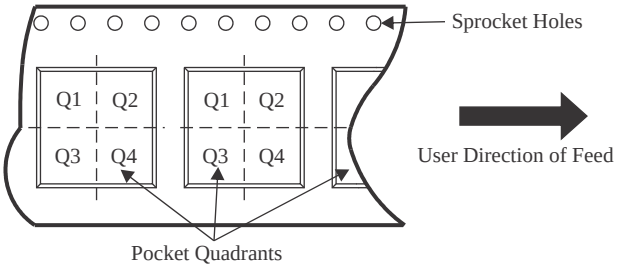


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

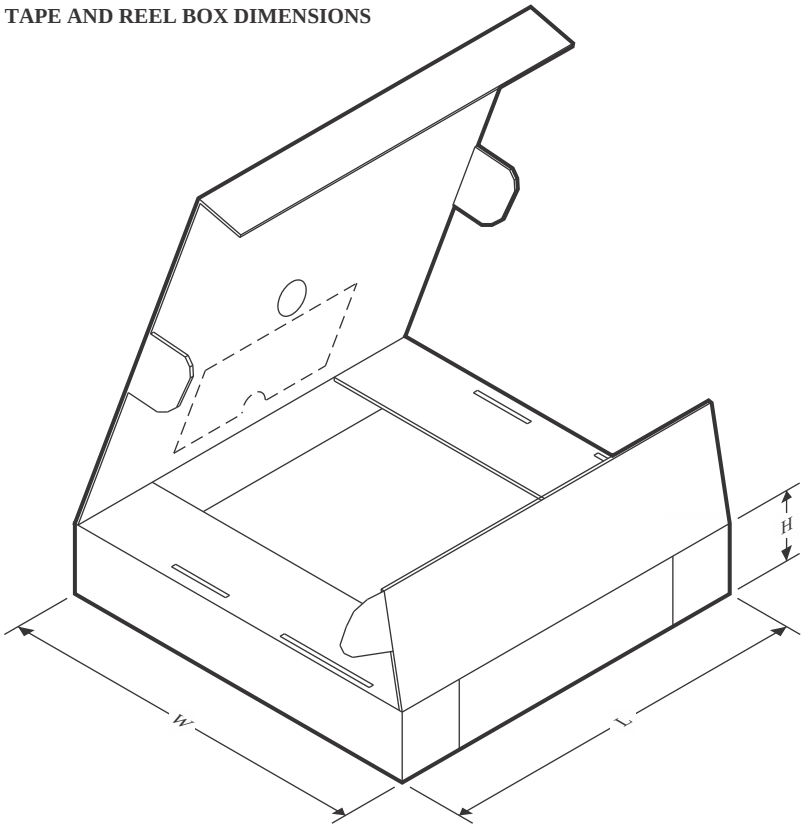
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3464AMHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.95	10.0	1.7	8.0	16.0	Q1
LM3464MHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.95	10.0	1.7	8.0	16.0	Q1

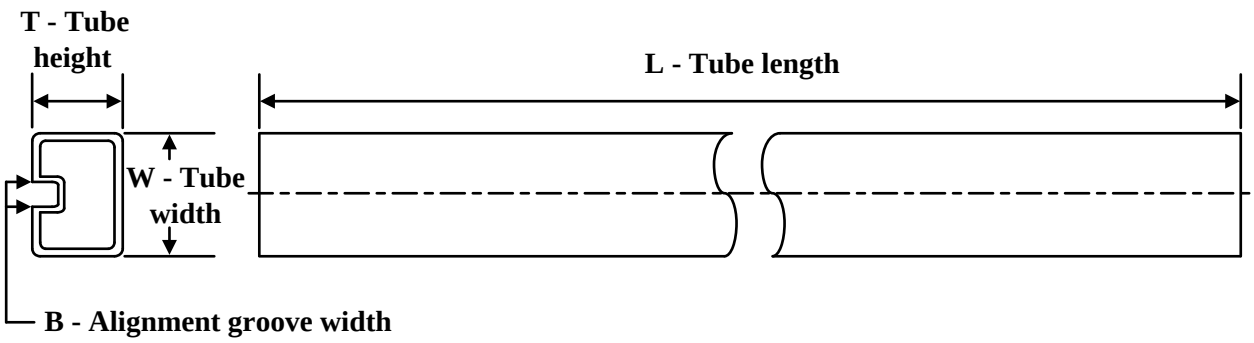
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

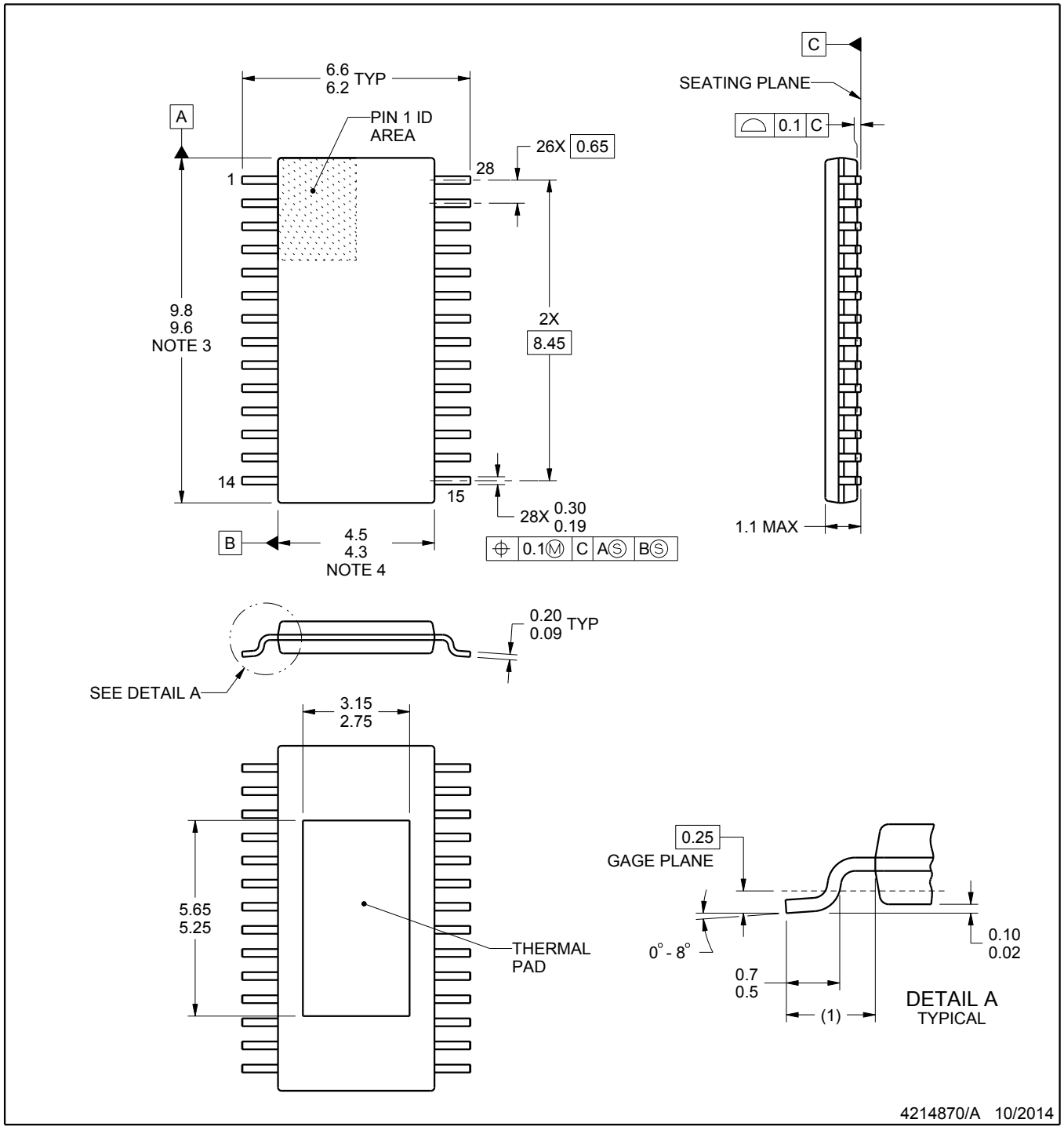
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3464AMHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	35.0
LM3464MHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

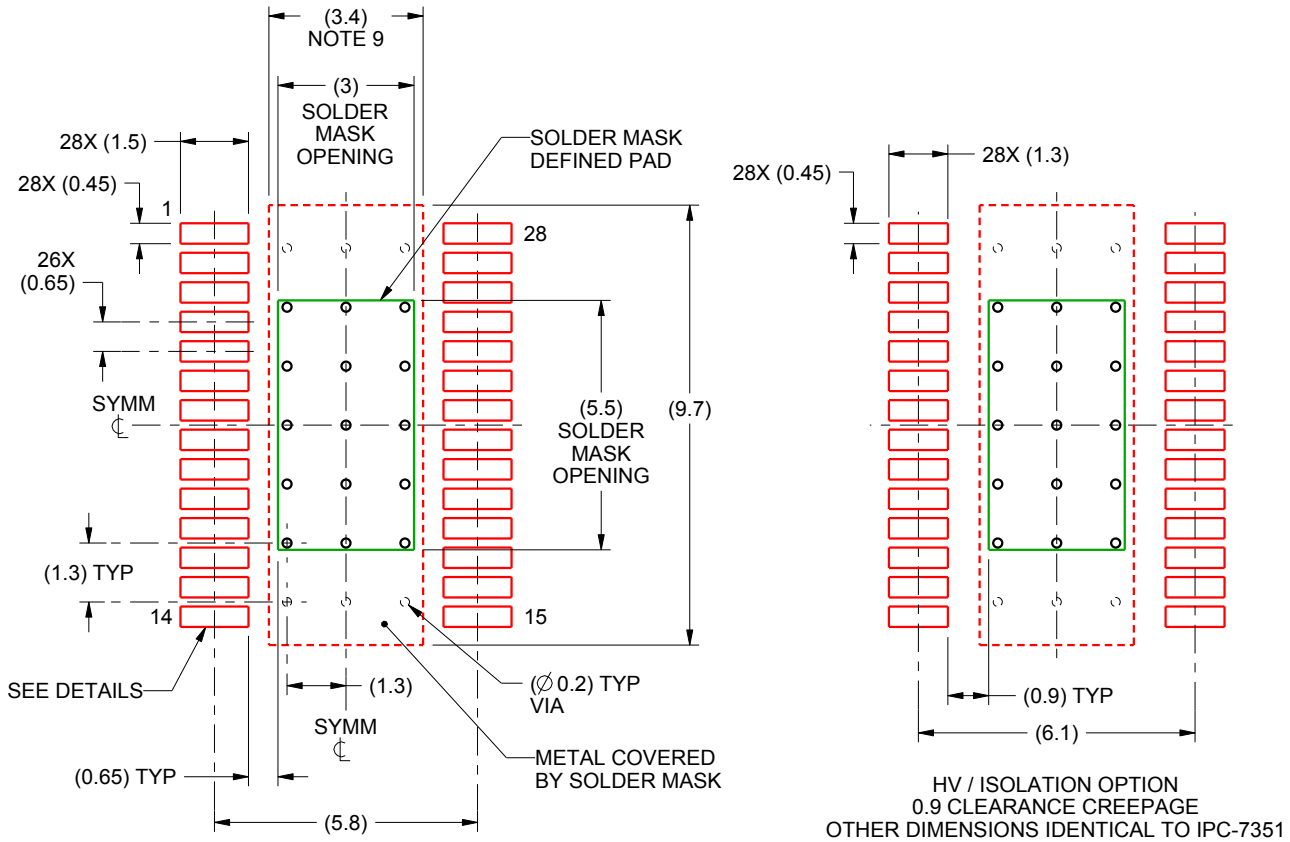
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM3464AMH/NOPB	PWP	HTSSOP	28	48	495	8	2514.6	4.06
LM3464AMH/NOPB.A	PWP	HTSSOP	28	48	495	8	2514.6	4.06
LM3464MH/NOPB	PWP	HTSSOP	28	48	495	8	2514.6	4.06
LM3464MH/NOPB.A	PWP	HTSSOP	28	48	495	8	2514.6	4.06



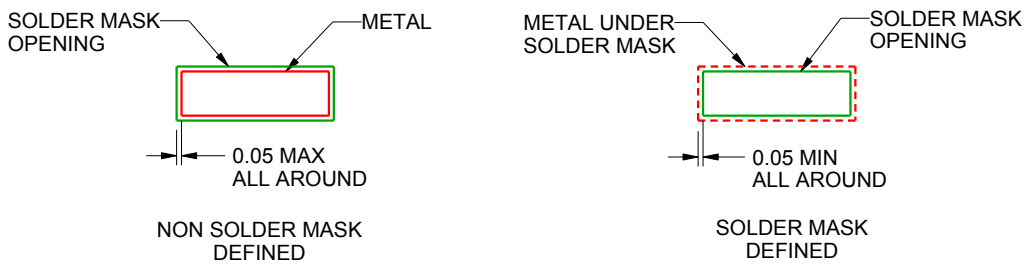
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-153, variation AET.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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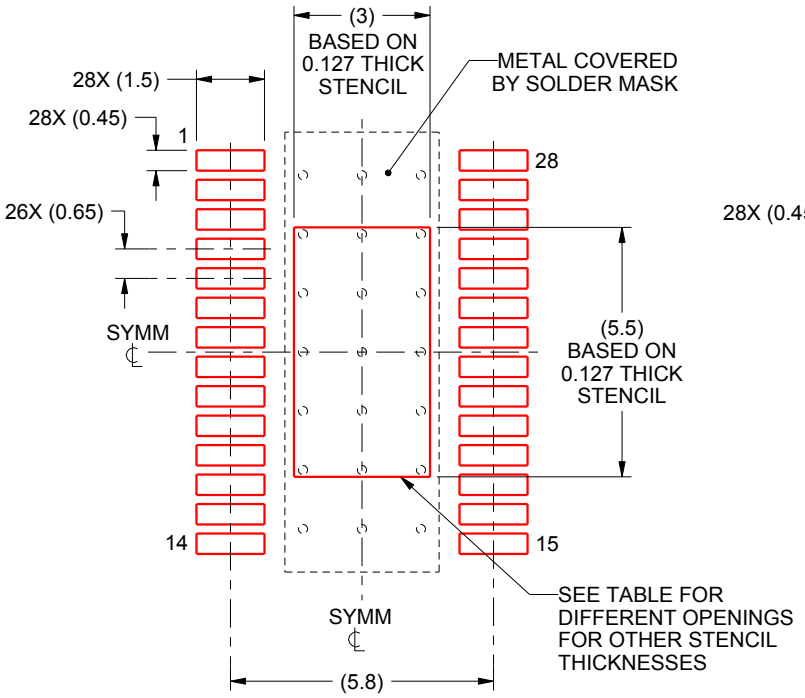
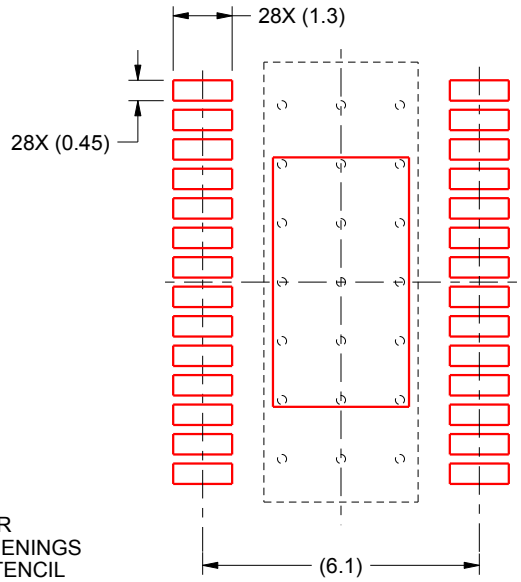
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE



HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.55 X 6.37
0.127	3.0 X 5.5 (SHOWN)
0.152	2.88 X 5.16
0.178	2.66 X 4.77

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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