

Fast-Charge ICs

Features

- Fast charge and conditioning of nickel cadmium or nickel-metal hydride batteries
- Hysteretic PWM switch-mode current regulation or gated control of an external regulator
- Easily integrated into systems or used as a stand-alone charger
- Pre-charge qualification of temperature and voltage
- Configurable, direct LED outputs display battery and charge status
- Fast-charge termination by Δ temperature/ Δ time, peak voltage detection, $-\Delta V$, maximum voltage, maximum temperature, and maximum time
- Optional top-off charge and pulsed current maintenance charging
- Logic-level controlled low-power mode ($< 5\mu A$ standby current)

General Description

The bq2004E and bq2004H Fast Charge ICs provide comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device.

Integration of closed-loop current control circuitry allows the bq2004 to be the basis of a cost-effective solution for stand-alone and system-integrated chargers for batteries of one or more cells.

Switch-activated discharge-before-charge allows bq2004E/H-based chargers to support battery conditioning and capacity determination.

High-efficiency power conversion is accomplished using the bq2004E/H as a hysteretic PWM controller for switch-mode regulation of the charging current. The bq2004E/H may alternatively be used to gate an externally regulated charging current.

Fast charge may begin on application of the charging supply, replacement of the battery, or switch depression. For safety, fast charge is inhibited unless/until the battery tempera-

ture and voltage are within configured limits.

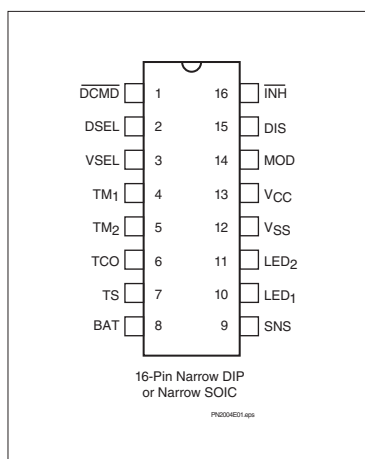
Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Rate of temperature rise ($\Delta T/\Delta t$)
- Peak voltage detection (PVD)
- Negative delta voltage ($-\Delta V$)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, optional top-off and pulsed current maintenance phases with appropriate display mode selections are available.

The bq2004H differs from the bq2004E only in that fast charge, hold-off, and top-off time units have been scaled up by a factor of two, and the bq2004H provides different display selections. Timing differences between the two ICs are illustrated in Table 1. Display differences are shown in Table 2.

Pin Connections



SLUS081A - APRIL 2005

Pin Names

DCMD	Discharge command	SNS	Sense resistor input
DSEL	Display select	LED ₁	Charge status output 1
VSEL	Voltage termination select	LED ₂	Charge status output 2
TM ₁	Timer mode select 1	V _{SS}	System ground
TM ₂	Timer mode select 2	V _{CC}	5.0V $\pm$ 10% power
TCO	Temperature cutoff	MOD	Charge current control
TS	Temperature sense	DIS	Discharge control output
BAT	Battery voltage	INH	Charge inhibit input

bq2004E/H

Pin Descriptions

DCMD	Discharge-before-charge control input The $\overline{\text{DCMD}}$ input controls the conditions that enable discharge-before-charge. DCMD is pulled up internally. A negative-going pulse on DCMD initiates a discharge to end-of-discharge voltage (EDV) on the BAT pin, followed by a new charge cycle start. Tying $\overline{\text{DCMD}}$ to ground enables automatic discharge-before-charge on every new charge cycle start.
DSEL	Display select input This three-state input configures the charge status display mode of the LED ₁ and LED ₂ outputs and can be used to disable top-off and pulsed-trickle. See Table 2.
VSEL	Voltage termination select input This three-state input controls the voltage-termination technique used by the bq2004E/H. When high, PVD is active. When floating, $-\Delta V$ is used. When pulled low, both PVD and $-\Delta V$ are disabled.
TM₁– TM₂	Timer mode inputs TM ₁ and TM ₂ are three-state inputs that configure the fast charge safety timer, voltage termination hold-off time, “top-off”, and trickle charge control. See Table 1.
TCO	Temperature cut-off threshold input Input to set maximum allowable battery temperature. If the potential between TS and SNS is less than the voltage at the TCO input, then fast charge or top-off charge is terminated.
TS	Temperature sense input Input, referenced to SNS, for an external thermister monitoring battery temperature.
BAT	Battery voltage input BAT is the battery voltage sense input, referenced to SNS. This is created by a high-impedance resistor-divider network connected between the positive and the negative terminals of the battery.

SNS

Charging current sense input

SNS controls the switching of MOD based on an external sense resistor in the current path of the battery. SNS is the reference potential for both the TS and BAT pins. If SNS is connected to V_{SS}, then MOD switches high at the beginning of charge and low at the end of charge.

**LED₁–
LED₂**

Charge status outputs

Push-pull outputs indicating charging status. See Table 2.

V_{SS}

Ground

V_{CC}

V_{CC} supply input

5.0V, $\pm 10\%$ power input.

MOD

Charge current control output

MOD is a push-pull output that is used to control the charging current to the battery. MOD switches high to enable charging current to flow and low to inhibit charging current flow.

DIS

Discharge control output

Push-pull output used to control an external transistor to discharge the battery before charging.

$\overline{\text{INH}}$

Charge inhibit input

When low, the bq2004E/H suspends all charge actions, drives all outputs to high impedance, and assumes a low-power operational state. When transitioning from low to high, a new charge cycle is started.

Functional Description

Figure 2 shows a block diagram and Figure 3 shows a state diagram of the bq2004E/H.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a two-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{RB1}{RB2} = \frac{N}{2} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1MΩ.

A ground-referenced negative temperature coefficient thermistor placed in proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 1. Both the BAT and TS inputs are referenced to SNS, so the signals used inside the IC are:

$$V_{BAT} - V_{SNS} = V_{CELL}$$

and

$$V_{TS} - V_{SNS} = V_{TEMP}$$

Discharge-Before-Charge

The $\overline{DCMD}$ input is used to command discharge-before-charge via the DIS output. Once activated, DIS becomes active (high) until V_{CELL} falls below V_{EDV}, at which time DIS goes low and a new fast charge cycle begins.

The $\overline{DCMD}$ input is internally pulled up to V_{CC} (its inactive state). Leaving the input unconnected, therefore, results in disabling discharge-before-charge. A negative going pulse on DCMD initiates discharge-before-charge at any time regardless of the current state of the bq2004. If DCMD is tied to V_{SS}, discharge-before-charge will be the first step in all newly started charge cycles.

Starting A Charge Cycle

A new charge cycle is started by:

1. Application of V_{CC} power.
2. V_{CELL} falling through the maximum cell voltage, V_{MCV} where:

$$V_{MCV} = 0.8 * V_{CC} \pm 30mV$$

3. A transition on the $\overline{INH}$ input from low to high.

If $\overline{DCMD}$ is tied low, a discharge-before-charge will be executed as the first step of the new charge cycle. Otherwise, pre-charge qualification testing will be the first step.

The battery must be within the configured temperature and voltage limits before fast charging begins.

The valid battery voltage range is V_{EDV} < V_{BAT} < V_{MCV} where:

$$V_{EDV} = 0.4 * V_{CC} \pm 30mV$$

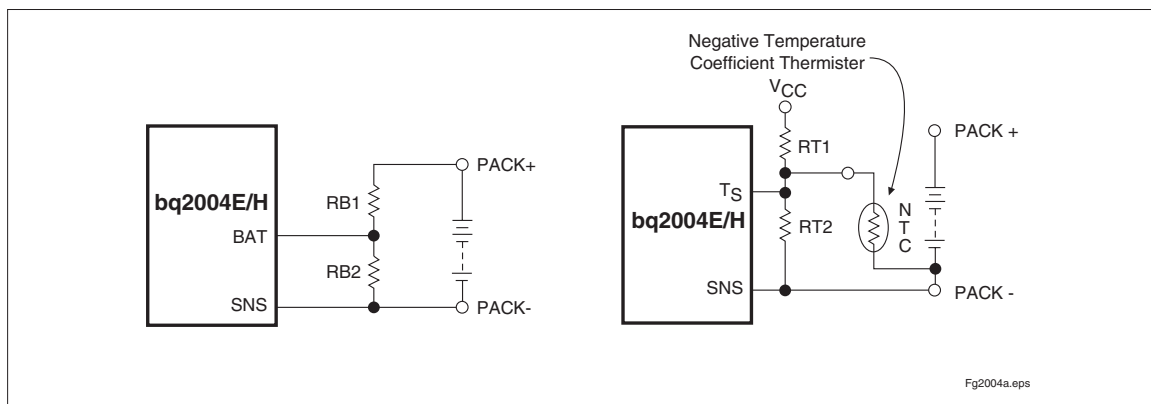


Figure 1. Voltage and Temperature Monitoring



111

— — — — —

0 0 0

VSEL Input	Voltage Termination
Low	Disabled
Float	-ΔV
High	PVD

Voltage Sampling

Each sample is an average of voltage measurements. The IC takes 32 measurements in PVD mode and 16 measurements in -ΔV mode. The resulting sample periods (9.17ms and 18.18ms, respectively) filter out harmonics centered around 55Hz and 109Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Temperature and Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off period, -ΔV and ΔT/Δt termination are disabled. The MOD pin is enabled at a duty cycle of 260μs active for every 1820μs inactive. This modulation results in an average rate 1/8th that of the fast charge rate. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. Maximum voltage and maximum temperature terminations are not affected by the hold-off period.

ΔT/Δt Termination

The bq2004E/H samples at the voltage at the TS pin every 34s, and compares it to the value measured two samples earlier. If V_{TEMP} has fallen 16mV ±4mV or more, fast charge is terminated. The ΔT/Δt termination test is valid only when $V_{TCO} < V_{TEMP} < V_{LTF}$.

Temperature Sampling

Each sample is an average of 16 voltage measurements. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Maximum Voltage, Temperature, and Time

Anytime V_{CELL} rises above V_{MCV} , the LEDs go off and current flow into the battery ceases immediately. If V_{CELL} then falls back below V_{MCV} before $t_{MCV} = 1.5s \pm 0.5s$, the chip transitions to the Charge Complete state (maximum voltage termination). If V_{CELL} remains above V_{MCV} at the expiration of t_{MCV} , the bq2004E/H transitions to the Battery Absent state (battery removal). See Figure 3.

Maximum temperature termination occurs anytime V_{TEMP} falls below the temperature cutoff threshold V_{TCO} . Charge will also be terminated if V_{TEMP} rises above the low temperature fault threshold, V_{LTF} , after fast charge begins.

Table 1. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast-Charge Rate		TM1	TM2	Typical Fast-Charge Safety Time (min)		Typical PVD, -ΔV Hold-Off Time (s)		Top-Off Rate		Pulse-Trickle Rate	Pulse-Trickle Period (Hz)	
2004E	2004H			2004E	2004H	2004E	2004H	2004E	2004H		2004E	2004H
C/4	C/8	Low	Low	325	650	137	273	Disabled		Disabled	Disabled	
C/2	C/4	Float	Low	154	325	546	546	Disabled		C/512	15	30
1C	C/2	High	Low	77	154	273	546	Disabled		C/512	7.5	15
2C	1C	Low	Float	39	77	137	273	Disabled		C/512	3.75	7.5
4C	2C	Float	Float	19	39	68	137	Disabled		C/512	1.88	3.75
C/2	C/4	High	Float	154	325	546	546	C/16	C/32	C/512	15	30
1C	C/2	Low	High	77	154	273	546	C/8	C/16	C/512	7.5	15
2C	1C	Float	High	39	77	137	273	C/4	C/18	C/512	3.75	7.5
4C	2C	High	High	19	39	68	137	C/2	C/4	C/512	1.88	3.75

Note: Typical conditions = 25°C, $V_{CC} = 5.0V$.

bq2004E/H

Table 2. bq2004E/H LED Output Summary

Mode 1 bq2004E	Charge Action State	LED₁	LED₂
DSEL = V _{SS}	Battery absent	Low	Low
	Fast charge pending or a discharge-before-charge in progress	High	High
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low
Mode 1 bq2004H	Charge Action State	LED₁	LED₂
DSEL = V _{SS}	Battery absent	Low	Low
	Discharge-before-charge in progress	High	High
	Fast charge pending	Low	$\frac{1}{8}$ second high $\frac{1}{8}$ second low
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low
Mode 2 bq2004E	Charge Action State (See note)	LED₁	LED₂
DSEL = Floating	Battery absent	Low	Low
	Fast charge pending or discharge-before-charge in progress	High	High
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low
Mode 2 bq2004H	Charge Action State (See note)	LED₁	LED₂
DSEL = Floating	Battery absent	Low	Low
	Discharge-before-charge in progress	High	High
	Fast charge pending	Low	$\frac{1}{8}$ second high $\frac{1}{8}$ second low
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low
Mode 3 bq2004E/H	Charge Action State	LED₁	LED₂
DSEL = V _{CC}	Battery absent	Low	Low
	Fast charge pending or discharge-before-charge in progress	Low	$\frac{1}{8}$ second high $\frac{1}{8}$ second low
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low

Note: Pulse trickle is inhibited in Mode 2.

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/4, C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for the C/2 through 4C rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time equal to 0.235* the fast-charge safety time (See Table 1.) During top-off, the MOD pin is enabled at a duty cycle of 260µs active for every 1820µs inactive. This modulation results in an average rate 1/8th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle charging may be configured to follow the fast charge and optional top-off charge phases to compensate for self-discharge of the battery while it is idle in the charger.

In the pulse-trickle mode, MOD is active for 260µs of a period specified by the settings of TM1 and TM2. See Table 1. The resulting trickle-charge rate is C/512. Both pulse trickle and top-off may be disabled by tying TM1 and TM2 to V_{SS} or by selecting Mode 2 in the display.

Charge Status Indication

Charge status is indicated by the LED₁ and LED₂ outputs. The state of these outputs in the various charge cycle phases is given in Table 2 and illustrated in Figure 3.

In all cases, if V_{CELL} exceeds the voltage at the MCV pin, both LED₁ and LED₂ outputs are held low regardless of other conditions. Both can be used to directly drive an LED.

Charge Current Control

The bq2004E/H controls charge current through the MOD output pin. The current control circuitry is designed to support implementation of a constant-current switching regulator or to gate an externally regulated current source.

When used in switch mode configuration, the nominal regulated current is:

$$I_{REG} = 0.225V/R_{SNS}$$

Charge current is monitored at the SNS input by the voltage drop across a sense resistor, R_{SNS}, between the low side of the battery pack and ground. R_{SNS} is sized to provide the desired fast charge current.

If the voltage at the SNS pin is less than V_{SNSLO}, the MOD output is switched high to pass charge current to the battery.

When the SNS voltage is greater than V_{SNSHI}, the MOD output is switched low—shutting off charging current to the battery.

$$V_{SNSLO} = 0.04 * V_{CC} \pm 25mV$$

$$V_{SNSHI} = 0.05 * V_{CC} \pm 25mV$$

When used to gate an externally regulated current source, the SNS pin is connected to V_{SS}, and no sense resistor is required.



Figure 3. Charge Algorithm State Diagram

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V _{CC}	V _{CC} relative to V _{SS}	-0.3	+7.0	V	
V _T	DC voltage applied on any pin excluding V _{CC} relative to V _{SS}	-0.3	+7.0	V	
T _{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T _{STG}	Storage temperature	-55	+125	°C	
T _{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T _{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = T_{OPR}; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V _{SNSHI}	High threshold at SNS resulting in MOD = Low	0.05 * V _{CC}	±0.025	V	
V _{SNSLO}	Low threshold at SNS resulting in MOD = High	0.04 * V _{CC}	±0.025	V	
V _{LTF}	Low-temperature fault	0.4 * V _{CC}	±0.030	V	V _{TEMP} ≥ V _{LTF} inhibits/terminates charge
V _{HTF}	High-temperature fault	(1/3 * V _{LTF}) + (2/3 * V _{TCO})	±0.030	V	V _{TEMP} ≤ V _{HTF} inhibits charge
V _{EDV}	End-of-discharge voltage	0.4 * V _{CC}	±0.030	V	V _{CELL} < V _{EDV} inhibits fast charge
V _{MCV}	Maximum cell voltage	0.8 * V _{CC}	±0.030	V	V _{CELL} > V _{MCV} inhibits/terminates charge
V _{THERM}	TS input change for ΔT/Δt detection	-16	±4	mV	V _{CC} = 5V, T _A = 25°C
-ΔV	BAT input change for -ΔV detection	-12	±4	mV	V _{CC} = 5V, T _A = 25°C
PVD	BAT input change for PVD detection	-6	±2	mV	V _{CC} = 5V, T _A = 25°C

bq2004E/H

Recommended DC Operating Conditions (T_A = T_{OPR})

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V _{CC}	Supply voltage	4.5	5.0	5.5	V	
V _{BAT}	Battery input	0	-	V _{CC}	V	
V _{CELL}	BAT voltage potential	0	-	V _{CC}	V	V _{BAT} - V _{SNS}
V _{TS}	Thermistor input	0	-	V _{CC}	V	
V _{TEMP}	TS voltage potential	0	-	V _{CC}	V	V _{TS} - V _{SNS}
V _{TCO}	Temperature cutoff	0.2 * V _{CC}	-	0.4 * V _{CC}	V	Valid ΔT/Δt range
V _{IH}	Logic input high	2.0	-	-	V	DCMD, INH
	Logic input high	V _{CC} - 0.3	-	-	V	TM ₁ , TM ₂ , DSEL, VSEL
V _{IL}	Logic input low	-	-	0.8	V	DCMD, INH
	Logic input low	-	-	0.3	V	TM ₁ , TM ₂ , DSEL, VSEL
V _{OH}	Logic output high	V _{CC} - 0.8	-	-	V	DIS, MOD, LED ₁ , LED ₂ , I _{OH} ≤ -10mA
V _{OL}	Logic output low	-	-	0.8	V	DIS, MOD, LED ₁ , LED ₂ , I _{OL} ≤ 10mA
I _{CC}	Supply current	-	1	3	mA	Outputs unloaded
I _{SB}	Standby current	-	-	1	μA	INH = V _{IL}
I _{OH}	DIS, LED ₁ , LED ₂ , MOD source	-10	-	-	mA	@V _{OH} = V _{CC} - 0.8V
I _{OL}	DIS, LED ₁ , LED ₂ , MOD sink	10	-	-	mA	@V _{OL} = V _{SS} + 0.8V
I _L	Input leakage	-	-	±1	μA	INH, BAT, V = V _{SS} to V _{CC}
	Input leakage	50	-	400	μA	DCMD, V = V _{SS} to V _{CC}
I _{IL}	Logic input low source	-	-	70	μA	TM ₁ , TM ₂ , DSEL, VSEL, V = V _{SS} to V _{SS} + 0.3V
I _{IH}	Logic input high source	-70	-	-	μA	TM ₁ , TM ₂ , DSEL, VSEL, V = V _{CC} - 0.3V to V _{CC}
I _{IZ}	Tri-state	-2	-	2	μA	TM ₁ , TM ₂ , DSEL, and VSEL should be left disconnected (floating) for Z logic input state

Note: All voltages relative to V_{SS} except as noted.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R _{BAT}	Battery input impedance	50	-	-	MΩ
R _{TS}	TS input impedance	50	-	-	MΩ
R _{TCO}	TCO input impedance	50	-	-	MΩ
R _{SNS}	SNS input impedance	50	-	-	MΩ

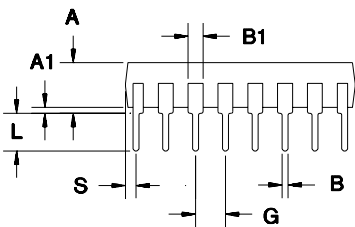
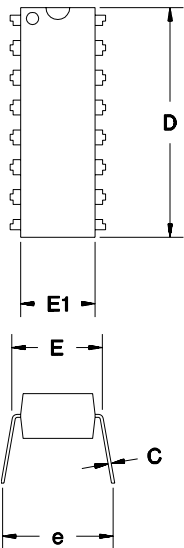
Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t _{pw}	Pulse width for $\overline{\text{DCMD}}$ and $\overline{\text{INH}}$ pulse command	1	-	-	μs	Pulse start for charge or discharge before charge
d _{FCV}	Time base variation	-16	-	16	%	V _{CC} = 4.75V to 5.25V
f _{REG}	MOD output regulation frequency	-	-	300	kHz	
t _{MCV}	Maximum voltage termination time limit	1	-	2	s	Time limit to distinguish battery removed from charge complete.

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

bq2004E/H

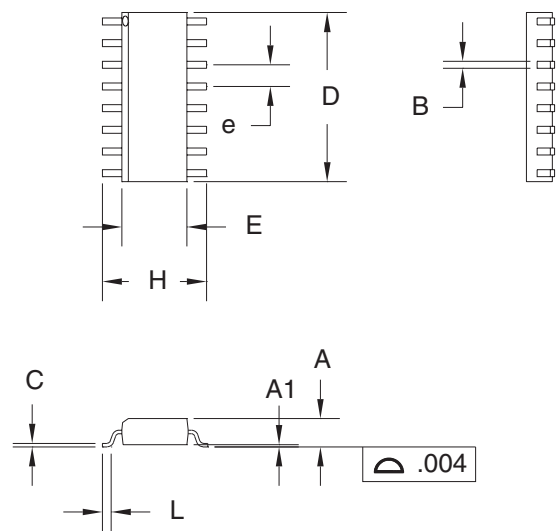
16-Pin DIP Narrow (PN)



16-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.740	0.770	18.80	19.56
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

16-Pin SOIC Narrow (SN)



16-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

bq2004E/H

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	All	Combined bq2004E and bq2004H, revised and expanded format of this data sheet	Clarification
2	7	Separated bq2004E and bq2004H in Table 2, LED Output Summary	Clarification
3	5	Description of charge-pending state	Clarification
4			
5	9	Corrected V_{SNSLO} tolerance	Was: ± 0.010 Is: ± 0.025

Note: Change 1 = Oct. 1997 B changes from Sept. 1996 (bq2004E), Feb. 1997 (bq2004H).
Change 2 = Feb. 1998 C changes from Oct. 1997 B.
Change 3 = Dec. 1998 D changes from Feb. 1998 C.
Change 4 = June 1999 E changes from Dec. 1998 D.
Change 5 = Apr. 2005 F changes from June 1999 E.

Ordering Information

bq2004

Package Option:

PN = 16-pin narrow plastic DIP
SN = 16-pin narrow SOIC

Device:

E = bq2004E Fast-Charge IC
H = bq2004H Fast-Charge IC

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ2004EPN	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 70	2004EPN -A6
BQ2004EPN.B	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 70	2004EPN -A6
BQ2004ESN	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2004E (-A6, A6)
BQ2004ESN.B	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2004E (-A6, A6)
BQ2004ESNTR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2004E (-A6, A6)
BQ2004ESNTR.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2004E (-A6, A6)
BQ2004HPN	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 70	2004HPN -A7
BQ2004HPN.B	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 70	2004HPN -A7
BQ2004HSN	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2004H (-A7, A7)
BQ2004HSN.B	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2004H (-A7, A7)
BQ2004HSNTR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2004H (-A7, A7)
BQ2004HSNTR.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2004H (-A7, A7)

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

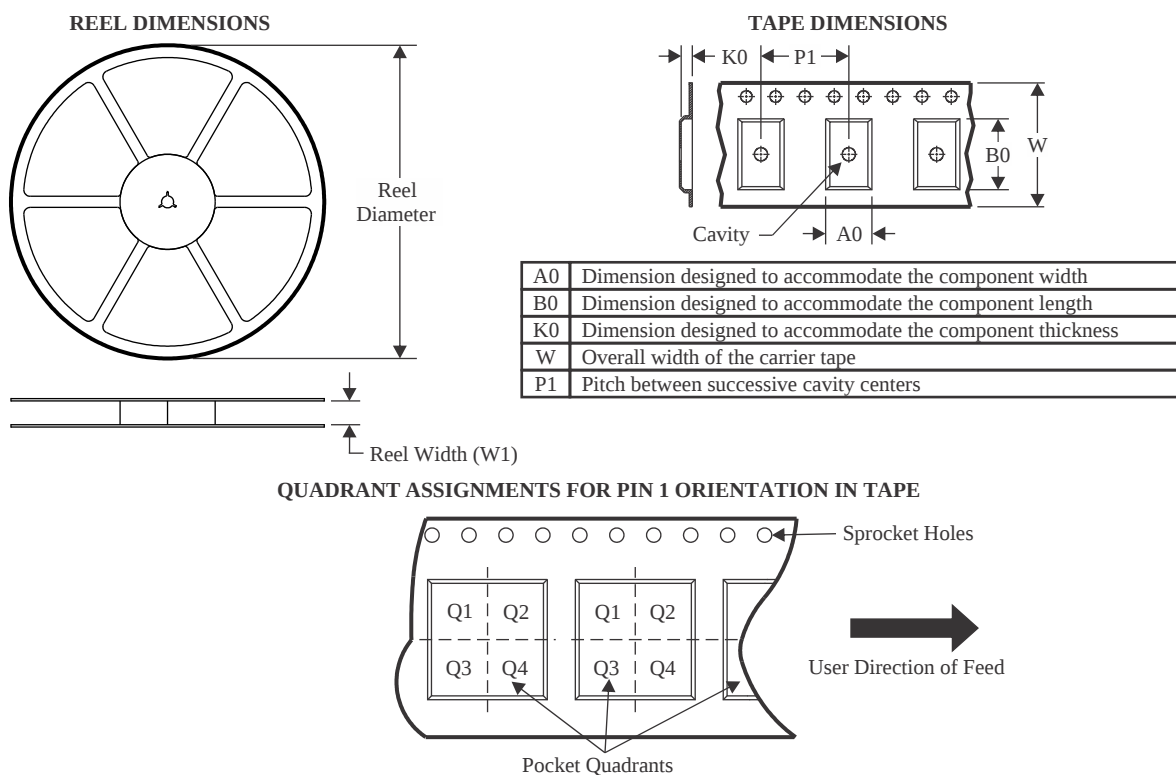
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

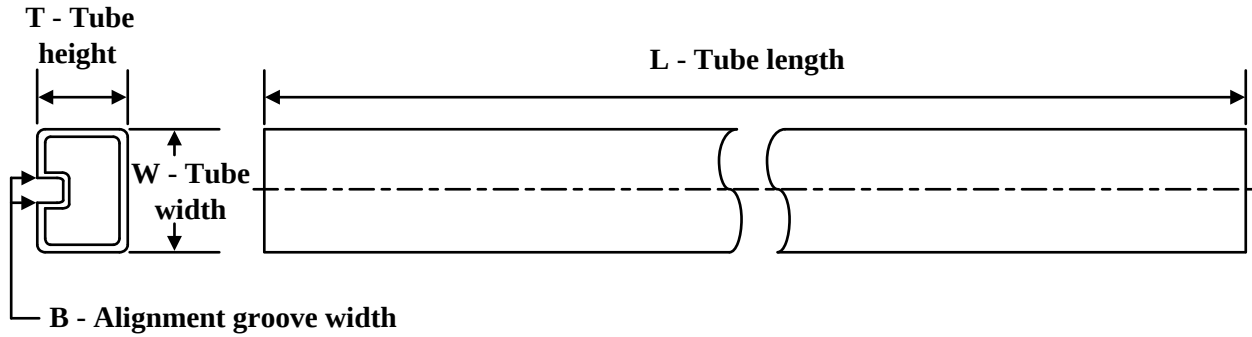
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2004ESNTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
BQ2004HSNTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2004ESNTR	SOIC	D	16	2500	356.0	356.0	35.0
BQ2004HSNTR	SOIC	D	16	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
BQ2004EPN	N	PDIP	16	25	506	13.97	11230	4.32
BQ2004EPN.B	N	PDIP	16	25	506	13.97	11230	4.32
BQ2004ESN	D	SOIC	16	40	506.6	8	3940	4.32
BQ2004ESN.B	D	SOIC	16	40	506.6	8	3940	4.32
BQ2004HPN	N	PDIP	16	25	506	13.97	11230	4.32
BQ2004HPN.B	N	PDIP	16	25	506	13.97	11230	4.32
BQ2004HSN	D	SOIC	16	40	506.6	8	3940	4.32
BQ2004HSN.B	D	SOIC	16	40	506.6	8	3940	4.32

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



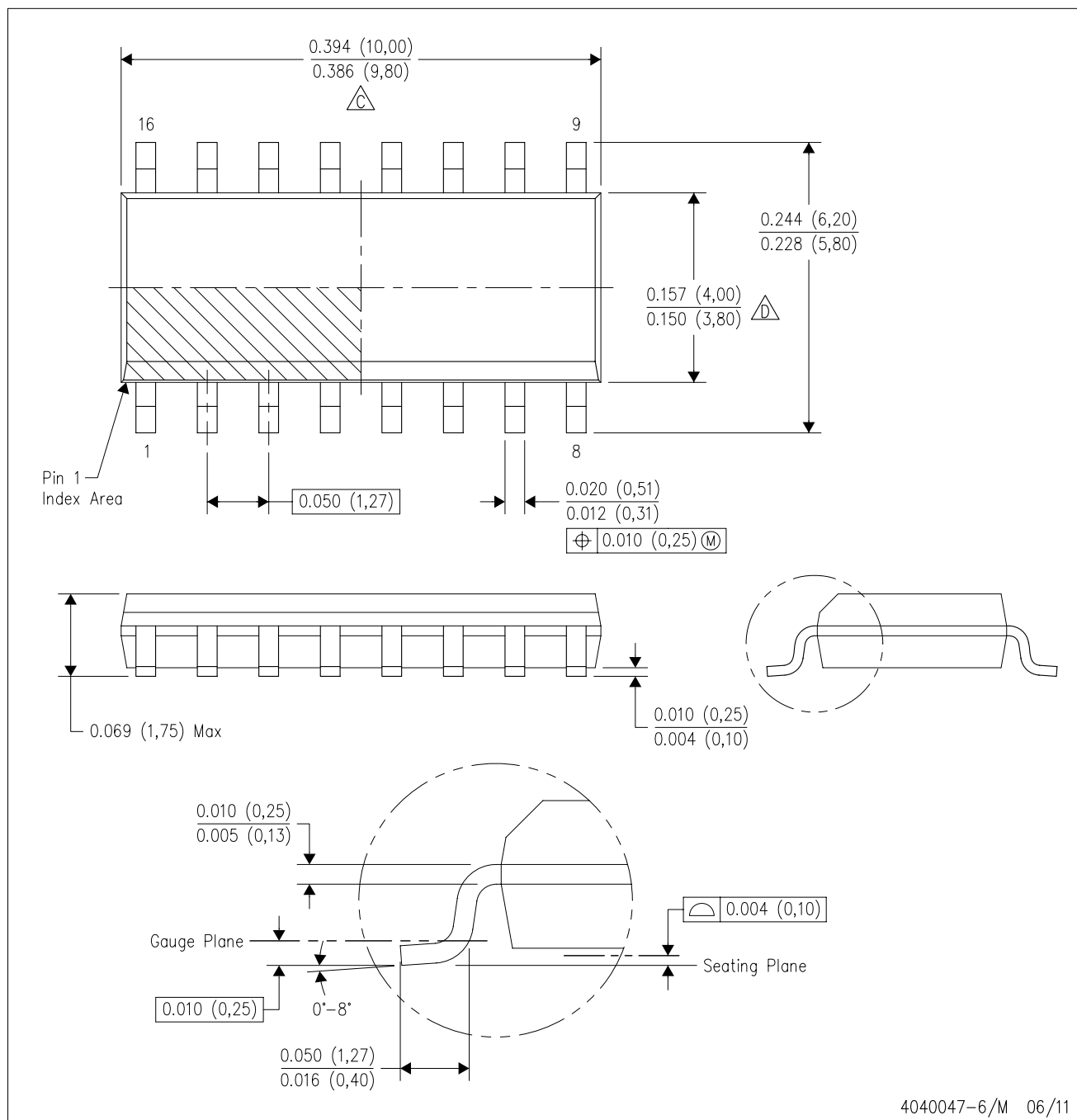
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated