

3.3 V FULL-DUPLEX RS-485/RS-422 DRIVERS AND BALANCED RECEIVERS

FEATURES

- Designed for INTERBUS Applications
- Designed for RS-422 and RS-485 Networks
- Balanced Receiver Thresholds
- 1/2 Unit-Load (up to 64 nodes on the bus)
- Bus-Pin ESD Protection 15 kV HBM
- Bus-Fault Protection of –7 V to 12 V
- Thermal Shutdown Protection
- Power-Up/Down Glitch-free Bus Inputs and Outputs
- High Input Impedance With Low V_{CC}
- Monotonic Outputs During Power Cycling
- 5-V Tolerant Inputs

APPLICATIONS

- Digital Motor Control
- Utility Meters
- Chassis-to-Chassis Interconnections
- Electronic Security Stations
- Industrial, Process, and Building Automation
- Point-of-Sale (POS) Terminals and Networks
- DTE/DCE Interfaces

DESCRIPTION

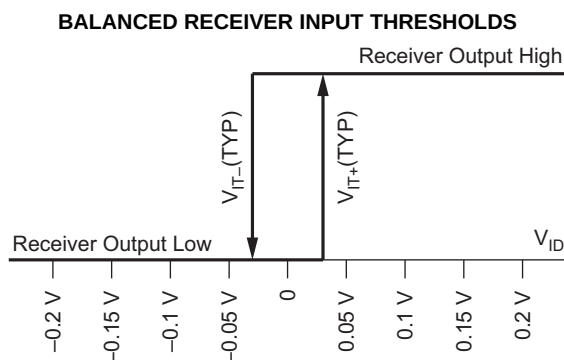
The SN65HVD379 is a differential line driver and differential-input line receiver that operates with a 3.3-V power supply. Each driver and receiver has separate input and output pins for full-duplex bus communication designs. They are designed for balanced transmission lines and interoperation with ANSI TIA/EIA-485A, TIA/EIA-422-B, ITU-T v.11, and ISO 8482:1993 standard-compliant devices.

These differential bus drivers and receivers are monolithic, integrated circuits designed for full-duplex bi-directional data communication on multipoint bus-transmission lines at signaling rates⁽¹⁾ up to 25 Mbps. The SN65HVD379 is fully enabled with no external enabling pins.

The 1/2 unit load receiver has a higher receiver input resistance. This results in lower bus leakage currents over the common-mode voltage range, and reduces the total amount of current that an RS-485 driver is forced to source or sink when transmitting.

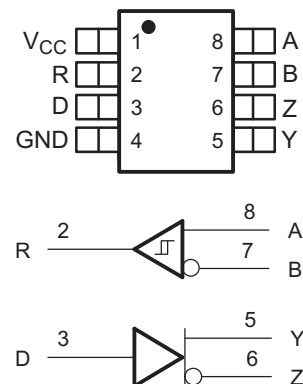
The balanced differential receiver input threshold makes the SN65HVD379 more compatible with fieldbus requirements that define an external failsafe structure.

- (1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).



SN65HVD379

**D PACKAGE
(TOP VIEW)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

SIGNALING RATE	UNIT LOADS	PART NUMBER ⁽¹⁾	SOIC MARKING
25 Mbps	1/2	SN65HVD379	

(1) These are The D package is available taped and reeled. Add an R suffix to the part number (ie. SN65HVD379DR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted^{(1) (2)}

		UNIT
V_{CC}	Supply voltage range	–0.3 V to 6 V
V_A, V_B, V_Y, V_Z	Voltage range at any bus terminal (A, B, Y, Z)	–9 V to 14 V
V_{TRANS}	Voltage input, transient pulse through 100 Ω . See Figure 8 (A, B, Y, Z) ⁽³⁾	–50 to 50 V
V_I	Input voltage range (D, DE, $\overline{RE}$)	–0.5 V to 7 V
P_{CONT}	Continuous total power dissipation	Internally limited ⁽⁴⁾
I_O	Output current (receiver output only, R)	11 mA

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) This tests survivability only and the output state of the receiver is not specified.
- (4) The Thermal shutdown protection circuit internally limits the continuous total power dissipation. Thermal shutdown typically occurs when the junction temperature reaches 165°C.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3		3.6	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)	–7 ⁽¹⁾		12	
$1/t_{UI}$	Signaling rate			25	Mbps
R_L	Differential load resistance	54	60		Ω
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	
V_{ID}	Differential input voltage	–12		12	
I_{OH}	High-level output current	Driver		–60	mA
		Receiver		–8	
I_{OL}	Low-level output current	Driver		60	mA
		Receiver		8	
T_A	Ambient still-air temperature	–40		85	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ELECTROSTATIC DISCHARGE PROTECTION

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
Human body model	Bus terminals and GND		16		kV
Human body model ⁽²⁾	All pins		4		
Charged-device-model ⁽³⁾	All pins		1		

(1) All typical values at 25°C with 3.3-V supply.

(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(3) Tested in accordance with JEDEC Standard 22, Test Method C101.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$V_{I(K)}$ Input clamp voltage	$I_I = -18$ mA	-1.5			V
$ V_{OD(SS)} $ Steady-state differential output voltage	$I_O = 0$	2		V_{CC}	
	$R_L = 54 \Omega$, See Figure 1 ⁽²⁾ (RS-485)	1.5	2.0		
	$R_L = 100 \Omega$, See Figure 1 (RS-422)	2	2.3		
	$V_{test} = -7$ V to 12 V, See Figure 2	1.5			
$\Delta V_{OD(SS)} $ Change in magnitude of steady-state differential output voltage between states	$R_L = 54 \Omega$, See Figure 1 and Figure 2	-0.2		0.2	
$V_{OD(RING)}$ Differential output voltage overshoot and undershoot	$R_L = 54 \Omega$, $C_L = 50$ pF, See Figure 5 (Figure 3 for definitions)			10% ⁽³⁾	
$V_{OC(PP)}$ Peak-to-peak common-mode output voltage	See Figure 3		0.5		
$V_{OC(SS)}$ Steady-state common-mode output voltage			1.6	2.3	
$\Delta V_{OC(SS)}$ Change in steady-state common-mode output voltage		-0.05		0.05	
$I_{Z(Z)}$ or $I_{Y(Z)}$ High-impedance state output current	$V_{CC} = 0$ V, V_Z or $V_Y = 12$ V, Other input at 0 V			90	μ A
	$V_{CC} = 0$ V, V_Z or $V_Y = -7$ V, Other input at 0 V	-10			
$I_{Z(S)}$ or $I_{Y(S)}$ Short-circuit output current ⁽⁴⁾	V_Z or $V_Y = -7$ V	Other input at 0 V	-250	250	mA
	V_Z or $V_Y = 12$ V		-250	250	
I_I Input current	D $V_I = 0$ or $V_I = 2.0$	0		100	A
$C_{(OD)}$ Differential output capacitance	$V_{OD} = 0.4 \sin(4E6\pi t) + 0.5$ V, V_{CC} at 0 V		16		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) V_{CC} is 3.3 Vdc 5%.

(3) 10% of the peak-to-peak differential-output voltage swing, per TIA/EIA-485.

(4) Under some conditions of short-circuit to negative voltages, output currents exceeding the ANSI TIA/EIA-485-A maximum current of 250 mA may occur. Continuous exposure may affect device reliability.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$R_L = 54 \Omega$, $C_L = 50$ pF, See Figure 5	4	10	18	ns
t_{PHL} Propagation delay time, high-to-low-level output					
t_r Differential output signal rise time		2.5	5	12	ns
t_f Differential output signal fall time					
$t_{sk(p)}$ Pulse skew ($ t_{PHL} - t_{PLH} $)			0.6		ns
$t_{sk(pp)}$ ⁽²⁾ Part-to-part skew			1		ns

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going differential input threshold voltage	I _O = –8 mA			0.2	V
V _{IT–}	Negative-going differential input threshold voltage	I _O = 8 mA	–0.2			
V _{hys}	Hysteresis voltage (V _{IT+} – V _{IT–})			50		mV
V _O	Output voltage	V _{ID} = 200 mV, I _O = –8 mA, See Figure 7	2.4			V
		V _{ID} = –200 mV, I _O = 8 mA, See Figure 7			0.4	
I _A or I _B	Bus input current	V _A or V _B = 12 V		0.20	0.35	mA
		V _A or V _B = 12 V, V _{CC} = 0 V		0.24	0.40	
		V _A or V _B = –7 V	–0.35	–0.18		
		V _A or V _B = –7 V, V _{CC} = 0 V	–0.25	–0.13		
C _{ID}	Differential input capacitance	V _{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		15		pF
I _{CC}	Supply current	D at 0 V or V _{CC} and No Load			2.1	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	V _{ID} = –1.5 V to 1.5 V, C _L = 15 pF, See Figure 7		26	45	ns
t _{PHL}	Propagation delay time, high-to-low-level output					
t _{sk(p)}	Pulse skew (t _{PHL} – t _{PLH})				7	
t _{sk(pp)}	Part-to-part skew ⁽²⁾			5		
t _r	Output signal rise time				5	
t _f	Output signal fall time				6	

(1) All typical values are at 25°C and with a 3.3-V supply

(2) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

DEVICE POWER DISSIPATION – P_D

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P _D Device power dissipation	R _L = 60 Ω, C _L = 50 pF, Input to D a 50% duty cycle square wave at indicated signaling rate T _A = 85°C			197	mW

FUNCTION TABLES

DRIVER			RECEIVER	
INPUT	OUTPUTS		DIFFERENTIAL INPUTS	OUTPUTS
D	Y	Z	V _{ID} = V _A –V _B	R
H	H	L	V _{ID} ≤ –0.2 V	L
L	L	H	–0.2 V < V _{ID} < 0.2 V	?
Open	L	H	0.2 V ≤ V _{ID}	H

PARAMETER MEASUREMENT INFORMATION

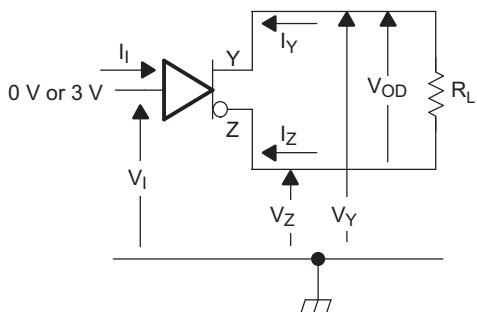


Figure 1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

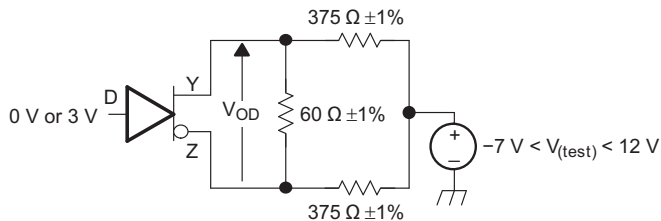


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit

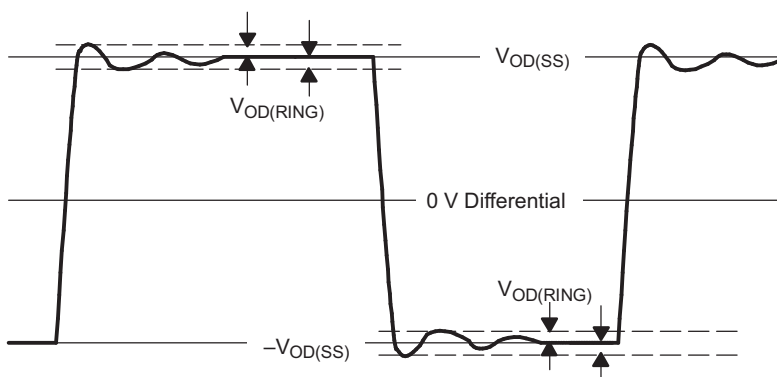
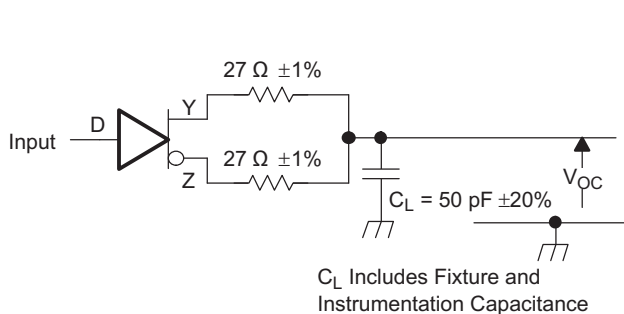


Figure 3. $V_{OD(RING)}$ Waveform and Definitions

$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.



C_L Includes Fixture and Instrumentation Capacitance

Input: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_O = 50 \Omega$

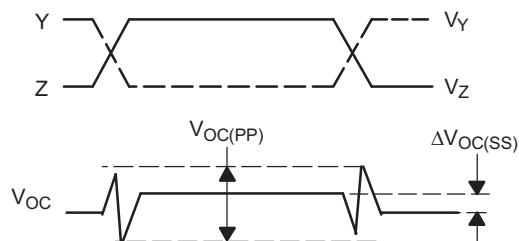


Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)

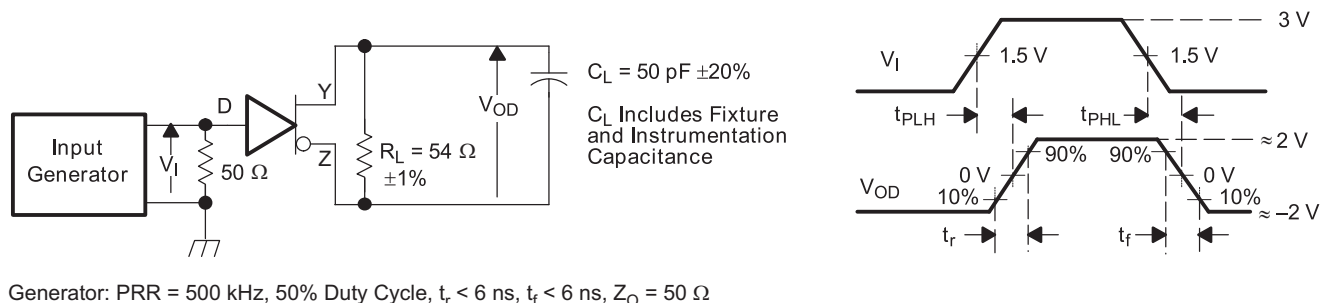


Figure 5. Driver Switching Test Circuit and Voltage Waveforms

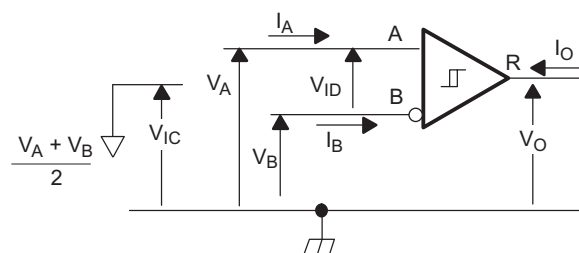


Figure 6. Receiver Voltage and Current Definitions

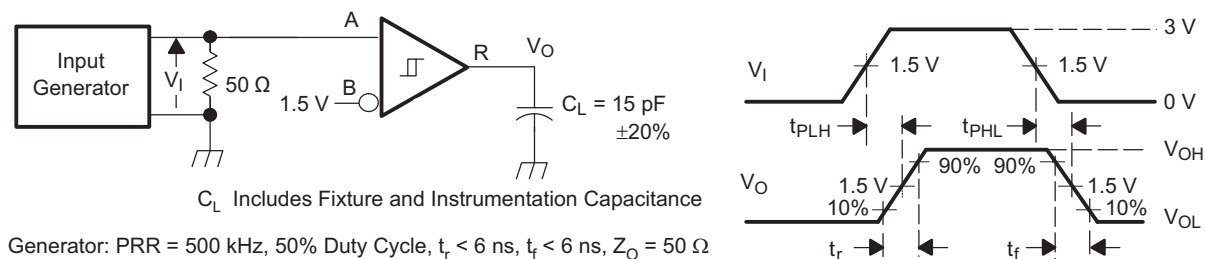


Figure 7. Receiver Switching Test Circuit and Voltage Waveforms

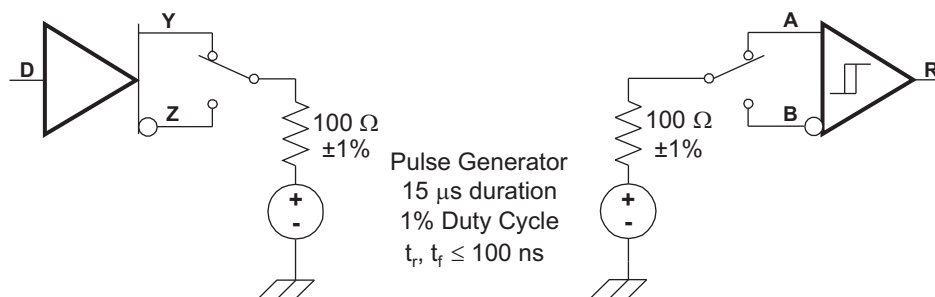
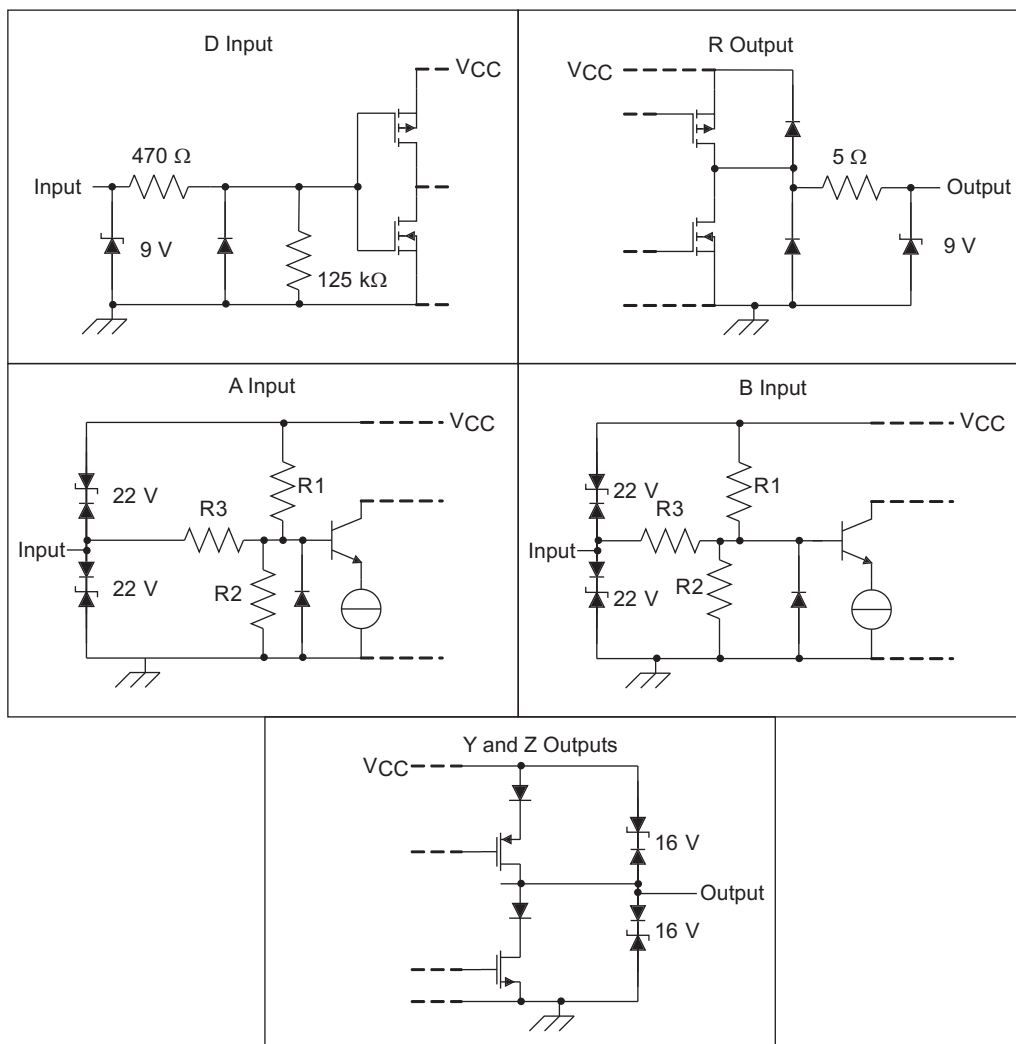


Figure 8. Test Circuit, Transient Over Voltage Test

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD379	9 kΩ	45 kΩ

TYPICAL CHARACTERISTICS

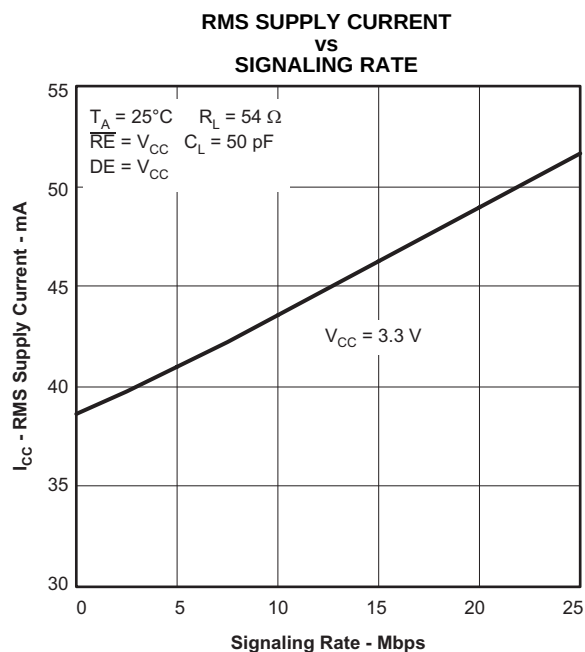


Figure 9.

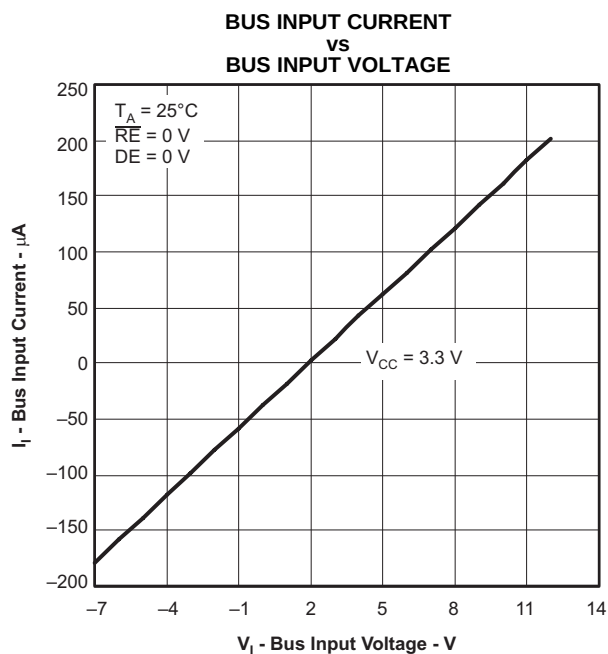


Figure 10.

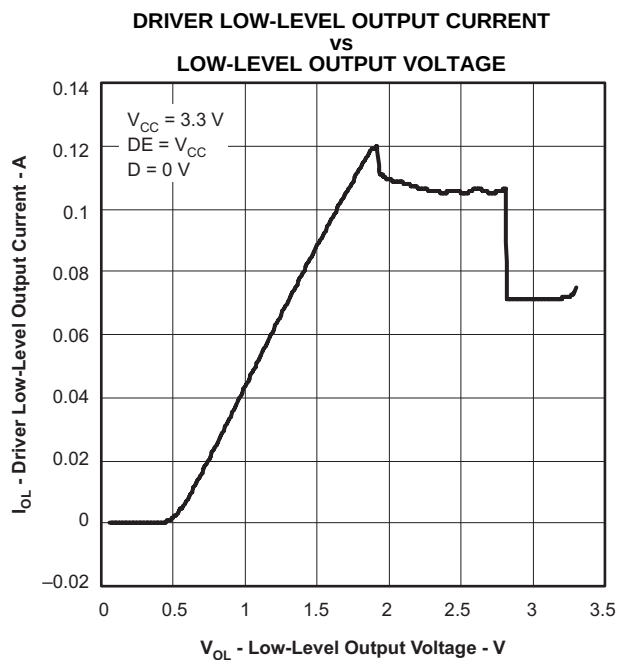


Figure 11.

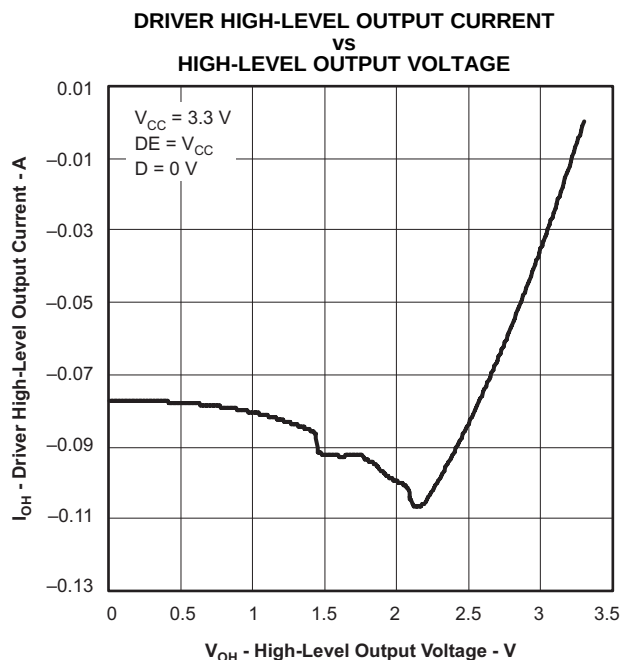
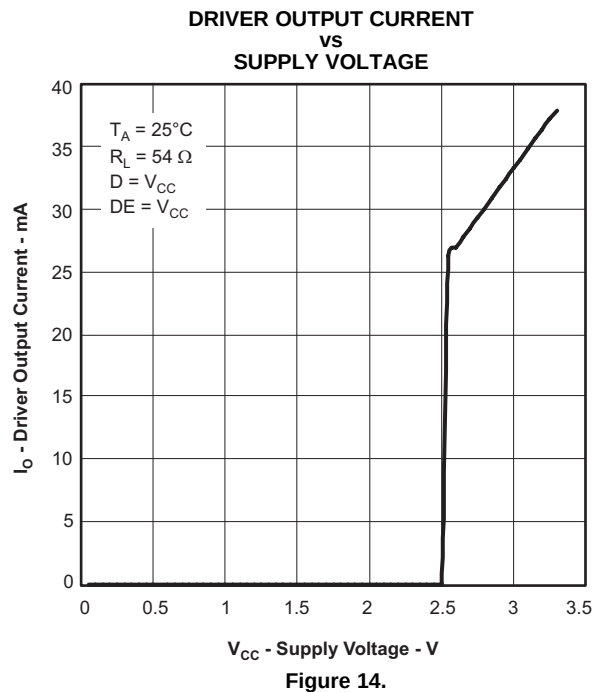
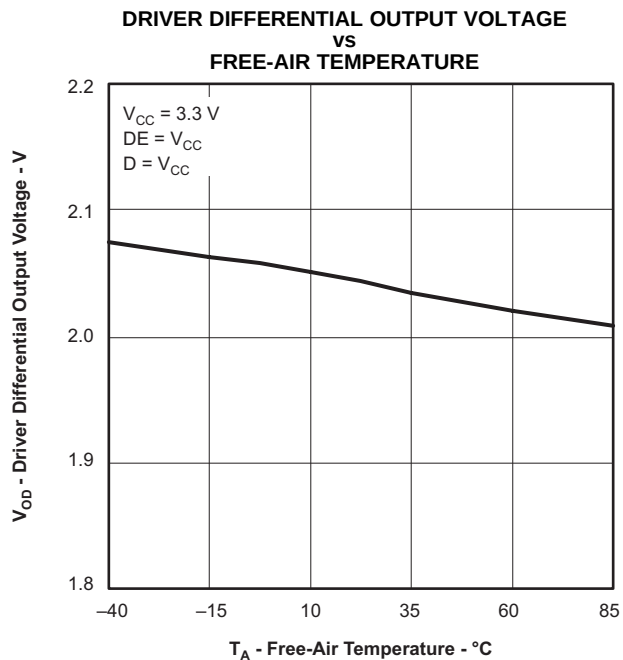


Figure 12.

TYPICAL CHARACTERISTICS (continued)



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD379DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP379
SN65HVD379DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP379

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

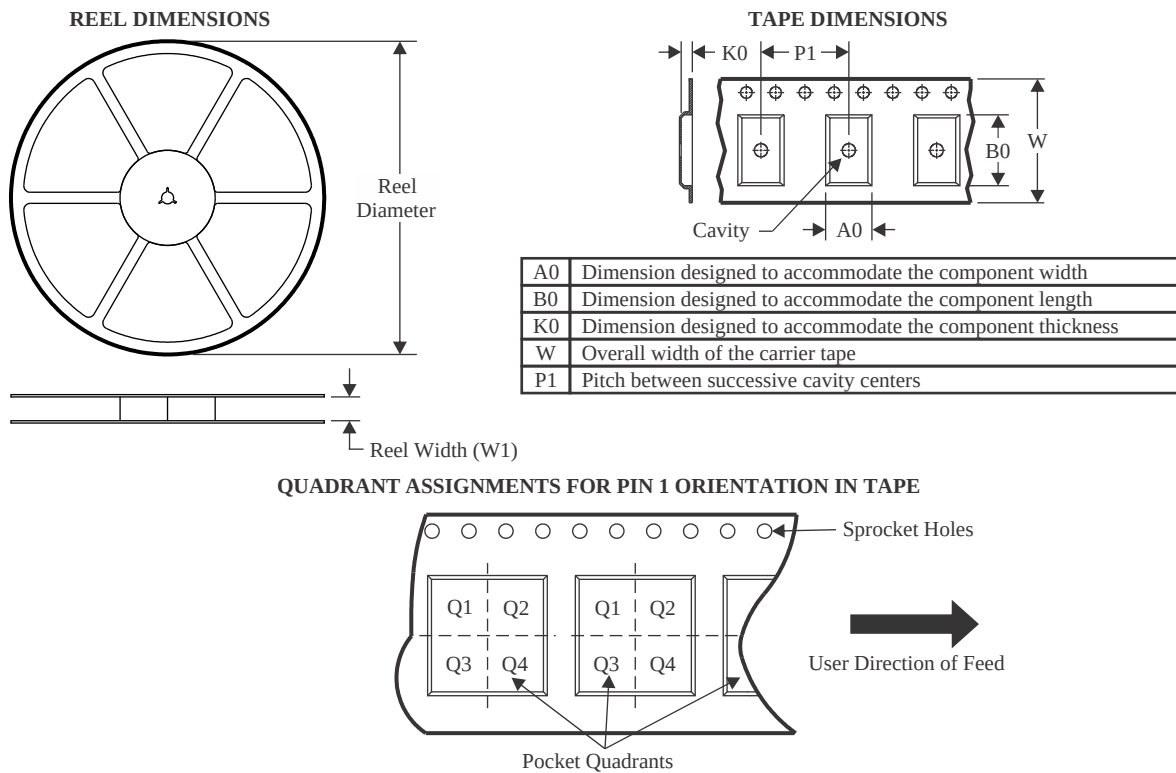
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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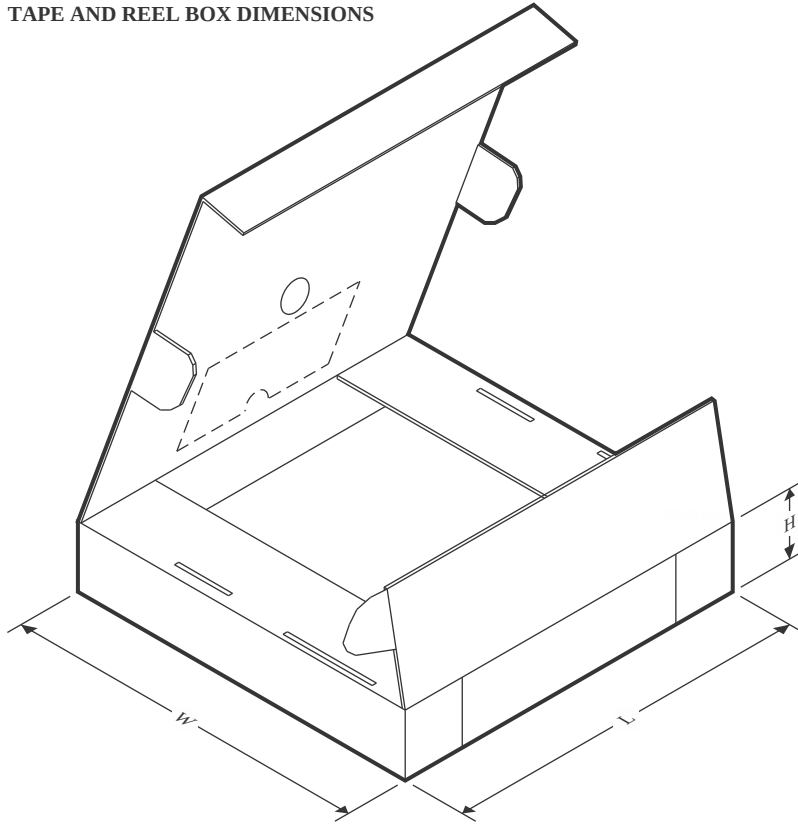
TAPE AND REEL INFORMATION



*All dimensions are nominal

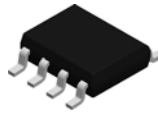
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD379DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD379DR	SOIC	D	8	2500	356.0	356.0	35.0

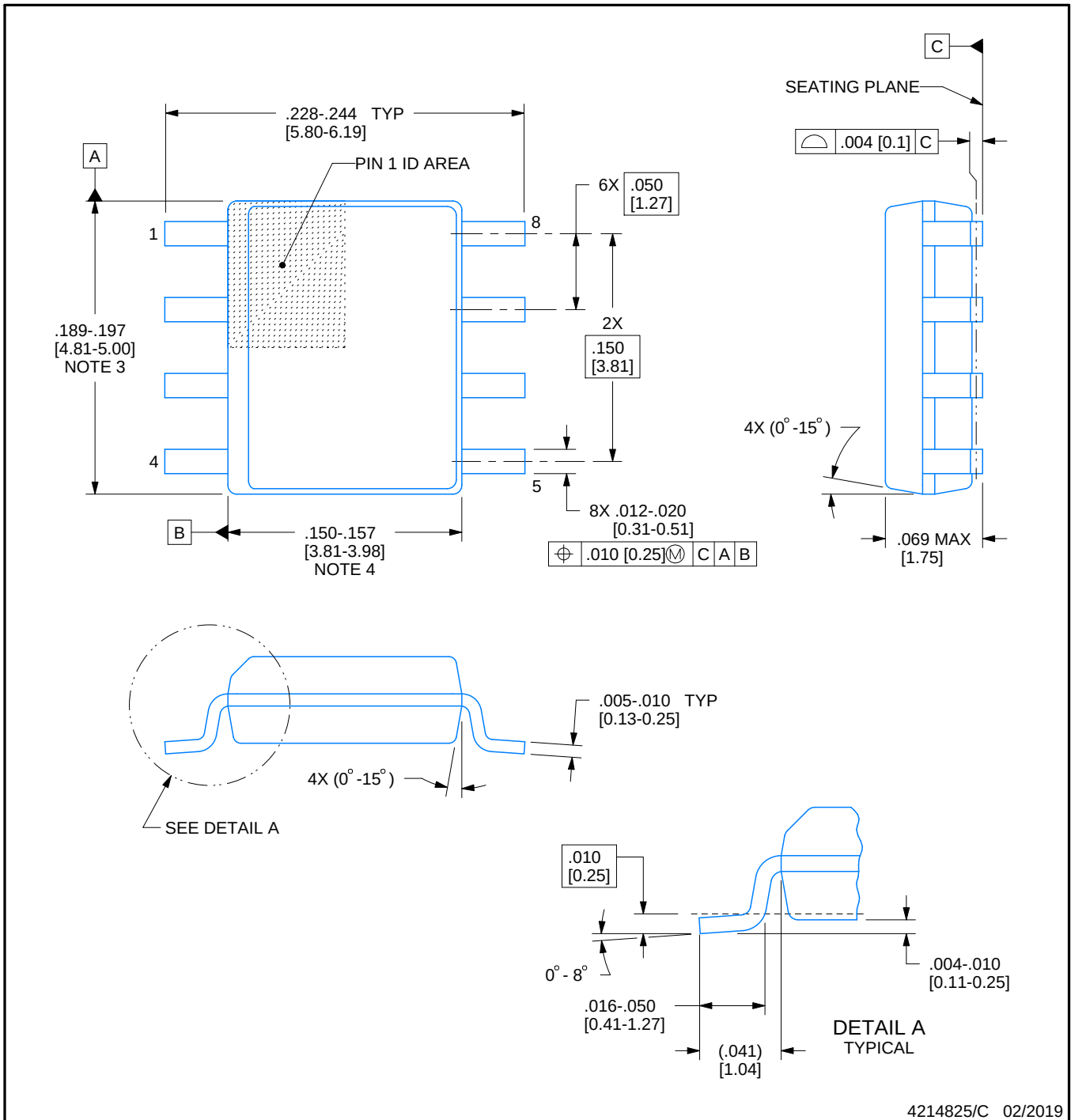


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

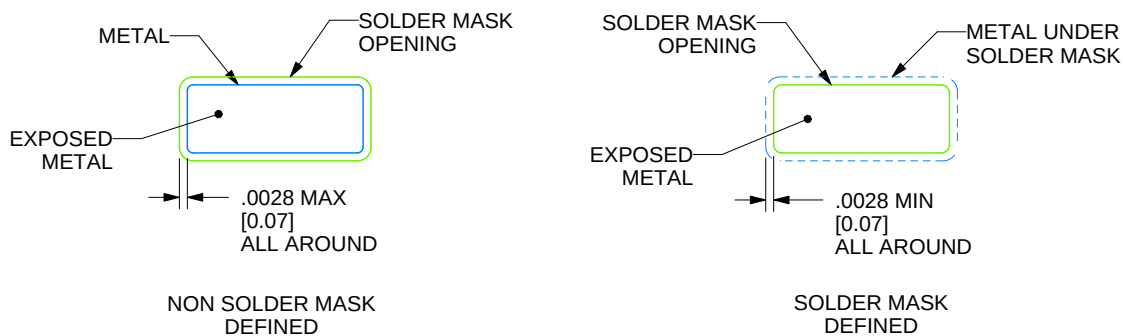
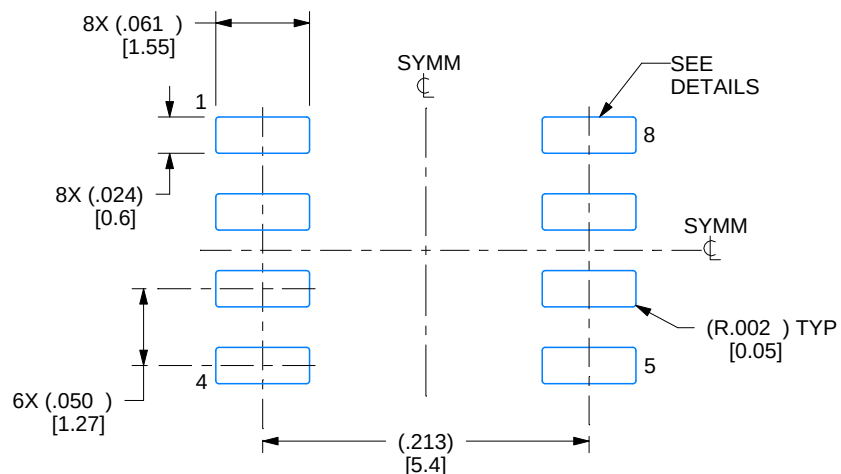
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

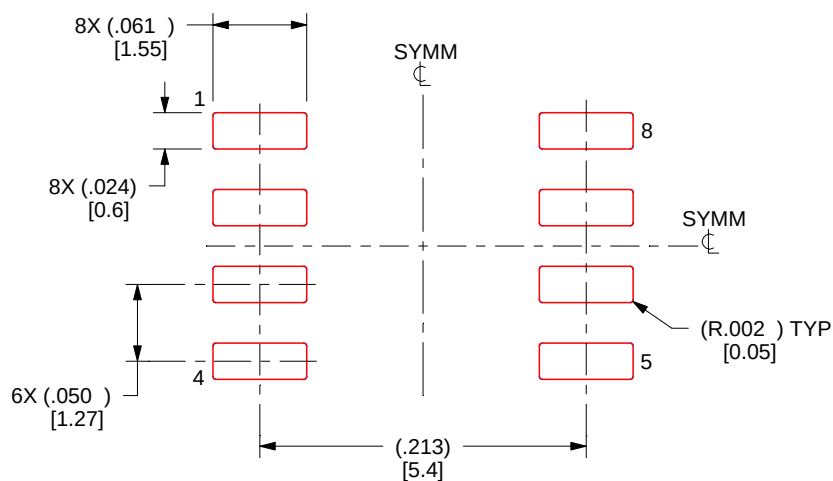
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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