

LM324-MIL Quadruple Operational Amplifier

1 Features

- Wide Supply Ranges
 - Single Supply: 3 V to 32 V
 - Dual Supplies: ± 1.5 V to ± 16 V
- Low Supply-Current Drain Independent of Supply Voltage: 0.8 mA Typical
- Common-Mode Input Voltage Range Includes Ground, Allowing Direct Sensing Near Ground
- Low Input Bias and Offset Parameters
 - Input Offset Voltage: 3 mV Typical
 - Input Offset Current: 2 nA Typical
 - Input Bias Current: 20 nA Typical
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: 32 V
- Open-Loop Differential Voltage Amplification: 100 V/mV Typical
- Internal Frequency Compensation
- On Products Compliant to MIL-PRF-38535, All Parameters are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Blu-ray Players and Home Theaters
- Chemical and Gas Sensors
- DVD Recorders and Players
- Digital Multimeter: Bench and Systems
- Digital Multimeter: Handhelds
- Field Transmitter: Temperature Sensors
- Motor Control: AC Induction, Brushed DC, Brushless DC, High-Voltage, Low-Voltage, Permanent Magnet, and Stepper Motor
- Oscilloscopes
- TV: LCD and Digital
- Temperature Sensors or Controllers Using Modbus
- Weigh Scales

3 Description

This device consist of four independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply or split supply over a wide range of voltages.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM324-MIL	SOIC (14)	8.65 mm × 3.91 mm
	CDIP (14)	19.56 mm × 6.67 mm
	PDIP (14)	19.30 mm × 6.35 mm
	CFP (14)	9.21 mm × 5.97 mm
	TSSOP (14)	5.00 mm × 4.40 mm
	SO (14)	9.20 mm × 5.30 mm
	SSOP (14)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Symbol (Each Amplifier)

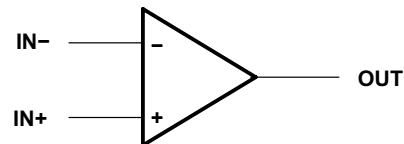


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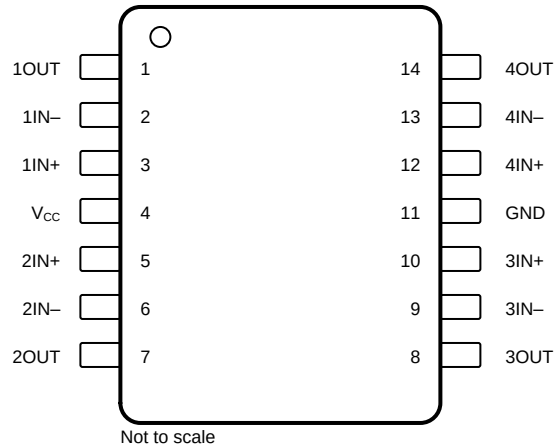
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4 Revision History

DATE	REVISION	NOTES
June 2017	*	Initial release.

5 Pin Configuration and Functions

D, DB, J, N, NS, PW, W PACKAGE
14-Pin SOIC, SSOP, CDIP, PDIP, SO, TSSOP, CFP
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Negative input
1IN+	3	I	Positive input
1OUT	1	O	Output
2IN–	6	I	Negative input
2IN+	5	I	Positive input
2OUT	7	O	Output
3IN–	9	I	Negative input
3IN+	10	I	Positive input
3OUT	8	O	Output
4IN–	13	I	Negative input
4IN+	12	I	Positive input
4OUT	14	O	Output
GND	11	—	Ground
NC	—	—	Do not connect
V _{CC}	4	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, V_{CC} ⁽²⁾	±16	32	V
Differential input voltage, V_{ID} ⁽³⁾		±32	V
Input voltage, V_I (either input)	–0.3	32	V
Duration of output short circuit (one amplifier) to ground at (or below) $T_A = 25^\circ\text{C}$, $V_{CC} \leq 15\text{ V}$ ⁽⁴⁾	Unlimited		
Operating virtual junction temperature, T_J		150	°C
Case temperature for 60 seconds	FK package		260
Storage temperature, T_{stg}	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
- (3) Differential voltages are at $IN+$, with respect to $IN-$.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±500
	Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{CC} Supply voltage	3	30	V
V_{CM} Common-mode voltage	0	$V_{CC} - 2$	V
T_A Operating free air temperature	0	70	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	J (CDIP)	W (CFP)	UNIT
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$ ⁽²⁾⁽³⁾ Junction-to-ambient thermal resistance	86	86	80	76	113	—	—	°C/W
$R_{\theta JC}$ ⁽⁴⁾ Junction-to-case (top) thermal resistance	—	—	—	—	—	15.05	14.65	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
- (3) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_C . The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_{J(max)} - T_C)/R_{\theta JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

6.5 Electrical Characteristics

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS ⁽¹⁾		T _A ⁽²⁾	MIN	TYP ⁽³⁾	MAX	UNIT
V _{IO}	Input offset voltage	V _{CC} = 5 V to MAX, V _{IC} = V _{ICR} min, V _O = 1.4 V		25°C		3		7	mV
				Full range				9	
I _{IO}	Input offset current	V _O = 1.4 V		25°C		2		50	nA
				Full range				150	
I _{IB}	Input bias current	V _O = 1.4 V		25°C		–20		–250	nA
				Full range				–500	
V _{ICR}	Common-mode input voltage range	V _{CC} = 5 V to MAX		25°C		0 to V _{CC} – 1.5			V
				Full range		0 to V _{CC} – 2			
V _{OH}	High-level output voltage	R _L = 2 kΩ		25°C		V _{CC} – 1.5			V
		R _L = 10 kΩ		25°C					
		V _{CC} = MAX	R _L = 2 kΩ	Full range		26			
			R _L ≥ 10 kΩ	Full range		27	28		
V _{OL}	Low-level output voltage	R _L ≤ 10 kΩ		Full range		5		20	mV
A _{VD}	Large-signal differential voltage amplification	V _{CC} = 15 V, V _O = 1 V to 11 V, R _L ≥ 2 kΩ		25°C		25	100		V/mV
				Full range		15			
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min		25°C		65	80		dB
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC} /ΔV _{IO})			25°C		65	100		dB
V _{O1} / V _{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C		120			dB
I _O	Output current	V _{CC} = 15 V, V _{ID} = 1 V, V _O = 0	Source	25°C		–20	–30	–60	mA
				Full range		–10			
		V _{CC} = 15 V, V _{ID} = –1 V, V _O = 15 V	Sink	25°C		10	20		
				Full range		5			
		V _{ID} = –1 V, V _O = 200 mV		25°C		12	30		μA
I _{OS}	Short-circuit output current	V _{CC} at 5 V, V _O = 0, GND at –5 V		25°C		±40		±60	mA
I _{CC}	Supply current (four amplifiers)	V _O = 2.5 V, no load		Full range		0.7		1.2	mA
		V _{CC} = MAX, V _O = 0.5 V _{CC} , no load		Full range		1.4		3	

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX V_{CC} for testing purposes is 30 V.

(2) Full range is 0°C to 70°C for LM324-MIL.

(3) All typical values are at $T_A = 25^\circ\text{C}$

6.6 Operating Conditions

$V_{CC} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 30\text{ pF}$, $V_I = \pm 10\text{ V}$ (see Figure 7)	0.5	V/ μs
B_1	Unity-gain bandwidth	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$ (see Figure 7)	1.2	MHz
V_n	Equivalent input noise voltage	$R_S = 100\text{ }\Omega$, $V_I = 0\text{ V}$, $f = 1\text{ kHz}$ (see Figure 8)	35	nV/ $\sqrt{\text{Hz}}$

6.7 Typical Characteristics

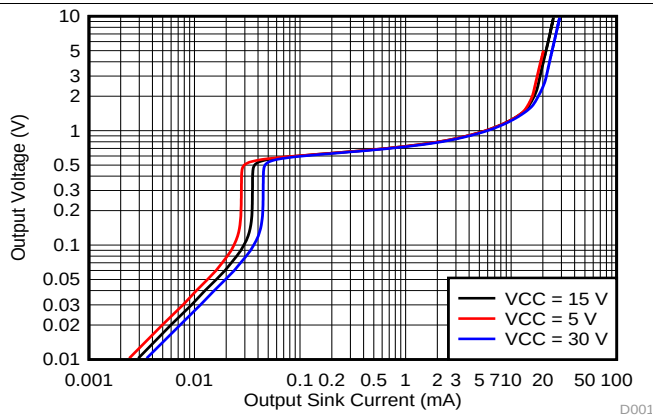


Figure 1. Output Sinking Characteristics

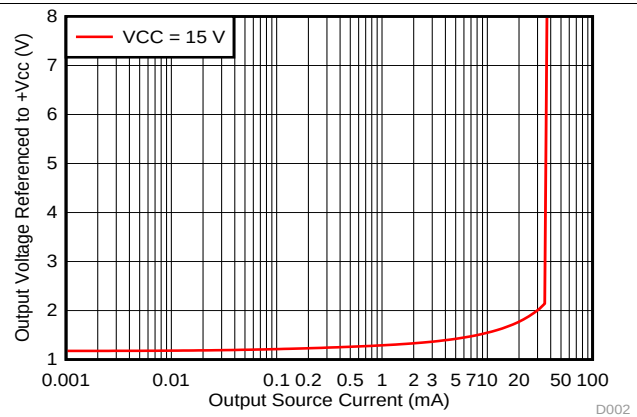


Figure 2. Output Sourcing Characteristics

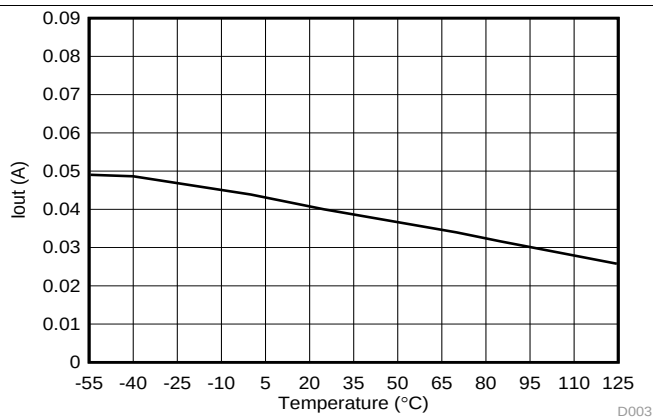


Figure 3. Source Current Limiting

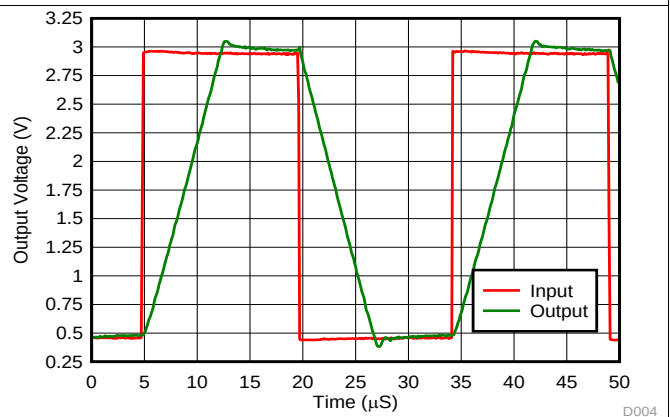


Figure 4. Voltage Follower Large Signal Response (50 pF)

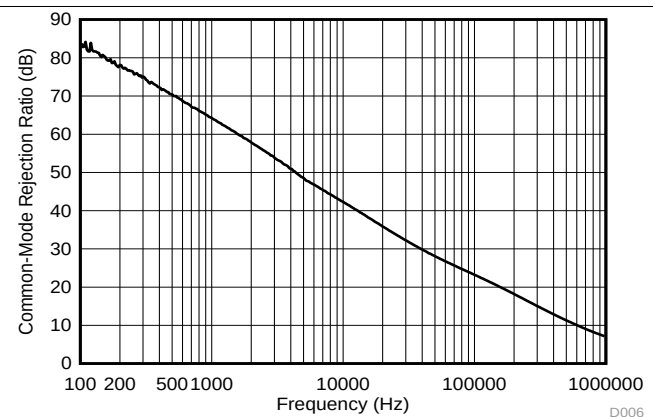


Figure 5. Common-Mode Rejection Ratio

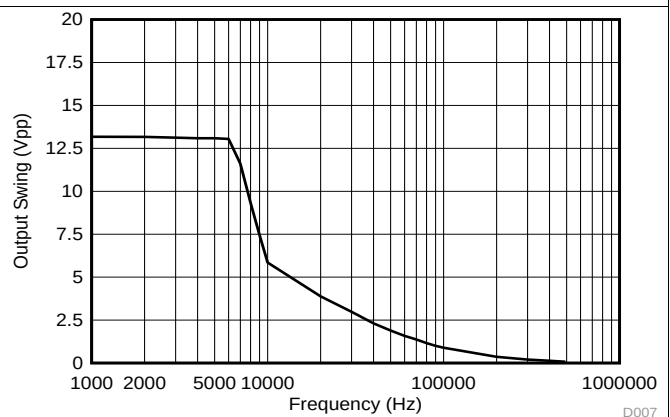


Figure 6. Maximum Output Swing vs. Frequency (VCC = 15 V)

7 Parameter Measurement Information

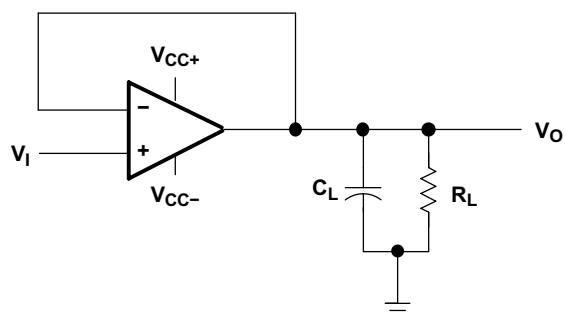


Figure 7. Unity-Gain Amplifier

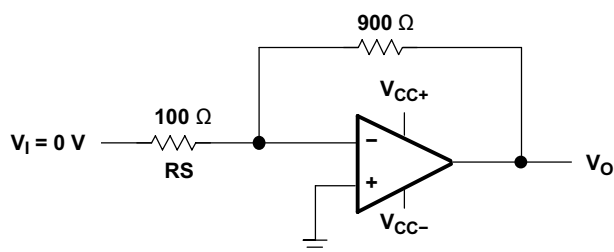


Figure 8. Noise-Test Circuit

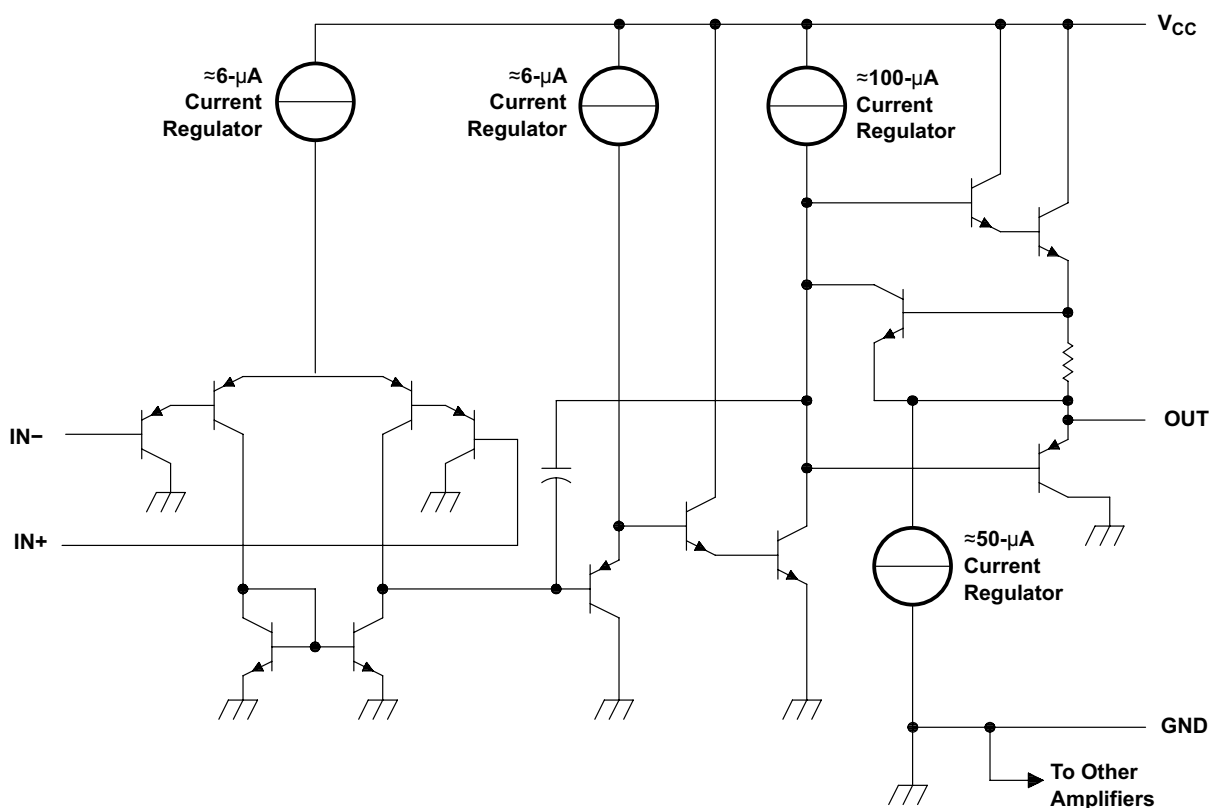
8 Detailed Description

8.1 Overview

The device consists of four independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is 3 V to 32 V, and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, DC amplification blocks, and all the conventional operational-amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM324-MIL device can be operated directly from the standard 5-V supply that is used in digital systems and provides the required interface electronics, without requiring additional ± 15 -V supplies.

8.2 Functional Block Diagram



COMPONENT COUNT (total device)	
Epi-FET	1
Transistors	95
Diodes	4
Resistors	11
Capacitors	4

8.3 Feature Description

8.3.1 Unity-Gain Bandwidth

Gain bandwidth product is found by multiplying the measured bandwidth of an amplifier by the gain at which that bandwidth was measured. These devices have a high gain bandwidth of 1.2 MHz.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5-V/ μ s slew rate.

8.3.3 Input Common Mode Range

The valid common mode range is from device ground to $V_{CC} - 1.5$ V ($V_{CC} - 2$ V across temperature). Inputs may exceed V_{CC} up to the maximum V_{CC} without device damage. At least one input must be in the valid input common mode range for output to be correct phase. If both inputs exceed valid range then output phase is undefined. If either input is less than -0.3 V then input current should be limited to 1 mA and output phase is undefined.

8.4 Device Functional Modes

The device is powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

9 Application and Implementation

NOTE

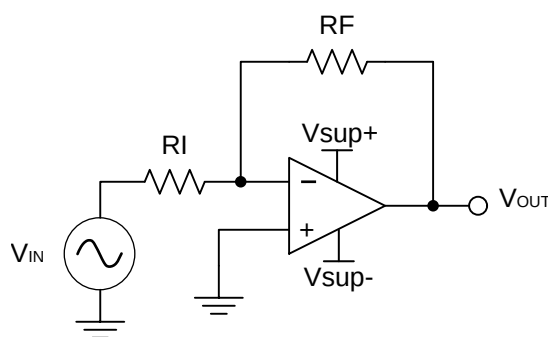
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM324-MIL operational amplifier is useful in a wide range of signal conditioning applications. Inputs can be powered before VCC for flexibility in multiple supply circuits.

9.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.



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Figure 9. Application Schematic

9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ± 0.5 V to ± 1.8 V. Setting the supply at ± 12 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for R_I or R_F . Choosing a value in the kilohm range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 k Ω for R_I which means 36 k Ω will be used for R_F . This was determined by [Equation 3](#).

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

Typical Application (continued)

9.2.3 Application Curve

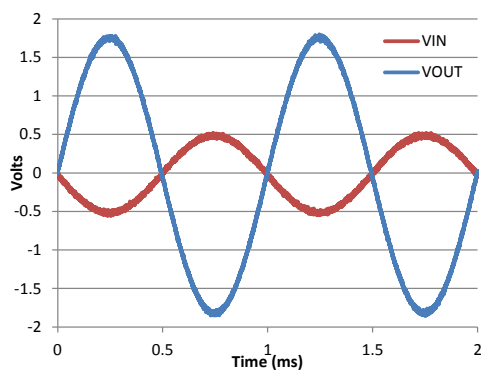


Figure 10. Input and Output Voltages of the Inverting Amplifier

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 32 V for a single supply, or outside the range of ± 16 V for a dual supply can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout](#).

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Examples](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Examples

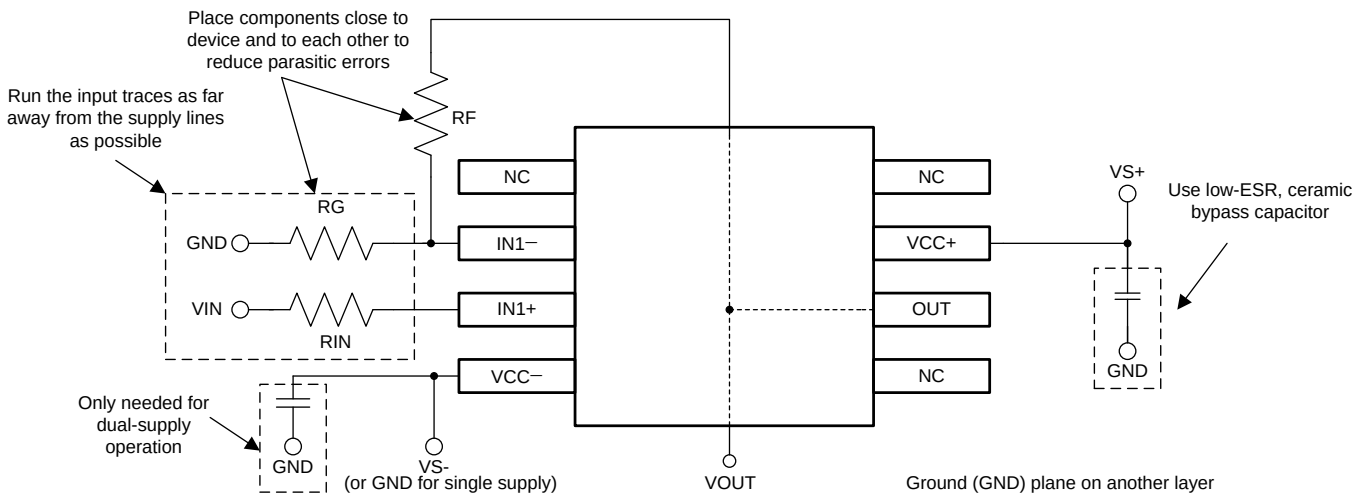


Figure 11. Operational Amplifier Board Layout for Noninverting Configuration

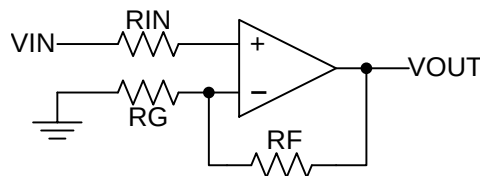


Figure 12. Operational Amplifier Schematic for Noninverting Configuration

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

[Circuit Board Layout Techniques](#), SLOA089

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM324 MWA	Active	Production	WAFERSALE (YS) 0	1 NOT REQUIRED	-	Call TI	Level-1-NA-UNLIM	-40 to 85	

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

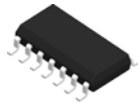
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

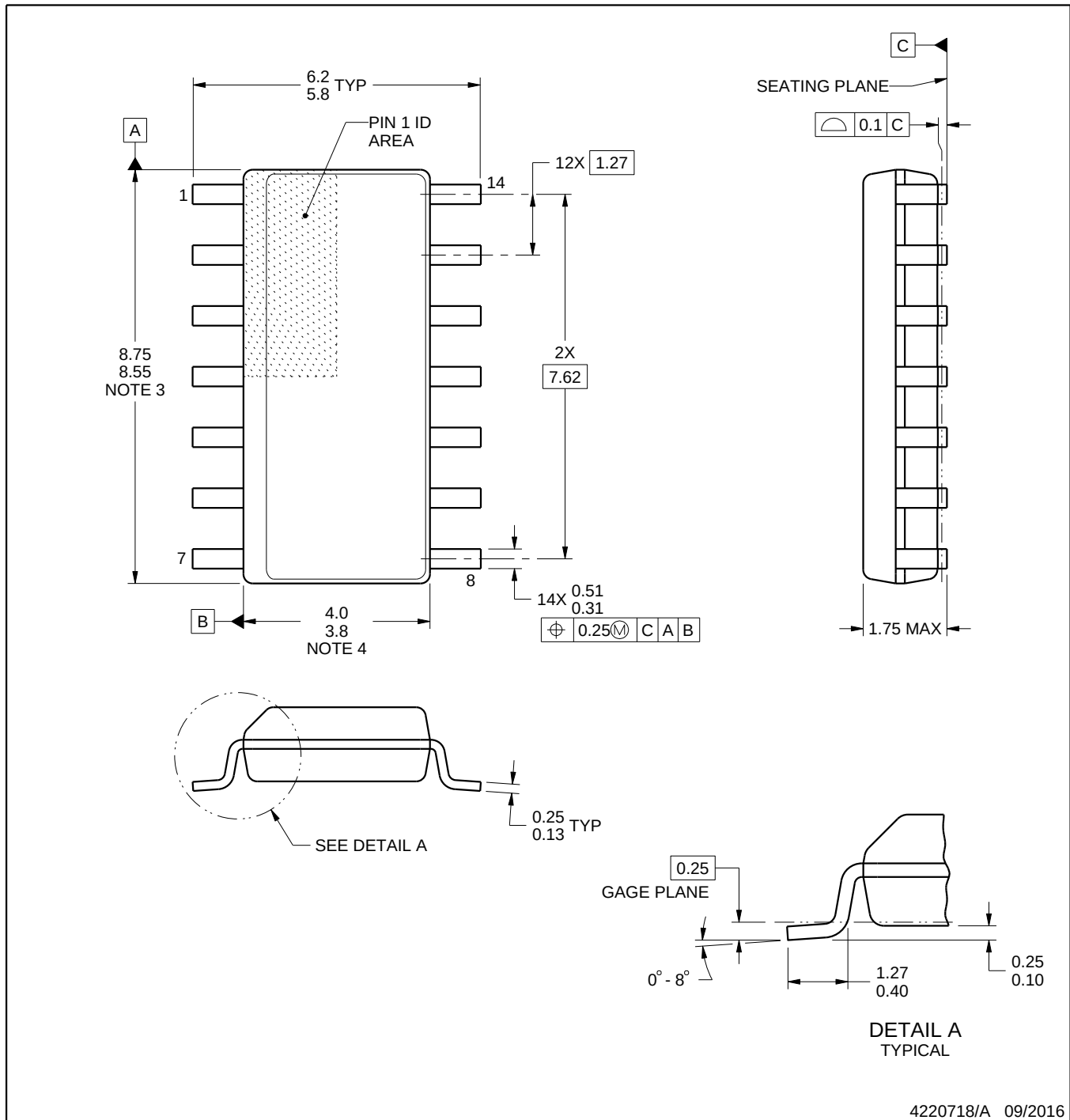
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

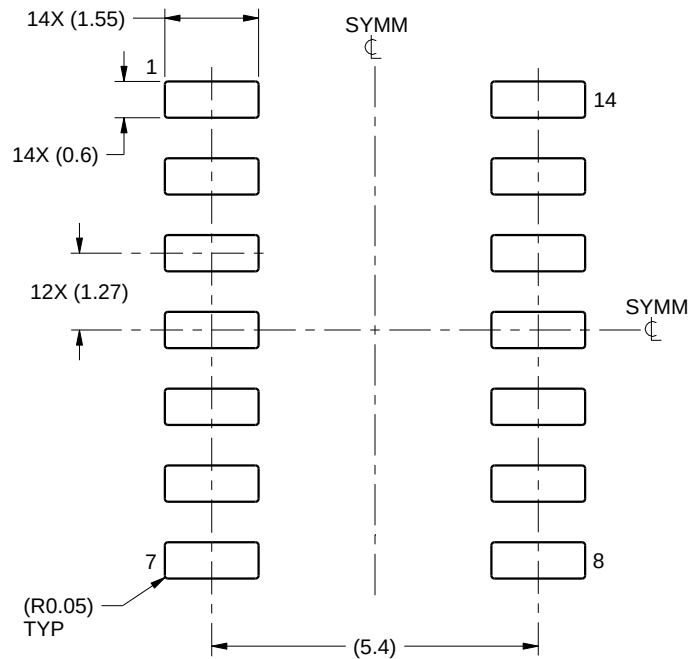
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

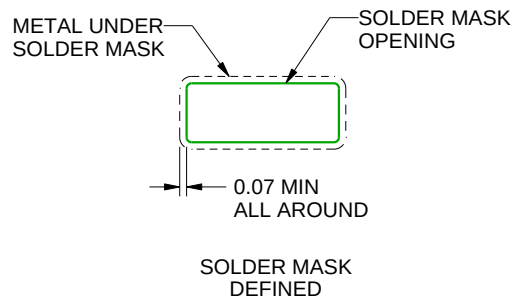
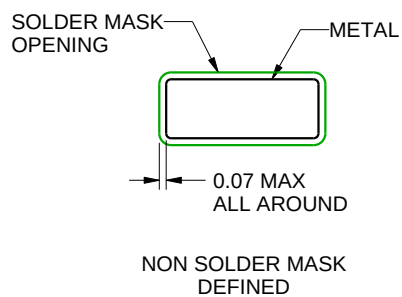
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

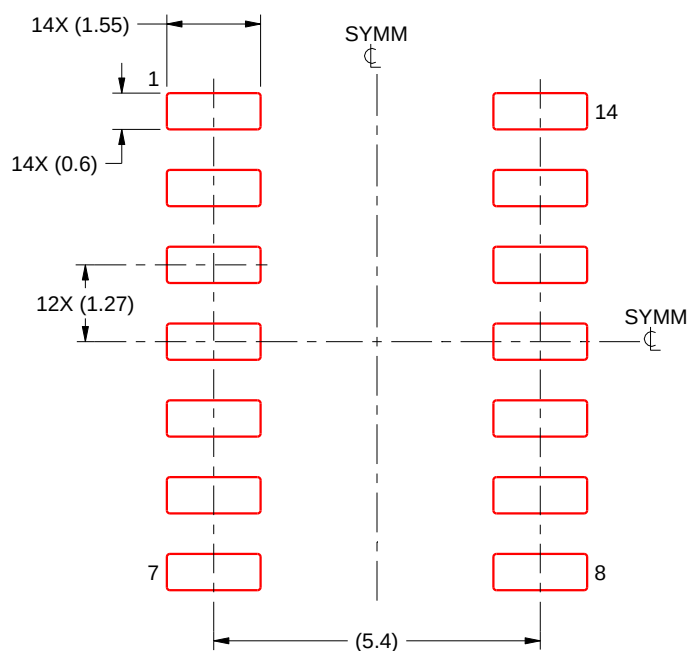
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

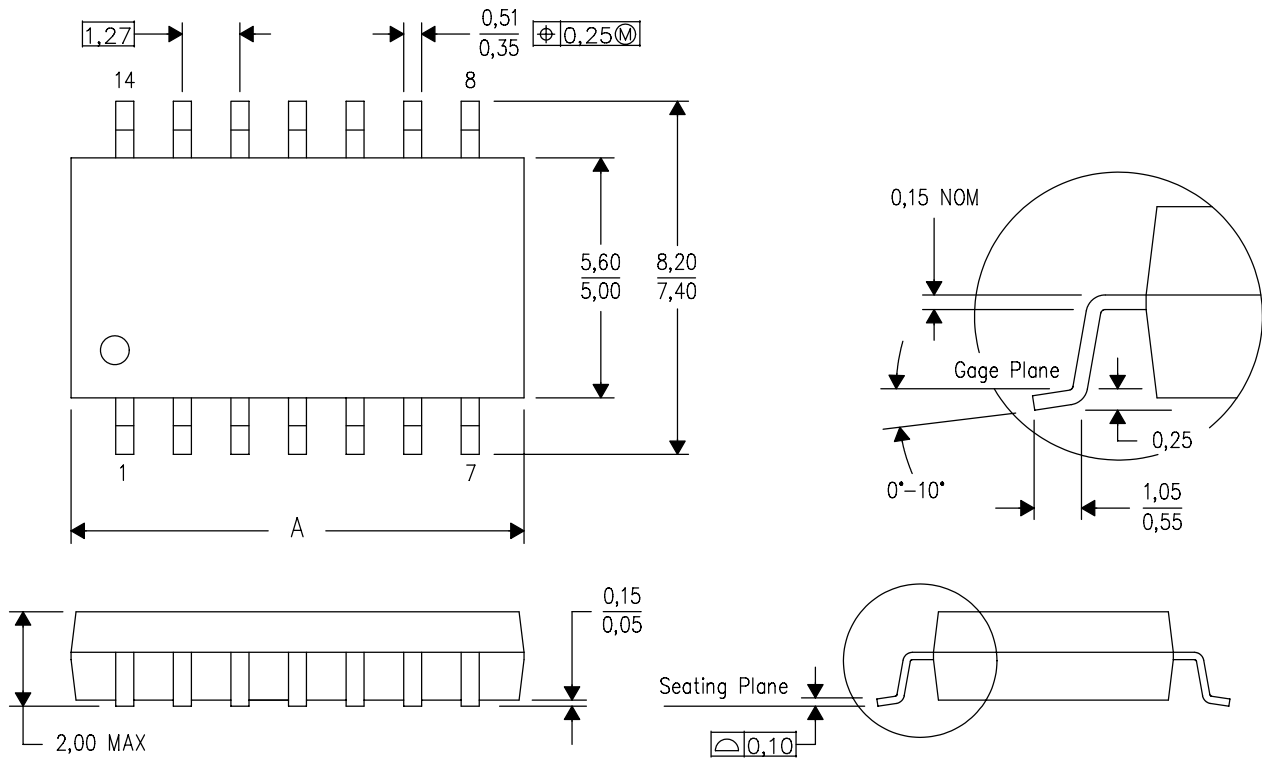
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



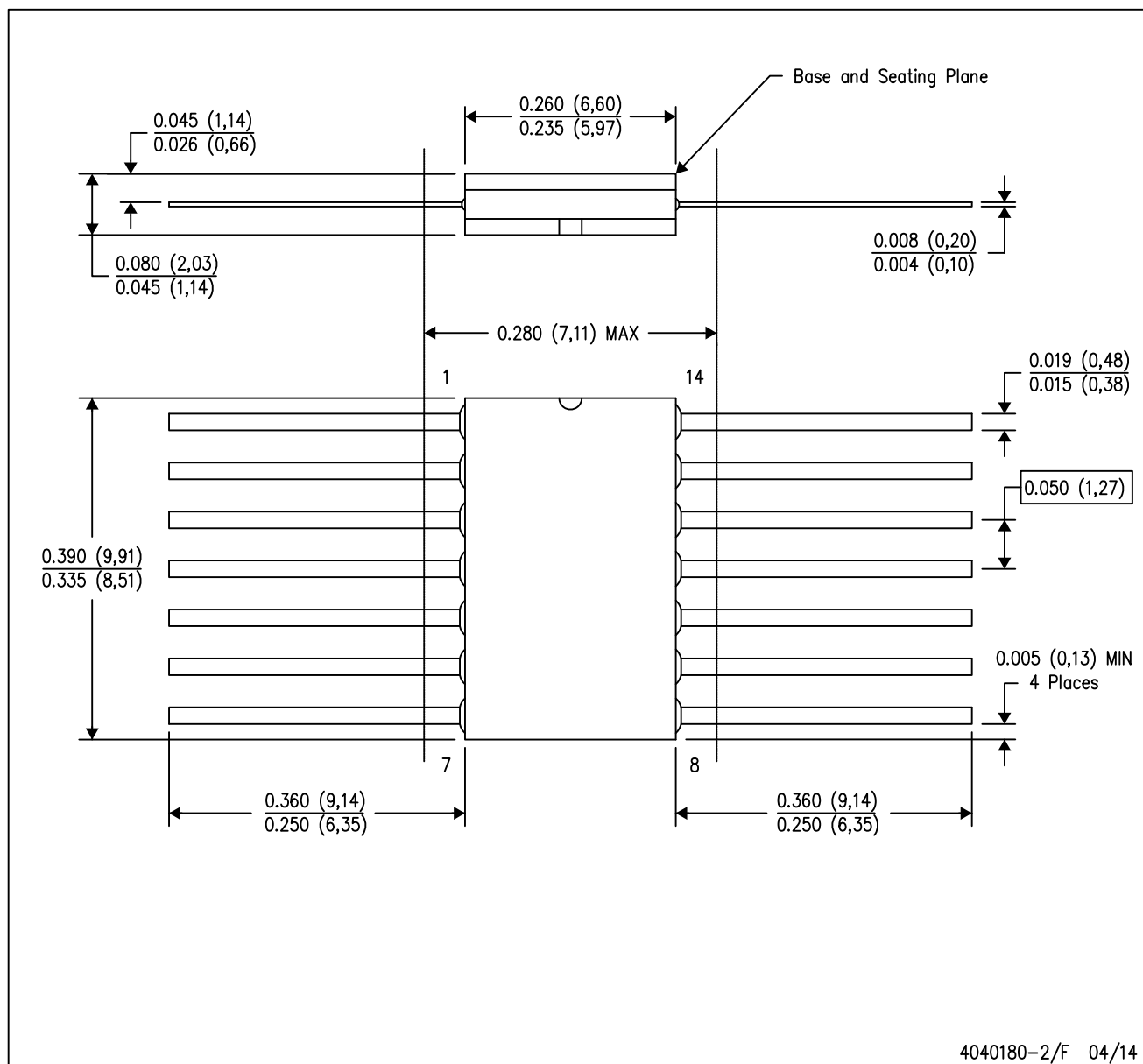
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

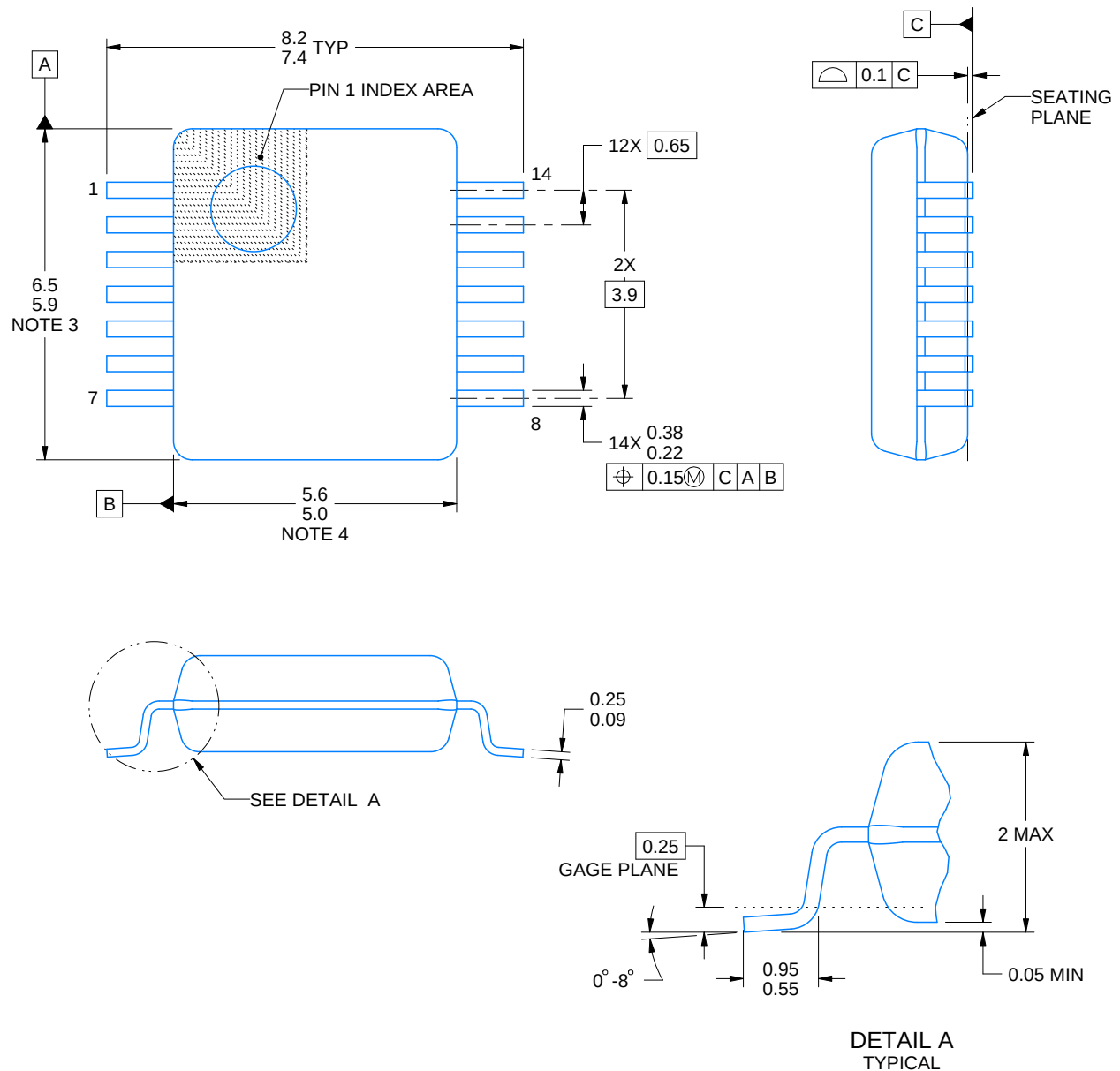
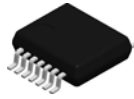
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK





4220762/A 05/2024

NOTES:

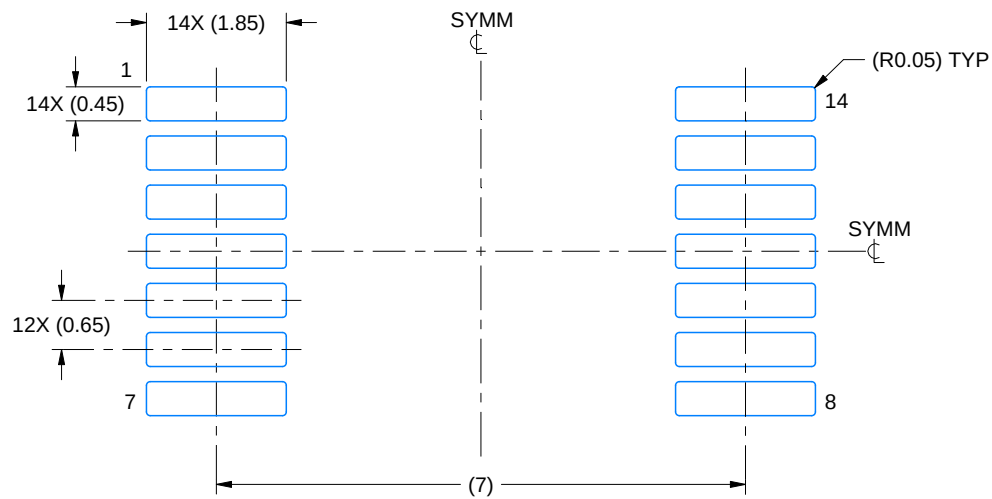
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

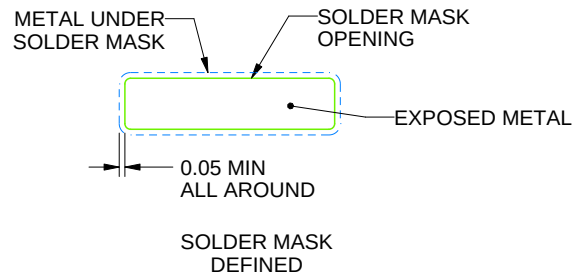
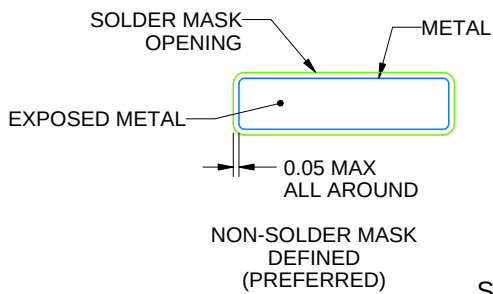
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

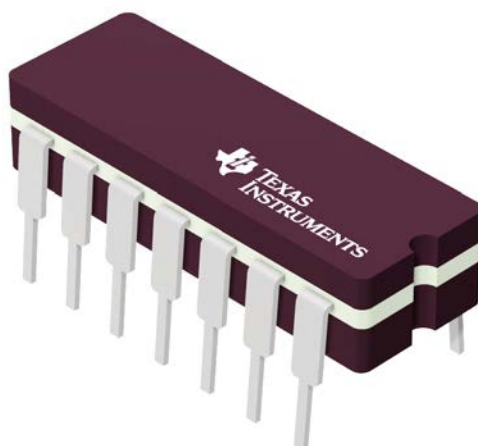
- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

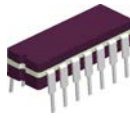
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

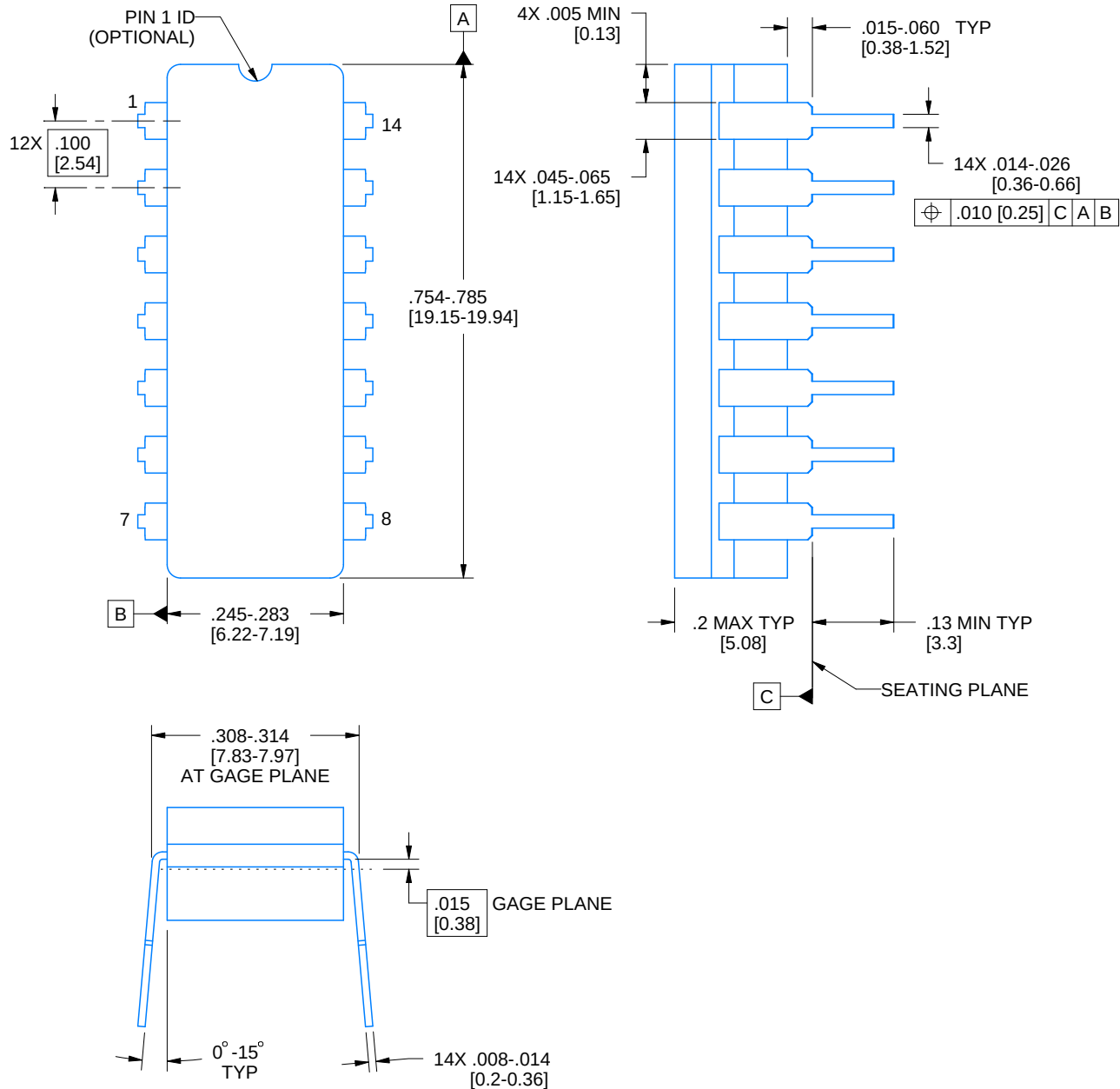
J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

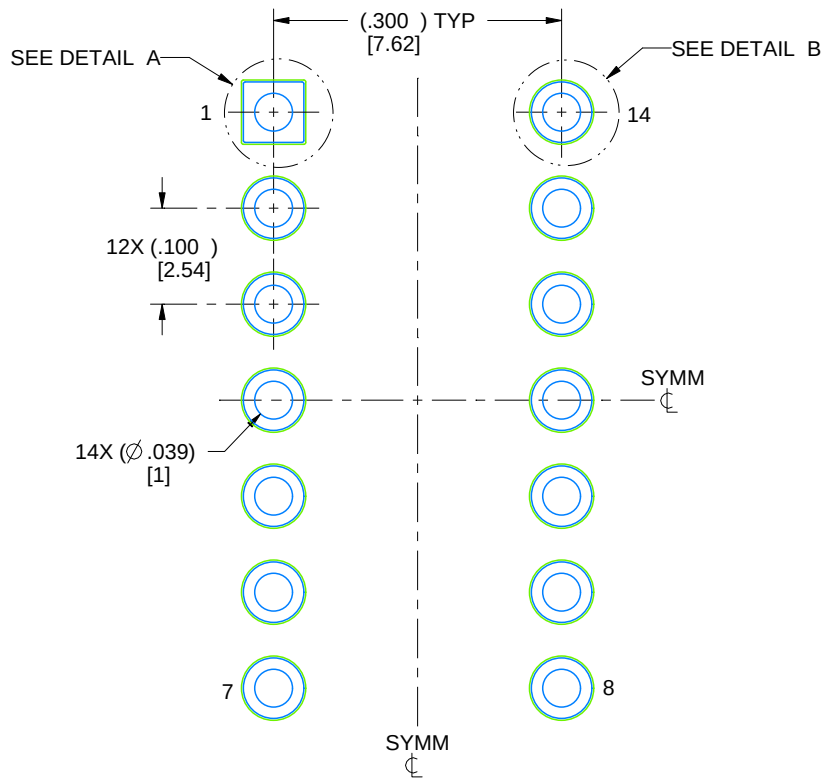
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

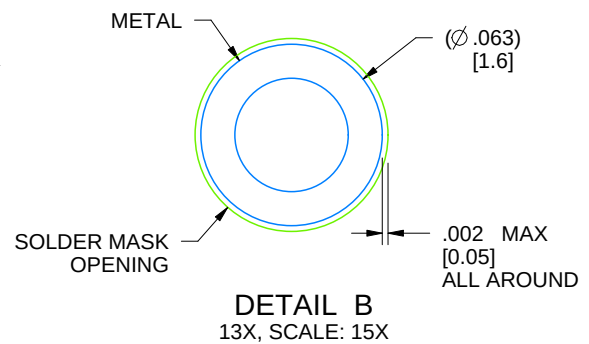
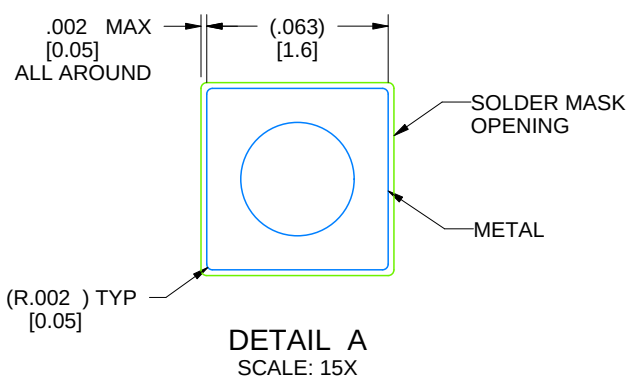
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

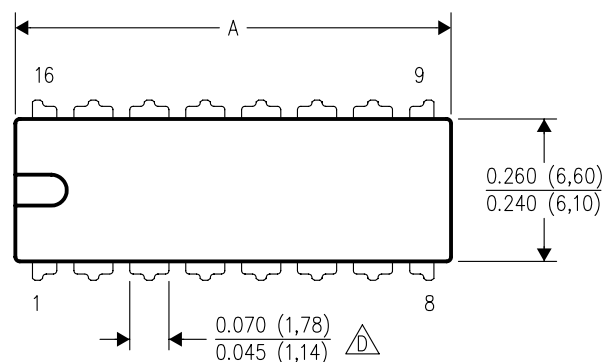


4214771/A 05/2017

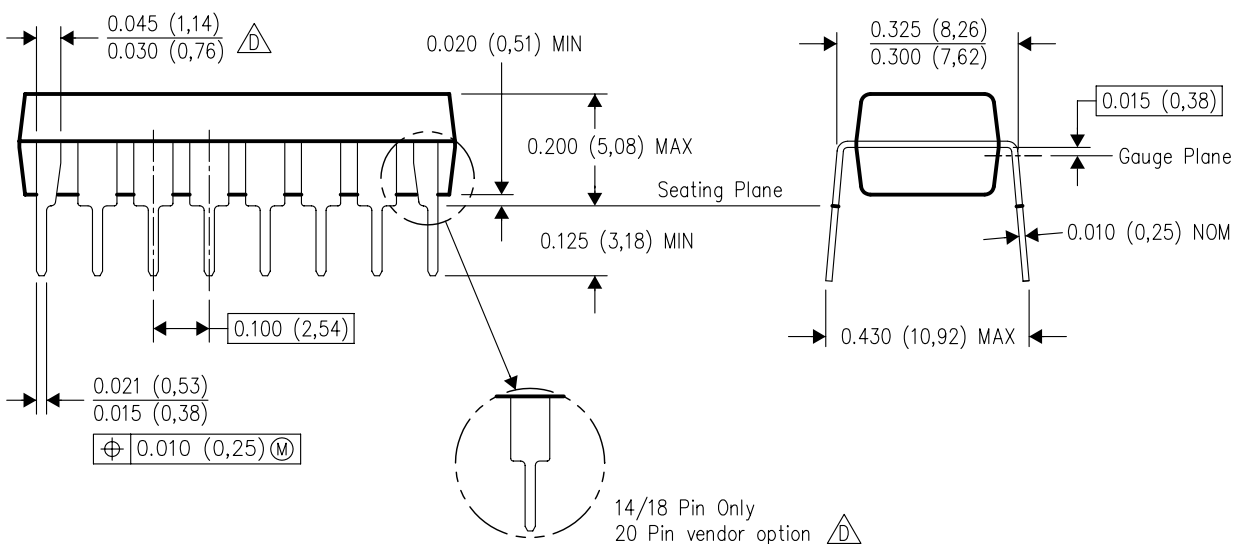
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



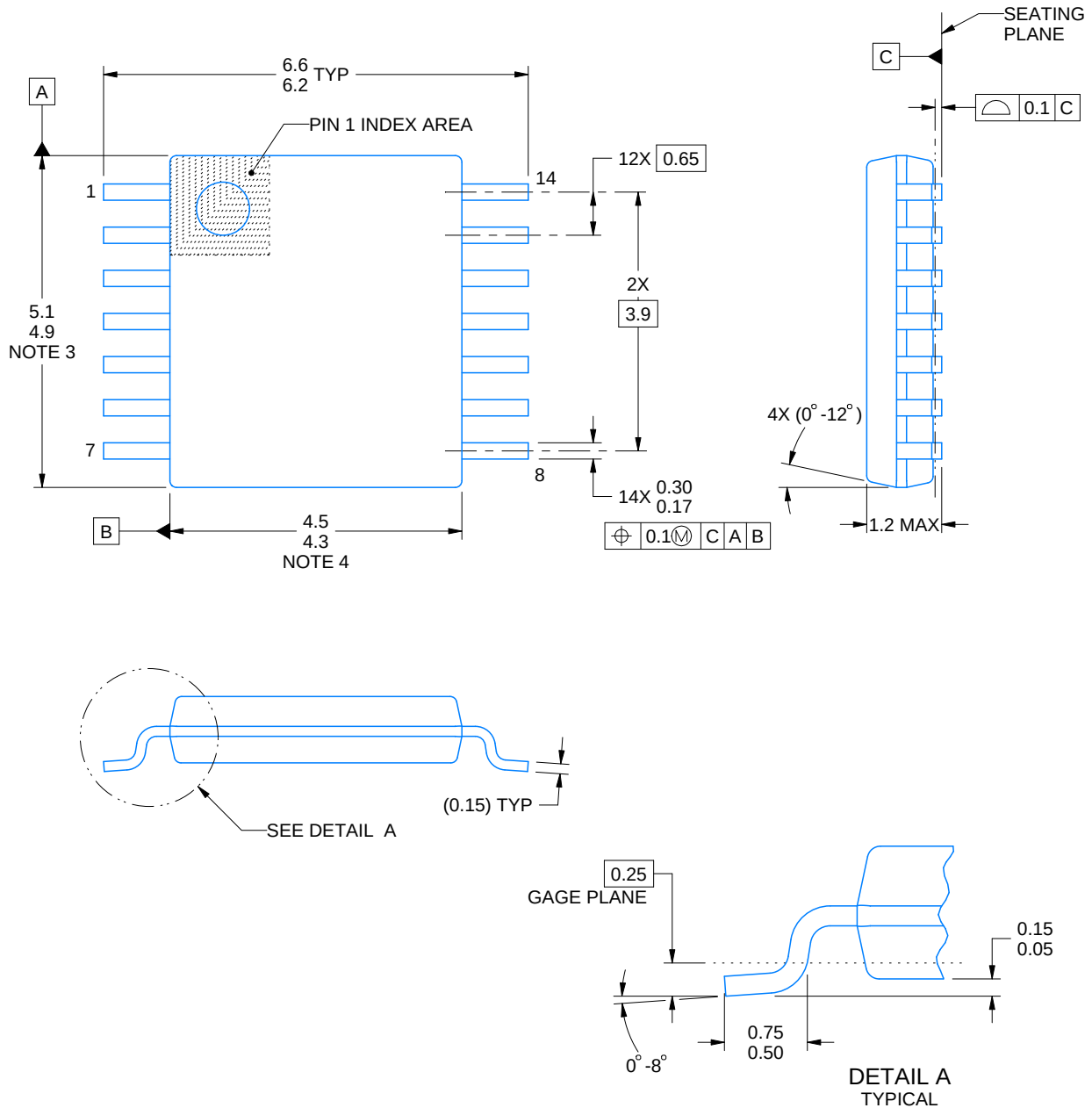
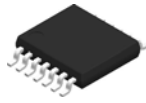
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220202/B 12/2023

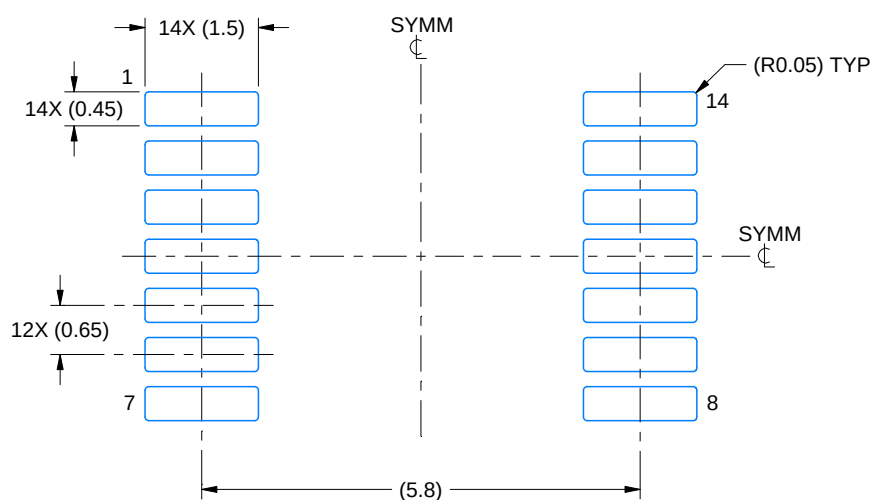
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

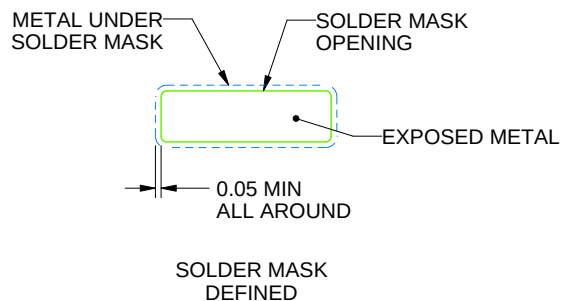
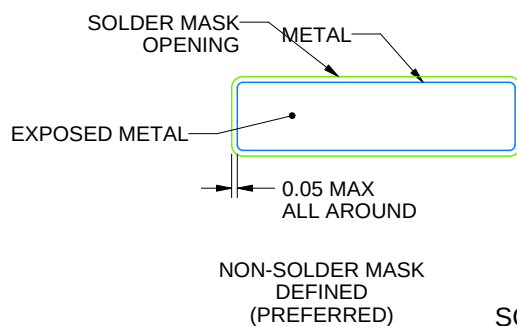
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

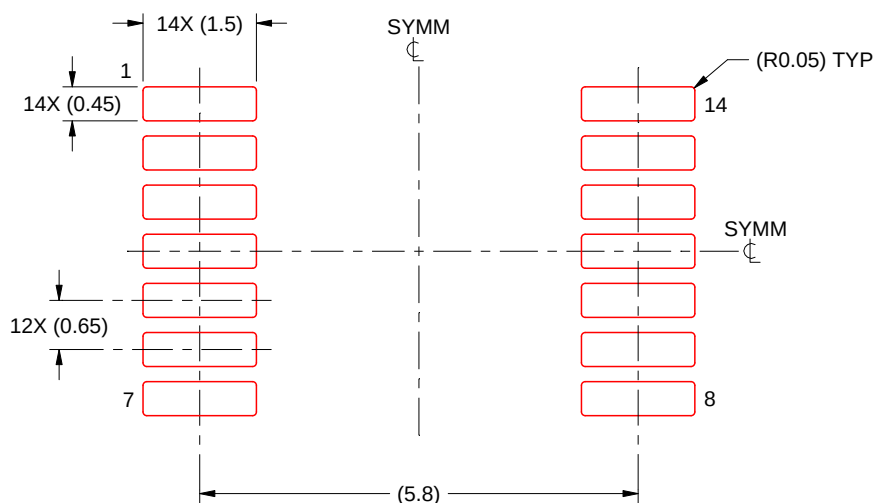
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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