TLC5954 48-Channel, Constant-Current LED Driver with Global Brightness Control, LED Open-Short Detection, and Power-Save Mode

1 Features

- 48 Constant-Current Sink Output Channels with On or Off Control
- Current Capability:
  - 34.9 mA for 32 Channels
  - 24.4 mA 16 Channels
- No External Resistor for Current Setting
- Maximum Current Control (MC): 3 Bits (8 Steps)
- Global Brightness Control (BC) for Each Color Group: 7 Bits (128 Steps), Three Groups
- LED Power-Supply Voltage: Up to 10 V
- VCC = 3.0 V to 3.6 V
- Constant-Current Accuracy:
  - Channel-to-Channel = ±1% (typ), ±3% (max)
  - Device-to-Device = ±2% (typ), ±4% (max)
- Data Transfer Rate: 30 MHz
- BLANK Pulse Duration: 40 ns (min)
- LED Open Detection (LOD)
- LED Short Detection (LSD)
- Power-Save Mode (PSM): 7-µA Consumption, High-Speed Recovery
- Undervoltage Lockout Sets Default Data
- Delayed Switching Minimizes Inrush Current
- Operating Temperature: –40°C to +85°C

2 Applications

- LED Video Displays
- Variable Message Signs (VMS)
- Illumination

3 Description

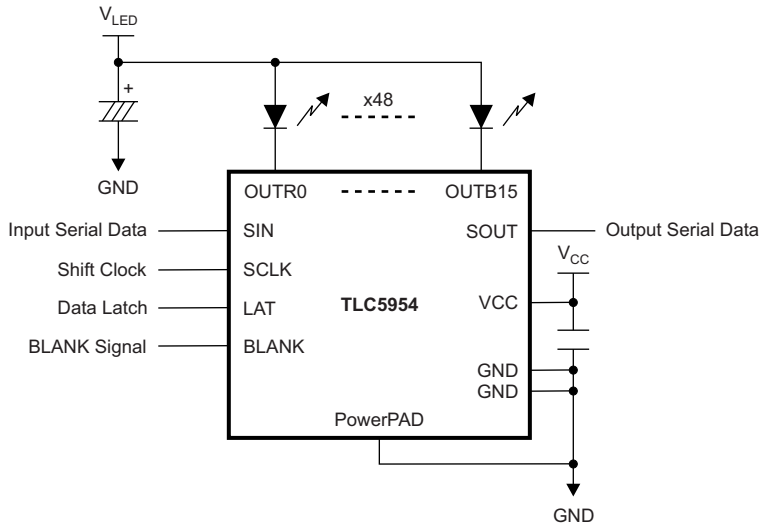
The TLC5954 is a 48-channel, constant-current sink LED driver. Each channel can be turned on or off by writing data to an internal register. The output channels (OUTX*n*) are grouped into three groups of 16 channels. Each channel group (R, G, and B) has a 128-step global brightness control (BC) function. The maximum current value of all 48 channels can be set with an 8-step maximum current control (MC) function. The device has two error flags: LED open detection (LOD) and LED short detection (LSD). The error flags can be read via a serial interface port. The device also has a power-save mode that sets the total current consumption to 7 µA (typ) when all outputs are off.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE
TLC5954	VQFN (56)	8 mm × 8 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Date	Revision	Notes
April 2014	*	Initial release.

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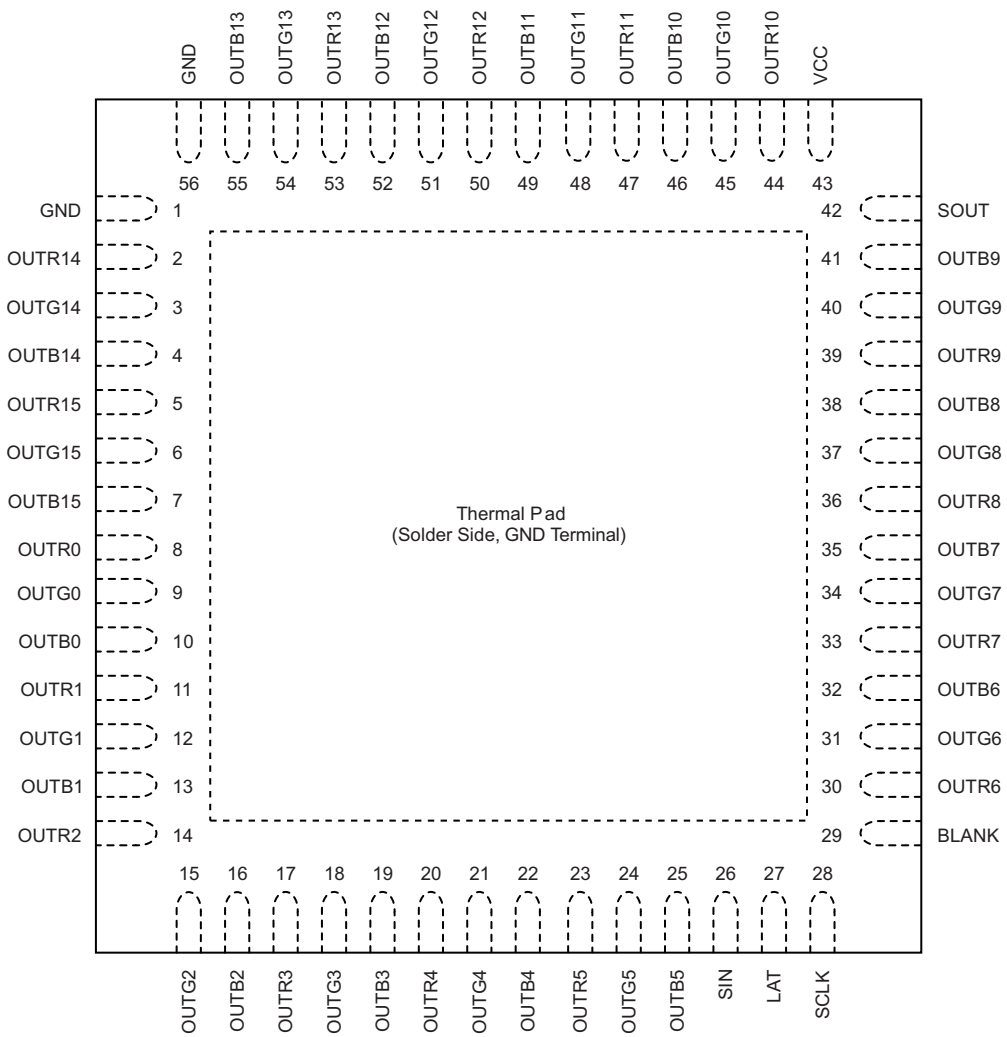
5 Pin Configuration and Functions

RTQ Package
VQFN-56
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1, 56	—	Ground. All GND pins are connected internally.
OUTR0 to OUTR15	2, 5, 8, 11, 14, 17, 20, 23, 30, 33, 36, 39, 44, 47, 50, 53	O	Red LED constant-current outputs (OUTR*n*). Multiple outputs can be tied together to increase the constant-current capability. Different voltages can be applied to each output. These outputs are turned on or off by the BLANK signal and the data in the output on or off control data latch.
OUTG0 to OUTG15	3, 6, 9, 12, 15, 18, 21, 24, 31, 34, 37, 40, 45, 48, 51, 54	O	Green LED constant-current outputs (OUTG*n*). Multiple outputs can be tied together to increase the constant-current capability. Different voltages can be applied to each output. These outputs are turned on or off by the BLANK signal and the data in the output on or off control data latch.
OUTB0 to OUTB15	4, 7, 10, 13, 16, 19, 22, 25, 32, 35, 38, 41, 46, 49, 52, 55	O	Blue LED constant-current outputs (OUTB*n*). Multiple outputs can be tied together to increase the constant-current capability. Different voltages can be applied to each output. These outputs are turned on or off by the BLANK signal and the data in the output on or off control data latch.
SIN	26	I	Serial data input of the 49-bit common shift register, Schmitt buffer input. When SIN is high, the LSB is set to 1 for only one SCLK input rising edge. If two SCLK rising edges are input while SIN is high, then the 49-bit shift register LSB and LSB+1 are set to 1. When SIN is low, the LSB is set to 0 at the SCLK input rising edge.
LAT	27	I	Edge-triggered latch, Schmitt buffer input. The LAT rising edge latches data from the common shift register either into the output on or off data latch or the maximum current control (MC), brightness control (BC), or function control (FC) data latch. When the common shift register data are latched into the on or off data latch, data in the common shift register are simultaneously replaced with SID, which is selected by SIDLD. Refer to the *Output On or Off Data Latch* and *Status Information Data (SID)* sections for more details.
SCLK	28	I	Serial data shift clock, Schmitt buffer input. Data present on SIN are shifted to the 49-bit common shift register LSB with the SCLK rising edge. Data in the shift register are shifted towards the MSB at each SCLK rising edge. The common shift register MSB appears on SOUT.
BLANK	29	I	Blank all outputs, Schmitt buffer input. When BLANK is high, all constant-current outputs (OUTX*n*) are forced off. When BLANK is low, all OUTX*n* are controlled by the on or off control data in the data latch.
SOUT	42	O	Serial data output of the 49-bit common shift register. SOUT is connected to the MSB of the register. Data are clocked out at the SCLK rising edge.
VCC	43	—	Power-supply voltage
Thermal pad		—	Ground. The thermal pad must be connected to GND on the printed circuit board (PCB).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
VCC	Supply voltage[(2)]		–0.3	4.0	V
V_{IN}	Input voltage range	SIN, SCLK, LAT, BLANK	–0.3	V_{CC} + 0.3	V
V_{OUT}	Output voltage range	SOUT	–0.3	V_{CC} + 0.3	V
		OUTR0 to OUTR15, OUTG0 to OUTG15, OUTB0 to OUTB15	–0.3	11	V
T_J (max)	Operating junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to device ground pin.

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6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–200	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

At T_A= –40°C to +85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DC CHARACTERISTICS (VCC = 3 V to 3.6 V)						
V_{CC}	Supply voltage		3.0		3.6	V
V_O	Voltage applied to output	OUTR0 to OUTR15, OUTG0 to OUTG15, OUTB0 to OUTB15			10	V
V_{IH}	High-level input voltage	SIN, SCLK, LAT, BLANK	0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	SIN, SCLK, LAT, BLANK	GND		0.3 × V_{CC}	V
I_{OH}	High-level output current	SOUT			–2	mA
I_{OL}	Low-level output current	SOUT			2	mA
T_A	Operating free-air temperature range		–40		+85	°C
T_J	Operating junction temperature range		–40		+125	°C
AC CHARACTERISTICS (VCC = 3 V to 3.6 V)						
$f_{CLK\ (SCLK)}$	Data shift clock frequency	SCLK			30	MHz
t_{WH0}	Pulse duration	SCLK	10			ns
t_{WL0}		SCLK	10			ns
t_{WH1}		LAT	15			ns
t_{WH2}		BLANK	60			ns
t_{WL2}		BLANK	40			ns
t_{SU0}	Setup time	SIN to SCLK↑	4			ns
t_{SU1}		LAT↓ to SCLK↑	20			ns
t_{SU2}		SCLK↑ resumes normal mode, BLANK↓, PSMODE bit = 01b	12			µs
t_{SU3}		LAT↑ for all data latching except all 0s resumes normal mode, BLANK↓, PSMODE bit = 10b	12			µs
t_{H0}	Hold time	SCLK↑ to SIN	3			ns
t_{H1}		SCLK↑ to LAT↑	10			ns

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6.4 Thermal Information

THERMAL METRIC[1]		TLC5954 RTQ (VQFN) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	16.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	7.7	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	7.7	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = –40°C to +85°C and V_{CC} = 3.0 V to 3.6 V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA at SOUT		V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA at SOUT				0.4	V
V_{LOD0}	LED open-detection threshold	LODVLT = 000b		0.15	0.20	0.25	V
V_{LOD1}		LODVLT = 001b, 101b, 110b, 111b		0.25	0.30	0.35	V
V_{LOD2}		LODVLT = 010b		0.35	0.40	0.45	V
V_{LOD3}		LODVLT = 011b		0.45	0.50	0.55	V
V_{LOD4}		LODVLT = 100b		0.55	0.60	0.65	V
V_{LSD0}	LED short-detection threshold	LSDVLT = 00b		0.45 × V_{CC}	0.50 × V_{CC}	0.55 × V_{CC}	V
V_{LSD1}		LSDVLT = 01b		0.65 × V_{CC}	0.70 × V_{CC}	0.75 × V_{CC}	V
V_{LSD2}		LSDVLT = 10b, 11b		0.85 × V_{CC}	0.90 × V_{CC}	0.95 × V_{CC}	V
I_{IN}	Input current	V_{IN} = V_{CC} or GND at SIN, SCLK, LAT, and BLANK		–1		1	µA
I_{CC0}	Supply current (V_{CC})	SIN, SCLK, LAT = GND, BLANK = VCC, V_{OUTXn} = 1 V, BCX = 7Fh, MC = 0h (I_{OUTRn}, I_{OUTGn} = 2.9-mA target, I_{OUTBn} = 2.0-mA target)[1]			15	19	mA
I_{CC1}		SIN, SCLK, LAT = GND, BLANK = VCC, V_{OUTXn} = 1 V, BCX = 7Fh, MC = 5h (I_{OUTRn}, I_{OUTGn} = 17.4-mA target, I_{OUTBn} = 12.2-mA target)			17.5	22	mA
I_{CC2}		SIN, SCLK, LAT, BLANK = GND, all OUTX*n* = on, V_{OUTXn} = 1 V, BCX = 7Fh, MC = 5h			17.5	22	mA
I_{CC3}		SIN, SCLK, LAT, BLANK = GND, all OUTX*n* = on, V_{OUTXn} = 1 V, BCX = 7Fh, MC = 7h (I_{OUTRn}, I_{OUTGn} = 34.9-mA target, I_{OUTBn} = 24.4-mA target)			20.5	25.5	mA
I_{CC4}		In power-save mode, SIN, SCLK, LAT = GND, BLANK = VCC			7	60	µA
I_{OLC0}	Constant output current	All OUTX*n* = on, V_{OUTXn} = V_{OUTfix} = 1 V, BC = 7Fh, MC = 7h, at OUTR0 to OUTR15 and OUTG0 to OUTG15		32.5	34.9	37.3	mA
I_{OLC1}		All OUTX*n* = on, V_{OUTXn} = V_{OUTfix} = 1 V, BC = 7Fh, MC = 7h, at OUTB0 to OUTB15		22.7	24.4	26.1	mA
I_{OLKG}	Output leakage current	BLANK = VCC, V_{OUTXn} = V_{OUTfix} = 10 V, MC = 7h, at OUTX*n*	T_J = +25°C			0.1	µA
			T_J = +85°C			0.2	µA
			T_J = +125°C			0.5	µA
ΔI_{OLC0}	Constant-current error (channel-to-channel)[2]	All OUTX*n* = on, BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 1 V, MC = 7h, at same color group (OUTX*n*)			±1%	±3%	

(1) X = R, G, and B. n = 0 to 15.
(2) The deviation of each output in the same color group (OUTR*n*, OUTG*n*, OUTB*n*) from the average of the same OUTX*n* group constant-current. Deviation is calculated by the formula:

$$\Delta\,(\%) = \left(\frac{I_{OUTXn}}{\left(\frac{I_{OUTX0} + I_{OUTX1} + \ldots + I_{OUTX14} + I_{OUTX15}}{16} \right)} - 1 \right) \times 100$$

, where X = R, G, or B, and n = 0 to 15.

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Electrical Characteristics (continued)

At T_A = –40°C to +85°C and V_{CC} = 3.0 V to 3.6 V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔI_{OLC1}	Constant-current error (device-to-device)(3)	All OUTX*n* = on, BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 1 V, MC = 7h, at same color group (OUTX*n*)		±0.5%	±3%	
ΔI_{OLC2}	Line regulation(4)	All OUTX*n* = on, BCX = 7Fh, V_{OUTXn} = V_{OUTfix} = 1 V, MC = 7h, at OUTX*n*		±0.5	±1	%/V
ΔI_{OLC3}	Load regulation(5)	All OUTX*n* = on, BCX = 7Fh, V_{OUTXn} = 1 V to 3 V, V_{OUTfix} = 1 V, MC = 7h, at OUTX*n*		±1	±3	%/V

(3) The deviation of the OUTX*n* constant-current average from the ideal constant-current value. Deviation is calculated by the formula:

$$\Delta\,(\%) = \left(\frac{\left[\dfrac{I_{OUTX0} + I_{OUTX1} + \ldots + I_{OUTX15}}{16}\right] - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is 34.9 mA for OUTR*n* and OUTG*n*. Ideal current is 24.4 mA for OUTB*n* with MC data equal to 7h.
, where X = R, G, or B, and n = 0 to 15.

(4) Line regulation is calculated by the formula:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTXn} \text{ at VCC = 3.6 V}) - (I_{OUTXn} \text{ at VCC = 3.0 V})}{I_{OUTXn} \text{ at VCC = 3.0 V}} \right) \times \frac{100}{3.6\text{ V} - 3.0\text{ V}}$$

X = R, G, or B. n = 0 to 15.

(5) Load regulation is calculated by the equation:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTXn} \text{ at } V_{OUTXn} = 3\text{ V}) - (I_{OUTXn} \text{ at } V_{OUTXn} = 1\text{ V})}{I_{OUTXn} \text{ at } V_{OUTXn} = 1\text{ V}} \right) \times \frac{100}{3\text{ V} - 1\text{ V}}$$

, where X = R, G, or B, and n = 0 to 15.

6.6 Switching Characteristics

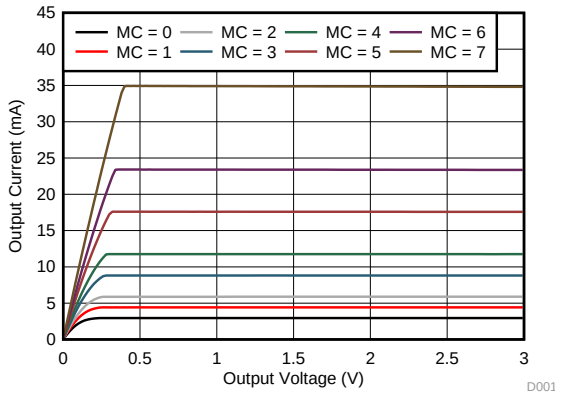
At T_A = –40°C to +85°C, V_{CC} = 3.0 V to 3.6 V, C_L = 15 pF, R_L = 100 Ω for OUTR*n* and OUTG*n*, R_L = 150 Ω for OUTB*n*, MC = 7h, and V_{LED} = 4.5 V, unless otherwise noted. Typical values at T_A = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{R0}	Rise time	SOUT		2	5	ns
t_{R1}		OUTX*n*, BCX = 7Fh(1)		20	50	ns
t_{F0}	Fall time	SOUT		2	5	ns
t_{F1}		OUTX*n*, BCX = 7Fh		20	50	ns
t_{D0}	Propagation delay(2)	SCLK↑ to SOUT		13	23	ns
t_{D1}		LAT↑ to OUTR0 on to off or OUTR0 off to on, BCX = 7Fh		30	60	ns
t_{D2}		BLANK↓↑ to OUTR0 on to off or OUTR0 off to on, BCX = 7Fh		30	60	ns
t_{D3}		OUTR*n* on to OUTG*n* on, OUTG*n* on to OUTB*n* on, and OUTB*n* on to the next OUTR*n* on, BCX = 7Fh		1.5	5	ns
t_{D4}		OUTR*n* off to OUTG*n* off, OUTG*n* off to OUTB*n* off, and OUTB*n* off to the next OUTR*n* off, BCX = 7Fh		1.5	5	ns
t_{D5}		LAT↑ to power-save mode by writing data for all OUTXn off		150	300	ns
t_{ON_ERR}	Output on-time error(3)	OUTXn on or off data = all 1s, BCX = 7Fh, 40-ns BLANK low-level one-shot pulse input	–35		35	ns

(1) X = R, G, or B. n = 0 to 15.
(2) t_{D3} (OUTR*n* on to OUTG*n* on, OUTG*n* on to OUTB*n* on, and OUTB*n* on to the next OUTR*n* on) and t_{D4} (OUTR*n* off to OUTG*n* off, OUTG*n* off to OUTB*n* off, and OUTB*n* off to the next OUTR*n* off) are calculated by:
t_{D3} (ns) = (the propagation delay between OUTR0 on to OUTB7 on) / 47 and
t_{D4} (ns) = (the propagation delay between OUTR0 off to OUTB7 off) / 47.
(3) Output on-time error (t_{ON_ERR}) is calculated by the formula: t_{ON_ERR} (ns) = t_{OUT_ON} – BLANK low-level pulse duration.
t_{OUT_ON} is the actual on-time of OUTX*n*.

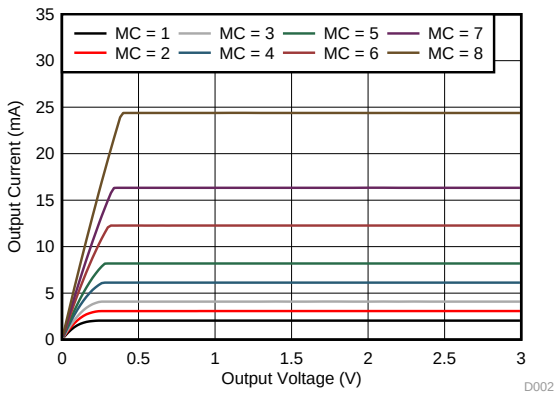
6.7 Typical Characteristics

At T_A = +25°C and VCC = 3.3 V, unless otherwise noted.



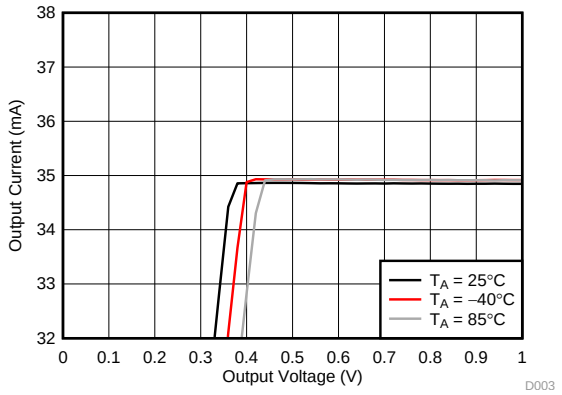
BCR, BCG = 7Fh

Figure 1. Output Current vs Output Voltage (OUTR*n*, OUTG*n*)



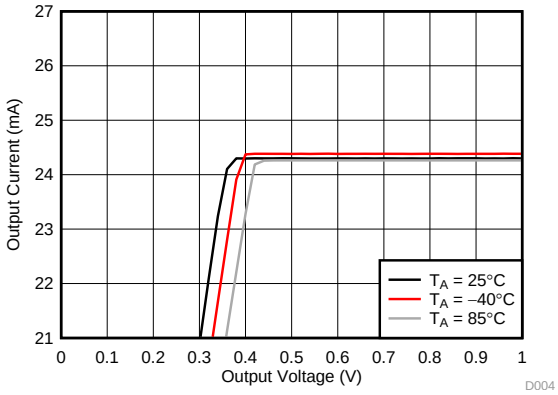
BCB = 7Fh

Figure 2. Output Current vs Output Voltage (OUTB*n*)



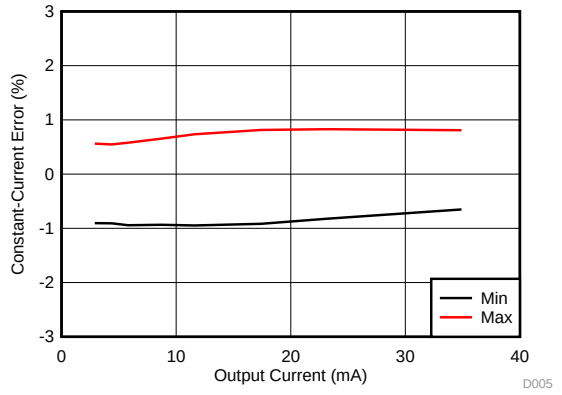
BCR = BCG = 7Fh MC = 7

Figure 3. Output Current vs Output Voltage (OUTR*n*, OUTG*n*)



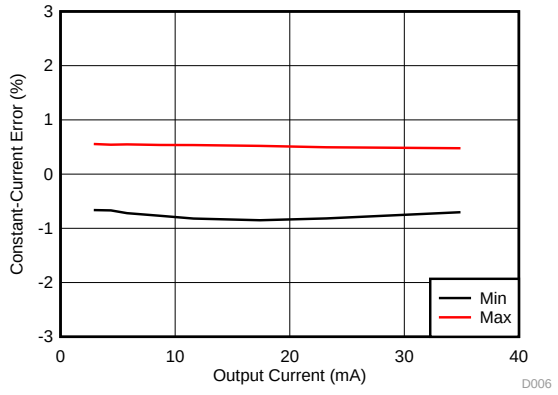
BCB = 7Fh MC = 7

Figure 4. Output Current vs Output Voltage (OUTB*n*)



BCR = 7Fh MC = 7

Figure 5. Constant-Current Error vs Output Current (Channel-to-Channel, OUTR*n*)



BCG = 7Fh MC = 7

Figure 6. Constant-Current Error vs Output Current (Channel-to-Channel, OUTG*n*)

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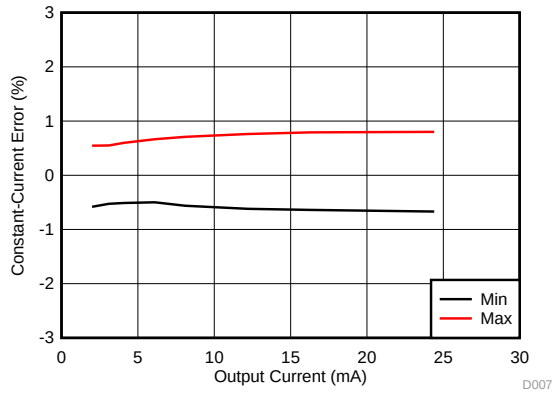
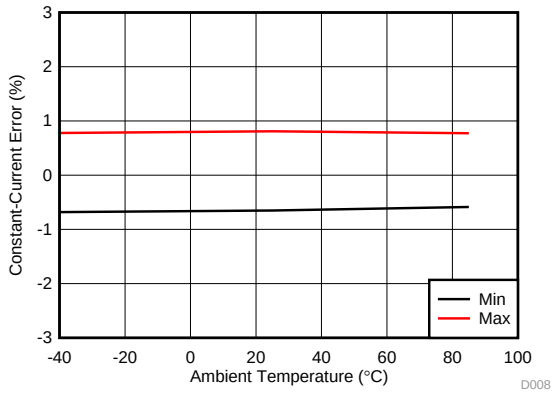
Typical Characteristics (continued)

At T_A = +25°C and VCC = 3.3 V, unless otherwise noted.



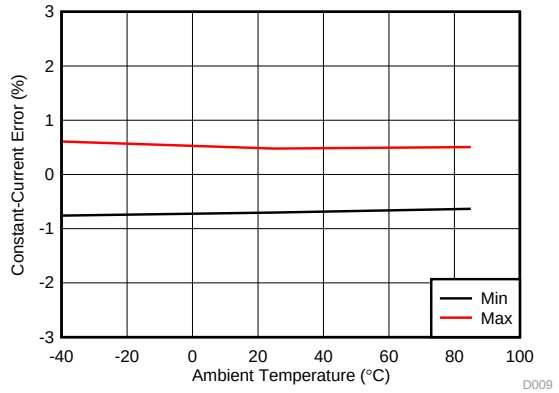
BCB = 7Fh MC = 7

Figure 7. Constant-Current Error vs Output Current (Channel-to-Channel, OUTB*n*)



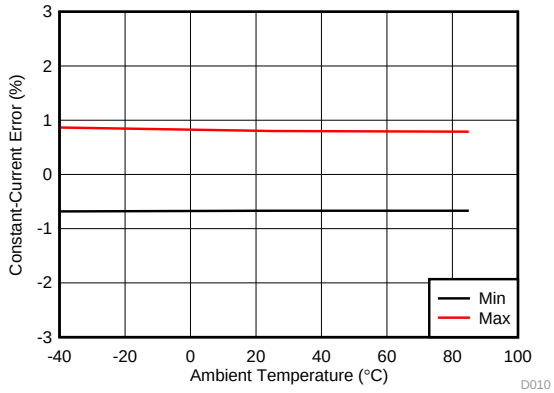
BCR = 7Fh MC = 7h

Figure 8. Constant-Current Error vs Ambient Temperature (Channel-to-Channel, OUTR*n*)



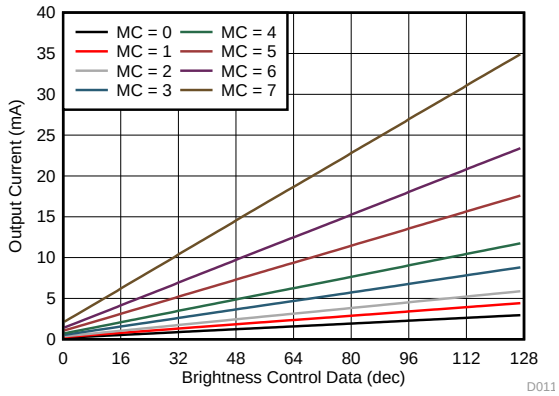
BCG = 7Fh MC = 7h

Figure 9. Constant-Current Error vs Ambient Temperature (Channel-to-Channel, OUTG*n*)



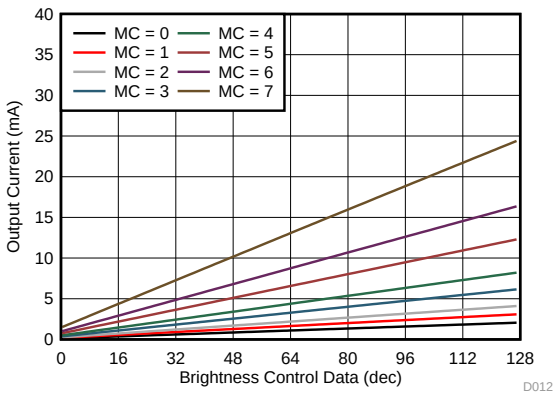
BCB = 7Fh MC = 7

Figure 10. Constant-Current Error vs Ambient Temperature (Channel-to-Channel, OUTB*n*)



BCR = BCG = 7Fh

Figure 11. Global Brightness Control Linearity (OUTR*n*, OUTG*n*)

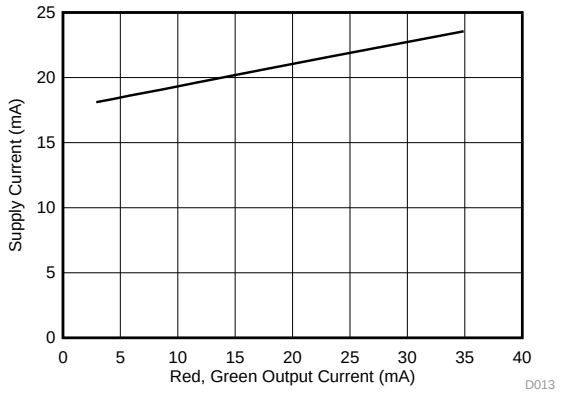


BCB = 7Fh

Figure 12. Global Brightness Control Linearity (OUTB*n*)

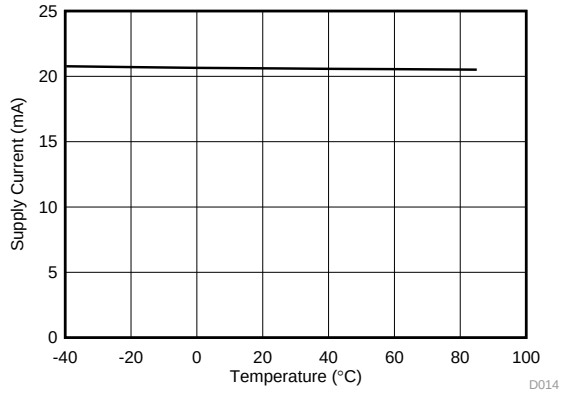
Typical Characteristics (continued)

At T_A = +25°C and VCC = 3.3 V, unless otherwise noted.



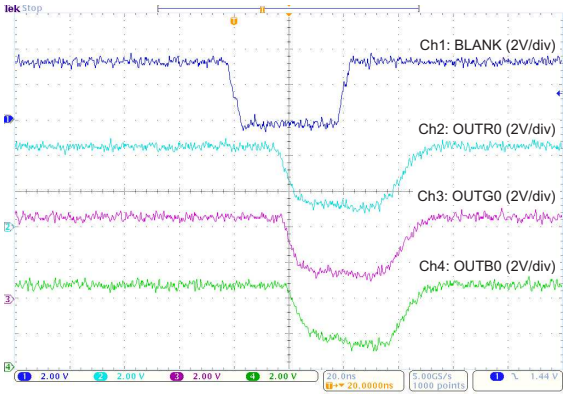
SIN = 15 MHz | SCLK = 30 MHz | BCX = 7Fh
MC = 0h to 7h | All OUTX*n* = On | BLANK = Low
SOUT = No Load | V_{OUT} = 0.8 V

Figure 13. Supply Current vs Output Current



SIN = 15 MHz | BCX = 7Fh | MC = 5h
All OUTX*n* = On | SCLK = 30 MHz | BLANK = Low
SOUT = No Load | V_{OUT} = 0.8 V
T_A = –40°C to +85°C

Figure 14. Supply Current vs Ambient Temperature



V_{CC} = 3.3 V | MC = 7h | BCX = 7Fh | V_{LED} = 4.5 V
R_L = 100 Ω (OUTR*n*, OUTG*n*) | R_L = 150 Ω (OUTB*n*)
C_L = 15 pF | BLANK Low Pulse Duration = 40 ns

Figure 15. Constant-Current Output Voltage Waveform

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7 Parameter Measurement Information

7.1 Pin Equivalent Input and Output Schematic Diagrams

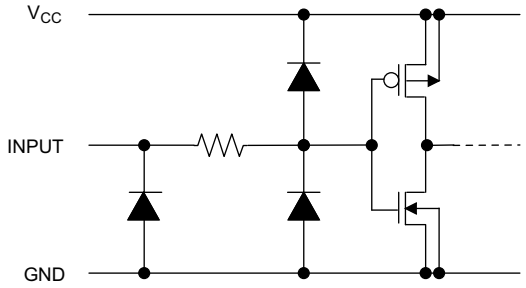


Figure 16. SIN, SCLK, LAT, BLANK

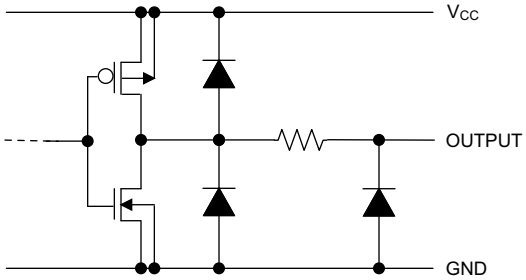
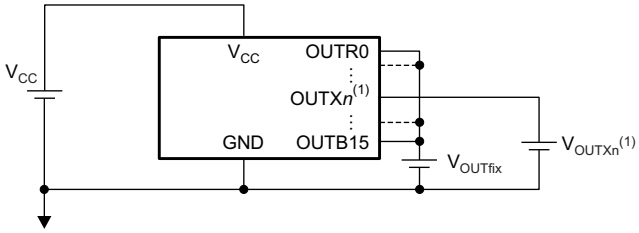


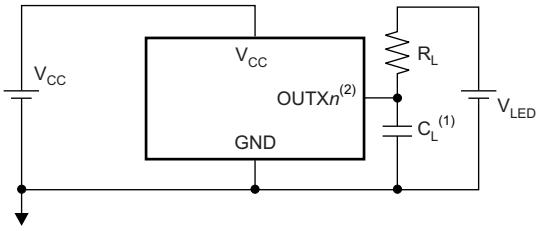
Figure 17. SOUT



(1) X = R, G, or B. n = 0 to 15.

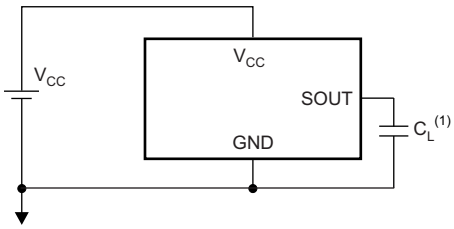
Figure 18. OUTX*n*

7.2 Test Circuits



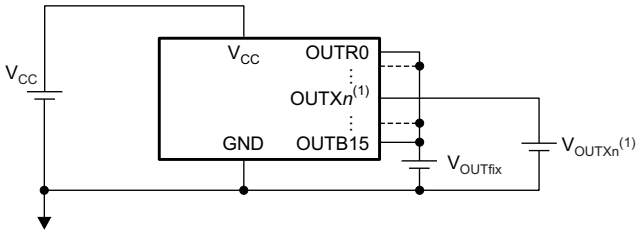
(1) C_L includes measurement probe and jig capacitance.
(2) X = R, G, or B. n = 0 to 15.

Figure 19. Rise and Fall Time Test Circuit for OUTX*n*



(1) C_L includes measurement probe and jig capacitance.

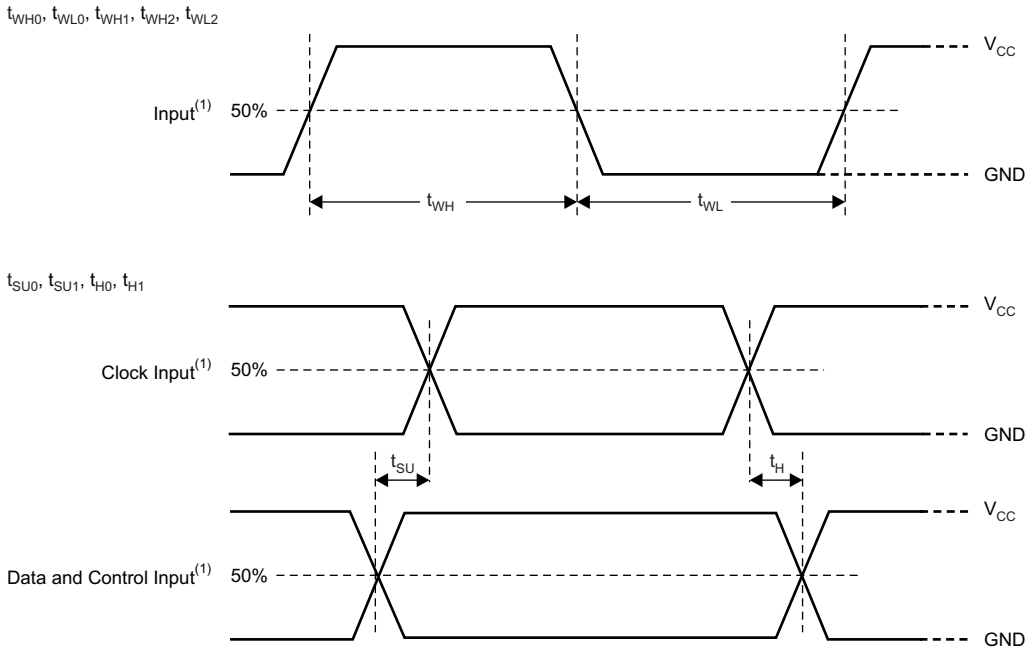
Figure 20. Rise and Fall Time Test Circuit for SOUT



(1) X = R, G, or B. n = 0 to 15.

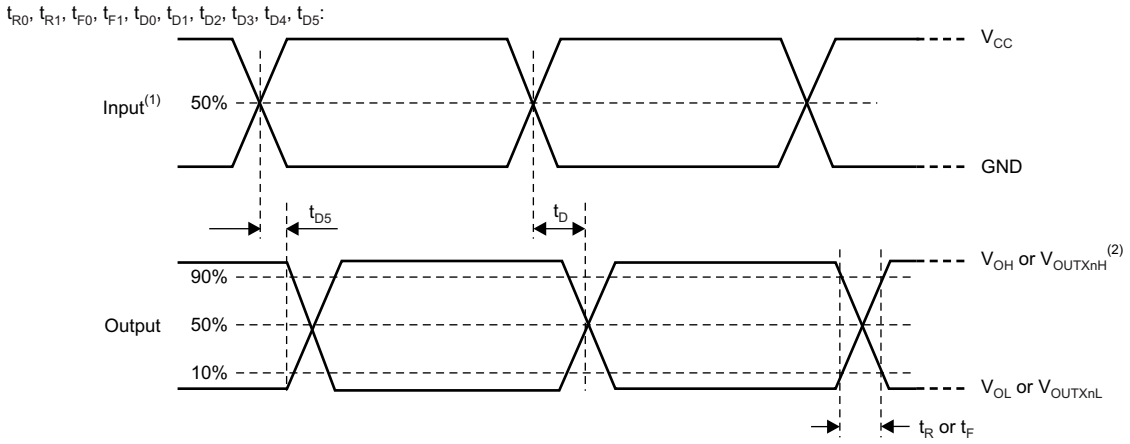
Figure 21. Constant-Current Test Circuit for OUTX*n*

7.3 Timing Diagrams



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 22. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

(2) X = R, G, or B. n = 0 to 15.

Figure 23. Output Timing

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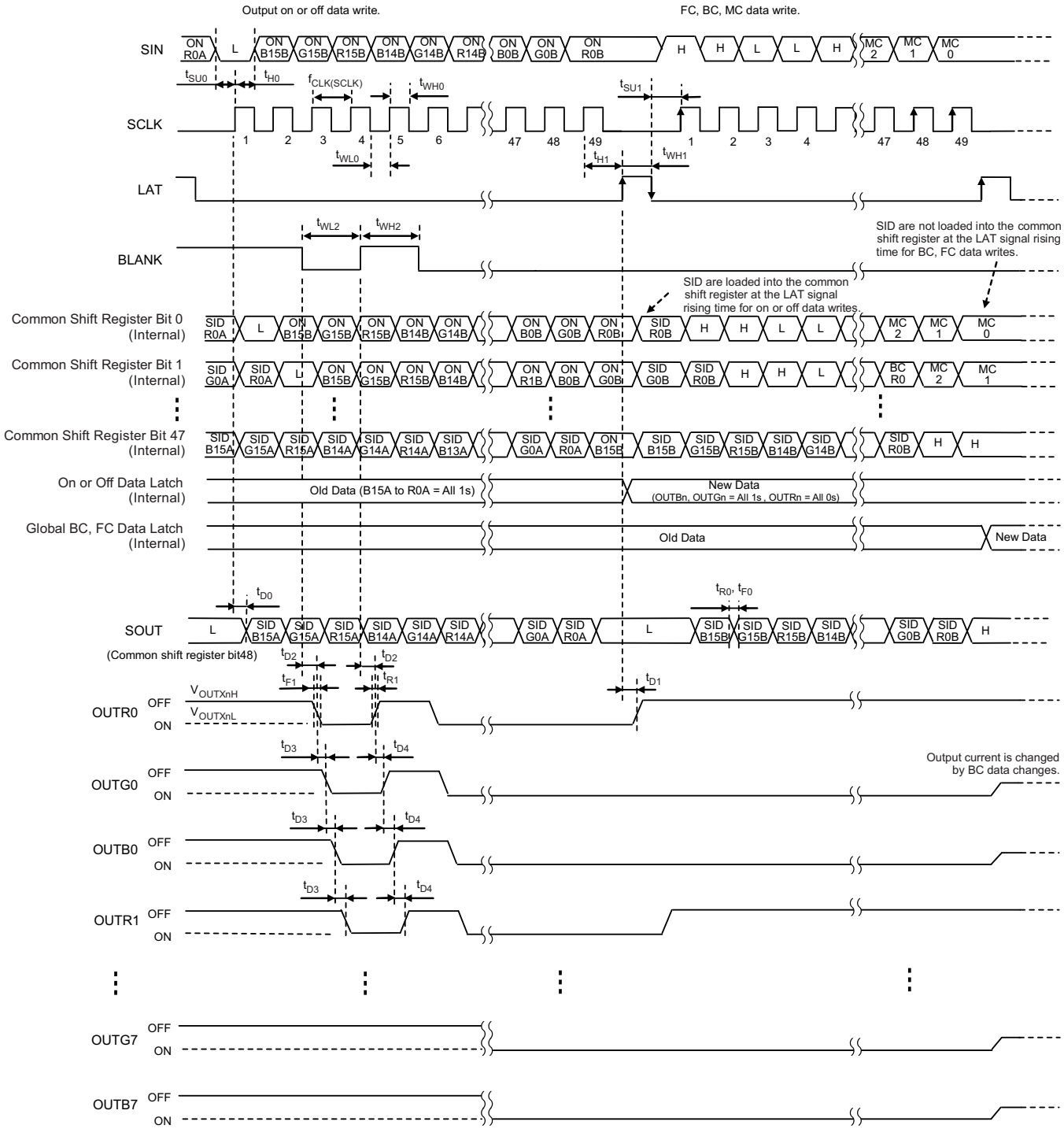
Timing Diagrams (continued)



(1) X = R, G, or B. n = 0 to 15.

Figure 24. Data Write and OUTX*n* On or Off Timing Diagram

Timing Diagrams (continued)

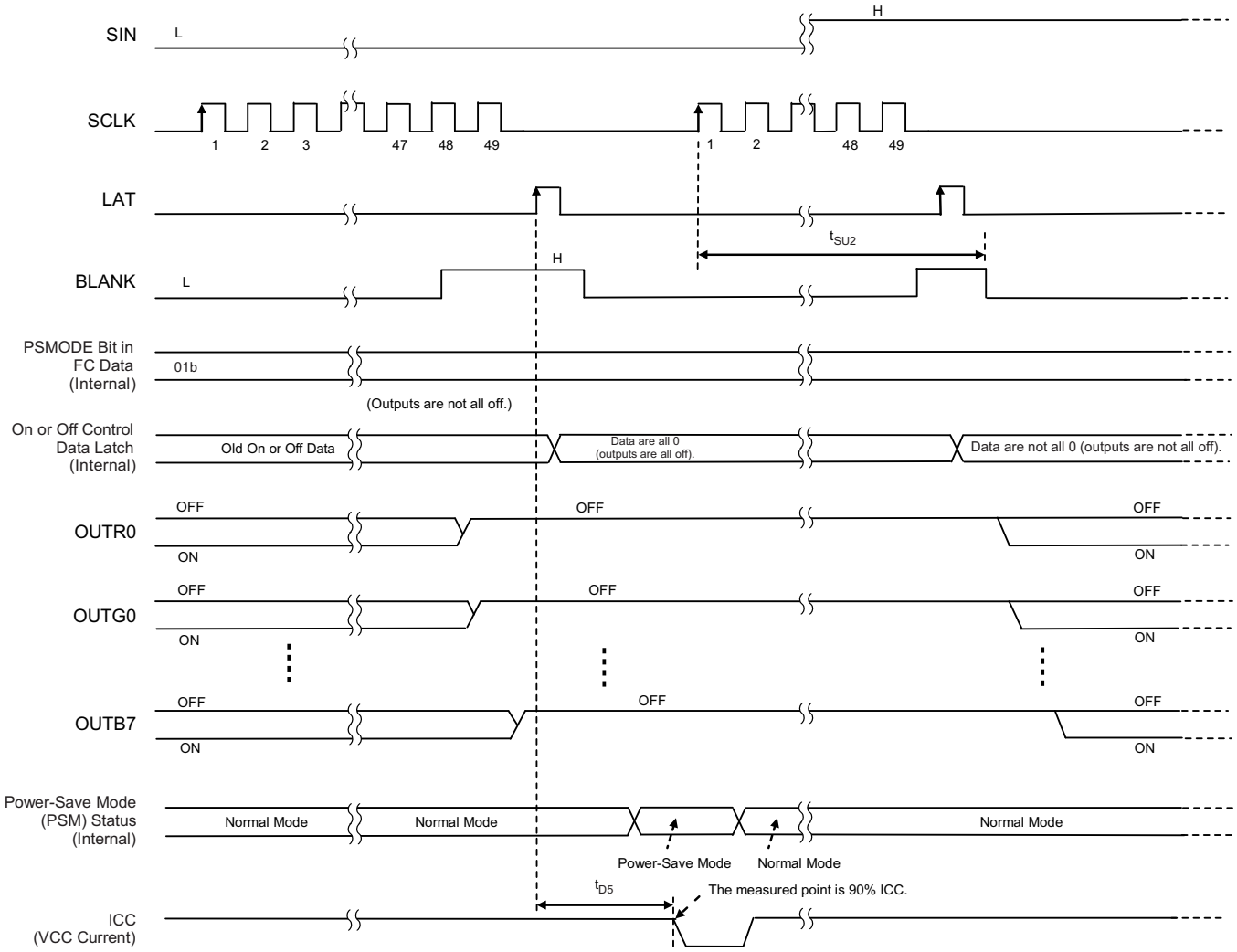


Figure 25. Power-Save Mode Timing Diagram (PSMODE = 01b)

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Timing Diagrams (continued)

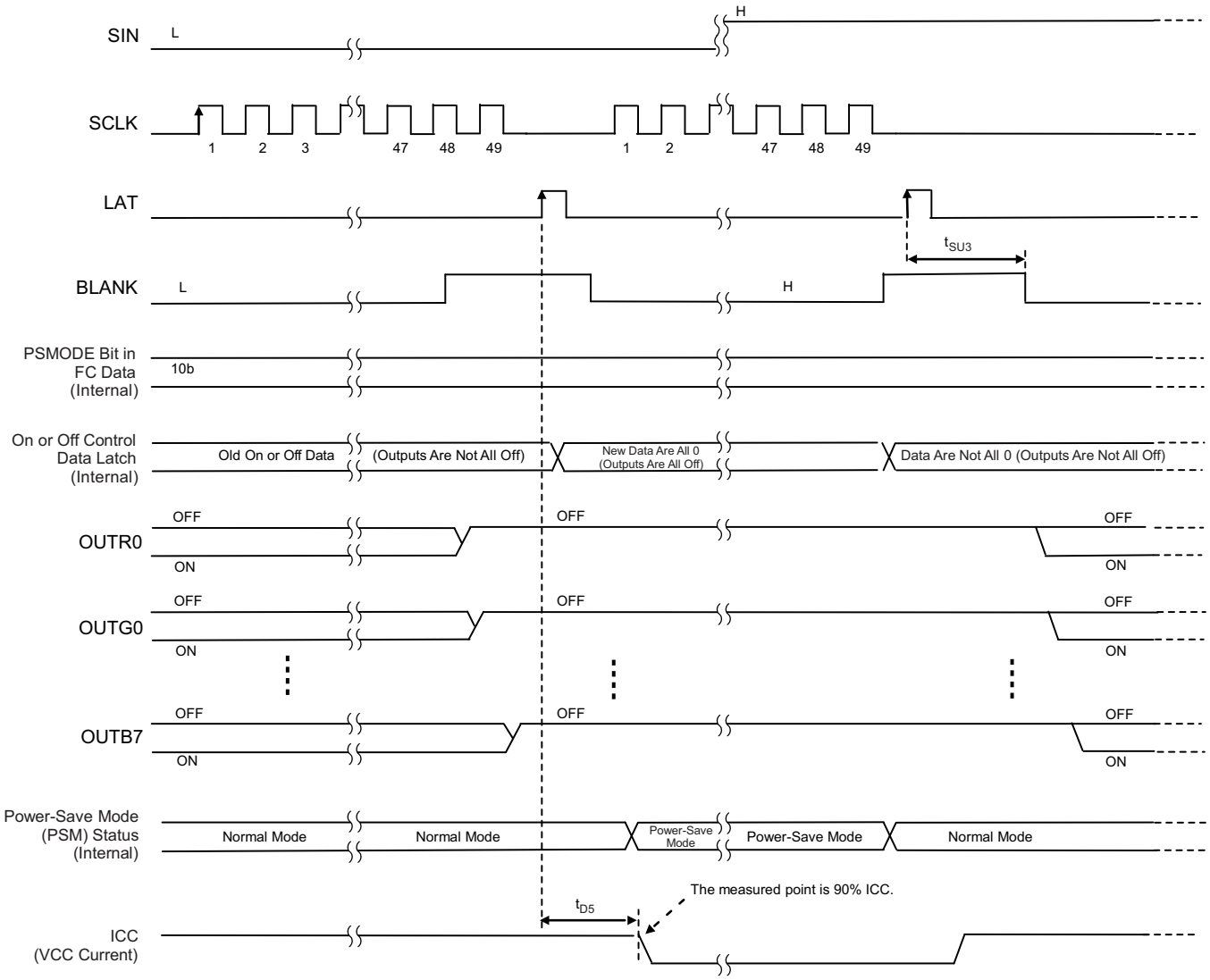

Figure 26. Power-Save Mode Timing Diagram (PSMODE = 10b)

8 Detailed Description

8.1 Overview

The TLC5954 is 48-channel, 34.9-mA or 24.4-mA, constant-current LED driver that can control the LED on of off settings with the BLANK signal for grayscale (GS) control. The minimum 40-ns BLANK signal pulse duration can be input to generate very short LED on-time.

The device has a 128-step, 7-bit, output current control function termed global brightness control (BC) that can control each color group output. The BC function can adjust the red, green, and blue LED intensity for true white with constant-current control. The device contributes higher image quality to LED displays with fine white balance tuning by using these BLANK pulse durations and MC, BC functions.

The display controller can locate LED lamp failures via the device because the controller can detect LED lamp failures with the LED open detection (LOD) and LED short detection (LSD) functions. Furthermore, the reliability of the display can be improved by the LOD and LSD function.

The device maximum constant-current output value can be set by an internal register data function referred to as maximum current control (MC), instead of the general method of using an external resistor setting. Thus, any failure modes that occur from the external resistor can be eliminated. One resistor can also be eliminated with the MC function.

The device constant-current output can drive approximately 17.4 mA at a 0.32-V output voltage and a +25°C ambient temperature. This voltage is called *knee voltage*. This 0.32-V, low-knee voltage can contribute to the design of a lower-power display system.

The total number of LED drivers on one LED display panel can be reduced because 48 LED lamps can be driven by one LED driver. Therefore, designing fine-pitch LED displays is simplified.

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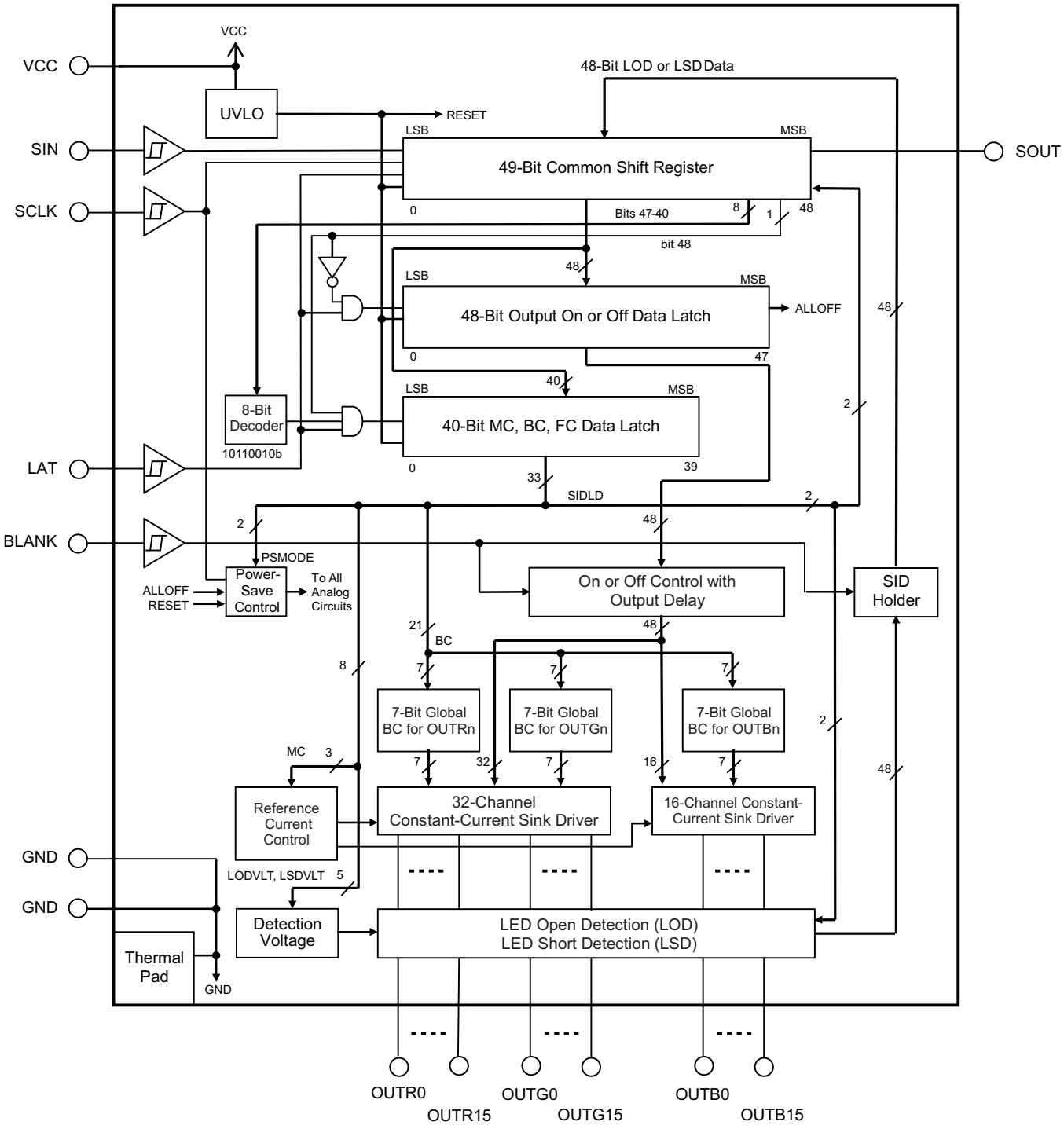
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Output Current Calculation

The output current value controlled by MC and BC can be calculated by Equation 1.

$$I_{OUTn}\,(mA) = I_{OLCMax}\,(mA) \times \left(0.06 + 0.94 \times \frac{BCX}{127}\right)$$

where:

- I_{OLCMax} = the maximum constant-current value for all OUTX*n* for each color group programmed by MC data,
- BCX = the global brightness control value (0h to 7Fh),
- X = R, G, or B for the red, green, or blue color group, and
- n = 0 to 15. (1)

Each output sinks the I_{OLCMax} current when they turn on and the global brightness control (BC) data are set to the maximum value of 7Fh (127d).

8.3.2 Status Information Data (SID)

The status information data (SID) contains the status of the LED open detection (LOD) and LED short detection (LSD).

When the output on-off data latch is written, the SID selected by the SIDLD bits are loaded into lower 48 bits in the common shift register at the LAT rising edge after the original data in the common shift register are copied to the on-off data latch. When the BC and FC data are written, SID data are not loaded to the common shift register. After SID data are copied into the common shift register, new SID data are not loaded until new data are written into the common shift register even if a LAT rising edge is input.

When the device resumes normal operation after the power-save mode, a BLANK rising edge must be input after t_{SU2} or t_{SU3} elapses in order to retain correct LOD and LSD data in the SID holder because the SID analog circuit does not function during power-save mode. The SID load configuration and SID read timing are shown in Figure 27 and Figure 28, respectively.

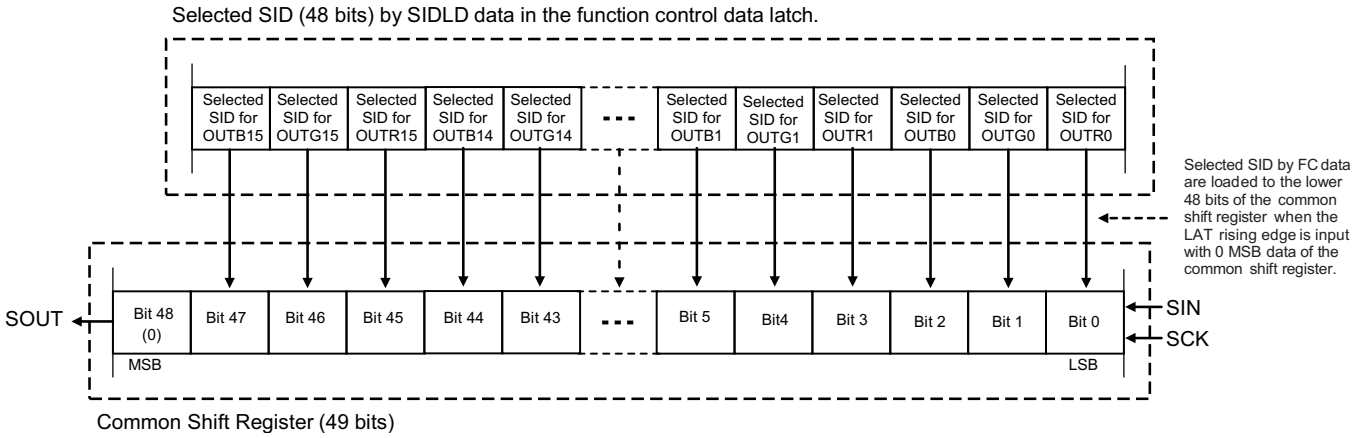


Figure 27. SID Load Configuration

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Feature Description (continued)

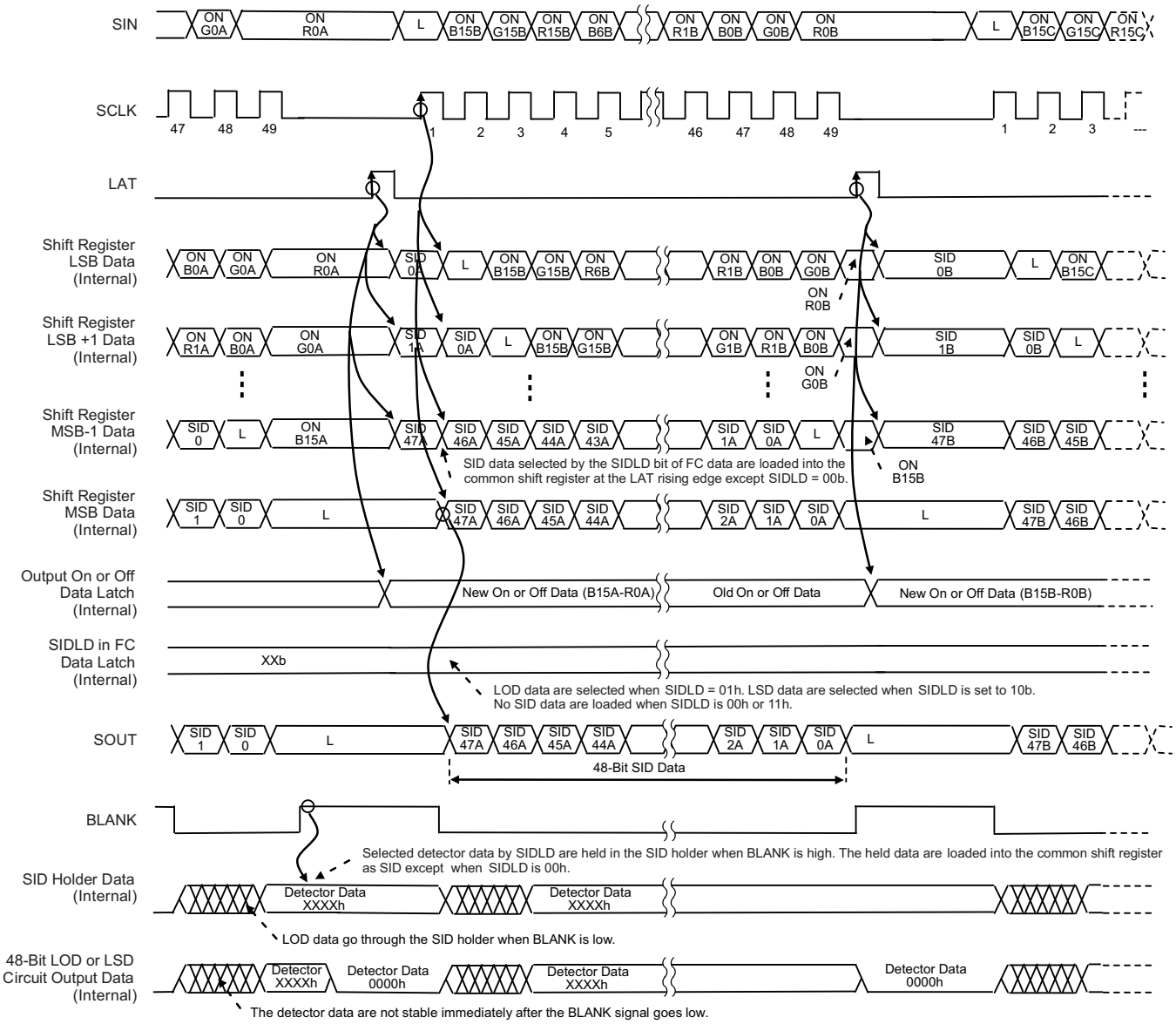

Figure 28. SID Read Timing Diagram

Feature Description (continued)

8.3.3 LED Open Detection (LOD)

LOD detects a fault caused by an open circuit in the *n*th LED string, or a short from OUTX*n* to ground with low impedance, by comparing the OUTX*n* voltage to the LOD detection threshold voltage level set by LODVLT in the function control data latch (see Table 6 and Table 8). If the OUTX*n* voltage is lower than the programmed voltage, the corresponding output LOD bit is set to 1 to indicate a shorted LED. Otherwise, the LOD bit is set to 0. LOD data are only valid for outputs that are set to 1 in the output on-off data latch. LOD data are always 0 for outputs that are set to 0 in the output on-off data latch.

LOD data are stored in a 48-bit register called the SID holder (see the *Functional Block Diagram*) at the BLANK rising edge when the SIDLD bits are set to 01b (see Table 7). The loaded LOD data can be read out through the common shift register as SID data at the SOUT pin. LOD data are not valid for 1 µs after the output is turned on. If the OUTX*n* controlled by the BLANK pin is less than 1 µs, the LOD data must be ignored.

When the device resumes operation from power-save mode, all OUTX*n* can be controlled by the internal on-off control data and the BLANK level after the setup time (t_{SU2}) elapses. LOD data are valid after the propagation delay. Figure 29 illustrates an LOD and LSD circuit, Table 1 shows the SID bit settings for LOD and LSD, and Figure 30 illustrates the LED open-detection operating timing diagram.

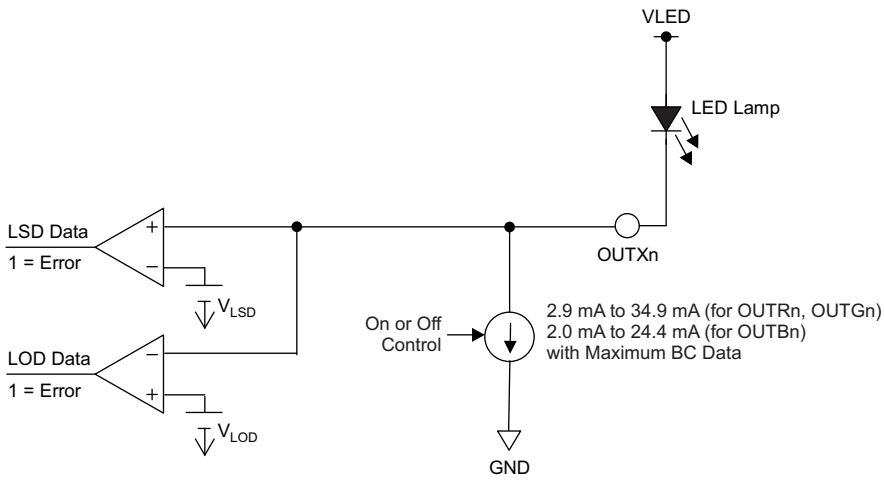

Figure 29. LOD, LSD Circuit

Table 1. LOD, LSD Truth Table

LOD	LSD	CORRESPONDING BIT IN SID
LED is not open ($V_{OUTXn} > V_{LOD}$)	LED is not shorted ($V_{OUTXn} \le V_{LSD}$)	0
LED is open or shorted to GND ($V_{OUTXn} \le V_{LOD}$)	LED is shorted between anode and cathode, or shorted to higher voltage side ($V_{OUTXn} > V_{LSD}$)	1

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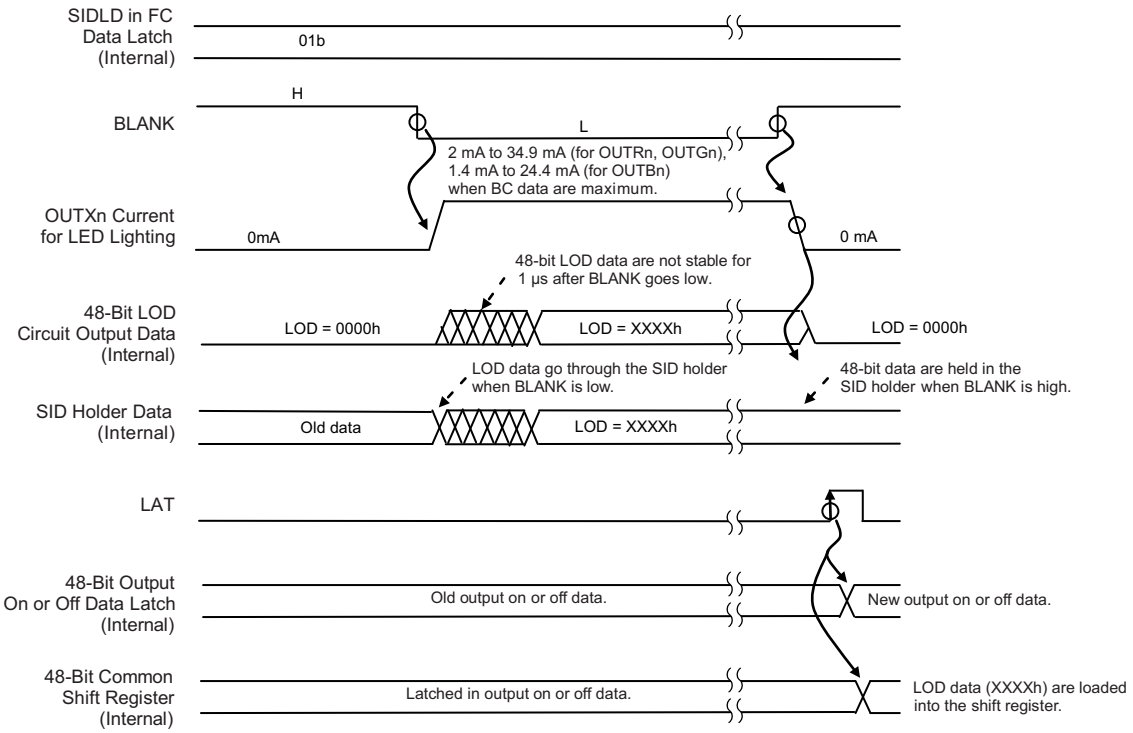

Figure 30. LOD Operation Timing Diagram

8.3.4 LED Short Detection (LSD)

LSD data detect a fault caused by a shorted LED by comparing the OUTX*n* voltage to the LSD detection threshold voltage level set by LSDVLT in the function control data latch (see Table 6 and Table 9). If the OUTX*n* voltage is higher than the programmed voltage, the corresponding output LSD bit is set to 1 to indicate a shorted LED. Otherwise, the LSD bit is set to 0. LSD data are only valid for outputs that are set to 1 in the output on-off data latch. LSD data are always 0 for outputs that are set to 0 in the output on-off data latch.

LSD data are loaded into a 48-bit register called the SID holder at the BLANK rising edge when the SIDLD bits are set to 10b (see Table 7). The loaded LSD data can be read out through the common shift register as SID data at the SOUT pin. LSD data are not valid for 1 µs after the output is turned on. If the OUTX*n* controlled by the BLANK pin is less than 1 µs, the LSD data must be ignored.

When the device resumes operation from power-save mode, all OUTX*n* can be controlled by the internal on-off control data and the BLANK level after the setup time (t_{SU2}) elapses. LSD data are valid after the propagation delay. Figure 29 illustrates an LOD and LSD circuit and Figure 31 shows LED short-detection operating timing diagram.

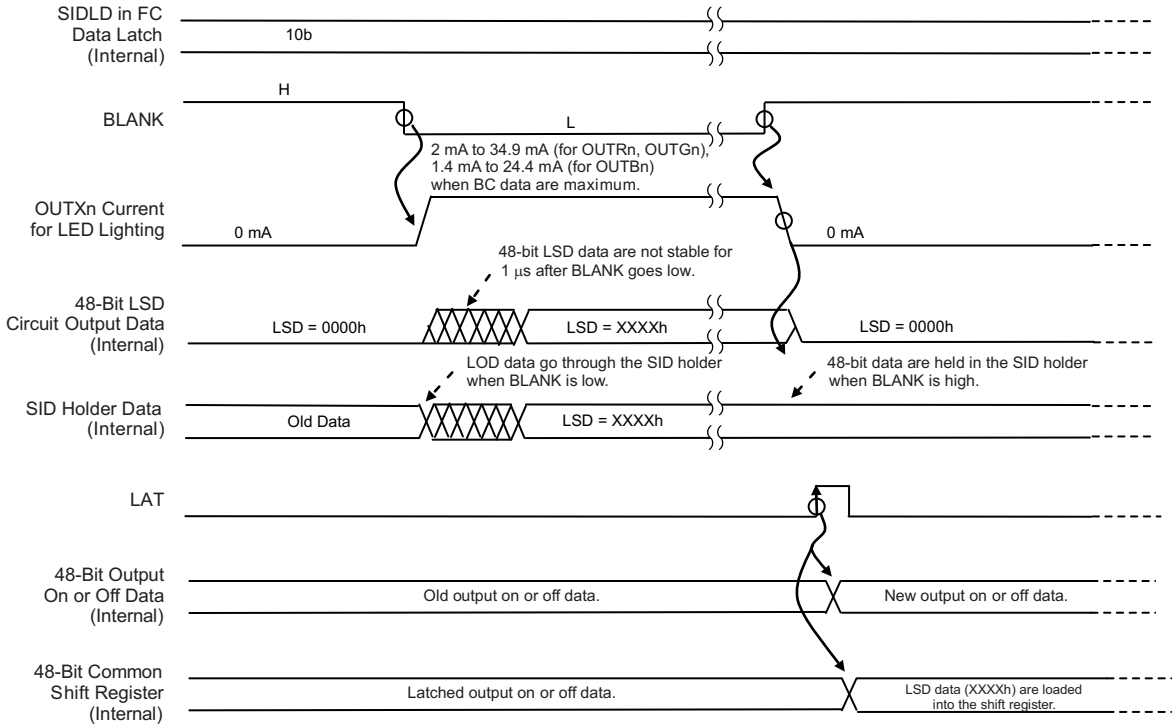

Figure 31. LSD Operation Timing Diagram

8.3.5 Noise Reduction

Large surge currents may flow through the device and the board on which the device is mounted if all 48 LED channels turned on simultaneously when BLANK toggles from high to low. These large current surges can induce detrimental noise and electromagnetic interference (EMI) into other circuits. The device turns on the LED channels in a series delay to provide a circuit soft-start feature. A small delay circuit is implemented between each output. When all bits of the on-off data latch are set to 1, each constant-current output turns on in the following order: OUTR0, OUTG0, OUTB0, OUTR15, OUTG15, OUTB15, OUTR1, OUTG1, OUTB1, OUTR14, OUTG14, OUTB14, OUTR2, OUTG2, OUTB2, OUTR13, OUTG13, OUTB13, OUTR3, OUTG3, OUTB3, OUTR12, OUTG12, OUTB12, OUTR4, OUTG4, OUTB4, OUTR11, OUTG11, OUTB11, OUTR5, OUTG5, OUTB5, OUTR10, OUTG10, OUTB10, OUTR6, OUTG6, OUTB6, OUTR9, OUTG9, OUTB9, OUTR7, OUTG7, OUTB7, OUTR8, OUTG8, and OUTB8 with a small delay for each OUTX*n* after BLANK goes low or LAT goes high, see Figure 24. Both turn-on and turn-off times are delayed.

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8.4 Device Functional Modes

8.4.1 Maximum Constant Sink Current

The maximum output current of each channel (I_{OLCMax}) is programmed by maximum current (MC) data and can be set by the serial interface.

I_{OLCMax} is the highest current for each output. Each OUTX*n* sinks I_{OLCMax} current when they turn on with the global brightness control (BC) data set to the maximum value of 7Fh (127d). MC data are updated when the same data are written to the MC bits twice. When the device is powered on, the MC data latch is set to 0.

Table 2 shows the characteristics of the constant-current sink versus the MC control data.

Table 2. Maximum Constant-Current Output versus MC Data

MC DATA			I_{OLCMax} (mA)	
BINARY	DECIMAL	HEX	OUTR*n*, OUTG*n*	OUTB*n*
000 (default)	0 (default)	0 (default)	2.9	2.0
001	1	1	4.4	3.1
010	2	2	5.8	4.1
011	3	3	8.7	6.1
100	4	4	11.6	8.1
101	5	5	17.4	12.2
110	6	6	23.2	16.3
111	7	7	34.9	24.4

8.4.2 Global Brightness Control (BC) Function: Sink Current Control

The device is capable of simultaneously adjusting the output current of each color group (OUTR0 to OUTR15, OUTG0 to OUTG15, and OUTB0 to OUTB15). This function is called *global brightness control* (BC). The BC function allows the global BC data of LEDs connected to the three color groups to be adjusted. All OUTX*n* can be adjusted in 128 steps from 6% to 100% of the maximum output current, I_{OLCMax}. The BC data are transmitted to the device by the serial interface. When BC data change, the output current also changes immediately.

Table 3 shows the BC data versus the constant-current ratio against I_{OLCMax}.

Table 3. BC Data versus Current Ratio and Set Current Value

BC DATA			OUTPUT CURRENT RATIO TO I_{OLCMax} (%, typ)	OUTPUT CURRENT (mA, typ)			
BINARY				OUTR*n*, OUTG*n*		OUTB*n*	
MSB LSB	DECIMAL	HEX		MC = 7h (I_{OLCMax} = 34.9 mA)	MC = 0h (I_{OLCMax} = 2.9 mA)	MC = 7h (I_{OLCMax} = 24.4 mA)	MC = 0h (I_{OLCMax} = 2.0 mA)
000 0000	0	00	6.0	2.09	0.17	1.47	0.12
000 0001	1	01	6.7	2.35	0.20	1.65	0.14
000 0010	2	02	7.5	2.61	0.22	1.83	0.15
…	…	…	…	…	…	…	…
111 1101	125	7D	98.5	34.4	2.86	24.1	1.96
111 1110	126	7E	99.3	34.7	2.88	24.3	1.98
111 1111	127	7F	100.0	34.9	2.90	24.4	2.00

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8.4.3 Constant-Current Output On or Off Control

When BLANK is low, each OUTX*n* is controlled by the data in the output on or off data latch. When data corresponding to an output equal 1, the output turns on; when data corresponding to an output equal 0, the output turns off. When BLANK is high, all OUTX*n* are forced off. When the device is powered on, the data in the output on or off data latch are set to 0. A truth table for the on or off control data is shown in Table 4.

Table 4. On or Off Control Data Truth Table

ON OR OFF CONTROL DATA	CONSTANT-CURRENT OUTPUT STATUS
0 (default)	Off
1	On

8.4.4 Power-Save Mode

The power-save mode control bits are assigned in the BC and FC data latch. The device dissipation current becomes 7 µA (typ) in this mode. In PSM, all analog circuits (such as the constant-current outputs and the LOD and LSD circuit) do not function. However, logic circuits (such as the common shift register, on-off data latch, and BC and FC data latch) do function. When the two bits in PSMODE are 01b, 10b, or 11b, the power-save mode is enabled. When the two bits are 11b, the device is always in power-save mode. When the two bits are set to 00b, the device is always in normal operation. If all 0s are written in the output on-off data latch, the device goes into power-save mode when the two bits are 01b or 10b. When a rising edge is generated at SCLK with the two PSMODE bits set to 01b, the device exits PSM and returns to normal operation. When data in the output on-off data latch are not all 0s, and when the two PSMODE bits set to 10b, the device exits PSM and returns to normal operation. All OUTX*n* are turned on after the device exits PSM. Figure 32 and Figure 33 provide power-save mode timing diagrams for PSMODE set to 01b and 10b, respectively. The BLANK level should go low after t_{SU2} or t_{SU3} when the device exists PSM and returns to normal mode because the output current may be unstable immediately after starting normal mode.

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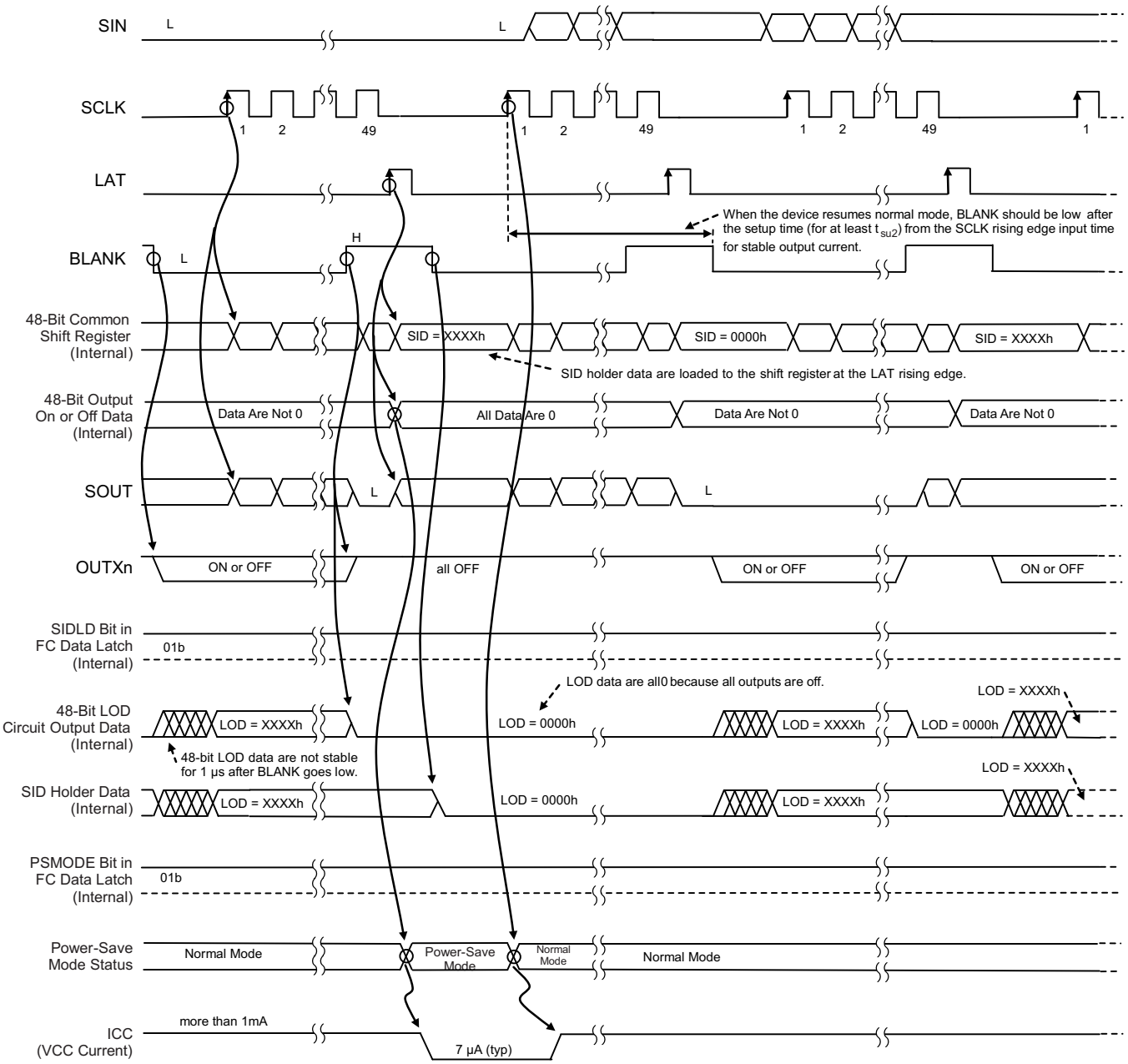

Figure 32. Power-Save Mode (FC Data PSMODE Bits = 01b)

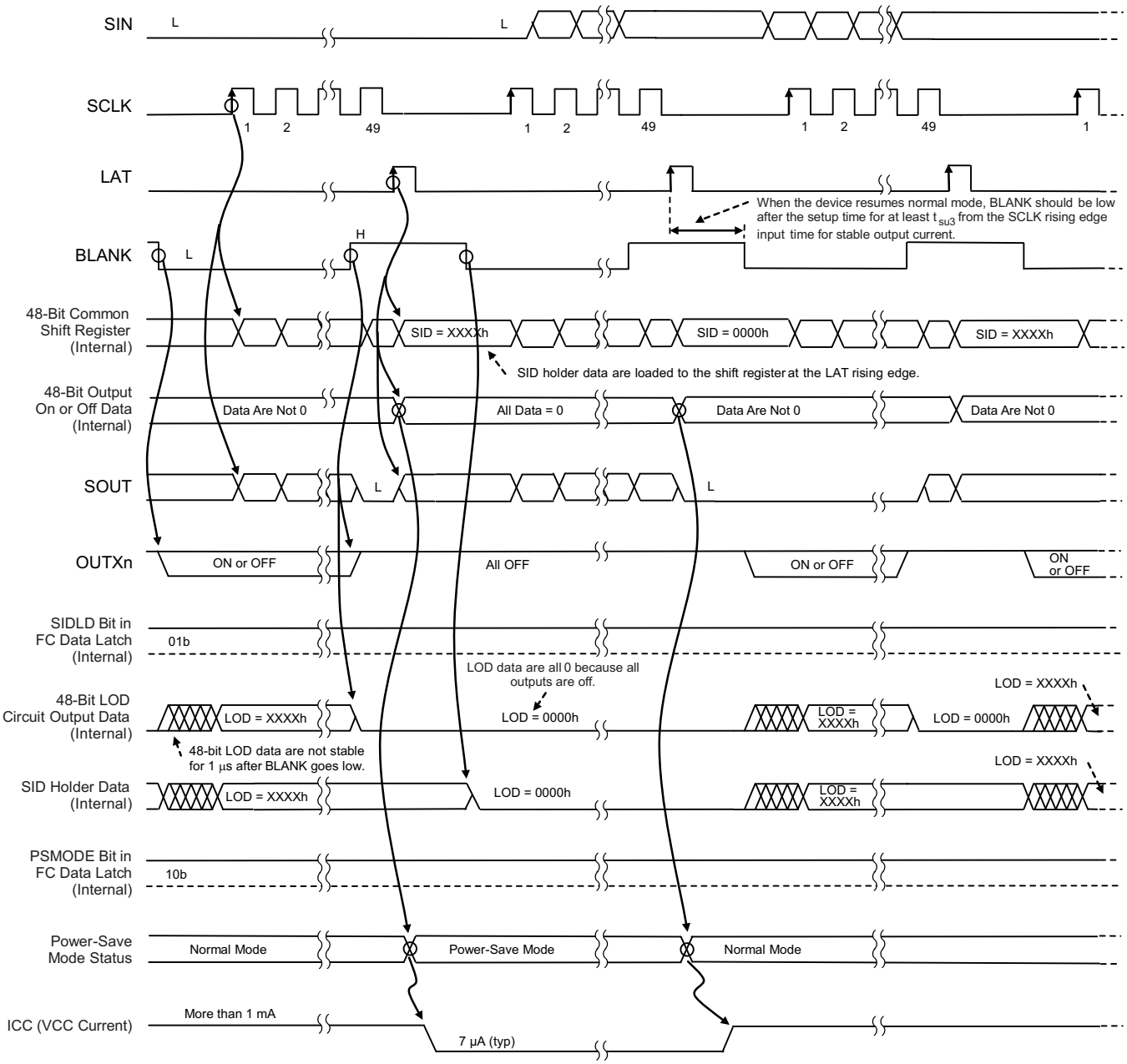

Figure 33. Power-Save Mode (FC Data PSMODE Bits = 10b)

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8.5 Register Maps

8.5.1 Register and Data Latch Configuration

The device has one common shift register and four control data latches. These data latches are the output on or off data latch, the maximum current control (MC) data latch, the global brightness control (BC) data latch, and the function control (FC) data latch.

The common shift register is 49 bits long, the output on or off data latch is 48 bits long, and another 48-bit data latch is comprised of the 40-bit MC, BC, and FC data latches with an 8-bit write command decoder. If the common shift register MSB is 0, the least significant 48 bits of data from the 49-bit common shift register are latched into the output on or off data latch. If the MSB (bit 48) from the 49-bit common shift register is 1 and MSB 1 through MSB 9 (bits [47:40]) are 96h (10010110b) for the write command data, the middle 37 bits (bits [39:3]) in the common shift register are latched into the BC and FC data latch. MC data are updated when the same data are written to the MC bits twice with the write command data (96h) and the MSB (bit 48) set to 1. Figure 34 shows the configuration of the common shift register and the four data latches.

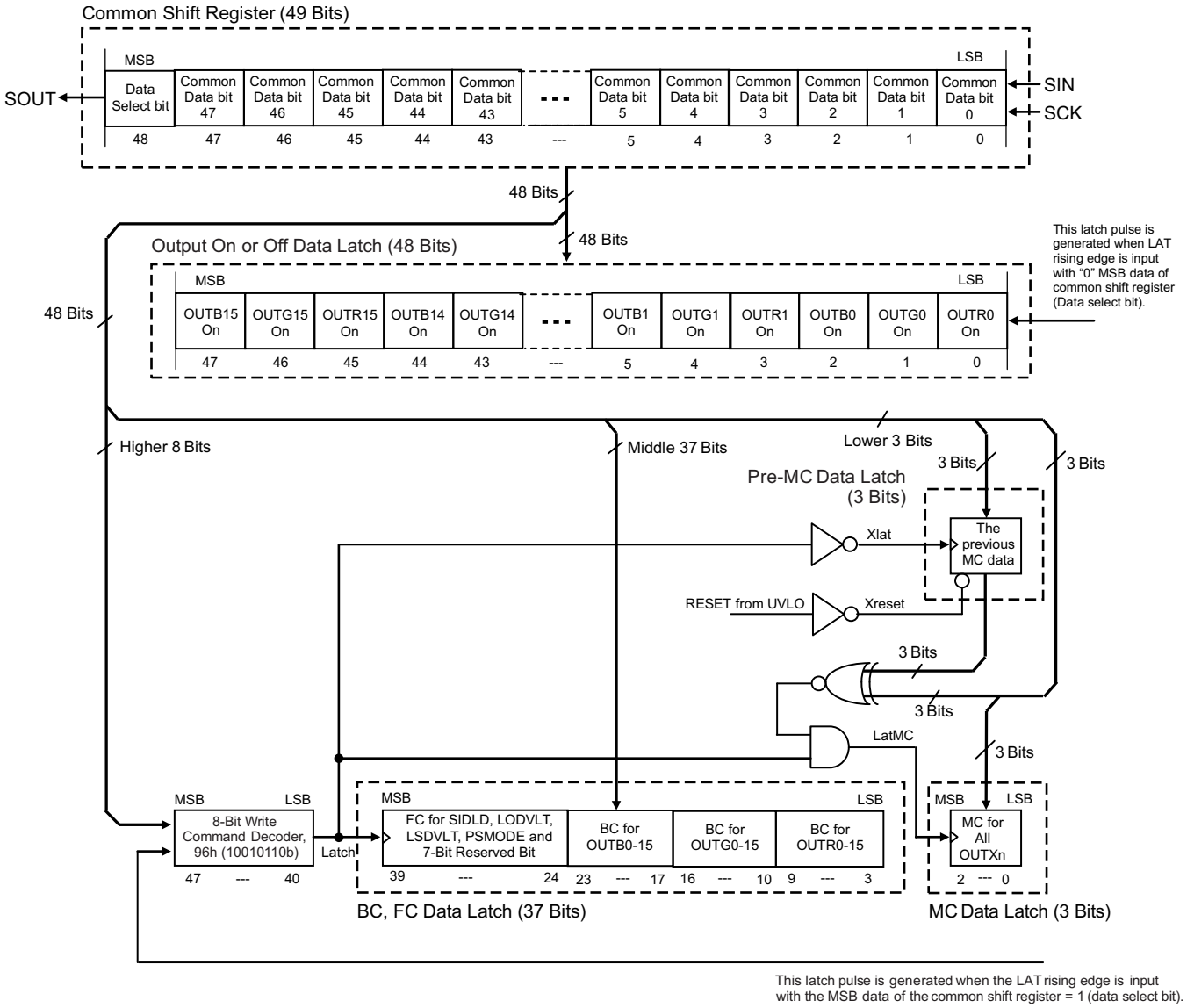

Figure 34. Common Shift Register and Data Latch Configuration

Register Maps (continued)

8.5.1.1 Common Shift Register

The 49-bit common shift register is used to shift data from the SIN pin into the device. The data shifted into the register are used for the output on or off control, MC, BC, and several FC functions, and the write command. The LSB of the common shift register is connected to SIN and the MSB is connected to SOUT. On each SCLK rising edge, the data on SIN are shifted into the LSB and all 49 bits are shifted towards the MSB. The register MSB is always connected to SOUT. In addition, the status information data (SID) selected by the SIDLD bits in the FC data latch are loaded to the lower 48 bits of the 49-bit common shift register when a rising edge is input on LAT for the output on or off control data write operation except when SIDLD = 00b and 11b (see Table 7). When the device is powered on, all 49 bits of the common shift register are set to 0.

8.5.1.2 Output On or Off Data Latch

The output on or off data latch is 48 bits long and sets the on or off status for each constant-current output (OUTR*n*, OUTG*n*, OUTB*n*). When BLANK is low, the output corresponding to the specific bit in the output on or off data latch is turned on if the data are 1 and remains off if the data are 0. When BLANK is high, all outputs are forced off, but the data in the latch do not change as long as LAT does not latch in new data. When the MSB of the common shift register is set to 0, the lower 48 bits are written to the output on or off data latch on the LAT rising edge. When the device is powered on, all bits in the data latch are set to 0. The output on or off data latch bit assignment is shown in Table 5. See Figure 35 for an output on or off data write timing diagram.

Table 5. On or Off Control Data Latch Bit Assignment

BIT NUMBER	BIT NAME	CONTROL LED CHANNEL	DESCRIPTION	BIT NUMBER	BIT NAME	CONTROL LED CHANNEL	DESCRIPTION
0	OUTR0ON	OUTR0	0 = Output off 1 = Output on with BLANK low. When the device is powered on, all bits are set to 0.	24	OUTR8ON	OUTR8	0 = Output off 1 = Output on with BLANK low. When the device is powered on, all bits are set to 0.
1	OUTG0ON	OUTG0		25	OUTG8ON	OUTG8	
2	OUTB0ON	OUTB0		26	OUTB8ON	OUTB8	
3	OUTR1ON	OUTR1		27	OUTR9ON	OUTR9	
4	OUTG1ON	OUTG1		28	OUTG9ON	OUTG9	
5	OUTB1ON	OUTB1		29	OUTB9ON	OUTB9	
6	OUTR2ON	OUTR2		30	OUTR10ON	OUTR10	
7	OUTG2ON	OUTG2		31	OUTG10ON	OUTG10	
8	OUTB2ON	OUTB2		32	OUTB10ON	OUTB10	
9	OUTR3ON	OUTR3		33	OUTR11ON	OUTR11	
10	OUTG3ON	OUTG3		34	OUTG11ON	OUTG11	
11	OUTB3ON	OUTB3		35	OUTB11ON	OUTB11	
12	OUTR4ON	OUTR4		36	OUTR12ON	OUTR12	
13	OUTG4ON	OUTG4		37	OUTG12ON	OUTG12	
14	OUTB4ON	OUTB4		38	OUTB12ON	OUTB12	
15	OUTR5ON	OUTR5		39	OUTR13ON	OUTR13	
16	OUTG5ON	OUTG5		40	OUTG13ON	OUTG13	
17	OUTB5ON	OUTB5		41	OUTB13ON	OUTB13	
18	OUTR6ON	OUTR6		42	OUTR14ON	OUTR14	
19	OUTG6ON	OUTG6		43	OUTG14ON	OUTG14	
20	OUTB6ON	OUTB6		44	OUTB14ON	OUTB14	
21	OUTR7ON	OUTR7		45	OUTR15ON	OUTR15	
22	OUTG7ON	OUTG7		46	OUTG15ON	OUTG15	
23	OUTB7ON	OUTB7		47	OUTB15ON	OUTB15	

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Table 6. MC, BC, and FC Data Latch and Write Command Bit Description

BIT NUMBER	BIT NAME	DEFAULT VALUE (BINARY)	DESCRIPTION
[2:0]	MAXCUR (MC)	000b	Maximum current control (MC) data for all OUTX*n* (data = 0h to 7h, see Table 2)
[9:3]	BCR (BC)	—	Global brightness control (BC) data for RED color group (data = 00h to 7Fh, see Table 3)
[16:10]	BCG (BC)	—	Global brightness control (BC) data for GREEN color group (data = 00h to 7Fh, see Table 3)
[23:17]	BCB (BC)	—	Global brightness control (BC) data for BLUE color group (data = 00h to 7Fh, see Table 3)
[25:24]	SIDLD (FC)	—	SID load control. These two bits select the SID loaded to the common register when the LAT rising edge is input for on or off data writes. Table 7 shows the selected data truth table.
[28:26]	LODVLT (FC)	—	LOD detection voltage select. These three bits select the detection threshold voltage for the LED open detection (LOD). Table 8 shows the detect voltage truth table.
[30:29]	LSDVLT (FC)	—	LSD detection voltage select. These two bits select the detection threshold voltage for the LED short detection (LSD). Table 9 shows the detect voltage truth table.
[32:31]	PSMODE (FC)	11b	Power-save mode select. These two bits select the power-save mode between the four modes. Table 10 shows the power-save mode truth table. Figure 32 and Figure 33 illustrate the power-save mode operation timing diagrams.
[39:33]	RSV	—	Reserved data, don't care.
[47:40]	WRTCMD	—	Write command. When this data are 96h (10010110b), MC, BC, and FC data can be updated. In order to update MC data, the same data must be written twice to the MC bit.

Table 7. SID Load Control Truth Table

SIDLD		STATUS INFORMATION DATA (SID) LOADED TO THE COMMON SHIFT REGISTER
BIT 25	BIT 24	
0	0	No data are loaded (default value)
0	1	LED open detection (LOD) data are loaded
1	0	LED short detection (LSD) data are loaded
1	1	No data are loaded

Table 8. LOD Threshold Voltage Truth Table

LODVLT			LED OPEN DETECTION (LOD) THRESHOLD VOLTAGE
BIT 28	BIT 27	BIT 26	
0	0	0	VLOD0 (0.20 V, typ)
0	0	1	VLOD1 (0.30 V, typ)
0	1	0	VLOD2 (0.40 V, typ)
0	1	1	VLOD3 (0.50 V, typ)
1	0	0	VLOD4 (0.60 V, typ)
1	0	1	VLOD1 (0.30 V, typ)
1	1	0	VLOD1 (0.30 V, typ)
1	1	1	VLOD1 (0.30 V ,typ)

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Table 9. LSD Threshold Voltage Truth Table

LSDVLT		LED SHORT DETECTION (LSD) THRESHOLD VOLTAGE
BIT 30	BIT 29	
0	0	VLSD0 (0.50 × VCC, typ)
0	1	VLSD1 (0.70 × VCC, typ)
1	0	VLSD2 (0.90 × VCC, typ)
1	1	VLSD2 (0.90 × VCC, typ)

Table 10. Power-Save Mode Truth Table

PSMODE		POWER-SAVE MODE FUNCTION
BIT 32	BIT 31	
0	0	Power-save mode is disabled in every condition.
0	1	When all zeroes (0s) are written to the output on or off data latch, the device goes to power-save mode. When an SCLK rising edge occurs, the device goes to normal operation and starts to control the output current. However, after the setup time (t_{SU2}) elapses from the SCLK input timing, BLANK must go low. Otherwise, the output current may not reach the set constant-current value. If these two bits are set to 01b from 10b or 11b when the device is in power-save mode (PSM), the device remains in PSM and does not resume normal mode. When an SCLK rising edge is input after PSMODE = 01 is selected, the device returns to normal mode.
1	0	When all zeroes (0s) are written to the output on or off data latch, the device goes to power-save mode. When the data (except all 0s) are written to the output on or off data latch, the device goes to normal operation and starts to control the output current. However, after the setup time (t_{SU3}) elapses from the LAT input timing, BLANK must go low. Otherwise, the output current may not reach the set constant-current value. If this bit set is selected from other bit set to this bit set when the device is in PSM, the device remains in power-save mode. When data that are not all set to off are written to the on or off data latch after this bit set is selected, the device goes to normal mode.
1 (default)	1 (default)	Power-save mode is enabled in every condition.

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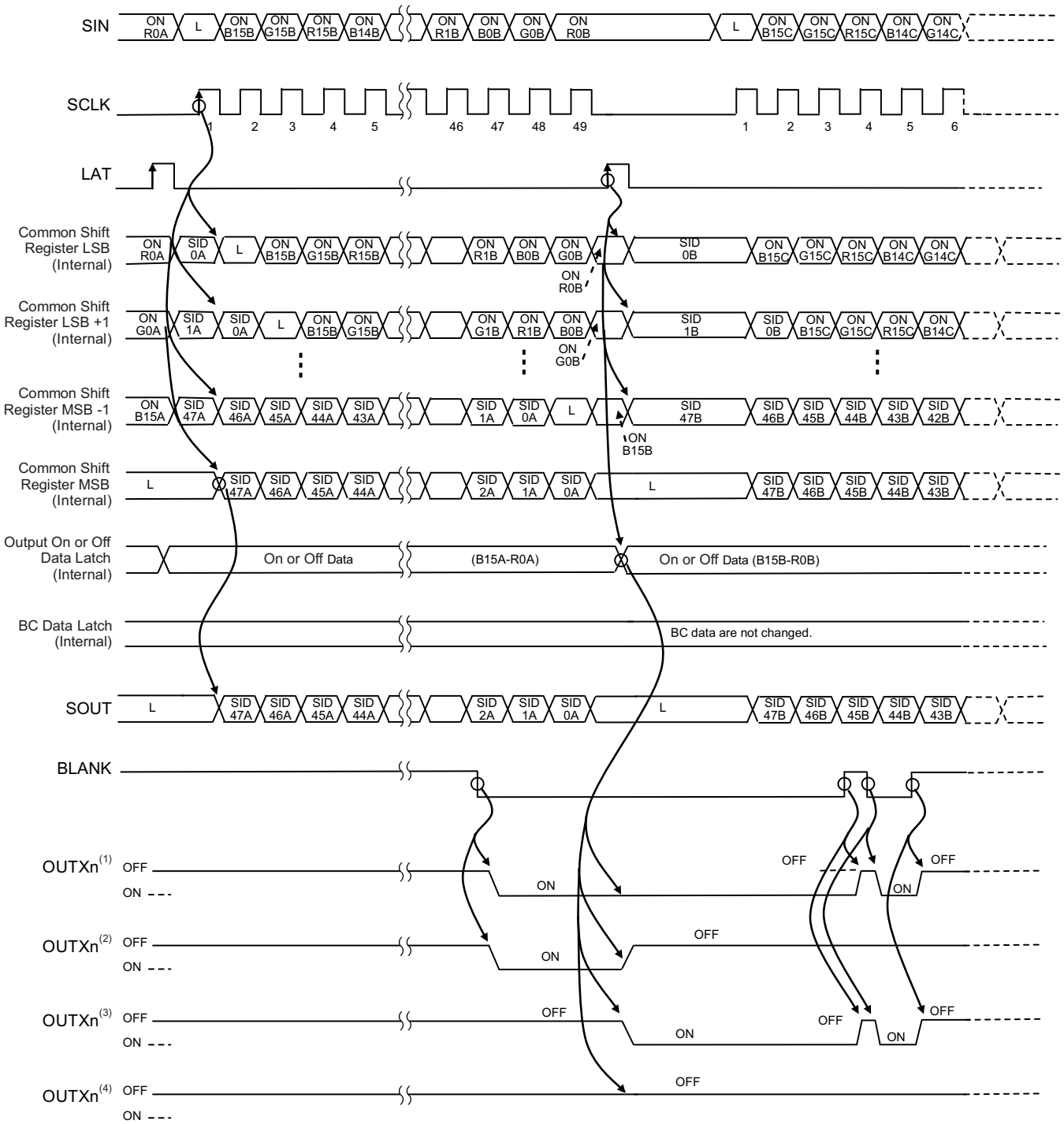

(1) On or off latched data are 1.

(2) On or off latched data change from 1 to 0 at the second LAT signal.

(3) On or off latched data change from 0 to 1 at the second LAT signal.

(4) On or off latched data are 0.

Figure 35. Output On or Off Timing Diagram: Data Write and OUTX*n* Control

8.5.1.3 Maximum Current Control (MC), Global Brightness Control (BC), and Function Control (FC) Data Latch

The MC, BC, and FC data latch (FC contains the PSMODE, LSDVLT, LODVLT, and SIDLD bits) is 40 bits long and is used to adjust the output current of all OUTX*n* (OUTR*n*, OUTG*n*, OUTB*n*), to select the status information data (SID) load data, to select LED open detection (LOD) and LED short detection (LSD) voltage, and to select the power-save mode (PSM).

Data are latched from the lower 40 bits of the 49-bit common shift register into the MC, BC, and FC data latch at the LAT rising edge when the MSB of the common shift register is set to 1 and the MSB 1 to MSB 9 bit data (bits [47:40]) of the common shift register MSB side is 96h (10010110b). However, MC data are only updated when the same data as the previous written data are written. Table 6 lists the MC, BC, and FC data latch bit assignment. The MC, BC, and FC data write timing diagram is shown in Figure 36. When the device is powered on, the MC data latch is set to 000b and the PSMODE bits in the FC data latch are set to 11b.

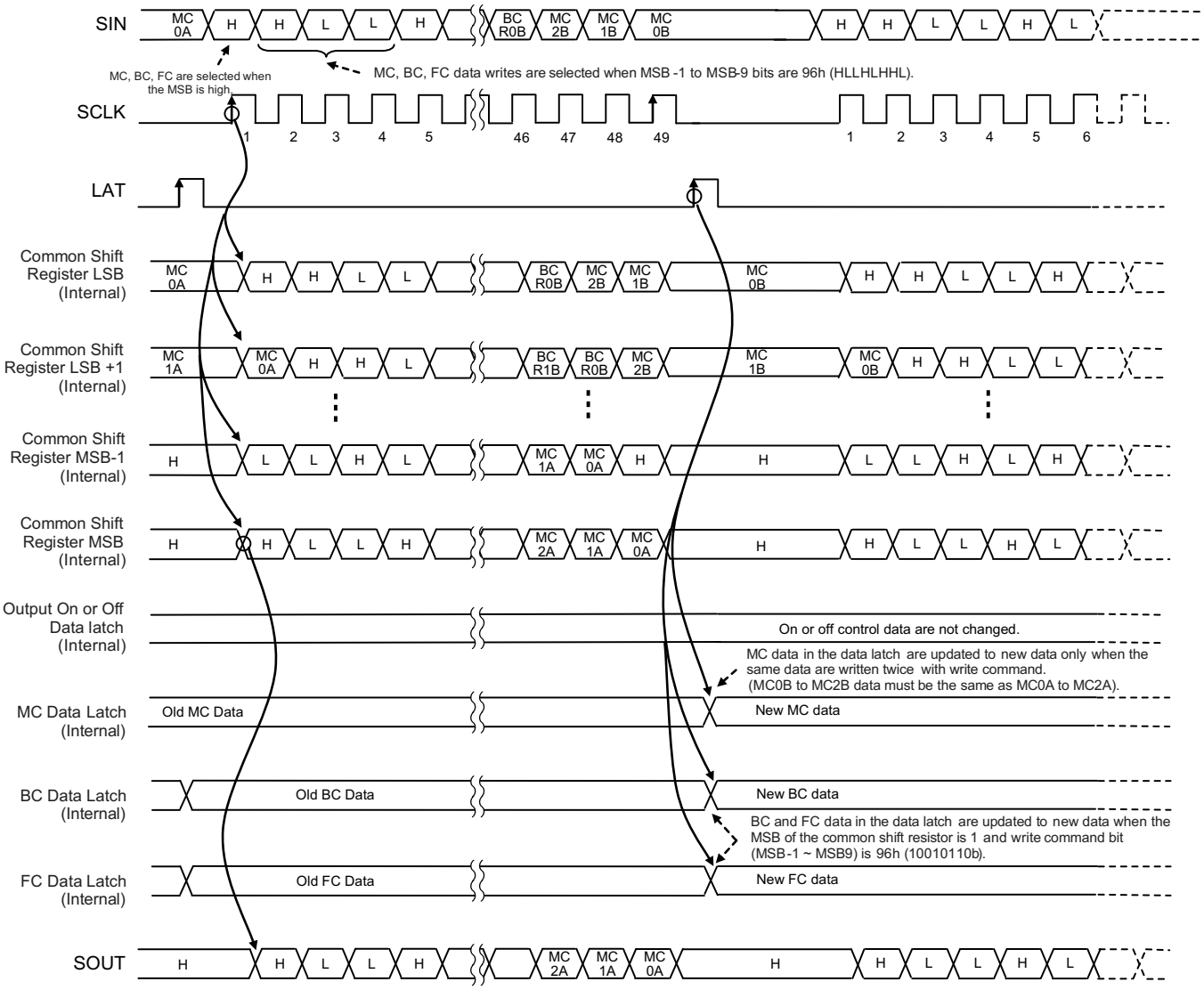

Figure 36. Maximum Current Control (MC), Global Brightness Control (BC), and Function Control (FC) Data Write Timing Diagram

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9 Applications and Implementation

9.1 Application Information

The device is a 48-channel, constant sink current, LED driver. This device is typically connected in series to drive many LED lamps with only a few controller ports. Output current control data and on or off control data can be written from the SIN input pin. The on or off timing can be controlled by the BLANK signal. Also, the LED open and short error flag can be read out from the SOUT output pin.

9.2 Typical Application

In this application, the device VCC and LED lamp anode voltages are supplied from different power supplies.

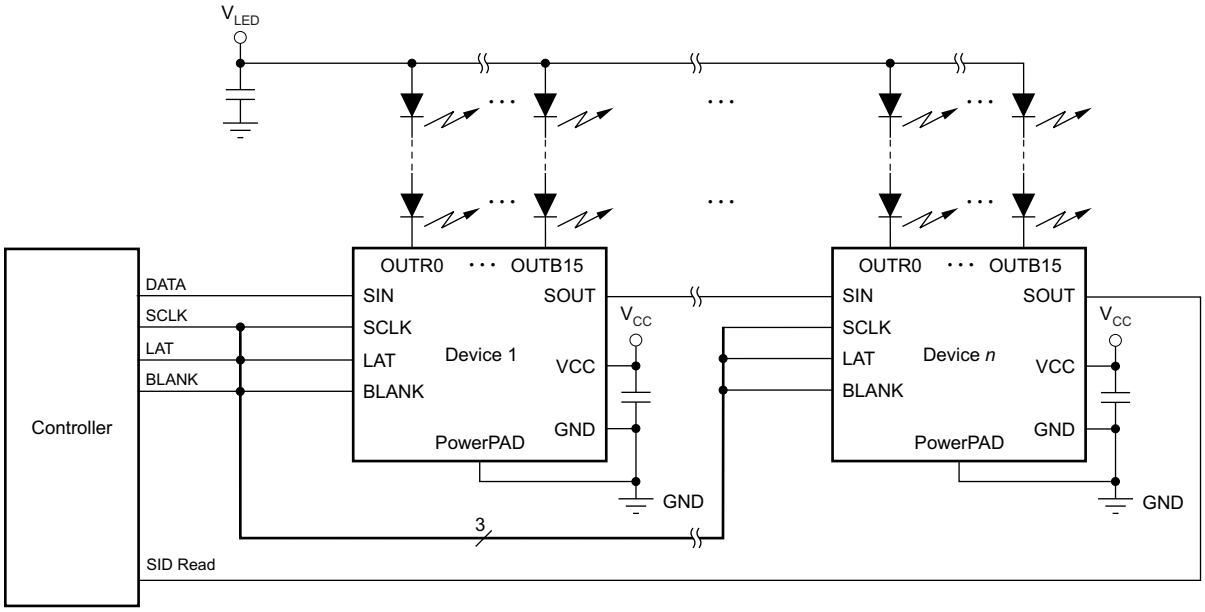

Figure 37. Typical Application Circuit (Multiple Daisy-Chained Devices)

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 11. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VCC input voltage range	3.0 V to 3.6 V
LED lamp (V_{LED}) input voltage range	Maximum LED forward voltage (V_F) + 0.4 V (knee voltage)
SIN, SCLK, LAT, and BLANK voltage range	Low level = GND, high level = VCC

9.2.2 Detailed Design Procedure

9.2.2.1 Step-by-Step Design Procedure

To begin the design process, a few parameters must be decided upon. The designer needs to know the following:

- Maximum output constant-current value for all colors of the LED ramp.
- Maximum LED forward voltage (V_F).
- Current ratio of red, green, and blue LED lamps for the best white balance.
- Is the LED open detect (LOD) function used? If so, which detection level (0.20 V, 0.30 V, 0.40 V, 0.50 V, or 0.60 V) is used?
- Is the LED short detect (LSD) function used? If so, which detection level (50% VCC, 70% VCC, or 90% VCC) is used?

9.2.2.2 Maximum Current (MC) Data

There are a total of three bits of MC data that set the output current of all constant-current outputs (OUTX*n*). Select the MC data to be greater than the target LED ramp current if the output current is reduced white balanced by the global brightness control data and write the data with other control data.

9.2.2.3 Global Brightness Control (BC) Data

There are a total of three sets of 7-bit BC data for the red, green, and blue LED ramp. Select the BC data for the best white balance of the red, green, and blue LED ramp and write the data with other control data.

9.2.2.4 On or Off Data

There are a total of 48 bits of on or off data for the on or off control of each output. Select the on or off data of the LED lamp on or off status control and write the data.

9.2.2.5 Other Control Data

There are a total of 8 bits of control data to set the function mode for the status information data (SID) load control, LOD voltage setting, LSD voltage setting, and power save mode (PSM) explained in the *Device Functional Modes* section. Write the 8-bit control data for the appropriate operation of the display system with MC and BC data as the control data.

9.2.2.6 Grayscale Control

All constant-current outputs are controlled by the BLANK pin logic level. When BLANK is GND, all constant-current outputs are turned on except that the output is set to 0 in the 48-bit output on-off data latch. When BLANK is VCC, all outputs are forced off. The LED lamp grayscale can be controlled by the BLANK low pulse duration.

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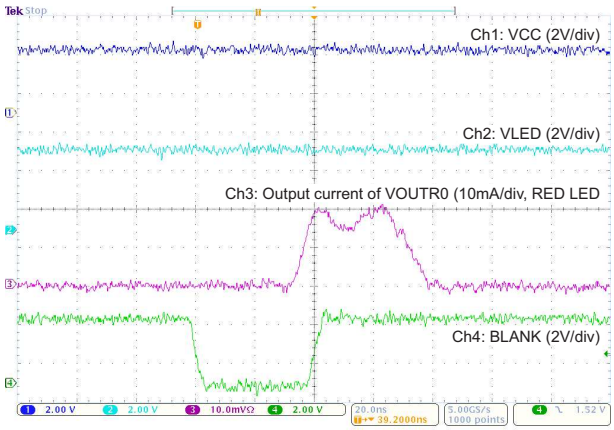
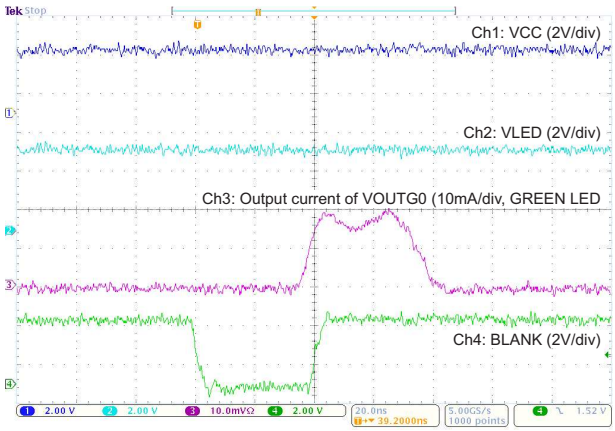
9.2.3 Application Curves

One LED connected to each output. BLANK low pulse duration = 40 ns.



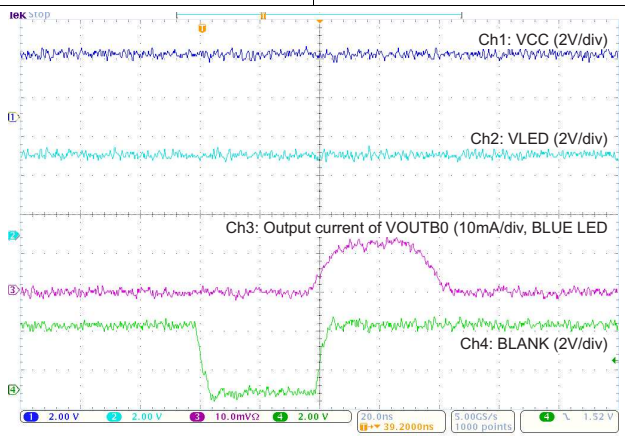
MCX = 5 BCX = 7Fh V_{LED} = 4.2 V
V_{CC} = 3.3 V SIDLD = LODVLT = LSDVLT = PSMODE = 0

Figure 38. OUTR0 Output Current Waveform



MCX = 5 BCX = 7Fh V_{LED} = 4.2 V
V_{CC} = 3.3 V SIDLD = LODVLT = LSDVLT = PSMODE = 0

Figure 39. OUTG0 Output Current Waveform



MCX = 5 BCX = 7Fh V_{LED} = 4.2 V
V_{CC} = 3.3 V SIDLD = LODVLT = LSDVLT = PSMODE = 0

Figure 40. OUTB0 Output Current Waveform

10 Power Supply Recommendations

The V_{CC} power-supply voltage should be well regulated. An electrolytic capacitor must be used to reduce the voltage ripple to less than 5% of the input voltage. Furthermore, the V_{LED} voltage should be set to the voltage calculated by Equation 2:

$V_{LED} \geq$ LED Maximum $V_F \times$ Number of LED Lamps Connected in Series + 0.4 V (5 mA for MC Data Example)

where:

- V_F = Forward voltage (2)

Because the total current of the constant-current output is large, some electrolytic capacitors must be used to prevent the OUTX*n* pin voltage from dropping lower than the calculated voltage from Equation 2.

11 Layout

11.1 Layout Guidelines

1. The decoupling capacitor should be placed near the VCC and GND pin.
2. The GND pattern should be routed as widely as possible for large GND currents. Maximum GND current is approximately 1.52 A.
3. The routing between the LED cathode side and the device OUTX*n* should be routed to be as short and straight as possible to reduce wire inductance.
4. The PowerPAD should be connected to the GND layer because the pad is connected to GND internally. The PowerPAD also should be connected to the heat sink layer to reduce device temperature.

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11.2 Layout Example

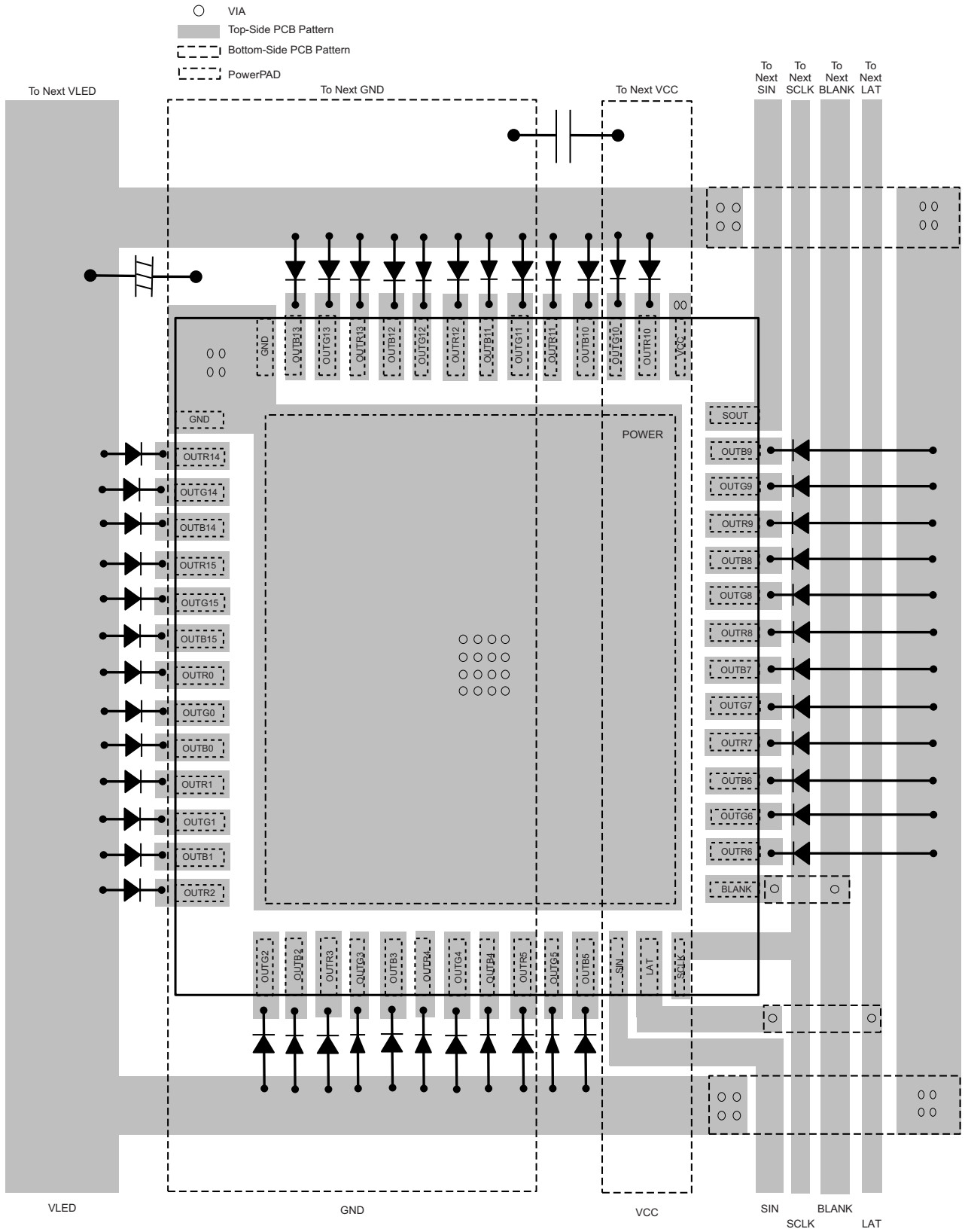

Figure 41. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For the LED driver solution, go to www.ti.com/solution/lighting_signage.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- PowerPAD™ Thermally Enhanced Package Application Report, SLMA002

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC5954RTQR	Active	Production	QFN (RTQ) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5954
TLC5954RTQR.A	Active	Production	QFN (RTQ) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5954
TLC5954RTQRG4	Active	Production	QFN (RTQ) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5954
TLC5954RTQRG4.A	Active	Production	QFN (RTQ) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5954
TLC5954RTQT	Active	Production	QFN (RTQ) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5954
TLC5954RTQT.A	Active	Production	QFN (RTQ) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5954

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

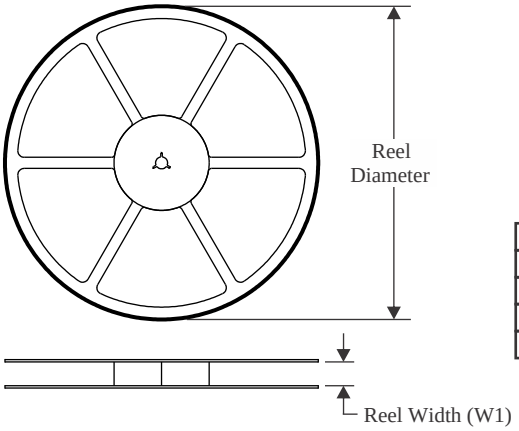
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

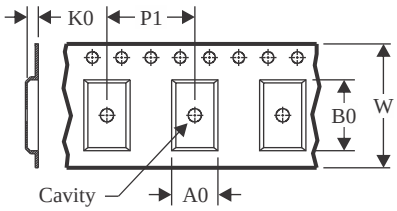
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

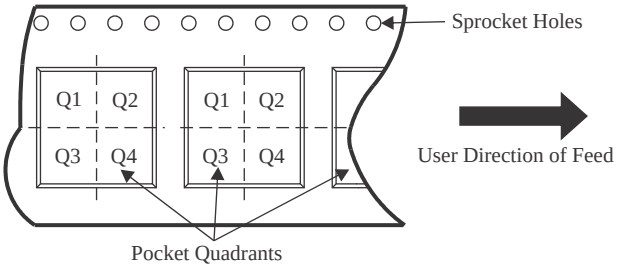


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

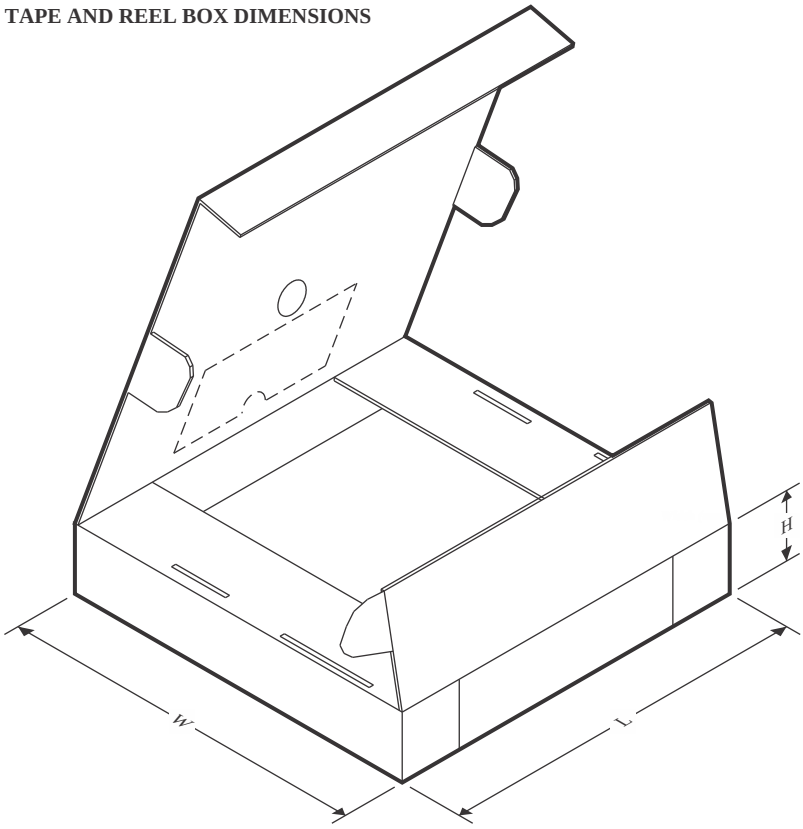
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5954RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TLC5954RTQRG4	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TLC5954RTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5954RTQR	QFN	RTQ	56	2000	367.0	367.0	38.0
TLC5954RTQRG4	QFN	RTQ	56	2000	367.0	367.0	38.0
TLC5954RTQT	QFN	RTQ	56	250	210.0	185.0	35.0

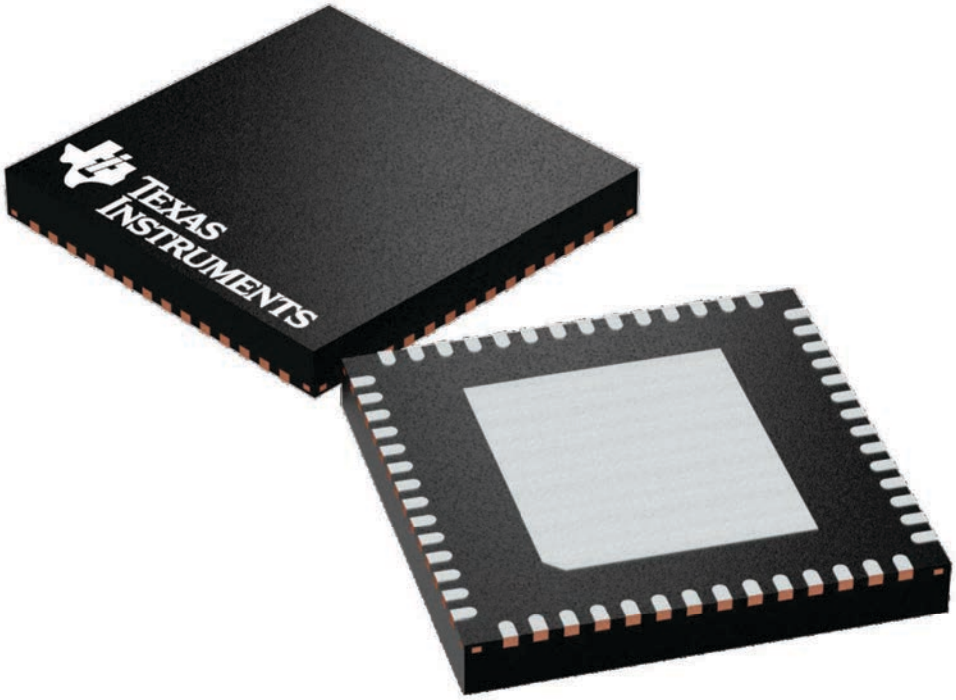
GENERIC PACKAGE VIEW

RTQ 56

VQFN - 1 mm max height

8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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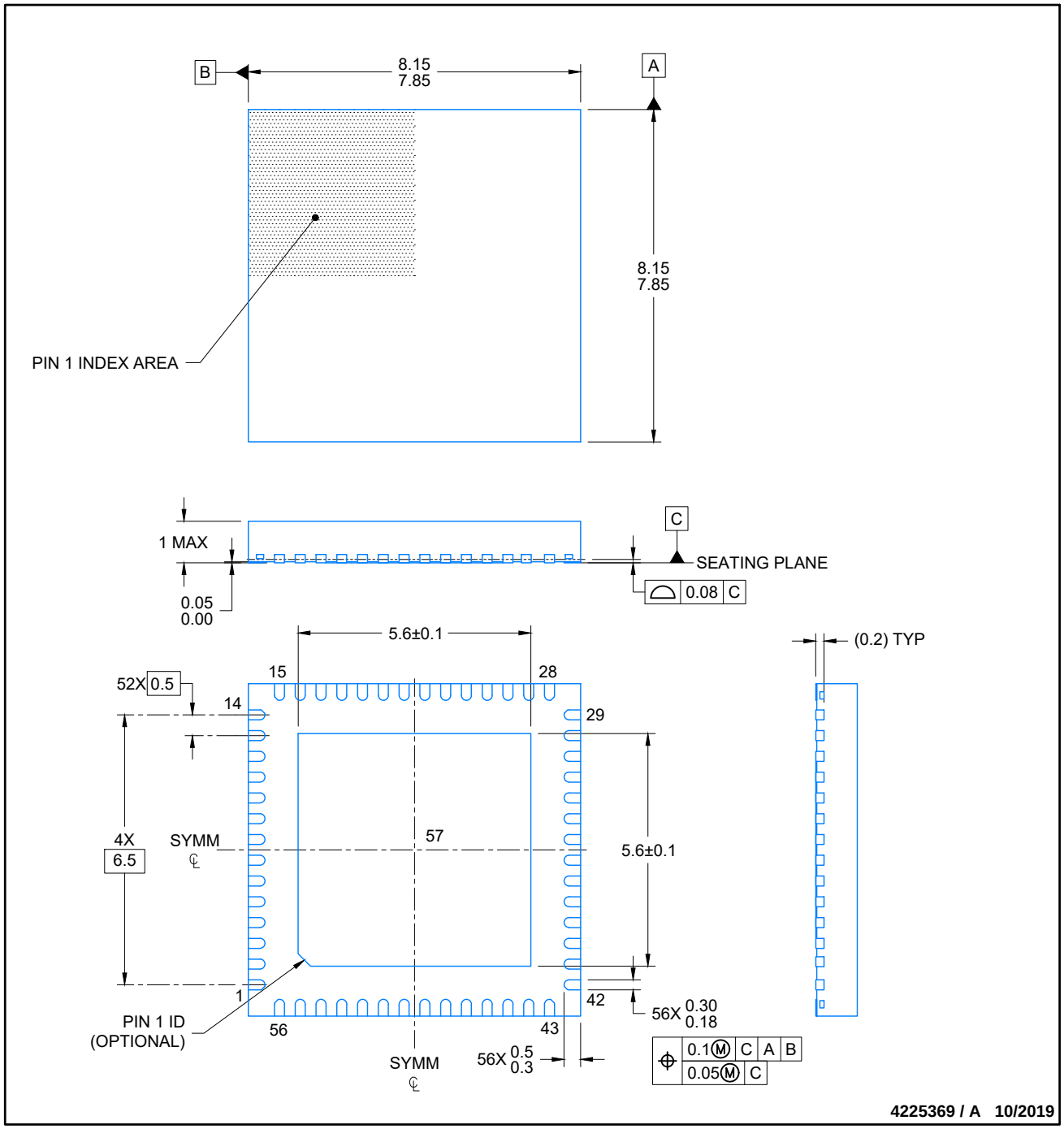
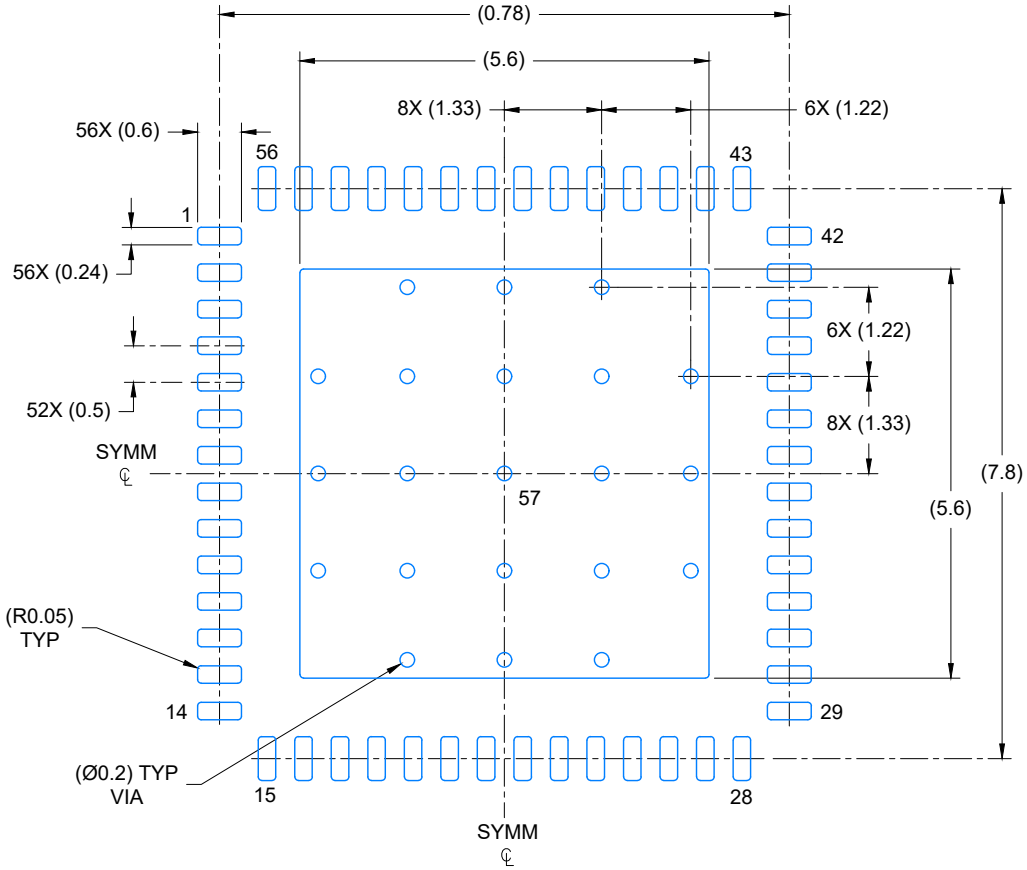
PLASTIC QUAD FLATPACK-NO LEAD

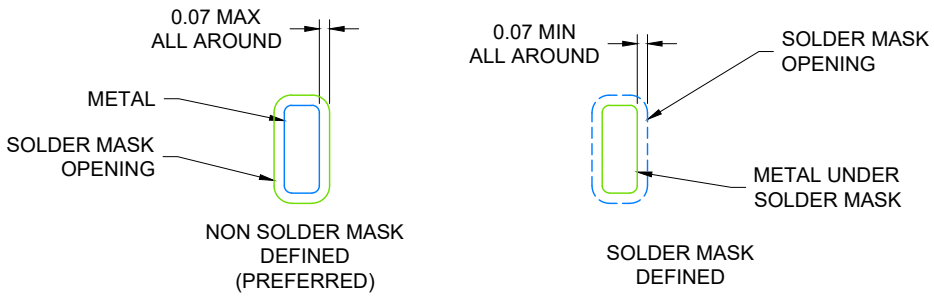


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 10X



SOLDER MASK DETAILS

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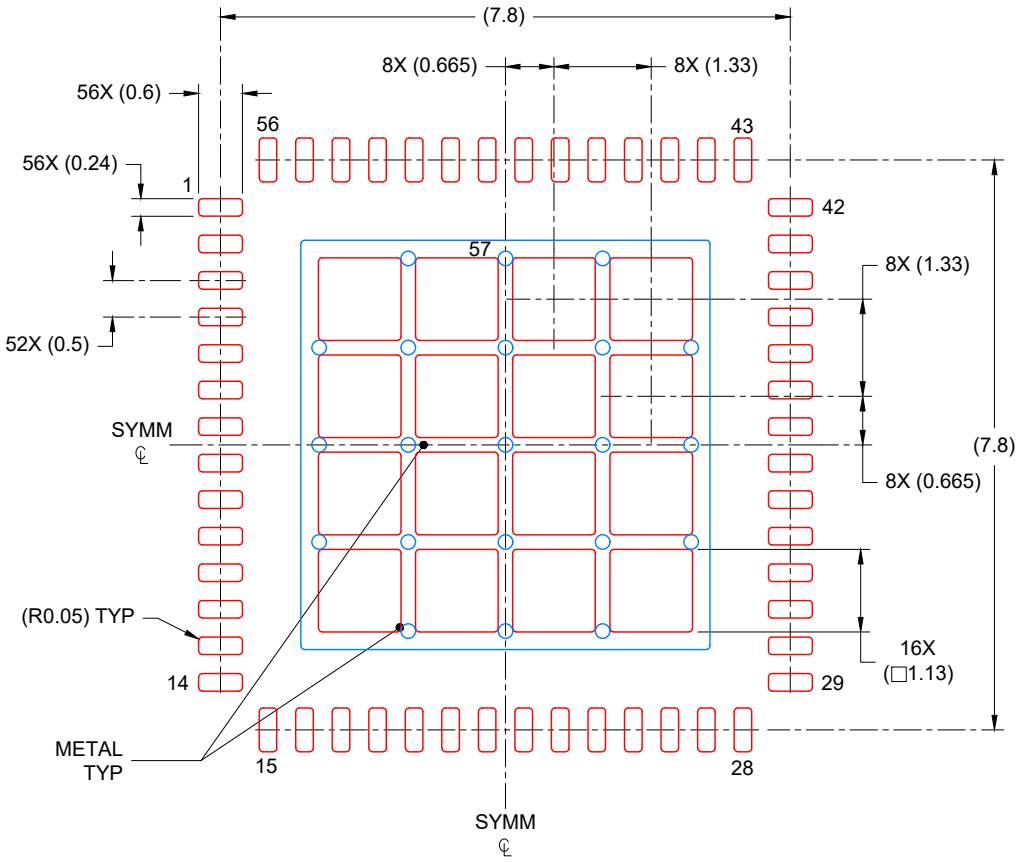
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. it is recommended thar vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
66% PRINTED COVERAGE BY AREA
SCALE: 10X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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