Micropower 250-mA CMOS LDO Regulator With Error Flag and Power-On-Reset

Check for Samples: LP3997

FEATURES

- **Low 140-mV Dropout at 250-mA Load**
- **Stable With Ceramic Capacitor.**
- **Low Noise With Bypass Capacitor**
- **Less Than 80 µA Typical I_Q at 250 mA**
- **Virtually Zero I_Q (Disabled)**
- **Thermal and Short Circuit Protection**
- **3.3-V Output** (1)
- **8-Lead VSSOP Package** (2)

APPLICATIONS

- **Portable Consumer Electronics**
- **Cellular Handsets**
- **Laptop and Palm Computers**
- **PDAs**
- **Digital Cameras**

(1) For other voltage options, contact your TI sales office
(2) For other package options, contact your TI sales office.

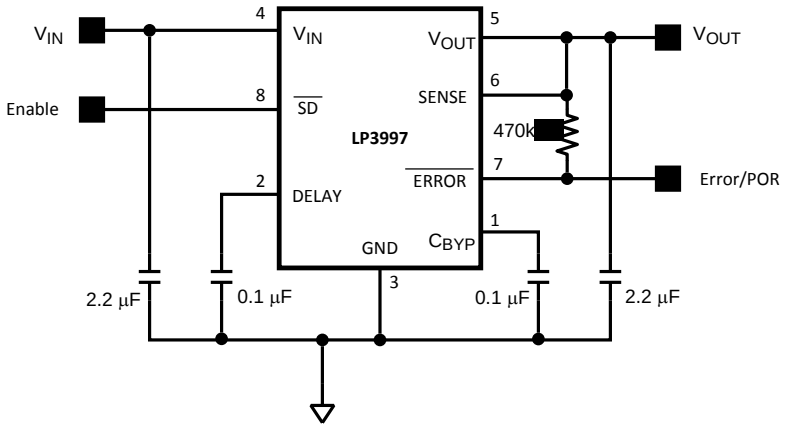
DESCRIPTION

The LP3997 regulator is designed to meet the requirements of portable, battery-powered systems, providing accurate output voltage, low noise, and low quiescent current. The LP3997 provides 3.3V output at up to 250mA load current. The chip architecture is capable of providing output voltages as low as 0.8V. When switched in shutdown mode, the power consumption is virtually zero.

The LP3997 is designed to be stable with space saving ceramic output capacitor as small as 1µF.

The LP3997 also includes an out-of-regulation error flag. When the output is more than 5% below its nominal voltage, the error flag sets to low. If a capacitor is connected to device's delay pin, a delayed power-on reset signal will be generated.

Typical Application Circuit



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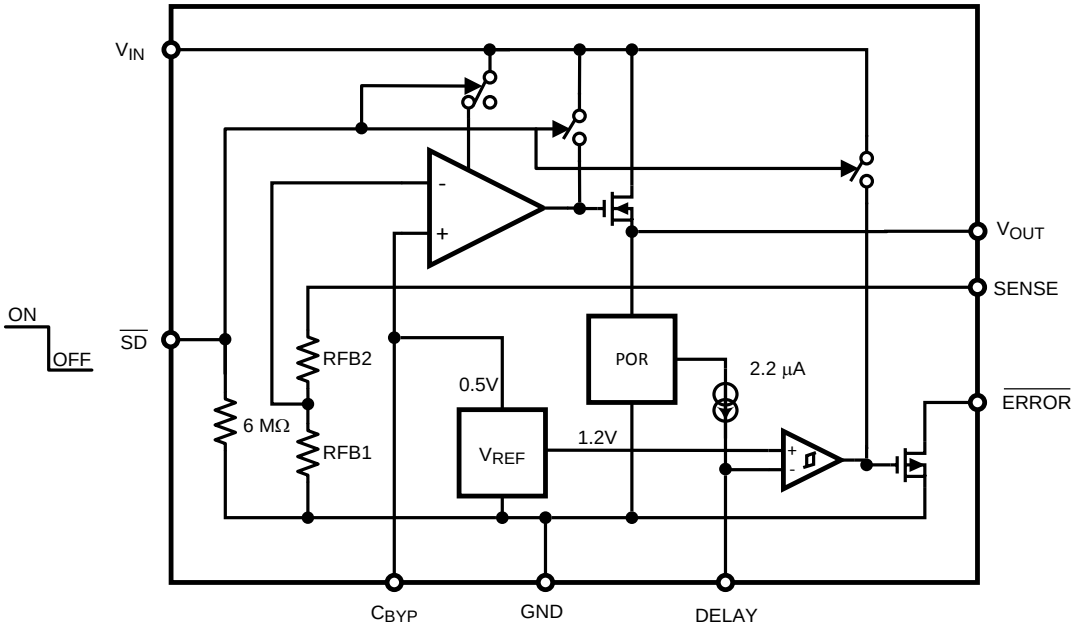
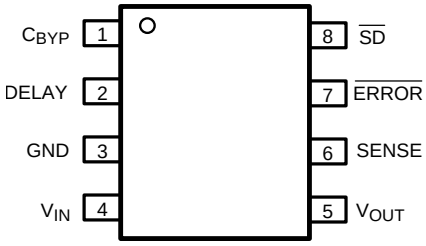
Functional Block Diagram



Pin Descriptions

Pin No.	Name	Description
1	C_{BYP}	Noise bypass pin. For low noise applications a 0.1µF or larger ceramic capacitor should be connected from this pin to ground. This will also improve PSSR.
2	DELAY	A capacitor connected from this pin to ground will allow a delayed power-on-reset signal at the ERROR (pin 7) output. See Applications Information.
3	GND	Ground pin. Local ground for C_{BYP} ,C_{IN}, C_{OUT} and C_{DELAY}.
4	V_{IN}	Input supply pin. Connect C_{IN} between this pin and GND.
5	V_{OUT}	Output voltage, Connect C_{OUT} between this pin and ground.
6	SENSE	Connect this pin to V_{OUT} (pin 5). For best performance the connection should be made as close to the load as possible.
7	$\overline{\text{ERROR}}$	This open drain output is an error flag output which goes low when V_{OUT} drops 5% below its nominal voltage. This pin also provides a power-on-reset signal if a capacitor is connected to the DELAY pin.
8	$\overline{\text{SD}}$	Shutdown. Disables the regulator when less than 0.4V is applied. Enables the regulator when greater than 0.9V. The Shutdown pin is pulled down internally by a 6MΩ resistor.

Connection Diagram



8-Lead VSSOP
Package Number DGK

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1] [2][3]

Input Voltage			-0.3 to 6.5V
Output Voltage			-0.3 to (V_{IN} + 0.3V) with 6.5V (max)
$\overline{SD}$ Input Voltage			-0.3 to (V_{IN} + 0.3V) with 6.5V (max)
Junction Temperature			150°C
Lead/Pad Temp.			
VSSOP			260°C
Storage Temperature			-65 to 150°C
Continuous Power Dissipation			Internally Limited[4]
ESD	All Pins Except C_{BYP}	Human Body Model[5]	2KV
		Machine Model	200V
	C_{BYP} Pin	Human Body Model[5]	1KV
		Machine Model	100V

(1) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All Voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.
(5) The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Operating Ratings[1]

Input Voltage	2V to 6V
Junction Temperature	-40°C to 125°C
Ambient Temperature T_A Range[2]	-40°C to 85°C

(1) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$.

Thermal Properties[1]

Junction To Ambient Thermal Resistance[2], θ_{JA} (VSSOP)	210°C/W

(1) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.

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Electrical Characteristics

Unless otherwise noted, $\overline{SD}$ = 950mV, V_{IN} = V_{OUT} + 1.0V, C_{IN} = 2.2 µF, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF and C_{BYP} = 0.1 µF. Typical values and limits appearing in normal type apply for T_J = 27°C. Limits appearing in **boldface** type apply over the full temperature range for operation, −40 to +125°C. (1)

Symbol	Parameter	Test Conditions		Typ	Limit		Unit
					Min	Max	
V_{IN}	Input Voltage				2	6	V
ΔV_{OUT}	Output Voltage Tolerance	Over full line and load regulation			-1.5	+1.5	%
					-3	**+3**	
	Line Regulation Error	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 6.0V, I_{OUT} = 1mA		0.02		**0.3**	%/V
	Load Regulation Error	I_{OUT} = 1mA to 250mA		20		**80**	µV/mA
V_{DO}	Dropout Voltage (2)	I_{OUT} = 250mA		140		**400**	mV
I_{LOAD}	Load Current	See (3) (4)			0		µA
I_Q	Quiescent Current	$\overline{SD}$ = 950mV, I_{OUT} = 0mA		55		**100**	µA
		$\overline{SD}$ = 950mV, I_{OUT} = 250mA		80		**150**	
		$\overline{SD}$ = 0.4V		0.01		0.5	
I_{SC}	Short Circuit Current Limit	See (5)		600		**1000**	mA
I_{OUT}	Maximum Output Current				**250**		mA
PSRR	Power Supply Rejection Ratio	C_{BYP} = 0.1µF	f = 1kHz, I_{OUT} = 1mA to 150mA	61			dB
			f = 10kHz, I_{OUT} = 150mA	55			
		Without C_{BYP}	f = 1kHz, I_{OUT} = 1mA to 150mA	61			
			f = 10kHz, I_{OUT} = 150mA	39			
e_n	Output noise Voltage (4)	BW = 10Hz to 100kHz, V_{IN} = $V_{OUT(nom)}$ +1V	w/o C_{BYP}	180			μV_{RMS}
			C_{BYP} = 0.1µF	100			
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature		150			°C
		Hysteresis		10			
Shutdown Control Characteristics							
$I_{\overline{SD}}$	Maximum Input Current at $\overline{SD}$ Input	$\overline{SD}$ = 0.0V		0.01			µA
		$\overline{SD}$ = 6V (6)		1			
V_{IL}	Low Input Threshold	V_{IN} = 2V to 6V				**0.4**	V
V_{IH}	High Input Threshold	V_{IN} = 2V to 6V			**0.95**		V
Error Flag Characteristics							
V_{TH}	Power Good Trip Threshold	V_{IN} Rising		95	91	99	$\%V_{OUT}$
V_{HYST}	Hysteresis	V_{IN} Rising or Falling		2.5			$\%V_{OUT}$
V_{OL}	ErrorError OutputOutput low Voltage	I_{SINK} = 2mA		0.1		**0.4**	V
I_{OFF}	Error Output High Leakage	$\overline{ERROR}$ = $V_{OUT(NOM)}$		10		**2000**	nA
I_{DELAY}	Delay Pin Current Source	V_{OUT} > 95% $V_{OUT(NOM)}$		2.2	1.2	3	µA

(1) All limits are ensured. All electrical characteristics having room-temperature limits are tested during production at T_J = 25°C or correlated using Statistical Quality Control methods. Operation over the temperature specification is ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Dropout voltage is defined as the voltage difference between input and output when the output voltage drops 100mV below its nominal value.
(3) The device maintains the regulated output voltage without the load.
(4) This electrical specification is ensured by design.
(5) Short circuit current is measured on the input supply line at the point when the short circuit condition reduces the output voltage to 5% of its nominal value.
(6) $\overline{SD}$ Pin has 6MΩ typical, resistor connected to GND.

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Electrical Characteristics (continued)

Unless otherwise noted, $\overline{SD}$ = 950mV, V_{IN} = V_{OUT} + 1.0V, C_{IN} = 2.2 µF, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF and C_{BYP} = 0.1 µF. Typical values and limits appearing in normal type apply for T_J = 27°C. Limits appearing in **boldface** type apply over the full temperature range for operation, −40 to +125°C. (1)

Symbol	Parameter	Test Conditions		Typ	Limit		Unit
					Min	Max	
Timing Characteristics							
t_{ON}	Turn On Time (7)	To 95% Level	w/o C_{BYP}	150		**250**	µs
			C_{BYP} = 0.1µF	2			ms
Transient Response	Line Transient Response $\lvert\delta V_{OUT}\rvert$	T_{rise} = T_{fall} = 30µs (7) δV_{IN} = 600mV	w/o C_{BYP}	40			mV (pk - pk)
			C_{BYP} = 0.1µF	4			
	Load Transient Response $\lvert\delta V_{OUT}\rvert$	T_{rise} = T_{fall} = 1µs (7) I_{OUT} = 1mA to 150mA		70		**80**	mV

(7) This electrical specification is ensured by design.

Output Capacitor, Recommended Specifications

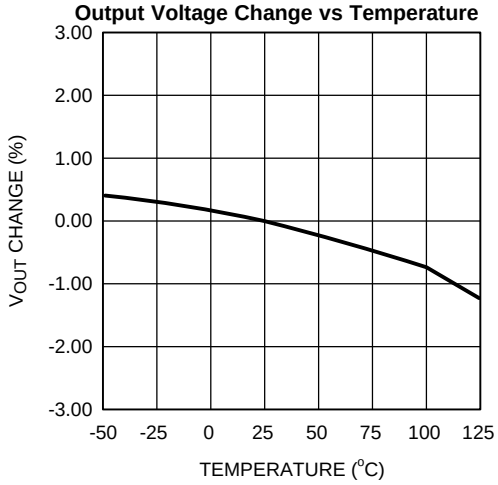
Symbol	Parameter	Conditions	Typ	Limit		Unit
				Min	Max	
C_o	Output Capacitor	Capacitance (1)	2.2	0.7		µF
		ESR		5	500	mΩ

(1) The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. (See capacitor characteristics section in Applications Information).

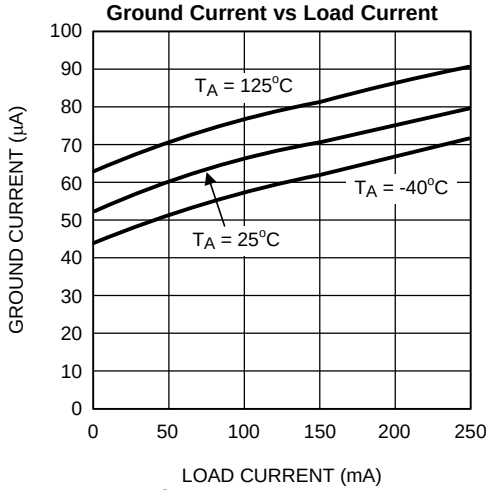
Typical Performance Characteristics.

Unless otherwise noted, $\overline{SD}$ = 950mV, $V_{IN} = V_{OUT}$ + 1.0V, C_{IN} = 2.2 µF, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF and C_{BYP} = 0.1 µF. Typical values and limits appearing in normal type apply for T_J = 27°C. Limits appearing in **boldface** type apply over the full temperature range for operation, −40 to +125°C.

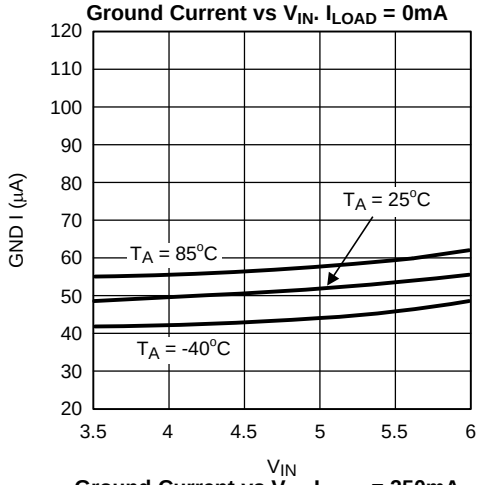
Output Voltage Change vs Temperature



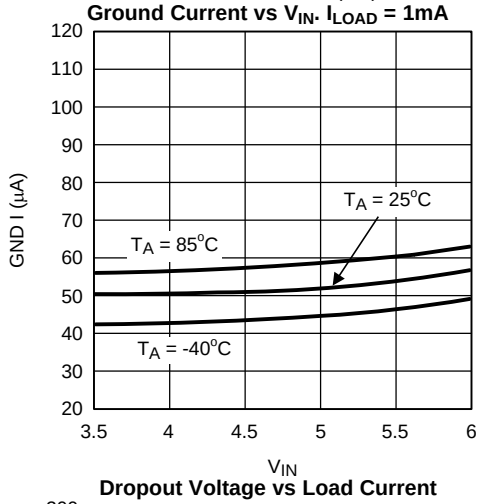
Ground Current vs Load Current



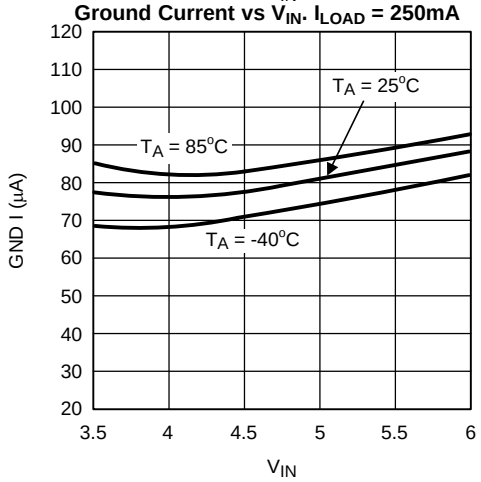
Ground Current vs V_{IN}. I_{LOAD} = 0mA



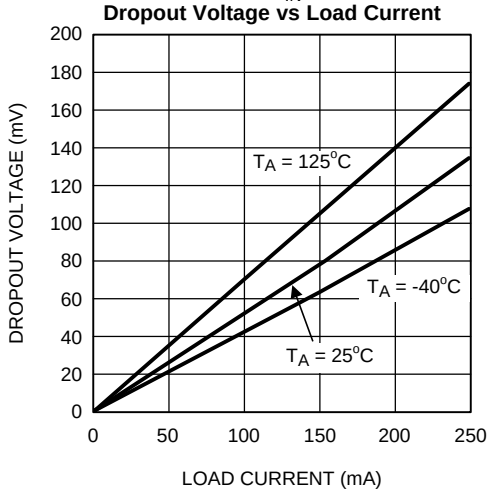
Ground Current vs V_{IN}. I_{LOAD} = 1mA



Ground Current vs V_{IN}. I_{LOAD} = 250mA



Dropout Voltage vs Load Current



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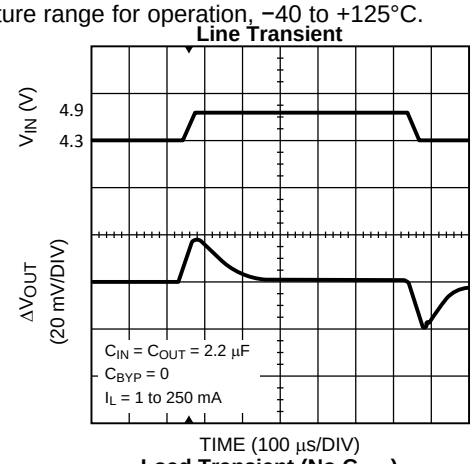
Typical Performance Characteristics. (continued)

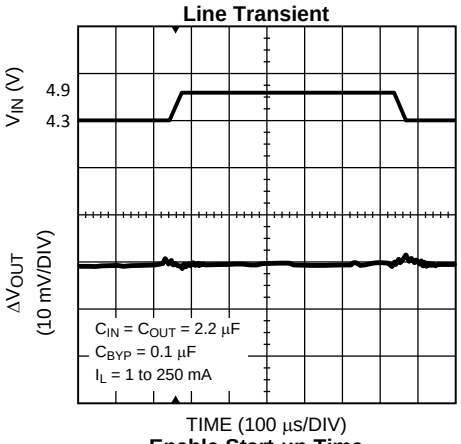
Unless otherwise noted, $\overline{SD}$ = 950mV, $V_{IN} = V_{OUT}$ + 1.0V, C_{IN} = 2.2 µF, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF and C_{BYP} = 0.1 µF.

Typical values and limits appearing in normal type apply for T_J = 27°C. Limits appearing in **boldface** type apply over the full temperature range for operation, −40 to +125°C.

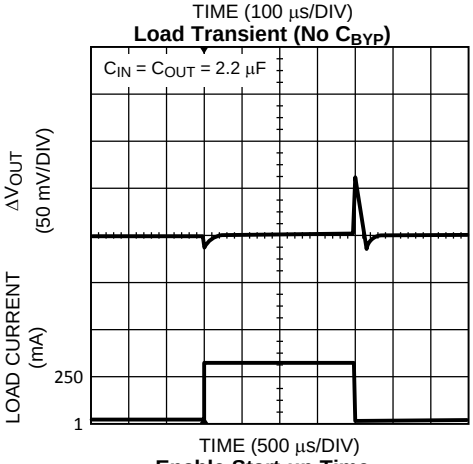
Line Transient



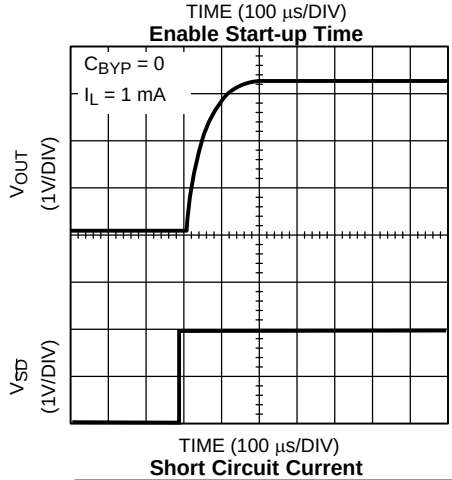
Line Transient



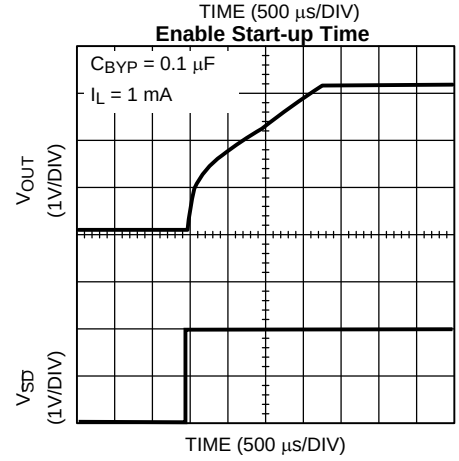
Load Transient (No C_{BYP})



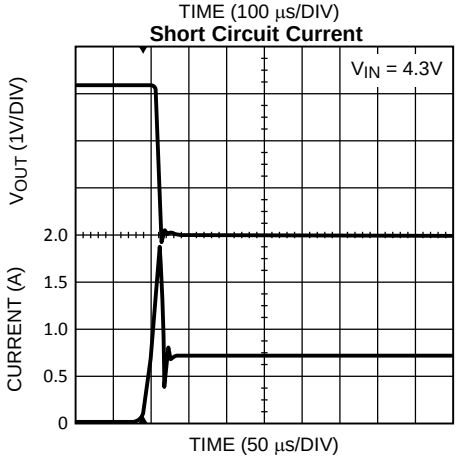
Enable Start-up Time



Enable Start-up Time



Short Circuit Current



Typical Performance Characteristics. (continued)

Unless otherwise noted, $\overline{SD}$ = 950mV, $V_{IN} = V_{OUT}$ + 1.0V, C_{IN} = 2.2 µF, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF and C_{BYP} = 0.1 µF.

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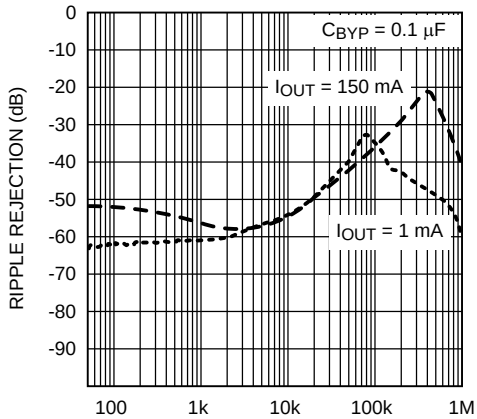
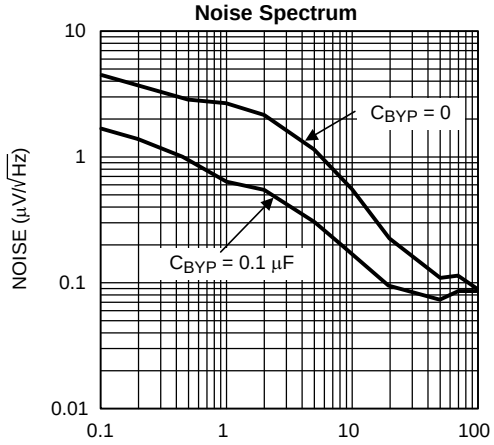
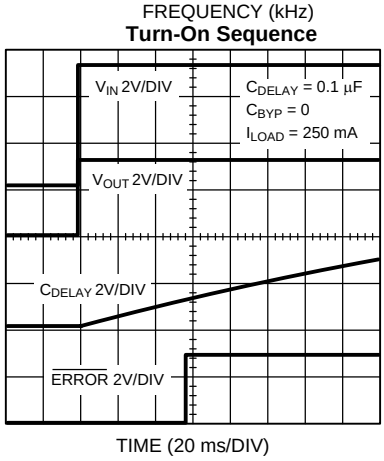
Power Supply Rejection Ratio



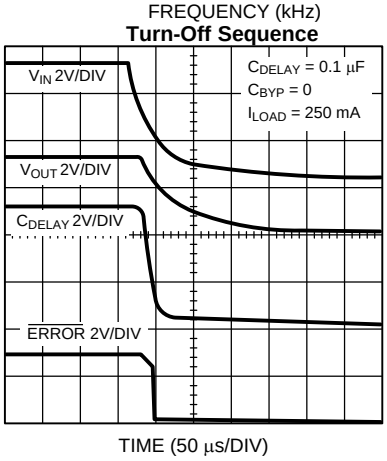
Noise Spectrum



Turn-On Sequence



Turn-Off Sequence



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Applications Information

External Capacitors

In common with most regulators, the LP3997 requires the inclusion of external capacitors.

V_{IN}

An input capacitor is required for stability. It is recommended that a minimum of 1.0µF capacitor is connected between the LP3997 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB design practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long wire leads are used to connect the battery or other power source to the LP3997, then it is recommended to increase the input capacitor to at least 2.2µF. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain ≅ 1.0µF over the entire operating temperature range.

V_{OUT}

V_{OUT} is the output voltage of the regulator. Connect capacitance (minimum 1.0µF) to ground from this pin. To ensure stability the capacitor must meet the minimum value for capacitance and have an ESR in the range 5mΩ to 500mΩ. Ceramic X7R types are recommended. If an output capacitor larger than 4.7µF is fitted then checks on in-rush current, transient performance and stability, should be made.

SENSE

SENSE is used to sense the output voltage. Connect sense to V_{OUT}

SHUTDOWN

$\overline{SD}$ controls the turning on and off of the LP3997. V_{OUT} is ensured to be on when the voltage on the $\overline{SD}$ pin is greater than 0.95V. V_{OUT} is ensured to be off when the voltage on the $\overline{SD}$ pin is less than 0.4V.

$\overline{ERROR}$

$\overline{ERROR}$ is an open drain output which is set low when V_{OUT} is more than 5% below its nominal value. An external pull up resistor is required on this pin. When a capacitor is connected from DELAY to GROUND, the error signal is delayed (see DELAY section). This delayed error signal can be used as the power-on reset signal for the application system. The $\overline{ERROR}$ pin is disconnected when not used.

DELAY

A capacitor from DELAY to GROUND sets the time delay for $\overline{ERROR}$ changing from low to high state. The delay time is set by the following formula.

$$t_{DELAY} = \frac{V_{TH(DELAY)} \times C_{DELAY}}{I_{DELAY}}$$

$V_{TH(DELAY)}$ is nominally 1.2V.

The DELAY pin should be open circuit if not used.

C_{BYP}

For low noise application, connect a high frequency ceramic capacitor from C_{BYP} to ground, A 0.01µF to 0.1µF X5R or X7R is recommended. This capacitor is connected directly to high impedance node in the band gap reference circuit. Any significant loading on this node will cause a change in the regulated output voltage. For this reason, DC leakage current from this pin must be kept as low as possible for best output voltage accuracy.

CAPACITOR CHARACTERISTICS

In common with most regulators, the LP3997 requires external capacitors for regulator stability. The LP3997 is specifically designed for portable applications requiring minimum board space and can use capacitors in the range 1µF to 4.7µF.These capacitors must be correctly selected for good performance. Ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3997.These capacitors must be correctly selected to ensure good performance of the LP3997.

For both input and output capacitors careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type.

In particular the output capacitor selection should take account of all the capacitor parameters to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general. As an example Figure 1 shows a typical graph showing a comparison of capacitor case sizes in a Capacitance versus DC Bias plot. As shown in the graph, as a result of the DC Bias condition, the capacitance value may drop below the minimum capacitance value given in the recommended capacitor table (0.7µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

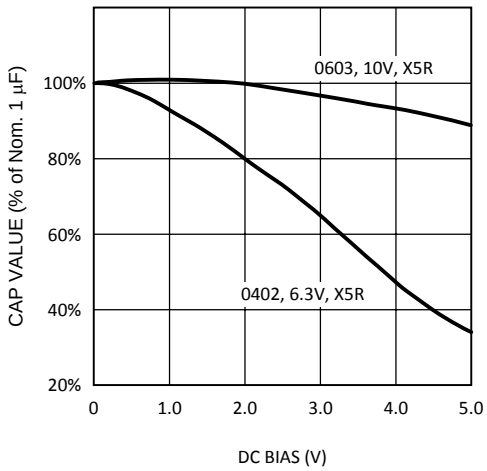

Figure 1. Capacitance versus DC Bias Plot

The value of ceramic capacitors can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55°C to +85°C. Most large value ceramic capacitors, larger than 1µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature goes from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

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Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	11

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3997MM-3.3/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SAKB
LP3997MM-3.3/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SAKB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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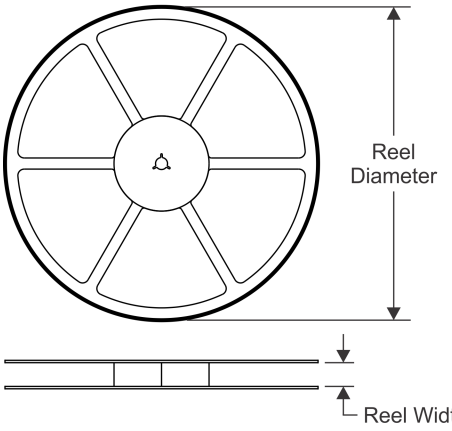
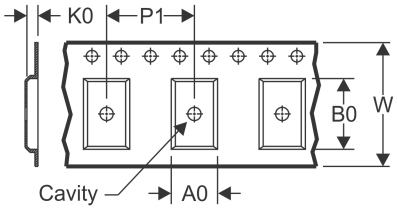
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

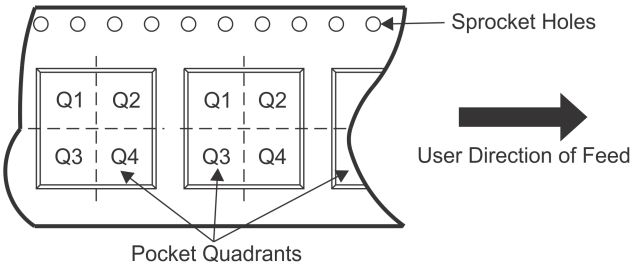


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

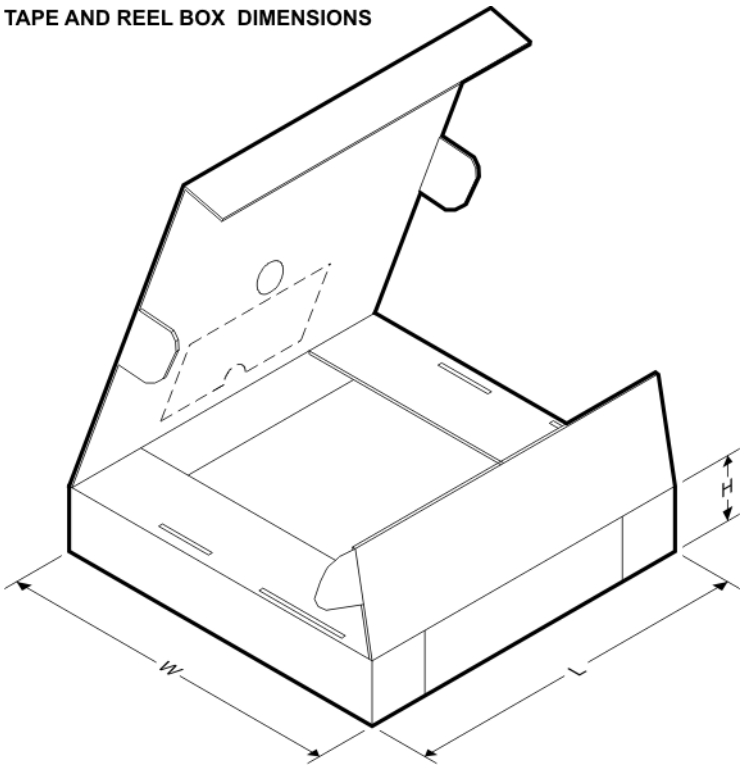
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3997MM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

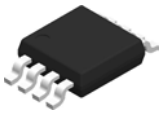


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3997MM-3.3/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0

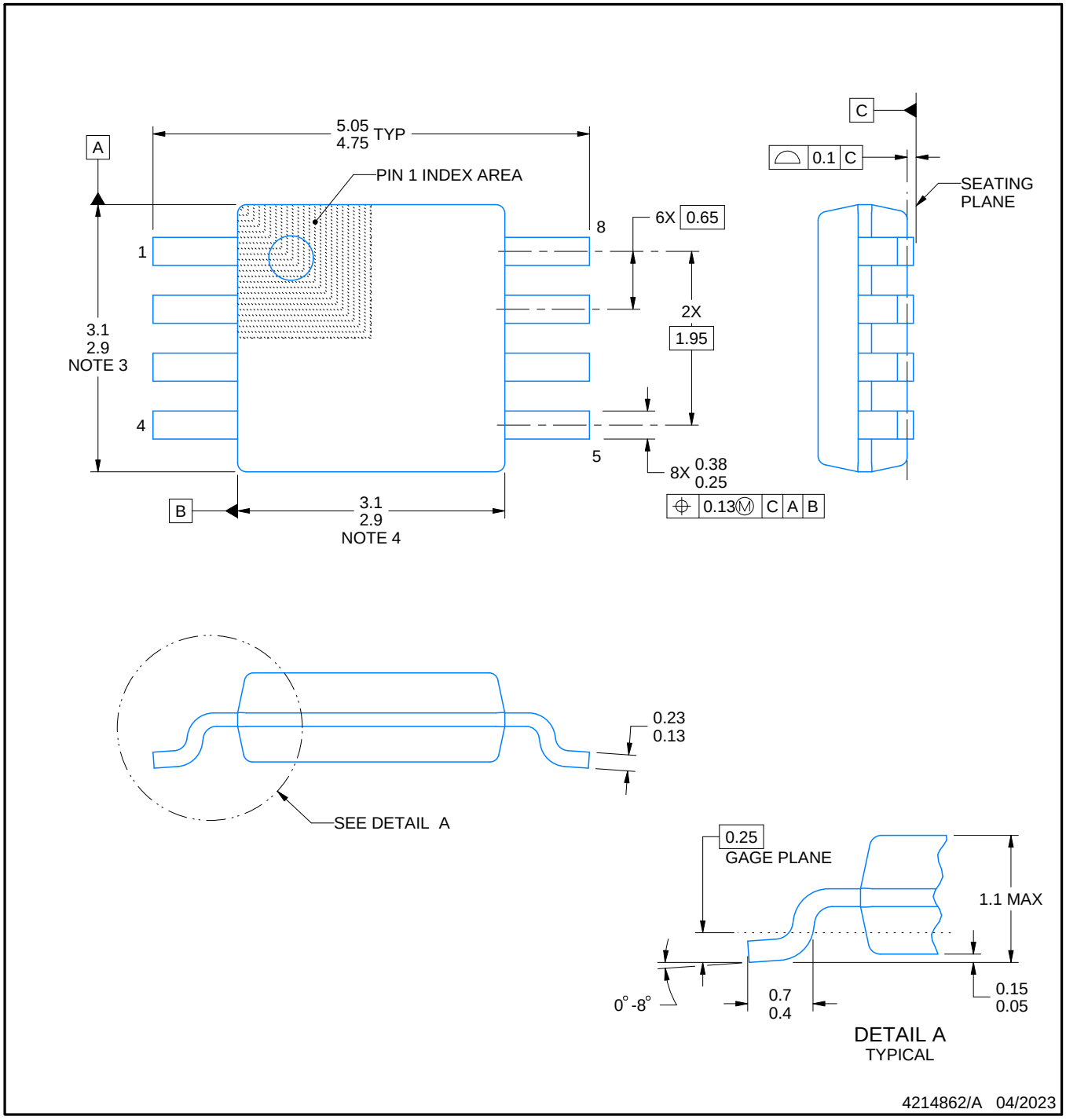
PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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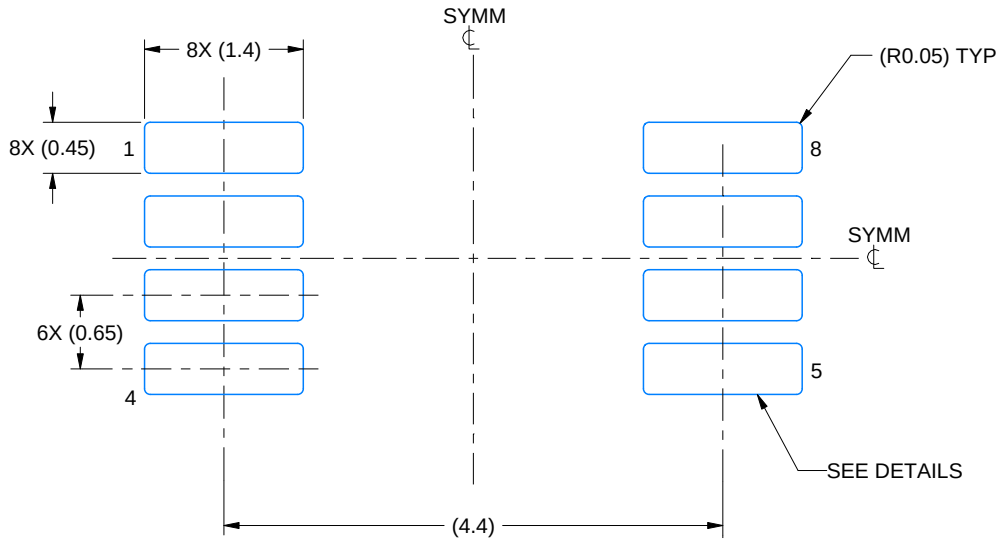
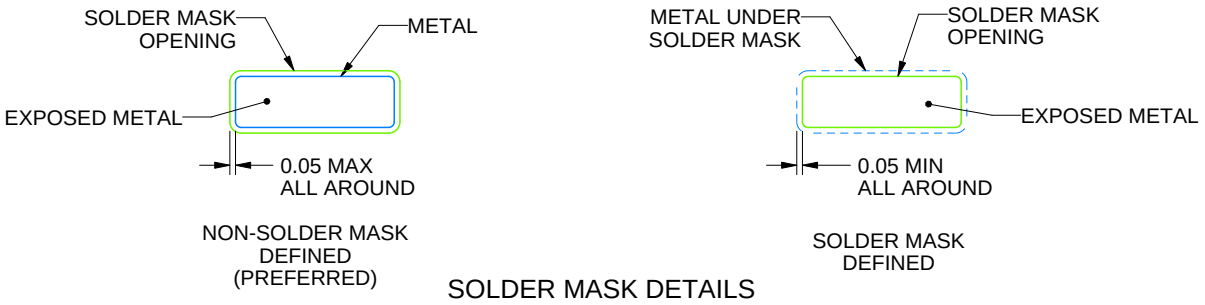
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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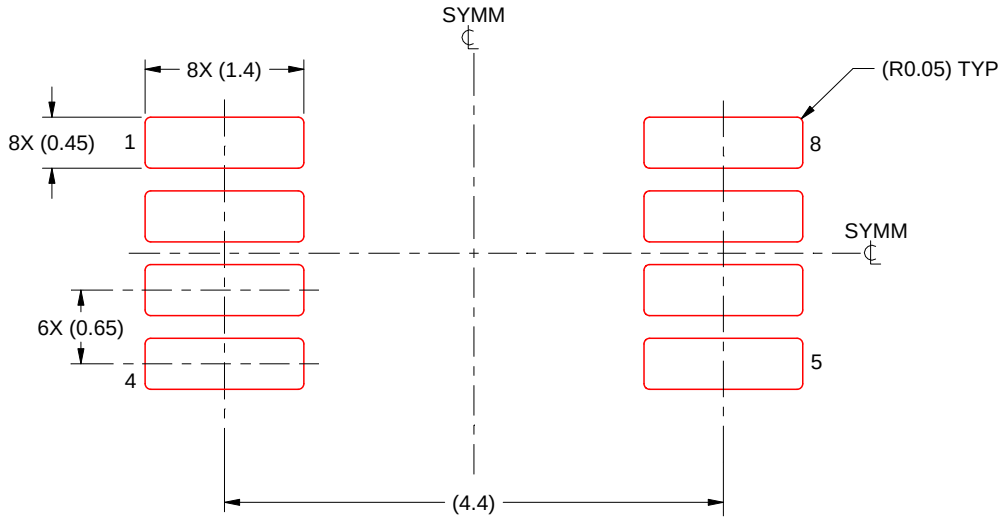
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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