LMH0387 3 Gbps HD/SD SDI Configurable I/O Adaptive Cable Equalizer / Cable Driver

1 Features

- ST 424, ST 292, ST 344, and ST 259 Compliant (1)
- Supports DVB-ASI at 270 Mbps
- Data Rates: 125 Mbps to 2.97 Gbps when Receiving (DC to 2.97 Gbps when Driving Cable)
- Equalizes up to 120 Meters of Belden 1694A at 2.97 Gbps, up to 200 Meters of Belden 1694A at 1.485 Gbps, or up to 400 Meters of Belden 1694A at 270 Mbps
- Integrated Return Loss Network (No External Components Required)
- Power Saving Modes
- Cable Driver Selectable Slew Rate
- Internally Terminated 100-Ω LVDS Receiver Outputs With Programmable Common Mode Voltage and Swing
- Programmable Launch Amplitude Optimization for Receiver
- Cable Length Indication
- Single 3.3-V Supply Operation
- 48-Pin Laminate TLGA Package
- Industrial Temperature Range: −40°C to 85°C

2 Applications

- ST 424 (SMPTE 424M), ST 292 (SMPTE 292M), and ST 259 (SMPTE 259M) Serial Digital Interfaces (1)
- Digital Video Servers and Modular Equipment
- Video Encoders and Decoders
- Distribution Amplifiers

(1) Due to SMPTE naming convention, all SMPTE Engineering Documents will be numbered as a two-letter prefix and a number. Documents and references with the same root number and year are functionally identical; for example ST 424-2006 and SMPTE 424M-2006 refer to the same document.

3 Description

The LMH0387 3 Gbps HD/SD SDI Configurable I/O Adaptive Cable Equalizer / Cable Driver provides a single chip interface to a BNC. The device can be configured either in the input mode as an equalizer to receive data over coaxial cable or in the output mode as a cable driver to transmit data over coaxial cable. The same I/O pin is used both for the input and the output functions of the device, allowing the system designer the flexibility to use a BNC attached to the device as either an input or an output.

The device operates over a wide range of data rates from 125 Mbps to 2.97 Gbps (DC to 2.97 Gbps when driving cable) and supports ST 424, ST 292, ST 344, and ST 259. The return loss network is integrated within the device so no external components are required to meet the SMPTE return loss specification. The LMH0387 offers designers flexibility in system design and quicker time to market.

In the input mode, the LMH0387 features include a power-saving sleep mode, programmable output common mode voltage and swing, cable length indication, launch amplitude optimization, input signal detection, and an SPI interface. In the output mode, the LMH0387 features include two selectable slew rates for ST 424 / 292 and ST 259 compliance, and output driver power-down control.

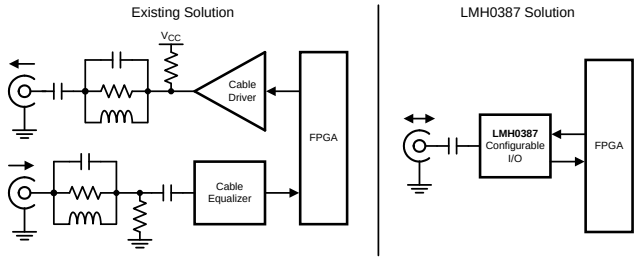
The device is available in a 7-mm × 7-mm 48-pin laminate Thin Laminate Grid Array (TLGA) Package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH0387	TLGA (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2013) to Revision H **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision F (April 2013) to Revision G **Page**

- Changed layout of National Data Sheet to TI format ... 18

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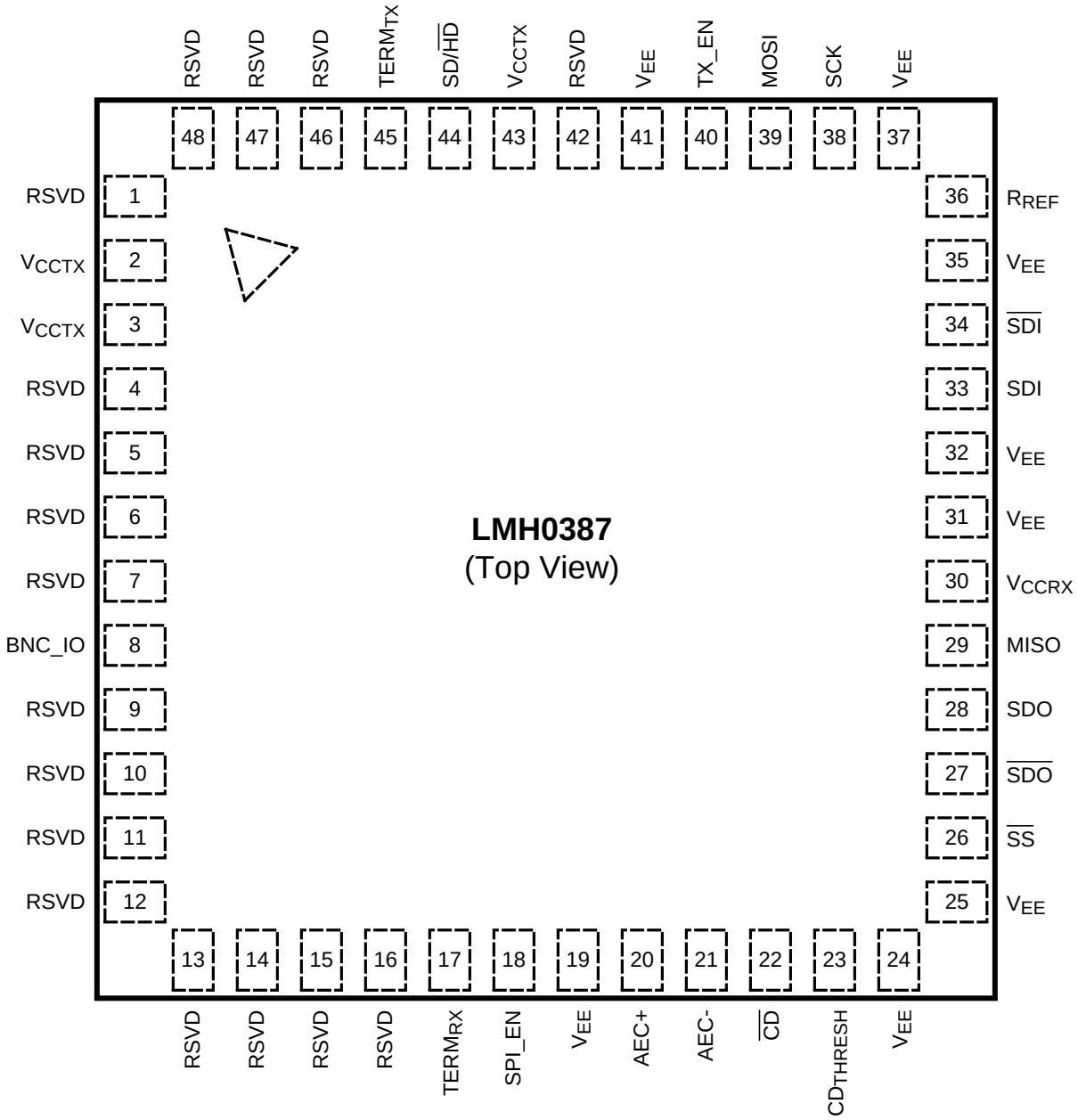
5 Pin Configuration and Functions

NPD Package
48-Pin TLGA
Top View



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
AEC+, AEC-	20, 21	I/O, Analog	AEC loop filter external capacitor for equalizer (1 µF connected between AEC+ and AEC-).
BNC_IO	8	I/O, Analog	Serial digital interface input or output for connection to a BNC. Connect this pin to the BNC through an AC coupling capacitor (nominally 4.7 µF).
$\overline{CD}$	22	O, LVCMOS	Carrier detect for BNC_IO pin. H = No input signal detected on BNC_IO pin. L = Input signal detected on BNC_IO pin.
CD_{THRESH}	23	I, Analog	Carrier detect threshold input. Sets the threshold for $\overline{CD}$. CD_{THRESH} may be either unconnected or connected to ground for normal $\overline{CD}$ operation.
MISO (SPI)	29	O, LVCMOS	SPI Master Input / Slave Output. LMH0387 control data transmit.
MOSI (SPI)	39	I, LVCMOS	SPI Master Output / Slave Input. LMH0387 control data receive.
R_{REF}	36	I, Analog	BNC_IO output driver level control. Connect a resistor (nominally 715 Ω) to V_{CC} to set the output voltage swing for the BNC_IO pin.
RSVD	1, 4-7, 9–16, 42, 46-48	N/A	Do not connect.
SCK (SPI)	38	I, LVCMOS	SPI serial clock input.
SD/$\overline{HD}$	44	I, LVCMOS	BNC_IO output slew rate control. SD/$\overline{HD}$ has an internal pulldown. H = BNC_IO output rise/fall time complies with SMPTE 259M (SD). L = BNC_IO output rise/fall time complies with SMPTE 424M / 292M (3G/HD).
SDI, $\overline{SDI}$	33, 34	I, Analog	Serial data differential input for transmitter (cable driver).
SDO, $\overline{SDO}$	27, 28	O, LVDS	Serial data differential output from receiver (equalizer).
SPI_EN	18	I, LVCMOS	SPI register access enable (equalizer). This pin should always be high; it must be pulled high while operating in the input mode and may optionally be pulled high while operating in the output mode. This pin has an internal pulldown.
$\overline{SS}$ (SPI)	26	I, LVCMOS	SPI slave select. This pin has an internal pullup.
$TERM_{RX}$	17	I, Analog	Termination for unused receiver (equalizer) input. This network should consist of a 1-µF capacitor followed by a 220-Ω resistor to ground.
$TERM_{TX}$	45	O, Analog	Termination for unused transmitter (cable driver) output. This network should consist of a 4.7-µF capacitor followed by a 75-Ω resistor to ground.
TX_EN	40	I, LVCMOS	Transmitter output driver enable. TX_EN has an internal pullup. H = BNC_IO output driver is enabled. L = BNC_IO output driver is powered off. To configure the LMH0387 as a receiver, the BNC_IO output driver must be disabled by tying TX_EN low. To configure the LMH0387 as a transmitter, the output driver must be enabled by tying TX_EN high and the receiver may be powered down using the sleep mode setting through the SPI.
V_{CCTX}	2, 3, 43	Power	Positive power supply for transmitter (3.3 V).
V_{EE}	19, 24, 25, 31, 32, 35, 37, 41	Power	Negative power supply (ground).
V_{CCRX}	30	Power	Positive power supply for receiver (3.3 V).

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply Voltage		4	V
Input Voltage (all inputs)	−0.3	V_{CC}+0.3	V
Junction Temperature		125	°C
Storage Temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2500	
	Machine model	±300	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage (V_{CC} – V_{EE})	3.14	3.3	3.46	V
BNC_IO Input / Output Coupling Capacitance		4.7		µF
AEC Capacitor (Connected between AEC+ and AEC-)		1		µF
Operating Free Air Temperature (T_A)	−40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMH0387 NPD (TLGA) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Control Pin Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input Voltage High Level		2		V_{CC}	V
V_{IL}	Input Voltage Low Level		V_{EE}		0.8	V
V_{OH}	Output Voltage High Level	I_{OH} = –2 mA	2.4			V
V_{OL}	Output Voltage Low Level	I_{OL} = 2 mA			0.4	V

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.
(2) Typical values are stated for V_{CC} = +3.3 V and T_A = 25°C.

6.6 Input Mode (Equalizer) DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Swing	0-m cable length(3)	720	800	950	mV_{P-P}
V_{SSP-P}	Differential Output Voltage, P-P	100-Ω load, default register settings, Figure 1(4)	500	700	900	mV_{P-P}
V_{OD}	Differential Output Voltage		250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for complementary Output States				50	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for complementary Output States				50	mV
I_{OS}	Output Short Circuit Current				30	mA
CD_{THRESH}	CD_{THRESH} DC Voltage (floating)			1.3		V
CD_{THRNG}	CD_{THRESH} Range			0.8		V
I_{CC}	Supply Current	Equalizing cable > 120 m (Belden 1694A), TX_EN = 0		91	113	mA
		Equalizing cable ≤ 120 m (Belden 1694A), TX_EN = 0(5)		71		mA
		Power save mode (equalizer in sleep mode, TX_EN = 0)		11		mA

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.
(2) Typical values are stated for V_{CC} = +3.3 V and T_A = 25°C.
(3) The LMH0387 equalizer can be optimized for different launch amplitudes through the SPI.
(4) The differential output voltage and offset voltage are adjustable through the SPI.
(5) The equalizer automatically shifts equalization stages at cable lengths less than or equal to 120 m (Belden 1694A) to reduce power consumption. This power saving is also achieved by setting Extended 3G Reach Mode = 1 through the SPI. (Note: Forcing the Extended 3G Reach Mode in this way increases the cable reach for 3G data rates but also limits the achievable cable lengths at HD and SD data rates).

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6.7 Output Mode (Cable Driver) DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CMOUT}	BNC_IO Output Common Mode Voltage			V_{CC} – V_{OUT}		V
V_{OUT}	BNC_IO Output Voltage Swing	R_{REF} = 715 Ω ±1%	720	800	880	mV_{P-P}
V_{CMIN}	SDI, $\overline{SDI}$ Input Common Mode Voltage		0.9 + V_{ID}/2		V_{CC} – V_{ID}/2	V
V_{ID}	SDI, $\overline{SDI}$ Input Voltage Swing	Differential	100		2200	mV_{P-P}
I_{CC}	Supply Current	SD/$\overline{HD}$ = 0, equalizer in sleep mode		57	71	mA
		SD/$\overline{HD}$ = 1, equalizer in sleep mode		50		mA
		Power save mode (TX_EN = 0, equalizer in sleep mode)		11		mA
		Loopback mode (Tx and Rx both enabled), SD/$\overline{HD}$ = 0		117		mA

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.
(2) Typical values are stated for V_{CC} = +3.3 V and T_A = 25°C.

6.8 Input Mode (Equalizer) AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR_{MIN}	Minimum Input Data Rate			125		Mbps
DR_{MAX}	Maximum Input Data Rate				2970	Mbps
t_{jit}	Equalizer Jitter for Various Cable Lengths (SDO, $\overline{SDO}$)	2.97 Gbps, Belden 1694A, 0-100 meters(2)(3)			0.3	UI
		2.97 Gbps, Belden 1694A, 100-120 meters(3)		0.35		UI
		1.485 Gbps, Belden 1694A, 0-170 meters(2)(3)			0.25	UI
		1.485 Gbps, Belden 1694A, 170-200 meters(3)		0.3		UI
		270 Mbps, Belden 1694A, 0-350 meters(2)(3)			0.2	UI
		270 Mbps, Belden 1694A, 350-400 meters(3)		0.2		UI
t_r, t_f	Output Rise Time, Fall Time	20% – 80%, 100 Ω load, Figure 1(4)		80	130	ps
Δt_r, Δt_f	Mismatch in Rise/Fall Time(4)			2	15	ps
t_{OS}	Output Overshoot(4)			1%	5%	
RL_{IN}	BNC_IO Return Loss	5 MHz - 1.5 GHz(4)(5)	15			dB
		1.5 GHz - 3 GHz(4)(5)	10			dB

(1) Typical values are stated for V_{CC} = +3.3 V and T_A = 25°C.
(2) Based on design and characterization data over the full range of recommended operating conditions of the device. Jitter is measured in accordance with ST RP 184, ST RP 192, and the applicable serial data transmission standard: ST 424, ST 292, or ST 259.
(3) LMH0387 equalizer launch amplitude fine tuning set to nominal through the SPI by writing 30h (“00110000 binary”) to SPI register 02h.
(4) Specification is ensured by characterization.
(5) Return loss is dependent on board design. The LMH0387 exceeds this specification on the SD387EVK evaluation board.

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6.9 Output Mode (Cable Driver) AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR_{MAX}	Maximum Input Data Rate				2970	Mbps
t_{jit}	Additive Jitter	2.97 Gbps(2)		20		ps_{P-P}
		1.485 Gbps(2)		18		ps_{P-P}
		270 Mbps(2)		15		ps_{P-P}
t_r, t_f	Output Rise Time, Fall Time	SD/$\overline{HD}$ = 0, 20% – 80%		65	130	ps
		SD/$\overline{HD}$ = 1, 20% – 80%	400		800	ps
Δt_r, Δt_f	Mismatch in Rise/Fall Time	SD/$\overline{HD}$ = 0			30	ps
		SD/$\overline{HD}$ = 1			50	ps
	Duty Cycle Distortion	SD/$\overline{HD}$ = 0(3)			30	ps
		SD/$\overline{HD}$ = 1(3)			100	ps
t_{OS}	Output Overshoot	SD/$\overline{HD}$ = 0(3)			10%	
		SD/$\overline{HD}$ = 1(3)			8%	
RL_{OUT}	BNC_IO Output Return Loss	5 MHz - 1.5 GHz(3)(4)	15			dB
		1.5 GHz - 3 GHz(3)(4)	10			dB

(1) Typical values are stated for V_{CC} = +3.3 V and T_A = 25°C.
(2) Cable driver additive jitter is measured with the input AC coupled.
(3) Specification is ensured by characterization.
(4) Return loss is dependent on board design. The LMH0387 exceeds this specification on the SD387EVK evaluation board.

6.10 Input Mode (Equalizer) SPI Interface AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCK}	SCK Frequency				20	MHz
t_{PH}	SCK Pulse Width High	Figure 2, Figure 3	40%			SCK period
t_{PL}	SCK Pulse Width Low		40%			SCK period
t_{SU}	MOSI Setup Time	Figure 2, Figure 3	4			ns
t_H	MOSI Hold Time		4			ns
t_{SSSU}	$\overline{SS}$ Setup Time	Figure 2, Figure 3	4			ns
t_{SSH}	$\overline{SS}$ Hold Time		4			ns
t_{SSOF}	$\overline{SS}$ Off Time		10			ns
t_{ODZ}	MISO Driven-to-Tristate Time	Figure 3			15	ns
t_{OZD}	MISO Tristate-to-Driven Time				15	ns
t_{OD}	MISO Output Delay Time				15	ns

(1) Typical values are stated for V_{CC} = +3.3 V and T_A = 25°C.

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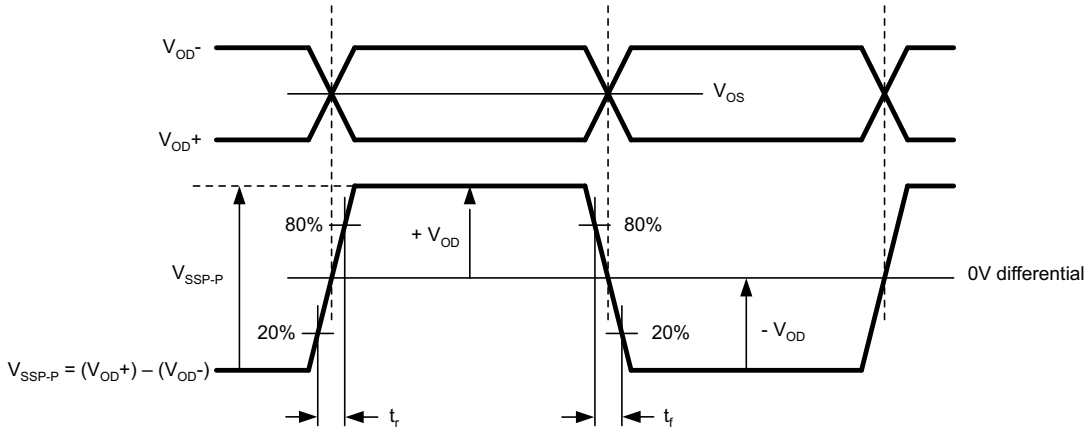


Figure 1. LVDS Output Voltage, Offset, and Timing Parameters

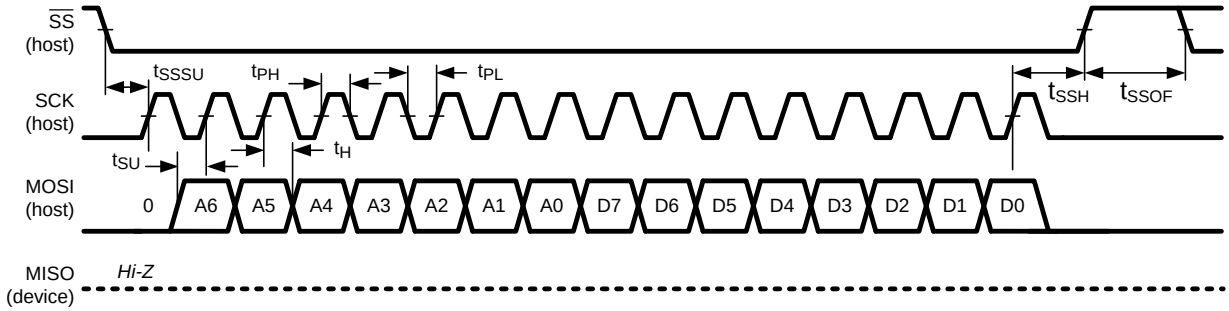


Figure 2. SPI Write Operation

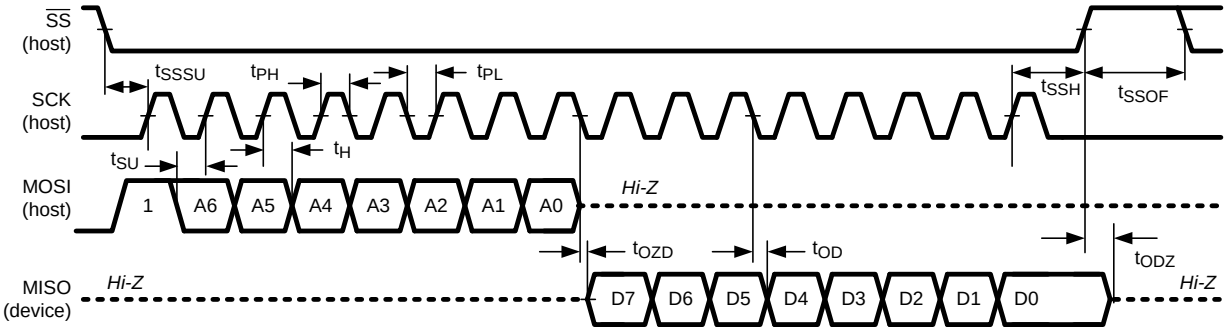
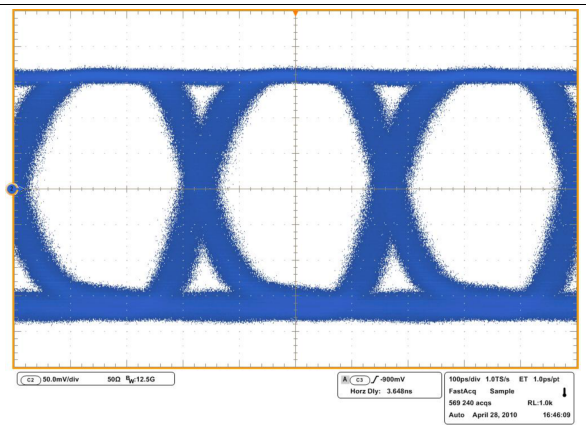


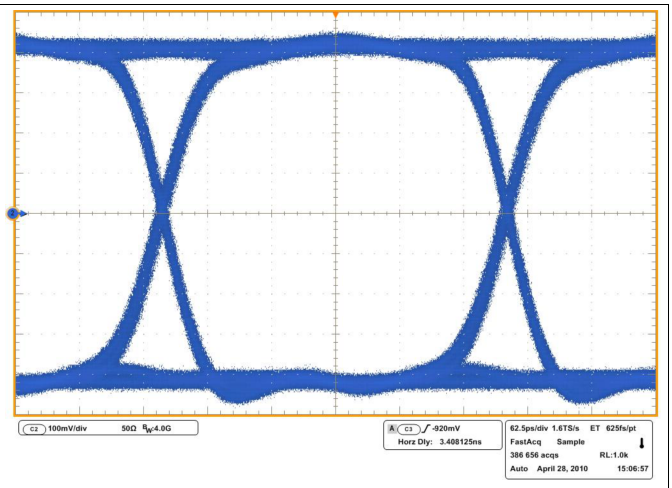
Figure 3. SPI Read Operation

6.11 Typical Characteristics



120m 0f B1694A at 2.97 Gbps, PRBS10 H: 100 ps / div, V: 50 mV / div (SDO Output Shown)

Figure 4. Differential Serial Data Output After Equalizing



H: 62.5 ps / div, V: 100 mV / div (BNC_IO Output Shown)

Figure 5. Cable Driver Output at 2.97 Gbps, PRBS10

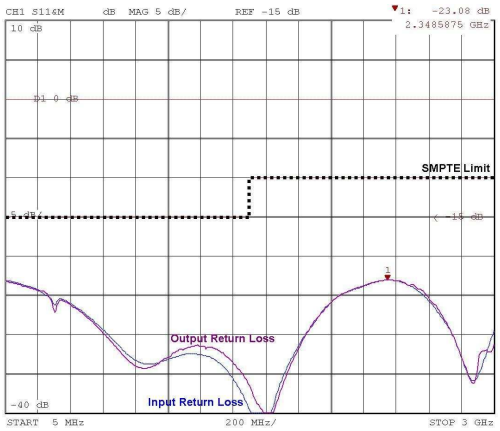


Figure 6. BNC_IO Return Loss

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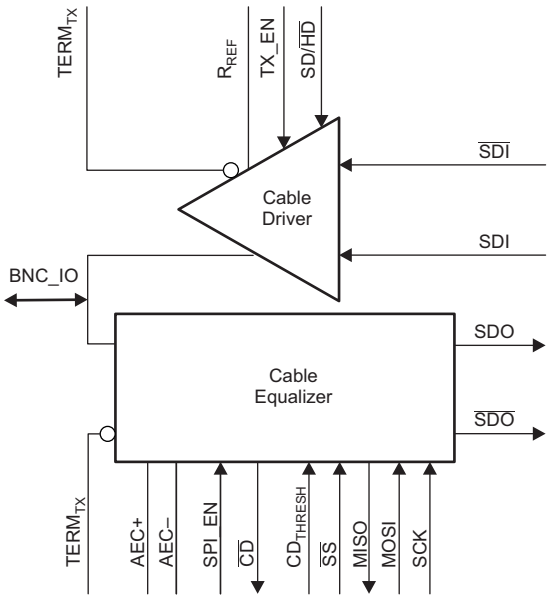
7 Detailed Description

7.1 Overview

The LMH0387 3 Gbps HD/SD SDI Configurable I/O Adaptive Cable Equalizer / Cable Driver provides a single chip interface to a BNC. The same I/O pin is used both for the input and the output functions of the device, allowing the system designer to use a BNC attached to the device as either an input or an output. The LMH0387 operates over a wide range of data rates from 125 Mbps to 2.97 Gbps and supports ST 424, ST 292, ST 344, ST 259, and DVB/ASI standards. The LMH0387 includes passive components for the return loss network – simplifying board design and development time.

7.2 Functional Block Diagram



7.3 Feature Description

The LMH0387 can be configured either in the input mode as an equalizer to receive data over coaxial cable or in the output mode as a cable driver to transmit data over coaxial cable. The LMH0387 requires register programming to operate either in Input Mode (Equalizer) or Output Mode (Cable Driver).

7.3.1 Input Mode (Equalizer) Description

SPI register access is required while operating the LMH0387 in the input mode. The equalizer launch amplitude fine tuning must be set to nominal through the SPI for correct equalizer operation. To do this, write 30h (“00110000 binary”) to SPI register 02h. The SPI registers provide access to many other useful LMH0387 features while in the input mode. Refer to the *Input Mode (Equalizer) SPI Register Access* section for details.

7.3.1.1 Input Interfacing

The LMH0387 accepts a single-ended input at the BNC_IO pin. The input must be AC coupled as shown in Figure 9 . The TERM$_{RX}$ input must be properly terminated with a 1-µF capacitor followed by a 220-Ω resistor to ground.

The LMH0387 BNC_IO input can be optimized for different launch amplitudes through the SPI (see *Launch Amplitude Optimization (Register 02h)* in the *Input Mode (Equalizer) SPI Register Access* section).

The LMH0387 correctly handles equalizer pathological signals for standard and high definition serial digital video, as described in ST RP 178 and RP 198, respectively.

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Feature Description (continued)

7.3.1.2 Output Interfacing

The LMH0387 equalizer outputs, SDO and $\overline{SDO}$, are internally terminated 100-Ω LVDS outputs. These outputs can be DC coupled to most common differential receivers.

The default output common mode voltage (V_{OS}) is 1.25 V. The output common mode voltage may be adjusted through the SPI in 200 mV increments, from 1.05 V to 1.85 V (see *Output Driver Adjustments (Register 01h)* in the *Input Mode (Equalizer) SPI Register Access* section). This adjustable output common mode voltage offers flexibility for interfacing to many types of receivers.

The default differential output swing (V_{SSP-P}) is 700 mV_{P-P}. The differential output swing may be adjusted through the SPI in 100 mV increments from 400 mV_{P-P} to 800 mV_{P-P} (see *Output Driver Adjustments (Register 01h)* in the *Input Mode (Equalizer) SPI Register Access* section).

The LMH0387 equalizer output should be DC coupled to the input of the receiving device as long as the common mode ranges of both devices are compatible. 100-Ω differential transmission lines should be used to connect between the LMH0387 outputs and the input of the receiving device where possible.

The LMH0387 allows flexibility when interfacing to low voltage crosspoint switches (that is, 1.8 V) and other devices with limited input ranges. The LMH0387 equalizer outputs can be DC coupled to these devices in most cases.

The LMH0387 may be AC coupled to the receiving device when necessary. For example, the LMH0387 equalizer outputs are not strictly compatible with 3.3 V CML and thus should not be connected through 50-Ω resistors to 3.3 V. If the input common mode range of the receiving device is not compatible with the output common mode range of the LMH0387, then AC coupling is required. Following the AC coupling capacitors, the signal may have to be biased at the input of the receiving device.

7.3.1.3 Carrier Detect ($\overline{CD}$)

Carrier detect $\overline{CD}$ indicates if a valid signal is present at the LMH0387 BNC_IO pin. If CD_{THRESH} is used, the carrier detect threshold will be altered accordingly. $\overline{CD}$ provides a high voltage when no signal is present at the LMH0387 BNC_IO pin. $\overline{CD}$ is low when a valid input signal is detected.

7.3.1.4 Carrier Detect Threshold (CD_{THRESH})

The CD_{THRESH} pin sets the threshold for the carrier detect. The carrier detect threshold is set by applying a voltage inversely proportional to the length of cable to equalize before loss of carrier is triggered. The applied voltage must be greater than the CD_{THRESH} floating voltage (typically 1.3 V) to change the $\overline{CD}$ threshold. As the applied CD_{THRESH} voltage is increased, the amount of cable that will be equalized before carrier detect is deasserted is decreased. CD_{THRESH} may be left unconnected or connected to ground for normal $\overline{CD}$ operation.

Figure 7 shows the minimum CD_{THRESH} input voltage required to force carrier detect to inactive vs. Belden 1694A cable length. The results shown are valid for Belden 1694A cable lengths of 0 m to 120 m at 2.97 Gbps, 0 m to200 m at 1.485 Gbps, and 0 m to 400 m at 270 Mbps.

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Feature Description (continued)

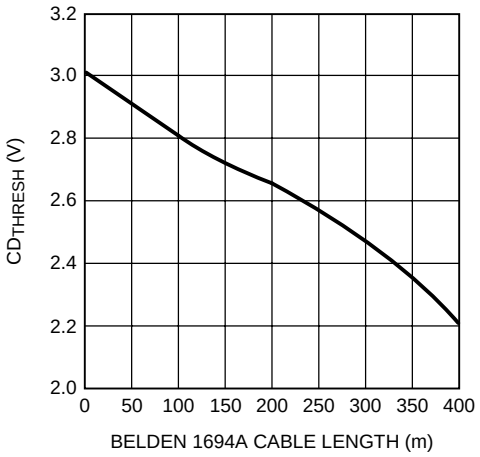

Figure 7. CD_{THRESH} vs Belden 1694A Cable Length

7.3.1.5 Auto Sleep

The LMH0387 equalizer is set for auto sleep operation by default. The equalizer portion of the LMH0387 powers down when no input signal is detected on the BNC_IO pin. The equalizer powers on again once an input signal is detected. The auto sleep functionality can be changed to force sleep or turned off completely through the SPI registers.

In auto sleep mode, the time to power down the equalizer when the input signal is removed is less than 200 µs and should not have any impact on the system timing requirements. The equalizer will wake up automatically once an input signal is detected, and the delay between signal detection and full functionality of the equalizer is negligible. The overall system will be limited only by the settling time constant of the equalizer adaptation loop.

7.3.2 Output Mode (Cable Driver) Description

7.3.2.1 Input Interfacing

The LMH0387 cable driver accepts differential input signals which can be DC or AC coupled.

7.3.2.2 Output Interfacing

The LMH0387 cable driver uses 75-Ω internally terminated current mode outputs. The output level is 800 mV_{P-P} with an R_{REF} resistor of 715 Ω. The R_{REF} resistor is connected between the R_{REF} pin and V_{CC}, and should be placed as close as possible to the R_{REF} pin.

The output should be AC coupled as shown in the Figure 9. The $TERM_{TX}$ output must be properly terminated with a 4.7-µF capacitor followed by a 75-Ω resistor to ground as shown.

7.3.2.3 Output Slew Rate Control

The LMH0387 cable driver output rise and fall times are selectable for either ST 259 or ST 424 / 292 compliance through the SD/$\overline{HD}$ pin. For slower rise and fall times, or ST 259 compliance, SD/$\overline{HD}$ is set high. For faster rise and fall times, or ST 424 and ST 292 compliance, SD/$\overline{HD}$ is set low. SD/$\overline{HD}$ has an internal pulldown.

7.3.2.4 Output Enable

The LMH0387 cable driver can be enabled or disabled with the TX_EN pin. When set low, the cable driver is powered off. TX_EN has an internal pullup to enable the cable driver by default. When using the LMH0387 in the input mode (as an equalizer), the cable driver must be disabled by setting the TX_EN pin low.

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7.4 Device Functional Modes

SPI register access is required while operating the LMH0387 in the input mode. The equalizer launch amplitude fine tuning must be set to nominal through the SPI for correct equalizer operation. To do this, write 30h ("00110000 binary") to SPI register 02h. The SPI registers provide access to many other useful LMH0387 features while in the input mode.

To configure the LMH0387 in the output mode, the cable driver must be enabled. The equalizer may either be disabled for power savings or enabled to provide a loopback path for the data being transmitted. For the normal output mode (equalizer disabled for power savings) follow these steps:

1. Disable the equalizer by forcing it to sleep through the SPI. To do this, write "10" (force sleep) to bits [4:3] of SPI register 00h.
2. Enable the cable driver by pulling the TX_EN pin high.

7.5 Programming

The LMH0387 3 Gbps HD/SD SDI Configurable I/O Adaptive Cable Equalizer / Cable Driver is used at the input or output port of digital video equipment. It is designed to allow the sharing of a single BNC connector for either input or output. The LMH0387 must be configured in either the output mode as a cable driver, or the input mode as an equalizer.

7.5.1 Output Mode (Cable Driver)

To configure the LMH0387 in the output mode, the cable driver must be enabled. The equalizer may either be disabled for power savings or enabled to provide a loopback path for the data being transmitted. For the normal output mode (equalizer disabled for power savings) follow these steps:

1. Disable the equalizer by forcing it to sleep through the SPI. To do this, write "10" (force sleep) to bits [4:3] of SPI register 00h.
2. Enable the cable driver by pulling the TX_EN pin high.

To configure the LMH0387 for the output mode with the loopback path, the equalizer can be enabled in output mode by writing either "01" (auto sleep – default) or "00" (never sleep) to bits [4:3] of SPI register 00h. In this case, the LMH0387 input/output mode may be configured simply by toggling the TX_EN pin because the equalizer remains active in either mode (TX_EN set low for input mode and high for output mode).

7.5.2 Input Mode (Equalizer)

To configure the LMH0387 in the input mode, the equalizer must be enabled and the cable driver must be disabled as described in the following steps:

1. Disable the cable driver by pulling the TX_EN pin low.
2. Enable the equalizer by setting the sleep mode through the SPI to either auto sleep or disabled (never sleep). To do this, write either "01" (auto sleep – default) or "00" (never sleep) to bits [4:3] of SPI register 00h.
3. Set the equalizer launch amplitude fine tuning to the nominal setting through the SPI. To do this, write 30h ("00110000" binary) to SPI register 02h.

7.5.3 Input Mode (Equalizer) SPI Register Access

SPI register access is required for correct input mode (equalizer) operation. The SPI registers provide access to all of the equalizer features along with a cable length indicator, programmable output common mode voltage and swing, and launch amplitude optimization. There are four supported 8-bit registers in the device (see *SPI Registers*).

Note: The SPI_EN pin must always be pulled high while using the LMH0387 in the input mode (equalizer), and may optionally be pulled high while using the LMH0387 in the output mode (cable driver) as well.

7.5.3.1 SPI Write

The SPI write is shown in Figure 2. The MOSI payload consists of a "0" (write command), seven address bits, and eight data bits. The $\overline{SS}$ signal is driven low, and the 16 bits are sent to the LMH0387's MOSI input. Data is latched on the rising edge of SCK. The MISO output is normally tri-stated during this operation. After the SPI write, $\overline{SS}$ must return high.

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Programming (continued)

7.5.3.2 SPI Read

The SPI read is shown in *Figure 3*. The MOSI payload consists of a “1” (read command) and seven address bits. The $\overline{SS}$ signal is driven low, and the eight bits are sent to the LMH0387's MOSI input. The addressed location is accessed immediately after the rising edge of the 8th clock and the eight data bits are shifted out on MISO starting with the falling edge of the 8th clock. MOSI must be tri-stated immediately after the rising edge of the 8th clock. After the SPI read, $\overline{SS}$ must return high.

7.5.3.3 Output Driver Adjustments (Register 01h)

The equalizer output driver swing (amplitude) and offset voltage (common mode voltage) are adjustable through SPI register 01h.

7.5.3.3.1 Output Swing

The output swing is adjustable through bits [7:5] of SPI register 01h. The default value for these register bits is “011” for a peak-to-peak differential output voltage of 700 mV_{P-P}. The output swing can be adjusted in 100 mV increments from 400 mV_{P-P} to 800 mV_{P-P}.

7.5.3.3.2 Offset Voltage

The offset voltage is adjustable through bits [4:2] of SPI register 01h. The default value for these register bits is “001” for an output offset of 1.25 V. The output common mode voltage may be adjusted in 200 mV increments, from 1.05 V to 1.85 V. It can also be set to “101” for the maximum offset voltage. At this maximum offset voltage setting, the outputs are referenced to the positive supply and the offset voltage is around 2.1 V.

7.5.3.4 Launch Amplitude Optimization (Register 02h)

The LMH0387 can compensate for attenuation of the input signal before the equalizer. This compensation is useful for applications with a passive splitter at the equalizer input or a non-ideal input termination network, and is controlled by SPI register 02h.

NOTE

For correct equalizer operation with the default SMPTE 800 mV_{P-P} launch amplitude and no external attenuation, the equalizer launch amplitude fine tuning must be set to the “nominal” setting through the SPI. To do this, write 30h (“00110000” binary) to SPI register 02h.

7.5.3.4.1 Coarse Control

Bit 7 of SPI register 02h is used for coarse control of the launch amplitude setting. At the default setting of “0”, the equalizer operates normally and expects a launch amplitude of 800 mV_{P-P}. Bit 7 may be set to “1” to optimize the equalizer for input signals with 6 dB of attenuation (400 mV_{P-P}).

7.5.3.4.2 Fine Control

Once the coarse control is set, the equalizer input compensation may be further fine tuned by bits [6:3] of SPI register 02h. These bits may be used to tweak the input gain stage -2% to 60% around the coarse control setting. For typical equalizer operation, bits [6:3] of SPI register 02h should be changed from the default setting of “0000” to the nominal setting of “0110”.

7.5.3.5 Cable Length Indicator (CLI (Register 03h)

The Cable Length Indicator (CLI) provides an indication of the length of cable attached to the equalizer input. CLI is accessible through bits [7:3] of SPI register 03h. The 5-bit CLI ranges in decimal value from 0 to 25 (“00000” to “11001” binary) and increases as the cable length is increased. Figure 8 shows typical CLI values vs. Belden 1694A cable length. CLI is valid for Belden 1694A cable lengths of 0 m to 120 m at 2.97 Gbps, 0 m to 200 m at 1.485 Gbps, and 0 m to 400 m at 270 Mbps.

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Programming (continued)

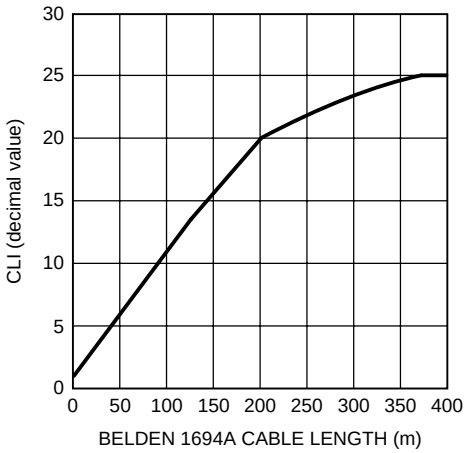

Figure 8. CLI vs. Belden 1694A Cable Length

7.5.4 Input Mode (Equalizer) SPI Register Access

7.5.4.1 General Control (Register 00h)

SPI Register 00h, General Control, provides access to many basic features of the equalizer, including the carrier detect status and the mute, sleep mode, and extended 3G reach mode controls.

7.5.4.1.1 Carrier Detect

This bit shows the status of the carrier detect for the BNC_IO pin.

7.5.4.1.2 Mute

The mute control can be used to manually mute or enable SDO and $\overline{\text{SDO}}$. Setting this bit to “1” will mute the equalizer outputs by forcing them to logic zero. Setting the mute bit to “0” will force the equalizer outputs to be active.

7.5.4.1.3 Sleep Mode

The sleep mode is used to automatically or selectively power down the equalizer for power savings when it is not needed. The auto sleep mode allows the equalizer to power down when no input signal is detected, and is activated by default or by writing “01” to bits [4:3] of SPI register 00h. If the auto sleep mode is active, the equalizer goes into a deep power save mode when no input signal is detected on the BNC_IO pin. The device powers on again once an input signal is detected. The sleep functionality can be turned off completely (equalizer will never sleep) by writing “00” to bits [4:3] of SPI register 00h. Additionally, the equalizer can be forced to power down regardless of whether there is an input signal or not by writing “10” to bits [4:3] of SPI register 00h. The sleep mode has precedence over the mute mode.

7.5.4.1.4 Extended 3G Reach Mode

The LMH0387 equalizer provides a mode to extend the 3G cable reach in systems that have margin in the jitter budget. This allows for additional cable reach at 2.97 Gbps at the expense of slightly higher output jitter. The extended 3G reach mode provides 10m of additional Belden 1694A cable reach, with an increase of output jitter at this longer cable length of 0.05 to 0.1 UI. (Note: In Extended 3G Reach Mode, the maximum equalizable cable lengths for HD and SD data rates will be limited to less than what can be achieved in normal mode).

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7.6 Register Maps

7.6.1 SPI Registers

Table 1. SPI Register Descriptions

ADDRESS	R/W	NAME	BITS	FIELD	DEFAULT	DESCRIPTION
00h	R/W	General Control	7	Carrier Detect		Read only. 0: No carrier detected on BNC_IO pin. 1: Carrier detected on BNC_IO pin.
			6	Mute	0	0: Normal operation. 1: Equalizer outputs muted.
			5	Reserved	0	Reserved as 0. Always write 0 to this bit.
			4:3	Sleep Mode	01	Equalizer sleep mode control. Sleep has precedence over Mute. 00: Never sleep. Disable sleep mode (force equalizer to stay enabled). 01: Auto sleep. Sleep mode active when no input signal detected. 10: Force sleep. Force equalizer into sleep mode (powered down) regardless of whether there is an input signal or not. 11: Reserved.
			2	Extended 3G Reach Mode	0	Extended 3G reach mode to extend the equalizable cable length for 2.97 Gbps applications. 0: Normal operation. 1: Extended 3G reach mode.
			1:0	Reserved	00	Reserved as 00. Always write 00 to these bits.
01h	R/W	Output Driver	7:5	Output Swing	011	Equalizer output driver swing (V_{SSP-P}). 000: V_{SSP-P} = 400 mV_{P-P}. 001: V_{SSP-P} = 500 mV_{P-P}. 010: V_{SSP-P} = 600 mV_{P-P}. 011: V_{SSP-P} = 700 mV_{P-P}. 100: V_{SSP-P} = 800 mV_{P-P}. 101, 110, 111: Reserved.
			4:2	Offset Voltage	001	Equalizer output driver offset voltage (common mode voltage). 000: V_{OS} = 1.05V. 001: V_{OS} = 1.25V. 010: V_{OS} = 1.45V. 011: V_{OS} = 1.65V. 100: V_{OS} = 1.85V. 101: V_{OS} referenced to positive supply. 110, 111: Reserved.
			1:0	Reserved	00	Reserved as 00. Always write 00 to these bits.

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Register Maps (continued)

Table 1. SPI Register Descriptions (continued)

ADDRESS	R/W	NAME	BITS	FIELD	DEFAULT	DESCRIPTION
02h	R/W	Launch Amplitude	7	Coarse Control	0	Coarse launch amplitude optimization for equalizer input. 0: Normal optimization with no external attenuation (800 mV_{P-P} launch amplitude). 1: Optimized for -6 dB external attenuation (400 mV_{P-P} launch amplitude).
			6:3	Fine Control	0000	Launch amplitude optimization fine tuning for equalizer input. 0000: +20% from nominal. 0001: +16% from nominal. 0010: +12% from nominal. 0011: +9% from nominal. 0100: +6% from nominal. 0101: +3% from nominal. **0110: Nominal.** (The default setting must be changed to this nominal setting for most applications). 0111: -2% from nominal. 1001: +24% from nominal. 1010: +29% from nominal. 1011: +34% from nominal. 1100: +40% from nominal. 1101: +46% from nominal. 1110: +53% from nominal. 1111: +60% from nominal. 1000: Reserved.
			2:0	Reserved	000	Reserved as 000. Always write 000 to these bits.
03h	R	CLI	7:3	CLI		Cable Length Indicator. Provides an indication of the length of cable attached to the equalizer input. CLI increases as the cable length increases.
			2:0	Reserved	000	Reserved.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMH0387 is a single channel SDI cable driver and equalizer that supports different application spaces. The following sections describe the typical use cases and common implementation practices.

8.1.1 General Guidance for Applications

The LMH0387 supports SPI interface for configuring the device. Registers must be programmed (see *Programming*) for proper operation of the device. Attention must be paid to the PCB layout for the high speed signals to facilitate the SMPTE specification compliance. SMPTE specifies requirements for the Serial Digital Interface to transport digital video over coaxial cable. SMPTE specifies the use of AC coupling capacitors for transporting uncompressed serial data with heavy low-frequency content. This specification requires the use of a 4.7-µF AC coupling capacitor to avoid low-frequency DC wander. The 75-Ω trace impedance is required to meet SMPTE specified rise/fall requirements to facilitate highest eye opening for the receiving device.

8.2 Typical Application

To meet SMPTE requirements, the optimal placement of the LMH0387 is to be as close to the BNC as possible. Figure 9 shows the application circuit for the LMH0387.

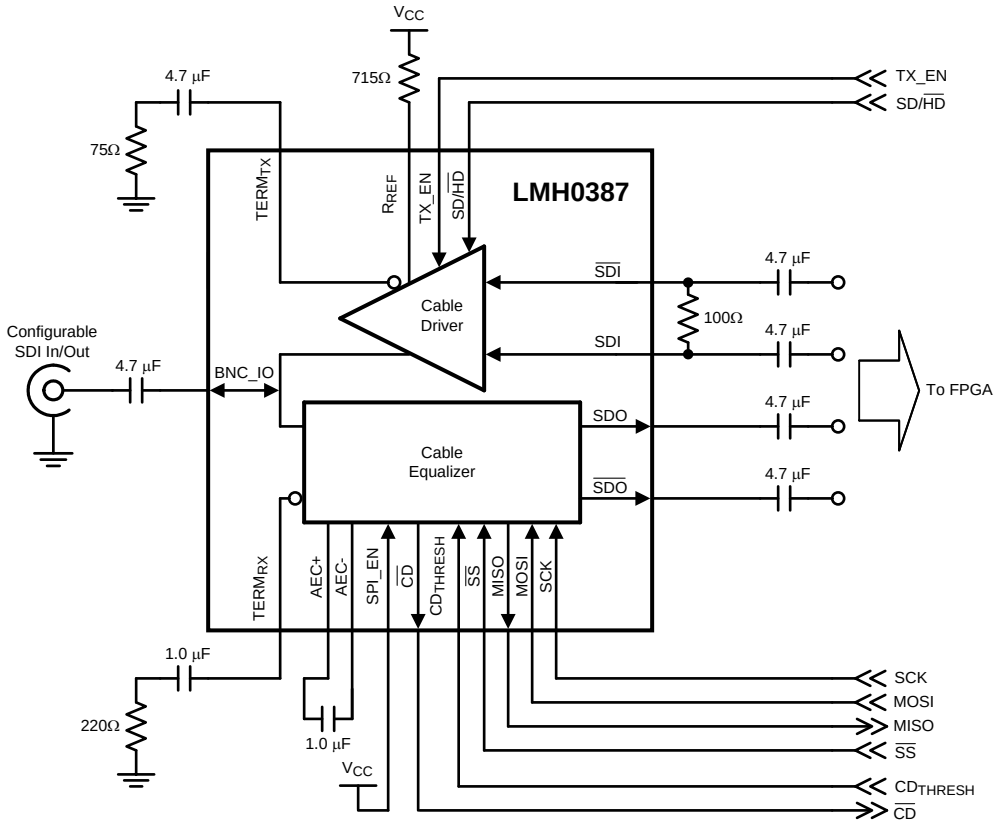

Figure 9. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 2 lists the key design parameters of the LMH0387.

Table 2. Design Parameters

DESIGN PARAMETER	REQUIREMENTS
Input AC coupling capacitor	Required. A common type of AC coupling capacitor is 4.7-µF ±10% X7R ceramic capacitor (0402 or 0201 size).
Trace or via under the device	No trace or via under the device.
Distance from device to BNC	Keep this distance as short as possible to minimize the parasitic.
BNC_IO, $TERM_{TX}$, $TERM_{RX}$ trace impedance	Design single-ended trace impedance with 75 Ω ± 5%.
$\overline{SDI}$, SDI and $\overline{SDO}$, SDO differential trace impedance	Design differential trace impedance with 100 Ω ± 5%.
DC power supply coupling capacitors	To minimize power supply noise, use 0.1-µF shunt across 10-µF capacitors as close to the device as possible.

8.2.2 Detailed Design Procedure

To begin the design process, determine the followings:

- Maximum power consumption for PCB regulator selection: Use maximum current consumption in the data sheet to compute the maximum power consumption.
- Closely compare schematic against typical connection diagram in the data sheet.
- With layout guideline in mind (see *Layout Guidelines*) plan out the PCB layout and component placement to minimize parasitic.
- Consult the BNC vendor for optimum BNC landing pattern.

8.2.3 Application Curve

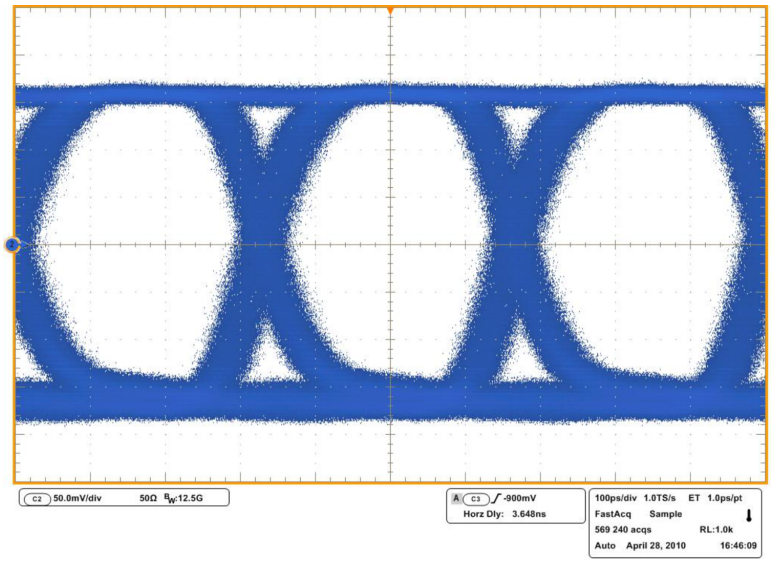

Figure 10. Differential Serial Data Output After Equalizing 200m of B1694A at 1.485 Gbps, PRBS10

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9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

- The power supply should be designed to provide the recommended operating conditions in terms of DC voltage and maximum current consumption.
- The maximum current draw for the LMH0387 is provided in the data sheet. This number can be used to calculate the maximum current the supply must provide.
- The LMH0387 does not require any special power supply filtering, provided the recommended operating conditions are met. Use 0.1-µF capacitors as close to the device V_{CCRX} and V_{CCTX} pins as possible.

10 Layout

10.1 Layout Guidelines

For information on layout and soldering of the laminate TLGA package, refer to the following application note: AN-1125 (SNAA002), *Laminate CSP/FBGA*.

NOTE

For a CSP package, it is a general requirement not to have any metal (traces or vias) on the top layer in the area directly underneath the device, other than the footprint. This is intended to provide a flat planar surface for the package.

The ST 424, 292, and 259 standards have stringent requirements for the input and output return loss of receivers and transmitters, which essentially specify how closely they must resemble a 75-Ω network. Any non-idealities in the network between the BNC and the LMH0387 will degrade the return loss. Take care to minimize impedance discontinuities both for the BNC footprint and for the trace between the BNC and the LMH0387 to ensure that the characteristic impedance is 75 Ω. Best return loss performance is achieved with the LMH0387 placed closely to the BNC to minimize the trace length between the BNC and the LMH0387's BNC_IO pin. Consider the following PCB recommendations:

- Place the LMH0387 in close proximity to the BNC.
- Use surface mount components, and use the smallest components available. In addition, use the smallest size component pads.
- Select trace widths that minimize the impedance mismatch between the BNC and the LMH0387.
- Select a board stack up that supports both 75-Ω single-ended traces and 100-Ω loosely-coupled differential traces.
- Maintain symmetry on the complementary signals.
- Route 100-Ω traces uniformly (keep trace widths and trace spacing uniform along the trace).
- Avoid sharp bends in the signal path; use 45° or radial bends.
- Place bypass capacitors close to each power pin, and use the shortest path to connect device power and ground pins to the respective power or ground planes.
- Remove ground plane under input/output components to minimize parasitic capacitance.

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10.2 Layout Example

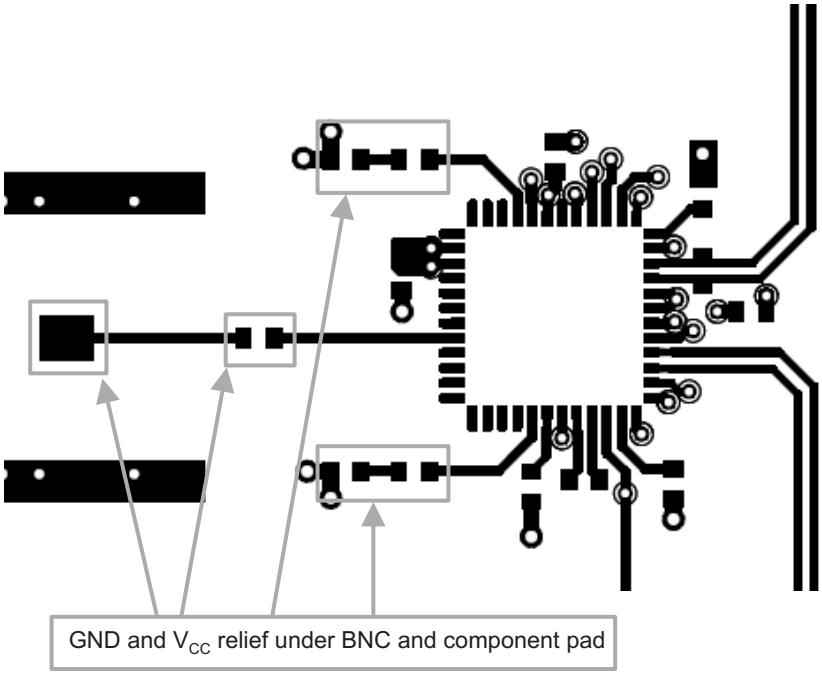

Figure 11. Ground and VCC Relief Under Controlled Impedance Component Pads

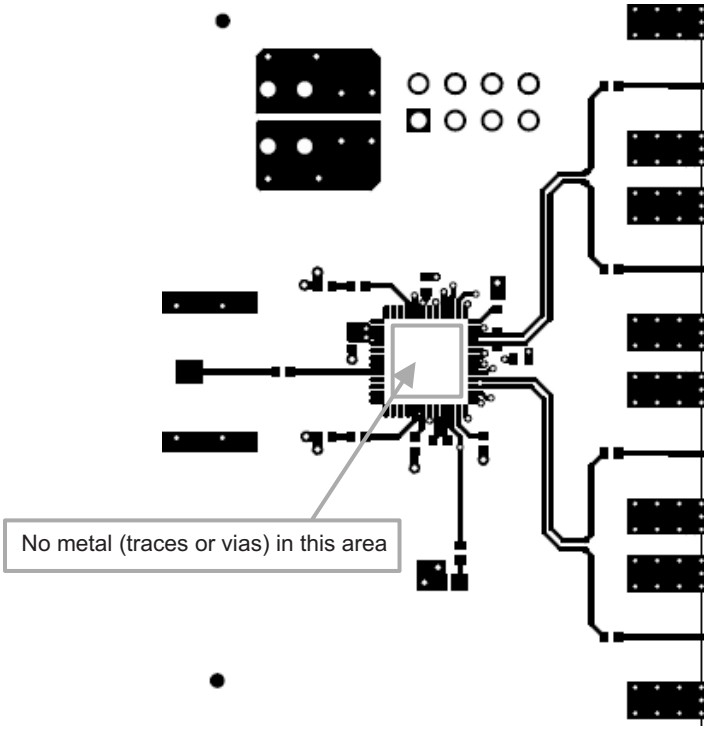

Figure 12. Top Etch Routing Restriction

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *AN-1125 Laminate CSP/FBGA*, SNAA002

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH0387SL/NOPB	Active	Production	TLGA (NPD) | 48	1000 | LARGE T&R	Exempt	NIAU	Level-3-260C-168 HR	-40 to 85	LMH0387SL
LMH0387SL/NOPB.A	Active	Production	TLGA (NPD) | 48	1000 | LARGE T&R	Exempt	NIAU	Level-3-260C-168 HR	-40 to 85	LMH0387SL
LMH0387SL/NOPB.B	Active	Production	TLGA (NPD) | 48	1000 | LARGE T&R	Exempt	NIAU	Level-3-260C-168 HR	-40 to 85	LMH0387SL
LMH0387SLE/NOPB	Active	Production	TLGA (NPD) | 48	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMH0387SL
LMH0387SLE/NOPB.A	Active	Production	TLGA (NPD) | 48	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMH0387SL
LMH0387SLE/NOPB.B	Active	Production	TLGA (NPD) | 48	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMH0387SL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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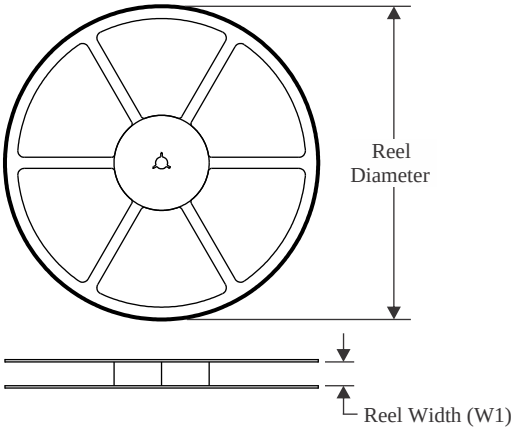
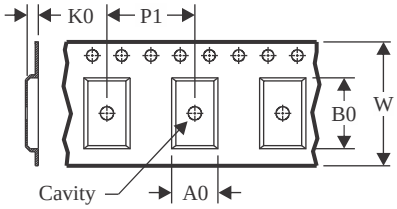
TAPE AND REEL INFORMATION

REEL DIMENSIONS

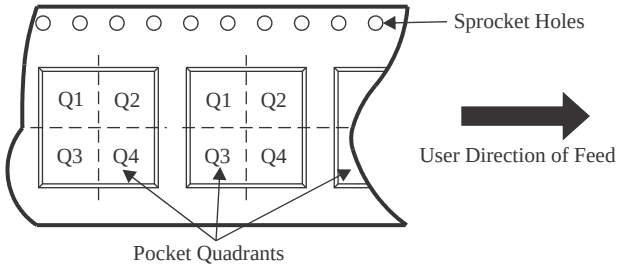


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

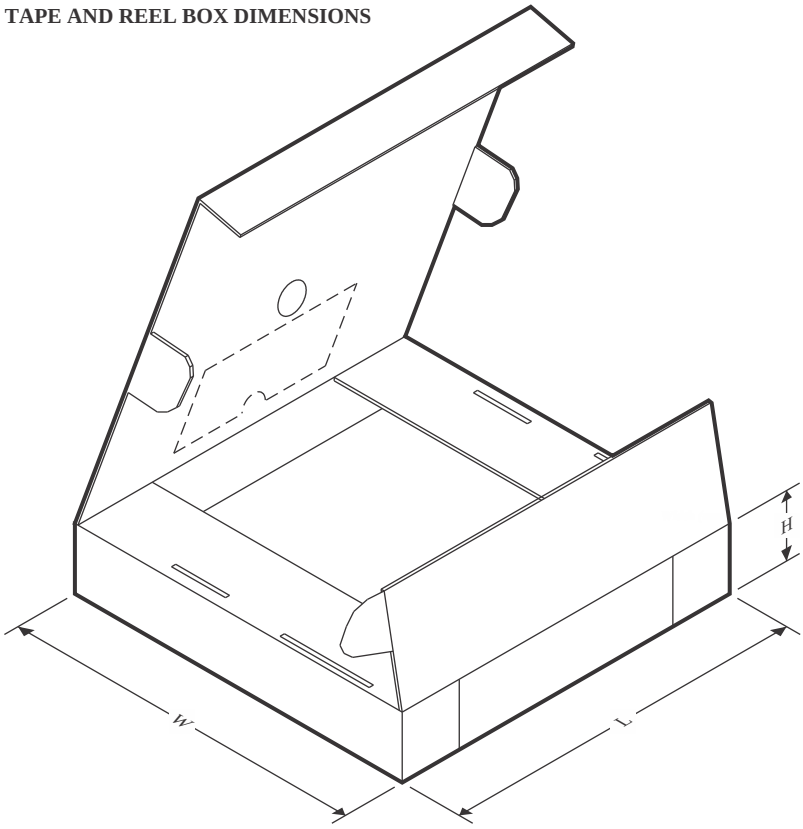
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0387SL/NOPB	TLGA	NPD	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
LMH0387SLE/NOPB	TLGA	NPD	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

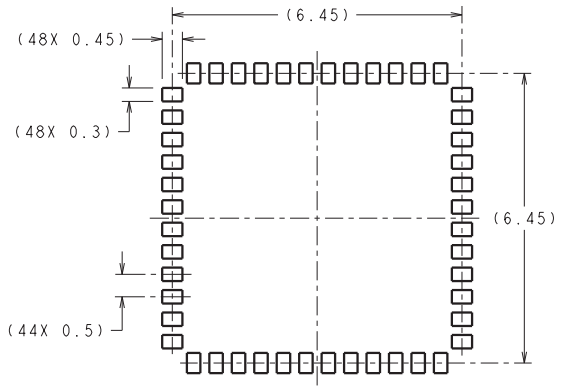
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

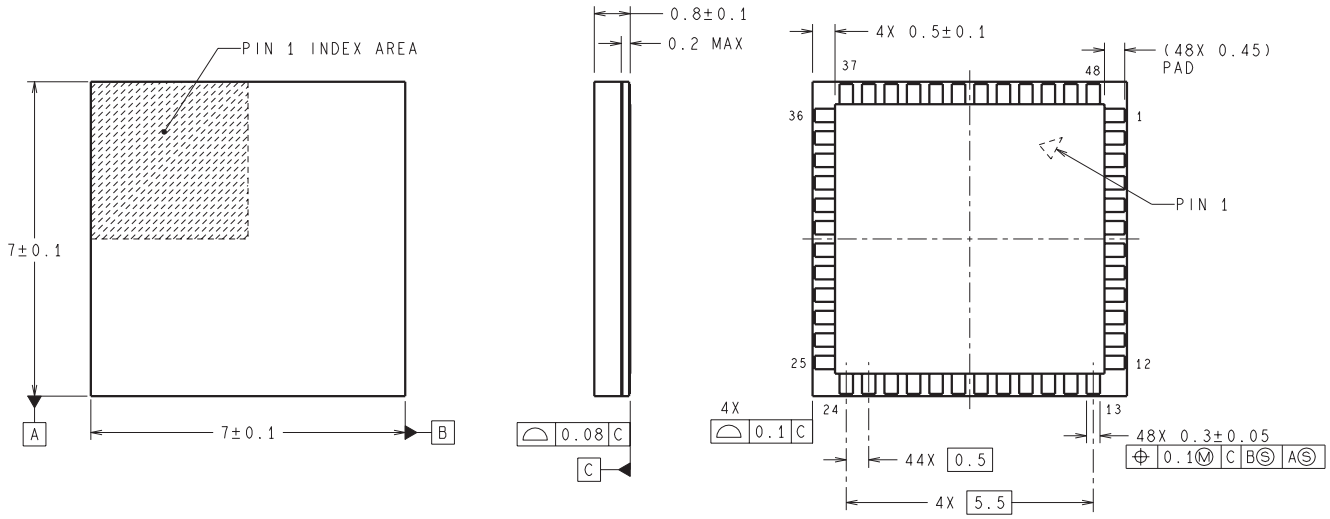
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0387SL/NOPB	TLGA	NPD	48	1000	356.0	356.0	36.0
LMH0387SLE/NOPB	TLGA	NPD	48	250	208.0	191.0	35.0

NPD0048A



RECOMMENDED LAND PATTERN
1:1 RATIO WITH PACKAGE SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



SLD48A (Rev B)

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