16-Bit, 4-Channel, CCD/CMOS Sensor Analog Front-End with LED Driver

Check for Samples: VSP5620, VSP5621, VSP5622

FEATURES

- **Four-Channel CCD/CMOS Signal: 2-Channel, 3-Channel, and 4-Channel Selectable**
- **Power Supply: 3.3 V Only, Typ (Built-in LDO, 3.3 V to 1.8 V)**
- **Maximum Conversion Rate:**
  - **VSP5620: 35 MSPS**
  - **VSP5621: 50 MSPS**
  - **VSP5622: 70 MSPS**
- **16-Bit Resolution**
- **CDS/SH Selectable**
- **Maximum Input Signal Range: 2.0 V**
- **Analog and Digital Hybrid Gain:**
  - **Analog Gain: 0.5 V/V to 3.5 V/V in 3/64-V/V Steps**
  - **Digital Gain: 1 V/V to 2 V/V in 1/256-V/V Steps**
- **Offset Correction DAC: ±250 mV, 8-Bit**
- **Standard LVDS/CMOS Selectable Output:**
  - **LVDS:**
    - **Data Channel: 2-Channel**
    - **Clock Channel: 1-Channel**
    - **8-Bit/7-Bit Serializer Selectable**
  - **CMOS: 4 Bits × 4**
- **Timing Generator**
  - **Fast Transfer Clock: One Signal**
  - **Slow Transfer Clock: One Signal**
- **LED Driver: Three Channels**
  - **Current: 60-mA/Channel Max, 16-Steps/Channel**
- **Timing Adjustment Resolution: $t_{MCLK}/48$**
- **Input Clamp/Input Reference Level Internal/External Selectable**
- **Reference DAC: 0.5 V, 1.1 V, 1.5 V, 2 V**
- **SPI™: Three-Wire Serial**
- **GPIO: Four-Port**
- **Power (at 4-channel, LVDS, 3.3 V, without LED Driver):**
  - **VSP5620: 320 mW at 35 MSPS**
  - **VSP5621: 406 mW at 50 MSPS**
  - **VSP5622: 523 mW at 70 MSPS**

APPLICATIONS

- **Copiers**
- **Facsimile Machines**
- **Scanners**

DESCRIPTION

The VSP5620/21/22 are high-speed, high-performance, 16-bit analog-to-digital-converters (ADCs) that have four independent sampling circuit channels for multi-output charge-coupled device (CCD) and complementary metal oxide semiconductor (CMOS) line sensors. Pixel data from the sensor are sampled by the sample/hold (SH) or correlated double sampler (CDS) circuit, and are then converted to digital data by an ADC. Data output is selectable in low-voltage differential signaling (LVDS) or CMOS modes.

The VSP5620/21/22 include a programmable gain to support the pixel level inflection caused by luminance and a built-in light-emitting diode (LED) driver to adjust the brightness. The integrated digital-to-analog-converter (DAC) can be used to adjust the offset level for the analog input signal. Furthermore, the timing generator (TG) is integrated in these devices for the control of sensor operation.

The VSP5620/21/22 use 1.65 V to 1.95 V for the core voltage and 3.0 V to 3.6 V for I/Os. The core voltage is supplied by a built-in low-dropout regulator (LDO).

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
VSP5621RSLR	Active	Production	VQFN (RSL) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	VSP 5621
VSP5621RSLR.A	Active	Production	VQFN (RSL) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	VSP 5621

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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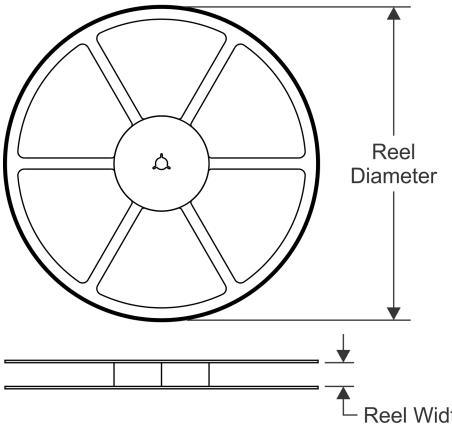
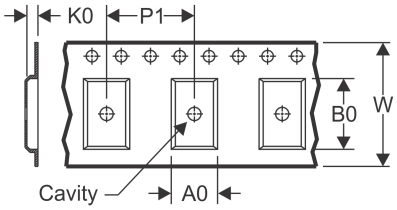
TAPE AND REEL INFORMATION

REEL DIMENSIONS

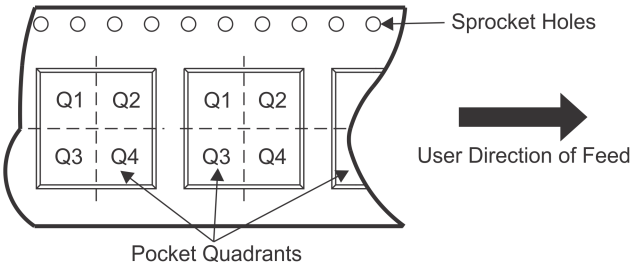


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

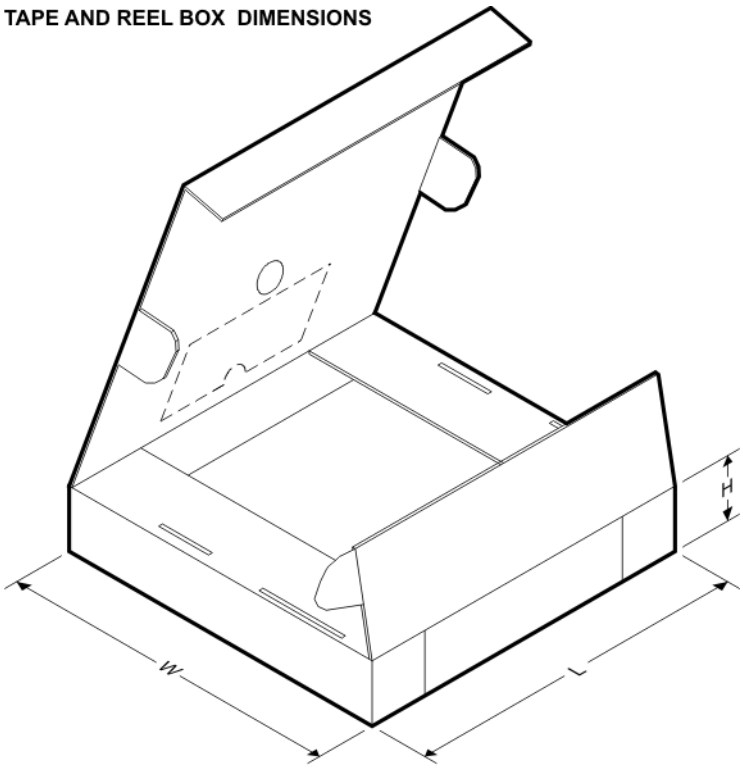
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP5621RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP5621RSLR	VQFN	RSL	48	2500	367.0	367.0	38.0

GENERIC PACKAGE VIEW

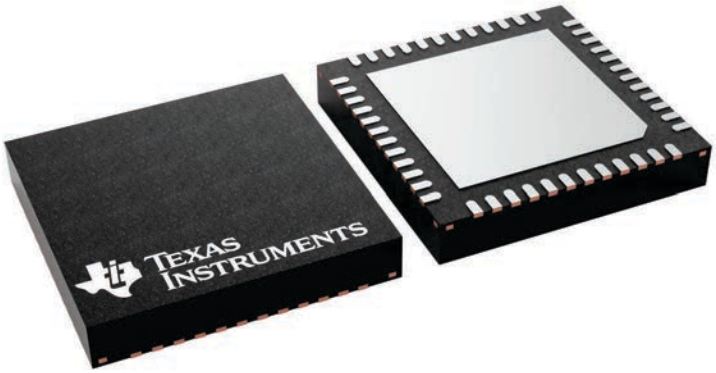
RSL 48

VQFN - 1 mm max height

6 x 6, 0.4 mm pitch

QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



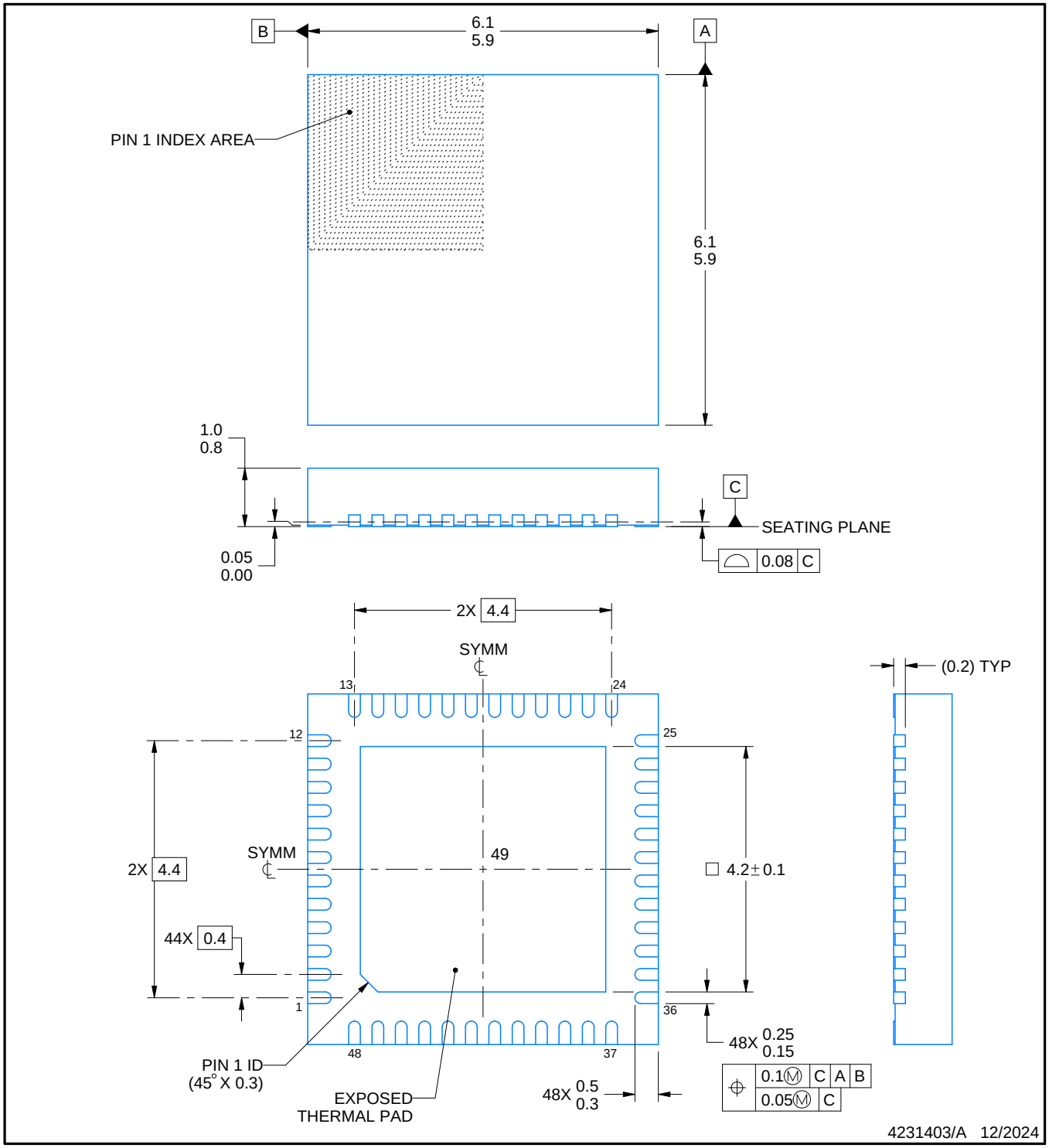
4225749/A

RSL0048G

PACKAGE OUTLINE

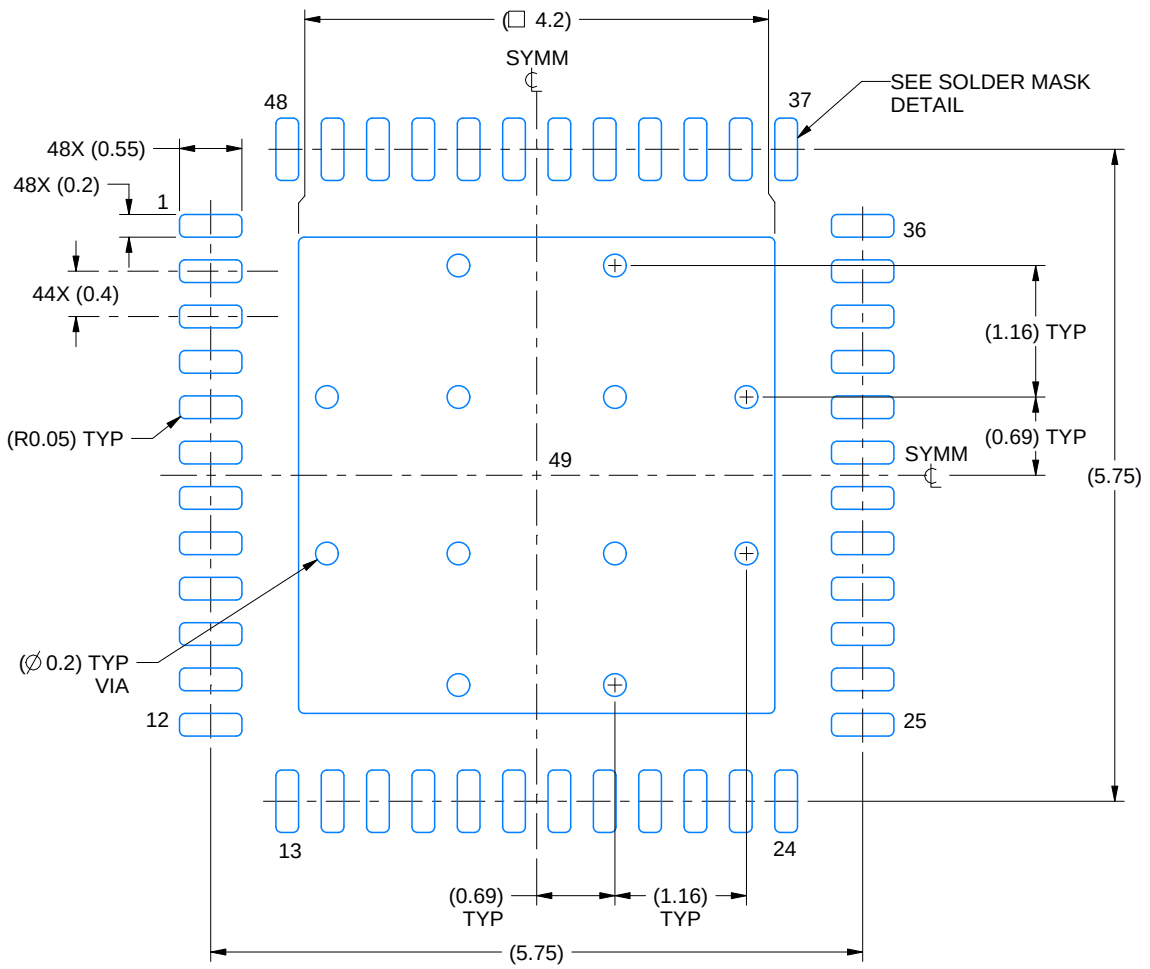
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

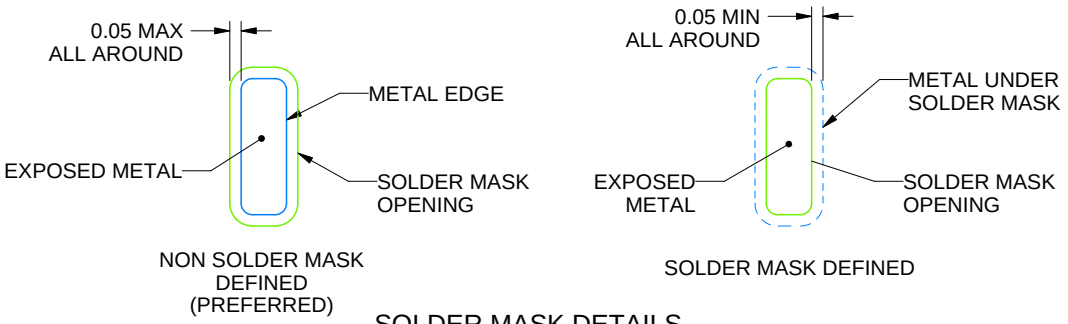


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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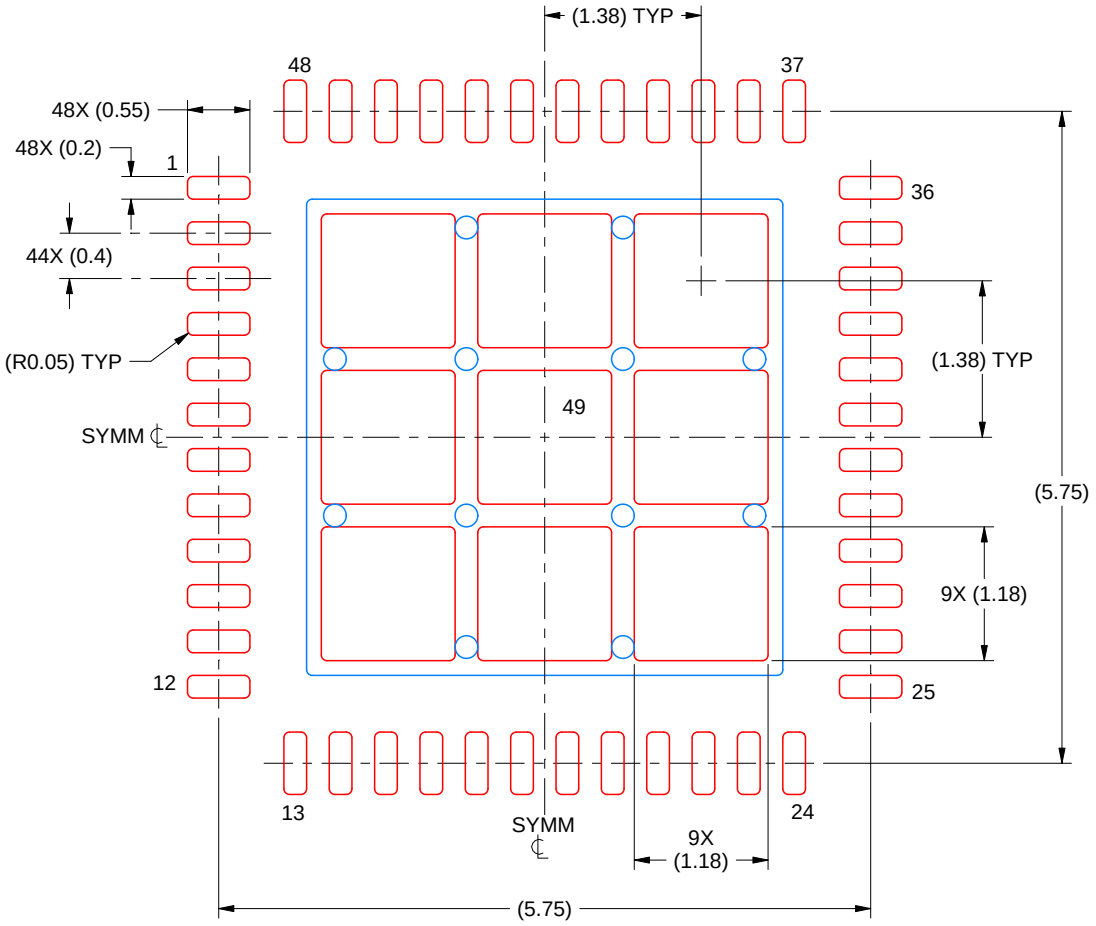
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 49
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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