TPS7H502x-SP and TPS7H502x-SEP Radiation-Hardened 1MHz Current Mode PWM Controller With Integrated Gate Driver

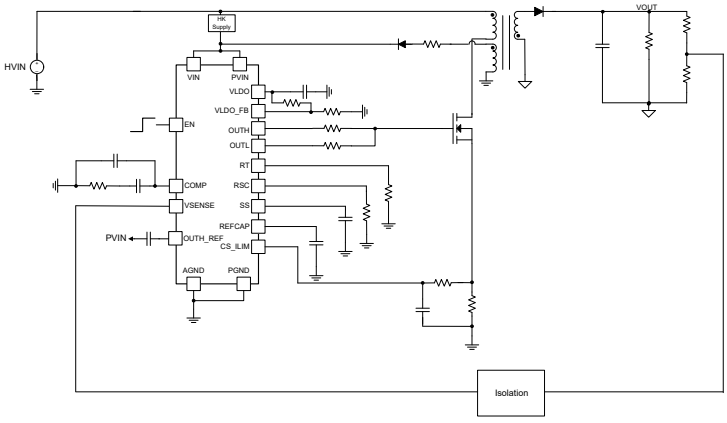
ADVANCE INFORMATION

1 Features

- Radiation performance:
  - Radiation hardness assurance (RHA) up to total ionizing dose (TID) of 100krad(Si)
  - Single-event latchup (SEL), single-event burnout (SEB) and single-event gate rupture (SEGR) immune to LET = 75MeV-cm^2/mg
  - Single-event transient (SET) and single-event functional interrupt (SEFI) characterized up to LET = 75MeV-cm^2/mg
- 4.5V to 14V input voltage range for both controller and driver stages
- Dedicated gate driver voltage input pin (PVIN) allows for driving both silicon and GaN devices
  - 1.2A peak source and sink capability at 12V
  - Optional connection of VLDO linear regulator output to PVIN for driving GaN
  - Programmable linear regulator (VLDO) from 4.5V to 5.5V
- 0.6V ±1% voltage reference over temperature, radiation, and line and load regulation
- Switching frequency from 100kHz to 1MHz
- External clock synchronization capability
- Adjustable slope compensation and soft start
- Plastic packages outgas tested per ASTM E595

2 Applications

- Space satellite power supplies
- Communications payload
- Radar imaging payload
- Satellite electrical power system



Typical Application Circuit

3 Description

The TPS7H502x is a radiation-hardness-assured, current mode, single-ended PWM controller with an integrated gate driver that can be utilized in both silicon and gallium nitride (GaN) power semiconductor based converter designs. The TPS7H502x integrates several key functions, such as soft-start, enable, and adjustable slope compensation while maintaining a small package size. The controller also features a 0.6V ±1% voltage reference tolerance to support highly accurate power converter designs.

The TPS7H502x can be operated using an external clock through the SYNC pin or by programming the internal oscillator using the RT pin at a frequency determined by the user. The device is capable of switching at frequencies up to 1MHz. The driver stage for the controller has a wide input voltage range from 4.5V to 14V and supports peak source and sink currents up to 1.2A. The programmable regulator, VLDO, can also be connected directly to the input of the driver stage (PVIN) in order to supply well-controlled gate voltage for operation with GaN FETs. The programmable regulator has a voltage range from 4.5V to 5.5V. The TPS7H5020 device has a maximum duty cycle of 100% while the TPS7H5021 has a 50% maximum duty cycle. The controller supports numerous power converter topologies, including flyback, forward, and boost.

Device Information

PART NUMBER(1)	GRADE	PACKAGE(2) (3)
5962R2420101PYE(4)	QMLP-RHA	24-pin plastic 4.40mm × 7.80mm Mass = 100.6mg
5962R2420102PYE(4)		
TPS7H5020MPWPTSEP(5)	SEP	
TPS7H5021MPWPTSEP(4)		

(1) For additional information, view the *Device Options* table.
(2) The package size (length × width) is a nominal value and does not include pins.
(3) Mass is a nominal value.
(4) Product preview.
(5) Advance information.

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4 Device Comparison Table

DEVICE	DUTY CYCLE LIMIT (NOMINAL)
TPS7H5020[1] [2]	100%
TPS7H5021[3] [2]	50%

(1) Advance information (SEP).
(2) Product preview (QMLP).
(3) Product preview (SEP).

5 Device Options Table

GENERIC PART NUMBER	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H5020-SP	TID of 100krad(Si) RLAT, DSEE free up to LET = 75MeV-cm^2/mg	QMLP-RHA	24-pin HTSSOP PWP	5962R2420101PYE(3)
TPS7H5020-SEP	TID of 50krad(Si) RLAT, DSEE free up to LET = 43MeV-cm^2/mg	Space Enhanced Plastic	24-pin HTSSOP PWP	TPS7H5020MPWPTSEP (4)
TPS7H5021-SP	TID of 100krad(Si) RLAT, DSEE free up to LET = 75MeV-cm^2/mg	QMLP-RHA	24-pin HTSSOP PWP	5962R2420102PYE(3)
TPS7H5021-SEP	TID of 50krad (Si) RLAT, DSEE free up to LET = 43MeV-cm^2/mg	Space Enhanced Plastic	24-pin HTSSOP PWP	TPS7H5021MPWPTSEP (3)

(1) Refer to the device product folder for full radiation testing results in the associated TID and SEE reports.
(2) For additional information about part grade, view SLYB235.
(3) Product preview.
(4) Advance information.

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6 Pin Configuration and Functions

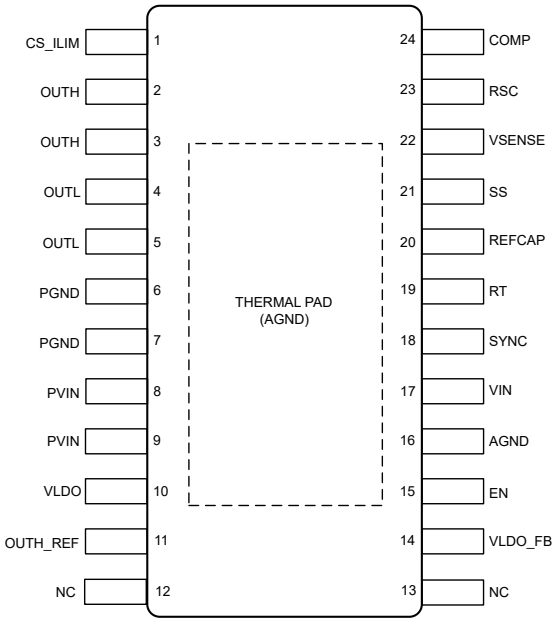

Figure 6-1. PWP Package
24-Pin HTSSOP With Thermal Pad
(Top View)

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	HTSSOP		
CS_ILIM	1	I	Current sense for PWM control and cycle-by-cycle overcurrent protection. An input voltage over 1V on CS_ILIM triggers an overcurrent in the PWM controller. The sensed waveform on CS_ILIM contains a 150mV offset when compared to the COMP/CCSR voltage at the input of the PWM comparator.
OUTH	2, 3	O	Driver stage source current output. Connect to the gate of the power transistor using a short, low-inductance path. A resistor between OUTH and the gate of the transistor can be used to adjust the turn-on speed.
OUTL	4, 5	O	Driver stage sink current output. Connect to the gate of the power transistor using a short, low-inductance path. A resistor between OUTL and the gate of the transistor can be used to adjust the turn-off speed.
PGND	6, 7	—	Driver stage power ground. Connect to the source of the power transistor. Connect to AGND at the printed circuit board level.
PVIN	8, 9	I	Driver stage voltage input. The voltage range of PVIN is from 4.5V to 14V. The voltage being supplied to the gate of the power transistor is approximately equal to the input voltage at PVIN. This pin can be connected to VIN for single-supply operation. Can also be connected to VLDO to provide a regulated gate drive voltage, between 4.5V and 5.5V, to the power transistor gate.
VLDO	10	O	Programmable output of internal regulator. Can be connected to PVIN for regulated GaN compatible driver voltage. Able to be programmed from 4.5V to 5.5V using a resistor divider than consists of a resistor from VLDO to VLDO_FB and another from VLDO_FB to AGND. These resistors must always be populated for proper operation. Requires at least 1µF external capacitor to AGND.

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Table 6-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	HTSSOP		
OUTH_REF	11	O	OUTH driver stage return. The voltage at OUTH_REF is nominally 6V less than the voltage present at PVIN. When the voltage at PVIN is 6V or greater, connect a 220nF capacitor between OUTH_REF and PVIN. This improves transient performance and minimizes potential radiation-induced single-event transients (SETs). For PVIN voltage less than 6V, connect OUTH_REF to PGND at the printed circuit board level.
VLDO_FB	14	I	VLDO feedback pin. Used to program the VLDO output voltage. Nominally set to 1.2V using resistor divider from VLDO to AGND. The resistor divider must always be populated for proper operation.
EN	15	I	Enable. Connecting the EN pin to a voltage greater than 0.6V enables the device. In addition, input undervoltage lockout (UVLO) can be adjusted by the user with a resistor divider from VIN to GND.
AGND	16	—	Ground. Return for the controller circuitry. Connect to PGND at printed circuit board level.
VIN	17	I	Controller input voltage. The voltage range of VIN is from 4.5V to 14V. Powers internal control circuitry. Can be connected to PVIN for single-supply operation.
SYNC	18	I	External clock input. SYNC accepts a 100kHz to 1MHz external clock. Use a duty cycle between 40% and 60% for the external clock. The switching frequency of the controller outputs are the same as the external clock frequency. RT must be populated such that the frequency set by the resistor coincides with the external clock frequency.
RT	19	I/O	Switching frequency programming for controller. Connect a resistor from RT to GND to set the switching frequency of the controller. If an external clock input is used, the resistor still must be connected and selected to match the external clock frequency.
REFCAP	20	O	1.2V internal reference output. Requires a 470nF external capacitor to AGND. Do not load with external circuitry.
SS	21	I/O	Soft start. An external capacitor connected to this pin sets the internal voltage reference rise time. Can be used for tracking and sequencing.
VSENSE	22	I	Inverting input of the error amplifier. Feedback pin that is nominally set to 0.6V using a resistor divider from the converter output.
RSC	23	I/O	Slope compensation programming for the controller. A resistor from RSC to AGND sets the desired slope compensation.
COMP	24	I/O	Error amplifier output. The output is divided down by a factor CCSR and this scaled voltage is the input to the PWM comparator. Connect frequency compensation to this pin.
NC	12, 13	—	No connect. This pin is not internally connected. These pins can be connected to GND to prevent charge buildup.
THERMAL PAD	—	—	Thermal pad. Internally connected to AGND. Connect to one or more ground planes on the printed circuit board for improved thermal dissipation.

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VIN	–0.3	16	V
PVIN	–0.3	16	V
SYNC	–0.3	7.5	V
EN	–0.3	7.5	V
RT	–0.3	3.6	V
VSENSE	–0.3	3.6	V
SS	–0.3	3.3	V
RSC	–0.3	3.6	V
COMP(2)	–0.3	6.0	V
	–0.3	VLDO+0.3	
CS_ILIM	–0.3	7.5	V
OUTH(2)	–0.3	16	V
	–0.3	PVIN+0.3	
OUTL	–0.3	16	V
OUTH_REF	–0.3	10	V
VLDO(2)	–0.3	7.5	V
	–0.3	VIN+0.3	
VLDO_FB	–0.3	1.9	V
REFCAP(2)	–0.3	1.9	V
	–0.3	VLDO+0.3	
Operating junction temperature	–55	150	°C
Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The absolute maximum voltage of the pin should adhere to the lower of the two presented conditions.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VIN	4.5		14	V
PVIN	4.5		14	V
SYNC	0		7	V
EN	0		7	V
COMP(1)	0		2.3	V
VSENSE	0	0.6	1	V
VLDO_FB	0	1.2	1.3	V
SS	0		1.5	V
CS_ILIM	0		1.5	V
OUTH, OUTL	0		14	V
Input voltage slew rate (VIN)			0.03	V/µs
Input voltage slew rate (PVIN)			0.03	V/µs
Operating junction temperature	–55		125	°C

(1) See *Current Sense and PWM Generation* for additional details.

7.4 Thermal Information

THERMAL METRIC(1)		TP7H502x HTSSOP 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

T_A = –55°C to 125°C, PVIN = VIN = 4.5V to 14V, VLDO = 5V, no load on OUT (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SUBGROUP[1]	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGES AND CURRENTS								
IDD	Operating supply current	No load for OUT, PVIN = VIN	f_{SW} = 100kHz	1, 2, 3		6.8	10	mA
			f_{SW} = 500kHz	1, 2, 3		8.5	15.5	
			f_{SW} = 1MHz	1, 2, 3		10.3	18	
		C_{LOAD} = 1000pF for OUT, PVIN = VIN	f_{SW} = 100kHz	1, 2, 3		8.5	12	
			f_{SW} = 500kHz	1, 2, 3		14.5	20	
			f_{SW} = 1MHz	1, 2, 3		22.5	28	
		C_{LOAD} = 1000pF for OUT, VIN = 12V, PVIN = VLDO = 5V	f_{SW} = 100kHz	1, 2, 3		7	10	
			f_{SW} = 500kHz	1, 2, 3		10	13	
			f_{SW} = 1MHz	1, 2, 3		13.5	20	
I_{start}	Startup current	VIN = 3.5V		1, 2, 3		3.8	5	mA
$I_{DD(dis)}$	Standby current	EN = 0V		1, 2, 3			7	mA
VLDO	Internal linear regulator output voltage	C_{VLDO} = 1µF	5V ≤ VIN ≤ 14V, RVT = 10kΩ, RVB = 3.74kΩ	1, 2, 3	4.36	4.49	4.62	V
			5.5V ≤ VIN ≤ 14V, RVT = 10kΩ, RVB = 3.24kΩ	1, 2, 3	4.84	4.99	5.14	
			6V ≤ VIN ≤ 14V, RVT = 10 kΩ, RVB = 2.87kΩ	1, 2, 3	5.31	5.48	5.65	
VLDO_DO	Internal linear dropout voltage	I_{VLDO} = 25mA, C_{VLDO} = 1µF		1, 2, 3			0.4	V
I_VLDO	Maximum VLDO output current	VLDO ≥ 96% of VLDO at no load, C_{VLDO} = 1µF	VIN = VLDO + 0.5V	1, 2, 3	30[4]			mA
			VIN = VLDO + 1V	1, 2, 3	60[4]			
			VIN ≥ 7V	1, 2, 3	95[4]			
ENABLE AND UNDERVOLTAGE LOCKOUT								
V_{ENR}	Enable rising threshold			1, 2, 3	0.57	0.63	0.66	V
V_{ENF}	Enable falling threshold			1, 2, 3	0.48	0.52	0.55	V
I_{EN}	Enable input leakage current	VIN = 14V	EN = 1V	1, 2, 3		0.1	100	nA
			EN = 7V	1, 2, 3		1.5	250	nA
$PVIN_{UVLOR}$	PVIN UVLO rising			1, 2, 3	3.65	3.76	3.95	V
$PVIN_{UVLOF}$	PVIN UVLO falling			1, 2, 3	3.45	3.56	3.75	V
VIN_{UVLOR}	VIN UVLO rising			1, 2, 3	3.85	3.96	4.15	V
VIN_{UVLOF}	VIN UVLO falling			1, 2, 3	3.65	3.76	3.95	V
$VLDO_{UVLOR}$	VLDO UVLO rising			1, 2, 3	3.65	3.77	3.95	V
$VLDO_{UVLOF}$	VLDO UVLO falling			1, 2, 3	3.45	3.59	3.75	V
SOFT START								
I_{SS}	Soft-start current	SS = 0.3V		1, 2, 3	2.0	2.8	3.3	µA
ERROR AMPLIFIER								
EA_{gm}	Error amplifier transconductance	–10µA < I_{COMP} < 10µA, $V_{(COMP)}$ = 1V		1, 2, 3	1150	1750	2650	µA/V
EA_{DC}	DC gain	V_{SENSE} = 0.6V				13000		V/V
EA_{ISRC}	Error amplifier source current	$V_{(COMP)}$ = 1V, 100mV input overdrive		1, 2, 3	95		195	µA

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7.5 Electrical Characteristics (continued)

T_A = –55°C to 125°C, PVIN = VIN = 4.5V to 14V, VLDO = 5V, no load on OUT (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SUBGROUP[1]	MIN	TYP	MAX	UNIT
EA_{ISNK}	Error amplifier sink current	$V_{(COMP)}$ = 1V, 100mV input overdrive		1, 2, 3	95		195	µA
EA_{ro}	Error amplifier output resistance					8		MΩ
EA_{OS}	Error amplifier input offset voltage			1, 2, 3	–4.5		5.5	mV
EA_{IB}	Error amplifier input bias current			1, 2, 3			25	nA
EA_{BW}	Bandwidth			1, 2, 3		7.5		MHz
OSCILLATOR								
$SYNC_{IL}$	SYNC in low-level	VLDO = 4.5V	VIN < 5V	1, 2, 3			0.8	V
			VIN ≥ 5V	1, 2, 3			0.8	
		VLDO = 5.5V	VIN < 6V	1, 2, 3			0.8	
			VIN ≥ 6V	1, 2, 3			0.8	
$SYNC_{IH}$	SYNC in high-level	VLDO = 4.5V	VIN < 5V	1, 2, 3	3.5			V
			VIN ≥ 5V	1, 2, 3	3.5			
		VLDO = 5.5V	VIN < 6V	1, 2, 3	3.5			
			VIN ≥ 6V	1, 2, 3	3.5			
f_{SYNC}	SYNC in frequency range			4, 5, 6	100		1000	kHz
D_{SYNC}	SYNC in duty cycle (TPS7H5020)	Duty cycle of external clock		4, 5, 6	40%		60%	
D_{SYNC}	SYNC in duty cycle (TPS7H5021)[5]	Duty cycle of external clock		4, 5, 6	48%		52%	
DT_{INT}	External clock to internal clock detection time	RT populated		9, 10, 11		2	5	$(1/f_{sw})$ s
DT_{EXT}	Internal clock to external clock detection time	RT populated		9, 10, 11		2	5	$(1/f_{sw})$ s
f_{SW}	RT programmed switching frequency	RT = 1.18MΩ		4, 5, 6	80	95	110	kHz
		RT = 560kΩ		4, 5, 6	180	195	220	
		RT = 210kΩ		4, 5, 6	475	500	550	
		RT = 100kΩ		4, 5, 6	950	1000	1100	
VOLTAGE REFERENCE								
VREF	Internal voltage reference[2]	Measured at COMP, COMP = VSENSE	T_A = 25°C	1	0.597	0.600	0.603	V
			T_A = –55°C	3	0.594	0.598	0.602	
			T_A = 125°C	2	0.597	0.601	0.604	
REFCAP	REFCAP voltage	C_{REFCAP} = 470nF		1, 2, 3	1.211	1.223	1.235	V
CURRENT SENSE								
CCSR	COMP to CS_ILIM ratio	RSC = open		1, 2, 3	1.94	2.0	2.06	
V_{CS_ILIM}	Current limit (overcurrent) threshold			1, 2, 3	0.96	1.0	1.04	V
	CS_ILIM to OUT delay	CS_ILIM = 1V to 90% of OUT falling				65	115	ns
SLOPE COMPENSATION								
SC	Slope compensation	f_{SW} = 100kHz, RSC = 1.18MΩ				0.029		V/µs
		f_{SW} = 200kHz, RSC = 562kΩ				0.072		
		f_{SW} = 500kHz, RSC = 100kΩ				0.306		
		f_{SW} = 1000kHz, RSC = 49.9kΩ				0.605		
THERMAL SHUTDOWN								
T_{SD}	Thermal shutdown entry					185		°C

ADVANCE INFORMATION

7.5 Electrical Characteristics (continued)

T_A = –55°C to 125°C, PVIN = VIN = 4.5V to 14V, VLDO = 5V, no load on OUT (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SUBGROUP[1]	MIN	TYP	MAX	UNIT
T_{SD_HYS}	Thermal shutdown hysteresis					15		°C
GATE DRIVER								
V_{OL}	Low-level voltage	I_{OL} = 50mA		1, 2, 3		0.08	0.15	V
PVIN - V_{OH}	High-level voltage	I_{OH} = 50mA		1, 2, 3		0.13	0.25	V
t_{R_OUT}	OUT rise time	C_{LOAD} = 1000pF, 10% to 90%	VIN = PVIN = 4.5V	9, 10, 11		7	16	ns
			VIN = PVIN = 5V	9, 10, 11		7	16	
			VIN = PVIN = 12V	9, 10, 11		9.5	20	
			VIN = PVIN = 14V	9, 10, 11		11	20	
			VIN = 12V, PVIN = VLDO	9, 10, 11		8.5	16	
		C_{LOAD} = 220pF, 10% to 90%	VIN = 12V, PVIN = VLDO	9, 10, 11		4.5	12	
t_{F_OUT}	OUT fall time	C_{LOAD} = 1000pF, 90% to 10%	VIN = PVIN = 4.5V	9, 10, 11		6.5	16	ns
			VIN = PVIN = 5V	9, 10, 11		6.5	16	
			VIN = PVIN = 12V	9, 10, 11		9.5	20	
			VIN = PVIN = 14V	9, 10, 11		10.5	20	
			VIN = 12V, PVIN = VLDO	9, 10, 11		6.5	16	
		C_{LOAD} = 220pF, 90% to 10%	VIN = 12V, PVIN = VLDO	9, 10, 11		5	12	
I_{OH}	Peak source current	PVIN = 4.5V		1, 2, 3		0.55		A
		PVIN = 5V		1, 2, 3		0.7		
		PVIN = 12V		1, 2, 3		1.2		
		PVIN = 14V		1, 2, 3		1.2		
		VIN = 12V, PVIN = VLDO	VLDO = 4.5V	1, 2, 3		0.55		
			VLDO = 5V	1, 2, 3		0.7		
			VLDO = 5.5V	1, 2, 3		0.85		
I_{OL}	Peak sink current	PVIN = 4.5V		1, 2, 3		0.7		A
		PVIN = 5V		1, 2, 3		0.8		
		PVIN = 12V		1, 2, 3		1.3		
		PVIN = 14V		1, 2, 3		1.3		
		VIN = 12V, PVIN = VLDO	VLDO = 4.5V	1, 2, 3		1.05		
			VLDO = 5V	1, 2, 3		1.3		
			VLDO = 5.5V	1, 2, 3		1.55		
R_{OH}	Pull-up resistance	100mA from OUT		1, 2, 3		2.6	4.7	Ω
R_{OL}	Pull-down resistance	100mA into OUT		1, 2, 3		1.6	2.8	Ω
V_{UCLAMP}	Unpowered OUT clamp voltage	Switching disabled, , 1mA pull-up applied to OUT	PVIN = 0V	1, 2, 3		0.7	1	V
			0V < PVIN < 5V	1, 2, 3		1.8	2.5	
PWM AND DUTY CYCLE								
T_{LEB}	Leading edge blank time	5V ≤ VIN ≤ 14V, 10% of OUT rising to end of blanking		9, 10, 11		35	80	ns

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7.5 Electrical Characteristics (continued)

T_A = –55°C to 125°C, PVIN = VIN = 4.5V to 14V, VLDO = 5V, no load on OUT (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
t_{on_min}	Minimum on-time(3)		9, 10, 11		135	165	ns
t_{off_min}	Minimum off-time (TPS7H5020)(3)		9, 10, 11		55	65	ns
D_{MAX}	Maximum duty cycle (TPS7H5021)(5)		9, 10, 11	43%	46%	50%	

(1) Subgroups are applicable for QML parts. For subgroup definitions, see Section 7.6.
(2) Measured at COMP pin to include error amplifier offset.
(3) See *Minimum On-Time and Off-Time* for additional details.
(4) VLDO can support this current, at the least, for test conditions specified. However, for controller operation with PVIN connected to VLDO, it is recommended to keep the external current drawn from VLDO below this value for the most reliable operation.
(5) TPS7H5021 is a product preview device. This specification is provided for information only.

7.6 Quality Conformance Inspection

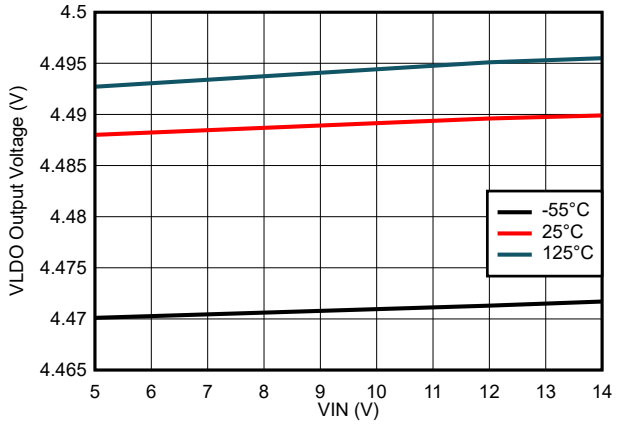
MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

ADVANCE INFORMATION

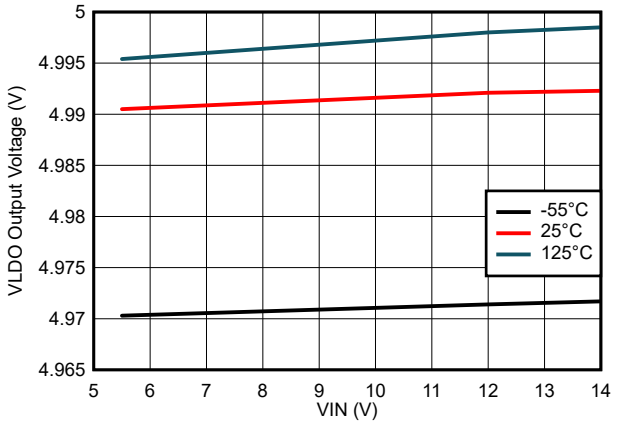
7.7 Typical Characteristics

Typical characteristics shown are with PVIN=VIN from 4.5V to 14V, 500kHz switching frequency, and at T_A = –55°C, 25°C, and 125°C, unless otherwise noted.



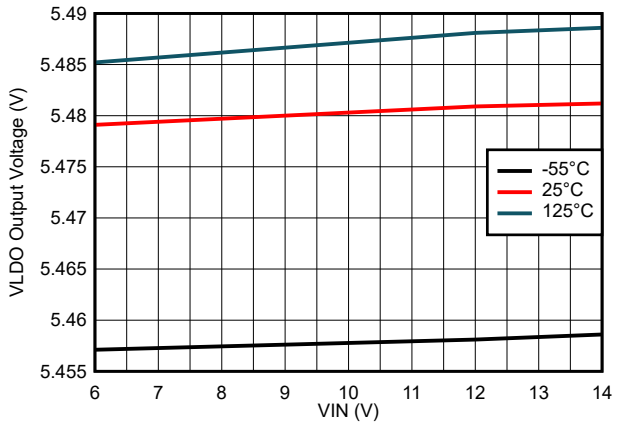
R_{VT} = 10kΩ, R_{VB} = 3.74kΩ

Figure 7-1. Internal Linear Regulator Output Voltage vs Input Voltage



R_{VT} = 10kΩ, R_{VB} = 3.24kΩ

Figure 7-2. Internal Linear Regulator Output Voltage vs Input Voltage



R_{VT} = 10kΩ, R_{VB} = 2.87kΩ

Figure 7-3. Internal Linear Regulator Output Voltage vs Input Voltage

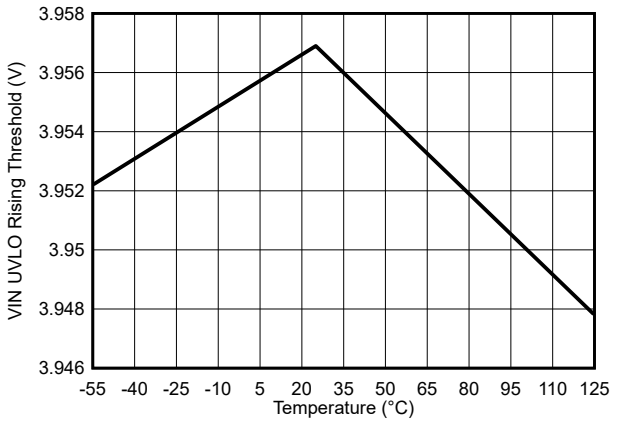


Figure 7-4. VIN UVLO Rising Threshold vs Temperature

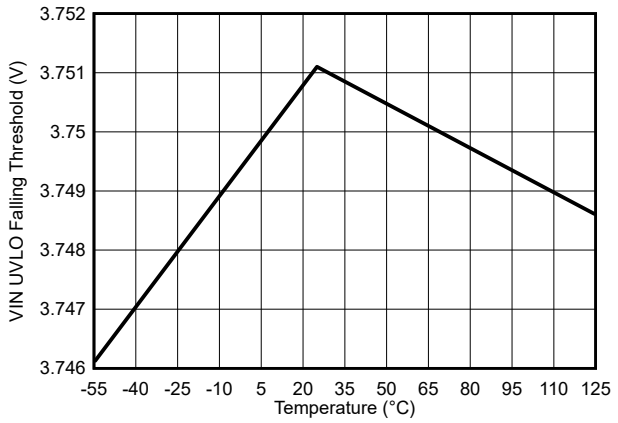


Figure 7-5. VIN UVLO Falling Threshold vs Temperature

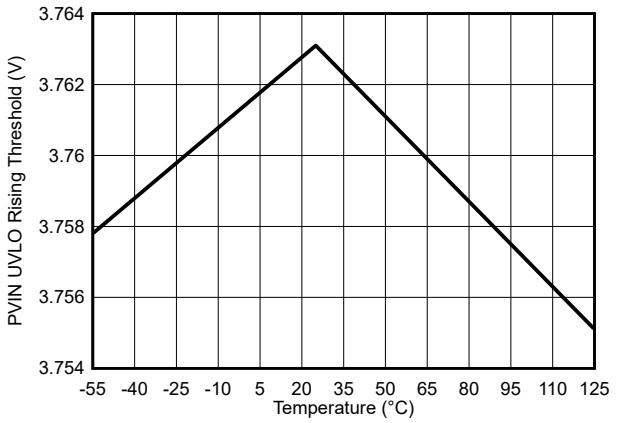


Figure 7-6. PVIN UVLO Rising Threshold vs Temperature

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7.7 Typical Characteristics (continued)

Typical characteristics shown are with PVIN=VIN from 4.5V to 14V, 500kHz switching frequency, and at T_A = –55°C, 25°C, and 125°C, unless otherwise noted.

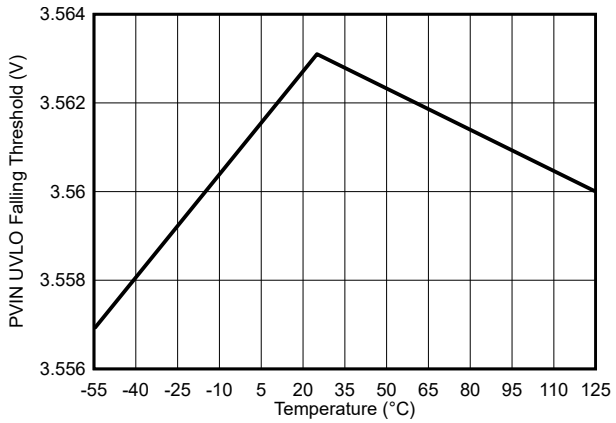
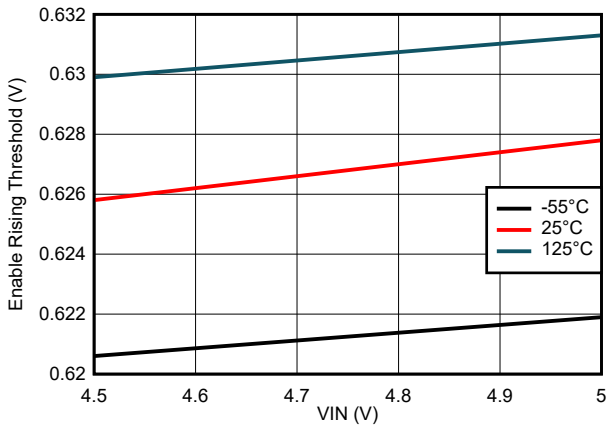
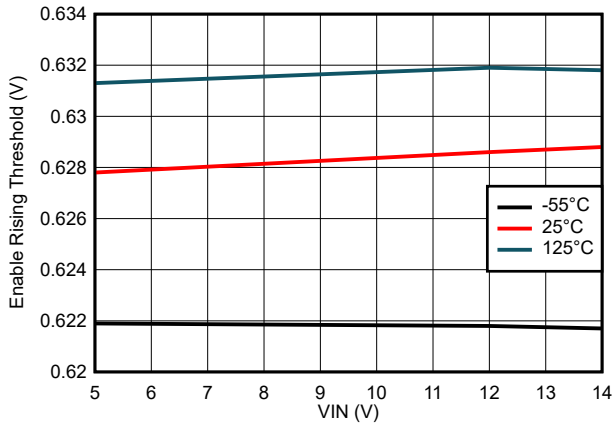


Figure 7-7. PVIN UVLO Falling Threshold vs Temperature



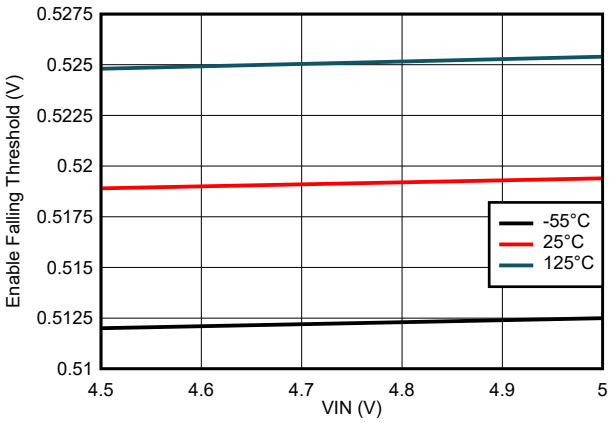
VIN = 4.5V to 5V

Figure 7-8. Enable Rising Threshold vs Input Voltage



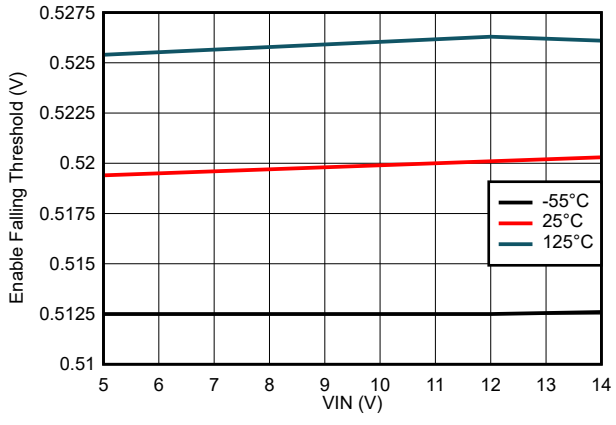
VIN = 5V to 14V

Figure 7-9. Enable Rising Threshold vs Input Voltage



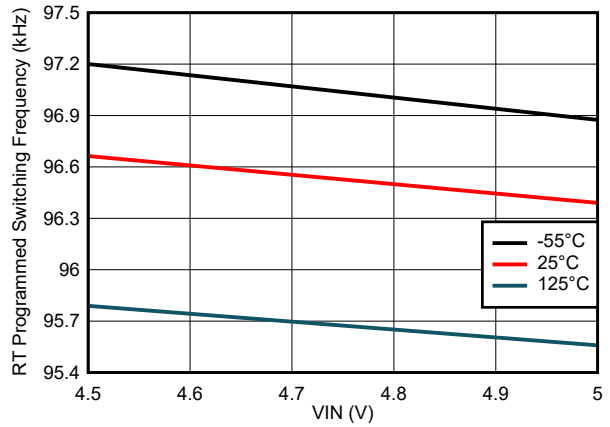
VIN = 4.5V to 5V

Figure 7-10. Enable Falling Threshold vs Input Voltage



VIN = 5V to 14V

Figure 7-11. Enable Falling Threshold vs Input Voltage

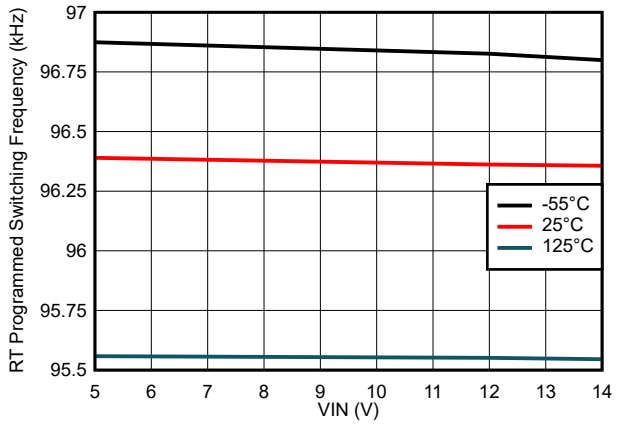


VIN = 4.5V to 5V, RT = 1.18MΩ

Figure 7-12. Switching Frequency vs Input Voltage

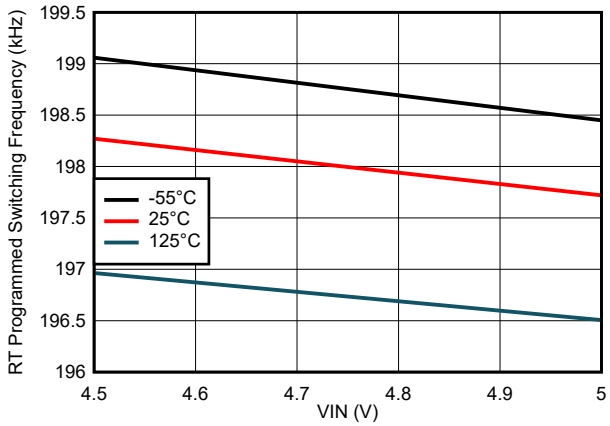
7.7 Typical Characteristics (continued)

Typical characteristics shown are with PVIN=VIN from 4.5V to 14V, 500kHz switching frequency, and at T_A = –55°C, 25°C, and 125°C, unless otherwise noted.



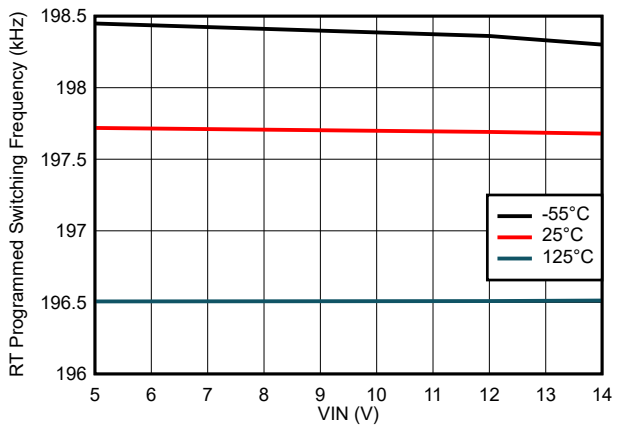
VIN = 5V to 14V, RT = 1.18MΩ

Figure 7-13. Switching Frequency vs Input Voltage



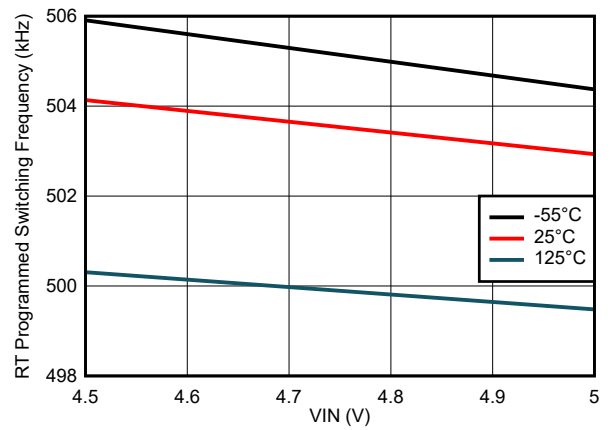
VIN = 4.5V to 5V, RT = 560kΩ

Figure 7-14. Switching Frequency vs Input Voltage



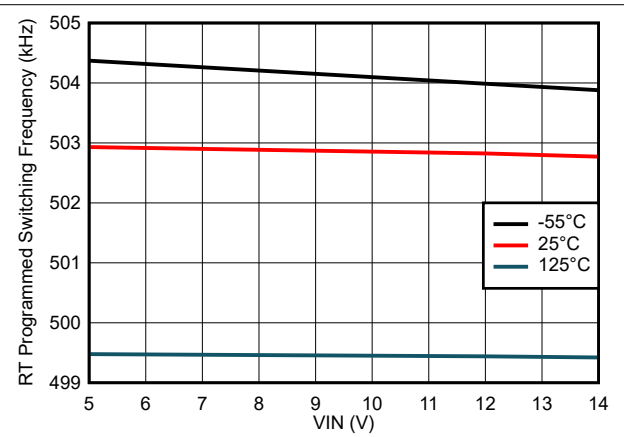
VIN = 5V to 14V, RT = 560kΩ

Figure 7-15. Switching Frequency vs Input Voltage



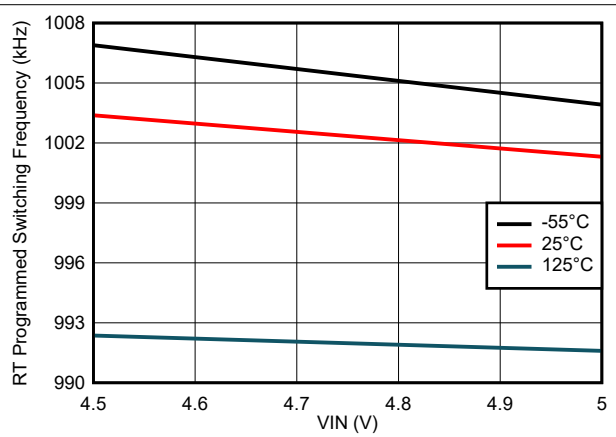
VIN = 4.5V to 5V, RT = 210kΩ

Figure 7-16. Switching Frequency vs Input Voltage



VIN = 5V to 14V, RT = 210kΩ

Figure 7-17. Switching Frequency vs Input Voltage



VIN = 4.5V to 5V, RT = 100kΩ

Figure 7-18. Switching Frequency vs Input Voltage

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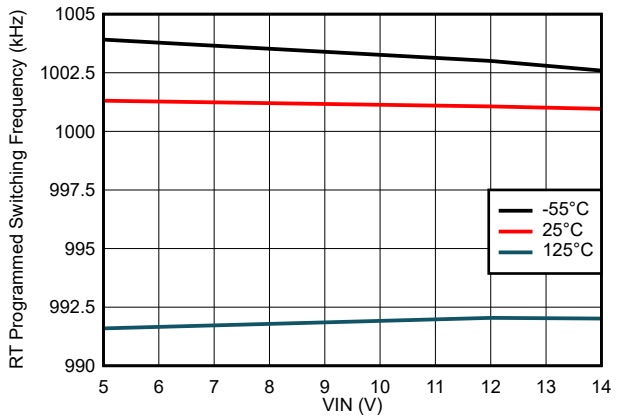
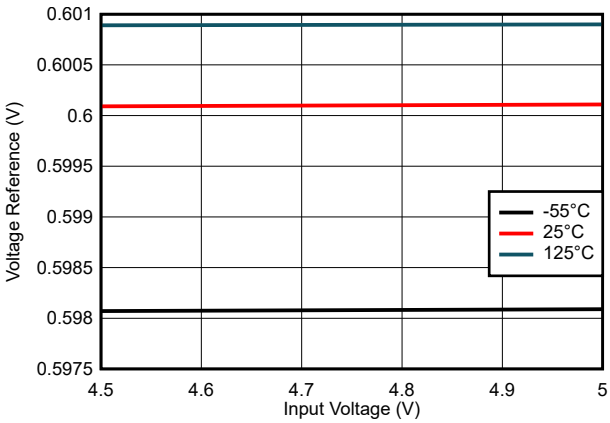
7.7 Typical Characteristics (continued)

Typical characteristics shown are with PVIN=VIN from 4.5V to 14V, 500kHz switching frequency, and at T_A = –55°C, 25°C, and 125°C, unless otherwise noted.



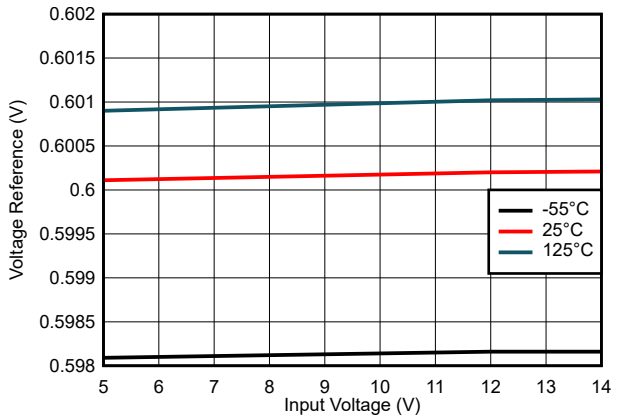
VIN = 5V to 14V, RT = 100kΩ

Figure 7-19. Switching Frequency vs Input Voltage



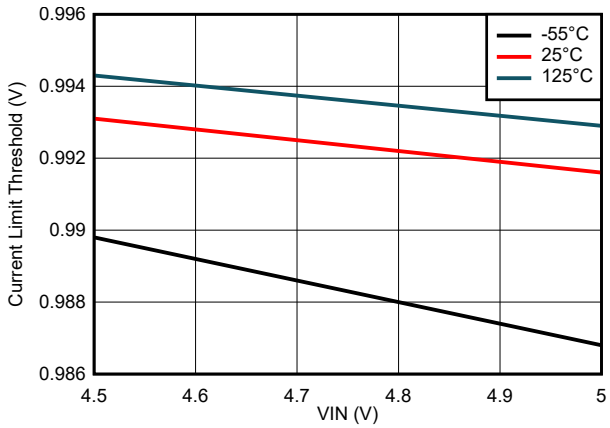
VIN = 4.5V to 5V

Figure 7-20. Internal Voltage Reference vs Input Voltage



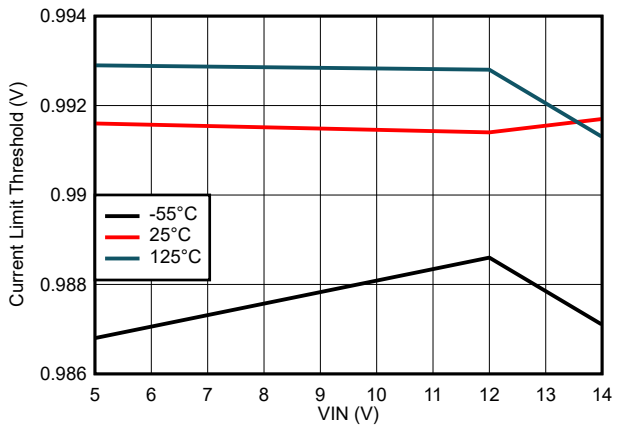
VIN = 5V to 14V

Figure 7-21. Internal Voltage Reference vs Input Voltage



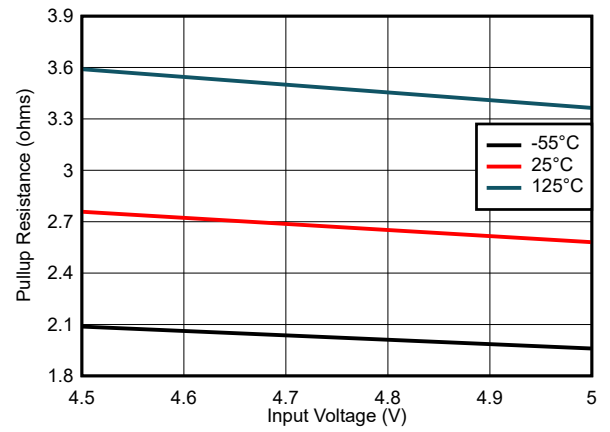
VIN = 4.5V to 5V

Figure 7-22. Current Limit Threshold vs Input Voltage



VIN = 5V to 14V

Figure 7-23. Current Limit Threshold vs Input Voltage

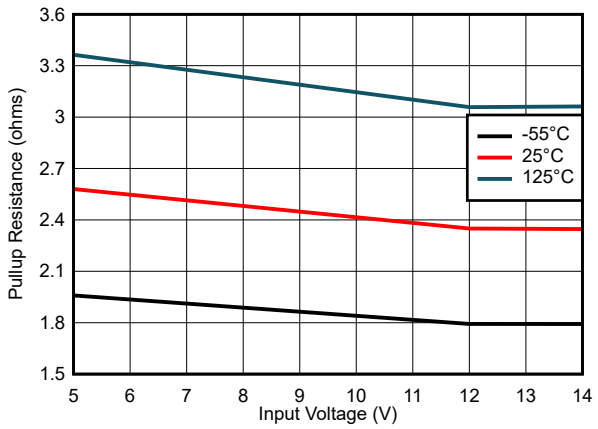


VIN = 4.5V to 5V

Figure 7-24. Pullup Resistance vs Input Voltage

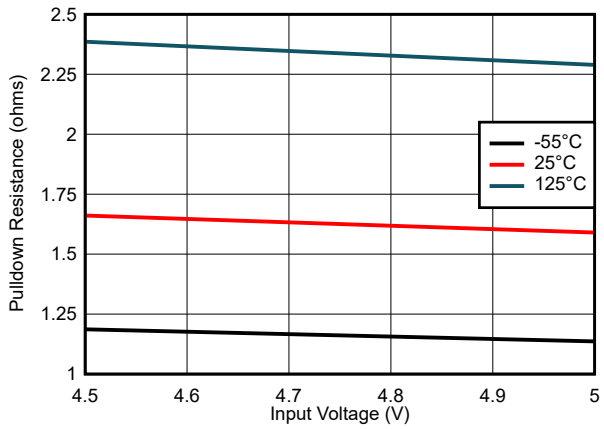
7.7 Typical Characteristics (continued)

Typical characteristics shown are with PVIN=VIN from 4.5V to 14V, 500kHz switching frequency, and at T_A = –55°C, 25°C, and 125°C, unless otherwise noted.



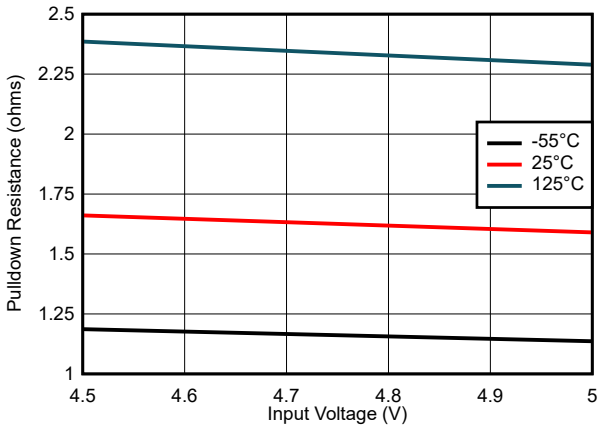
VIN = 5V to 14V

Figure 7-25. Pullup Resistance vs Input Voltage



VIN = 4.5V to 5V

Figure 7-26. Pulldown Resistance vs Input Voltage



VIN = 5V to 14V

Figure 7-27. Pulldown Resistance vs Input Voltage

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8 Detailed Description

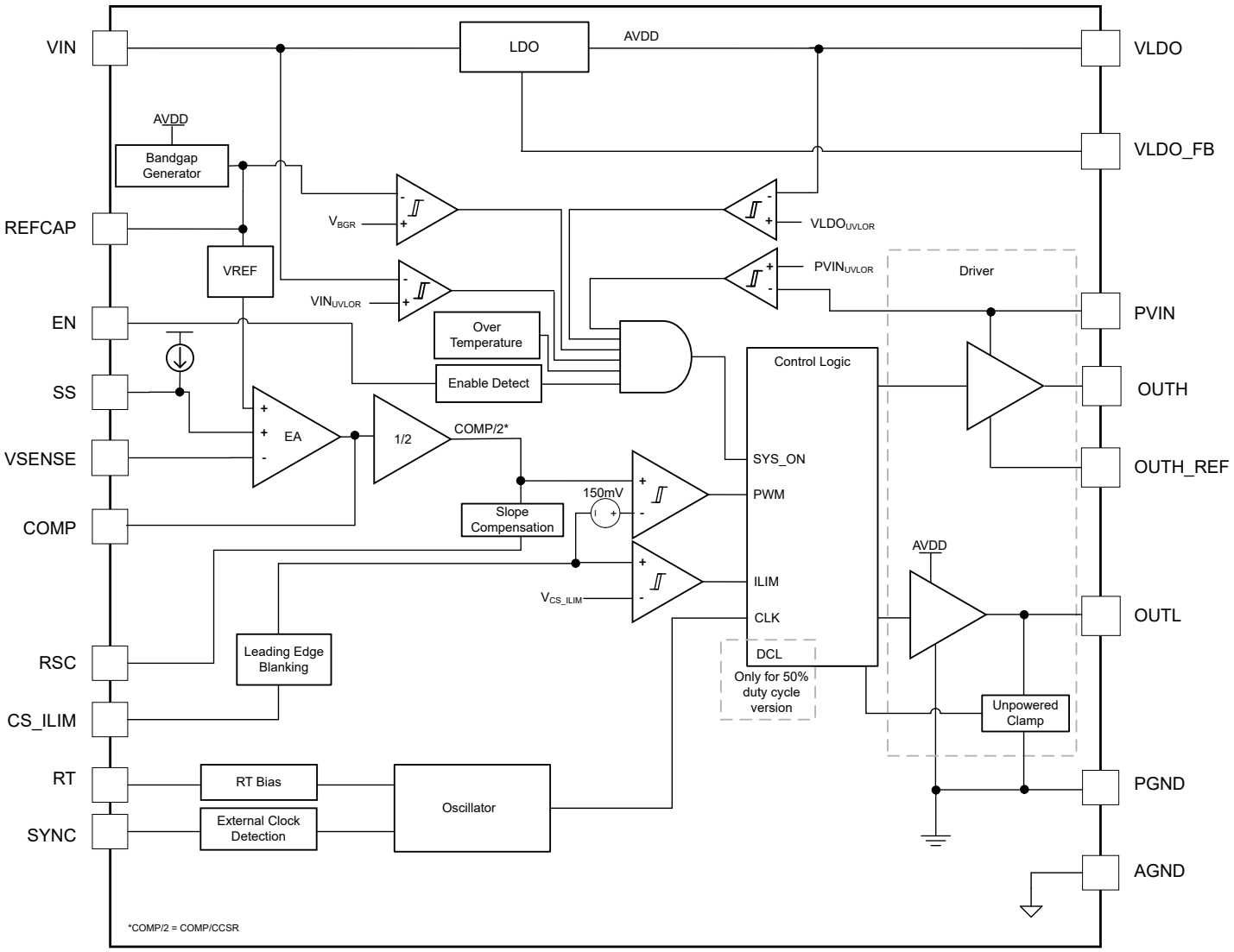
8.1 Overview

The TPS7H502x is a radiation-hardened current mode, single-ended PWM controller that contains an integrated gate driver. The device is capable of operation up to 1MHz in all operational modes. This controller is intended for use in space-grade power controller designs and can support topologies such as the flyback, forward, and the boost. The TPS7H5020 has a nominal maximum duty cycle of 100%, while the TPS7H5021 has a nominal 50% duty cycle limit.

The controller also features a 0.6V ±1% voltage reference to enable high accuracy converter designs. Features such as soft-start, enable, and adjustable slope-compensation are included in the controller, simplifying the overall converter design and minimizing the external components needed. The converter also can be synchronized to an external clock through the SYNC pin. The external clock synchronization range is from 100kHz to 1MHz, which is the same as the frequency range in internal oscillator mode.

The controller offers separate voltage inputs for the controller voltage and driver stage though the VIN and PVIN pins, respectively. The voltage range for both of these inputs is from 4.5V to 14V, and offers the user a great deal of flexibility. The integrated driver can be used with both silicon FETs (typical 12V gate voltage) as well as GaN power semiconductor devices (typical 5V gate voltage). When driving GaN devices, the VLDO regulator output can be tied directly to PVIN or a separate supply can be utilized at PVIN if the user desires. VLDO is programmable from 4.5V to 5.5V.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Voltage (VIN) and VLDO

During steady state operation, the input voltage of the TPS7H502x must be between 4.5V and 14V. A minimum bypass capacitance of at least 0.1µF is needed between VIN and AGND. The input bypass capacitors should be placed as close to the controller as possible. A resistor divider connected between VIN, EN, and GND can be used to adjust the input voltage UVLO.

The voltage applied at VIN serves as the input for the internal regulator that generates the voltage at VLDO. The VLDO output is programmable from 4.5V to 5.5V. This allows for connecting VLDO to PVIN and driving GaN power semiconductor devices using the controller. When programming VLDO, the resistor divider consists of two resistors: R_{VT} between VLDO and VLDO_FB, and R_{VB} between VLDO_FB and AGND. Equation 1 can be used to select the proper R_{VB} resistor.

$$R_{VB} = \frac{V_{REFCAP}}{V_{LDO} - V_{REFCAP}} \times R_{VT} \quad (1)$$

where:

- V_{REFCAP} is 1.223V (typical)
- VLDO is the desired output voltage of the internal regulator between 4.5V and 5.5V
- R_{VT} is the value of the top resistor, between VLDO and VLDO_FB, selected by the user (i.e. 10kΩ)

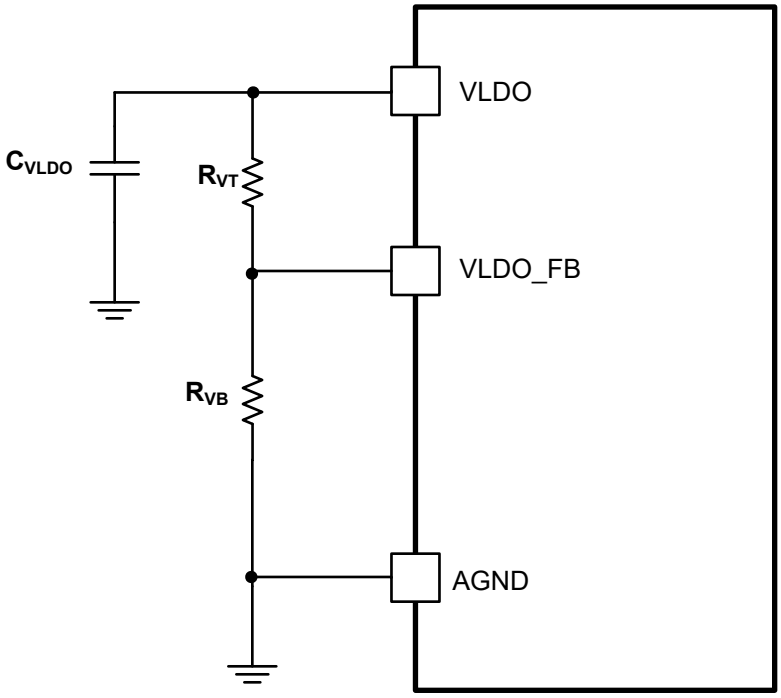

Figure 8-1. Configuration for Programming VLDO Output Voltage

For applications in which VLDO is not used as the input to the driver stage, it is recommended to select resistors to set VLDO to 5V. The resistors R_{VT} and R_{VB} must always be populated. The maximum dropout voltage for the VLDO regulator is 0.4V. Note that as the headroom voltage increases for the VLDO regulator, its output current capacity also increases until the input voltage reaches 7V. At this point, the full current capability of the VLDO regulator is realized. See the Electrical Characteristics for more details. This becomes critical for applications in which VLDO is used to provide a regulated input voltage at PVIN for driving GaN FETs, as the gate current demanded by the FET is determined by:

$$I_g = Q_g \times f_{sw} \quad (2)$$

where:

- I_g is the gate current of the GaN FET
- Q_g is the total gate charge of the GaN FET (found in the manufacturer's data sheet)
- f_{sw} is the power converter switching frequency

The external current to be supplied to the FET by VLDO in this scenario should not exceed the capability of the regulator. The recommended capacitance to be connected at VLDO is 1µF. The EN pin of the device can also be tied to VLDO.

8.3.2 Driver Input Voltage (PVIN)

The input voltage range of the driver stage of the TPS7H502x is between 4.5V and 14V. The voltage provided at the OUT pins of the device is approximately equal to the voltage supplied at PVIN. As such, the controller is able to be used to supply proper gate voltages for both silicon MOSFET and GaN FET based power converter designs. For silicon MOSFETs, the typical gate voltage is from 10V to 12V. GaN power semiconductor devices usually require 4.5V to 6V gate voltages. Since the required gate voltage is dependent on the switching device that is selected, the controller allows the user the capability to provide a voltage to the driver stage that is adequate for the specific application. PVIN can be tied directly to VIN for single supply operation. This configuration can be utilized for driving either silicon MOSFETs or GaN FETs. In this setup, the recommendation is to select R_{VT} and R_{VB} such that VLDO provides 5V for the internal circuitry. See *Input Voltage (VIN) and VLDO* for more details on programming the VLDO output.

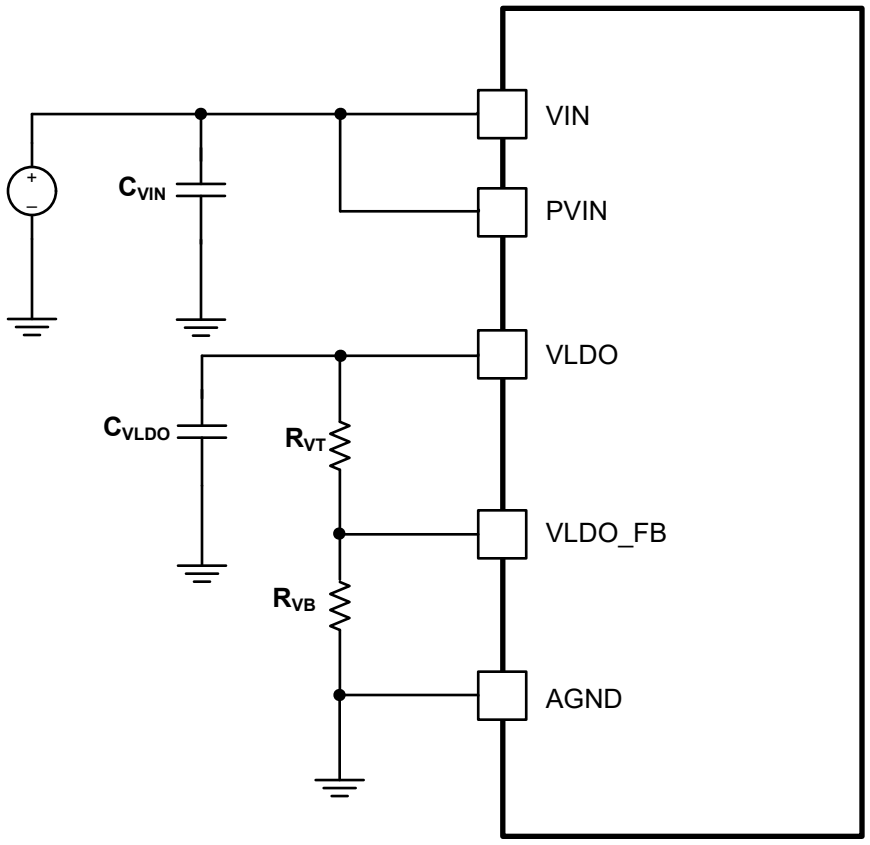

Figure 8-2. Configuration for PVIN to VIN Connection

VLDO can also be connected to PVIN for a 4.5V to 5.5V regulated gate drive voltage. A minimum capacitance of 1µF is recommended from PVIN to PGND. When PVIN is connected to VLDO, this can include the 1µF capacitance required at VLDO. Additional capacitance can be used, but the total capacitance is not to exceed 4.7µF to maintain proper stability for the VLDO regulator.

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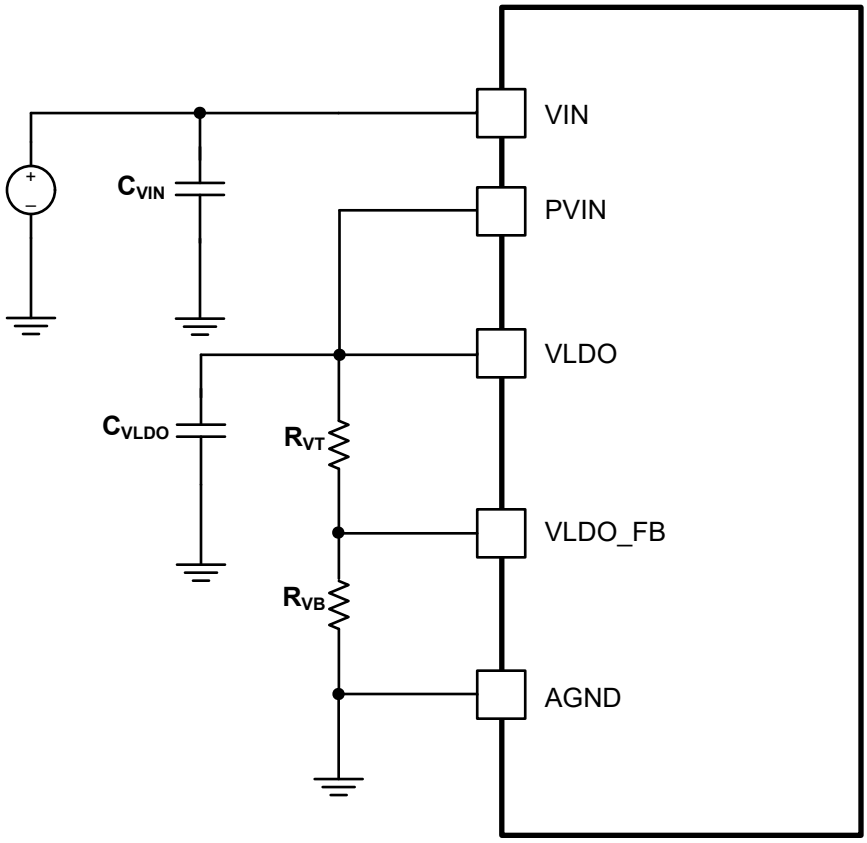

Figure 8-3. Configuration for PVIN to VLDO connection

8.3.3 Start-Up

Before the output of the controller will start switching, the following conditions must be met:

- VLDO exceeds its rising UVLO threshold
- VIN exceeds its rising UVLO threshold
- PVIN exceeds its rising UVLO threshold
- The internal 1.2V bandgap voltage is available
- The enable signal EN is above the rising voltage threshold
- The device junction temperature is below the thermal shutdown threshold

Once all of the aforementioned conditions are satisfied, the soft-start process will be initiated.

8.3.4 Enable and Undervoltage Lockout (UVLO)

There are several methods for enabling the TPS7H502x through the EN pin. The pin can be tied directly to VLDO, which would allow for the device to be enabled as soon as the voltage on VLDO surpasses the rising edge voltage threshold of the EN pin. The pin can also be driven with an externally generated signal or a compatible PGOOD signal for instances in which sequencing is desired. Lastly, two resistors can be used to program the controller to enable when VIN surpasses a user determined threshold, as shown in Figure 8-4 . The two resistors are configured as a divider, with one between VIN and EN and the other between EN and AGND.

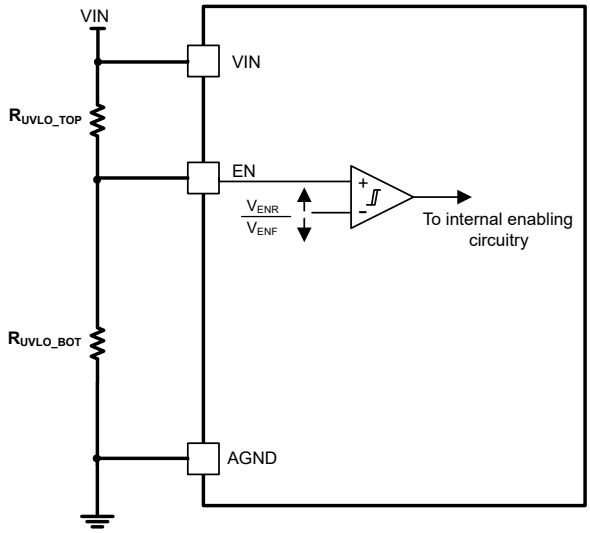

Figure 8-4. Enable Pin Configuration Using Two External Resistors

Using Equation 3, the user can calculate the value for R_{UVLO_TOP} for a chosen value of R_{UVLO_BOT} based on the desired maximum start-up voltage for the device. With these selected resistors Equation 4 can be used to determine the minimum start-up voltage.

$$R_{UVLO\_TOP} = R_{UVLO\_BOT} \times \left(\frac{V_{START\_MAX}}{V_{ENR\_MAX}} - 1 \right) \quad (3)$$

$$V_{START\_MIN} = V_{ENR\_MIN} \times \left(\frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1 \right) \quad (4)$$

In the two-resistor configuration of Figure 8-4, the controller will also shut down due to undervoltage lockout when the input voltage falls below a particular threshold. This is due to the hysteresis of the EN pin. In order to determine the voltages at which shutdown is expected to occur, use Equation 5 and Equation 6.

$$V_{STOP\_MAX} = V_{ENF\_MAX} \times \left(\frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1 \right) \quad (5)$$

$$V_{STOP\_MIN} = V_{ENF\_MIN} \times \left(\frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1 \right) \quad (6)$$

It is important to note that the user should take care when selecting the values for R_{UVLO_TOP} and R_{UVLO_BOT}. It is recommended to optimize the selection of these resistors for start-up in order to ensure proper operation. The UVLO value must be approximately 75% or less of the input voltage in order to ensure that the device turns on as expected under all circumstances. Setting the UVLO any higher may cause issues with the turn-on of the device. Figure 8-5 shows the expected start-up and UVLO voltages on a 12V rail where the maximum start-up voltage is 90% of the nominal input voltage. In this instance, turn-off will occur when the input voltage falls to between 75% and 65% of its nominal value.

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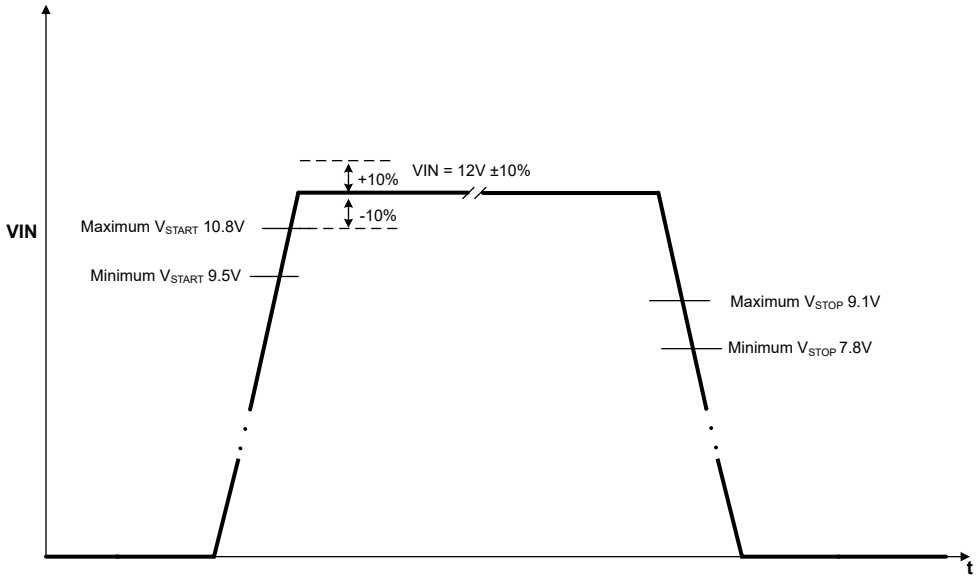

Figure 8-5. Start-Up and UVLO Values for Two-Resistor Configuration With VIN = 12V

8.3.5 Voltage Reference

The controller generates an internal 1.2V bandgap reference that is utilized throughout the various control logic blocks. This is the voltage present on the REFCAP pin during steady state operation. This voltage is divided down to 0.6V to produce the reference for the error amplifier. The error amplifier reference is measured at the COMP pin to account for offsets in the error amplifier and maintains regulation within ±1% as shown in *Specifications*. This tight reference tolerance allows for the user to design a highly accurate power converter. A 470nF capacitor to ground is required at the REFCAP pin for proper electrical operation as well as to ensure robust single-event transient (SET) performance of the device.

8.3.6 Error Amplifier

The TPS7H502x controller uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS pin voltage or the internal 0.6V voltage reference. The transconductance of the error amplifier is 1500µA/V during normal operation. The frequency compensation network is connected between COMP pin and AGND. The error amplifier DC gain is typically 14,500V/V.

8.3.7 Output Voltage Programming

The output voltage of the power converter is set by using a resistor divider from V_{OUT} of the converter to the VSENSE pin. The output voltage must be divided down to nominal voltage reference of 0.6V. Equation 7 can be used to select R_{BOTTOM}.

$$R_{BOTTOM} = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_{TOP} \quad (7)$$

where:

- V_{REF} is 0.6V (typical)
- V_{OUT} is the desired output voltage
- R_{TOP} is the value of the top resistor, selected by the user (i.e. 10kΩ)

The recommendation is to use low tolerance resistors (1% or less) for R_{BOTTOM} and R_{TOP} for improved output voltage setpoint accuracy.

8.3.8 Soft Start (SS)

The soft-start circuit increases the output voltage of the converter gradually until the steady-state programmed output is reached. During soft start, the error amplifier uses the voltage on the soft-start pin as its reference until the SS pin voltage rises above V_{REF}. Once the voltage at SS pin is above V_{REF}, the soft-start period is complete.

A capacitor between the SS pin and AGND controls the soft-start time of the PWM controller. The following equation can be used to select the capacitor for the desired soft-start time:

$$t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (8)$$

where:

- t_{SS} is the desired soft-start time
- V_{REF} is voltage reference of 0.6V (typical)
- I_{SS} is the soft-start charging current of 2.8µA (typical)

8.3.9 Switching Frequency and External Synchronization

The TPS7H502x controller has two modes for setting the switching frequency of the device: internal oscillator and external synchronization. The device is placed in one of these modes based on the state of the RT and SYNC pins. If there is a clock input detected on SYNC, it will run in external synchronization mode. Otherwise, the device runs on its internal oscillator at a frequency determined by a resistor from RT to AGND. RT must be populated in both operational modes.

Table 8-1. Oscillator Modes and Configurations

MODE	RT	SYNC	SWITCHING FREQUENCY
Internal Oscillator	Populated with resistor to AGND.	Floating	Configurable from 100kHz to 1MHz depending on RT value.
External Synchronization	Populated with resistor to AGND. Must be selected to match input clock frequency on SYNC.	Input for 100kHz to 1MHz external clock.	Synchronized to SYNC input clock. Switching is in phase with external clock at 1:1 frequency.

8.3.9.1 Internal Oscillator Mode

A resistor from the RT pin to AGND sets the switching frequency of the device. The TPS7H502x controller has a nominal switching frequency range of 100kHz to 1MHz. In internal oscillator mode, the RT pin must be populated. Equation 9 shows the calculation for the RT value based on the desired switching frequency. The curve in Figure 8-6 shows the RT value that corresponds to a given switching frequency for the TPS7H502x.

$$RT = \frac{112390}{f_{SW}} - 14.2 \quad (9)$$

where:

- RT is in kΩ
- f_{sw} is in kHz

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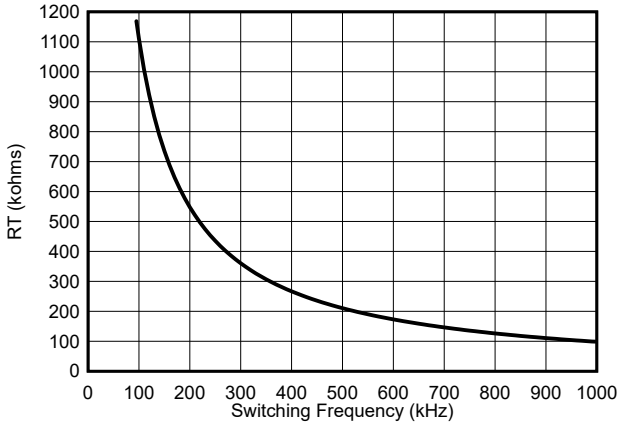

Figure 8-6. RT vs Switching Frequency

8.3.9.2 External Synchronization Mode

The controller can be used in external synchronization mode by applying a clock to the SYNC pin. The external clock that is applied must be set to the desired switching frequency. The external clock must be in the range of 100kHz to 1MHz with a duty cycle of 50%. It is recommended to use an external clock with 50% duty cycle. The controller will switch in phase with the clock signal that is applied at the SYNC pin during this mode. Note that the SYNC pin only operates as an input for the controller.

When operating in external syncrhonization mode, the RT pin must be populated with a resistor to AGND. The switching frequency set by the RT resistor should be within ±10% of the external clock frequency. The switching frequency is 1:1 with the external clock frequency. In the event that the controller is operating in internal oscillator mode before the application of the clock on the SYNC pin, it will take approximately 2-5 cycles after the clock is applied before the detection and switchover is made. If operating in external synchronization mode and the clock is lost, it takes approximately 2-5 cycles for the detection to be made, after which the switch to the internal oscillator will occur.

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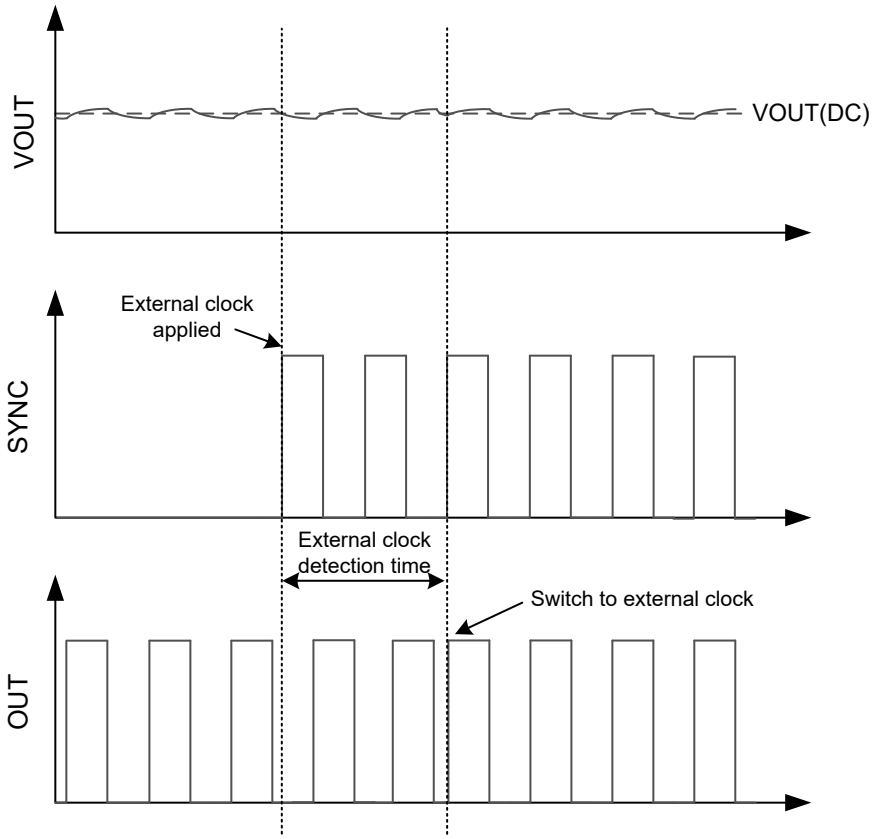

Figure 8-7. Internal to External Clock Transition

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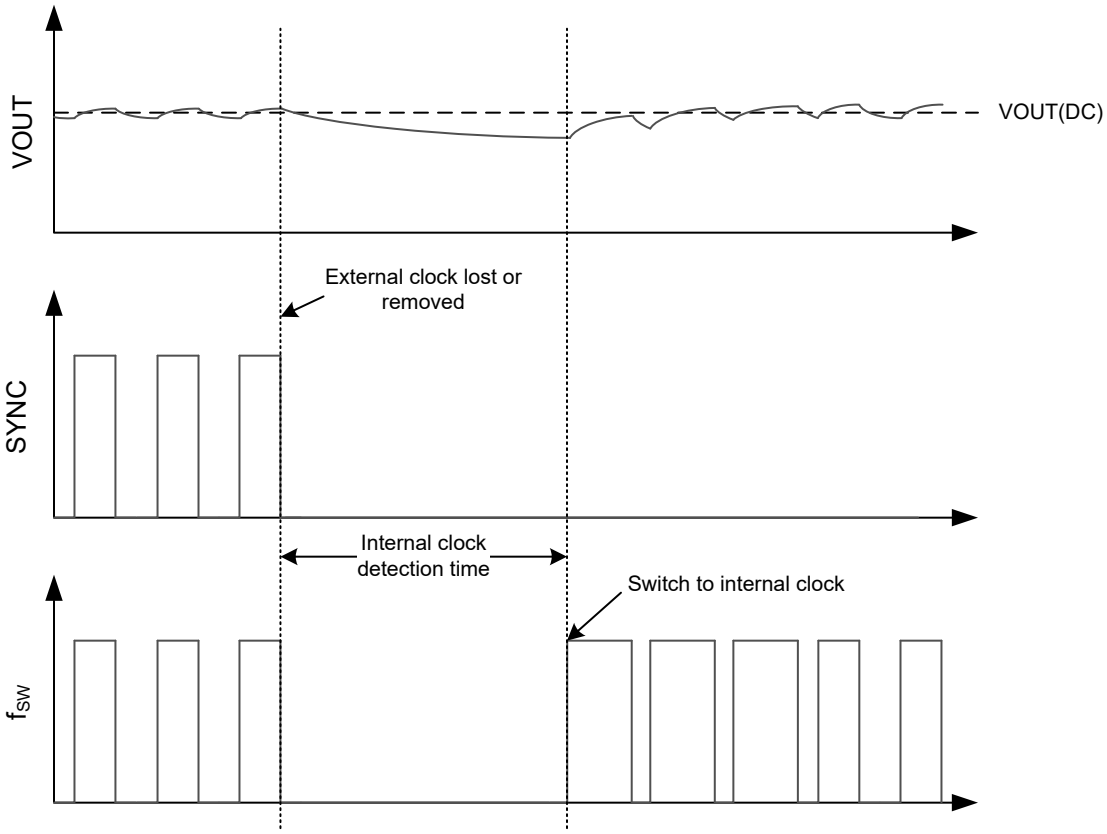

Figure 8-8. External to Internal Clock Transition

8.3.10 Duty Cycle Limit

The TPS7H5020 controller has a nominal 100% maximum duty cycle. In this controller, the output is capable of 100% duty cycle, but it is advised that the user impose a maximum duty cycle based on the controller minimum off-time as described in *Minimum On-Time and Off-Time*.

The TPS7H5021 controller has a nominal 50% maximum duty cycle. Refer to *Specifications* for the specifications related to this duty cycle limit. Note that if the external synchronization oscillator mode is used with this device, it is advised to provide an external clock with a precise 50% duty cycle in order to ensure that the device specifications are met. Using an external clock with a duty cycle range beyond 50 ±2% may result in sub-optimal maximum duty cycles.

Table 8-2. TPS7H502x Maximum Duty Cycles

DEVICE	MAXIMUM DUTY CYCLE (NOMINAL)
TPS7H5020	100%
TPS7H5021	50%

8.3.11 Minimum On-Time and Off-Time

The TPS7H502x output has a minimum on-time of approximately 120ns (typical). The minimum on-time is the smallest time duration for which the output remains in the on-state. As such, the minimum on-time can impose a restraint on the input-to-output conversion ratio of the power converter design. To overcome minimum on-time restrictions, careful selection of both the converter switching frequency and the transformer turns ratio (if applicable) is needed. For single switch forward, flyback, and boost converters in continuous conduction mode, the following equations can be used to check that the on time of the main power switch is sufficient for the intended design.

For forward:

$$t_{on\_min} < \frac{V_{OUT} + V_D}{(V_{IN} \times N_{SP}) \times f_{SW}} \quad (10)$$

where:

- t_{on_min} is the minimum on-time of the controller, with a maximum value of 130ns
- V_{OUT} is the desired output voltage of the converter
- V_{IN} is the input voltage of the converter
- V_D is the forward voltage of the rectifier diode
- N_{PS} is the primary-to-secondary turns ratio of the transformer
- N_{SP} is the secondary-to-primary turns ratio of the transformer (the inverse of N_{PS})
- f_{SW} is the desired switching frequency of the converter

For flyback:

$$t_{on\_min} < \frac{(V_{OUT} + V_D) \times N_{PS}}{(V_{IN} + (V_{OUT} + V_D) \times N_{PS}) \times f_{SW}} \quad (11)$$

For boost:

$$t_{on\_min} < \frac{V_{OUT} + V_D - V_{IN}}{(V_{OUT} + V_D) \times f_{SW}} \quad (12)$$

Likewise, the minimum off-time also imposes restrictions on the converter operation. The minimum off-time is the smallest time duration that the output must remain off before subsequent turn-on. If the output is turned off during the switching cycle due to normal PWM operation, the output remains in the off-state for at least 40ns (typical). In most applications, the duty cycle of the converter during steady state remains well below 100% and allows for the output to be off much longer than this duration. The minimum off-time for the controller is not a concern for the TPS7H5021 in which the duty cycle is restricted to a 50% nominal maximum.

There are circumstances in which the mimimum off-time must be taken into consideration when using the TPS7H5020 in power converter designs. Specifically, such cases occur when duty cycle is near 100% and turn-off happens close to the beginning of the next switching cycle. The intended off-time in these applications, as dictated by the converter feedback loop, is less than the minimum off-time of the controller. As such, the minimum off-time duration of the controller delays the output turn-on in the following switching cycle. While this must be taken into account at all operational frequencies, the effect is more pronounced at higher frequencies in which the minimum off-time constitutes a higher portion of the switching period. For example, at 1MHz switching frequency, the turn-on of the next cycle is delayed if the duty cycle surpasses 96% (nominal). To maintain the expected operation of the converter during steady-state, a maximum duty cycle can be imposed by the user on the converter design as shown in Equation 13.

$$D_{MAX} < 1 - (t_{off\_min} \times f_{SW}) \quad (13)$$

where:

- D_{MAX} is the recommended maximum converter duty cycle to avoid delayed turn-on in the next cycle
- t_{off_min} is the minimum off-time of the controller, with a maximum limit of 60ns
- f_{SW} is the converter switching frequency

8.3.12 Pulse Skipping

In order to prevent converter operational issues related to the minimum on-time of the controller during start-up and transient periods, specifically during high frequency operation, a pulse skipping mode has been implemented for the TPS7H502x controller. During this mode, the output will stop switching periodically. Having a minimum on-time that is too long in duration during high frequency operation can lead to an issue such as current runaway during the soft-start period. Pulse skipping allows for overcoming this issue by reducing the

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peak current during the start-up period. In high frequency converter designs where the V_{IN} to V_{OUT} ratio of the converter may lead to required duty cycles that are less than the minimum on-time, the controller output will skip pulses in order to maintain the required output voltage. Pulse skipping will occur when both of the following conditions are present:

- The voltage at the COMP pin is less than 0.3V at the rising edge of the system clock
- The previous duty cycle was less than 50%

Note that for the TPS7H5021, the duty cycle is always less than 50% so only the first condition is necessary to initiate the pulse skipping.

8.3.13 Leading Edge Blank Time

After OUT goes high, a leading edge blank time is implemented to prevent transients and noise on the sensed current waveform from being detected by the current sensing loop after the initial turn-on of the primary power switch. The leading edge blank time is fixed at 35ns (typical). An RC filter can also be used at the CS_ILIM pin to further remove any noise, provided that the cutoff frequency is sufficiently larger than the switching frequency of the converter. The general rule-of-thumb is that the target cutoff is 10× the switching frequency.

8.3.14 Current Sense and PWM Generation (CS_ILIM)

The CS_ILIM pin is driven by a signal representative of the main switch current of the power converter. The current signal has to have compatible input range of the COMP pin. As shown in Figure 8-9, the COMP pin voltage is used as the reference for the peak current. The output of the controller, OUT, is turned on by the internal clock signal and turned off when the peak of the sensed current signal reaches the COMP/CCSR pin voltage (which is approximately COMP/2). Note that this peak sensed current signal that is compared to COMP/CCSR at the PWM comparator contains an offset voltage of 150mV. The CS_ILIM pin is also used to configure the current limit for the controller. If slope compensation is implemented using the RSC pin, then the slope compensation ramp is subtracted from the COMP/CCSR signal, and turn-off of OUT occurs when the peak sensed current intersects the slope-compensated COMP/CCSR voltage. In instances which the user desires to bypass the internal error amplifier and drive COMP externally, the usable voltage range of the pin is approximately up to 2.3V. Since the CS_ILIM threshold for activating current limit is 1V and COMP is scaled down by CCSR, any external voltage applied to COMP that is greater than 2.3V is beyond the voltage to which the PWM comparator and feedback loop will react.

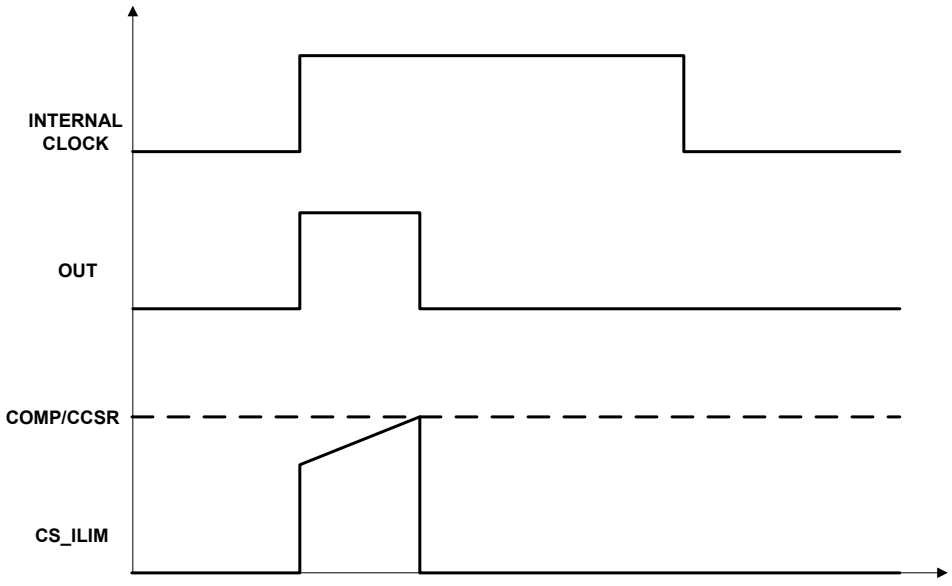

Figure 8-9. Peak Current Mode Control and PWM Generation

A resistor from CS_ILIM to AGND is used to detect current for both proper PWM operation and overcurrent protection. The current limit threshold V_{CS_ILIM}, is specified as 1V (nominal) in the electrical specifications. This

indicates that when the voltage on this pin reaches this threshold, the device will enter current limiting and turn off the output (OUT). Equation 14 shows the calculation for determining the value of the sense resistor for a selected current limit.

$$R_{CS} = \frac{V_{CS\_ILIM}}{I_{LIM}} \quad (14)$$

Note that the value of I_{LIM} has to account for where and how the current is being sensed. In the case of an isolated converter using primary-side control with the sense resistor between source of primary FET to AGND, I_{LIM} must be calculated appropriately with respect to the load current. Regardless of the topology, the user should ensure that there is sufficient margin between the peak current during normal operation and the overcurrent trip point when determining the value of R_{CS}.

8.3.15 Gate Driver Output

The TPS7H502x can be used to drive power semiconductor devices that require a gate voltage from 4.5V to 14V, making the controller acceptable for both silicon MOSFET and GaN FET based power converters. The gate driver stage has split outputs. These outputs are OUTH and OUTL, which are the sourcing and sinking outputs, respectively. These split outputs offer the flexibility to adjust the turn-on and turn-off speed independently by placing additional resistance to either the turn-on or turn-off path of the power device that is being driven. These outputs are capable of both sourcing and sinking 1.2A (typical) at 12V input on PVIN.

8.3.16 Unpowered Voltage Clamp

The TPS7H502x includes a voltage clamp on the gate driver output. This clamp is active only when VIN is less than approximately 2V. With low voltage on VIN, the internal OUTL driver is not adequately powered and thus is incapable of actively pulling the driver output low. This potentially leaves the driver output in a high-impedance state, and the unpowered voltage clamp was added to mitigate this issue. This unpowered clamp is only operational while the controller is disabled.

The bus voltage VBUS of the converter can begin to rise while the controller input VIN is low. Without a sufficiently low impedance between OUTL and PGND, the slew rate (dV/dt) of the bus voltage can cause an unintentional turn-on of the FET through the gate-drain capacitance C_{GD}. The induced current through C_{GD} can charge the gate-source capacitance C_{GS} above the gate-source threshold of the FET, enabling undesired current flow from VBUS to PGND. The unpowered voltage clamp limits the voltage at the gate of the FET until such time as the driver has sufficient voltage and the controller is enabled. The voltage clamp values can be viewed in the *Specifications* table. After the controller is enabled, the voltage clamp is deactivated and does not interfere with the normal operation of the controller and driver. Note that the criteria for deactivating the clamp are the same as those required for start-up of the device, as outlined in *Start-Up*. An external pull-down resistor can be used between OUT to PGND as a supplement to the unpowered voltage clamp to further mitigate issues related to unintentional turn-on. A pull-down resistor in the range of 10kΩ to 50kΩ is recommended, if used. Note that the addition of the external resistor slightly increases the quiescent and operating currents for the device, with a smaller resistor causing a larger increase in these currents.

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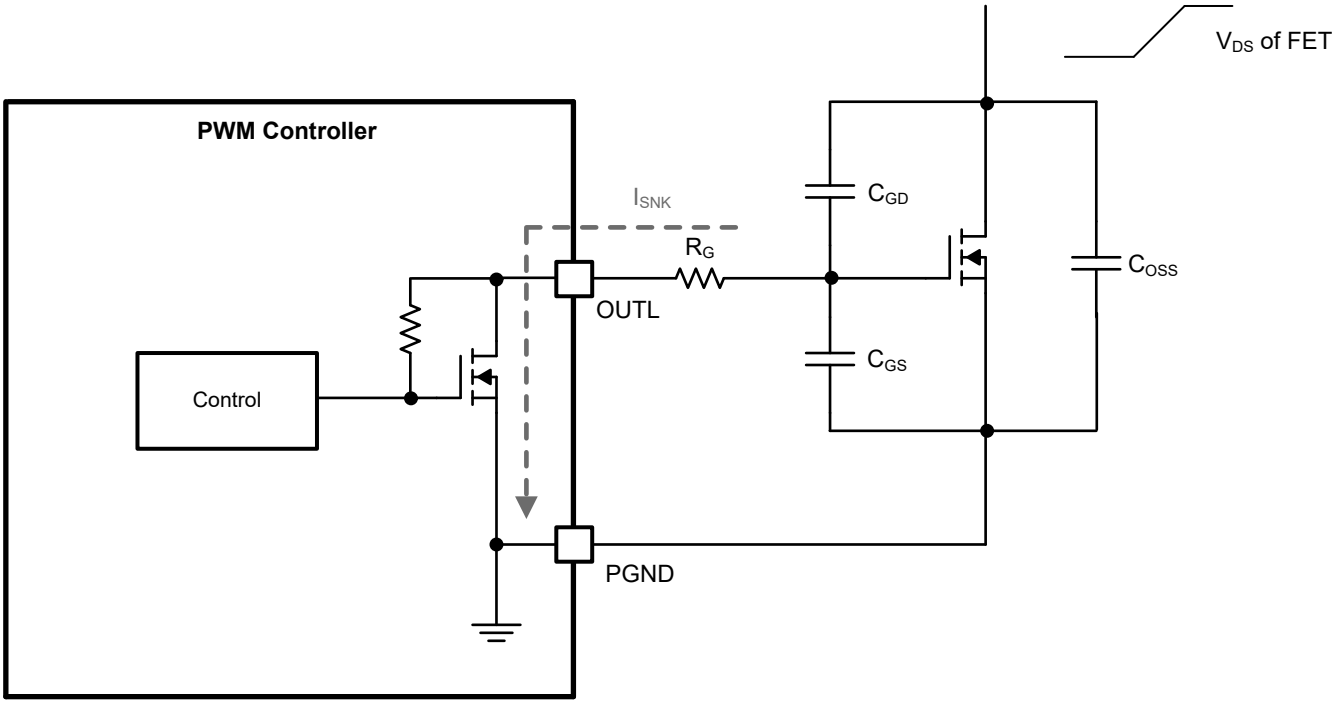

Figure 8-10. Unpowered Voltage Clamp

8.3.17 Sourcing Driver Return (OUTH_REF)

The return for the sourcing driver (OUTH) stage of the driver is pinned out to OUTH_REF so that a 220nF external capacitor can be connected during certain operating conditions. The voltage at OUTH_REF is nominally 6V less than that at PVIN. Allowing for an external capacitor connection between this pin and PVIN not only improves the transient performance of the driver, but also provides mitigation against radiation induced single-event transients (SETs). Note that the OUTH_REF capacitor is only needed when the external voltage applied at PVIN is greater than or equal to 6V. When PVIN is less than 6V, OUTH_REF can be directly connected to PGND.

Table 8-3. OUTH_REF Connections

DRIVER INPUT VOLTAGE	CONFIGURATION
PVIN < 6V	Connect OUTH_REF to PGND
PVIN ≥ 6V	Connect a 220nF capacitor between OUTH_REF and PVIN

8.3.18 Slope Compensation (RSC)

When utilizing peak current mode control in switching power converter design, the converter can enter into an unstable state when the duty cycle for the main power switch rises above 50%. Basically, the converter will be in a state where the error between the peak current and average current increases with each subsequent switching cycle. This instability, known as subharmonic oscillation, can be mitigated by adding slope compensation. For the TPS7H502x, the slope compensation is in the form of a voltage ramp that is subtracted from the error amplifier output divided down by the parameter CCSR (COMP to CS_ILIM ratio). The minimum slope compensation for stability over the entire duty cycle range is equal to 0.5 × *m*, where *m* is the inductor falling current slope. The recommended slope compensation is 1 × *m*, as any increase above this value will not improve stability.

For the forward converter and boost converter, the slope compensation can be set equal to the downward slope of the output inductor current. For the flyback converter, the slope compensation is calculated using the downward slope of the current in the flyback transformer. In the isolated topologies, note that the sensed current waveform would also need to take into account the turns ratio of the transformer.

For forward:

$$SC = \frac{V_{OUT} \times R_{CS} \times A_{CS}}{L_{OUT} \times N_{PS}} \quad (15)$$

For flyback:

$$SC = \frac{V_{OUT} \times R_{CS} \times A_{CS}}{L_{PRI} \times N_{PS}} \quad (16)$$

For boost:

$$SC = \frac{(V_{OUT} - V_{IN}) \times R_{CS} \times A_{CS}}{L} \quad (17)$$

where:

- SC is the slope compensation value in V/µs
- L_{OUT} is the output inductor value in µH (forward)
- L_{PRI} is the primary inductance value in µH (flyback)
- L is the inductor value in µH (boost)
- N_{PS} is the primary-to-secondary turns ratio
- R_{CS} is the value of the current sense resistor in Ω
- A_{CS} is the gain associated with the current sense stage, including the current sense amplifier and transformer, if used
- V_{OUT} is the converter output voltage
- V_{IN} is the converter input voltage

For the TPS7H502x controller, a resistor from the RSC pin to AGND can be used to set the desired slope compensation. Equation 18 shows the calculation for determining the proper resistor value for RSC.

$$RSC = \frac{29.5}{SC^{1.07}} \quad (18)$$

where:

- SC is the desired slope compensation is V/µs
- RSC is in kΩ

8.3.19 Frequency Compensation

Since the TPS7H502x uses a transconductance error amplifier (OTA), either Type 2A or Type 2B frequency compensation can be applied. The primary difference between the two compensation schemes is that Type 2A has an additional capacitor C_{HF} in parallel with R_{COMP} and C_{COMP} in order to provide high-frequency noise attenuation. These components will be connected between the COMP pin of the controller, which is the OTA output, and AGND.

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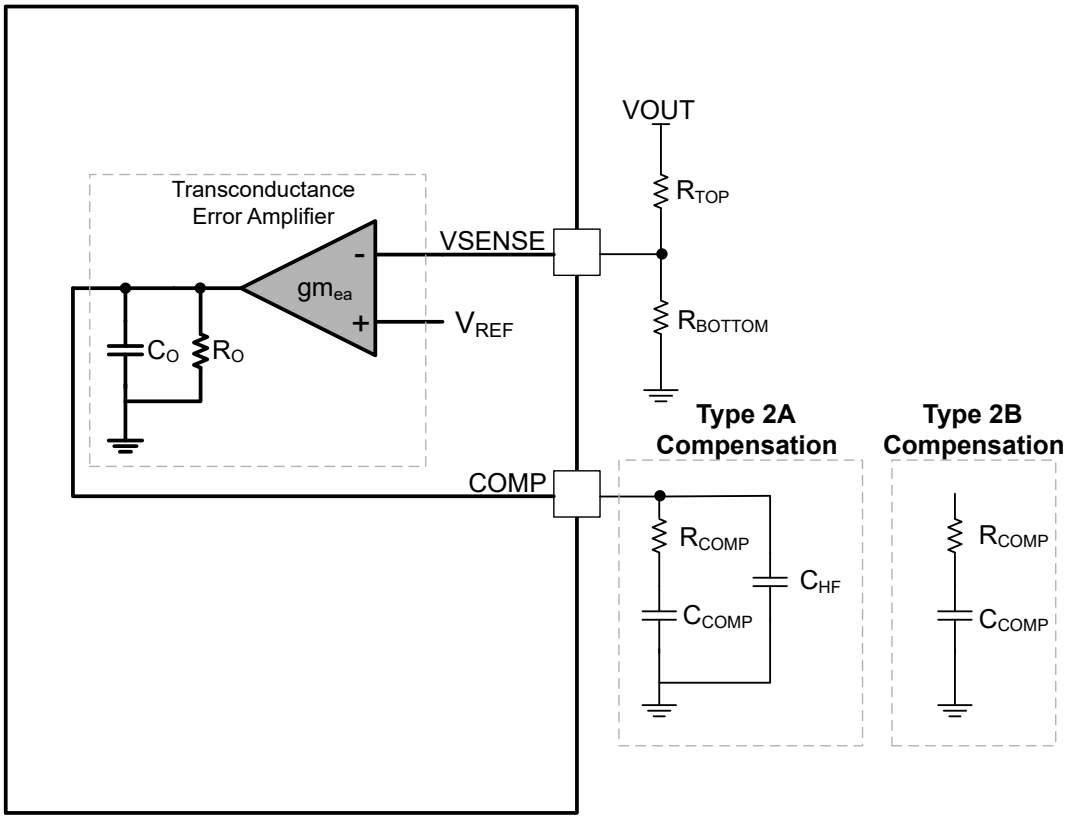

Figure 8-11. TPS7H502x Frequency Compensation Options

For the topologies supported by the TPS7H502x, the following procedure and equations can be used to select the compensation components. All parameters in the equations are in standard units unless otherwise indicated (that is, H for inductance, F for capacitance, Hz for frequency, and so on).

1. Select the desired crossover frequency (f_c) for the converter. Note that for boost and flyback converters, there is a right-half-plane (RHP) zero, which limits the target crossover frequency of the converter. For these topologies, the crossover should be between one-fourth to one-tenth of the RHP zero frequency. For the forward converter, the crossover frequency should be no more than one-tenth of the switching frequency.
2. Calculate the transconductance G_M of the power stage.
   - For the forward converter:

$$G_M = \frac{N_{PS}}{A_{CS} \times R_{CS}} \quad (19)$$

   - For the flyback converter:

$$G_M = \frac{(1 - D_{MAX}) \times N_{PS}}{A_{CS} \times R_{CS}} \quad (20)$$

   - For the boost converter:

$$G_M = \frac{(1 - D_{MAX})}{A_{CS} \times R_{CS}} \quad (21)$$

where:

- N_{PS} is the primary-to-secondary turns ratio of the transformer
- A_{CS} is the gain associated with the current sense stage
- R_{CS} is the current sense resistor value in Ω

- D_{MAX} is the maximum duty cycle for the application

3. Calculate the gain A_{VM} of the error amplifier network in order to achieve the target crossover frequency:

$$A_{VM} = \frac{2\pi \times f_C \times C_{OUT}}{G_M} \quad (22)$$

where:

- f_C is the target crossover frequency
- C_{OUT} is converter output capacitance
- G_M is the power stage transconductance

4. Calculate R_{COMP} based on the required gain A_{VM}, the error amplifier transconductance g_{mea}, and the feedback resistor values:

$$R_{COMP} = \frac{A_{VM}}{g_{mea} \times K_{FB}} \quad (23)$$

where:

$$K_{FB} = \frac{R_{BOTTOM}}{R_{BOTTOM} + R_{TOP}} \quad (24)$$

5. The zero of the error amplifier network should be set equal to approximately one-tenth of the target crossover frequency:

$$f_{ZEA} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} = \frac{f_C}{10} \quad (25)$$

therefore:

$$C_{COMP} = \frac{1}{2\pi \times (0.1 \times f_C) \times R_{COMP}} \quad (26)$$

6. Set the high frequency pole of the compensator. For the forward converter, this can be set equal to frequency of the ESR zero for the converter. For the boost and flyback, it should be set to the lower of the ESR zero and RHP zero.

$$f_{HF} = \frac{1}{2\pi \times R_{COMP} \times C_{HF}} = f_{Z\_ESR} \text{ or } f_{RHPZ} \quad (27)$$

therefore:

$$C_{HF} = \frac{1}{2\pi \times f_{Z\_ESR} \times R_{COMP}} \quad (28)$$

or:

$$C_{HF} = \frac{1}{2\pi \times f_{RHPZ} \times R_{COMP}} \quad (29)$$

Note that the procedure outlined is intended as a starting point for component selection. Frequency compensation is often an iterative process and the best values are typically obtained through hardware testing of the converter.

8.3.20 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 185°C (typical). The device reinitiates the power-up sequence when the junction temperature drops below 170°C (typical).

8.4 Device Functional Modes

The TPS7H502x series uses fixed frequency, peak current mode control. The controller regulates the peak current and duty cycle of the converter. The internal oscillator initiates the turn-on of the gate driver output for the power switch. The external power switch current is sensed through an external resistor and compared via

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internal comparator. The voltage generated at the COMP pin is stepped down via internal resistors. When the sensed current reaches the stepped down COMP voltage, the power switch is then turned off.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H502x is a radiation-hardness-assured PWM controller with an integrated gate driver. The driver has an input voltage range of 4.5V to 14V and offers a programmable switching frequency up to 1MHz. Furthermore, the integrated driver can be configured to operate with GaN FETs by utilizing the programmable LDO of the controller and making a connection from its output to PVIN. A higher voltage input up to 14V can be used at PVIN in order to use the driver in conjunction with silicon MOSFETs. The controller can support a number of different power supply topologies, including but not limited to: flyback, forward, and boost.

9.2 Typical Application

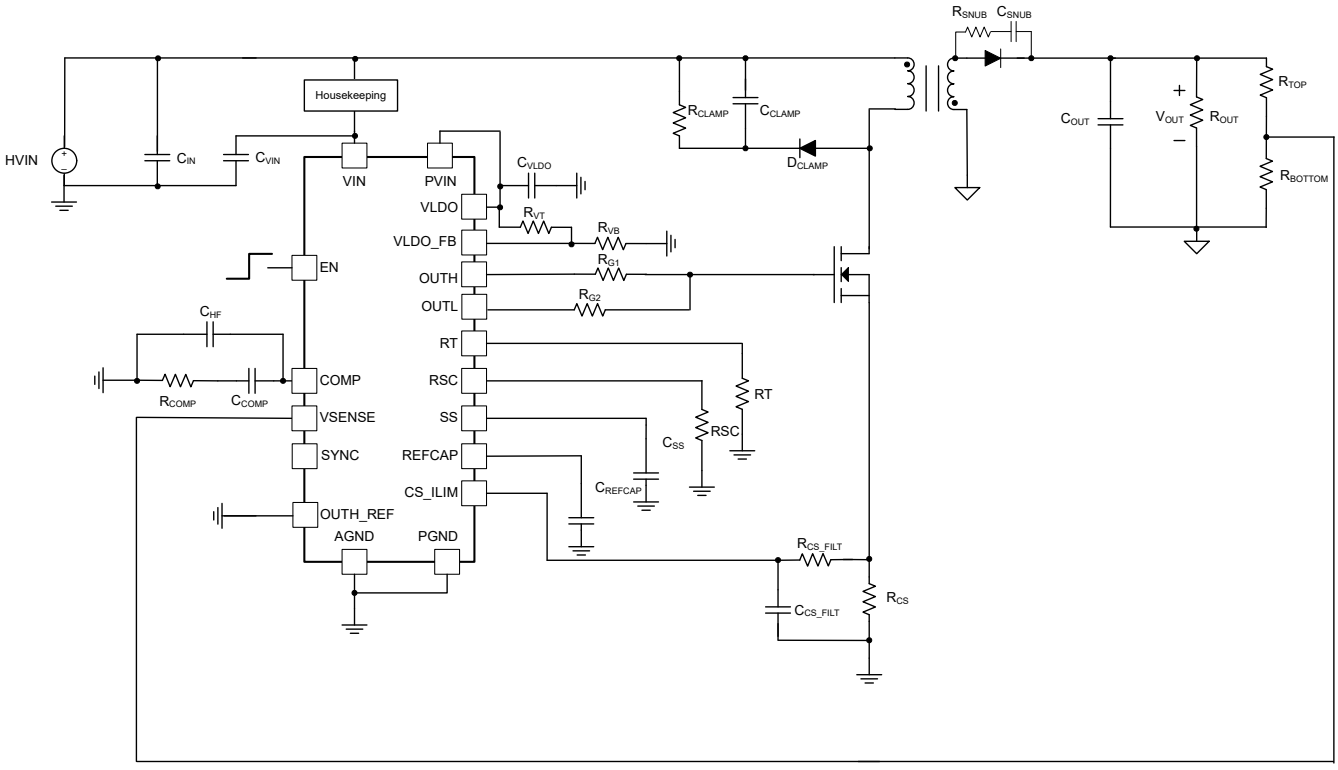

Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

The example provided details the design of a flyback converter using a GaN power semiconductor device as the primary switching FET. The intent is to show how to determine the component selection for the TPS7H5020 as well as key components of the converter power stage.

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Table 9-1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range	22V to 36V, 28V nominal
Output voltage	5V ±10%
Maximum output current	4A
Switching frequency	500kHz
Target bandwidth	~4kHz
Full load step (4A) transient response	≤ 375mV

9.2.2 Detailed Design Procedure

9.2.2.1 Switching Frequency

The flyback converter was designed to operate at a switching frequency of 500kHz. For space-grade converter designs, the benefits of GaN power devices over silicon counterparts are readily apparent at this switching frequency. Using Equation 30, the required RT resistor for the desired frequency can be determined. Note that the value of f_{SW} is in kHz and RT is giving in kΩ.

$$\mathrm{RT} = \frac{112390}{\mathrm{f_{SW}}} - 14.2 \tag{30}$$

$$\mathrm{RT} = \frac{112390}{500} - 14.2 = 210.5\mathrm{k\Omega} \tag{31}$$

A standard resistor value of 210kΩ is ideal for the design. A slightly lower value of 205kΩ was used due to availability.

9.2.2.2 Output Voltage Programming Resistor Selection

The converter has an output voltage of 5V. Select the feedback resistor divider connected to VSENSE to correspond to the desired V_{OUT}. With a resistor of 10kΩ selected for R_{TOP}, the value of the bottom resistor in the divider can be calculated.

$$\mathrm{R_{BOTTOM}} = \frac{\mathrm{V_{REF}}}{\mathrm{V_{OUT} - V_{REF}}} \times \mathrm{R_{TOP}} \tag{32}$$

$$\mathrm{R_{BOTTOM}} = \frac{0.6\mathrm{V}}{5\mathrm{V} - 0.6\mathrm{V}} \times 10\mathrm{k\Omega} = 1.36\mathrm{k\Omega} \tag{33}$$

The values for R_{TOP} and R_{BOTTOM} needed are 10kΩ and 1.37kΩ, respectively.

9.2.2.3 Driver PVIN Configuration

For the design example, the intended power semiconductor device is a GaN FET. As such, VLDO will be connected to PVIN of the driver. VLDO can be programmed from 4.5V to 5.5V, and in this instance a nominal drive voltage of 5V is selected. In order to program VLDO for 5V operation, Equation 34 is used to select the proper resistor between VLDO_FB and GND.

$$\mathrm{R_{VB}} = \frac{\mathrm{V_{REFCAP}}}{\mathrm{V_{LDO} - V_{REFCAP}}} \times \mathrm{R_{VT}} \tag{34}$$

$$\mathrm{R_{VB}} = \frac{1.225\mathrm{V}}{5\mathrm{V} - 1.225\mathrm{V}} \times 10\mathrm{k\Omega} = 3245\Omega \tag{35}$$

The value of R_{VB} is selected as 3.24kΩ. Since PVIN is connected to VLDO and less than 6V, OUTH_REF should be connected directly to GND per Table 8-3.

9.2.2.4 Soft-Start Capacitor Selection

The soft-start time was chosen to be sufficiently long to limit inrush current for this design. The value of the soft-start capacitor selected was 33nF. Based on this value, the soft-start time can be calculated.

$$t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \tag{36}$$

$$t_{SS} = \frac{33nF \times 0.6V}{2.8\mu A} = 7.07ms \tag{37}$$

The soft-start time is approximately 7.1ms for the design.

9.2.2.5 Transformer Design

The turns ratio and primary inductance of the transformer are determined based on the target specifications of the converter. The turns ratio is calculated based on a maximum duty cycle of 35% targeted for the design.

$$N_{PS\_MAX} = \frac{V_{IN\_MIN} \times D_{MAX}}{(V_{OUT} + V_D) \times (1 - D_{MAX})} \tag{38}$$

$$N_{PS\_MAX} = \frac{22V \times 0.35}{(5V + 0.7) \times (1 - 0.35)} = 2.08 \tag{39}$$

A turns ratio of 2 is selected for the design. Based on the actual turns ratio, the minimum and maximum duty cycle can be calculated.

$$D_{MIN} = \frac{(V_{OUT} + V_D) \times N_{PS}}{(V_{OUT} + V_D) \times N_{PS} + V_{IN\_MAX}} \tag{40}$$

$$D_{MIN} = \frac{(5V + 0.7V) \times 2}{(5V + 0.7V) \times 2 + 22V} = 0.241 \tag{41}$$

$$D_{MAX} = \frac{(V_{OUT} + V_D) \times N_{PS}}{(V_{OUT} + V_D) \times N_{PS} + V_{IN\_MIN}} \tag{42}$$

$$D_{MAX} = \frac{(5V + 0.7V) \times 2}{(5V + 0.7V) \times 2 + 22V} = 0.341 \tag{43}$$

The primary inductance was calculated based on a 20% current ripple.

$$L_P = \frac{V_{IN\_MAX}{}^2 \times D_{MIN}{}^2}{V_{OUT} \times I_{OUT} \times f_{SW} \times \%_{RIPPLE}} \tag{44}$$

$$L_P = \frac{36V^2 \times 0.24^2}{5V \times 4A \times 500kHz \times 0.2} = 37.3\mu H \tag{45}$$

The primary inductance selected for the actual design was 30µH, which results in an actual ripple of approximately 25%. The following equations detail how to calculate transformer primary and secondary currents that are critical for proper design of the transformer. These equations are useful for defining the physical structure of the transformer.

$$I_{RIPPLE} = \frac{V_{OUT} \times I_{OUT} \times \%_{RIPPLE}}{V_{IN\_MAX} \times D_{MIN}} \tag{46}$$

$$I_{RIPPLE} = \frac{5V \times 4A \times 0.25}{36V \times 0.24} = 0.58A \tag{47}$$

$$I_{PRI\_PEAK} = \frac{V_{OUT} \times I_{OUT}}{V_{IN\_MIN} \times D_{MAX} \times \eta} + \frac{I_{RIPPLE}}{2} \tag{48}$$

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$$I_{PRI\_PEAK} = \frac{5V \times 4A}{22V \times 0.35 \times 0.85} + \frac{0.58A}{2} = 3.35A \quad (49)$$

$$I_{PRI\_RMS} = \sqrt{D_{MAX} \times \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN\_MIN} \times D_{MAX}}\right)^2 + \frac{I_{RIPPLE}^2}{3}} \quad (50)$$

$$I_{PRI\_RMS} = \sqrt{0.35 \times \left(\frac{5V \times 4A}{22V \times 0.35}\right)^2 + \frac{0.58A^2}{3}} = 1.57A \quad (51)$$

$$I_{SEC\_RMS} = \sqrt{(1 - D_{MAX}) \times I_{OUT}^2 + \frac{(I_{RIPPLE} \times N_{PS})^2}{3}} \quad (52)$$

$$I_{SEC\_RMS} = \sqrt{(1 - 0.35) \times 4A^2 + \frac{(0.58A \times 2)^2}{3}} = 3.29A \quad (53)$$

9.2.2.6 Primary Power Switch Selection

In the flyback topology, the maximum voltage that can be applied at the drain of the FET is calculated according to Equation 54.

$$V_{DS} = (V_{IN\_MAX} + V_L) + N_{PS} \times (V_{OUT} + V_D) \quad (54)$$

$$V_{DS} = (36V + 12V) + 2 \times (5V + 0.7V) = 59.4V \quad (55)$$

At a minimum, a 60V rated FET is needed for the application. Practically, a FET with a higher voltage rating needs to be selected to allow for transient spikes and ringing. Furthermore, the current rating of the FET needs to be higher than the primary currents that were calculated in *Transformer Design*. The selected GaN device has a voltage rating of 200V, with a 22A current rating.

9.2.2.7 Output Diode Selection

The maximum voltage stress experienced by the diode on the secondary side can be calculated using Equation 56.

$$V_{D\_STRESS} = V_{OUT} + \frac{V_{IN\_MAX}}{N_{PS}} \quad (56)$$

$$V_{D\_STRESS} = 5V + \frac{36V}{2} = 23V \quad (57)$$

The maximum expected voltage is 23V, but a higher rating needs to be selected to provide margin by allowing for transient voltage spikes. Note that an RC snubber across the output diode is potentially required depending on the extent and magnitude of the ringing across the power diode at turn-off. The current rating of the diode needs to be sufficient to handle the maximum load current of the converter. The diode was selected to have ratings of 80V and 15A to provide significant margin above the maximum operating conditions.

9.2.2.8 RCD Clamp

Since the leakage inductance and parasitic capacitances in the converter and printed circuit board can create excessive ringing at the drain of the FET which can ultimately prove problematic, a RCD clamp is used to sufficiently dampen the magnitude and frequency of the ringing to well within the selected voltage rating of the FET.

Generally, these values are optimized during testing since the ringing is highly dependent on the printed circuit board parasitics. However, as a starting point, the following equations can be used to determine the value of the clamping resistor and capacitor, R_{CLAMP} and C_{CLAMP}, respectively, based on the desired allowable overshoot.

$$V_{CLAMP} = K_{CLAMP} \times N_{PS} \times (V_{OUT} + V_D) \quad (58)$$

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The parameter K_{CLAMP} defines the target overshoot value. For example, set K_{CLAMP} to 1.5 for 50% allowable overshoot.

Next, the leakage inductance $L_{LEAKAGE}$ and peak primary current I_{PRI_PEAK} of the transformer can be used to approximate the clamp resistor. The clamp capacitor value can be determined thereafter. Note that ΔV_{CLAMP} defines the allowable ripple for the clamp capacitor as a percentage of the desired clamp voltage. For example, for 2% ripple set ΔV_{CLAMP} to 0.02.

$$R_{CLAMP} = \frac{{V_{CLAMP}}^2}{\frac{1}{2} \times L_{LEAKAGE} \times {I_{PRI\_PEAK}}^2 \times \frac{V_{CLAMP}}{V_{CLAMP} - N_{PS} \times (V_{OUT} + V_D)} \times f_{SW}} \quad (59)$$

$$C_{CLAMP} = \frac{1}{\Delta V_{CLAMP} \times V_{CLAMP} \times R_{CLAMP} \times f_{SW}} \quad (60)$$

9.2.2.9 Output Capacitance Selection

Generally, there are two different calculations that can be used to determine the output capacitance required for the converter. The first, shown in Equation 61 , determines the amount of output capacitance that is needed to meet the output voltage ripple requirements of the design. The first calculates the amount of capacitance required to meet the maximum allowable voltage deviation at the output in response to a worst-case load transient as shown in Equation 63. Once the two calculations are performed, the maximum of these should be chosen as the output capacitance for the design. The calculations are shown for target voltage ripple of 2% of the output voltage and maximum allowable voltage deviation of 7.5% of the output voltage.

$$C_{OUT} > \frac{I_{OUT} \times D_{MAX}}{V_{RIPPLE} \times f_{SW}} \quad (61)$$

$$C_{OUT} > \frac{4A \times 0.35}{100mV \times 500kHz} = 28\mu F \quad (62)$$

$$C_{OUT} > \frac{\Delta I_{STEP}}{2\pi \times \Delta V_{OUT} \times f_C} \quad (63)$$

$$C_{OUT} > \frac{4A}{2\pi \times 375mV \times 4kHz} = 424.4\mu F \quad (64)$$

Based on the calculations, at least 425µF of output capacitance is required. When selecting capacitors, consider any derating of capacitance that is needed to account for aging, temperature, and DC bias.

For space-grade converter designs, there is another consideration when selecting the output capacitance. This is the impact of radiation induced single event transients (SET). Single energetic particle strikes can lead to momentary variation in the PWM variation of the controller, which in turn can lead to output voltage transients in the converter. Thus, even though the value above provides a minimum value to account for voltage ripple and/or load transients, additional capacitance is likely needed for adequate SET mitigation. For the design example, approximately 470µF of total output capacitance was used.

An additional output filter can be used to further reduce the noise of the output stage if deemed necessary. This output filter consists of an additional inductor and a small amount of ceramic capacitance. The filter inductance is then located between the added ceramic capacitance and the bulk output capacitance that was determined to be required for the design. This approach can drastically reduce the output voltage ripple without significantly increasing the size and/or number of components required. The key for the secondary filter design is to choose the resonant frequency such that it is higher than the targeted crossover frequency yet well below the switching frequency and ESR zero of the bulk output capacitance. Equation 65, Equation 66, and Equation 67 can be used to determine the ESR zero as well as the resonant frequency and attenuation of the additional output filter.

$$f_{resonant} = \frac{1}{2\pi \times L_f \times C_{OUT\_BULK}} \quad (65)$$

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$$f_{zero} = \frac{1}{2\pi \times C_{OUT\_BULK} \times ESR_{BULK}} \quad (66)$$

$$Att_{fsw} = 40\log_{10}\left(\frac{f_{sw}}{f_{resonant}}\right) - 20\log10\left(\frac{f_{sw}}{f_{zero}}\right) \quad (67)$$

In the event that there is peaking at high frequencies due to the output filter, a resistor can be used to dampen this peaking effect. Equation 68 and Equation 69 can be used to determine the frequency of the peaking and the value of the resistor needed to provide adequate damping.

$$\omega_o = \frac{2 \times \left(C_{OUT\_CER} + C_{OUT\_BULK}\right)}{L_f \times C_{OUT\_CER} \times C_{OUT\_BULK}} \quad (68)$$

$$R_f = \frac{R_{OUT} \times L_f \times \left(C_{OUT\_CER} + C_{OUT\_BULK}\right) - \frac{L_f}{\omega_o}}{\frac{R_{OUT} \times \left(C_{OUT\_CER} + C_{OUT\_BULK}\right)}{\omega_o} - \left(L_f \times C_{OUT\_CER}\right)} \quad (69)$$

9.2.2.10 Current Sense Resistor

There are considerations and tradeoffs that can be made when selecting the current sense resistor that is connected between CS_ILIM and GND. Generally, the resistor is simply selected such that the converter will enter into cycle-by-cycle limiting at a selected maximum current. For example, if the sense resistor was chosen such that the overcurrent protection activates 125% of the maximum load current, this equates to 5A in this particular design. Using Equation 48, the corresponding peak primary current would be roughly 4.1A. The corresponding value of R_{CS} could be found based on the following equation, where V_{CS_ILIM} is the current limit threshold of the controller:

$$R_{CS} = \frac{V_{CS\_ILIM}}{I_{LIM}} \quad (70)$$

It is important to note that in instances where the sense resistor is connected between the source of the primary FET and ground, that the voltage across the sense resistor can subtract from the total gate-source voltage that is applied to the FET. This is the case when the driver is also referenced to ground rather than the source of the FET. As such, when driving GaN FETs, the user must be mindful of the voltage drop across the sense resistor. When using the controller to drive GaN devices with PVIN connected to VLDO, the programmable VLDO output can be set to a higher voltage, resulting in a larger V_{GS} applied to the FET that compensates for the sense resistor voltage. If the risk of overcurrent is low, then the sense resistor can also be made small in order to minimize the R_{CS} voltage. For this design, the sense resistor was selected to be 100mΩ. This corresponds to a I_{LIM} value of approximately 10A in the primary GaN FET.

Although the controller does have leading edge blanking to reduce the likelihood of incorrect PWM or current operation due to noise spikes at FET turn-on, a low-pass RC filter is needed to further remove noise from the sensed current signal. It is recommended that the cutoff frequency of the filter be at least a decade above the selected switching frequency.

9.2.2.11 Frequency Compensation Component Selection

The poles and zeros of the flyback converter can be determined with the following equations. Note that the flyback converter also has a right-half-plane zero.

$$f_{Z\_ESR} = \frac{1 + D_{MAX}}{2\pi \times C_{OUT} \times R_{ESR}} \quad (71)$$

$$f_{Z\_ESR} = \frac{1 + 0.35}{2\pi \times 470\mu F \times 4m\Omega} = 114.3kHz \quad (72)$$

$$f_P = \frac{1}{2\pi \times C_{OUT} \times \frac{V_{OUT}}{I_{OUT}}} \quad (73)$$

$$f_P = \frac{1}{2\pi \times 470\mu F \times \frac{5V}{4A}} = 270.9Hz \quad (74)$$

$$f_{RHPZ} = \frac{\frac{V_{OUT}}{I_{OUT}} \times (1 - D_{MAX})^2}{2\pi \times \frac{L_{PRI}}{N_{PS}^2} \times D_{MAX}} \quad (75)$$

$$f_{RHPZ} = \frac{\frac{5V}{4A} \times (1 - 0.35)^2}{2\pi \times \frac{30\mu H}{2^2} \times 0.35} = 32.0kHz \quad (76)$$

Type 2A compensation network can be utilized in order to properly place the pole and zero of the error amplifier to achieve stability. Note that this compensation technique is for a flyback operating in continuous conduction mode. The crossover frequency is typically targeted to be anywhere from one-fourth of the RHP zero frequency to a full decade below. A crossover frequency of 4kHz was targeted for this design. The error amplifier network gain is set to achieve the target crossover frequency, which is dependent on R_{COMP}. The equation for R_{COMP}, as derived from Equation 20, Equation 22, and Equation 23, is shown in Equation 77. The calculation of K_{FB} is as shown in Equation 24.

$$R_{COMP} = \frac{2\pi \times f_C \times C_{OUT} \times A_{CS} \times R_{CS}}{(1 - D_{MAX}) \times N_{PS} \times K_{FB} \times g_m} \quad (77)$$

$$R_{COMP} = \frac{2\pi \times 4kHz \times 470\mu F \times 1 \times 0.1\Omega}{(1 - 0.35) \times 2 \times 0.12 \times 1750\frac{\mu A}{V}} = 4326.88\Omega \quad (78)$$

The error amplifer zero is set to one-tenth of the crossover frequency, which allows for selecting the value of C_{COMP}.

$$C_{COMP} = \frac{1}{2\pi \times (0.1 \times f_C) \times R_{COMP}} \quad (79)$$

$$C_{COMP} = \frac{1}{2\pi \times (0.1 \times 4kHz) \times 4.32k\Omega} = 91.96nF \quad (80)$$

Lastly, the high frequency pole is set to the lower of the ESR zero and the RHP zero. In this specific case, the RHP zero is lower.

$$C_{HF} = \frac{1}{2\pi \times f_{RHPZ} \times R_{COMP}} \quad (81)$$

$$C_{HF} = \frac{1}{2\pi \times 32kHz \times 4.32k\Omega} = 1.15nF \quad (82)$$

Using standard component values, the initial values of R_{COMP}, C_{COMP}, and C_{HF} selected were 4.32 kΩ, 100nF, and 1nF, respectively. It is important to note that these calculated values provide a starting point. The frequency compensation is often tuned during both simulation and testing in order to settle on the final compensation values of the design.

ADVANCE INFORMATION

9.2.3 Application Curves

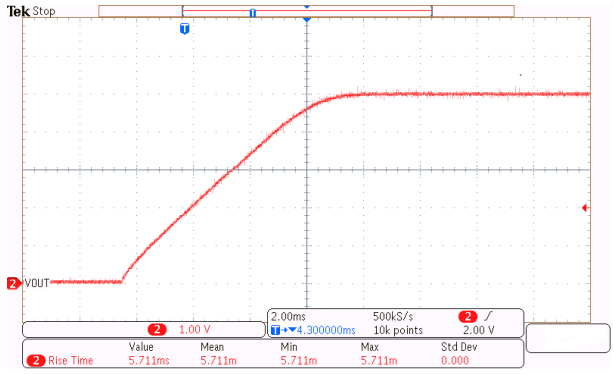

Figure 9-2. V_{OUT} Startup of Flyback Converter

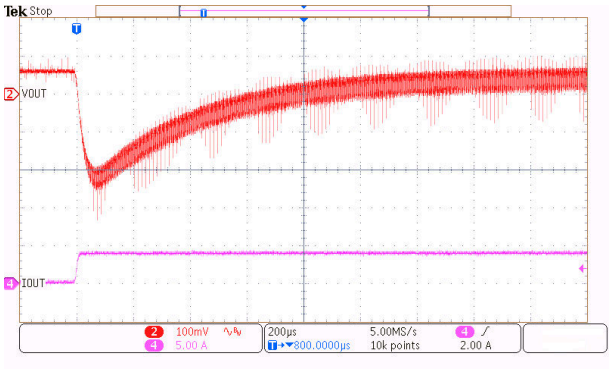

Figure 9-3. 4A Load Step Response for Flyback Converter

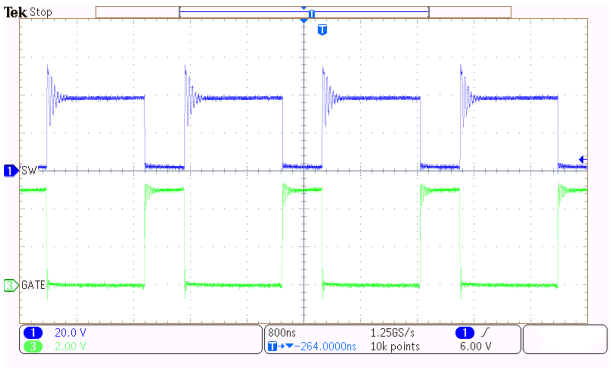

Figure 9-4. Gate and Switch Node Signal

9.3 Power Supply Recommendations

The TPS7H502x-SP controllers are designed to operate from an input voltage supply range between 4.5V and 14V. The input voltage supply for the controller should be well regulated and properly bypassed for best electrical performance. A minimum input bypass capacitor of 0.1µF is required from VIN to GND, but additional capacitance can be used to help improve the noise and radiation performance of the controller. It is recommended to use ceramic capacitors (X7R or better) for bypassing, and these capacitors should be placed as close as possible to the controller with a low impedance path to GND. Additional bulk capacitors should be used if the input supply is more than a few inches from TPS7H502x-SP controller.

The PVIN supply also is designed to operate from an input supply range between 4.5V and 14V. PVIN can be tied to VIN, tied to VLDO, or connected to another user generated voltage rail. A minimum bypass capacitor of 1µF is recommended here. In instances, where PVIN is tied to VLDO, the total bypass capacitance must not exceed 4.7µF.

9.4 Layout

9.4.1 Layout Guidelines

In order to increase the reliability of the converter design using the TPS7H502x series, the following layout guidelines should be followed.

- Route the feedback trace as far away as possible from power magnetics components (inductor and/or power transformer) and other noise inducting traces on the printed circuit board (PCB) such as the switch node. If the feedback trace is routed beneath the power magnetic component, ensure that this trace is on another layer of the PCB with at least one ground layer separating the trace from the inductor or transformer.

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- Minimize the copper area of the converter switch node for the best noise performance and reduction of parasitic capacitance to reduce switching losses. Ensure that any noise sensitive signals, such as the feedback trace, are routed away from this node as it contains a high dv/dt switching signal.
- All high di/dt and dv/dt switching loops in the power stage should have the paths minimized. This will help to reduce EMI, lower stresses on the power devices, and reduce any noise coupling into the control loop.
- Keep the analog ground of the controller separate from the power ground of the power stage that contains high frequency, high di/dt currents. These two grounds should be connected at a single point in the PCB layout. The sources of power semiconductor switches, the returns for bulk input capacitors of the power stage, and the ouput capacitor return should all be connected to the PCB power ground.
- All high current traces on the PCB should be short, direct, and as wide as possible. A good rule is to make the traces a minimum of 15mils (0.381mm) per ampere.
- Place all filtering and bypass capacitors for VIN, PVIN, REFCAP, and VLDO as close as possible to the controller. Surface mount ceramic capacitors with lower ESR and ESL are recommended as these reduce the potential for noise coupling compared to through-hole capacitors. Care should be taken to minimize the loop area formed by the bypass capacitor connection, the respective pin, and GND. Each bypass capacitor should have a good, low impedance connection to GND.
- External compensation components should be placed near the COMP pin of the controller. Surface mount components are recommended here as well.
- Attempt to keep the resistor divider used to generate the voltage at VSENSE close to the device in order to reduce noise coupling. Minimize stray capacitance to the VSENSE pin.
- OUTH and OUTL are used to drive the gates of power semiconductor devices. The PCB traces connected to these pins carry high dv/dt signals. Reduce noise coupling by routing these PCB traces away from any traces connected to VSENSE, COMP, RT, and CS_ILIM.
- Use short, low-inductance traces to connect OUTH and OUTL, the gate resistors, and the gate of the power semiconductor device being driven. The FET should be placed as close to the controller as is feasible.
- To prevent excessive ringing on the input power bus, good decoupling practices are required by placing low-ESR capacitors adjacent to the MOSFET or GaN FET.
- In addition to utilizing the leading edge blank time of the controller, RC filtering may be required for the sensed current signal input to CS_ILIM. Keep the resistor and capacitor in close vicinity to CS_ILIM to filter any ringing and/or spikes that may be present on the sensed current signal.
- Connect the thermal pad to the ground plane of the PCB using multiple vias. It is recommended to avoid putting solder paste directly on top of the vias unless these vias are tented or filled.

9.4.2 Layout Example

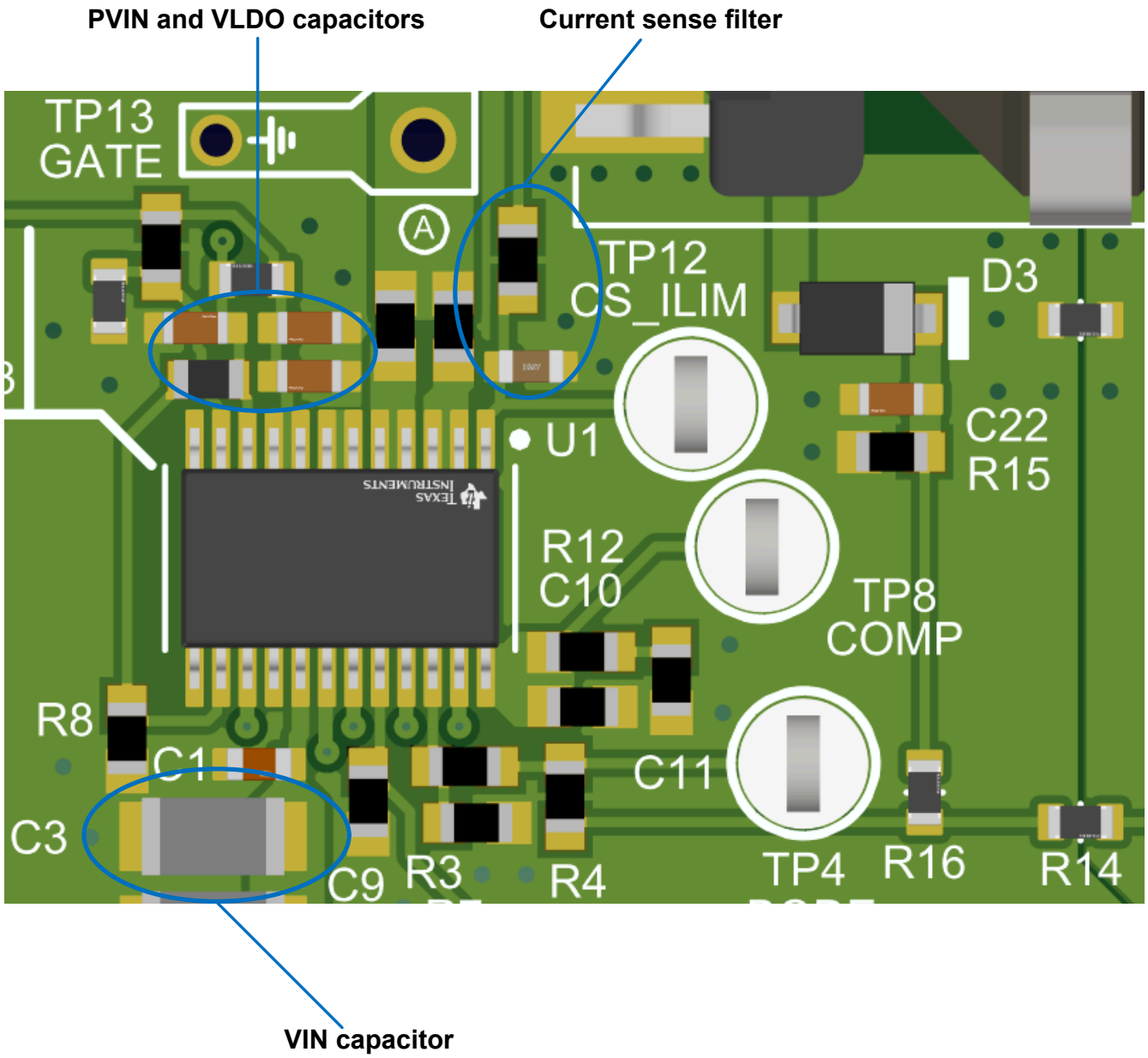


Figure 9-5. 3D Layout View From TPS7H5020FLYEVM

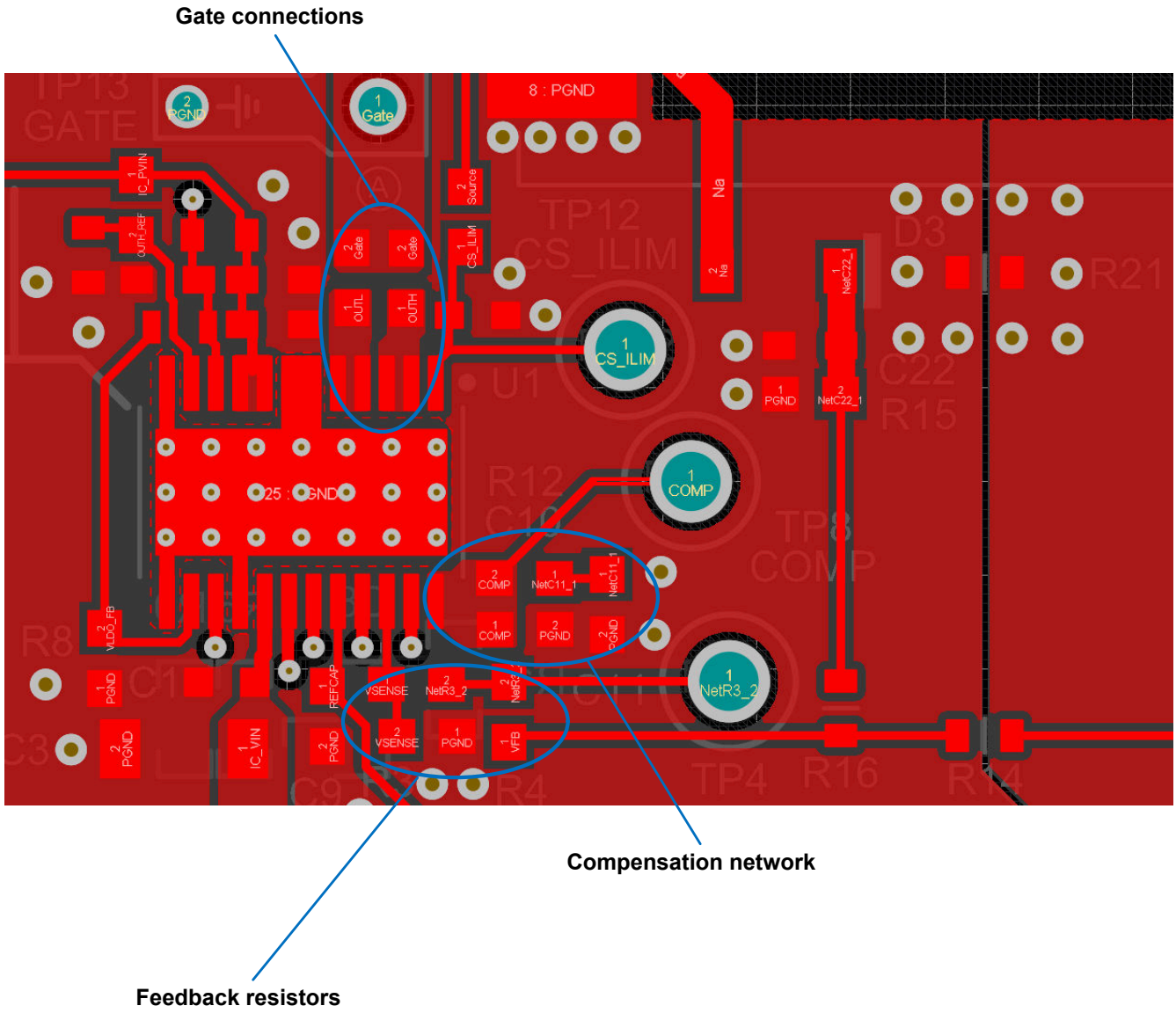


Figure 9-6. Top Layer Layout View From TPS7H5020FLYEVM

ADVANCE INFORMATION

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H5020EVM Evaluation Module* user's guide
- Texas Instruments, *TPS7H5020-SEP Preliminary Total Ionizing Dose (TID)* radiation report

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2025	*	Initial Release

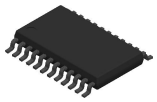
ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

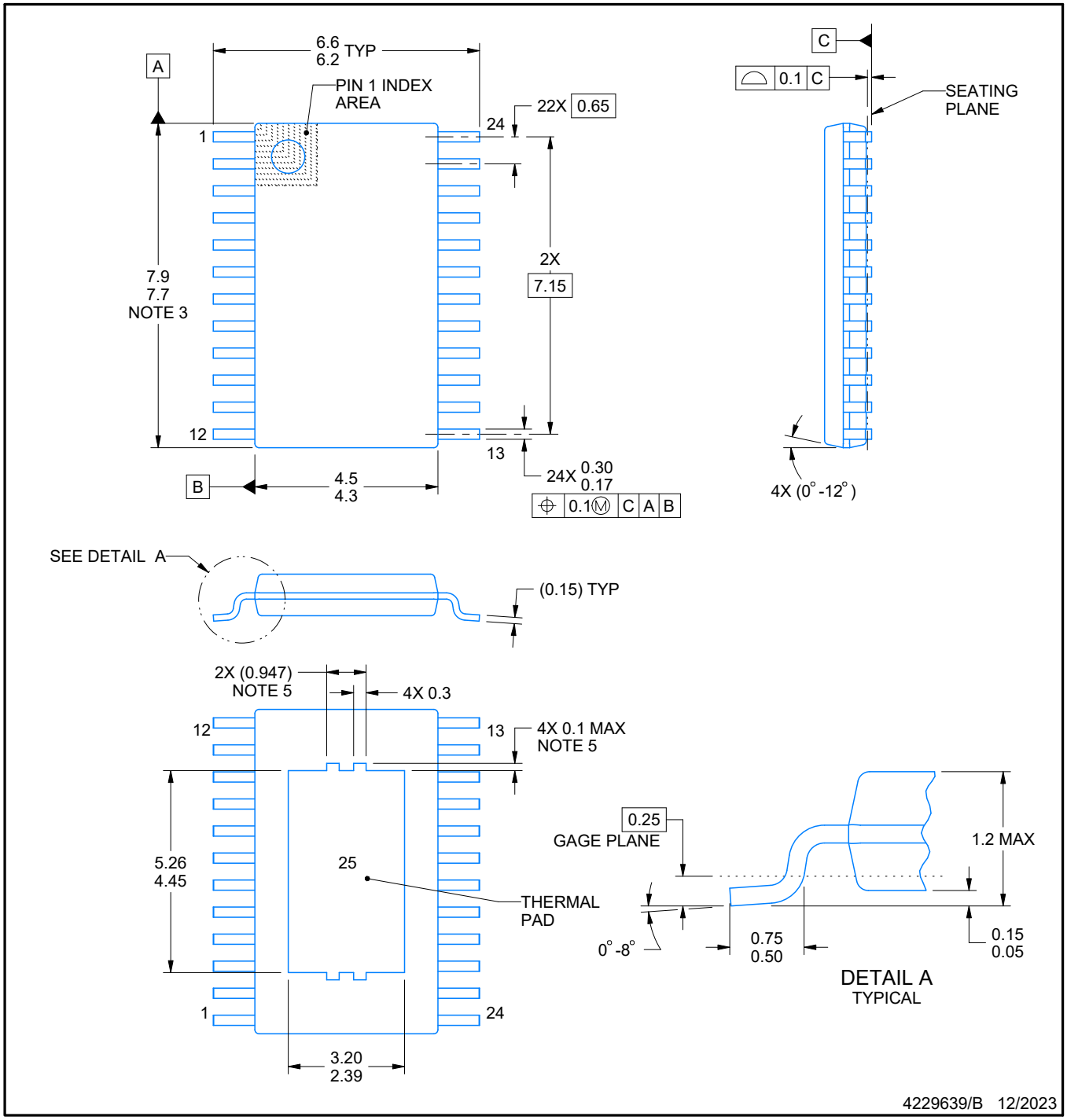
PACKAGE OUTLINE

PWP0024R



PowerPAD™ TSSOP - 1.2 mm max height

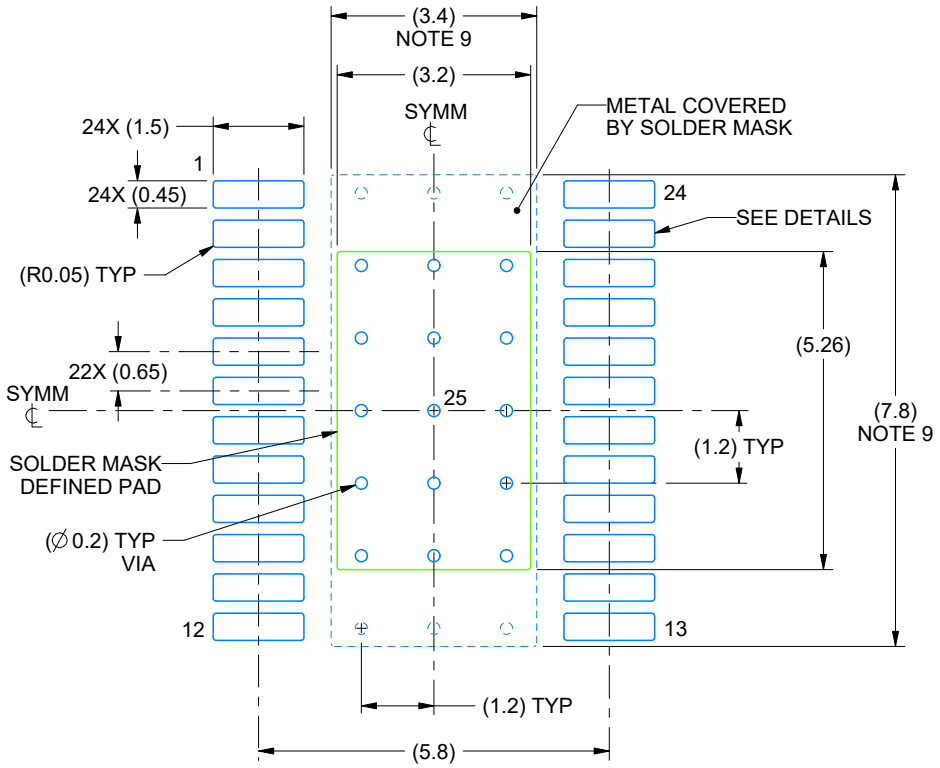
SMALL OUTLINE PACKAGE



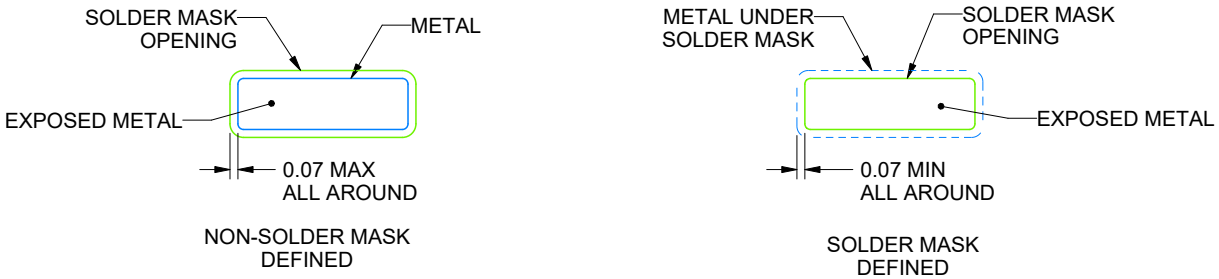
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

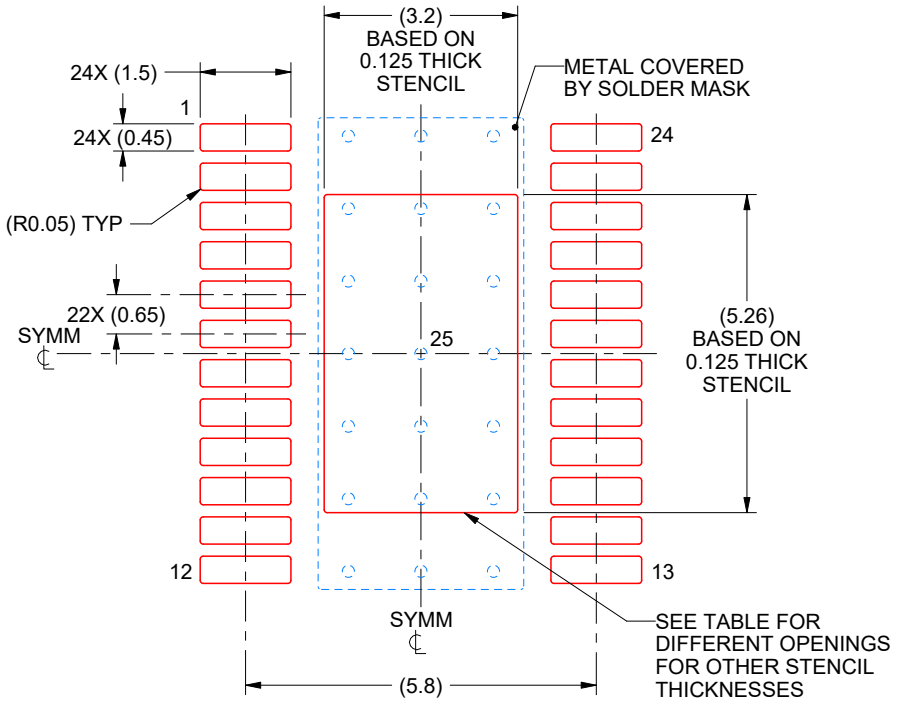


SOLDER MASK DETAILS

4229639/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.58 X 5.88
0.125	3.20 X 5.26 (SHOWN)
0.15	2.92 X 4.80
0.175	2.70 X 4.45

4229639/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS7H5020PWPTSEP	Active	Preproduction	HTSSOP (PWP) | 24	250 | SMALL T&R	-	Call TI	Call TI	-55 to 125	
PTPS7H5020PWPTSEP.A	Active	Preproduction	HTSSOP (PWP) | 24	250 | SMALL T&R	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

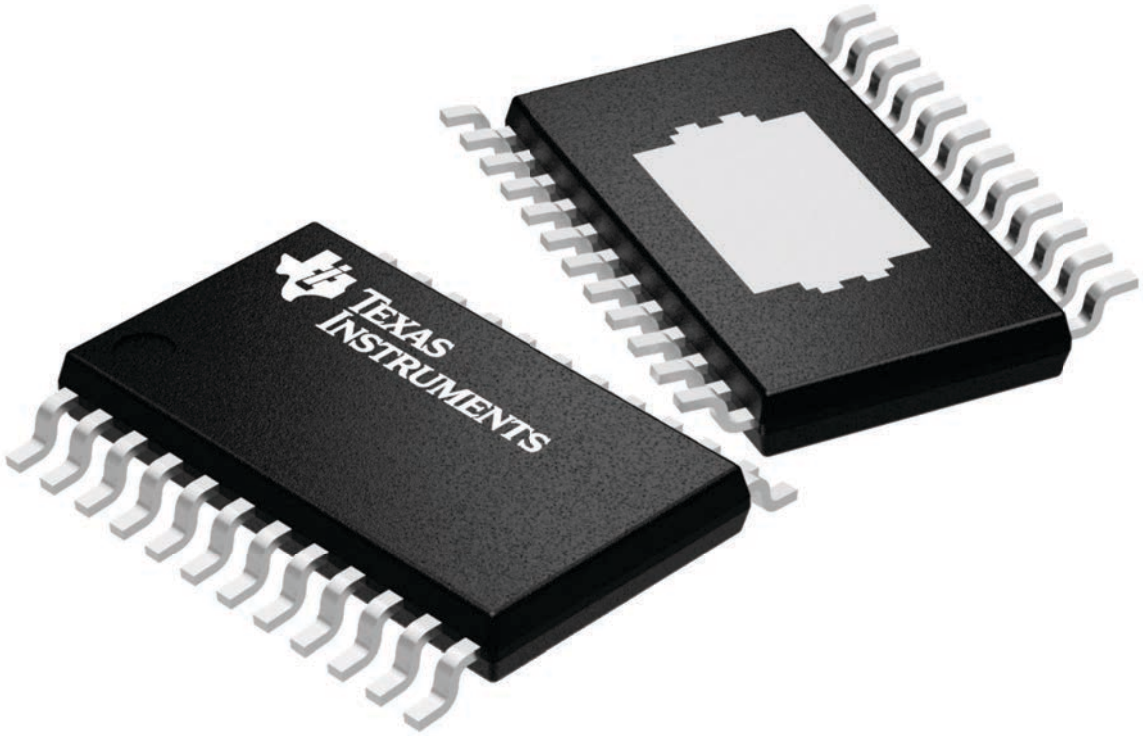
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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