MSP430i204x, MSP430i203x, MSP430i202x Mixed-Signal Microcontrollers

1 Features

- Supply voltage range: 2.2 V to 3.6 V
- High-performance analog
  - MSP430i204x: Four 24-bit sigma-delta analog-to-digital converters (ADCs) with differential PGA inputs
  - MSP430I203x: Three 24-bit sigma-delta analog-to-digital converters (ADCs) with differential PGA inputs
  - MSP430I202x: Two 24-bit sigma-delta analog-to-digital converters (ADCs) with differential PGA inputs
- Ultra-low power consumption
  - Active mode (AM):
    All system clocks active
    275 µA/MHz at 16.384-MHz, 3.0 V, flash program execution (typical)
  - Standby mode (LPM3):
    Watchdog timer active, full RAM retention
    210 µA at 3.0 V (typical)
  - Off mode (LPM4):
    Full RAM retention
    70 µA at 3.0 V (typical)
  - Shutdown mode (LPM4.5):
    75 nA at 3.0 V (typical)
- Intelligent digital peripherals
  - Two 16-bit timers with three capture/compare registers each
  - Hardware multiplier supports 16-bit operations
- Enhanced universal serial communication interfaces (eUSCIs)
  - eUSCI_A0
    - Enhanced UART with automatic baud-rate detection
    - IrDA encoder and decoder
    - Synchronous SPI
  - eUSCI_B0
    - Synchronous SPI
    - I^2C
- Flexible power management system
  - Integrated LDO with 1.8-V regulated core supply voltage
  - Supply voltage monitor with programmable level detection
  - Brownout detector
  - Built-in voltage reference
  - Temperature sensor
- Clock system
  - 16.384-MHz internal digitally controlled oscillator (DCO)
  - DCO operation with internal or external resistor
  - External digital clock source
- Development tools and software (also see Tools and Software)
  - EVM430-I2040S evaluation module (EVM) for metering
  - MSP-TS430RHB32A 100-pin target development board
  - MSP430Ware™ code examples
- Wake up from standby mode in 1 µs
- 16-bit RISC architecture, up to 16.384-MHz system clock
- Serial onboard programming, no external programming voltage needed
- Available in 28-pin TSSOP (PW) and 32-pin VQFN (RHB) packages
- Device Comparison summarizes the available family members
- Featured software and reference designs
  - Energy Measurement Design Center for MSP430 MCUs application software and frameworks
  - Digital Signal Processing (DSP) Library for MSP430 Microcontrollers software libraries
  - Single Phase and DC Embedded Metering reference design
  - Three Output Smart Power Strip reference design

2 Applications

- Metering
- Submetering
- Power monitoring and control
- Industrial sensors
- 1-phase AC and DC power monitoring
- 2-phase electronic meters
- Smart plugs
- Smart power strips
- Medical – multiple-parameter patient monitoring

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

3 Description

The Texas Instruments MSP430i204x, MSP430I203x and MSP430I202x microcontrollers (MCUs) are part of the MSP430™ Metrology and Monitoring portfolio. The architecture and integrated peripherals, combined with five extensive low-power modes, are optimized to achieve extended battery life in portable and battery-powered measurement applications. The devices feature a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the devices to wake up from low-power modes to active mode in less than 5 µs.

The MSP430i204x MCUs include four high-performance 24-bit sigma-delta ADCs, two eUSCIs (one eUSCI_A module and one eUSCI_B module), two 16-bit timers, a hardware multiplier, and up to 16 I/O pins.

The MSP430I203x MCUs include three high-performance 24-bit sigma-delta ADCs, two eUSCIs (one eUSCI_A module and one eUSCI_B module), two 16-bit timers, a hardware multiplier, and up to 16 I/O pins.

The MSP430I202x MCUs include two high-performance 24-bit sigma-delta ADCs, two eUSCIs (one eUSCI_A module and one eUSCI_B module), two 16-bit timers, a hardware multiplier, and up to 16 I/O pins.

Typical applications for these devices include energy measurement, analog and digital sensor systems, LED lighting, digital power supplies, motor controls, remote controls, thermostats, digital timers, and hand-held meters.

The MSP430i204x, MSP430I203x and MSP430I202x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get your design started quickly. Development kits include the EVM430-I2040S evaluation module (EVM) for metering and the MSP-TS430RHB32A 100-pin target development board. The Energy Measurement Design Center for MSP430 MCUs is provided as a rapid development tool that enables energy measurement on these devices. TI also provides free MSP430Ware™ software, which is available as a component of Code Composer Studio™ IDE desktop and cloud versions within TI Resource Explorer. The MSP430 MCUs are also supported by extensive online collateral, training, and online support through the TI E2E™ support forums.

For complete module descriptions, see the MSP430i2xx Family User's Guide.

Device Information

(1)PART NUMBER	PACKAGE	BODY SIZE(2)
MSP430i2041TPW	TSSOP (28)	9.7 mm × 4.4 mm
MSP430i2041TRHB	VQFN (32)	5 mm × 5 mm

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 12, or see the TI website at www.ti.com.

(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 12.

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4 Functional Block Diagram

Figure 4-1 shows the functional block diagram for the MSP430i204x devices in the RHB package. For the functional block diagrams of all device variants and packages, see Section 9.2.

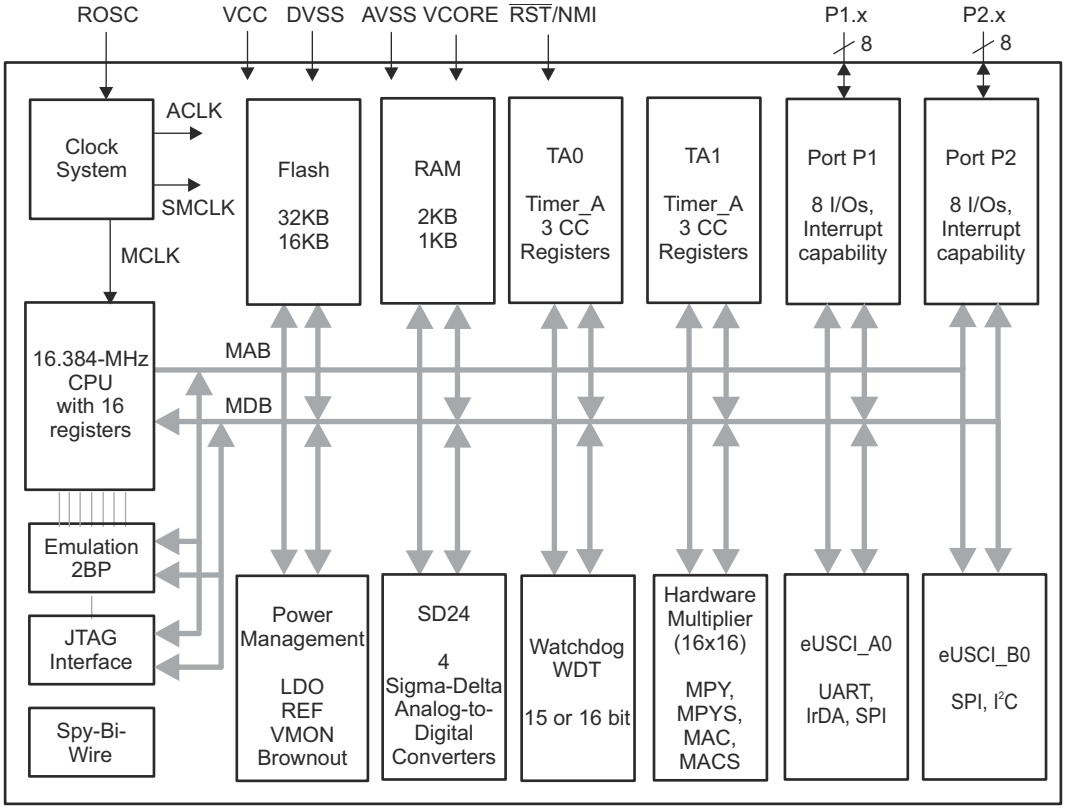

Figure 4-1. Functional Block Diagram – RHB Package – MSP430i204x

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from revision B to revision C

Changes from March 4, 2020 to March 16, 2021	Page
• Updated the numbering format for tables, figures, and cross references throughout the document	1
• Updated "Featured software and reference designs" in Section 1, *Features*	1

Changes from revision A to revision B

Changes from May 3, 2018 to March 3, 2020	Page
• Updated Section 1, *Features*	1
• Updated Section 3, *Description*	2
• Added 2 and 4 to the SD24GAINx options in the test conditions of the "Gain error" parameter in Section 8.7.7.5, *SD24 Performance, Internal Reference (SD24REFS = 1, SD24OSRx = 256)*	23
• Added 2 and 4 to the SD24GAINx options in the test conditions of the "Gain error" parameter in Section 8.7.7.6, *SD24 Performance, External Reference (SD24REFS = 0, SD24OSRx = 256)*	24
• Changed the MIN values for the $t_{HD,STA}$, $t_{SU,STA}$, $t_{HD,DAT}$, $t_{SU,DAT}$, and $t_{SU,STO}$ parameters in Section 8.7.8.6, *eUSCI (I^2C Mode) Timing*	30
• Updated descriptions and links in Section 10, *Applications, Implementation, and Layout*	61

Changes from the initial release to revision A

Changes from August 31, 2014 to May 2, 2018	Page
• Changed the list of applications in Section 2, *Applications*	1
• Added Section 6.1, *Related Products*	6
• Added typical conditions statements at the beginning of Section 8, *Specifications*	13
• Added SD24 input pins and AUXVCCx pins to exception list on "Voltage applied to pins" parameter, and added SD24 input pin limits in "Diode current at pins" parameter in Section 8.1, *Absolute Maximum Ratings*	13
• Added Section 8.2, *ESD Ratings*	13
• Added Section 8.6, *Thermal Resistance Characteristics*	15
• Changed the MAX value of the $t_{WAKE-UP-LPM4}$ parameter from 35 µs to 45 µs in Section 8.7.3.1, *Wake-up Times From Low Power Modes*	17
• Added the CAUTION that begins "The CPU will lock up if..." in Section 9.3, *CPU*	38

6 Device Comparison

Table 6-1 summarizes the available family members.

Table 6-1. Device Comparison

DEVICE(1)	FLASH (KB)	SRAM (KB)	SD24 CONVERTERS	MULTIPLIER	Timer_A(2)	eUSCI_A: UART, IrDA, SPI	eUSCI_B: SPI, I²C	I/O	PACKAGE
MSP430i2041	32	2	4	1	3, 3	1	1	16	32 RHB
								12	28 PW
MSP430i2040	16	1	4	1	3, 3	1	1	16	32 RHB
								12	28 PW
MSP430i2031	32	2	3	1	3, 3	1	1	16	32 RHB
								12	28 PW
MSP430i2030	16	1	3	1	3, 3	1	1	16	32 RHB
								12	28 PW
MSP430i2021	32	2	2	1	3, 3	1	1	16	32 RHB
								12	28 PW
MSP430i2020	16	1	2	1	3, 3	1	1	16	32 RHB
								12	28 PW

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 12, or see the TI website at www.ti.com.

(2) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

6.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers

High-performance, low-power solutions to enable the autonomous future

MSP430 ultra-low-power sensing and measurement microcontrollers

One platform. One ecosystem. Endless possibilities.

Reference designs for MSP430i2041

Find reference designs leveraging the best in TI technology to solve your system-level challenges. All designs include a schematic, test data and design files.

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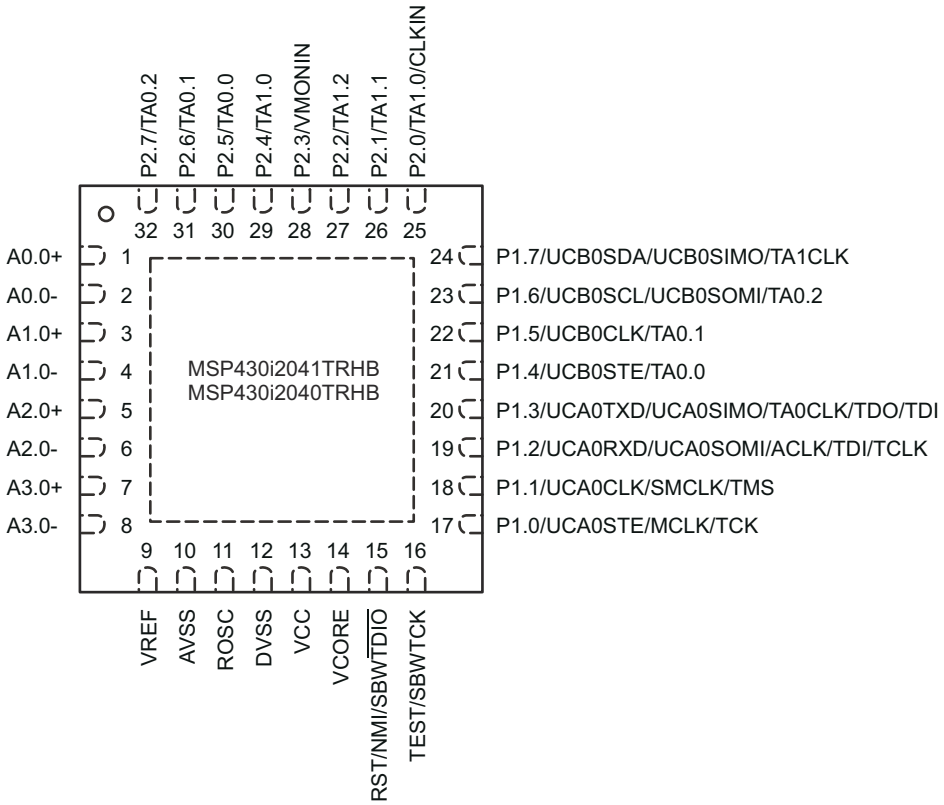
7 Terminal Configuration and Functions

7.1 Pin Diagrams

Figure 7-1 shows the pin assignments for the MSP430i2041 and MSP430i2040 devices in the RHB package.



NOTE: TI recommends connecting the thermal pad on the RHB package to DVSS.

Figure 7-1. 32-Pin RHB Package (Top View) – MSP430i2041, MSP430i2040

Figure 7-2 shows the pin assignments for the MSP430i2041 and MSP430i2040 devices in the PW package.

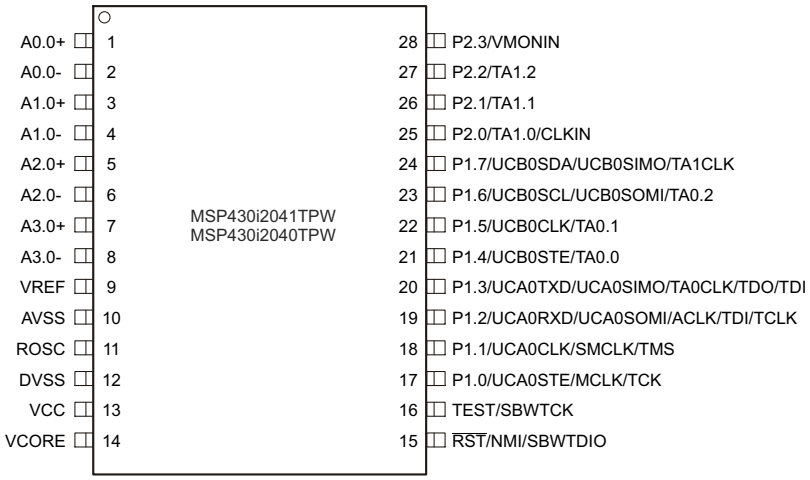
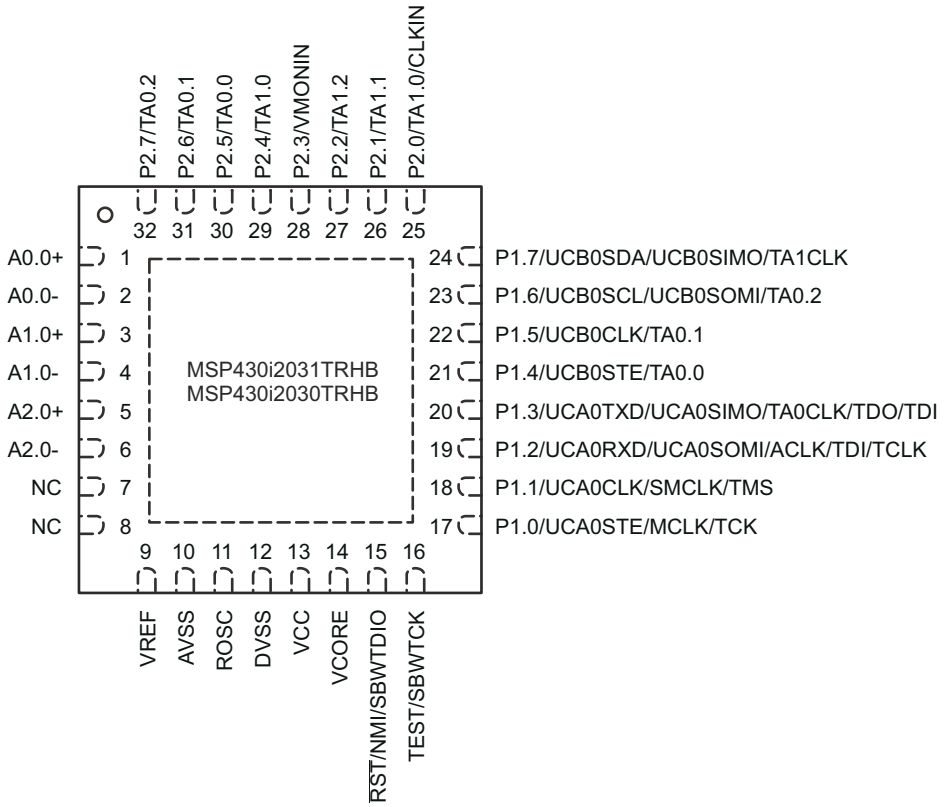


Figure 7-2. 28-Pin PW Package (Top View) – MSP430i2041, MSP430i2040

Figure 7-3 shows the pin assignments for the MSP430i2031 and MSP430i2030 devices in the RHB package.

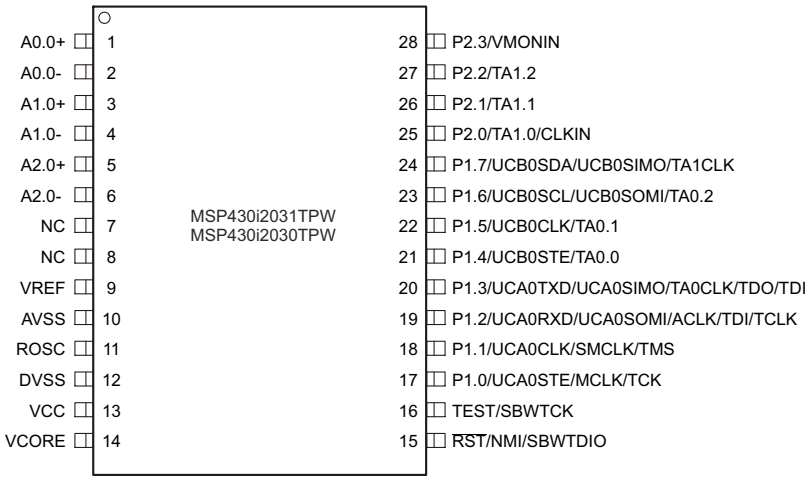


NOTE: TI recommends connecting the thermal pad on the RHB package to DVSS.

NOTE: TI recommends connecting NC pins to AVSS.

Figure 7-3. 32-Pin RHB Package (Top View) – MSP430i2031, MSP430i2030

Figure 7-4 shows the pin assignments for the MSP430i2031 and MSP430i2030 devices in the PW package.



NOTE: TI recommends connecting NC pins to AVSS.

Figure 7-4. 28-Pin PW Package (Top View) – MSP430i2031, MSP430i2030

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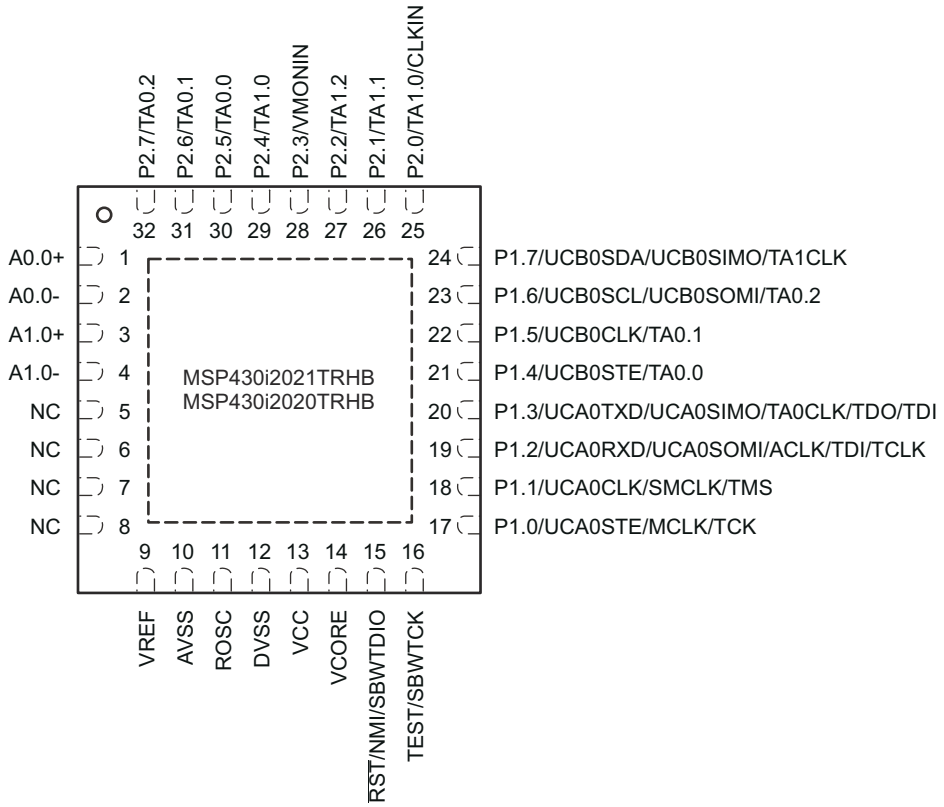
Figure 7-5 shows the pin assignments for the MSP430i2021 and MSP430i2020 devices in the RHB package.

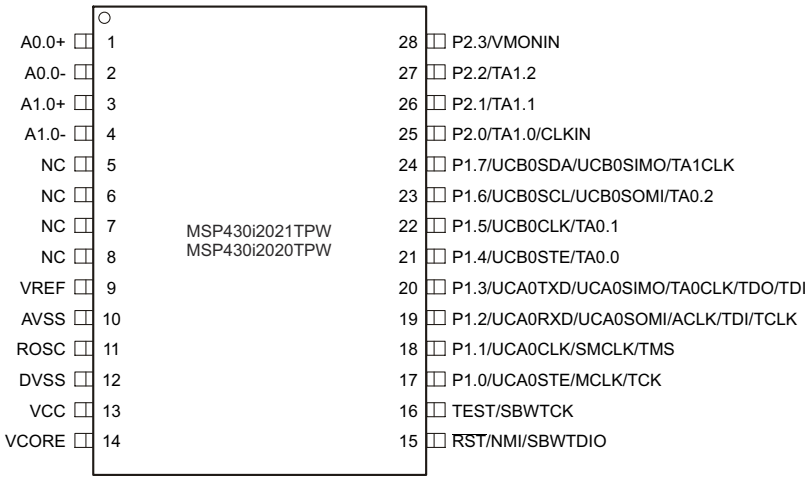


NOTE: TI recommends connecting the thermal pad on the RHB package to DVSS.

TI recommends connecting NC pins to AVSS.

Figure 7-5. 32-Pin RHB Package (Top View) – MSP430i2021, MSP430i2020

Figure 7-6 shows the pin assignments for the MSP430i2021 and MSP430i2020 devices in the PW package.



TI recommends connecting NC pins to AVSS.

Figure 7-6. 28-Pin PW Package (Top View) – MSP430i2021, MSP430i2020

7.2 Signal Descriptions

Section 7.2 describes the signals for all device variants and package options.

Table 7-1. Signal Descriptions

TERMINAL			I/O[1]	DESCRIPTION
NAME	NO.[2]			
	PW	RHB		
A0.0+	1	1	I	SD24 positive analog input A0.0[3]
A0.0-	2	2	I	SD24 negative analog input A0.0[3]
A1.0+	3	3	I	SD24 positive analog input A1.0[3]
A1.0-	4	4	I	SD24 negative analog input A1.0[3]
A2.0+	5	5	I	SD24 positive analog input A2.0[3] [4]
A2.0-	6	6	I	SD24 negative analog input A2.0[3] [4]
A3.0+	7	7	I	SD24 positive analog input A3.0 [3] [4] [5]
A3.0-	8	8	I	SD24 negative analog input A3.0 [3] [4] [5]
VREF[6]	9	9	I	SD24 external reference voltage input
AVSS	10	10		Analog supply voltage, negative terminal
ROSC	11	11		External resistor pin for DCO. Connect recommended resistor between ROSC and AVSS for DCO operation in external resistor mode. Connect ROSC to AVSS while operating DCO in internal resistor mode.
DVSS	12	12		Digital supply voltage, negative terminal
VCC	13	13		Analog and digital supply voltage, positive terminal
VCORE [7]	14	14		Regulated core power supply (internal use only, no external current loading)
$\overline{\text{RST}}$/NMI/SBWTDIO	15	15	I/O	Reset or nonmaskable interrupt input. Spy-Bi-Wire test data input/output for device programming and test.
TEST/SBWTCK	16	16	I	Selects test mode for JTAG pins on P1.0 to P1.3. Spy-Bi-Wire test clock input for device programming and test.
P1.0/UCA0STE/MCLK/TCK	17	17	I/O	General-purpose digital I/O pin. eUSCI_A0 SPI slave transmit enable (direction controlled by eUSCI). MCLK output. JTAG test clock. TCK is the clock input port for device programming and test.
P1.1/UCA0CLK/SMCLK/TMS	18	18	I/O	General-purpose digital I/O pin. eUSCI_A0 clock input/output (direction controlled by eUSCI). SMCLK output. JTAG test mode select. TMS is used as an input port for device programming and test.
P1.2/UCA0RXD/UCA0SOMI/ACLK/TDI/TCLK	19	19	I/O	General-purpose digital I/O pin. eUSCI_A0 UART receive data or eUSCI_A0 SPI slave out/master in (direction controlled by eUSCI). ACLK output. JTAG test data input or test clock input for device programming and test.
P1.3/UCA0TXD/UCA0SIMO/TA0CLK/TDO/TDI	20	20	I/O	General-purpose digital I/O pin. eUSCI_A0 UART transmit data or eUSCI_A0 SPI slave in/master out (direction controlled by eUSCI). Timer external clock input TACLK for TA0. JTAG test data output port. TDO/TDI data output or programming data input terminal.
P1.4/UCB0STE/TA0.0	21	21	I/O	General-purpose digital I/O pin. eUSCI_B0 SPI slave transmit enable (direction controlled by eUSCI). Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output.

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Table 7-1. Signal Descriptions (continued)

TERMINAL			I/O[1]	DESCRIPTION
NAME	NO.[2]			
	PW	RHB		
P1.5/UCB0CLK/TA0.1	22	22	I/O	General-purpose digital I/O pin. eUSCI_B0 clock input/output (direction controlled by eUSCI). Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output.
P1.6/UCB0SCL/UCB0SOMI/ TA0.2	23	23	I/O	General-purpose digital I/O pin. eUSCI_B0 I^2C clock or eUSCI_B0 SPI slave out/master in (direction controlled by eUSCI). Timer TA0 CCR2 capture: CCI2A input, compare: Out2 output.
P1.7/UCB0SDA/UCB0SIMO/ TA1CLK	24	24	I/O	General-purpose digital I/O pin. eUSCI_B0 I^2C data or eUSCI_B0 slave input/master output (direction controlled by eUSCI). Timer external clock input TACLK for TA1.
P2.0/TA1.0/CLKIN	25	25	I/O	General-purpose digital I/O pin. Timer TA1 CCR0 capture: CCI0A input, compare: Out0 output. DCO bypass clock input.
P2.1/TA1.1	26	26	I/O	General-purpose digital I/O pin. Timer TA1 CCR1 capture: CCI1A input, compare: Out1 output.
P2.2/TA1.2	27	27	I/O	General-purpose digital I/O pin. Timer TA1 CCR2 capture: CCI2A input, compare: Out2 output.
P2.3/VMONIN	28	28	I/O	General-purpose digital I/O pin. Voltage monitor input.
P2.4/TA1.0[8]	N/A	29	I/O	General-purpose digital I/O pin. Timer TA1 CCR0 capture: CCI0B input, compare: Out0 output.
P2.5/TA0.0[8]	N/A	30	I/O	General-purpose digital I/O pin. Timer TA0 CCR0 capture: CCI0B input, compare: Out0 output.
P2.6/TA0.1[8]	N/A	31	I/O	General-purpose digital I/O pin. Timer TA0 CCR1 compare: Out1 output.
P2.7/TA0.2[8]	N/A	32	I/O	General-purpose digital I/O pin. Timer TA0 CCR2 compare: Out2 output.

(1) I = input, O = output
(2) N/A = not available
(3) Short unused analog input pairs and connect them to analog ground (see Section 7.4 for recommendations on all unused pins).
(4) Not available on MSP430i2021 and MSP430i2020 devices.
(5) Not available on MSP430i2031 and MSP430i2030 devices.
(6) When the SD24 operates with the internal reference (SD24REFS = 1), the VREF pin must not be loaded externally. Connect only the recommended capacitor value (C_{VREF}) from the VREF pin to AVSS (see Section 8.7.7.2).
(7) VCORE is for internal use only. No external current loading is possible. Connect VCORE to only the recommended capacitor value (C_{VCORE}) (see Section 8.3).
(8) These pins are not available on the 28-pin PW package. Program these four pins to output direction and drive value 0 in software.

7.3 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see Section 9.11.

7.4 Connection of Unused Pins

Table 7-2 lists the correct termination of all unused pins.

Table 7-2. Connection of Unused Pins

PIN(1)	POTENTIAL	COMMENT
AVCC	DVCC	
AVSS	DVSS	
VREF	Open	
ROSC	AVSS	Connect the ROSC pin to AVSS when the DCO is used in internal resistor mode.
Px.0 to Px.7	Open	Set to port function, output direction.
Ax.0+ and Ax.0-	AVSS	Short unused analog input pairs and connect them to analog ground.
$\overline{\text{RST}}$/NMI	DVCC or VCC	47-kΩ pullup with 10 nF (or 2.2 nF(2)) pulldown
TEST	Open	This pin always has an internal pulldown enabled.
P1.3/TDO P1.2/TDI P1.1/TMS P1.0/TCK	Open	The JTAG pins are shared with general-purpose I/O function (P1.x). If these pins are not used, set them to port function and output direction. When used as JTAG pins, leave these pins open.

(1) For any unused pin with a secondary function that is shared with general-purpose I/O, follow the guidelines for the Px.0 to Px.7 unused pin connection.

(2) The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

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8 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted.

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

		MIN	MAX	UNIT
Supply voltage applied at VCC		–0.3	4.1	V
Voltage applied to pins	All pins except VCORE[3], ROSC[4], and SD24 input pins (A0.0+, A0.0-, A1.0+, A1.0-, A2.0+, A2.0-, A3.0+, A3.0-)[5]	–0.3	V_{CC} + 0.3	V
Diode current at pins	All pins except SD24 input pins (A0.0+, A0.0-, A1.0+, A1.0-, A2.0+, A2.0-, A3.0+, A3.0-)		±2	mA
	A0.0+, A0.0-, A1.0+, A1.0-, A2.0+, A2.0-, A3.0+, A3.0-[6]		2	
Maximum junction temperature, $T_{J,MAX}$			115	°C
Storage temperature, T_{stg} [7]		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are referenced to V_{SS}.

(3) VCORE is for internal device use only. Do not apply external DC loading or voltage at VCORE.

(4) Do not apply external DC loading or voltage at ROSC. Connect the recommended resistor at ROSC using the DCO in external resistor mode. Connect ROSC to AVSS when operating the DCO in internal resistor mode.

(5) See Section 8.7.7.1 for SD24 specifications.

(6) A protection diode is connected to V_{CC} for the SD24 input pins. No protection diode is connected to V_{SS}.

(7) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

8.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming or erase (VCC = V_{CC})		2.2		3.6	V
V_{SS}	Supply voltage (AVSS = DVSS = V_{SS})			0		V
T_A	Operating free-air temperature	T temperature range	–40		105	°C
T_J	Operating junction temperature	T temperature range	–40		105	°C
C_{VCORE}	Recommended capacitor at VCORE			470		nF
C_{VCC}/ C_{VCORE}	Capacitor ratio of VCC to VCORE		10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency) [1] [2]		0		16.384	MHz

(1) The MSP430i CPU is clocked directly with MCLK.

(2) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.

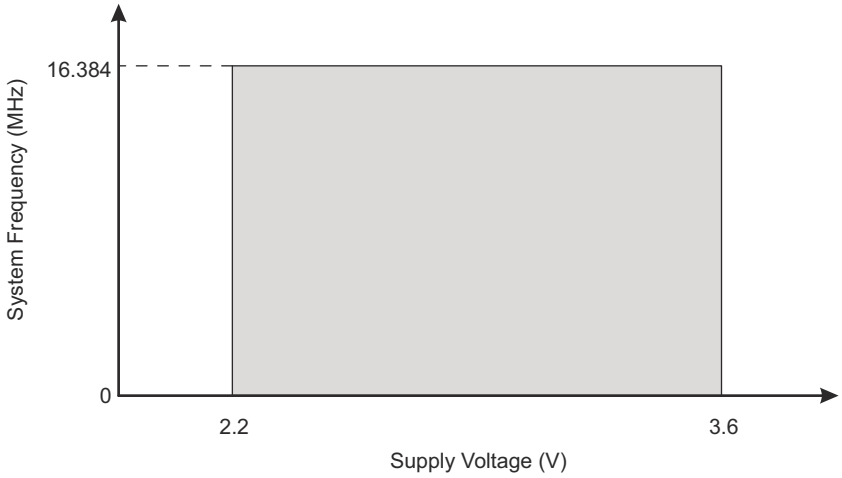

Figure 8-1. Maximum System Frequency

8.4 Active Mode Supply Current (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[(1) (2)]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM, 1.024MHz}$	Active mode current at 1.024 MHz	f_{DCO} = 16.384 MHz, f_{MCLK} = f_{SMCLK} = 1.024 MHz, f_{ACLK} = 32 kHz, Program executes from flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	3 V		1.6		mA
$I_{AM, 8.192MHz}$	Active mode current at 8.192 MHz	f_{DCO} = 16.384 MHz, f_{MCLK} = f_{SMCLK} = 8.192 MHz, f_{ACLK} = 32 kHz, Program executes from flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	3 V		3.0		mA
$I_{AM, 16.384MHz}$	Active mode current at 16.384 MHz	f_{DCO} = f_{MCLK} = f_{SMCLK} = 16.384 MHz, f_{ACLK} = 32 kHz, Program executes from flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	3 V		4.5		mA

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.

(2) All peripherals are inactive.

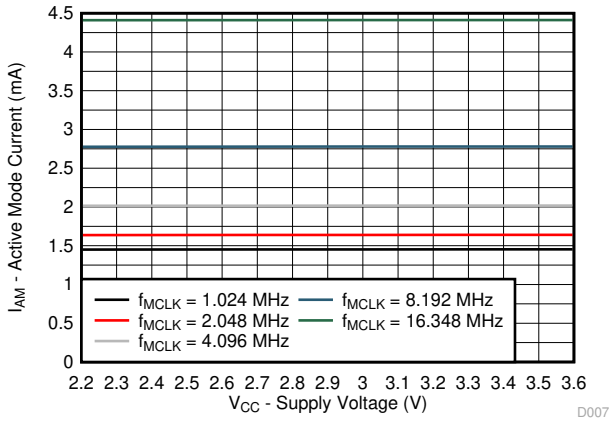

Figure 8-2. Active Mode Current vs Supply Voltage

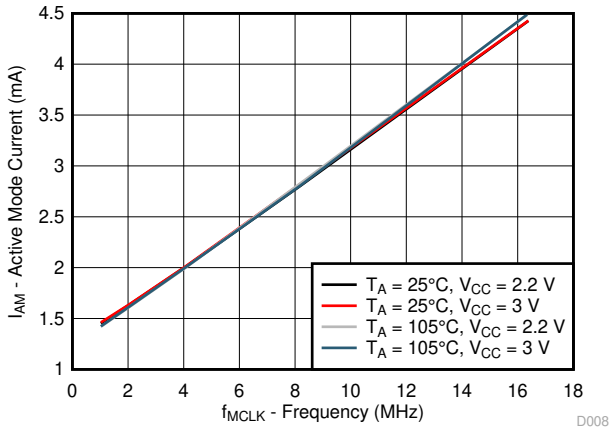

Figure 8-3. Active Mode Current vs MCLK Frequency

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8.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
I_{LPM3}	Low-power mode 3 (LPM3) current [2]	f_{DCO} = 16.384 MHz, f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32 kHz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	3 V		210		µA
I_{LPM4}	Low-power mode 4 (LPM4) current [3]	f_{DCO} = f_{MCLK} = f_{SMCLK} = f_{ACLK} = 0 MHz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	3 V		70		µA
$I_{LPM4.5}$	Low-power mode 4.5 (LPM4.5) current [3]	f_{DCO} = f_{MCLK} = f_{SMCLK} = f_{ACLK} = 0 MHz, REGOFF = 1, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	3 V		75		nA
			105°C			325		nA

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.

(2) Current for watchdog timer clocked by ACLK included. All other peripherals are inactive.

(3) All peripherals are inactive.

8.6 Thermal Resistance Characteristics

THERMAL METRIC[1]		PACKAGE	VALUE[2] [3]	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	QFN-32 (RHB)	35.9	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance		25.5	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance		8.6	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		8.6	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.3	°C/W
$R\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance		1.4	°C/W
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	TSSOP-28 (PW)	77.5	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance		18.2	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance		35.5	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		35.0	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.5	°C/W
$R\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC package thermal metrics.

(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(3) N/A = Not applicable

8.7 Timing and Switching Characteristics

8.7.1 Reset Timing

8.7.1.1 Reset Timing

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_{RESET}	Pulse duration required at the $\overline{RST}$/NMI pin to accept a reset	4		µs

8.7.2 Clock Specifications

8.7.2.1 DCO in External Resistor Mode

recommended resistor at ROSC pin: 20 kΩ, 0.1%, ±50 ppm/°C)[1]
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DCO}	DCO current consumption			85		µA
f_{DCO}	DCO frequency calibrated			16.384		MHz
	DCO absolute tolerance calibrated	V_{CC} = 3 V, T_A = 25°C			±0.25%	
df_{DCO}/d_T	DCO frequency temperature drift				±20	ppm/°C
df_{DCO}/dVCC	DCO frequency supply voltage drift			200	600	ppm/V
DC_{DCO}	Duty cycle			50%		
T_{dcoon}	DCO start-up time			40		µs

(1) The maximum parasitic capacitance at ROSC pin should not exceed 5 pF to ensure the specified DCO start-up time.

8.7.2.2 DCO in Internal Resistor Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DCO}	DCO current consumption			85		µA
f_{DCO}	DCO frequency calibrated			16.384		MHz
	DCO absolute tolerance calibrated	V_{CC} = 3 V, T_A = 25°C			±0.9%	
df_{DCO}/d_T	DCO frequency temperature drift				±200	ppm/°C
df_{DCO}/dVCC	DCO frequency supply voltage drift			200	600	ppm/V
DC_{DCO}	Duty cycle			50%		
T_{dcoon}	DCO start-up time			40		µs

8.7.2.3 DCO Overall Tolerance Table

over operating free-air temperature range (unless otherwise noted)

RESISTOR OPTION	TEMPERATURE CHANGE	TEMPERATURE DRIFT (%)	VOLTAGE CHANGE	VOLTAGE DRIFT (%)	OVERALL DRIFT (%)	OVERALL ACCURACY (%)
Internal resistor	–40°C to 105 °C	±2.9	2.2 V to 3.6 V	±0.084	±2.984	±3.884
	0°C	0	2.2 V to 3.6 V	±0.084	±0.084	±0.984
	–40°C to 105 °C	±2.9	0 V	0	±2.9	±3.8
External resistor with 50-ppm TCR	–40°C to 105 °C	±0.29	2.2 V to 3.6 V	±0.084	±0.374	±0.624
	0°C	0	2.2 V to 3.6 V	±0.084	±0.084	±0.334
	–40°C to 105 °C	±0.29	0 V	0	±0.29	±0.54

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8.7.2.4 DCO in Bypass Mode Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
f_{DCOBYP}	Frequency in DCO bypass mode[(1)]	0	16.384	MHz

(1) External digital clock frequency in DCO bypass mode must be 16.384 MHz for the SD24 module to meet the specified performance.

8.7.3 Wake-up Characteristics

8.7.3.1 Wake-up Times From Low Power Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{WAKE-UP-LPM3}$	Wake-up time from LPM3 to active mode	MCLK = SMCLK = 1.024 MHz		1		µs
$t_{WAKE-UP-LPM4}$	Wake-up time from LPM4 to active mode	MCLK = SMCLK = 1.024 MHz		45		µs
$t_{WAKE-UP-LPM4.5-IO}$	Wake-up time from LPM4.5 to active mode upon I/O event[(1)]	C_{VCORE} = 470 nF		0.45		ms
$t_{WAKE-UP-LPM4.5-RESET}$	Wake-up time from LPM4.5 to active mode upon external reset ($\overline{RST}$)[(1)]	C_{VCORE} = 470 nF		0.45		ms

(1) This value represents the time from the wake-up event to the reset vector execution by CPU.

8.7.4 I/O Ports

8.7.4.1 Schmitt-Trigger Inputs – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.5 V_{CC}		0.7 V_{CC}	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT-}$)		3 V	0.4		1.1	V
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

8.7.4.2 Inputs – Ports P1 and P2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing[(1)]	Port P1, P2: P1.x to P2.x, External trigger pulse duration to set interrupt flag	3 V	20		ns

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

8.7.4.3 Leakage Current – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Py.x)}$	High-impedance leakage current	See [(1) (2)]	3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input.

8.7.4.4 Outputs – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –6 mA[(1)]	3.0 V	V_{CC} – 0.60	V_{CC}	V
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 6 mA[(1)]	3.0 V	V_{SS}	V_{SS} + 0.60	V

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

8.7.4.5 Output Frequency – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
$f_{Py.x}$	Port output frequency (with load)	Py.x, C_L = 20 pF, R_L = 3.2 kΩ [(1) (2)]	3 V	16.384	MHz
f_{Port_CLK}	Clock output frequency	Py.x, C_L = 20 pF[(2)]	3 V	16.384	MHz

(1) A resistive divider with two times 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.

(2) The output voltage reaches at least 10% and 90% of V_{CC} at the specified toggle frequency.

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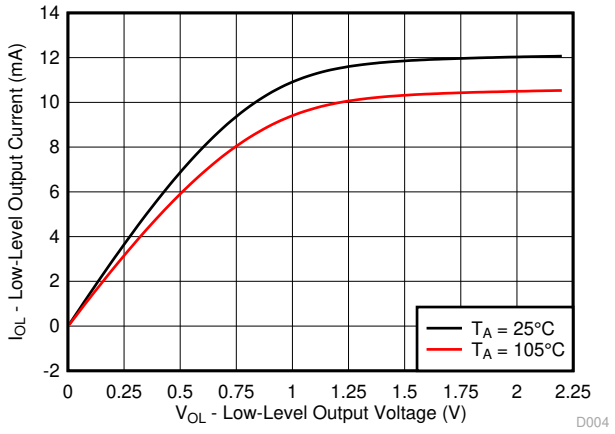
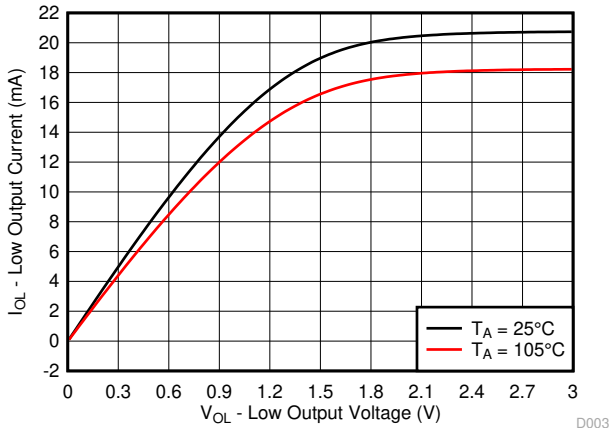
8.7.4.6 Typical Characteristics – Outputs

One output loaded at a time.



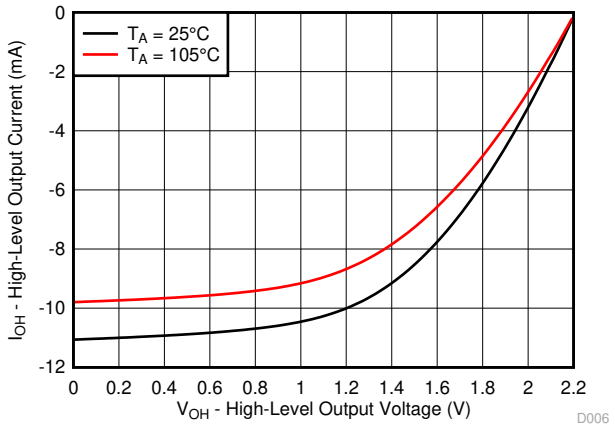
V_{CC} = 2.2 V Measured at P1.3

Figure 8-4. Typical Low-Level Output Current vs Low-Level Output Voltage



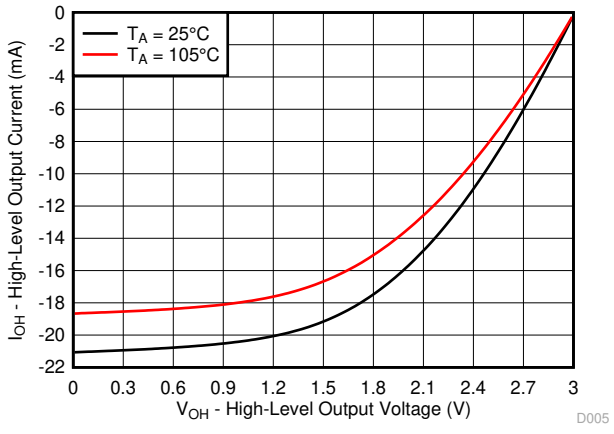
V_{CC} = 3 V Measured at P1.3

Figure 8-5. Typical Low-Level Output Current vs Low-Level Output Voltage



V_{CC} = 2.2 V Measured at P1.3

Figure 8-6. Typical High-Level Output Current vs High-Level Output Voltage



V_{CC} = 3 V Measured at P1.3

Figure 8-7. Typical High-Level Output Current vs High-Level Output Voltage

8.7.5 Power Management Module

8.7.5.1 PMM, High-Side Brownout Reset (BORH)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V(V_{CC}_BOR_IT–)$	BOR_H on voltage, V_{CC} falling level	$\lvert dV_{CC}/d_t \rvert < 3$ V/s		1.08		V
$V(V_{CC}_BOR_IT+)$	BOR_H off voltage, V_{CC} rising level	$\lvert dV_{CC}/d_t \rvert < 3$ V/s		1.18		V
$V(V_{CC}_BOR_hys)$	BOR_H hysteresis			100		mV
$t_{POWERUP}$ (1)	Cold power-up time				0.75	ms

(1) This is the time duration between application of V_{CC} and execution of reset vector by CPU.

8.7.5.2 PMM, Low-Side SVS (SVSL)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
V(SVSL)	SVSL trip voltage on VCORE		1.70		V
V(SVSL_hys)	SVSL hysteresis		14		mV
I(SVSL)	SVSL current consumption		3		µA

8.7.5.3 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
V_{CORE}	Core voltage		1.83		V

8.7.5.4 PMM, Voltage Monitor (VMON)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VMON_{trip_level}$	VMONIN trip level	VMONLVLx = 111b		1.17		V
	VCC trip level – 1	VMONLVLx = 001b		2.32		
	VCC trip level – 2	VMONLVLx = 010b		2.62		
	VCC trip level – 3	VMONLVLx = 011b		2.82		
I_{VMON}	VMON current consumption			6		µA
t_{VMON}	VMON settling time			0.5		µs

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8.7.6 Reference Module

8.7.6.1 Voltage Reference (REF)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range		2.2		3.6	V
V_{BG}	Bandgap output voltage calibrated	V_{CC} = 3 V	1.146	1.158	1.17	V
PSRR_DC	Power supply rejection ratio (DC)	V_{CC} = 2.2 V to 3.6 V		50		µV/V
PSRR_AC	Power supply rejection ratio (AC)	V_{CC} = 2.2 V to 3.6 V, f = 1 kHz, ΔVpp = 100 mV		0.35		mV/V
dV_{BG}/d_T	Bandgap reference temperature coefficient	V_{CC} = 3 V		10	50	ppm/°C

8.7.6.2 Temperature Sensor

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{sensor}	Temperature sensor output voltage	V_{CC} = 3 V, T_A = 30°C	610	650	690	mV
		V_{CC} = 3 V, T_A = 105°C	765	805	845	
I_{sensor}	Temperature sensor quiescent current consumption			3		µA
TC_{sensor}	Temperature coefficient of sensor		1.96	2.07	2.17	mV/°C

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8.7.7 SD24

8.7.7.1 SD24 Power Supply and Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	AVSS = DVSS = 0 V			2.2		3.6	V
I_{SD24}	Analog plus digital supply current per converter (reference current not included)	SD24OSRx = 256	GAIN: 1, 2, 4, 8, 16	3 V		190		µA
			GAIN: 1, 16	3 V			250	

8.7.7.2 SD24 Internal Voltage Reference

over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{SD24REF}$	SD24 internal reference voltage	SD24REFS = 1	3 V	1.146	1.158	1.17	V
C_{VREF}	Recommended capacitor at VREF				100		nF
$t_{SD24REF_settle}$	SD24 reference buffer settling time	SD24REFS = 0 → 1, C_{VREF} = 100 nF			200		µs

(1) When SD24 operates with internal reference (SD24REFS = 1), the VREF pin must not be loaded externally. Only the recommended capacitor value, C_{VREF} must be connected at the VREF pin to AVSS.

8.7.7.3 SD24 External Voltage Reference

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	SD24REFS = 0	3 V	1.0	1.2	1.5	V
$I_{REF(I)}$	Input current	SD24REFS = 0	3 V			50	nA

8.7.7.4 SD24 Input Range

over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{ID,FSR}$	Differential full-scale input voltage range	$V_{ID} = V_{I,A+} – V_{I,A–}$			$–V_{REF}$/GAIN		$+V_{REF}$/GAIN	V
V_{ID}	Differential input voltage range for specified performance[2]	SD24REFS = 1	SD24GAINx = 1			±928		mV
			SD24GAINx = 2			±464		
			SD24GAINx = 4			±232		
			SD24GAINx = 8			±116		
			SD24GAINx = 16			±58		
Z_I	Input impedance (pin A+ or A- to AV_{SS})[3]	SD24GAINx = 1, 16		3 V		200		kΩ
Z_{ID}	Differential input impedance (pin A+ to pin A-)[3]	SD24GAINx = 1, 16		3 V	300	400		kΩ
V_I	Absolute input voltage range				AV_{SS} – 1		V_{CC}	V
V_{IC}	Common-mode input voltage range				AV_{SS} – 1		V_{CC}	V

(1) All parameters pertain to each SD24 channel.

(2) The full-scale range is defined by $V_{FSR+} = +V_{REF}/GAIN$ and $V_{FSR–} = –V_{REF}/GAIN$; FSR = $V_{FSR+} – V_{FSR–} = 2xV_{REF}/GAIN$. If VREF is sourced externally, the analog input range should not exceed 80% of V_{FSR+} or $V_{FSR–}$; that is, V_{ID} = 0.8 $V_{FSR–}$ to 0.8 V_{FSR+}. If VREF is sourced internally, the given V_{ID} ranges apply.

(3) Applicable for SD24 modulator OFF as well as ON conditions.

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8.7.7.5 SD24 Performance, Internal Reference (SD24REFS = 1, SD24OSRx = 256)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD24GAINx = 1	f_{IN} = 50 Hz(1)	3 V	84	89		dB
		SD24GAINx = 2				89		
		SD24GAINx = 4				87		
		SD24GAINx = 8				83		
		SD24GAINx = 16				77		
THD	Total harmonic distortion	SD24GAINx = 1	f_{IN} = 50 Hz(1)	3 V		100		dB
		SD24GAINx = 8				95		
		SD24GAINx = 16				90		
SFDR	Spurious-free dynamic range	SD24GAINx = 1	f_{IN} = 50 Hz(1)	3 V		100		dB
		SD24GAINx = 8				95		
		SD24GAINx = 16				90		
INL	Integral nonlinearity, end-point fit	SD24GAINx: 1, 8, 16		3 V	–0.003		0.003	% FSR
G	Nominal gain	SD24GAINx = 1		3 V		1		
		SD24GAINx = 2				2		
		SD24GAINx = 4				4		
		SD24GAINx = 8				8		
		SD24GAINx = 16				16		
E_G	Gain error	SD24GAINx: 1, 2, 4, 8, 16		3 V	–2%		2%	
$\Delta E_G/\Delta T$	Gain error temperature coefficient	SD24GAINx: 1, 8, 16		3 V			50	ppm/°C
E_{OS}	Offset error	SD24GAINx = 1		3 V			4	mV
		SD24GAINx = 16					2	
ΔEOS/ΔT	Offset error temperature coefficient	SD24GAINx = 1		3 V		±5	±25	ppm FSR/°C
		SD24GAINx = 16				±3	±10	
CMRR,50Hz	Common-mode rejection ratio at 50 Hz	SD24GAINx = 1, Common-mode input signal: V_{ID} = 928 mV, f_{IN} = 50 Hz		3 V		–55		dB
		SD24GAINx = 16, Common-mode input signal: V_{ID} = 58 mV, f_{IN} = 50 Hz				–60		
AC PSRR	AC power supply rejection ratio	SD24GAINx: 1, V_{CC} = 3 V ±50 mV × sin(2π × f_{VCC} × t), f_{VCC} = 50 Hz, Inputs grounded (no analog signal applied)		3 V		–90		dB
		SD24GAINx: 8, V_{CC} = 3 V ±50 mV × sin(2π × f_{VCC} × t), f_{VCC} = 50 Hz, Inputs grounded (no analog signal applied)		3 V		–95		
		SD24GAINx: 16, V_{CC} = 3 V ±50 mV × sin(2π × f_{VCC} × t), f_{VCC} = 50 Hz, Inputs grounded (no analog signal applied)		3 V		–95		
XT	Crosstalk between converters	Crosstalk source: SD24GAINx = 1, Sine-wave with maximum possible V_{PP}, f_{IN} = 50 Hz or 100 Hz, Converter under test: SD24GAINx = 1		3 V		–120		dB
		Crosstalk source: SD24GAINx = 1, Sine-wave with maximum possible V_{PP}, f_{IN} = 50 Hz or 100 Hz, Converter under test: SD24GAINx = 8				–110		
		Crosstalk source: SD24GAINx = 1, Sine-wave with maximum possible V_{PP}, f_{IN} = 50 Hz or 100 Hz, Converter under test: SD24GAINx = 16				–110		

(1) The following voltages are applied to the SD24 inputs:
$V_{I,A+}(t) = 0\ V + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
$V_{I,A-}(t) = 0\ V - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{IN,A+}(t) - V_{IN,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24 input range).

8.7.7.6 SD24 Performance, External Reference (SD24REFS = 0, SD24OSRx = 256)

external reference voltage is 1.2 V., over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD24GAINx = 1	f_{IN} = 50 Hz(1)	3 V		91		dB
		SD24GAINx = 2				90		
		SD24GAINx = 4				88		
		SD24GAINx = 8				83		
		SD24GAINx = 16				77		
THD	Total harmonic distortion	SD24GAINx = 1	f_{IN} = 50 Hz(1)	3 V		100		dB
		SD24GAINx = 8				95		
		SD24GAINx = 16				90		
SFDR	Spurious-free dynamic range	SD24GAINx = 1	f_{IN} = 50 Hz(1)	3 V		100		dB
		SD24GAINx = 8				95		
		SD24GAINx = 16				90		
INL	Integral nonlinearity, end-point fit	SD24GAINx: 1, 8, 16		3 V	–0.003		0.003	% FSR
G	Nominal gain	SD24GAINx = 1		3 V		1		
		SD24GAINx = 2				2		
		SD24GAINx = 4				4		
		SD24GAINx = 8				8		
		SD24GAINx = 16				16		
E_G	Gain error	SD24GAINx: 1, 2, 4, 8, 16		3 V	–1%		+1%	
$\Delta E_G/\Delta T$	Gain error temperature coefficient	SD24GAINx: 1, 8, 16		3 V			10	ppm/°C
E_{OS}	Offset error	SD24GAINx = 1		3 V			4	mV
		SD24GAINx = 16					2	
ΔEOS/ΔT	Offset error temperature coefficient	SD24GAINx = 1		3 V		±5	±25	ppm FSR/°C
		SD24GAINx = 16				±3	±10	
CMRR,50Hz	Common-mode rejection ratio at 50 Hz	SD24GAINx = 1, Common-mode input signal: V_{ID} = 928 mV, f_{IN} = 50 Hz		3 V		–55		dB
		SD24GAINx = 16, Common-mode input signal: V_{ID} = 58 mV, f_{IN} = 50 Hz				–60		
AC PSRR	AC power supply rejection ratio	SD24GAINx: 1, V_{CC} = 3 V ±50 mV × sin(2π × f_{VCC} × t), f_{VCC} = 50 Hz, Inputs grounded (no analog signal applied)		3 V		–90		dB
		SD24GAINx: 8, V_{CC} = 3 V ±50 mV × sin(2π × f_{VCC} × t), f_{VCC} = 50 Hz, Inputs grounded (no analog signal applied)		3 V		–95		
		SD24GAINx: 16, V_{CC} = 3 V ±50 mV × sin(2π × f_{VCC} × t), f_{VCC} = 50 Hz, Inputs grounded (no analog signal applied)		3 V		–95		
XT	Crosstalk between converters	Crosstalk source: SD24GAINx = 1, Sine-wave with maximum possible V_{PP}, f_{IN} = 50 Hz or 100 Hz, Converter under test: SD24GAINx = 1		3 V		–120		dB
		Crosstalk source: SD24GAINx = 1, Sine-wave with maximum possible V_{PP}, f_{IN} = 50 Hz or 100 Hz, Converter under test: SD24GAINx = 8				–110		
		Crosstalk source: SD24GAINx = 1, Sine-wave with maximum possible V_{PP}, f_{IN} = 50 Hz or 100 Hz, Converter under test: SD24GAINx = 16				–110		

(1) The following voltages are applied to the SD24 inputs:
$V_{I,A+}(t) = 0\ V + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
$V_{I,A-}(t) = 0\ V - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{IN,A+}(t) - V_{IN,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24 input range).

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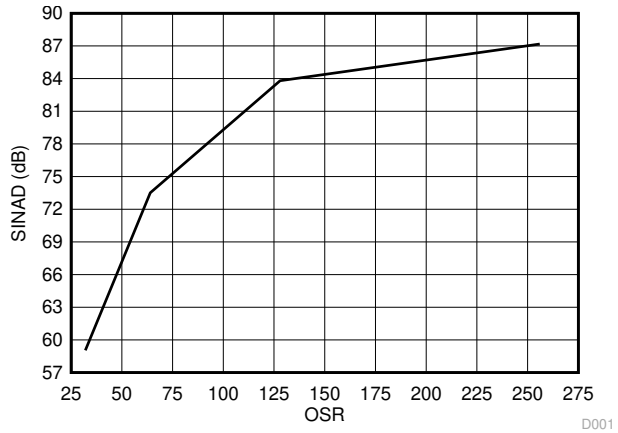
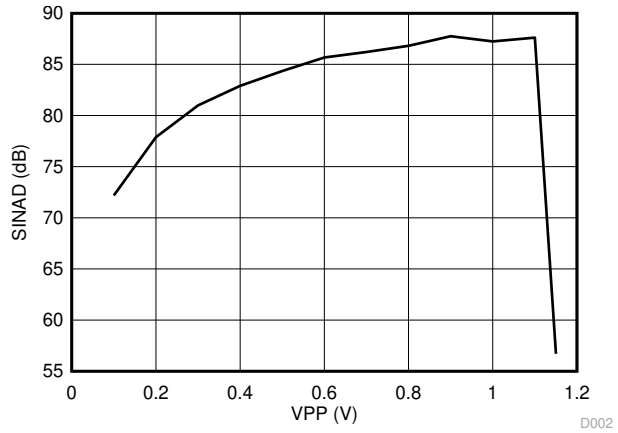
8.7.7.7 Typical Characteristics



A. f_{SD24} = 1.024 MHz SD24REFS = 1 SD24GAINx = 1

Figure 8-8. SINAD vs OSR



A. f_{SD24} = 1.024 MHz SD24REFS = 1

OSR = 256 SD24GAINx = 1

Figure 8-9. SINAD vs VPP

8.7.8 eUSCI

8.7.8.1 eUSCI (UART Mode) Clock Frequency

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK Duty cycle = 50% ±10%		f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)			4	MHz

8.7.8.2 eUSCI (UART Mode) Deglitch Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t	UART receive deglitch time(1)	UCGLITx = 0	2.2 V, 3 V	8	15	20	ns
		UCGLITx = 1		30	50	60	
		UCGLITx = 2		50	70	100	
		UCGLITx = 3		70	100	150	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

8.7.8.3 eUSCI (SPI Master Mode) Clock Frequency

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, Duty cycle = 50% ±10%		f_{SYSTEM}	MHz

8.7.8.4 eUSCI (SPI Master Mode) Timing

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10	2.2 V, 3 V	150		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10	2.2 V, 3 V	200		ns
$t_{STE,ACC}$	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V		40	ns
			3 V		30	
$t_{STE,DIS}$	STE disable time, STE inactive to SIMO high impedance	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V		40	ns
			3 V		30	
$t_{SU,MI}$	SOMI input data setup time		2.2 V	50		ns
			3 V	30		
$t_{HD,MI}$	SOMI input data hold time		2.2 V, 3 V	0		ns
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V		7	ns
			3 V		5	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	2.2 V, 3 V	0		ns

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, refer to the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 8-10 and Figure 8-11.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. Refer to the timing diagrams in Figure 8-10 and Figure 8-11.

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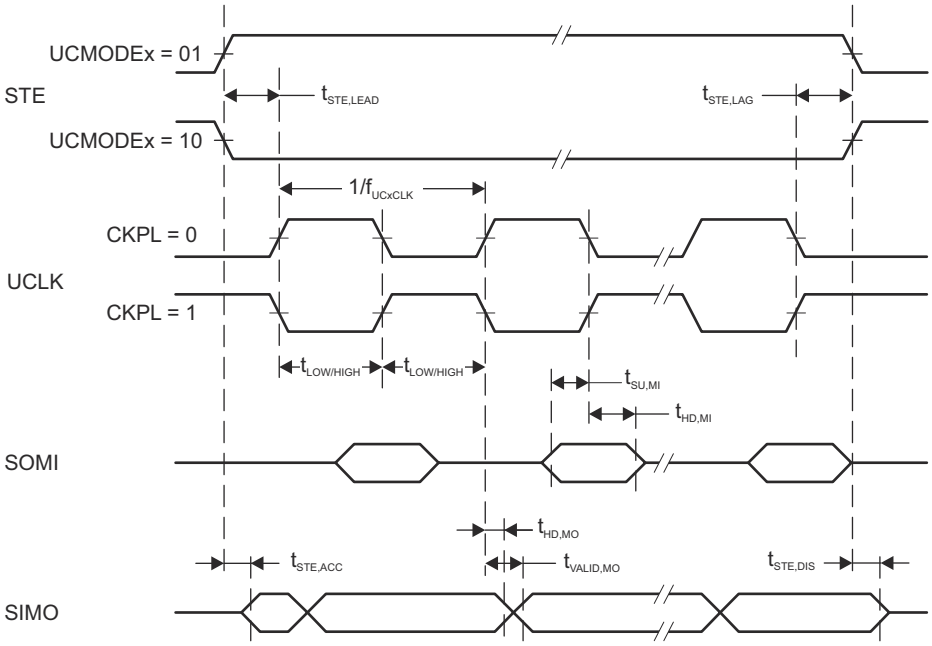

Figure 8-10. SPI Master Mode, CKPH = 0

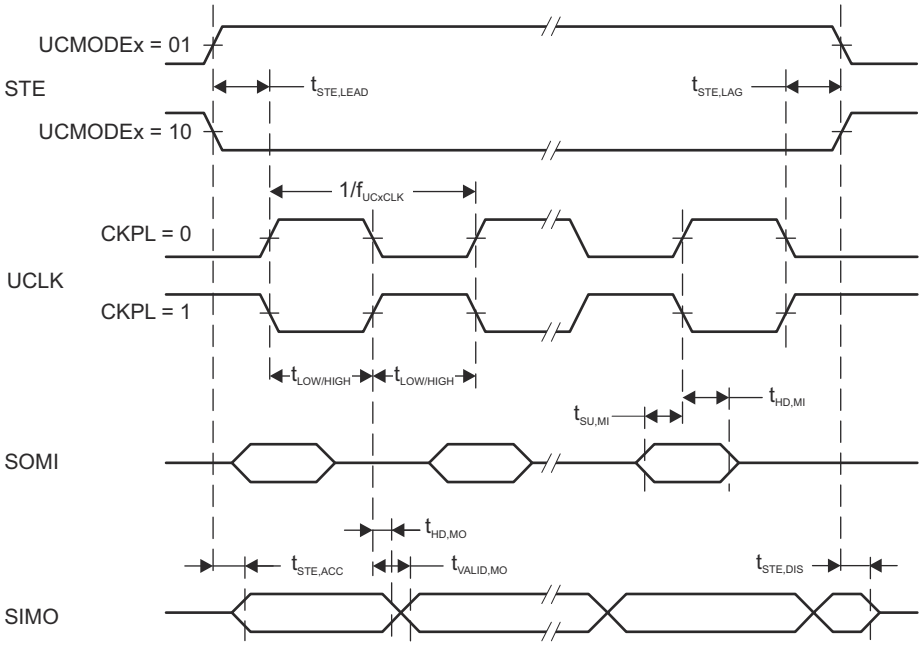

Figure 8-11. SPI Master Mode, CKPH = 1

8.7.8.5 eUSCI (SPI Slave Mode) Timing

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		2.2 V, 3 V	3		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		2.2 V, 3 V	0		ns
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		2.2 V		35	ns
			3 V		25	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		2.2 V, 3 V		35	ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V, 3 V	1		ns
$t_{HD,SI}$	SIMO input data hold time		2.2 V, 3 V	5		ns
$t_{VALID,SO}$	SOMI output data valid time[2]	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		35	ns
			3 V		25	
$t_{HD,SO}$	SOMI output data hold time[3]	C_L = 20 pF	2.2 V	35		ns
			3 V	25		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, refer to the SPI parameters of the attached master.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 8-12 and Figure 8-13.

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 8-12 and Figure 8-13.

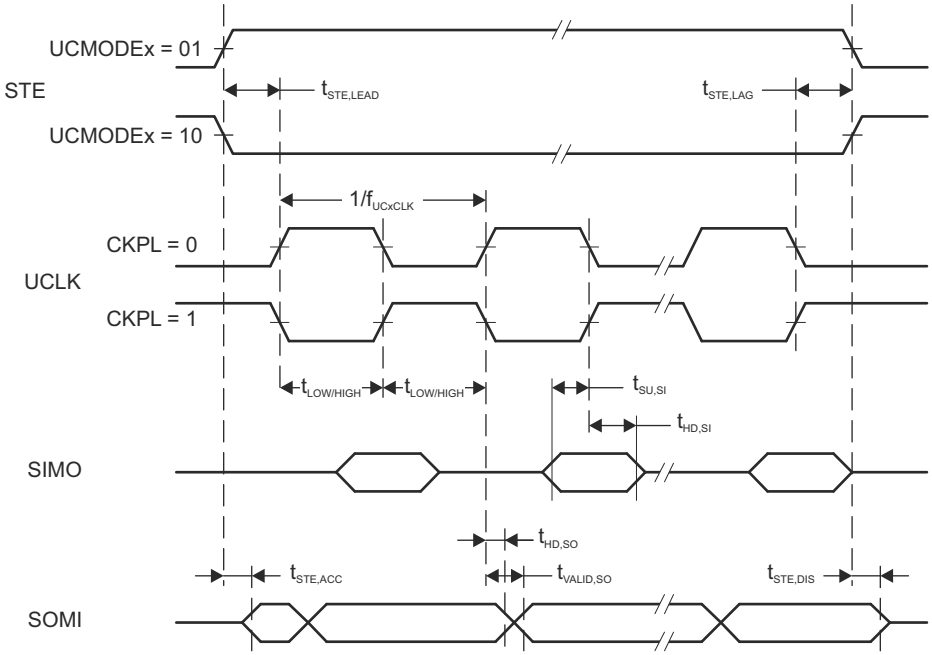

Figure 8-12. SPI Slave Mode, CKPH = 0

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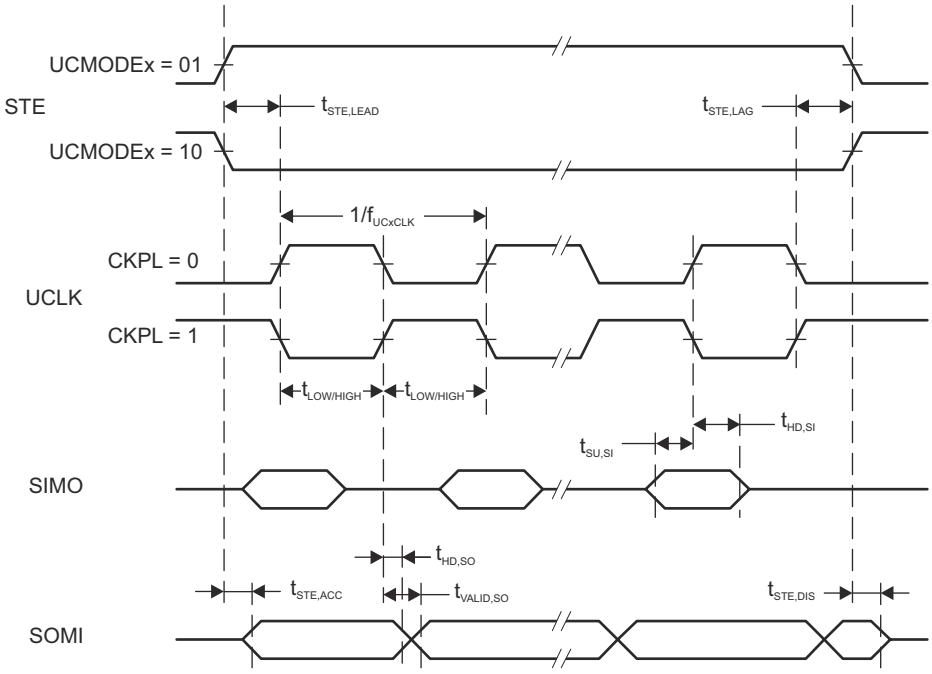

Figure 8-13. SPI Slave Mode, CKPH = 1

8.7.8.6 eUSCI (I²C Mode) Timing

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 8-14)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	2.2 V, 3 V	4.8			µs
		f_{SCL} > 100 kHz		1.2			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	2.2 V, 3 V	4.9			µs
		f_{SCL} > 100 kHz		1.26			
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0.12			µs
$t_{SU,DAT}$	Data setup time	f_{SCL} = 100 kHz	2.2 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz		1.08			
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	2.2 V, 3 V	4.9			µs
		f_{SCL} > 100 kHz		1.18			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	2.2 V, 3 V	75	110	160	ns
		UCGLITx = 1		35	50	80	
		UCGLITx = 2		15	25	40	
		UCGLITx = 3		10	15	20	
$t_{TIMEOUT}$	Clock low timeout	UCCLTOx = 1	2.2 V, 3 V		33		ms
		UCCLTOx = 2			37		
		UCCLTOx = 3			41		

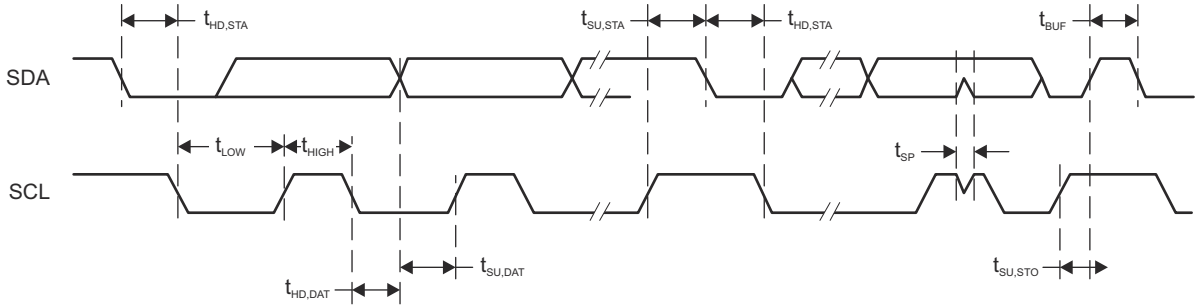

Figure 8-14. I²C Mode Timing

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8.7.9 Timer_A

8.7.9.1 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK External: TACLK	3.0 V			16.384	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture	3.0 V	20			ns

8.7.10 Flash

8.7.10.1 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V, 3.6 V			8	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V, 3.6 V			13	mA
t_{CPT}	Cumulative program time(1)		2.2 V, 3.6 V			8	ms
	Program and erase endurance			20000			cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	(2)			25		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word	(2)			20		
$t_{Block, 1-63}$	Block program time for each additional byte or word	(2)			11		
$t_{Block, End}$	Block program end-sequence wait time	(2)			6		
$t_{Mass\ Erase}$	Mass erase time	(2)			10593		
$t_{Seg\ Erase}$	Segment erase time	(2)			9628		

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word-write mode, individual byte-write mode, and block-write mode.

(2) These values are hardwired into the state machine of the flash controller ($t_{FTG} = 1/f_{FTG}$).

8.7.11 Emulation and Debug

8.7.11.1 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	3.0 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	3.0 V	0.025		15	µs
$t_{SBW, En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)(1)	3.0 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time	3.0 V	15		100	µs
f_{TCK}	TCK input frequency, 4-wire JTAG(2)	3.0 V	0		10	MHz
$R_{internal}$	Internal pulldown resistance on TEST	3.0 V	45	60	80	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the minimum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

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9 Detailed Description

9.1 Overview

The MSP430i204x, MSP430i203x, MSP430i202x devices consist of a powerful 16-bit RISC CPU, a DCO-based clock system that generates system clocks, a power-management module (PMM) with built-in voltage reference and voltage monitor, two to four 24-bit sigma-delta analog-to-digital converters (ADCs), a temperature sensor, a 16-bit hardware multiplier, two 16-bit timers, one eUSCI-A module and one eUSCI-B module, a watchdog timer (WDT), and up to 16 I/O pins.

9.2 Functional Block Diagrams

Figure 9-1 shows the functional block diagram for the MSP430i2041 and MSP430i2040 in the RHB package.

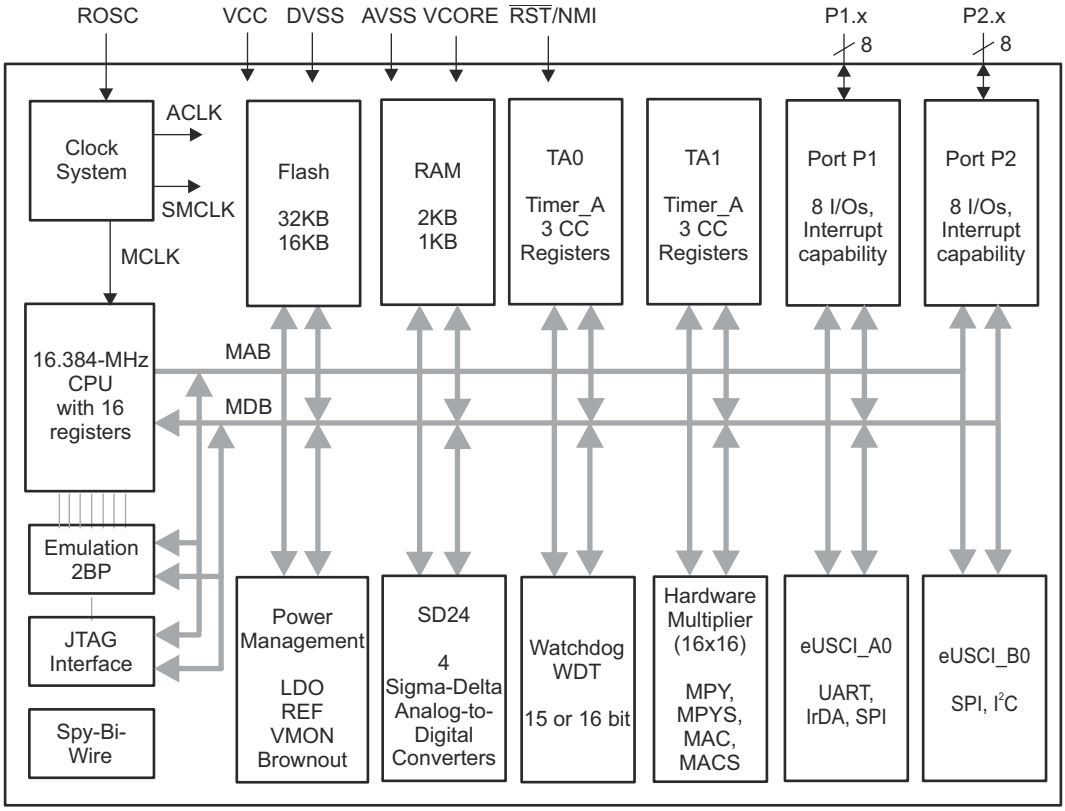

Figure 9-1. Functional Block Diagram – RHB Package – MSP430i2041, MSP430i2040

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Figure 9-2 shows the functional block diagram for the MSP430i2041 and MSP430i2040 in the PW package.

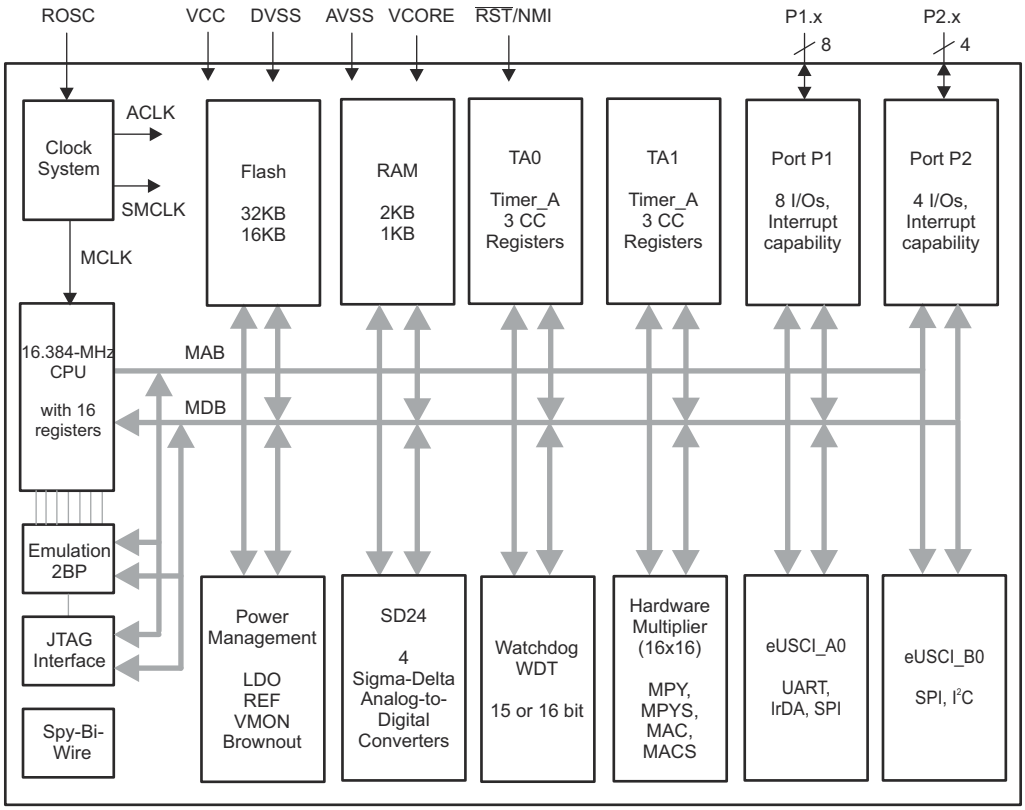

Figure 9-2. Functional Block Diagram – PW Package – MSP430i2041, MSP430i2040

Figure 9-3 shows the functional block diagram for the MSP430i2031 and MSP430i2030 in the RHB package.

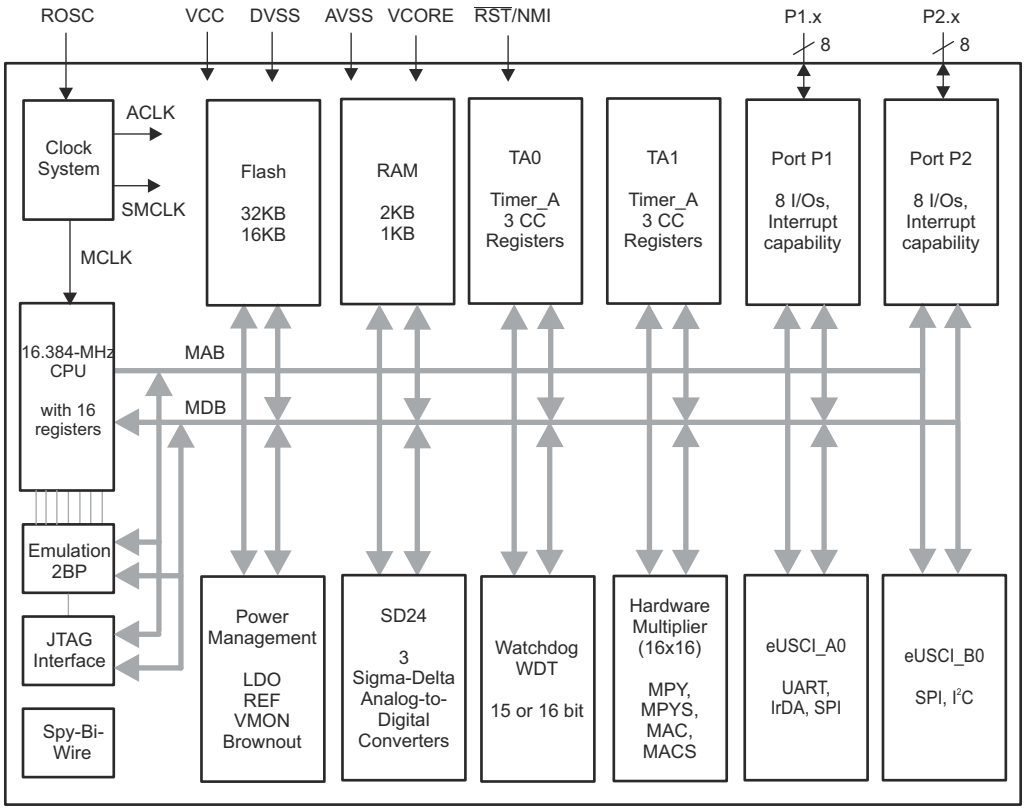

Figure 9-3. Functional Block Diagram – RHB Package – MSP430i2031, MSP430i2030

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Figure 9-4 shows the functional block diagram for the MSP430i2031 and MSP430i2030 in the PW package.

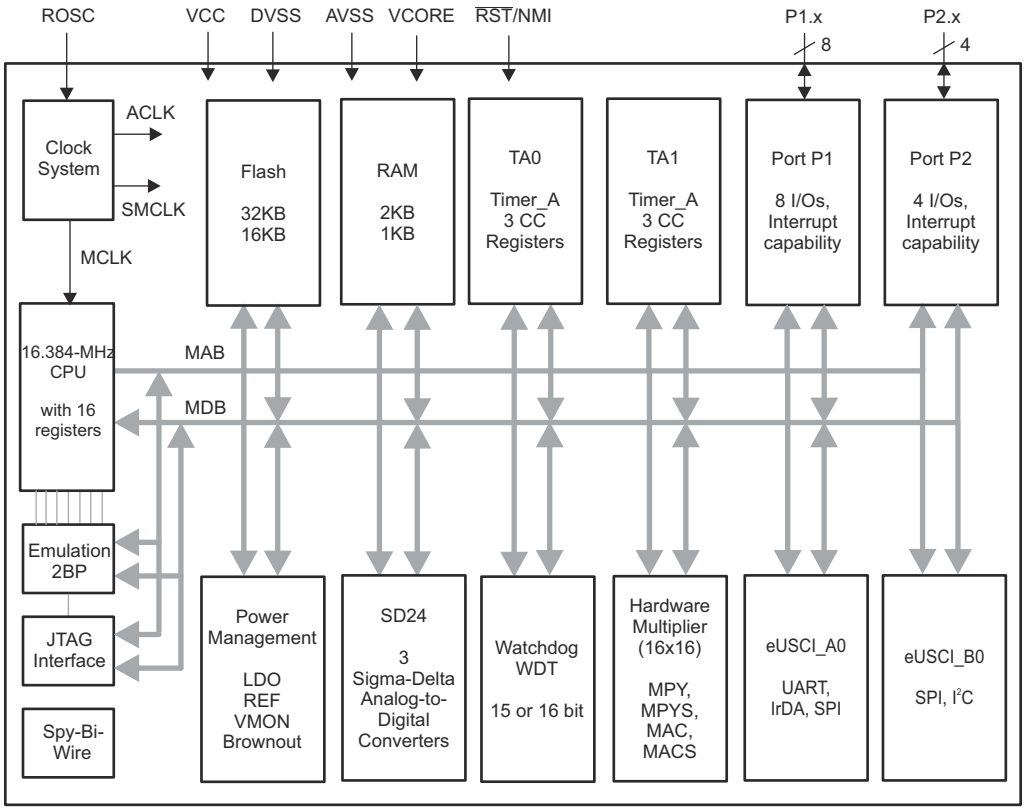

Figure 9-4. Functional Block Diagram – PW Package – MSP430i2031, MSP430i2030

Figure 9-5 shows the functional block diagram for the MSP430i2021 and MSP430i2020 in the RHB package.

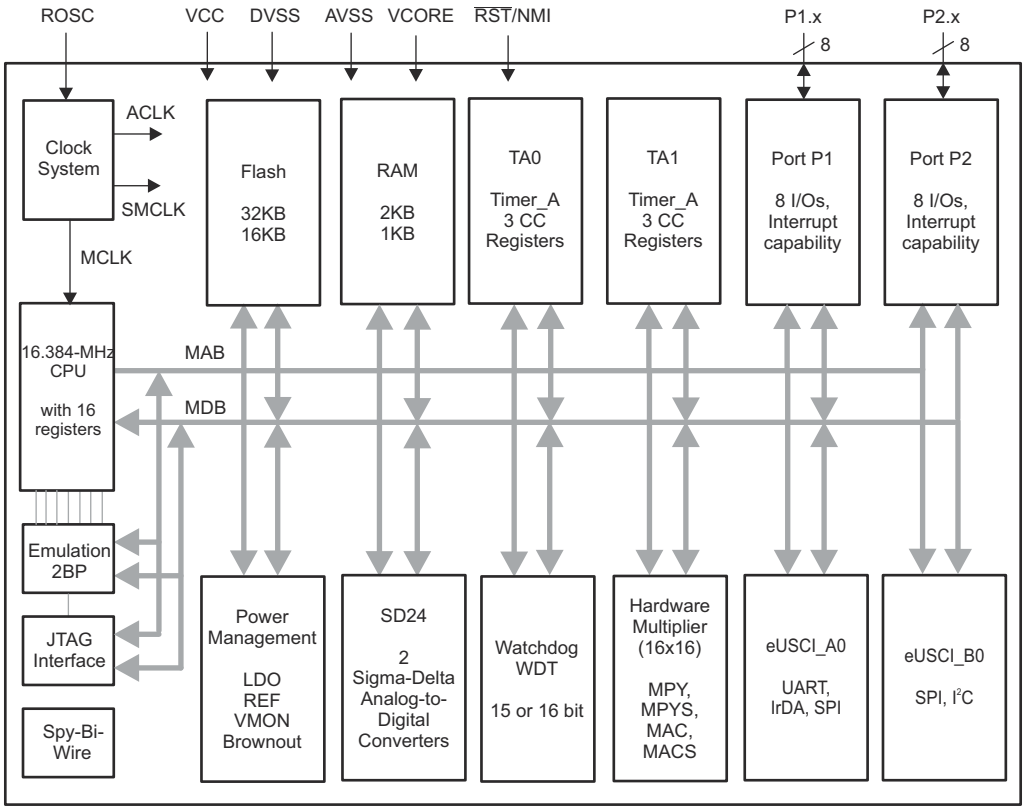

Figure 9-5. Functional Block Diagram – RHB Package – MSP430i2021, MSP430i2020

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Figure 9-6 shows the functional block diagram for the MSP430i2021 and MSP430i2020 in the PW package.

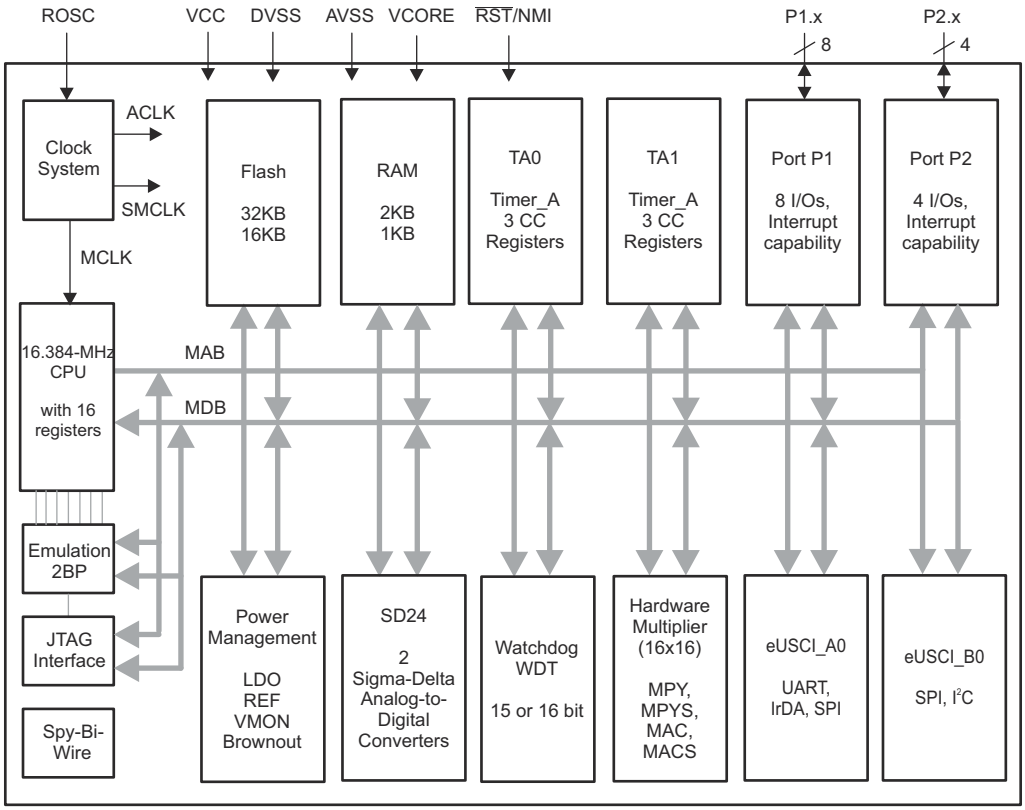

Figure 9-6. Functional Block Diagram – PW Package – MSP430i2021, MSP430i2020

9.3 CPU

The MSP430i CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers (see Figure 9-7).

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

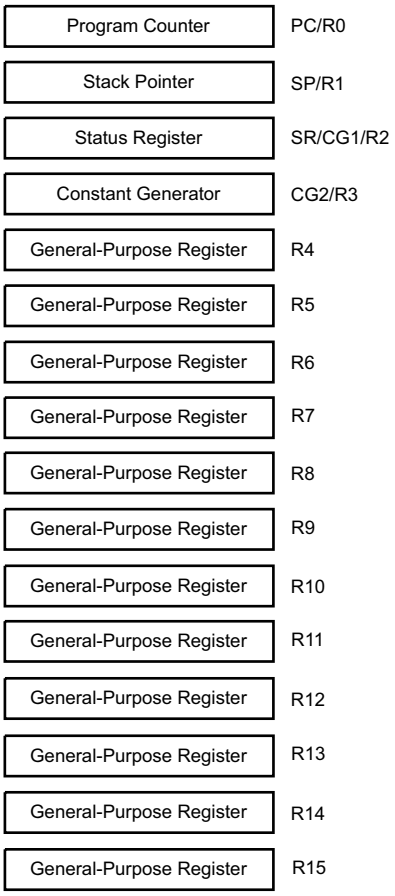

Figure 9-7. CPU Registers

CAUTION

The CPU will lock up if the device enters a low-power mode (CPU off) within 64 cycles after reset.

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9.4 Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 9-1 gives examples of the three types of instruction formats; Table 9-2 lists the address modes.

Table 9-1. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source and destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, unconditional or conditional	JNE	Jump-on-equal bit = 0

Table 9-2. Address Mode Descriptions

ADDRESS MODE	S (1)	D (2)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source

(2) D = destination

9.5 Operating Modes

MSP430i204x, MSP430i203x, MSP430i202x devices have one active mode and four software-selectable low-power modes. An interrupt event can wake up the device from the low-power modes LPM0 to LPM4, service the request, and restore back to the low-power mode on return from the interrupt program.

The following five operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 or low-power mode 1 (LPM0 = LPM1)
  - CPU is disabled
  - Internal regulator remains enabled
  - DCO remains enabled
  - MCLK is disabled
  - ACLK and SMCLK remain active
- Low-power mode 2 or low-power mode 3 (LPM2 = LPM3)
  - CPU is disabled
  - Internal regulator remains enabled
  - DCO remains enabled
  - MCLK and SMCLK are disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - Internal regulator remains enabled
  - DCO is disabled
  - MCLK, SMCLK, and ACLK are disabled
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator is disabled
  - No RAM retention
  - I/O pad state retention
  - Wake from $\overline{\text{RST}}$/NMI, ports pins P2.1 or P2.2

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9.6 Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are in the address range 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed), the CPU goes into LPM4 immediately after power up.

Table 9-3. Interrupt Vector Addresses

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power up External reset Watchdog Flash key violation PC out-of-range (1)	BORIFG RSTIFG WDTIFG KEYV (2)	Reset	0FFFEh	15, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (2) (4)	(Non)maskable, (Non)maskable, (Non)maskable	0FFFCh	14
Timer TA1	TA1CCR0 CCIFG (3)	Maskable	0FFFAh	13
Timer TA1	TA1CCR1 CCIFG, TA1CCR2 CCIFG, TA1CTL TAIFG (2) (3)	Maskable	0FFF8h	12
Voltage monitor	VMONIFG	Maskable	0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
eUSCI_A0 receive or transmit	UCA0RXIFG, UCA0TXIFG	Maskable	0FFF2h	9
eUSCI_B0 receive or transmit	UCB0RXIFG, UCB0TXIFG	Maskable	0FFF0h	8
SD24	SD24CCTLx SD24OVIFG, SD24CCTLx SD24IFG(2) (3)	Maskable	0FFEEh	7
Timer TA0	TA0CCR0 CCIFG (3)	Maskable	0FFECh	6
Timer TA0	TA0CCR1 CCIFG, TA0CCR2 CCIFG, TA0CTL TAIFG (2) (3)	Maskable	0FFEAh	5
I/O port P1	P1IFG.0 to P1IFG.7 (2) (3)	Maskable	0FFE8h	4
			0FFE6h	3
			0FFE4h	2
I/O port P2	P2IFG.0 to P2IFG.7 (2) (3)	Maskable	0FFE2h	1
			0FFE0h	0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address range.

(2) Multiple source flags

(3) Interrupt flags are in the module.

(4) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.

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9.7 Special Function Registers

Some interrupt enable and interrupt flag bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend

rw	Bit can be read and written.
rw-0, rw-1	Bit can be read and written. It is Reset or Set by PUC.
rw-(0), rw-(1)	Bit can be read and written. It is Reset or Set by POR.
rw-[0], rw-[1]	Bit can be read and written. It is Reset or Set by BOR.
	SFR bit is not present in device.

Table 9-4. Interrupt Enable 1 (Address = 00h)

7	6	5	4	3	2	1	0
		ACCVIE	NMIIE			OFIE	WDTIE
		rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
OFIE	Oscillator fault interrupt enable
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Table 9-5. Interrupt Flag Register 1 (Address = 02h)

7	6	5	4	3	2	1	0
			NMIIFG	RSTIFG	BORIFG	OFIFG	WDTIFG
			rw-0	rw-[0]	rw-[1]	rw-0	rw-(0)

WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.
OFIFG	Flag set on oscillator fault. This flag can be cleared by software when the oscillator runs free of fault.
BORIFG	Brown out reset flag. This bit is set after V_{CC} power up and can be cleared by software.
RSTIFG	External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power up.
NMIIFG	Set by the $\overline{RST}$/NMI pin in NMI configuration.

9.8 Flash Memory

The flash memory can be programmed through the Spy-Bi-Wire or JTAG port, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory:

- Flash memory has n segments of main memory and one segment of information memory.
- Segment size is 1KB for both main memory and information memory.
- Segments 0 to n in main memory can be erased in one step, or each segment may be individually erased.
- Information memory segment can be erased separately or as a group with main memory segments 0 to n.
- Information memory segment contains calibration data. After reset, information memory segment is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

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9.9 JTAG Operation

9.9.1 JTAG Standard Interface

The MSP430i family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430i development tools and device programmers. Table 9-6 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the MSP430 Hardware Tools User's Guide.

Table 9-6. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
P1.0/UCA0STE/MCLK/TCK	IN	JTAG clock input
P1.1/UCA0CLK/SMCLK/TMS	IN	JTAG state control
P1.2/UCA0RXD/UCA0SOMI/ACLK/TDI/TCLK	IN	JTAG data input/TCLK input
P1.3/UCA0TXD/UCA0SIMO/TA0CLK/TDO/TDI	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$/NMI/SBWTDIO	IN	External reset
VCC		Power supply
DVSS		Ground supply

9.9.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430i family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430i development tools and device programmers. Table 9-7 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the MSP430 Hardware Tools User's Guide.

Table 9-7. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
DVSS		Ground supply

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9.9.3 JTAG Disable Register

The SYSJTAGDIS register can disable the JTAG port to provide code protection and device security. JTAG is disabled when software writes the value 0xA5A5 to this register within 64 MCLK clock cycles after a BOR or POR reset; otherwise, the JTAG port is enabled. Any writes to this register after the first 64 MCLK clock cycles are ignored. Reads from this register at any time return the JTAG enable or disable status. The value 0xA5A5 indicates that JTAG is disabled, and 0x9696 indicates that JTAG is enabled. The SYSJTAGDIS register is mapped to address 01FEh.

Note

Application programming the device to any of the low power modes within first 64 MCLK clock cycles after a BOR or POR reset will lock the device for any JTAG/SBW access.

Table 9-8. SYSJTAGDIS Register

15	14	13	12	11	10	9	8
JTAGKEY							
rw-[1]	rw-[0]	rw-[1]	rw-[0]	rw-[0]	rw-[1]	rw-[0]	rw-[1]
7	6	5	4	3	2	1	0
JTAGKEY							
rw-[1]	rw-[0]	rw-[1]	rw-[0]	rw-[0]	rw-[1]	rw-[0]	rw-[1]

JTAGKEY 0xA5A5 indicates JTAG is disabled and 0x9696 indicates JTAG is enabled.

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9.10 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. The peripherals can be managed using all instructions. For complete module descriptions, see the MSP430i2xx Family User's Guide.

9.10.1 Clock System

The clock system consists of a fixed 16.384-MHz frequency internal DCO. The DCO can operate in internal resistor mode or external resistor mode. The DCO clock accuracy is higher when operating in external resistor mode especially upon variation in operating temperature. This feature can be useful in applications like utility metering in which accurate clock is necessary under varying operating temperature. When external resistor mode is selected by application, the resistor of recommended value must be connected to ROSC pin of the device. Refer to Section 8.7.2.1 for the recommended value of the resistor at the ROSC pin. TI recommends connecting the ROSC pin to AVSS when operating the DCO in internal resistor mode. When a resistor fault is detected in the external resistor mode, the DCO automatically switches to the internal resistor mode as a fail-safe mechanism to keep the system clocks active.

The DCO can be completely bypassed and the system clocks can be sourced by an external digital clock. The clock system generates MCLK, SMCLK, and ACLK. MCLK is used by the CPU, while SMCLK and ACLK are used by the peripheral modules. There are programmable clock dividers for MCLK and SMCLK. ACLK runs at a fixed 32-kHz frequency. The clock system supports active mode and four low-power modes.

9.10.2 Power-Management Module (PMM)

The PMM consists of voltage regulator that generates 1.8-V regulated core voltage. There is a brownout reset (BOR) circuit on the high-voltage domain, and a supply voltage supervisor (SVS) module on the low-voltage domain. The BOR and SVS provide the proper internal reset signal to the device during power on and power off.

A built-in voltage reference is used by submodules of the PMM and by the analog modules on the device. A temperature sensor is also available in the built-in voltage reference.

The voltage monitor (VMON) on the high-voltage domain can monitor external voltage on the VMONIN pin against the internal reference voltage or by comparing the on-chip V_{CC} to one of three programmable threshold voltages. During the LPM4.5 mode, the reference, voltage regulator, temperature sensor, and voltage monitor are turned off, and only the high-side brownout circuit is active.

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9.10.3 Digital I/O

Two 8-bit I/O ports (P1 and P2) are implemented on the MSP430i204x, MSP430i203x, MSP430i202x devices. On 32-pin RHB devices, ports P1 and P2 are complete, and 16 I/Os are available. On 28-pin PW devices, port P2 is reduced to 4 bits, and 12 I/Os are available. On 28-pin PW devices, the unavailable pins (P2.4 to P2.7) must be programmed to port function, output direction, and be driven with value 0.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all 8 bits of port P1 and P2
- LPM4.5 wake-up capability for Port pins P2.1 and P2.2
- Read and write access to port-control registers is supported by all instructions.

9.10.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

9.10.5 Timer TA0

Timer TA0 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing (see Table 9-9). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 9-9. TA0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P1.3	TA0CLK	TACLK	Timer	NA	NA	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P1.3	$\overline{\text{TA0CLK}}$	INCLK				
P1.4	TA0.0	CCI0A	CCR0	TA0	TA0.0	P1.4
P2.5	TA0.0	CCI0B				P2.5
	DVSS	GND				
	VCC	VCC				
P1.5	TA0.1	CCI1A	CCR1	TA1	TA0.1	P1.5
	ACLK (internal)	CCI1B				P2.6
	DVSS	GND				
	VCC	VCC				
P1.6	TA0.2	CCI2A	CCR2	TA2	TA0.2	P1.6
	TA1 CCR2 output (internal)	CCI2B				P2.7
	DVSS	GND			TA1 CCI2B input	
	VCC	VCC				

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9.10.6 Timer TA1

Timer TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 can support multiple capture/compares, PWM outputs, and interval timing (see Table 9-10). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 9-10. TA1 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P1.7	TA1CLK	TACLK	Timer	NA	NA	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P1.7	$\overline{\text{TA1CLK}}$	INCLK				
P2.0	TA1.0	CCI0A	CCR0	TA0	TA1.0	P2.0
P2.4	TA1.0	CCI0B				P2.4
	DVSS	GND				
	VCC	VCC				
P2.1	TA1.1	CCI1A	CCR1	TA1	TA1.1	P2.1
	ACLK (internal)	CCI1B				
	DVSS	GND				
	VCC	VCC				
P2.2	TA1.2	CCI2A	CCR2	TA2	TA1.2	P2.2
	TA0 CCR2 output (internal)	CCI2B				
	DVSS	GND			TA0 CCI2B input	
	VCC	VCC				

9.10.7 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI module is used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA.

The eUSCI_An module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3-pin or 4-pin) and I^2C.

One eUSCI_A and one eUSCI_B module are implemented on MSP430i20xx devices.

9.10.8 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16-bit, 16×8-bit, 8×16-bit, and 8×8-bit operations. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

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9.10.9 SD24

There are up to four independent 24-bit sigma-delta ADCs. Each converter is designed with a fully differential analog input pair and programmable gain amplifier input stage. Also the converters are based on second-order oversampling sigma-delta modulators and digital decimation filters. The decimation filters are comb-type filters with selectable oversampling ratios of up to 256.

The SD24 converters can operate with internal reference (SD24REFS = 1) or with external reference (SD24REFS = 0). When SD24 operates with internal reference the VREF pin must not be loaded externally. Connect only the recommended capacitor value (C_{VREF}) at VREF pin to AVSS (see Section 8.7.7.2).

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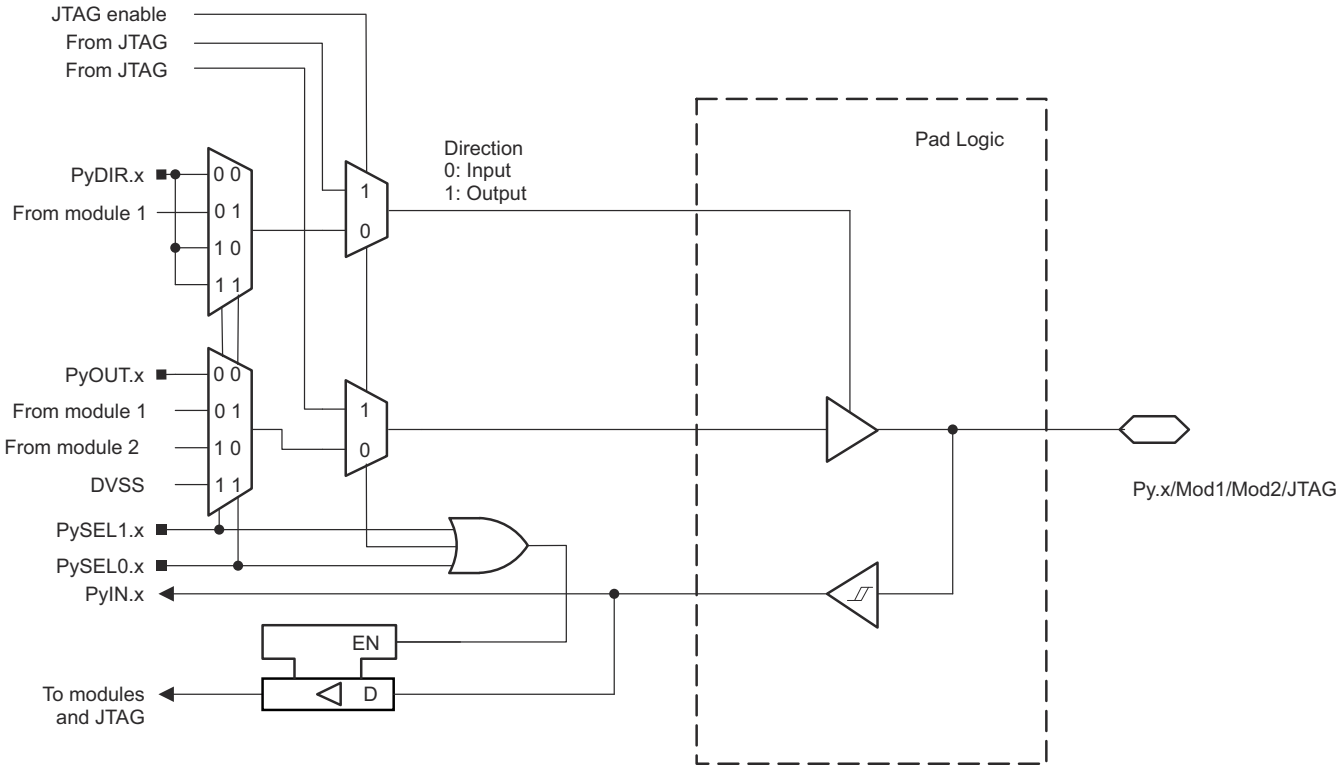
9.11 Input/Output Diagrams

9.11.1 Port P1, P1.0 to P1.3, Input/Output With Schmitt Trigger

Figure 9-8 shows the pin diagram. Table 9-11 summarizes the selection of the pin function.



Functional representation only.

Figure 9-8. Py.x/Mod1/Mod2/JTAG Pin Diagram

Table 9-11. Port P1 (P1.0 to P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]			
			P1DIR.x	P1SEL1.x	P1SEL0.x	JTAG Enable
P1.0/UCA0STE/MCLK/TCK	0	P1.0 (I/O)[2]	I: 0; O: 1	0	0	0
		UCA0STE	X[3]	0	1	0
		N/A	0	1	0	0
		MCLK	1			
		N/A	0	1	1	0
		DVSS	1			
		TCK[4]	X	X	X	1
P1.1/UCA0CLK/SMCLK/TMS	1	P1.1 (I/O)[2]	I: 0; O: 1	0	0	0
		UCA0CLK	X[3]	0	1	0
		N/A	0	1	0	0
		SMCLK	1			
		N/A	0	1	1	0
		DVSS	1			
		TMS[4]	X	X	X	1
P1.2/UCA0RXD/UCA0SOMI/ACLK/TDI/TCLK	2	P1.2 (I/O)[2]	I: 0; O: 1	0	0	0
		UCA0RXD/UCA0SOMI	X[3]	0	1	0
		N/A	0	1	0	0
		ACLK	1			
		N/A	0	1	1	0
		DVSS	1			
		TDI/TCLK[4]	X	X	X	1
P1.3/UCA0TXD/UCA0SIMO/TA0CLK/TDO/TDI	3	P1.3 (I/O)[2]	I: 0; O: 1	0	0	0
		UCA0TXD/UCA0SIMO	X[3]	0	1	0
		TA0CLK	0	1	0	0
		DVSS	1			
		N/A	0	1	1	0
		DVSS	1			
		TDO/TDI[4]	X	X	X	1

(1) X = Don't care
(2) Default condition
(3) Direction is controlled by eUSCI_A0 module.
(4) The pin direction is controlled by the JTAG module. The JTAG mode selection is made through the Spy-Bi-Wire 4-wire entry sequence. Neither P1SEL0.x and P1SEL1.x nor P1DIR.x have an effect in these cases.

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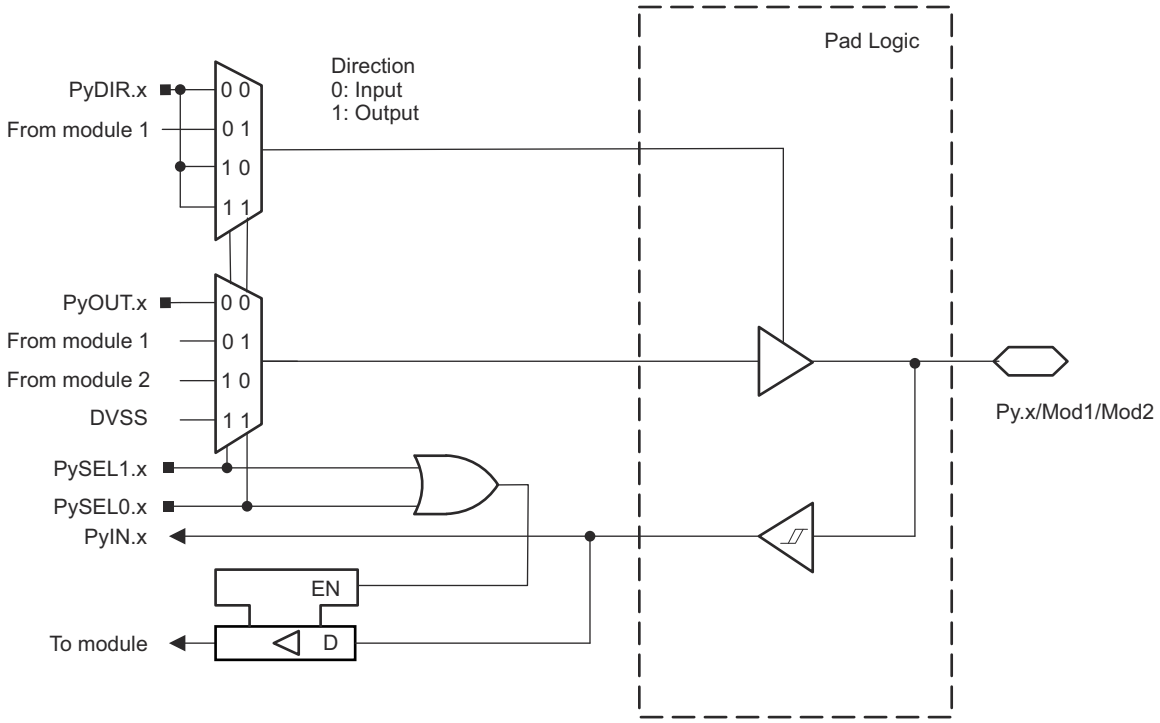
9.11.2 Port P1, P1.4 to P1.7, Input/Output With Schmitt Trigger

Figure 9-9 shows the pin diagram. Table 9-12 summarizes the selection of the pin function.



Functional representation only.

Figure 9-9. Py.x/Mod1/Mod2 Pin Schematic

Table 9-12. Port P1 (P1.4 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.4/UCB0STE/TA0.0	4	P1.4 (I/O)	I: 0; O: 1	0	0
		UCB0STE	X[2]	0	1
		TA0.CCI0A	0	1	0
		TA0.0	1		
		N/A	0	1	1
		DVSS	1		
P1.5/UCB0CLK/TA0.1	5	P1.5 (I/O)	I: 0; O: 1	0	0
		UCB0CLK	X[2]	0	1
		TA0.CCI1A	0	1	0
		TA0.1	1		
		N/A	0	1	1
		DVSS	1		
P1.6/UCB0SCL/UCB0SOMI/ TA0.2	6	P1.6 (I/O)	I: 0; O: 1	0	0
		UCB0SCL/UCB0SOMI	X[2]	0	1
		TA0.CCI2A	0	1	0
		TA0.2	1		
		N/A	0	1	1
		DVSS	1		
P1.7/UCB0SDA/UCB0SIMO/ TA1CLK	7	P1.7 (I/O)	I: 0; O: 1	0	0
		UCB0SDA/UCB0SIMO	X[2]	0	1
		TA1CLK	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

(1) X = Don't care

(2) Direction is controlled by eUSCI_B0 module.

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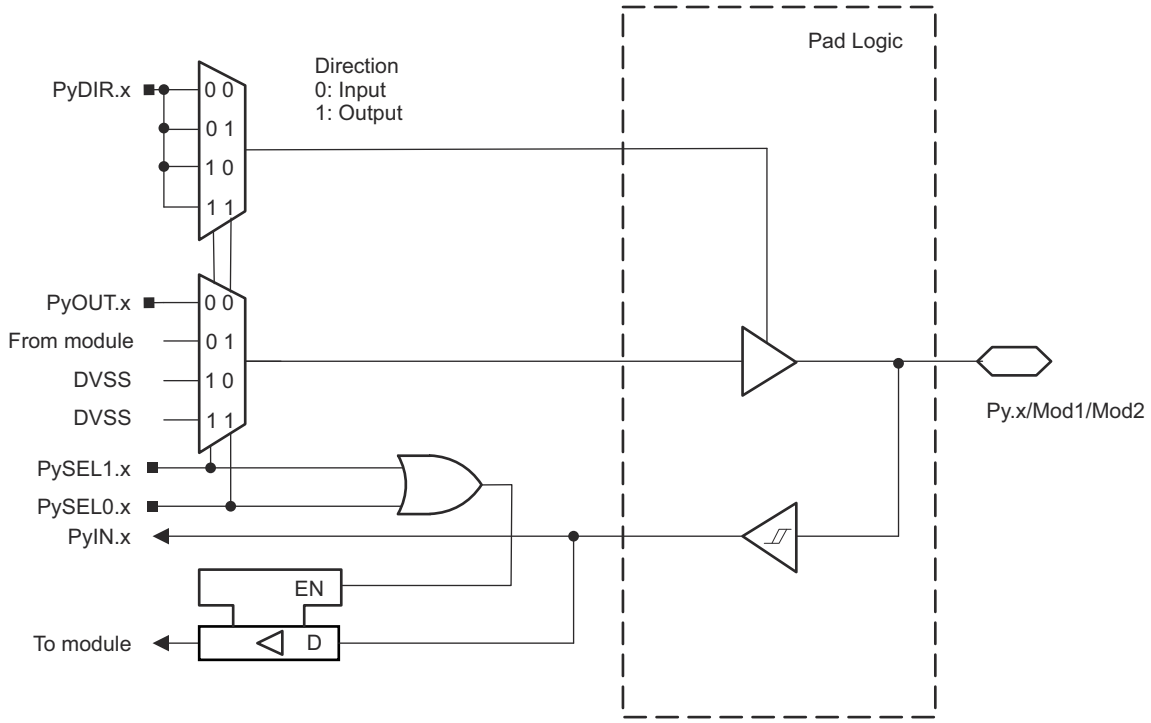
9.11.3 Port P2, P2.0 to P2.2 and P2.4 to P2.7, Input/Output With Schmitt Trigger

Figure 9-10 shows the pin diagram. Table 9-13 summarizes the selection of the pin function.



Functional representation only.

Figure 9-10. Py.x/Mod1/Mod2 Pin Schematic

Table 9-13. Port P2 (P2.0 to P2.2 and P2.4 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.0/TA1.0/CLKIN	0	P2.0 (I/O)	I: 0; O: 1	0	0
		TA1.CCI0A	0	0	1
		TA1.0	1		
		CLKIN (DCO bypass clock)	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P2.1/TA1.1	1	P2.1 (I/O)	I: 0; O: 1	0	0
		TA1.CCI1A	0	0	1
		TA1.1	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

Table 9-13. Port P2 (P2.0 to P2.2 and P2.4 to P2.7) Pin Functions (continued)

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.2/TA1.2	2	P2.2 (I/O)	I: 0; O: 1	0	0
		TA1.CCI2A	0	0	1
		TA1.2	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P2.4/TA1.0[(1)]	4	P2.4 (I/O)	I: 0; O: 1	0	0
		TA1.CCI0B	0	0	1
		TA1.0	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P2.5/TA0.0[(1)]	5	P2.5 (I/O)	I: 0; O: 1	0	0
		TA0.CCI0B	0	0	1
		TA0.0	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P2.6/TA0.1[(1)]	6	P2.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		TA0.1	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P2.7/TA0.2[(1)]	7	P2.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		TA0.2	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

(1) Available only on 32-pin RHB devices.

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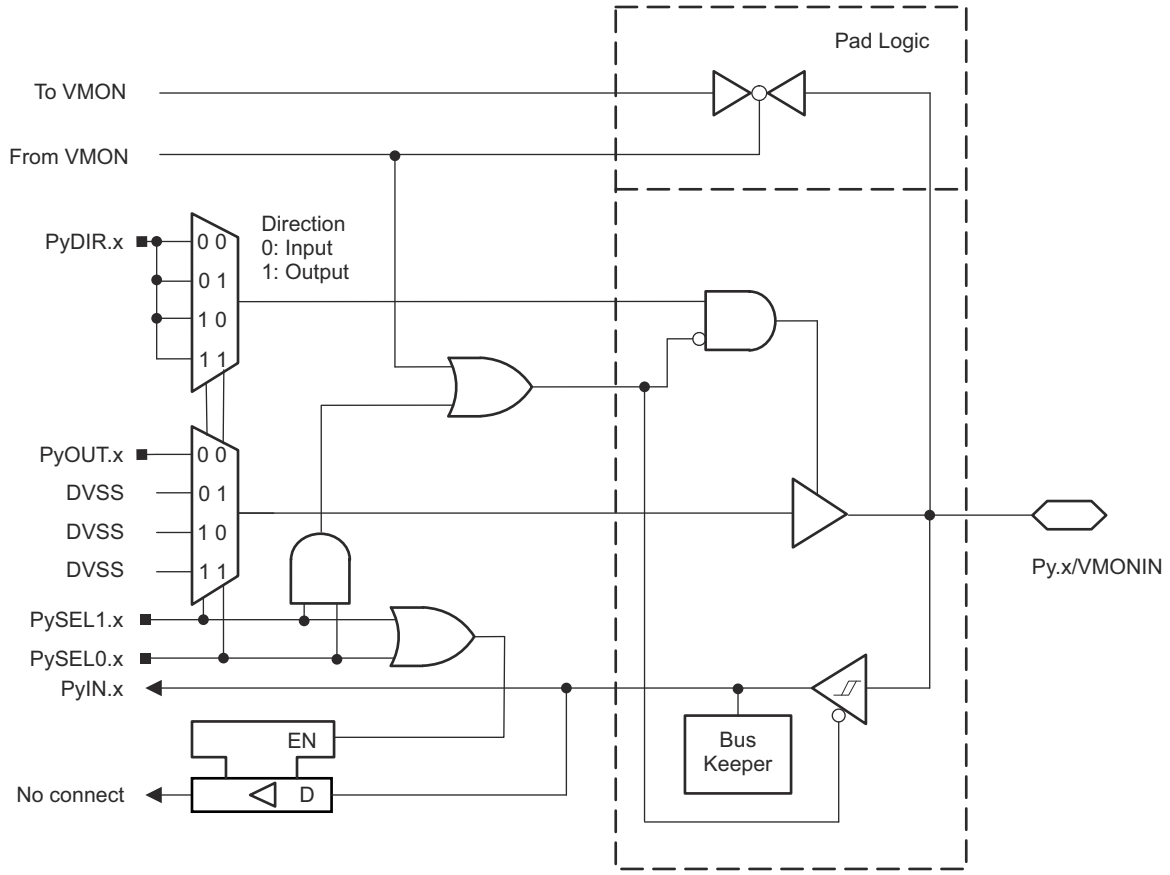
9.11.4 Port P2, P2.3, Input/Output With Schmitt Trigger

Figure 9-11 shows the pin diagram. Table 9-14 summarizes the selection of the pin function.



Functional representation only.

Figure 9-11. Py.x/VMONIN Pin Schematic

Table 9-14. Port P2 (P2.3) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.3/VMONIN	3	P2.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		VMONIN[2]	X	1	1

(1) X = Don't care

(2) Setting P2SEL1.3 and P2SEL0.3 disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying voltage at VMONIN pin. To enable the VMONIN function, VMONLVLx bits must be set to 3'b111 in the VMONCTL register.

9.12 Device Descriptor

Table 9-15 lists the contents of the tag-length-value (TLV) device descriptor structure for the MSP430i204x, MSP430i203x, and MSP430i202x devices.

Table 9-15. MSP430i204x, MSP430i203x, MSP430i202x TLV

DESCRIPTION		ADDRESS	SIZE (BYTES)	VALUE
Checksum	TLV checksum	013C0h	2	Per unit
Die Record	Die Record Tag	013C2h	1	01h
	Die Record Length	013C3h	1	0Ah
	Lot/Wafer ID	013C4h	4	Per unit
	Die X position	013C8h	2	Per unit
	Die Y position	013CAh	2	Per unit
	Test results	013CCh	2	Per unit
REF Calibration	REF Calibration Tag	013CEh	1	02h
	REF Calibration Length	013CFh	1	02h
	Calibrate REF – for REFCAL1 register	013D0h	1	Per unit
	Calibrate REF – for REFCAL0 register	013D1h	1	Per unit
DCO Calibration	DCO Calibration Tag	013D2h	1	03h
	DCO Calibration Length	013D3h	1	04h
	Calibrate DCO – for CSIRFCAL register	013D4h	1	Per unit
	Calibrate DCO – for CSIRTCAL register	013D5h	1	Per unit
	Calibrate DCO – for CSERFCAL register	013D6h	1	Per unit
	Calibrate DCO – for CSERTCAL register	013D7h	1	Per unit
SD24 Calibration	SD24 Calibration Tag	013D8h	1	04h
	SD24 Calibration Length	013D9h	1	02h
	Calibrate SD24 – for SD24TRIM register	013DAh	1	Per unit
	Empty	013DBh	1	FFh
Empty	Tag Empty	013DCh	1	FEh
	Empty Length	013DDh	1	22h
	Empty	013DEh	34	FFh

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9.13 Memory

Table 9-16 lists the memory organization for the specified devices.

Table 9-16. Memory Organization

		MSP430i2040 MSP430i2030 MSP430i2020	MSP430i2041 MSP430i2031 MSP430i2021
Memory	Size	16KB	32KB
Main: interrupt vector	Flash	0xFFFF to 0xFFE0	0xFFFF to 0xFFE0
Main: code memory	Flash	0xFFFF to 0xC000	0xFFFF to 0x8000
Information memory	Size	1KB	1KB
	Flash	0x13FFh to 0x1000	0x13FFh to 0x1000
RAM	Size	1KB	2KB
	Address	0x05FF to 0x0200	0x09FF to 0x0200
Peripherals	16-bit	0x01FF to 0x0100	0x01FF to 0x0100
	8-bit	0x00FF to 0x0010	0x00FF to 0x0010
	8-bit SFR	0x000F to 0x0000	0x000F to 0x0000

9.13.1 Peripheral File Map

Table 9-17 lists the peripherals that support word access, and Table 9-18 lists the peripherals that support byte access. Peripherals that support both access types are listed in both tables.

Table 9-17. Peripherals With Word Access

MODULE	REGISTER DESCRIPTION	ACRONYM	ADDRESS
SYS	JTAG disable register	SYSJTAGDIS	0x01FE
Timer TA1	Capture/compare register 2	TA1CCR2	0x0196
	Capture/compare register 1	TA1CCR1	0x0194
	Capture/compare register 0	TA1CCR0	0x0192
	Timer_A register	TA1R	0x0190
	Capture/compare control 2	TA1CCTL2	0x0186
	Capture/compare control 1	TA1CCTL1	0x0184
	Capture/compare control 0	TA1CCTL0	0x0182
	Timer_A control	TA1CTL	0x0180
	Timer_A interrupt vector	TA1IV	0x011E
Timer TA0	Capture/compare register 2	TA0CCR2	0x0176
	Capture/compare register 1	TA0CCR1	0x0174
	Capture/compare register 0	TA0CCR0	0x0172
	Timer_A register	TA0R	0x0170
	Capture/compare control 2	TA0CCTL2	0x0166
	Capture/compare control 1	TA0CCTL1	0x0164
	Capture/compare control 0	TA0CCTL0	0x0162
	Timer_A control	TA0CTL	0x0160
	Timer_A interrupt vector	TA0IV	0x012E

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Table 9-17. Peripherals With Word Access (continued)

MODULE	REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_A0	USCI_A control word 0	UCA0CTLW0	0x0140
	USCI _A control word 1	UCA0CTLW1	0x0142
	USCI_A baud rate 0	UCA0BR0	0x0146
	USCI_A baud rate 1	UCA0BR1	0x0147
	USCI_A modulation control	UCA0MCTLW	0x0148
	USCI_A status	UCA0STAT	0x014A
	USCI_A receive buffer	UCA0RXBUF	0x014C
	USCI_A transmit buffer	UCA0TXBUF	0x014E
	USCI_A LIN control	UCA0ABCTL	0x0150
	USCI_A IrDA transmit control	UCA0IRTCTL	0x0152
	USCI_A IrDA receive control	UCA0IRRCTL	0x0153
	USCI_A interrupt enable	UCA0IE	0x015A
	USCI_A interrupt flags	UCA0IFG	0x015C
	USCI_A interrupt vector word	UCA0IV	0x015E
eUSCI_B0	USCI_B control word 0	UCB0CTLW0	0x01C0
	USCI_B control word 1	UCB0CTLW1	0x01C2
	USCI_B bit rate 0	UCB0BR0	0x01C6
	USCI_B bit rate 1	UCB0BR1	0x01C7
	USCI_B status word	UCB0STATW	0x01C8
	USCI_B byte counter threshold	UCB0TBCNT	0x01CA
	USCI_B receive buffer	UCB0RXBUF	0x01CC
	USCI_B transmit buffer	UCB0TXBUF	0x01CE
	USCI_B I2C own address 0	UCB0I2COA0	0x01D4
	USCI_B I2C own address 1	UCB0I2COA1	0x01D6
	USCI_B I2C own address 2	UCB0I2COA2	0x01D8
	USCI_B I2C own address 3	UCB0I2COA3	0x01DA
	USCI_B received address	UCB0ADDRX	0x01DC
	USCI_B address mask	UCB0ADDMASK	0x01DE
	USCI I2C slave address	UCB0I2CSA	0x01E0
	USCI interrupt enable	UCB0IE	0x01EA
	USCI interrupt flags	UCB0IFG	0x01EC
	USCI interrupt vector word	UCB0IV	0x01EE
Hardware Multiplier	Sum extend	SUMEXT	0x013E
	Result high word	RESHI	0x013C
	Result low word	RESLO	0x013A
	Second operand	OP2	0x0138
	Multiply signed + accumulate/operand 1	MACS	0x0136
	Multiply + accumulate/operand 1	MAC	0x0134
	Multiply signed/operand 1	MPYS	0x0132
	Multiply unsigned/operand 1	MPY	0x0130
Flash Memory	Flash control 3	FCTL3	0x012C
	Flash control 2	FCTL2	0x012A
	Flash control 1	FCTL1	0x0128
Watchdog Timer	Watchdog/timer control	WDTCTL	0x0120

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Table 9-17. Peripherals With Word Access (continued)

MODULE	REGISTER DESCRIPTION	ACRONYM	ADDRESS
SD24 (also see Table 9-18)	SD24 interrupt vector word register	SD24IV	0x01F0
	Channel 3 conversion memory(1) (2)	SD24MEM3	0x0116
	Channel 2 conversion memory(2)	SD24MEM2	0x0114
	Channel 1 conversion memory	SD24MEM1	0x0112
	Channel 0 conversion memory	SD24MEM0	0x0110
	Channel 3 control(1) (2)	SD24CCTL3	0x0108
	Channel 2 control(2)	SD24CCTL2	0x0106
	Channel 1 control	SD24CCTL1	0x0104
	Channel 0 control	SD24CCTL0	0x0102
	General Control	SD24CTL	0x0100

(1) Not available on MSP430i2031 and MSP430i2030 devices.
(2) Not available on MSP430i2021 and MSP430i2020 devices.

Table 9-18. Peripherals With Byte Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	ADDRESS
SD24 (also see Table 9-17)	SD24 trim	SD24TRIM	0x00BF
	Channel 3 preload(1) (2)	SD24PRE3	0x00BB
	Channel 2 preload(2)	SD24PRE2	0x00BA
	Channel 1 preload	SD24PRE1	0x00B9
	Channel 0 preload	SD24PRE0	0x00B8
	Channel 3 input control(1) (2)	SD24INCTL3	0x00B3
	Channel 2 input control(2)	SD24INCTL2	0x00B2
	Channel 1 input control	SD24INCTL1	0x00B1
	Channel 0 input control	SD24INCTL0	0x00B0
PMM	Reference calibration 1	REFCAL1	0x0063
	Reference calibration 0	REFCAL0	0x0062
	Voltage monitor control	VMONCTL	0x0061
	LPM4.5 control	LPM45CTL	0x0060
Clock System	Clock system external resistor temperature calibration	CSERTCAL	0x0055
	Clock system external resistor frequency calibration	CSERFCAL	0x0054
	Clock system internal resistor temperature calibration	CSIRTCAL	0x0053
	Clock system internal resistor frequency calibration	CSIRFCAL	0x0052
	Clock system control 1	CSCTL1	0x0051
	Clock system control 0	CSCTL0	0x0050
Port P2	Port P2 interrupt flag	P2IFG	0x002D
	Port P2 interrupt enable	P2IE	0x002B
	Port P2 interrupt edge select	P2IES	0x0029
	Port P2 interrupt vector word	P2IV	0x002E
	Port P2 selection 1	P2SEL1	0x001D
	Port P2 selection 0	P2SEL0	0x001B
	Port P2 direction	P2DIR	0x0015
	Port P2 output	P2OUT	0x0013
	Port P2 input	P2IN	0x0011

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Table 9-18. Peripherals With Byte Access (continued)

MODULE	REGISTER DESCRIPTION	REGISTER NAME	ADDRESS
Port P1	Port P1 interrupt flag	P1IFG	0x002C
	Port P1 interrupt enable	P1IE	0x002A
	Port P1 interrupt edge select	P1IES	0x0028
	Port P1 interrupt vector word	P1IV	0x001E
	Port P1 selection 1	P1SEL1	0x001C
	Port P1 selection 0	P1SEL0	0x001A
	Port P1 direction	P1DIR	0x0014
	Port P1 output	P1OUT	0x0012
	Port P1 input	P1IN	0x0010
Special Function	SFR interrupt flag 1	IFG1	0x0002
	SFR interrupt enable 1	IE1	0x0000

(1) Not available on MSP430i2031 or MSP430i2030 devices.

(2) Not available on MSP430i2021 or MSP430i2020 devices.

9.14 Identification

9.14.1 Device Identification

The device type can be identified from the top-side marking on the device package. See the packaging information page or the device errata sheets listed in Section 11.4 for help.

9.14.2 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the MSP430 Programming With the JTAG Interface.

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10 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

The following resources provide application guidelines and best practices when designing with the MSP430i20xx devices.

Implementation of a One- or Two-Phase Electronic Watt-Hour Meter Using MSP430i20xx application report

This application report describes the implementation of a low-cost 1- or 2-phase electronic electricity meter that uses the TI MSP430i20xx metering processor. This application report includes information on metrology software and hardware procedures for this single-chip implementation.

Single-Phase and DC Embedded Metering Power Using MSP430i2040 application report

This application report describes an EVM that uses the MSP430i2040 microcontroller for embedded metering (submetering). In this application, the electricity measuring device is embedded in the end application and gives the user information about the voltage, current, and power consumption of the device. In addition, the EVM can compensate for line resistance and EMI filter capacitance.

Single Phase and DC Embedded Metering (Server Power Monitor) reference design

This reference design implements a high-accuracy single-phase embedded meter using an MSP430 MCU. This EVM has built-in support to measure AC voltage, current, active power, reactive power, apparent power, frequency, power factor, voltage THD, current THD, fundamental voltage, fundamental current, fundamental power and DC voltage, DC current, DC active power. It can detect the input voltage to work in DC or AC mode. It can also compensate for the effects of the wire resistance and the EMI filter capacitance so that the reading of voltage and power matches the reading of an external meter when EMI filter is connected to the input.

Three Output Smart Power Strip reference design

This reference design implements a high-accuracy single-phase embedded metering smart power strip using an MSP430 MCU. This design supports measurement of AC voltage, current, active power, reactive power, apparent power, frequency, and power factor with 3 sockets measured individually. Additional hardware is added to provide futher development like relay control and wired or wireless communication.

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11 Device and Documentation Support

11.1 Getting Started and Next Steps

For more information on the MSP430™ family of devices and the tools and libraries that are available to help with your development, visit the MSP430™ ultra-low-power sensing & measurement MCUs overview.

11.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

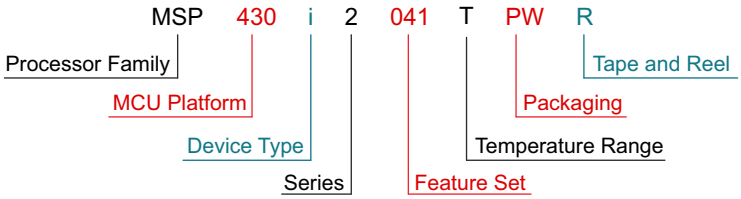
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 11-1 provides a legend for reading the complete device name.



Processor Family	MSP = Mixed-Signal Processor XMS = Experimental Silicon
MCU Platform	430 = TI's MSP430 Microcontroller Platform
Device Type	Specialized Application i = Flash Industrial
Series	2 = Flash 2 series up to 16.384 MHz
Feature Set	Various levels of integration within a series
Temperature Range	T = –40°C to 105°C
Packaging	http://www.ti.com/packaging
Tape and Reel	T = Small Reel R = Large Reel No markings = Tube or tray

Figure 11-1. Device Nomenclature

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11.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at MSP430 ultra-low-power MCUs – Design & development.

Design Kits and Evaluation Modules

32-pin target development board and MSP-FET programmer bundle for MSP430i2x MCUs

The MSP-FET430U32A is a stand-alone ZIF socket target board used to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy-Bi-Wire (2-wire JTAG) protocol.

MSP430 LaunchPad™ Value Line Development Kit

The MSP-EXP430G2 LaunchPad development kit is an easy-to-use microcontroller development board for the low-power and low-cost MSP430G2x MCUs. It has on-board emulation for programming and debugging and features a 14/20-pin DIP socket, on-board buttons and LEDs and BoosterPack plug-in module pinouts that support a wide range of modules for added functionality such as wireless, displays, and more.

MSP430i2040 Submetering EVM

This embedded metering (sub-meter or e-meter) EVM is designed based on the MSP430i2040. The EVM can be connected to the mains (or to DC) and the load directly. The EVM measures the electrical parameters of the load and the result of measurement can be read from the UART port. This EVM provided with built-in power supply and isolated serial connect to facilitate user quick start to the evaluation of the MSP430i2040 in embedded metering application.

Software

MSP430Ware™ Software

MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 MCU design resources, MSP430Ware software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

MSP430i20xx Code Examples

C code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

Floating Point Math Library for MSP430

Leveraging the intelligent peripherals of TI devices, this floating point math library of scalar functions brings you up to 26x better performance. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio and IAR IDEs.

Fixed Point Math Library for MSP

The TI MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

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Development Tools

Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers

Code Composer Studio (CCS) integrated development environment (IDE) supports all MSP microcontroller devices. CCS comprises a suite of embedded software utilities used to develop and debug embedded applications. CCS includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.

MSP Flasher - Command Line Programmer

MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) directly to the MSP microcontroller without an IDE.

MSP MCU Programmer and Debugger

The MSP-FET is a powerful emulation development tool – often called a debug probe – which lets users quickly begin application development on MSP low-power MCUs. Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging.

MSP-GANG Production Programmer

The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that let the user fully customize the process.

11.4 Documentation Support

The following documents describe the MSP430i20xx MCUs. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for example, MSP430i2041). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

MSP430i2041 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430i2040 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430i2031 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430i2031 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430i2021 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430i2021 Device Erratasheet

Describes the known exceptions to the functional specifications.

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User's Guides

MSP430i2xx Family User's Guide

Detailed description of all modules and peripherals available in this device family.

MSP430™ Flash Device Bootloader (BSL) User's Guide

The MSP430 bootloader (BSL) lets users communicate with embedded memory in the MSP430 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

MSP430 Programming With the JTAG Interface

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

MSP430 Hardware Tools User's Guide

This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

Application Reports

MSP430 32-kHz Crystal Oscillators

Selection of the correct crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

MSP430 System-Level ESD Considerations

System-level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses different ESD topics to help board designers and OEMs understand and design robust system-level designs.

11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.6 Trademarks

MSP430Ware™, MSP430™, Code Composer Studio™, TI E2E™, LaunchPad™, are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430I2020TPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2020T
MSP430I2020TPW.B	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2020T
MSP430I2020TPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2020T
MSP430I2020TPWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2020T
MSP430I2020TRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2020T
MSP430I2020TRHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2020T
MSP430I2020TRHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2020T
MSP430I2020TRHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2020T
MSP430I2021TPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T
MSP430I2021TPW.B	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T
MSP430I2021TPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T
MSP430I2021TPWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T
MSP430I2021TRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T
MSP430I2021TRHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T
MSP430I2021TRHBRG4	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T
MSP430I2021TRHBRG4.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T
MSP430I2021TRHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T
MSP430I2021TRHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T
MSP430I2030TPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2030T
MSP430I2030TPW.B	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2030T
MSP430I2030TPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2030T
MSP430I2030TPWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2030T
MSP430I2030TRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2030T
MSP430I2030TRHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2030T
MSP430I2030TRHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2030T
MSP430I2030TRHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2030T
MSP430I2031TPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2031T
MSP430I2031TPW.B	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2031T
MSP430I2031TPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2031T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430I2031TPWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2031T
MSP430I2031TRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2031T
MSP430I2031TRHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2031T
MSP430I2031TRHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2031T
MSP430I2031TRHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2031T
MSP430I2040TPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2040T
MSP430I2040TPW.B	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2040T
MSP430I2040TPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2040T
MSP430I2040TPWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2040T
MSP430I2040TRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2040T
MSP430I2040TRHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2040T
MSP430I2040TRHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2040T
MSP430I2040TRHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2040T
MSP430I2041TPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2041T
MSP430I2041TPW.B	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2041T
MSP430I2041TPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2041T
MSP430I2041TPWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2041T
MSP430I2041TRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2041T
MSP430I2041TRHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2041T
MSP430I2041TRHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2041T
MSP430I2041TRHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2041T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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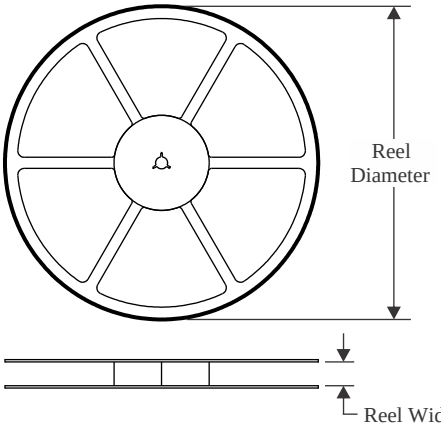
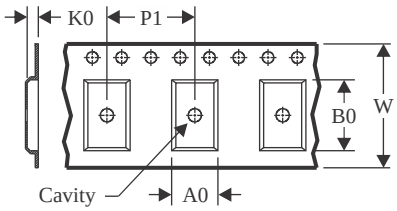
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

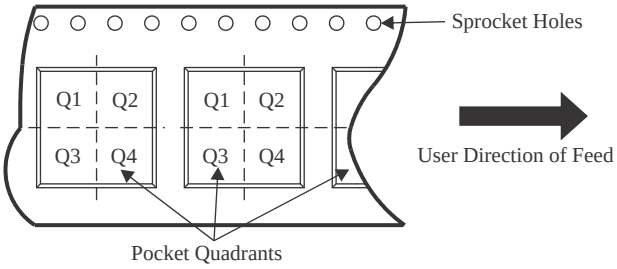


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

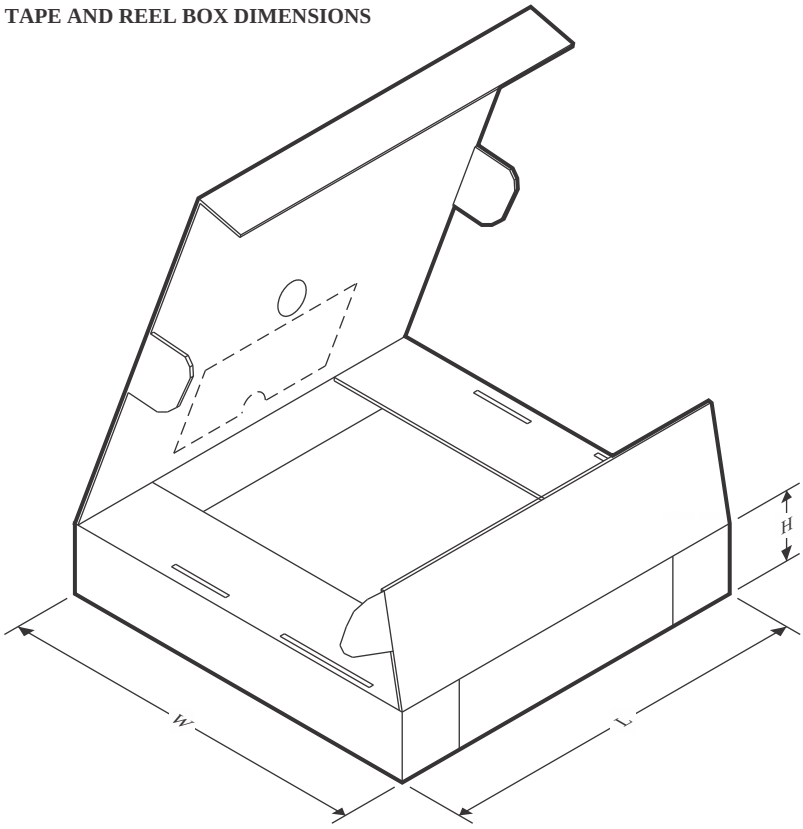


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430I2020TPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430I2020TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2020TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2020TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2020TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2021TPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430I2021TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2021TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2021TRHBRG4	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2021TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2021TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2030TPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430I2030TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2030TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2030TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2030TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430I2031TPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430I2031TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2031TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2031TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2031TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2040TPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430I2040TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2040TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2040TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2041TPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430I2041TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2041TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

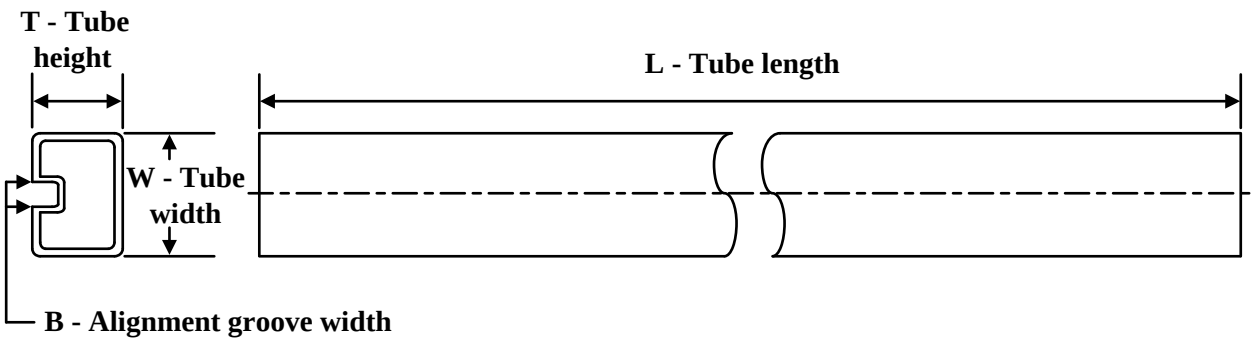


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430I2020TPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MSP430I2020TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430I2020TRHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
MSP430I2020TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2020TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2021TPWR	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430I2021TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430I2021TRHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
MSP430I2021TRHBRG4	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430I2021TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2021TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2030TPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MSP430I2030TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430I2030TRHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
MSP430I2030TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2030TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2031TPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MSP430I2031TRHBR	VQFN	RHB	32	3000	346.0	346.0	33.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430I2031TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430I2031TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2031TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2040TPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MSP430I2040TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430I2040TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2040TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2041TPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MSP430I2041TRHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
MSP430I2041TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430I2020TPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2020TPW.B	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2021TPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2021TPW.B	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2030TPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2030TPW.B	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2031TPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2031TPW.B	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2040TPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2040TPW.B	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2041TPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2041TPW.B	PW	TSSOP	28	50	530	10.2	3600	3.5

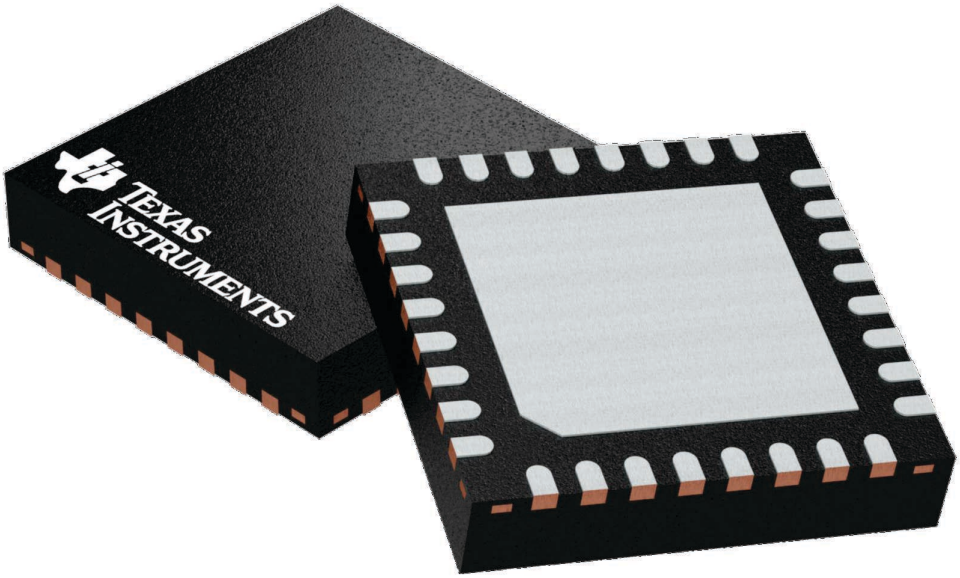
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

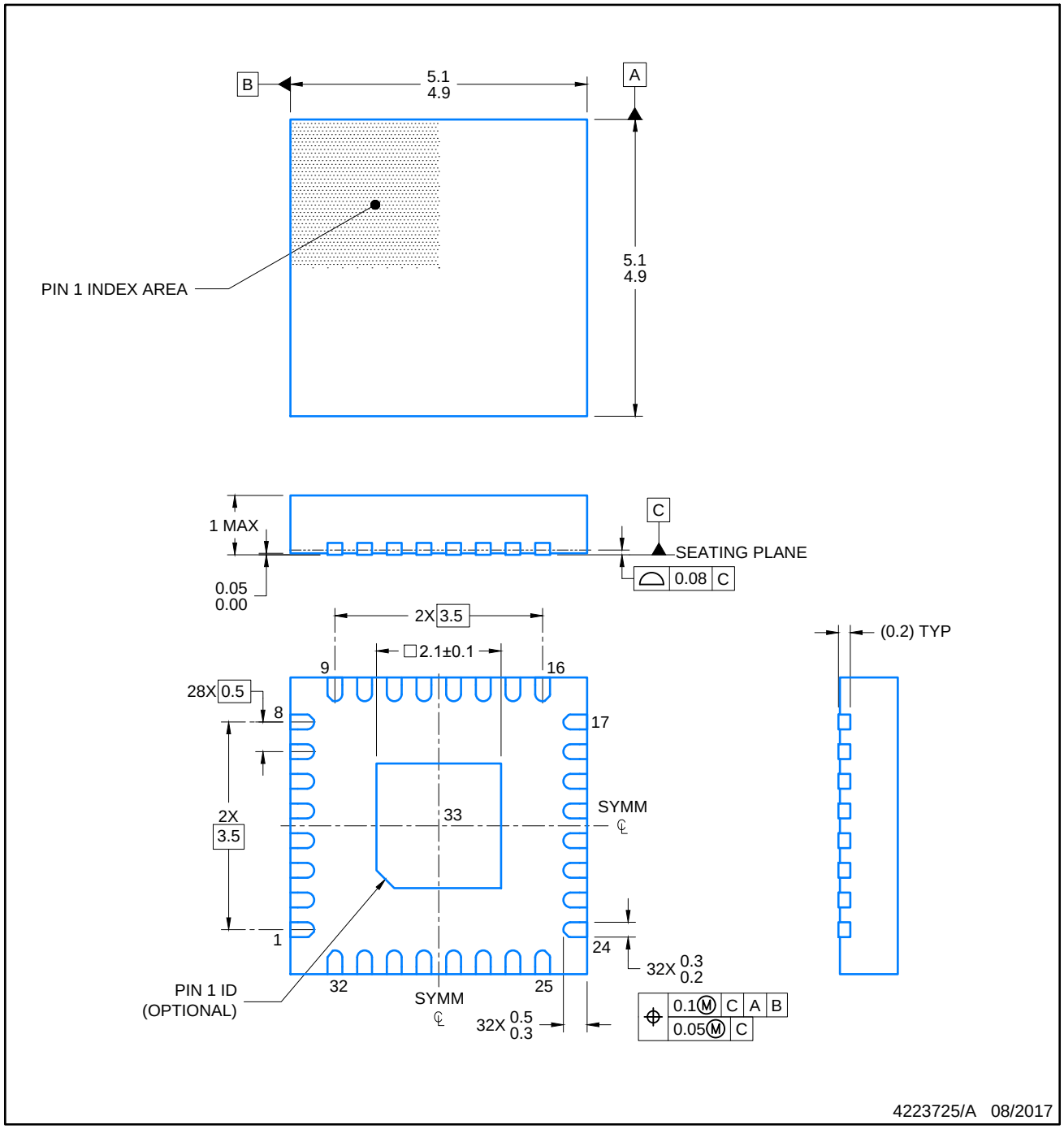
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



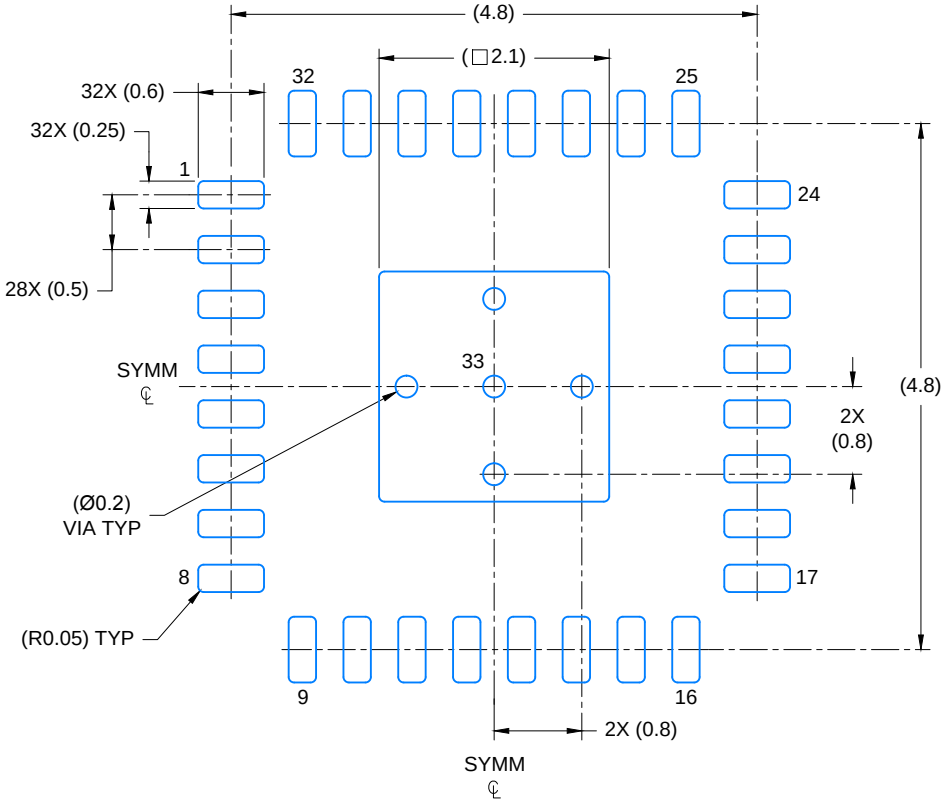
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

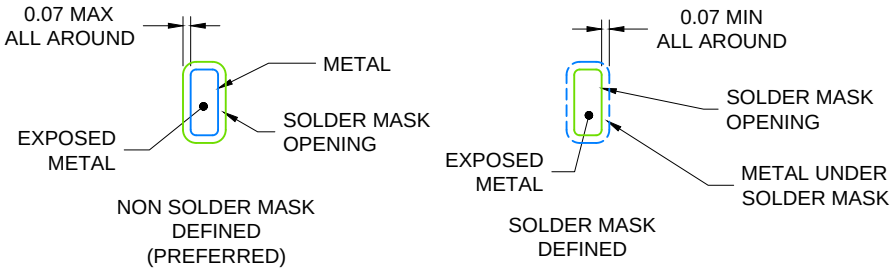


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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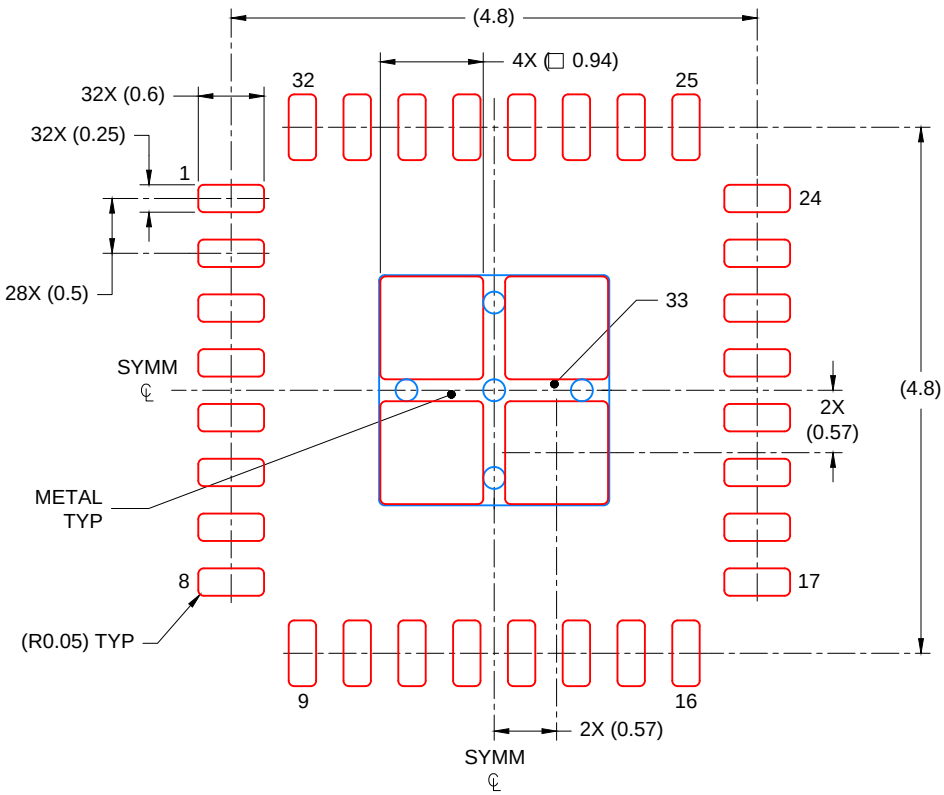
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

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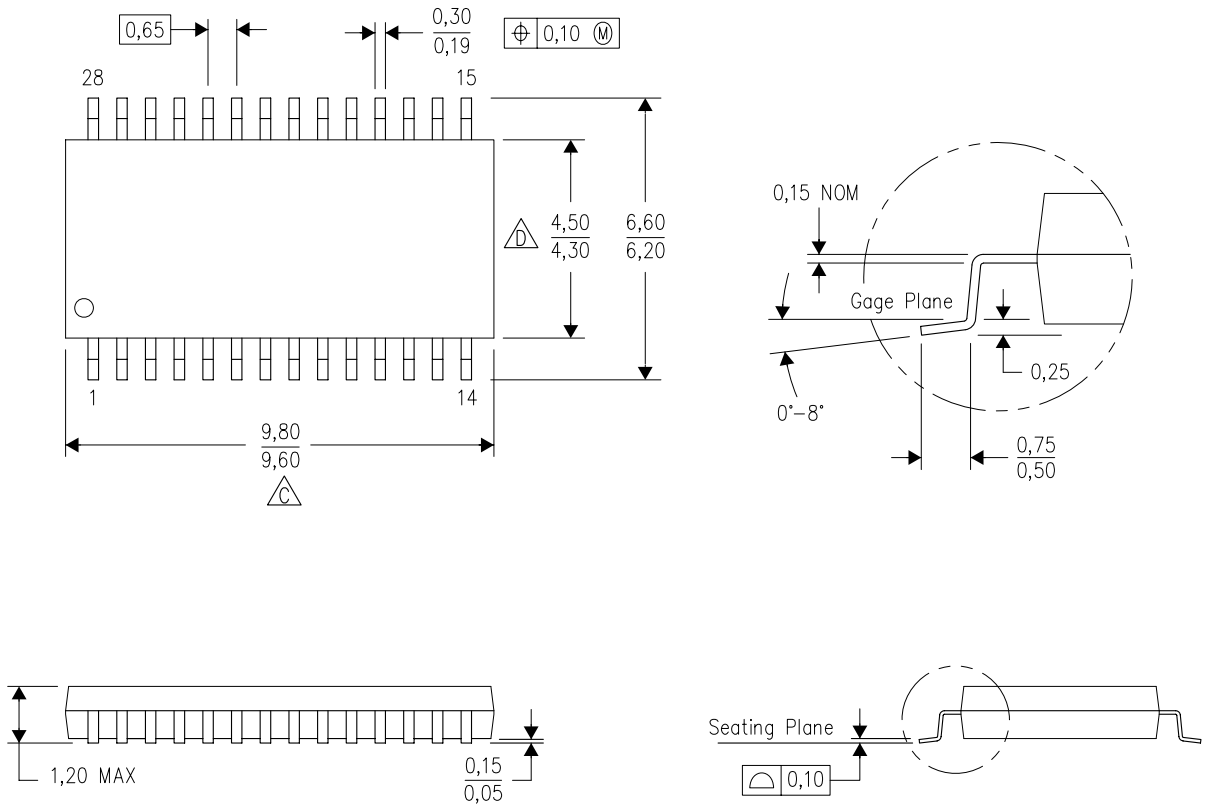
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW (R-PDSO-G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

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