CDx4AC257, CDx4ACT257, CD74ACT258 Quad 2-Input Multiplexer with Three-State Outputs

1 Features

- ’AC257, ’ACT257……. non-inverting outputs
- CD74ACT258 ……. inverting outputs
- Buffered inputs
- Typical propagation delay
  - 4.4ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- Exceeds 2kV ESD protection MIL-STD-883, method 3015
- SCR-latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST™/AS/S with significantly reduced power consumption
- Balanced Propagation Delays
- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply
- ±24mA output drive current
  - Fanout to 15 FAST™ ICs
- Drives 50Ω transmission lines

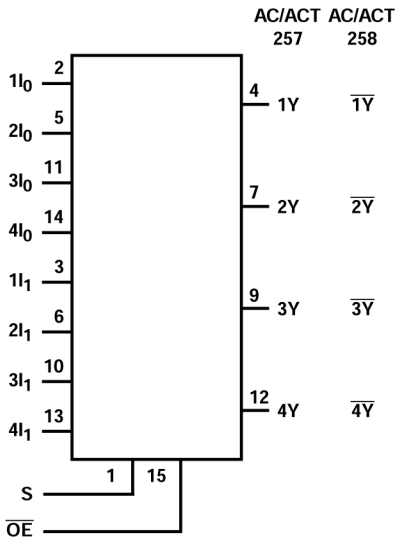
2 Description

The ’AC257, ’ACT257 and CD74ACT258 are quad 2-input multiplexers with three-state outputs that utilize Advanced CMOS Logic technology.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
CDx4AC257, CDx4ACT257, CD74ACT258	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm
	N (PDIP, 16)	19.3mm × 9.4mm	19.3mm × 6.35mm
	PW (TSSOP, 16)	5mm × 6.4mm	5mm × 4.4mm
	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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3 Pin Configuration and Functions

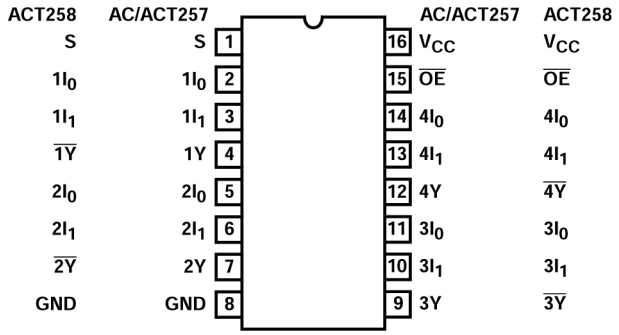

Figure 3-1. CD54AC257, CD54ACT257 J Package; CD74AC257, CD74ACT257, CD74ACT258 D, N, or PW Package; 16-Pin SOIC PDIP, or TSSOP (Top View)

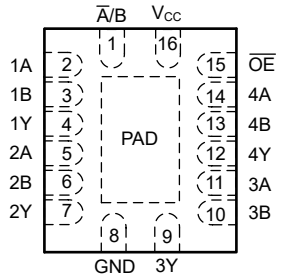

Figure 3-2. CD74AC257, CD74ACT257, CD74ACT258 BQB Package, 16-Pin WQFN (Top View)

Table 3-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
S	1	I	Select
$1I_0$	2	I	Channel 1 Input 0
$1I_1$	3	I	Channel 1 Input 1
1Y	4	O	Channel 1 Output
$2I_0$	5	I	Channel 2 Input 0
$2I_1$	6	I	Channel 2 Input 1
2Y	7	O	Channel 2 Output
GND	8	G	Ground
3Y	9	O	Channel 3 Output
$3I_1$	10	I	Channel 3 Input 1
$3I_0$	11	I	Channel 3 Input 0
4Y	12	O	Channel 4 Output
$4I_1$	13	I	Channel 4 Input 1
$4I_0$	14	I	Channel 4 Input 0
$\overline{OE}$	15	I	Output Enable
V_{CC}	16	P	Positive Supply
Thermal Pad[2]		–	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2) BQB Package only

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	6	V
I_{IK}	Input diode current	V_I < -0.5V or V_I > V_{CC} + 0.5V		±20	mA
I_{OK}	Output diode current	V_O < -0.5V or V_O > V_{CC} + 0.5V		±50	mA
I_O	Output source or sink current per output pin	V_O > -0.5V or V_O < V_{CC} + 0.5V		±50	mA
I_{CC} or I_{GND} [2]	V_{CC} or ground current			±100	mA
T_{stg}	Maximum storage temperature		-65	150	°C

(1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
(2) For up to 4 outputs per device, add ±25mA for each additional output.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Temperature Range	-55	125	°C
V_{CC} [1]	Supply Voltage Range			
	AC Types	1.5	5.5	V
	ACT Types	4.5	5.5	V
V_I, V_O	DC Input or Output Voltage	0	V_{CC}	V
dt/dv	Input Rise and Fall Slew Rate			
1.5V to 3V	AC Types		50	ns
3.6V to 5.5V	AC Types		20	ns
4.5V to 5.5V	ACT Types		10	ns

(1) Unless otherwise specified, all voltages are referenced to ground.

4.3 Thermal Information

THERMAL METRIC[1]		D (SOIC)	PW (TSSOP)	BQB (WQFN)	UNIT
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.9[2]	139.5	98.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	74.8	94.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	97.7	67.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	—	17.8	15.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	—	96.6	67.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	45.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application note.
(2) θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

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4.4 Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNIT
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES											
High Level Input Voltage	V_{IH}	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
Low Level Input Voltage	V_{IL}	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (1), (2)	5.5	-	-	3.85	-	-	-	V
			-50 (1), (2)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (1), (2)	5.5	-	-	-	1.65	-	-	V
			50 (1), (2)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I_I	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Three-State Leakage Current	I_{OZ}	V_{IH} or V_{IL} $V_O = V_{CC}$ or GND	-	5.5	-	±0.5	-	±5	-	±10	µA
Quiescent Supply Current MSI	I_{CC}	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA
ACT TYPES											
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (1), (2)	5.5	-	-	3.85	-	-	-	V
			-50 (1), (2)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (1), (2)	5.5	-	-	-	1.65	-	-	V
			50 (1), (2)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I_I	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Three-State or Leakage Current	I_{OZ}	V_{IH} or V_{IL} $V_O = V_{CC}$ or GND	-	5.5	-	±0.5	-	±5	-	±10	µA

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PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNIT
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Quiescent Supply Current MSI	I_{CC}	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
(2) Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

Table 4-1. ACT Input Load Table

INPUT	UNIT LOAD
Data	0.83
S	1.27
$\overline{OE}$	1.27

Note

Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

4.5 Switching Specifications

Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
Propagation Delay, In to Y AC/ ACT257	t_{PLH}, t_{PHL}	1.5	-	-	106	-	-	117	ns
		3.3 (1)	3.3	-	11.8	3.3	-	13	ns
		5(2)	2.4	-	8.5	2.3	-	9.3	ns
Propagation Delay, S to Y AC/ ACT257	t_{PLH}, t_{PHL}	1.5	-	-	153	-	-	168	ns
		3.3	4.8	-	17.1	4.7	-	18.8	ns
		5	3.5	-	12.2	3.4	-	13.4	ns
Propagation Delay, $\overline{OE}$ to Y AC/ ACT257	t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}	1.5	-	-	167	-	-	184	ns
		3.3	5.3	-	18.7	5.2	-	20.6	ns
		5	3.8	-	13.4	3.7	-	14.7	ns
Propagation Delay, In to $\overline{Y}$ 'AC/ CD74ACT258	t_{PLH}, t_{PHL}	1.5	-	-	91	-	-	100	ns
		3.3	2.9	-	10.2	2.8	-	11.2	ns
		5	2.1	-	7.3	2	-	8	ns
Propagation Delay, S to $\overline{Y}$ 'AC/ CD74ACT258	t_{PLH}, t_{PHL}	1.5	-	-	153	-	-	168	ns
		3.3	4.8	-	17.1	4.7	-	18.8	ns
		5	3.5	-	12.2	3.4	-	13.4	ns
Propagation Delay, $\overline{OE}$ to $\overline{Y}$ 'AC/ CD74ACT258	t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}	1.5	-	-	167	-	-	184	ns
		3.3	5.3	-	18.7	5.2	-	20.6	ns
		5	3.8	-	13.4	3.7	-	14.7	ns
Three-State Output Capacitance	C_O	-	-	-	15	-	-	15	pF
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (3)	-	-	130	-	-	130	-	pF
ACT TYPES									

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Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay, In to Y AC/ ACT257	t_{PLH}, t_{PHL}	5 (2)	2.8	-	9.7	2.7	-	10.7	ns
Propagation Delay, S to Y AC/ ACT257	t_{PLH}, t_{PHL}	5	4	-	14	3.9	-	15.4	ns
Propagation Delay, $\overline{OE}$ to Y AC/ ACT257	t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}	5	4.1	-	14.6	4	-	16.1	ns
Propagation Delay, In to $\overline{Y}$ 'AC/ CD74ACT258	t_{PLH}, t_{PHL}	5	2.4	-	8.5	2.3	-	9.3	ns
Propagation Delay, S to $\overline{Y}$ 'AC/ CD74ACT258	t_{PLH}, t_{PHL}	5	4	-	14	3.9	-	15.4	ns
Propagation Delay, $\overline{OE}$ to $\overline{Y}$ 'AC/ CD74ACT258	t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}	5	4.1	-	14.6	4	-	16.1	ns
Three-State Output Capacitance	C_O	-	-	-	15	-	-	15	pF
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (3)	-	-	130	-	-	130	-	pF

(1) 3.3V Min is at 3.6V, Max is at 3V.
(2) 5V Min is at 5.5V, Max is at 4.5V.
(3) C_{PD} is used to determine the dynamic power consumption per multiplexer.

Note

AC: $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o)$

ACT: $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

5 Parameter Measurement Information

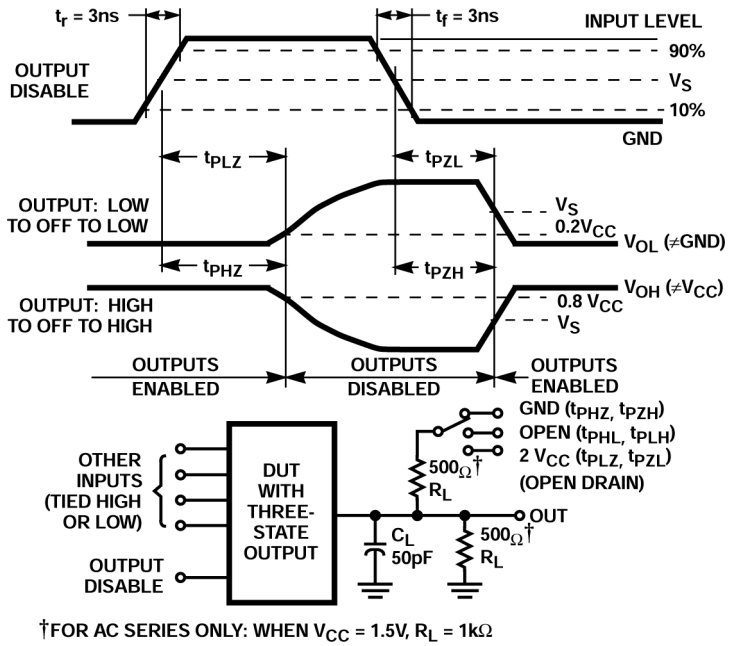

Figure 5-1. Three-State Propagation Delay Times and Test Circuit

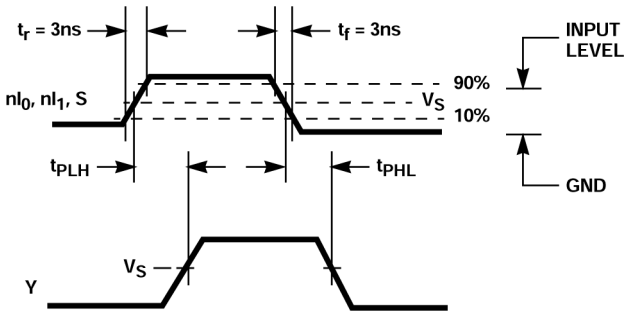

Figure 5-2. inputs or select to output propagation delays (ac/act257)

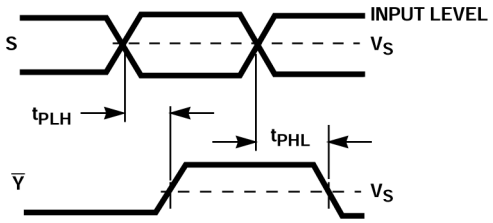

Figure 5-3. Select to Output Propagation Delays (CD74ACT258)

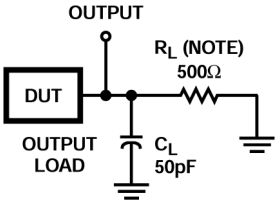

Figure 5-4.

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For AC Series Only: When V_{CC} = 1.5V, RL = 1kW.

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

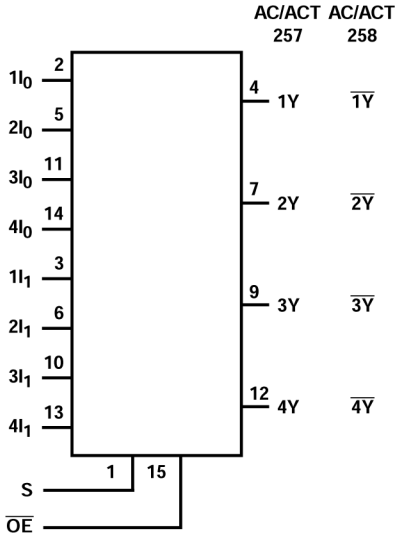
6 Detailed Description

6.1 Overview

Each of these devices selects four bits of data from two sources under the control of a common Select input (S). The Output Enable ($\overline{OE}$) is active LOW. When $\overline{OE}$ is HIGH, all of the outputs (Y or $\overline{Y}$) are in the high-impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the ’AC257, ’ACT257, and CD74ACT258. The state of the Select input determines the particular register from which the data comes. The ’AC257, ’ACT257 and CD74ACT258 can also be used as function generators.

6.2 Functional Block Diagram



6.3 Device Functional Modes

Table 6-1. Truth Table

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		257 OUTPUTS	258 OUTPUTS
$\overline{OE}$	S	I_0	I_1	Y	$\overline{Y}$
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

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8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54AC257	Click here	Click here	Click here	Click here	Click here
CD54ACT257	Click here	Click here	Click here	Click here	Click here
CD74AC257	Click here	Click here	Click here	Click here	Click here
CD74ACT257	Click here	Click here	Click here	Click here	Click here
CD74ACT258	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

FAST™ is a trademark of Fairchild Semiconductor.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision B (August 2024) to Revision C (April 2025) — **Page**

- Added PW and BQB packages to the data sheet. 1

Changes from Revision A (May 2000) to Revision B (August 2024) — **Page**

- Added *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes,*Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54AC257F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC257F3A
CD54AC257F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC257F3A
CD54ACT257F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT257F3A
CD54ACT257F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT257F3A
CD74AC257BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC257
CD74AC257E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC257E
CD74AC257E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC257E
CD74AC257M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	AC257M
CD74AC257M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC257M
CD74AC257M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC257M
CD74AC257PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	AC257
CD74AC257PWR.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC257
CD74ACT257BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AD257
CD74ACT257E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT257E
CD74ACT257E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT257E
CD74ACT257EE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT257E
CD74ACT257M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	ACT257M
CD74ACT257M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT257M
CD74ACT257M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT257M
CD74ACT257PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	AD257
CD74ACT257PWR.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AD257
CD74ACT258M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	ACT258M
CD74ACT258M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ACT258M
CD74ACT258M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ACT258M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54AC257, CD54ACT257, CD74AC257, CD74ACT257 :

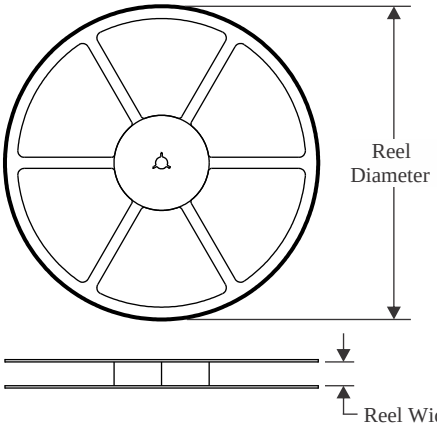
- Catalog : CD74AC257, CD74ACT257
- Military : CD54AC257, CD54ACT257

NOTE: Qualified Version Definitions:

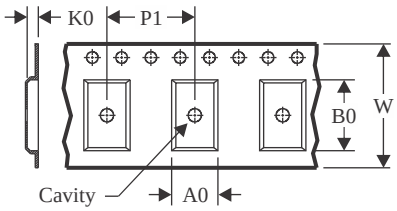
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

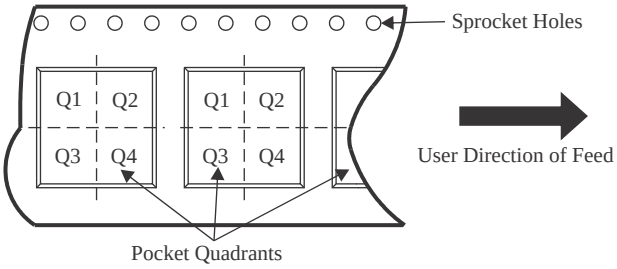


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

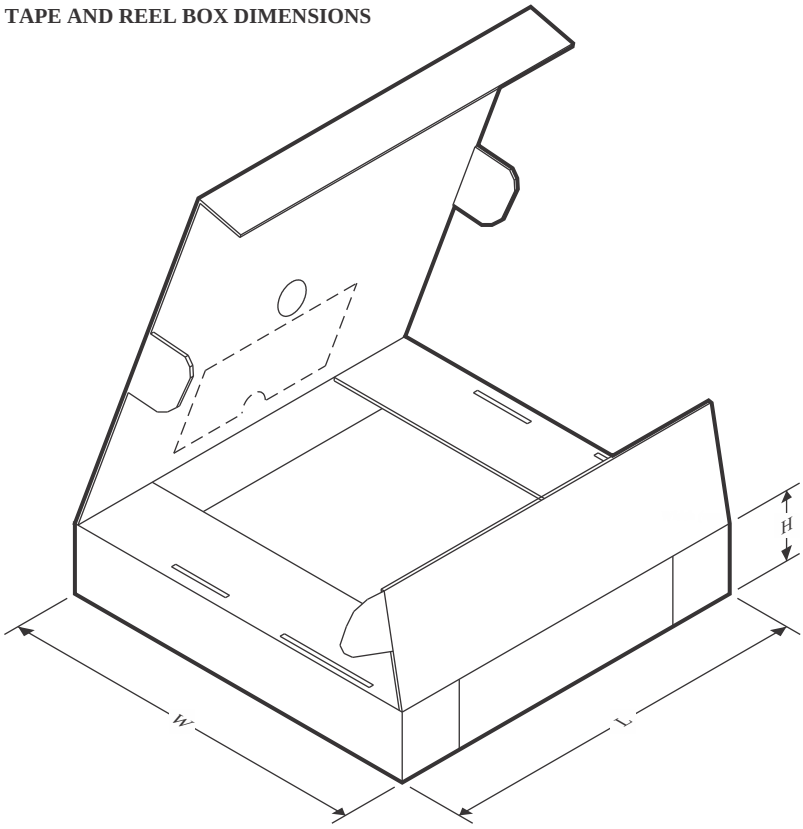
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC257BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
CD74AC257M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74AC257M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74AC257PWR	TSSOP	PW	16	3000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
CD74AC257PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74ACT257BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
CD74ACT257M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74ACT257M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74ACT257M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74ACT257PWR	TSSOP	PW	16	3000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
CD74ACT257PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74ACT258M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

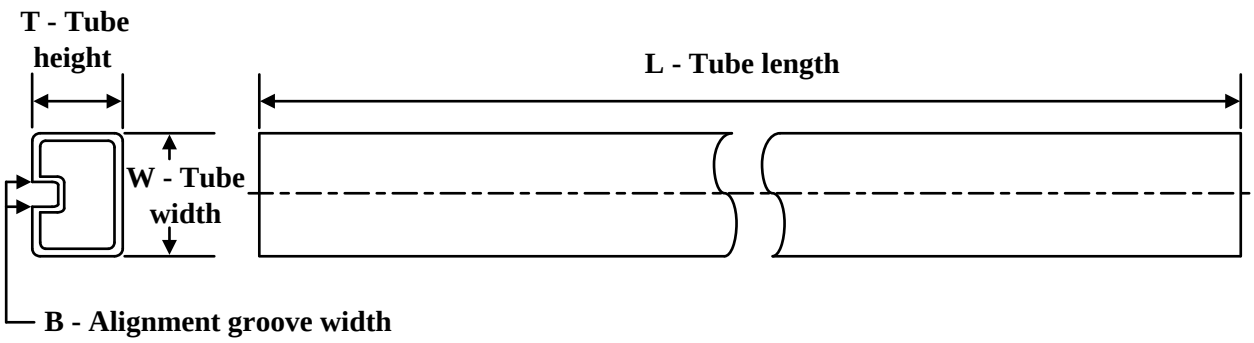
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC257BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
CD74AC257M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74AC257M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74AC257PWR	TSSOP	PW	16	3000	366.0	364.0	50.0
CD74AC257PWR	TSSOP	PW	16	3000	356.0	356.0	35.0
CD74ACT257BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
CD74ACT257M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74ACT257M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74ACT257M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74ACT257PWR	TSSOP	PW	16	3000	366.0	364.0	50.0
CD74ACT257PWR	TSSOP	PW	16	3000	353.0	353.0	32.0
CD74ACT258M96	SOIC	D	16	2500	340.5	336.1	32.0

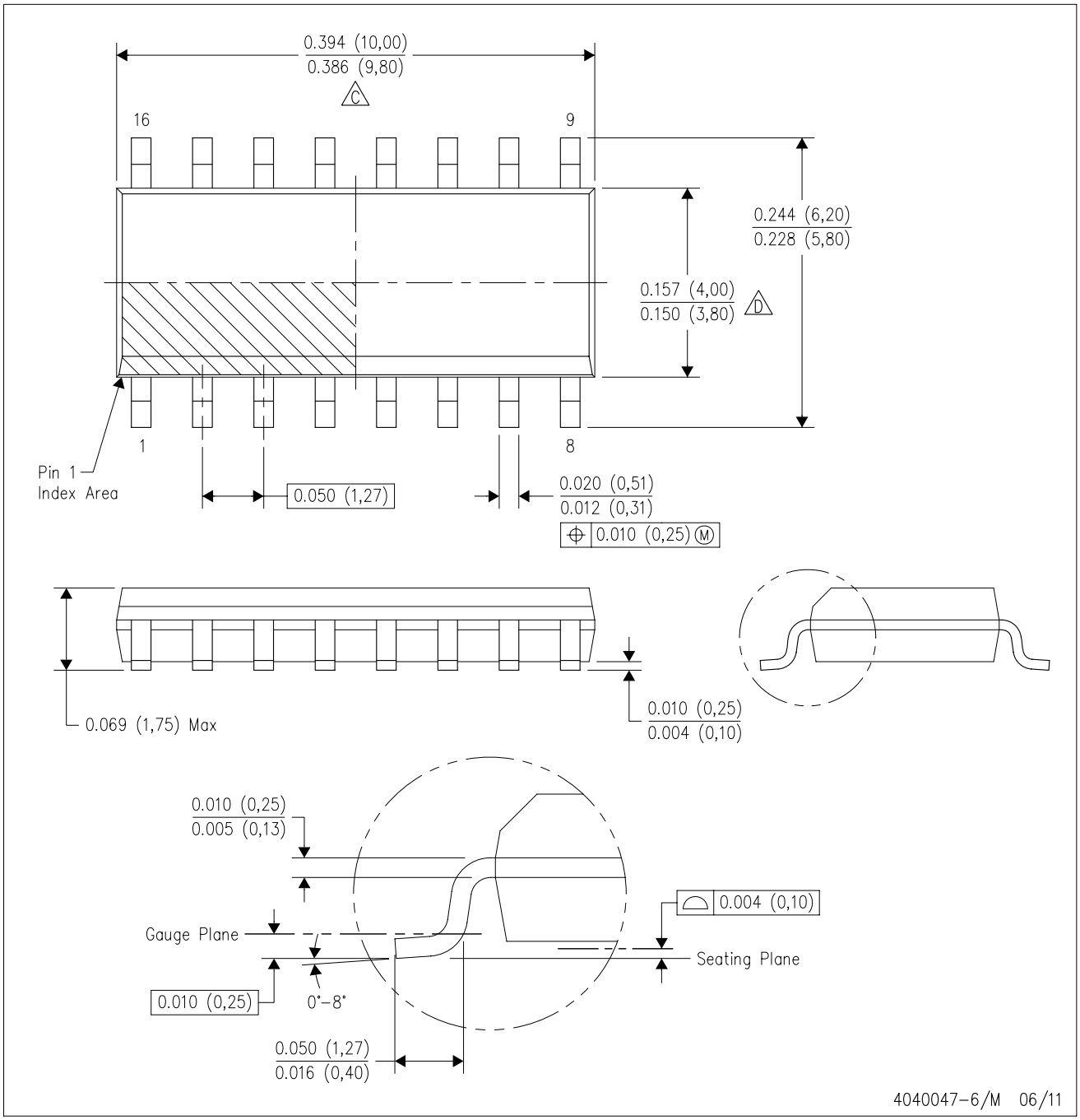
TUBE



*All dimensions are nominal

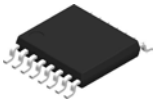
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC257E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC257E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC257E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC257E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT257E	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT257E	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT257E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT257E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT257EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT257EE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

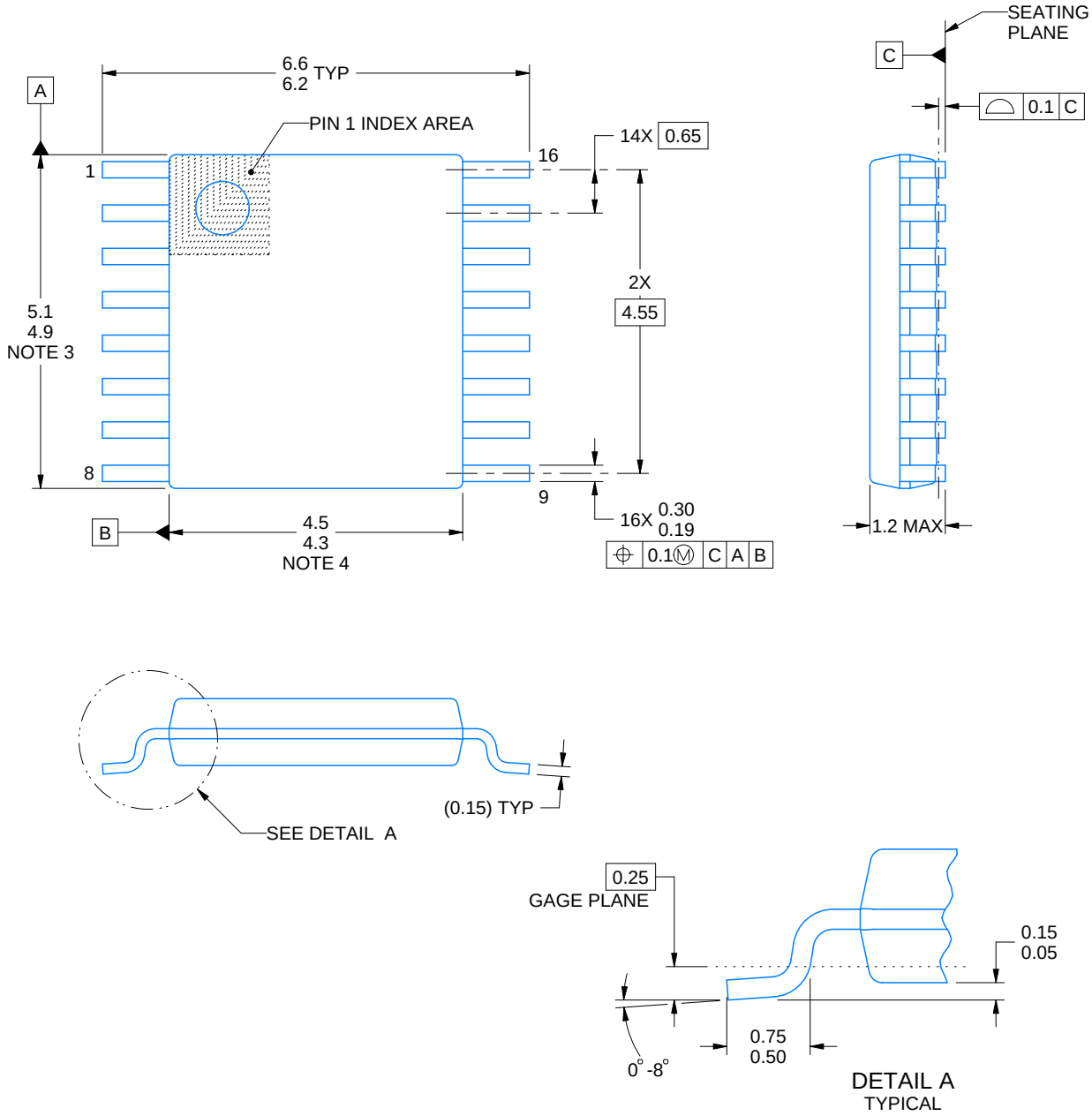
PW0016A



PACKAGE OUTLINE

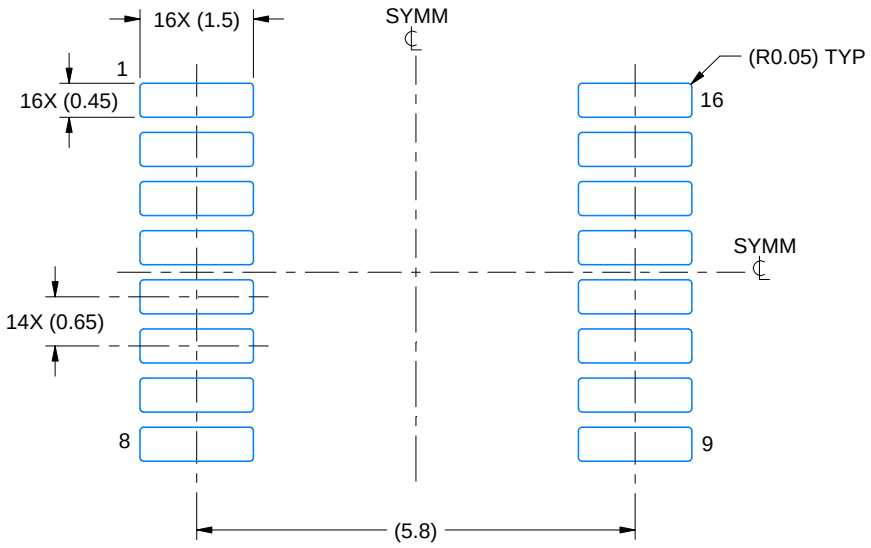
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

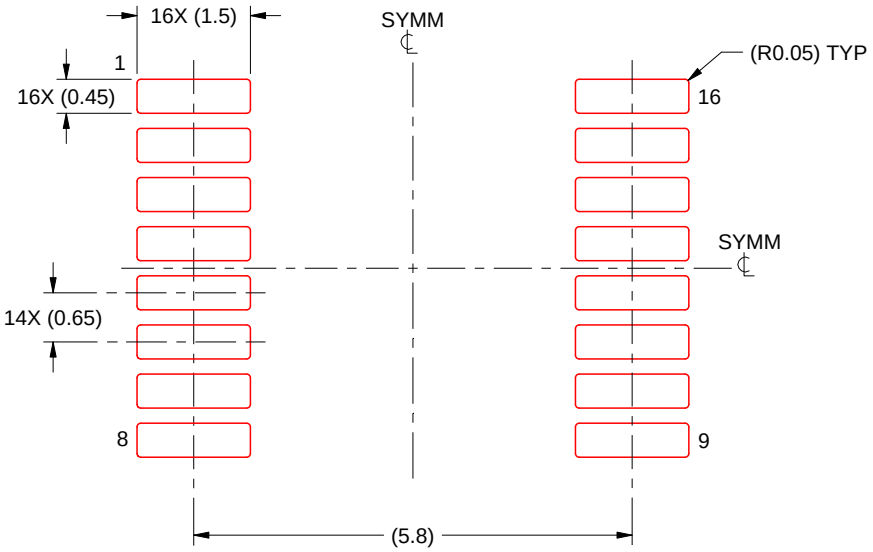
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

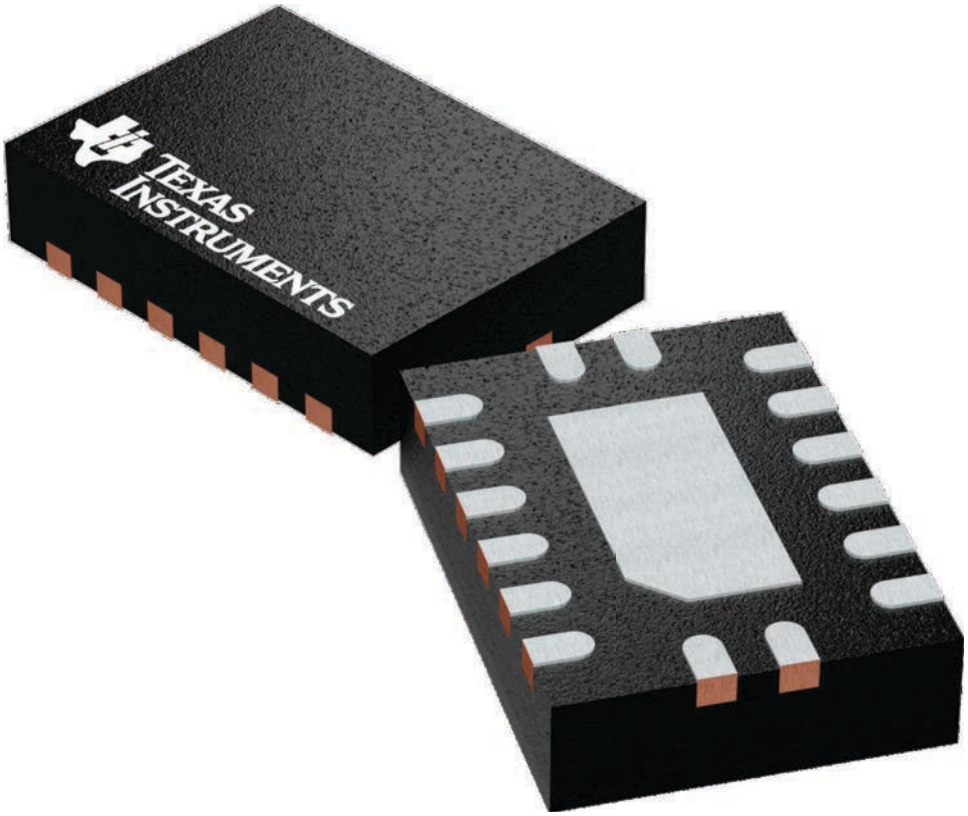
BQB 16

WQFN - 0.8 mm max height

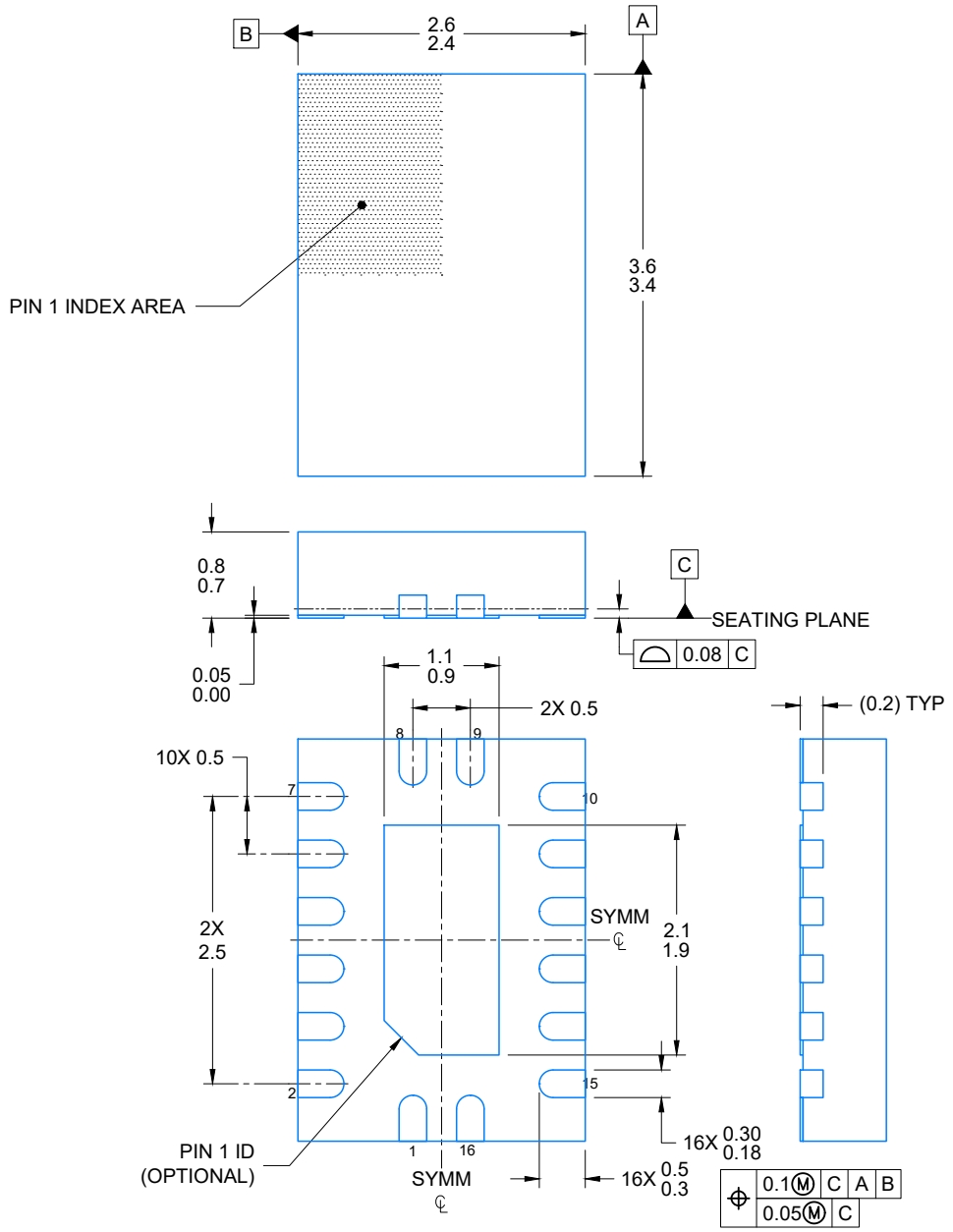
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



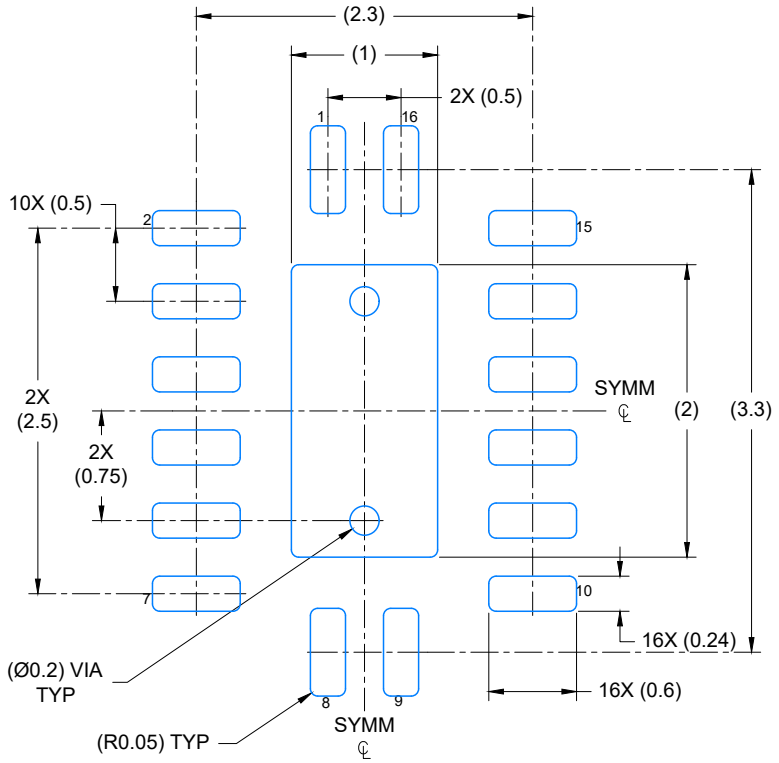
4226161/A



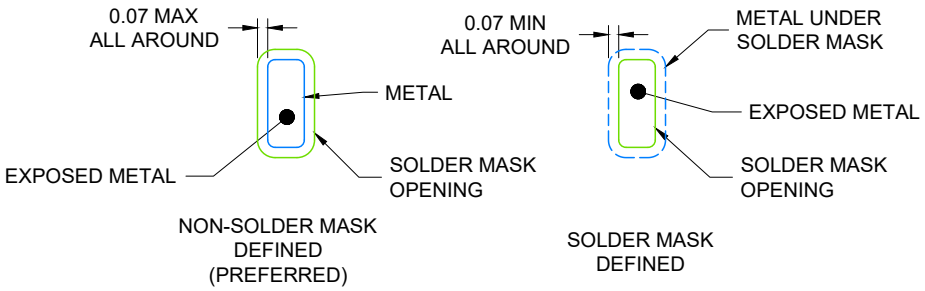
4224640/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



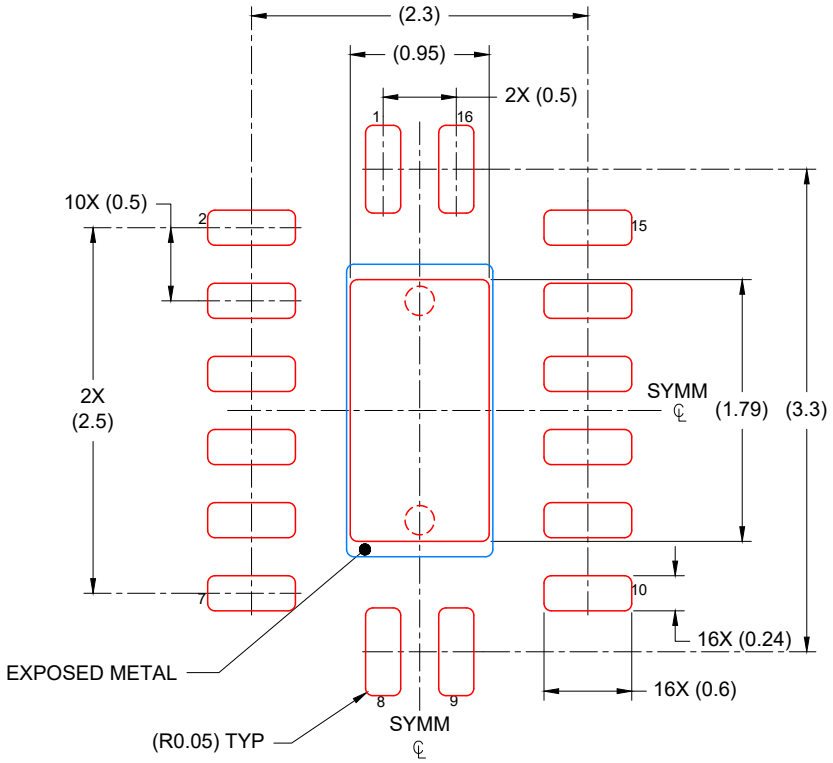
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

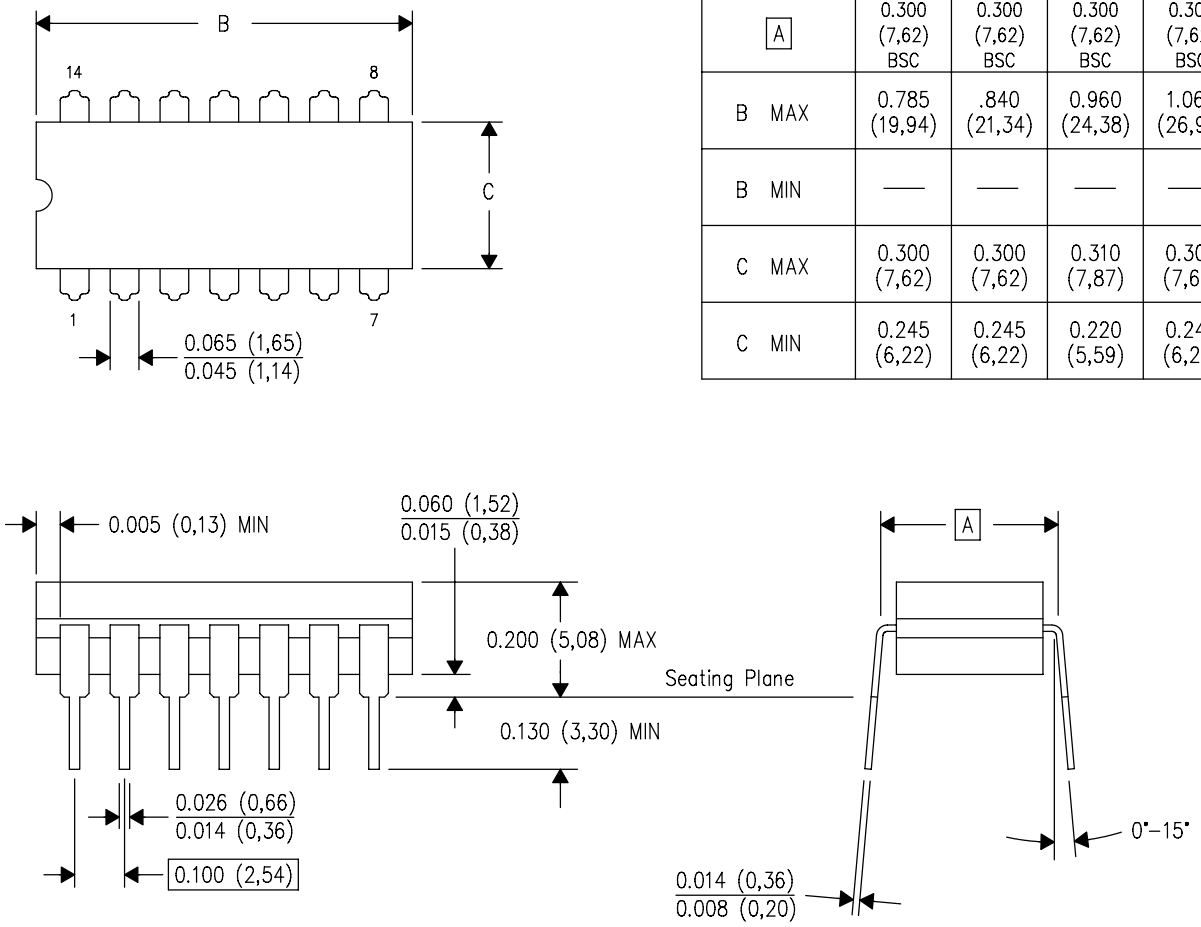
4224640/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



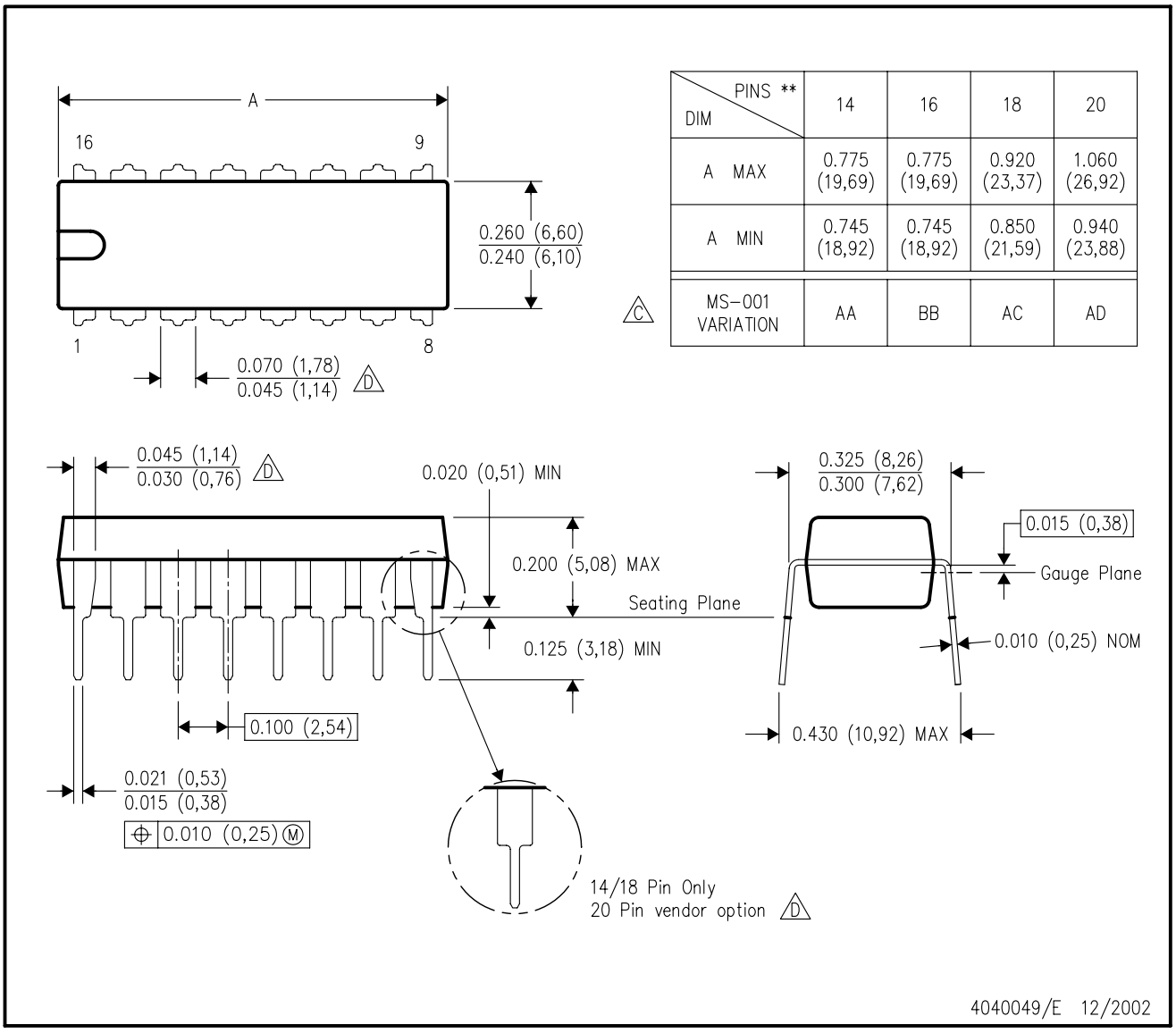
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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