DRV8334 Three-Phase Smart Gate Driver with Accurate Current Sensing and Advanced Monitoring

1 Features

- Three phase half-bridge gate driver
  - Drives six N-channel MOSFETs (NMOS)
  - 4.5 to 60V wide operating voltage range
  - Bootstrap architecture for high-side gate driver
  - Strong GVDD charge pump to support up to 50mA average gate switching current enables driving 400nC MOSFETs at 20kHz
  - Trickle charge pump to support 100% PWM duty cycle and to generate overdrive supply to drive external protection circuits
- Smart Gate Drive architecture
  - 45-level configurable peak gate drive current up to 1000 / 2000mA (source / sink)
  - Three-step dynamic drive current control
  - Configurable soft shutdown to minimize inductive voltage spikes during overcurrent shutdown
- Low-side Current Sense Amplifier
  - Sub-1mV low input offset across temperature
  - 9-level adjustable gain
- SPI-based detailed configuration and diagnostics
- DRVOFF pin to disable driver independently
- High voltage wake up pin (nSLEEP)
- 6x, 3x, 1x, and Independent PWM Modes
- Supports 3.3V, and 5V Logic Inputs
- Integrated protection features
  - Battery and power supply voltage monitors
  - Phase feedback comparator
  - MOSFET V_{DS} and R_{sense} over current monitors
  - MOSFET V_{GS} gate fault monitors
  - Device thermal warning and shutdown
  - Fault condition indicator pin

2 Applications

- Appliances, Cordless Garden and Power Tools, Lawnmowers
- Brushless-DC (BLDC) Motor Modules and PMSM
- Fans, Pumps, and Servo Drives
- E-Bikes, E-Scooters, and E-Mobility
- Cordless Vacuum Cleaners
- Drones, Industrial & Logistics Robots, and RC Toys

3 Description

The DRV8334 is an integrated smart gate driver for three-phase BLDC applications. The device provides three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The DRV8334 generates the correct gate drive voltages using an integrated bootstrap diode and a GVDD charge pump. The Smart Gate Drive architecture supports configurable peak gate drive current from 0.8mA up to 1A source and 2A sink. The DRV8334 can operate from a single power supply with a wide input range of 4.5 to 60V. A trickle charge pump enables 100% PWM duty cycle control, and provides overdrive supply voltage for external switches.

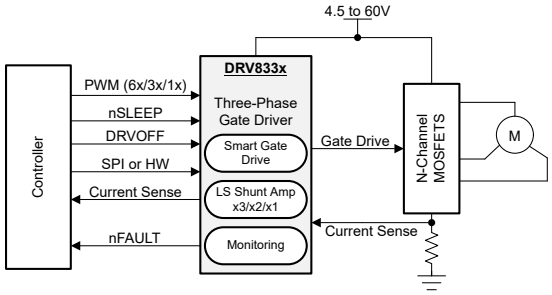
The DRV8334 provides low-side current sense amplifiers to support resistor based low-side current sensing. The low offset of the amplifiers enables the system to obtain precise motor current measurement.

A wide range of diagnostics and protection features integrated in the DRV8334 enable a robust motor drive system design and help eliminate the needs of external components. The highly configurable device response allows the device to be integrated seamlessly into a variety of system designs.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
DRV8334	HTQFP (48)	9mm x 9mm	7mm × 7mm
	QFN (48)	7mm × 7mm	7mm × 7mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

4.1 Pin Functions 48-Pin DRV8334

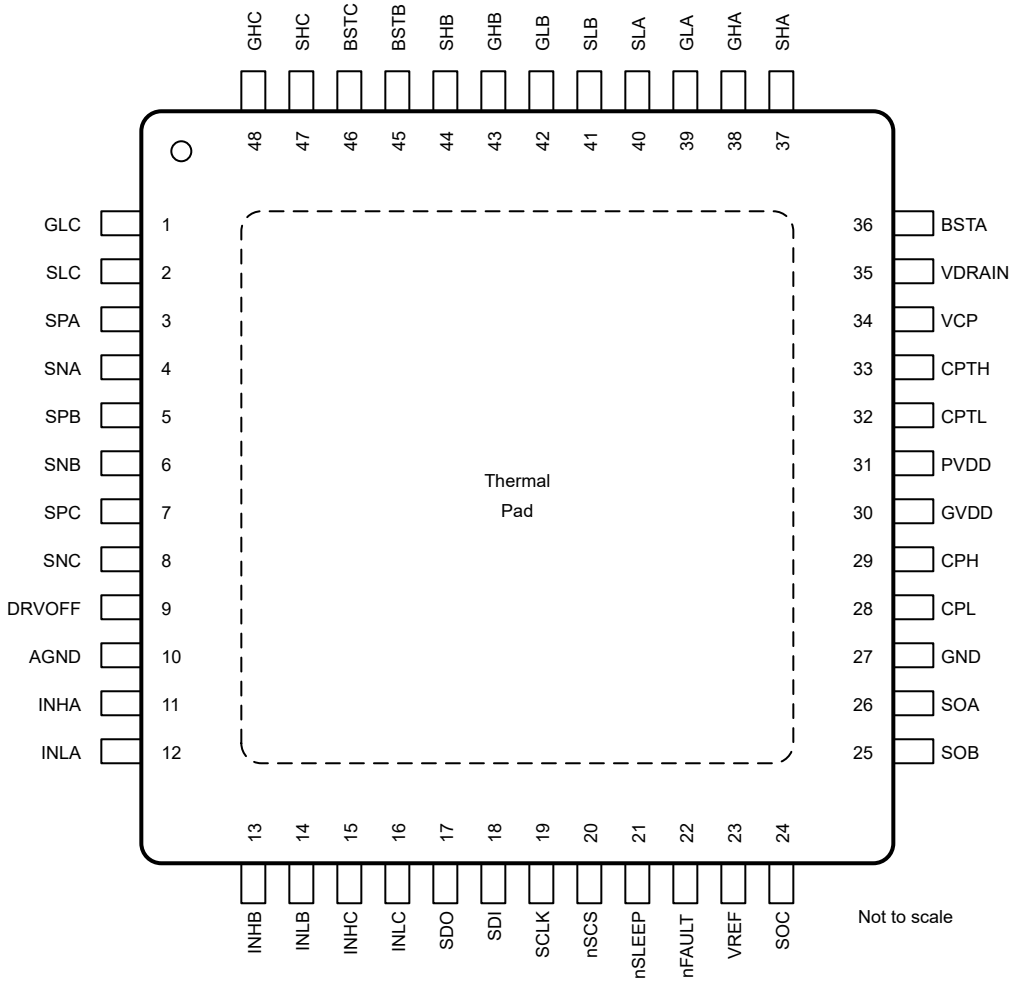

Figure 4-1. DRV8334 Package 48-Pin HTQFP With Exposed Thermal Pad Top View

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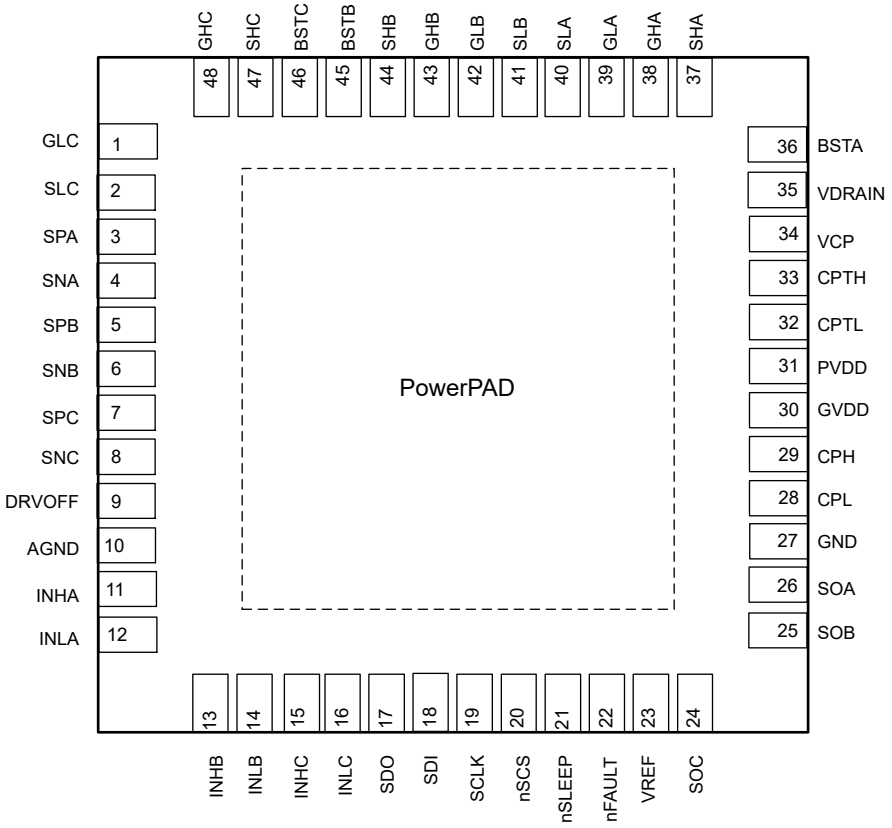

Figure 4-2. DRV8334xRGZ Package 48-Pin QFN (Preview) With Exposed Thermal Pad Top View

Table 4-1. Pin Functions 48-QFP

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
GLC	1	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
SLC	2	I	Low-side source sense input. Connect to the low-side power MOSFET source.
SPA	3	I	Low-side current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SNA	4	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
SPB	5	I	Low-side current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SNB	6	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
SPC	7	I	Low-side current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SNC	8	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
DRVOFF	9	I	Active high shutdown input to pull-down gate driver outputs GHx and GLx.
AGND	10	PWR	Device ground.
INHA	11	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	12	I/O	Low-side gate driver control input. This pin controls the output of the low-side gate driver. This pin can be configured to output buffer of phase comparator by SPI register bit PHC_OUTEN.
INHB	13	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLB	14	I/O	Low-side gate driver control input. This pin controls the output of the low-side gate driver. This pin can be configured to output buffer of phase comparator by SPI register bit PHC_OUTEN.
INHC	15	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.

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Table 4-1. Pin Functions 48-QFP (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
INLC	16	I/O	Low-side gate driver control input. This pin controls the output of the low-side gate driver. This pin can be configured to output buffer of phase comparator by SPI register bit PHC_OUTEN.
SDO	17	O	Serial data output.
SDI	18	I	Serial data input.
SCLK	19	I	Serial clock input.
nSCS	20	I	Serial chip select.
nSLEEP	21	I	Gate driver nSLEEP. When this pin is logic low the device goes to a low-power sleep mode.
nFAULT	22	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pullup resistor.
VREF	23	PWR	External voltage reference for current sense amplifiers.
SOC	24	O	Current sense amplifier output.
SOB	25	O	Current sense amplifier output.
SOA	26	O	Current sense amplifier output.
GND	27	PWR	Device ground
CPL	28	PWR	Charge pump switching node. Connect a flying capacitor between the CPH and CPL pins.
CPH	29	PWR	Charge pump switching node. Connect a flying capacitor between the CPH and CPL pins.
GVDD	30	PWR	Gate driver power supply output. Connect a GVDD-rated ceramic between the GVDD and GND pins.
PVDD	31	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect a PVDD-rated ceramic between the PVDD and GND pins.
CPTL	32	PWR	Trickle charge pump switching node. Connect a charge pump flying capacitor between CPTL and CPTH pins.
CPTH	33	PWR	Trickle charge pump switching node. Connect a charge pump flying capacitor between CPTL and CPTH pins.
VCP	34	PWR	Trickle charge pump storage capacitor. Connect a ceramic capacitor between VCP and VDRAIN pins.
VDRAIN	35	PWR	High-side drain sense and charge pump power supply input.
BSTA	36	O	Bootstrap output pin. Connect a bootstrap capacitor between BSTA and SHA
SHA	37	I	High-side source sense input. Connect to the high-side power MOSFET source.
GHA	38	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	39	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
SLA	40	I	Low-side source sense input. Connect to the low-side power MOSFET source.
SLB	41	I	Low-side source sense input. Connect to the low-side power MOSFET source.
GLB	42	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GHB	43	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
SHB	44	I	High-side source sense input. Connect to the high-side power MOSFET source.
BSTB	45	O	Bootstrap output pin. Connect a bootstrap capacitor between BSTB and SHB
BSTC	46	O	Bootstrap output pin. Connect a bootstrap capacitor between BSTC and SHC
SHC	47	I	High-side source sense input. Connect to the high-side power MOSFET source.
GHC	48	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
PAD	N/A	N/A	Exposed pad. Connect to the GND plane with the best heat sinking ability.This pad is not used as an electrical connection to GND for circuit operation.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output., PWR = Power

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5 Specification

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	PVDD	-0.3	65	V
High-side MOSFET drain pin voltage	VDRAIN	-0.3	65	V
Voltage difference between ground pins	AGND, GND	-0.3	0.3	V
Charge pump pin voltage	CPH	-0.3	V_{GVDD} + 0.3	V
Charge pump pin voltage	CPL	-0.3	V_{GVDD} + 0.9 V_{PVDD} + 0.6	V
Trickle Charge pump high-side pin voltage	CPTH	-0.3	80	V
Trickle Charge pump low-side pin voltage	CPTL	-0.3	V_{VDRAIN} + 0.3	V
Trickle Charge pump output pin voltage	VCP	-0.3	80	V
Gate driver regulator pin voltage V_{GVDD}	GVDD	-0.3	18	V
Logic pin voltage	nSLEEP	-0.3	65	V
Logic pin voltage	DRVOFF	-0.3	65	V
Logic pin voltage	INHx, INLx, nFAULT, SCLK, SDO, SDI, nSCS	-0.3	6.5	V
Logic pin voltage	INHx, INLx, nFAULT, SCLK, SDO, SDI, nSCS : Transient	-0.3	7.0	V
Bootstrap pin voltage	BSTx, Continuous	-0.3	80	V
	BSTx with respect to SHx	-0.3	20	V
	BSTx with respect to GHx	-0.3	20	V
Bootstrap pin transient current	BSTx, Transient (500 ns), Assumed external component R_{BST} = 2Ω and condition V(R_{BST}) = -7V,		3.5	A
High-side gate drive pin voltage	GHx, Continuous	–8	80	V
High-side gate drive pin voltage	GHx, Transient 1us	–15	80	V
High-side gate drive pin voltage with respect to SHx	GHx - SHx	–0.3	BSTx + 0.3	V
High-side source pin voltage	SHx, Continuous	–8	70	V
High-side source pin voltage	SHx, Transient 1us	–15	72	V
Low-side gate drive pin voltage	GLx with respect to SLx (LSS)	-0.3	20	V
Low-side gate drive pin voltage	GLx with respect to GVDD, V_{GLx} - V_{GVDD} if V_{GLx} > V_{GVDD}		0.3	V
Low-side gate drive pin voltage	GLx, Continuous	-8	20	V
Low-side gate drive pin voltage	GLx, Transient 1us	-15	20	V
Low-side source sense pin voltage	SLx, Continuous	–8	V_{GVDD}	V
Low-side source sense pin voltage	SLx, Transient 1us	–15	V_{GVDD}	V
Gate drive current	GHx, GLx	Internally Limited	Internally Limited	A
Reference input pin voltage	VREF	–0.3	6	V
Shunt amplifier input pin voltage	SNx, SPx, Continuous	–5	5	V
Shunt amplifier input pin voltage	SNx, SPx, Transient 1µs	–15	15	V
Shunt amplifier output pin voltage	SOx	–0.3	VREF + 0.3	V
Power supply transient voltage ramp	PVDD, VDRAIN, VREF		3	V/µs
High-side source slew rate	SHx, V_{BSTx} - V_{SHx} ≥ 5.5V nSLEEP = High and ENABLE_DRV = 1b		4	V/ns
Ambient temperature, T_A	Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	Junction temperature, T_J	–40	150	°C

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over operating temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

5.2 ESD Ratings DRV8334

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	PVDD Full device functionality. Operation at PVDD = 4.5V only when coming from higher PVDD. Minimum PVDD for startup = 4.85V	4.5		36	V
V_{VM}	Power supply voltage for logic operation	PVDD, Logic and SPI functional after battery falling from min PVDD for startup (during battery cranking after coming from full device functionality)	4.0		60	V
V_{VDRAIN}	High-side MOSFET Drain voltage	VDRAIN, Full functionality	4.5		60	V
V_{VDRAIN}	High-side MOSFET Drain voltage	VDRAIN, Limited functionality (VDS monitor). GVDD, TCP/VCP, BST and Gate drivers are functional.	0		60	V
V_{BST}	Bootstrap pin voltage with respect to SHx	nSLEEP = High, PWM switching, Gate Driver functional (1)	3.9		20	V
I_{VCP}	VCP external load	VCP, PVDD < 8V			3	mA
I_{VCP}	VCP external load	VCP, PVDD > 8V			5	mA
V_{IN}	Logic input voltage	DRVOFF, INHx, INLx	0		5.5	V
V_{IN}	Logic input voltage	nSLEEP,	0		60	V
V_{IN}	Logic input voltage	SCLK, SDI, nSCS	0		5.5	V
V_{OD}	Open drain pullup voltage	nFAULT			5.5	V
I_{OD}	Open drain output pull-up resistor	nFAULT	5			KΩ
I_{OD}	Open drain output current	SDO, PHC, DC condition			-1	mA
I_{GS}	Total average gate-drive current (Low Side and High Side Combined)	I_{GHx}. I_{GLx}			50	mA
V_{VREF}	Current sense amplifier reference voltage	VREF	3		5.5	V
V_{SL}	DC voltage of SLx	SLx pin, DC condition	-2		2	V
V_{CM_CSA}	Current sense input common mode voltage	SP, SN	–2		2	V
T_A	Operating ambient temperature		–40		125	°C

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over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature	–40		150	°C

(1) V_{BST} needs to be reviewed by users with over / under voltage detection threshold V_{BST_OV}/V_{BST_UV} as well as the requirements of external MOSFET .

5.4 Thermal Information

THERMAL METRIC(1)		DRV8334 PHP (QFP) 48 PINS	DRV8334 RGZ (QFN) PREVIEW 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.0	23.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.6	11.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.0	6.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.9	6.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	1.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (PVDD)						
I_{PVDDQ}	PVDD sleep mode current	V_{PVDD} = 12 V, nSLEEP = 0, T_A = 25°C, I_{PVDDQ} = PVDD + VDRAIN		16	20	µA
I_{PVDDQ}	PVDD sleep mode current	V_{PVDD} = 24 V, nSLEEP = 0, T_A = 25°C, I_{PVDDQ} = PVDD + VDRAIN		16	30	µA
I_{PVDDQ}	PVDD sleep mode current	V_{PVDD} = < 36V, nSLEEP = 0, TJ < 150C, I_{PVDDQ} = PVDD + VDRAIN		18	50	µA
I_{PVDD}	PVDD active mode current	V_{PVDD} = 24 V, nSLEEP = HIGH, INHx = INLX = Low. No FETs connected, I_{PVDD} = PVDD + VDRAIN, V_{DRAIN} = 24 V		28	38	mA
I_{PVDD}	PVDD active mode current	V_{PVDD} = 60 V, nSLEEP = HIGH, INHx = INLX = Low. No FETs connected, I_{PVDD} = PVDD + VDRAIN, V_{DRAIN} = 60 V, VCP_MODE = 00b, 01b, 11b		50		mA
I_{PVDD}	PVDD active mode current	V_{PVDD} = 24 V, nSLEEP = HIGH, INHx = INLX = Switching@20kHz, No FETs connected, I_{PVDD} = PVDD + VDRAIN		25	40	mA
I_{PVDD}	PVDD active mode current	V_{PVDD} = 60 V, nSLEEP = HIGH, INHx = INLX = Switching@20kHz. No FETs connected, I_{PVDD} = PVDD + VDRAIN, V_{DRAIN} = 60 V, VCP_MODE = 00b, 01b, 11b		55		mA
t_{WAKE}	Turn-on time	nSLEEP = Low to High; nFAULT goes High.		1	5	ms
LOGIC-LEVEL INPUTS (INHx, INLx, nSLEEP etc)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		2.1			V

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4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS}	Input hysteresis		200	330	450	mV
V_{IL}	DRVOFF Input logic low voltage	DRVOFF			0.65	V
V_{IH}	DRVOFF Input logic high voltage	DRVOFF	2.1			V
V_{HYS}	DRVOFF Input hysteresis	DRVOFF	200	400	600	mV
R_{PD}	Input pulldown resistance	To GND; INHx, INLx, SCLK, SDI	50	100	150	kΩ
R_{PD}	Input pulldown resistance	nSLEEP, DRVOFF	460	800	1700	kΩ
I_{IL}	Input logic low current	V_I = 0 V; nSCS (internal pull up); VIO = 3.3V	11	33	66	µA
I_{IL}	Input logic low current	V_I = 0 V; nSCS (internal pull up); VIO = 5V	25	50	100	µA
I_{IH}	Input logic high current	V_I = 5 V, INHx/INLx/SDI/SCLK	30	50	70	µA
V_{IH}	nSleep Input logic high voltage				2.1	V
V_{IL}	nSleep Input logic low voltage		0.8			V
V_{HYST}	nSleep Input logic hysteresis		0.1			V
LOGIC-LEVEL OUTPUTS (nFAULT, SDO, PHCx)						
V_{OL}	Output logic low voltage	I_{DOUT} = 1 mA, PHCOMP			0.5	V
V_{OL}	Output logic low voltage	I_{DOUT} = 1 mA, SDO			0.5	V
V_{OH}	Output logic high voltage	I_{DOUT} = 1 mA, SDO, 3.3V mode	2.7	3.3	3.6	V
V_{OH}	Output logic high voltage	I_{DOUT} = 1 mA, PHCOMP, 5V mode; V_{PVDD} ≥ 4.5V	4.0	5	5.5	V
V_{OH}	Output logic high voltage	I_{DOUT} = 1 mA, SDO, 5V mode; V_{PVDD} ≥ 4.5V	4.0	5	5.5	V
V_{OH}	Output logic high voltage	I_{DOUT} = 1 mA, SDO, 5V mode; 4V ≤V_{PVDD} < 4.5V	3.6	3.8	4.5	V
I_{OZ}	Output logic high current	nFAULT : Force nFAULT = 5 V, no fault event, nSLEEP = High SDO : Force V_{SDO} = 5V, nSCS = High or nSLEEP = Low	–12		25	µA
I_{OZ}	Output logic high current	SDO : Force V_{SDO} = 0V, nSCS = High or nSLEEP = Low	–12		10	µA
CHARGE PUMP (GVDD, VCP)						
V_{GVDD}	GVDD Gate driver regulator voltage (LDO mode)	22 V ≤V_{PVDD} ; I_{GS} ≤50 mA	11.5		13.5	V
		18 V ≤V_{PVDD} ≤ 22 V; I_{GS} ≤ 50 mA	11.5		13.5	V
	GVDD Gate driver regulator voltage (Charge pump mode)	7.2 V ≤V_{PVDD} ≤ 18 V; I_{GS} = 50 mA ; I_{VCP} = 5mV	11.5		13.5	V
		6.5 V ≤V_{PVDD} ≤ 7.2 V; I_{GS} ≤ 20 mA; I_{VCP} = 3mA DIS_GVDD_SS = 1b	11.5		13.5	V
		5 V ≤V_{PVDD} ≤ 6.5 V; I_{GS} ≤ 20 mA; I_{VCP} = 3mA DIS_GVDD_SS = 1b	9		13	V
		4.5 V ≤V_{PVDD} ≤ 5 V; I_{GS} ≤ 20 mA, I_{VCP} = 3mA; DIS_GVDD_SS = 1b	8		10	V
V_{VCP}	VCP charge pump voltage (with respect to VDRAIN)	V_{VCP} = $V_{(VCP - VDRAIN)}$; 13.5 ≥ GVDD ≥ 11 V; V_{DRAIN} > 4.5V; I_{VCP} 5 mA;	9.8		13.5	V
		V_{VCP} = $V_{(VCP - VDRAIN)}$; 9V ≤ GVDD < 11V; V_{DRAIN} > 4.5V; I_{VCP} = 3 mA;	8.4		11	
		V_{VCP} = $V_{(VCP - VDRAIN)}$; 8V ≤ GVDD < 9V; V_{DRAIN} > 4.5V; I_{VCP} = 3 mA;	7.4		9	

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4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BST_PRECHG}	VCP charge pump bootstrap cap pre-charge time	$V_{BST-SHX}$ = 5V ;INHx = INLx = Low. Tj = 150C, I_{VCP} = 3mA; C_{VCP} = 1.5uF; C_{BST} = 1.5uF (each phase), C_{VCP_FLY} = 1uF; V_{PVDD} = 4.5V		1.7	3	ms
V_{BST_TCPOFF}	BST monitor voltage for VCP to stop charging the BST cap (rising voltage)	INLx = 0; SHx = 0, VDRAIN; VDRAIN = PVDD = 12V, 60V;	12.0	13.2	14.6	V
BOOTSTRAP DIODES						
V_{BOOTD}	Bootstrap diode forward voltage	I_{BOOT} = 100 µA.			0.85	V
		I_{BOOT} = 10 mA.			1	V
		I_{BOOT} = 100 mA. T_J < 175℃			1.67	V
R_{BOOTD}	Bootstrap dynamic resistance ($\Delta V_{BOOTD}/\Delta I_{BOOT}$)	I_{BOOT} = 100 mA and 50 mA.		5.5		Ω
GATE DRIVERS (GHx, GLx, SHx, SLx)						
VGL_L	Low-side Low-level output voltage	IGLx = 10mA, GLx - SLx; IDRVN = 100100b: IHOLD_SEL = 0b; V_{GVDD} = 12V;	0		0.2	V
VGL_H	Low-side High-level output voltage	IGLx = 10mA, GVDD - GLx ; IDRVP = 100100b ; IHOLD_SEL = 0b; V_{GVDD} = 12V;	0		0.2	V
VGH_L	High-side Low-level output voltage	IGHx = 10mA, GHx - SHx; IDRVN = 100100b ; IHOLD_SEL = 0b; V_{GVDD} = 12V;	0		0.2	V
VGH_H	High-side High-level output voltage	IGHx = 10mA, BSTx - GHx; IDRVP = 100100b ; IHOLD_SEL = 0b; V_{GVDD} = 12V;	0		0.2	V
R_{PDSA_LS}	Low side semi active pull down resistor	GLx to SLx; nSLEEP = Low, V_{GLx} - V_{SLx} = 2V, GVDD (BSTx-SHx) > 2V	2	3	4.3	kΩ
R_{PDSA_HS}	High side semi active pull down resistor	GHx to SHx; nSLEEP = Low, V_{GHx} - V_{SHx} = 2V, GVDD (BSTx-SHx) > 2V	7	9	12	kΩ

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4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRVN}	Peak sink gate current	IDRVN=000000b; VGSx = 5V; BST-SHx = GVDD = 12V		0.75		mA
		IDRVN=000001b; VGSx = 5V; BST-SHx = GVDD = 12V		1.1		
		IDRVN=000010b; VGSx = 5V; BST-SHx = GVDD = 12V		1.5		
		IDRVN=000011b; VGSx = 5V; BST-SHx = GVDD = 12V		1.9		
		IDRVN=000100b; VGSx = 5V; BST-SHx = GVDD = 12V		2.3		
		IDRVN=000101b; VGSx = 5V; BST-SHx = GVDD = 12V		2.8		
		IDRVN=000110b; VGSx = 5V; BST-SHx = GVDD = 12V		3.4		
		IDRVN=000111b; VGSx = 5V; BST-SHx = GVDD = 12V		3.9		
		IDRVN=001000b; VGSx = 5V; BST-SHx = GVDD = 12V		4.4		
		IDRVN=001001b; VGSx = 5V; BST-SHx = GVDD = 12V		5.3		
		IDRVN=001010b; VGSx = 5V; BST-SHx = GVDD = 12V		6.3		
		IDRVN=001011b; VGSx = 5V; BST-SHx = GVDD = 12V		7.2		
		IDRVN=001100b; VGSx = 5V; BST-SHx = GVDD = 12V		8.1		
		IDRVN=001101b; VGSx = 5V; BST-SHx = GVDD = 12V		10		
		IDRVN=001110b; VGSx = 5V; BST-SHx = GVDD = 12V		11		
		IDRVN=001111b; VGSx = 5V; BST-SHx = GVDD = 12V		13		
		IDRVN=010000b; VGSx = 5V; BST-SHx = GVDD = 12V		14		
		IDRVN=010001b; VGSx = 5V; BST-SHx = GVDD = 12V		16		
		IDRVN=010010b; VGSx = 5V; BST-SHx = GVDD = 12V		18		
		IDRVN=010011b; VGSx = 5V; BST-SHx = GVDD = 12V		21		
		IDRVN=010100b; VGSx = 5V; BST-SHx = GVDD = 12V		25		
		IDRVN=010101b; VGSx = 5V; BST-SHx = GVDD = 12V		29		

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4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRVN}	Peak sink gate current	IDRVN=010110b; VGSx = 5V; BST-SHx = GVDD = 12V		33		mA
		IDRVN=010111b; VGSx = 5V; BST-SHx = GVDD = 12V		38		
		IDRVN=011000b; VGSx = 5V; BST-SHx = GVDD = 12V		44		
		IDRVN=011001b; VGSx = 5V; BST-SHx = GVDD = 12V		49		
		IDRVN=011010b; VGSx = 5V; BST-SHx = GVDD = 12V		68		
		IDRVN=011011b; VGSx = 5V; BST-SHx = GVDD = 12V		79		
		IDRVN=011100b; VGSx = 5V; BST-SHx = GVDD = 12V		88		
		IDRVN=011101b; VGSx = 5V; BST-SHx = GVDD = 12V		106		
		IDRVN=011110b; VGSx = 5V; BST-SHx = GVDD = 12V		125		
		IDRVN=011111b; VGSx = 5V; BST-SHx = GVDD = 12V		144		
		IDRVN=100000b; VGSx = 5V; BST-SHx = GVDD = 12V		163		
		IDRVN=100001b; VGSx = 5V; BST-SHx = GVDD = 12V		191		
		IDRVN=100010b; VGSx = 5V; BST-SHx = GVDD = 12V		219		
		IDRVN=100011b; VGSx = 5V; BST-SHx = GVDD = 12V		247		
I_{DRVP}	Peak source gate current	IDRV_CFG = 0b; IDRV_RATIO = 00b; IDRVN = 00000b to 100011b ; VGSx = 5V; BST-SHx = GVDD = 12V		1*I_{DRVN}		mA
		IDRV_CFG = 0b; IDRV_RATIO = 01b; IDRVN = 00000b to 100011b ; VGSx = 5V; BST-SHx = GVDD = 12V		0.75*I_{DRVN}		mA
		IDRV_CFG = 0b; IDRV_RATIO = 10b; IDRVN = 00000b to 100011b ; VGSx = 5V; BST-SHx = GVDD = 12V		0.5*I_{DRVN}		mA
		IDRV_CFG = 0b; IDRV_RATIO = 11b; IDRVN = 00000b to 100011b ; VGSx = 5V; BST-SHx = GVDD = 12V		0.25*I_{DRVN}		mA
I_{DRVN_VAR}	Peak sink gate current variation	IDRVN=000000b - 011001b	-50		+50	%
I_{DRVP_VAR}	Peak source gate current variation	IDRVN=011010b - 100011b	-50		+80	%

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4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDRVN	Peak sink gate current - switch mode	IDRVN=100100b; VGSx (GHx-SHx, GLx-SLx) = 12V; BST-SHx = GVDD = 12V. SGD_TMP_EN = 1b	400	600	980	mA
		IDRVN=100101b; VGSx (GHx-SHx, GLx-SLx) = 12V; BST-SHx = GVDD = 12V.	480	695	1020	mA
		IDRVN=100110b; VGSx (GHx-SHx, GLx-SLx) = 12V; BST-SHx = GVDD = 12V.	560	795	1060	mA
		IDRVN=100111b; VGSx (GHx-SHx, GLx-SLx) = 12V; BST-SHx = GVDD = 12V.	640	925	1240	mA
		IDRVN=101000b; VGSx (GHx-SHx, GLx-SLx) = 12V; BST-SHx = GVDD = 12V.	760	1090	1440	mA
		IDRVN=101001b; VGSx (GHx-SHx, GLx-SLx) = 12V; BST-SHx = GVDD = 12V.	880	1255	1660	mA
		IDRVN=101010b; VGSx (GHx-SHx, GLx-SLx) = 12V; BST-SHx = GVDD = 12V.	1020	1455	1920	mA
		IDRVN=101011b; VGSx (GHx-SHx, GLx-SLx) = 12V; BST-SHx = GVDD = 12V.	1080	1685	2500	mA
		IDRVN=101100b; VGSx (GHx-SHx, GLx-SLx) = 12V; BST-SHx = GVDD = 12V.	1080	2000	2600	mA
IDRVP	Peak source gate current - switch mode	IDRVP=100100b; VGSx (GHx-SHx, GLx-SLx) = 0V; GVDD = 12V	150	300	450	mA
IDRVP	Peak source gate current - switch mode	IDRVP=100101b; VGSx (GHx-SHx, GLx-SLx) = 0V; GVDD = 12V	177	355	533	mA
IDRVP	Peak source gate current - switch mode	IDRVP=100110b; VGSx (GHx-SHx, GLx-SLx) = 0V; GVDD = 12V	205	410	615	mA
IDRVP	Peak source gate current - switch mode	IDRVP=100111b; VGSx (GHx-SHx, GLx-SLx) = 0V; GVDD = 12V	237	475	713	mA
IDRVP	Peak source gate current - switch mode	IDRVP=101000b;VGSx (GHx-SHx, GLx-SLx) = 0V; GVDD = 12V	280	560	840	mA
IDRVP	Peak source gate current - switch mode	IDRVP=101001b;VGSx (GHx-SHx, GLx-SLx) = 0V; GVDD = 12V	322	645	968	mA
IDRVP	Peak source gate current - switch mode	IDRVP=101010b; VGSx (GHx-SHx, GLx-SLx) = 0V; GVDD = 12V	375	750	1125	mA
IDRVP	Peak source gate current - switch mode	IDRVP=101011b; VGSx (GHx-SHx, GLx-SLx) = 0V; GVDD = 12V	432	865	1298	mA
IDRVP	Peak source gate current - switch mode	IDRVP=101100b; VGSx (GHx-SHx, GLx-SLx) = 0V; GVDD = 12V	507	1015	1523	mA
I_{HOLD_PU}	Gate pull up hold current	IHOLD_SEL = 1b; BST-SHx = GVDD = 12V.	150	250	400	mA
I_{HOLD_PU}	Gate pull up hold current	IHOLD_SEL = 0b; BST-SHx = GVDD = 12V.	330	560	900	mA
I_{HOLD_PD}	Gate pull down hold current	IHOLD_SEL = 1b; BST-SHx = GVDD = 12V.	140	267	480	mA
I_{HOLD_PD}	Gate pull down hold current	IHOLD_SEL = 0b; BST-SHx = GVDD = 12V.	580	1100	1500	mA
I_{STRONG}	Gate pull down strong current	GHx-SHx = 12V (High side) or GLx = 12V (Low Side); BST-SHx = GVDD = 12V.	1000	2000	2800	mA

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4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVER TIMINGS (GHx, GLx)						
t_{PD}	Input to output propagation delay GHx/GLx falling	INHx, INLx to GHx, GLx. IDRVN = IDRVP = 101000b ; After INHx/INLx falling edge to VGS = VGHS/VGLS – 1 V; V_{GVDD} = $V_{BSTx-SHx}$ ≥ 8V		55	150	ns
t_{PD}	Input to output propagation delay GHx/GLx falling	INHx, INLx to GHx, GLx. IDRVN = IDRVP = 011101b ; After INHx/INLx falling edge to VGS = VGHS/VGLS – 1 V; V_{GVDD} = $V_{BSTx-SHx}$ ≥ 8V		75	150	ns
t_{PD}	Input to output propagation delay GHx/GLx rising	INHx, INLx to GHx, GLx. IDRVN = IDRVP = 101000b; After INHx/INLx rising edge to VGS = 1 V; V_{GVDD} = $V_{BSTx-SHx}$ ≥ 8V		55	150	ns
t_{PD}	Input to output propagation delay GHx/GLx rising	INHx, INLx to GHx, GLx.IDRVN = IDRVP = 011101b; After INHx/INLx rising edge to VGS = 1 V; V_{GVDD} = $V_{BSTx-SHx}$ ≥ 8V		70	150	ns
t_{PD_match}	Matching propagation delay per phase	GHx turning OFF to GLx turning ON, GLx turning OFF to GHx turning ON; V_{GVDD} = $V_{BSTx-SHx}$ ≥ 8V	–150	10	150	ns
t_{PD_match}	Matching propagation delay phase to phase	GHx/GLx turning ON to GHy/GLy turning ON, GHx/GLx turning OFF to GHy/GLy turning OFF; V_{GVDD} = $V_{BSTx-SHx}$ ≥ 8V	–50	10	50	ns
t_{DRIVE}	Peak current gate drive time	Typical value.TDRVP (TDRVN) = 0000b - 1111b. Refer to register map TDRNP and TDRVN.	140		3815	ns
t_{DRIVE_V}	Peak current gate drive time variation	With respect to typical value.TDRVP (TDRVN) = 0000b - 1111b	-20		20	%
t_{DEAD}	Digital Gate drive dead time	DEADTIME = 000b;	30	70	130	ns
		DEADTIME = 001b;	170	214	300	ns
		DEADTIME = 010b	230	286	380	ns
		DEADTIME = 011b	420	500	640	ns
		DEADTIME = 100b	640	750	930	ns
		DEADTIME = 101b	880	1000	1280	ns
		DEADTIME = 110b	1270	1500	1820	ns
		DEADTIME = 111b	1700	2000	2400	ns
CURRENT SHUNT AMPLIFIERS (SNx, SOx, SPx, VREF)						
A_{CSA}	Sense amplifier gain	CSAGAIN = 0000b		5		V/V
		CSAGAIN = 0001b;		10		V/V
		CSAGAIN = 0010b		12		V/V
		CSAGAIN = 0011b		16		V/V
		CSAGAIN = 0100b		20		V/V
		CSAGAIN = 0101b		23		V/V
		CSAGAIN = 0110b		25		V/V
		CSAGAIN = 0111b		30		V/V
		CSAGAIN = 1000b		40		V/V
EA_{CSA}	Sense amplifier gain error	All CSAGAIN setting V_{GVDD} > 7.2V (this GVDD condition is applied to all CSA items)	-0.5		0.5	%
t_{SET}	Settling time to ±1%	V_{STEP} = 1.6 V, A_{CSA} = 5 V/V, R_{SO} = 160Ω, C_{SO} = 470pF ; VREF = 5V/3V		0.6	1.35	µs
t_{SET}	Settling time to ±1%	V_{STEP} = 1.6 V, A_{CSA} = 10 V/V, C_{LOAD} = 470pF		0.65	1.35	µs

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4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SET}	Settling time to ±1%	V_{STEP} = 1.6 V, A_{CSA} = 20 V/V, R_{SO} = 160Ω, C_{SO} = 470pF VREF = 5V/3V		0.7	1.35	µs
t_{SET}	Settling time to ±1%	V_{STEP} = 1.6 V, A_{CSA} = 30 V/V, R_{SO} = 160Ω, C_{SO} = 470pF VREF = 5V		0.7	1.35	µs
t_{SET}	Settling time to ±1%	V_{STEP} = 1.6 V, A_{CSA} = 30 V/V, R_{SO} = 160Ω, C_{SO} = 470pF VREF = 3V		0.7	1.6	µs
t_{SET}	Settling time to ±1%	V_{STEP} = 1.6 V, A_{CSA} = 40 V/V, R_{SO} = 160Ω, C_{SO} = 470pF VREF = 5V		0.7	1.7	µs
t_{SET}	Settling time to ±1%	V_{STEP} = 1.6 V, A_{CSA} = 40 V/V, R_{SO} = 160Ω, C_{SO} = 470pF VREF = 3V		0.7	1.75	µs
UGB	Unity Gain Bandwidth	C_{LOAD} = 470pF; closed loop, BW @ unity gain	10			MHz
BW	Bandwidth	closed loop, -3db, no output load	1			MHz
V_{SWING}	Output voltage range	V_{VREF} = 3 to 5.5 V	0.25		V_{VREF} - 0.25	V
V_{COM}	Common-mode input range	VCOM = (V_{SP} + V_{SN}) / 2	-2		2	V
t_{com_rec}	Common-mode transient recovery timing	VCOM = -15V to 0V			2.2	µs
V_{DIFF}	Differential-mode input range		-0.3		0.3	V
V_{OFF}	Input offset voltage total	V_{SP} = V_{SN} = GND; Initial offset + Offset drift	–0.65		0.65	mV
V_{OFF_DRIFT}	Input drift offset voltage	V_{SP} = V_{SN} = GND; temperature drift + aging	–0.2		0.2	mV
I_{BIAS}	Input bias current	V_{SP} = V_{SN} = GND. CSA and SENSE_OCP total	20		100	µA
I_{BIAS_OFF}	Input bias current offset	I_{SP} – $I_{SN.}$ CSA and SENSE_OCP total	-1		1	µA
I_{VREF}	Reference input current	V_{CSAREF} = 3.3 V	3	6	9.25	mA
		V_{CSAREF} = 5 V	4	7	9.5	mA
CMRR	DC Common-mode rejection ratio	SN/SP = -2V to 2V	60	90		dB
CMRR	Transient Common-mode rejection ratio	20KHz	60	90		dB
PSRR	Power-supply rejection ratio			100		dB
Temperature Reporting						
SUPPLY VOLTAGE MONITORS						
V_{PVDD_UV}	PVDD undervoltage lockout threshold	V_{PVDD} rising	4.5	4.65	4.8	V
		V_{PVDD} falling	4.05	4.2	4.35	
$V_{PVDD_UV_HYS}$	PVDD undervoltage lockout hysteresis	Rising to falling threshold	400	450	500	mV
$t_{PVDD_UV_DG}$	PVDD undervoltage deglitch time	rising and falling edge	8	12	16	µs
V_{PVDD_UVW}	PVDD undervoltage warning threshold	V_{PVDD} rising; PVDD_UVW_LVL= 0b;	6.0		7	V
		V_{PVDD} falling; PVDD_ULW_LVL= 0b;	5.8		6.8	V
		V_{PVDD} rising; PVDD_UVW_LVL = 1b;	7.3		8.3	V
		V_{PVDD} falling; PVDD_UVW_LVL = 1b;	7.1		8.1	V
$V_{PVDD_UVW_HYS}$	PVDD undervoltage warning hysteresis	Rising to falling threshold	140	200	260	mV
$t_{PVDD_UVW_DG}$	PVDD undervoltage warning deglitch time	rising and falling edge	8	12	16	µs

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4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PVDD_OV}	PVDD overvoltage threshold	V_{PVDD} rising, PVDD_OV_LVL = 00b	28		31	V
		V_{PVDD} falling, PVDD_OV_LVL = 00b	27		30	
		V_{PVDD} rising, PVDD_OV_LVL = 01b	33		36	
		V_{PVDD} falling, PVDD_OV_LVL = 01b	32		35	
		V_{PVDD} rising, PVDD_OV_LVL = 10b	50		55	
		V_{PVDD} falling, PVDD_OV_LVL = 10b	47		52	
$V_{PVDD_OV_HYS}$	PVDD overvoltage hysteresis	Rising to falling threshold PVDD_OV_LVL = 00b, 01b	0.6	0.9	1.2	V
$V_{PVDD_OV_HYS}$	PVDD overvoltage hysteresis	Rising to falling threshold PVDD_OV_LVL = 10b	2.0	2.2	2.4	V
$t_{PVDD_OV_DG}$	PVDD overvoltage deglitch time	rising and falling edge	8	12	16	µs
V_{GVDD_UV}	GVDD undervoltage threshold	V_{GVDD} rising - after power up	7.0		7.8	V
		V_{GVDD} rising - power up only	7.5		8.1	V
		V_{GVDD} falling	6.8		7.6	V
$V_{GVDD_UV_HYS}$	GVDD undervoltage hysteresis	Rising to falling threshold	185	215	245	mV
$t_{GVDD_UV_DG}$	GVDD undervoltage deglitch time	rising and falling edge	8	12	16	µs
V_{GVDD_OV}	GVDD overvoltage threshold	V_{GVDD} rising	15		17	V
V_{GVDD_OV}	GVDD overvoltage threshold	V_{GVDD} falling	14.5		16.5	V
$V_{GVDD_OV_HYS}$	GVDD overvoltage hysteresis	Rising to falling threshold	490	560	620	mV
$t_{GVDD_OV_DG}$	GVDD overvoltage deglitch time	rising and falling edge	8	12	16	µs
V_{BST_UV}	Bootstrap undervoltage threshold	V_{BSTx}- V_{SHx}; V_{BSTx} rising; BST_UV_LVL = 1b	6.3	7.4	8.5	V
V_{BST_UV}	Bootstrap undervoltage threshold	V_{BSTx}- V_{SHx}; V_{BSTx} falling; BST_UV_LVL = 1b	6.1	7.2	8.3	V
V_{BST_UV}	Bootstrap undervoltage threshold	V_{BSTx}- V_{SHx}; V_{BSTx} rising; BST_UV_LVL = 0b	3.8	4.4	5	V
		V_{BSTx}- V_{SHx}; V_{BSTx} falling; BST_UV_LVL = 0b	3.65	4.2	4.8	V
$V_{BST_UV_HYS}$	Bootstrap undervoltage hysteresis	Rising to falling threshold BST_UV_LVL = 0b and 1b	120	200	280	mV
$t_{BST_UV_DG}$	Bootstrap undervoltage deglitch time	rising and falling edge	4	5	8	µs
V_{BST_OV}	Bootstrap overvoltage threshold	V_{BSTx}- V_{SHx}; V_{BSTx} rising	15.2		18	V
V_{BST_OV}	Bootstrap overvoltage threshold	V_{BSTx}- V_{SHx}; V_{BSTx} falling	15		17.8	V
$V_{BST_OV_HYS}$	Bootstrap overvoltage hysteresis		130	200	260	mV
$t_{BST_OV_DG}$	Bootstrap overvoltage deglitch time	rising and falling edge	8	12	16	µs
V_{CP_UV}	VCP undervoltage threshold	VCP - VDRAIN; rising	6	6.7	7.4	V
V_{CP_UV}	VCP undervoltage threshold	VCP - VDRAIN; falling	5.7	6.4	7.1	V
$t_{CP_UV_DG}$	VCP undervoltage deglitch time	rising and falling edge	8	12	16	µs
V_{CP_OV}	VCP overvoltage threshold	VCP - VDRAIN; rising	14		17.0	V
V_{CP_OV}	VCP overvoltage threshold	VCP - VDRAIN; falling	13.8		16.7	V
$t_{CP_OV_DG}$	VCP overvoltage deglitch time	rising and falling edge	8	12	16	µs
V_{DRAIN_UV}	VDRAIN undervoltage threshold	V_{VDRAIN} rising	4.25	4.35	4.45	V
V_{DRAIN_UV}	VDRAIN undervoltage threshold	V_{VDRAIN} falling	4.05	4.15	4.25	V
$V_{DRAIN_UV_HYS}$	VDRAIN undervoltage hysteresis		170	190	210	mV

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4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{VDRAIN_UV_DG}$	VDRAIN undervoltage deglitch time	rising and falling edge	8	12	16	µs
V_{DRAIN_OV}	VDRAIN overvoltage threshold	V_{VDRAIN} rising, VDRAIN_OV_LVL = 00b	28		31	V
		V_{VDRAIN} falling, VDRAIN_OV_LVL = 00b	27		30	V
		V_{VDRAIN} rising, VDRAIN_OV_LVL = 01b	33		36	V
		V_{VDRAIN} falling, VDRAIN_OV_LVL = 01b	32		35	V
		V_{VDRAIN} rising, VDRAIN_OV_LVL = 10b, 11b	50		55	V
		V_{VDRAIN} falling, VDRAIN_OV_LVL = 10b, 11b	48		353	V
$V_{DRAIN_OV_HYS}$	VDRAIN overvoltage hysteresis	Rising to falling threshold, VDRAIN_OV_LVL = 00b, 01b	0.7	1.0	1.3	V
$V_{DRAIN_OV_HYS}$	VDRAIN overvoltage hysteresis	Rising to falling threshold, VDRAIN_OV_LVL = 10b, 11b	2.0	2.3	2.6	V
$t_{VDRAIN_OV_DG}$	VDRAIN overvoltage deglitch time	rising and falling edge	8	12	16	µs
PROTECTION CIRCUITS						
$V_{GS_LVL_H}$	Gate voltage monitor threshold	V_{GHx} – V_{SHx}, V_{GLx} – V_{SLx}, INLx / INHx=H; VGS_LVL = 1'b1	7		8.5	V
$V_{GS_LVL_H}$	Gate voltage monitor threshold	V_{GHx} – V_{SHx}, V_{GLx} – V_{SLx}, INLx / INHx=H; VGS_LVL = 1'b0	5		6.3	V
$V_{GS_LVL_L}$	Gate voltage monitor threshold	V_{GHx} – V_{SHx}, V_{GLx} – V_{SLx}, INLx / INHx=L		1	2	V
t_{GS_DG}	VGS gate voltage monitor deglitch time	VGS_DG = 000b	0.3	0.6	0.8	µs
		VGS_DG = 001b	0.6	1.0	1.3	µs
		VGS_DG = 010b,	1.1	1.5	1.9	µs
		VGS_DG = 011b, VGS_DG = 1xxb	1.6	2.0	2.5	µs
t_{GS_BLK}	VGS gate voltage monitor blanking time	VGS_BLK = 000b	1.7	2.25	2.9	µs
		VGS_BLK = 001b	2.4	3	3.6	µs
		VGS_BLK = 010b	4.0	5	5.8	µs
		VGS_BLK = 011b	5.9	7	8.2	µs
		VGS_BLK = 100b, 101b, 110b, 111b	8.6	10	11.9	µs

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4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DS_LVL}	V_{DS} overcurrent protection threshold	VDS_LVL = 0000b; SLx = -0.2V to +2.0V. VDS_CM = 0b. !! TOSHIO UPDATE ! Tj <= 150	0.04	0.06	0.085	V
		VDS_LVL = 0001b; SLx = -0.2V to +2.0V. VDS_CM = 0b. !! TOSHIO UPDATE ! Tj <= 150	0.06	0.08	0.11	
		VDS_LVL = 0010b; SLx = -0.3V to +2.0V. VDS_CM = 0b. ! TOSHIO UPDATE ! Tj <= 150	0.075	0.10	0.13	
		VDS_LVL = 0011b; SLx = -0.3V to +2.0V. !! TOSHIO UPDATE ! Tj <= 150	0.09	0.12	0.16	
		VDS_LVL = 0100b; SLx = -0.3V to +2.0V.	0.13	0.16	0.20	
		VDS_LVL = 0101b; SLx = -0.3V to +2.0V.	0.2	0.24	0.29	
		VDS_LVL = 0110b; SLx = -0.3V to +2.0V.	0.27	0.32	0.385	
		VDS_LVL = 0111b; SLx = -0.3V to +2.0V.	0.35	0.4	0.48	
		VDS_LVL = 1000b; SLx = -0.3V to +2.0V.	0.44	0.5	0.58	
		VDS_LVL = 1001b; SLx = -0.3V to +2.0V.	0.59	0.67	0.77	
		VDS_LVL = 1010b; SLx = -0.3V to +2.0V.	0.75	0.83	0.96	
		VDS_LVL = 1011b; SLx = -0.3V to +2.0V.	0.90	1	1.15	
		VDS_LVL = 1100b; SLx = -0.3V to +2.0V.	1.13	1.25	1.42	
		VDS_LVL = 1101b; SLx = -0.3V to +2.0V.	1.36	1.5	1.70	
		VDS_LVL = 1110b;SLx = -0.3V to +2.0V.	1.58	1.75	1.98	
		VDS_LVL = 1111b;SLx = -0.3V to +2.0V.	1.81	2	2.26	
tDS_CMP	VDS comparator delay	VDS (comparator input voltage) from 0V to max of VDS_LVL (comparator output rising), delay time of internal comparator.		0.5	1.0	µs
tDS_CMP	VDS comparator delay	VDS (comparator input voltage) from VDRAIN to min of VDS_LVL (comparator output falling), delay time of internal comparator.		1.0	1.6	µs
t_{DS_DG}	V_{DS} overcurrent deglitch	VDS_DG = 000b	0.3	0.5	0.8	µs
		VDS_DG = 001b	0.7	1	1.3	
		VDS_DG = 010b	1.2	1.5	2.0	
		VDS_DG = 011b	1.5	2	2.5	
		VDS_DG = 100b	3.3	4	4.8	
		VDS_DG = 101b	5.2	6	7.3	
		VDS_DG = 110b, 111b	6.8	8	9.2	
t_{DS_BLK}	V_{DS} overcurrent blanking time	VDS_BLK = 000b		0	0.2	µs
		VDS_BLK = 001b	0.4	0.5	0.7	
		VDS_BLK = 010b	0.7	1	1.5	
		VDS_BLK = 011b	1.4	2	2.6	
		VDS_BLK = 100b	5.0	6	7.2	
		VDS_BLK = 101b	6.8	8	9.4	
		VDS_BLK = 110b	8.4	10	11.9	
		VDS_BLK = 111b	10.1	12	13.9	

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4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SENSE_LVL}	V_{SENSE} overcurrent threshold	SNS_OCP_LVL = 000b : Input common mode voltage +/-2V	37	50	58	mV
		SNS_OCP_LVL = 001b : Input common mode voltage +/-2V	62	75	84	
		SNS_OCP_LVL = 010b : Input common mode voltage +/-2V	87	100	110	
		SNS_OCP_LVL = 011b : Input common mode voltage +/-2V	112	125	135	
		SNS_OCP_LVL = 100b : Input common mode voltage +/-2V	135	150	165	
		SNS_OCP_LVL = 101b : Input common mode voltage +/-2V	185	200	215	
		SNS_OCP_LVL = 110b : Input common mode voltage +/-2V	280	300	320	
		SNS_OCP_LVL = 111b : Input common mode voltage +/-2V	475	500	525	
t_{SENSE_DG}	V_{SENSE} overcurrent deglitch time	SNS_OCP_DG = 00b	1.5	2.0	2.5	µs
		SNS_OCP_DG = 01b	3.0	4.0	5.0	
		SNS_OCP_DG = 10b	4.5	6.0	7.5	
		SNS_OCP_DG = 11b	8	10.0	12	
V_{PHC_H}	Phase comparator high level threshold over VDRAIN (This is a ratio to VDRAIN voltage)	PHC_THR = 0b	0.6	0.75	0.9	
V_{PHC_H}	Phase comparator high level threshold over VDRAIN (This is a ratio to VDRAIN voltage)	PHC_THR = 1b	0.37	0.52	0.67	
V_{PHC_L}	Phase comparator low level threshold over VDRAIN (This is a ratio to VDRAIN voltage)	PHC_THR = 0b	0.10	0.25	0.40	
V_{PHC_L}	Phase comparator low level threshold over VDRAIN (This is a ratio to VDRAIN voltage)	PHC_THR = 1b	0.33	0.48	0.63	
$t_{PHC_PD_HL}$	Phase comparator propagation delay	Propagation delay of phase comparator High to Low from SHx to PHCx, Cload=20pF; SHx input test condition 60V – 0V / 10ns (design target), From SHx = 88% to 15% of V_{DRAIN}			1.5	µs
$t_{PHC_PD_LH}$	Phase comparator propagation delay	Propagation delay of phase comparator Low to High from SHx to PHCx, Cload=20pF; SHx input test condition 0V – 60V / 10 ns (design target), From SHx = 15% to 88% of V_{DRAIN}			1.5	µs
$t_{PHC_OUT_DEG}$	Phase comparator output deglitch time	PHCOUT_DG_SEL = 1	0.8	1.0	1.4	µs
T_{OTW}	Thermal warning temperature	T_J rising, OT_LVL = 0b;	125		150	°C
T_{OTW_HYS}	Thermal warning hysteresis		15	22	25	°C
t_{OTW_DEG}	Thermal warning deglitch		8	12	16	µs
T_{OTSD}	Thermal shutdown temperature	T_J rising	155		180	°C
T_{OTSD_HYS}	Thermal shutdown hysteresis		16	23	27	°C
t_{OTSD_DEG}	Thermal shutdown deglitch		8	12	16	µs

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4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DRVN_SD}	Gate Drive Shutdown Sequence time			20		µs

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{SCLK}	SCLK minimum period	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns
t_{SU_SDI}	SDI input data setup time	15			ns
t_{H_SDI}	SDI input data hold time	25			ns
t_{D_SDO}	SDO output data delay time; SCLK high to SDO valid (DC VOH x 70% for rise, x30% for fall), C_L = 20pF; PVDD ≥ 4.5V;	5		38	ns
t_{D_SDO}	SDO output data delay time; SCLK high to SDO valid (DC VOH x 70% for rise, x30% for fall), C_L = 20pF; 4.5V ≥ PVDD 4V	5		48	ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{H_nSCS}	nSCS input hold time	25			ns
t_{HI_nSCS}	nSCS minimum high time before active low	450			ns
t_{EN_SDO}	SDO enable delay time; nSCS low to SDO ready			50	ns
t_{DIS_SDO}	SDO disable delay time; nSCS high to SDO high impedance			50	ns

5.7 SPI Timing Diagrams

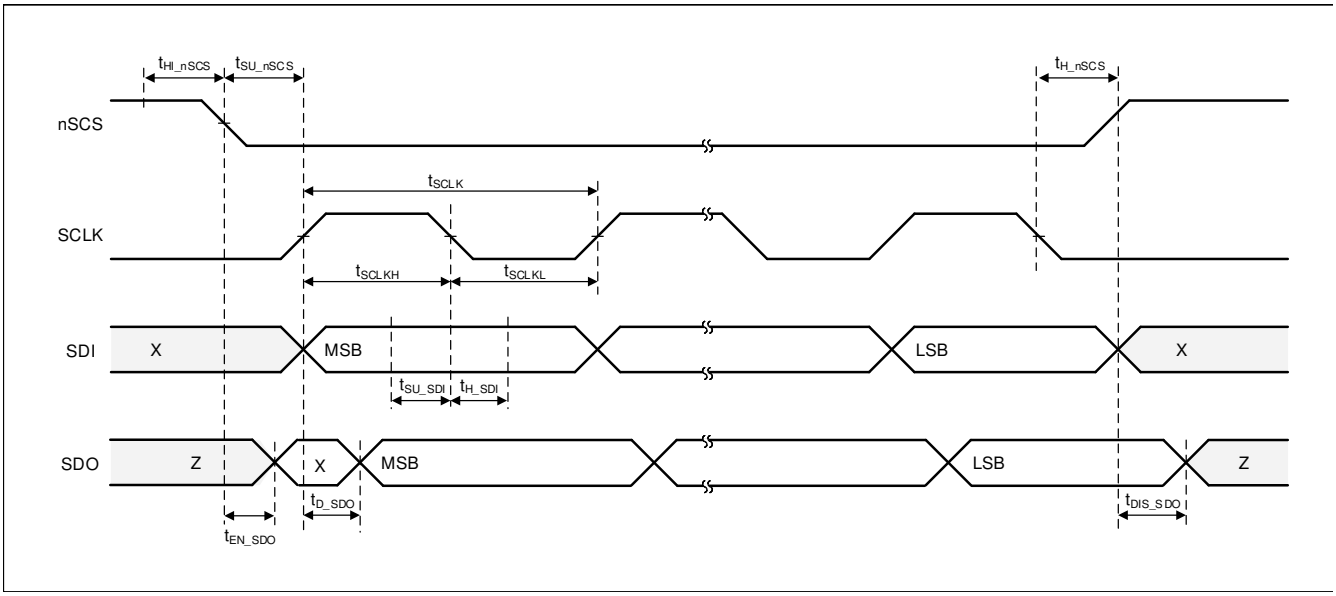

Figure 5-1. SPI Slave Mode Timing Diagram

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6 Detailed Description

6.1 Overview

The DRV8334 is an integrated 4.5V to 60V gate driver for three-phase motor drive applications. The device decreases system component count, cost, and complexity by integrating three independent half-bridge gate drivers, trickle charge pump, and linear regulator for the supply voltages of the high-side and low-side gate drivers. The device also integrates current shunt (or current sense) amplifiers. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller.

The gate driver supports external N-channel high-side and low-side power MOSFETs and can drive up to 1A source, 2A sink peak currents. A bootstrap capacitor generates the supply voltage of the high-side gate drive. The supply voltage of the low-side gate driver is generated using a linear regulator GVDD from the PVDD power supply that regulates to 12V.

A Smart Gate Drive architecture provides the ability to dynamically adjust the strength of the gate drive output current which lets the gate driver control the VDS switching speed of the power MOSFET. This feature lets the user remove the external gate drive resistors and diodes, reducing the component count in the bill of materials (BOM), cost, and area of the printed circuit board (PCB). The architecture also uses an internal state machine to protect against short-circuit events in the gate driver, control the half-bridge dead time, and protect against dV/dt parasitic turn on of the external power MOSFET.

The DRV8334 integrates current sense amplifiers for monitoring current level through all the external half-bridges using a low-side shunt resistor. The gain setting of the current sense amplifier can be adjusted through SPI commands.

In addition to the high level of device integration, the DRV8334 provides a wide range of integrated protection features. These features include power supply under voltage lockout (PVDD UV), regulator under voltage lockout (GVDDUV), VDS over current monitoring (VDS OCP), R_{SENSE} over current monitoring (SNS_OCP), and over temperature shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin.

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6.2 Functional Block Diagram

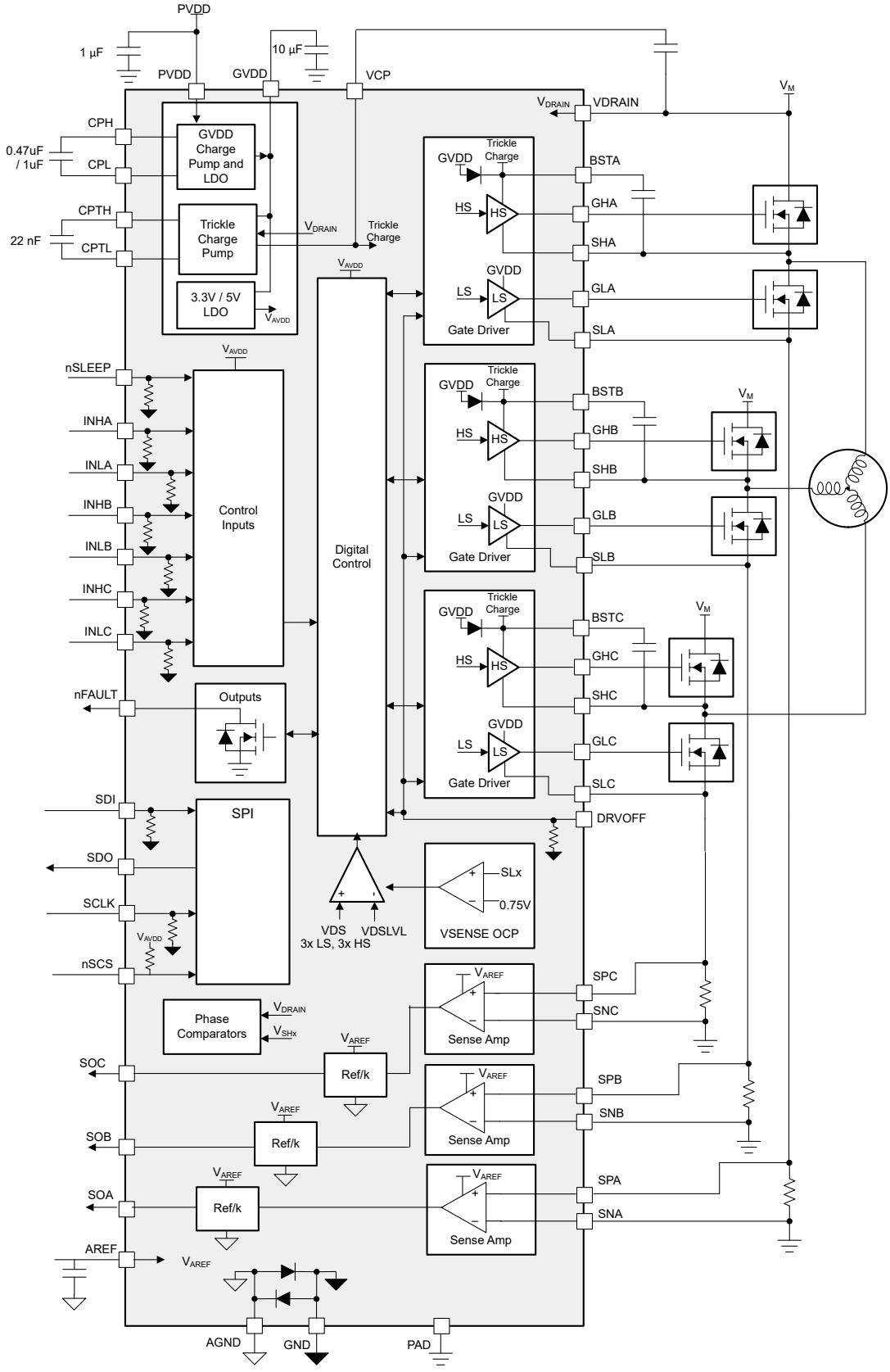

Figure 6-1. Block Diagram of DRV8334

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6.3 Feature Description

6.3.1 Three BLDC Gate Drivers

The DRV8334 integrates three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. A charge pump is used to generate the GVDD to supply the correct gate bias voltage across a wide operating voltage range of the PVDD supply input. The low side gate outputs are driven directly from GVDD, while the high side gate outputs are driven using a bootstrap circuit with an integrated diode. An internal trickle charge pump (VCP) provides 100% duty cycle support and an overdrive voltage of external switches. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

6.3.1.1 PWM Control Modes

The DRV8334 provides four different PWM control modes to support various commutation and control methods. The PWM control mode is adjustable through PWM_MODE register bits.

6.3.1.1.1 6x PWM Mode

In 6x PWM mode, the corresponding INHx and INLx signals control the output state as listed in Table 6-1.

Table 6-1. 6x PWM Mode Truth Table

INLx	INHx	GLx	GHx	Note
0	0	L	L	
0	1	L	H	
1	0	H	L	
1	1	L	L	Shoot through protection

6.3.1.1.2 3x PWM Mode with INLx enable control

In 3x PWM mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to put both high-side and low-side gate drive outputs low. If the state is not required, tie all INLx pins to logic high. The corresponding INHx and INLx signals control the output state as listed in Table 6-2.

Table 6-2. 3x PWM Mode Truth Table

INLx	INHx	GLx	GHx
0	X	L	L
1	0	H	L
1	1	L	H

6.3.1.1.3 3x PWM Mode with SPI enable control

In 3x PWM mode, the INHx pin controls output states of GHx and GLx. If SPI register bit DRVEN_x (x=A,B,C) is 0b, GHx and GLx are pulled low. INLx is not used by the device for PWM control. The corresponding INHx signal and DRVEN_x control the output state as listed in table.

Table 6-3. 3x PWM Mode (SPI Enable Control) Truth Table

DRVEN_x	INL	INHx	GLx	GHx
0	X	X	L	L
1	X	0	H	L
1	X	1	L	H

Note

SPI register bit DRVEN_x is valid for any PWM mode settings.

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6.3.1.1.4 1x PWM Mode

In 1x PWM mode, the device uses 6-step block commutation tables that are stored internally. This feature allows for a three-phase BLDC motor to be controlled using one PWM sourced from a simple controller. The PWM is applied on the INHA pin and determines the output frequency and duty cycle of the half-bridges.

The half-bridge output states are managed by the INLA, INHB, and INLB pins which are used as state logic inputs. The state inputs can be controlled by an external controller or connected directly to the digital outputs of the Hall effect sensor from the motor (INLA = HALL_A, INHB = HALL_B, INLB = HALL_C). The 1x PWM mode usually operates with synchronous rectification (low-side MOSFET recirculation).

The INHC input controls the direction through the 6-step commutation table which is used to change the direction of the motor when Hall effect sensors are directly controlling the state of the INLA, INHB, and INLB inputs. Tie the INHC pin low if this feature is not required.

The INLC input brakes the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when the INLC pin is pulled low. This brake is independent of the state of the other input pins. Tie the INLC pin high if this feature is not required.

Table 6-4. Synchronous 1x PWM Mode (PWM1X_COM = 0b)

LOGIC AND HALL INPUTS							GATE DRIVE OUTPUTS[1]						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	!PWM	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

(1) *!PWM* is the inverse of the PWM signal.

Table 6-5. Asynchronous 1x PWM Mode (PWM1X_COM = 1b)

LOGIC AND HALL INPUTS							GATE DRIVE OUTPUTS						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	L	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	L	L	H	B → C
2	1	0	0	0	1	1	PWM	L	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	L	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	L	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	L	C → A
6	0	1	0	1	0	1	L	H	PWM	L	L	L	B → A

Figure 6-2 and Figure 6-3 show the different possible configurations in 1x PWM mode.

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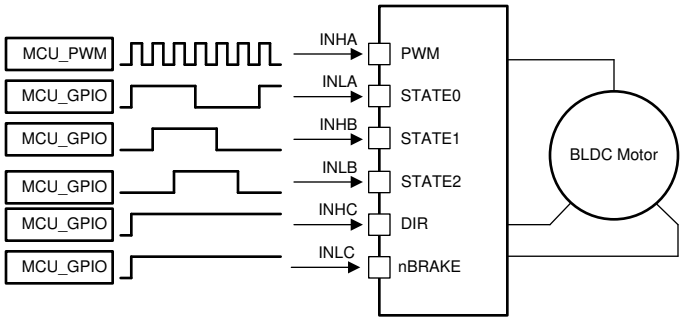

Figure 6-2. 1x PWM—Simple Controller

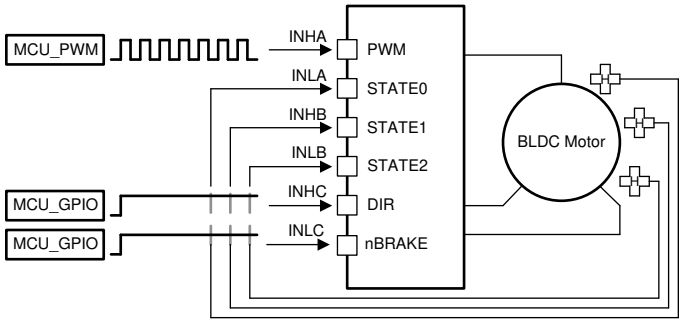

Figure 6-3. 1x PWM—Hall Effect Sensor

6.3.1.1.5 SPI Gate Drive Mode

In SPI Gate Drive Mode, the output state of GLx and GHx are controlled by the corresponding DRV_GLx and DRV_GHx SPI register bits as listed in Table 6-6.

Table 6-6. SPI Gate Drive Mode Truth Table

SPI DRV_GLx	SPI DRV_GHx	GLx	GHx
0	0	L	L
0	1	L	H
1	0	H	L
1	1	L	L

6.3.1.2 Gate Drive Architecture

The gate driver device use a complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates. The low side gate drivers are supplied directly from the GVDD regulator supply. For the high-side gate drivers, a bootstrap diode and capacitor are used to generate the floating high-side gate voltage supply. The bootstrap diode is integrated and an external bootstrap capacitor is used on the BSTx pin. To support 100% duty cycle control, a trickle charge pump is integrated into the device. The trickle charge pump is connected to the BSTx node to prevent bootstrap voltage drop during 100% duty cycle operation due to the leakage currents of the driver and external MOSFET.

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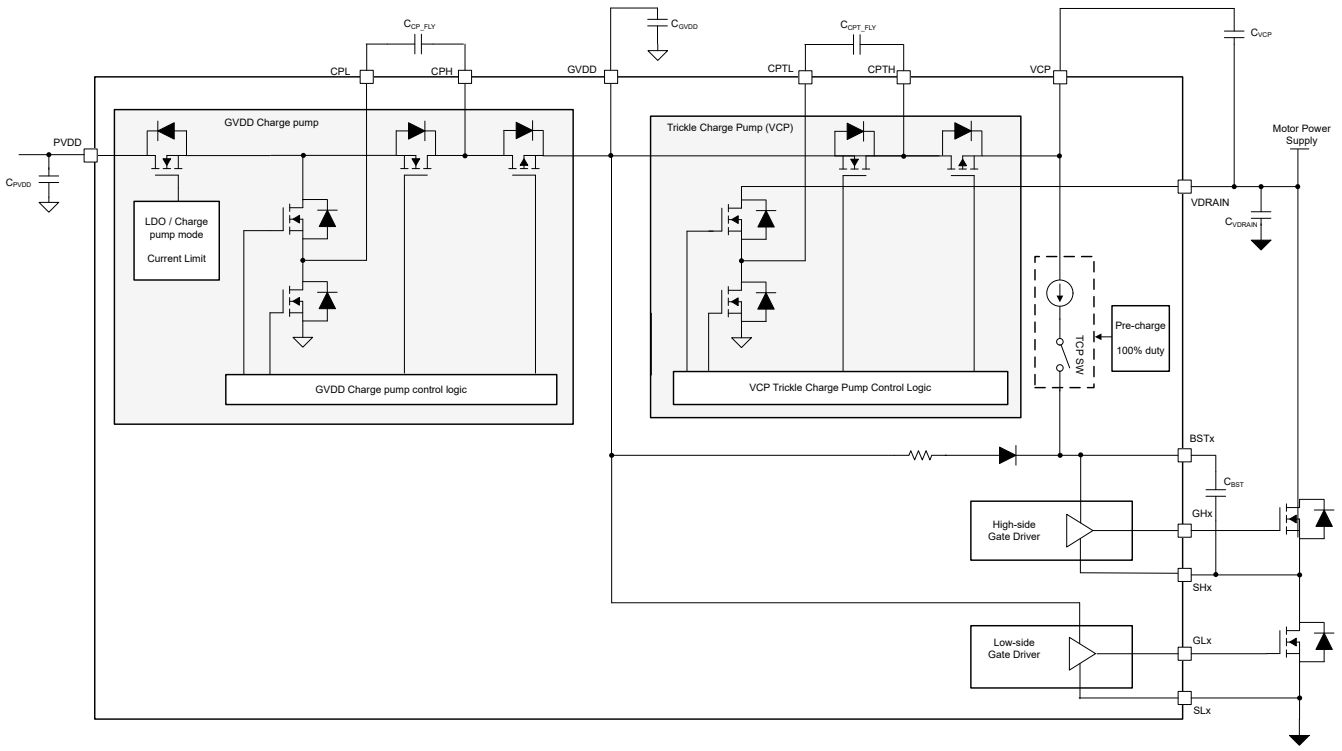

Figure 6-4. DRV8334 Gate Driver Power Supply Architecture

6.3.1.2.1 Bootstrap diode

The bootstrap diode is necessary to generate the high-side bias and is integrated inside the driver. The diode anode is connected to GVDD through an internal resistor and the cathode is connected to BSTx. With the C_{BST} capacitor connected to the BSTx and the SHx pins, the C_{BST} capacitor charge is refreshed every switching cycle when SHx transitions to ground. The capacitor value C_{BST} is dependent on the gate charge of the high-side MOSFET and must be selected considering PWM control and voltage drop of the MOSFET gate. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

6.3.1.2.2 GVDD Charge pump/LDO

The GVDD charge pump/LDO provides a regulated voltage of approximately 12V on the GVDD pin. GVDD is a power supply source of the bootstrap diode and also the VCP trickle charge pump.

Note

Setting DIS_GVDD_SS to 1b is recommended after power up. In case DIS_GVDD_SS remains 0b, the GVDD output load capability may not meet the test limits of electrical characteristic table when PVDD input voltage is lower than 7.2V.

6.3.1.2.3 VCP Trickle Charge pump

The device has a trickle charge pump that provides current to the C_{BST} bootstrap capacitors so that the bootstrap capacitor stays charged. This allows the gate driver to operate at 100% duty cycle. The charge pump also supports pre-charge of the C_{BST} capacitors at power up.

By default, the device monitors INLx pins and charging the bootstrap capacitor by VCP is enabled while INLx are inactive (=low). If TCP_SW_MODE register bit is 1b, charging bootstrap capacitor is enabled regardless of INLx pins.

In addition to the support of 100% PWM duty cycle operation, the VCP charge pump is designed to support an overdrive supply for external components. The supply voltage V_{VCP} is available on VCP pin and the voltage is

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regulated with respect to VDRAIN, where a capacitor is connected between VCP and VDRAIN pins. The VCP voltage may be used for an overdrive supply of external switch control circuits such as battery reverse protection switch, high-side switch, or motor phase isolation switches. While the VCP charge pump is designed to support these external loads, care must be taken to avoid exceeding the total current limit of the overdrive supply.

Note

At the device power up, a VCP under voltage flag VCP_UV is reported and remains latched. The VCP_UV status flag can be cleared through a SPI write command CLR_FLT by MCU.

6.3.1.2.4 Gate Driver Output

The gate drivers use a Smart Gate Drive architecture to provide switching control of the external power MOSFETs, additional steps to protect the MOSFETs, and optimize tradeoffs between efficiency and robustness. This architecture is implemented through two components called IDRIVE and TDRIVE. The IDRIVE gate drive current and TDRIVE gate drive time are initially selected based on the parameters of the external power MOSFET used in the system and the desired rise and fall times.

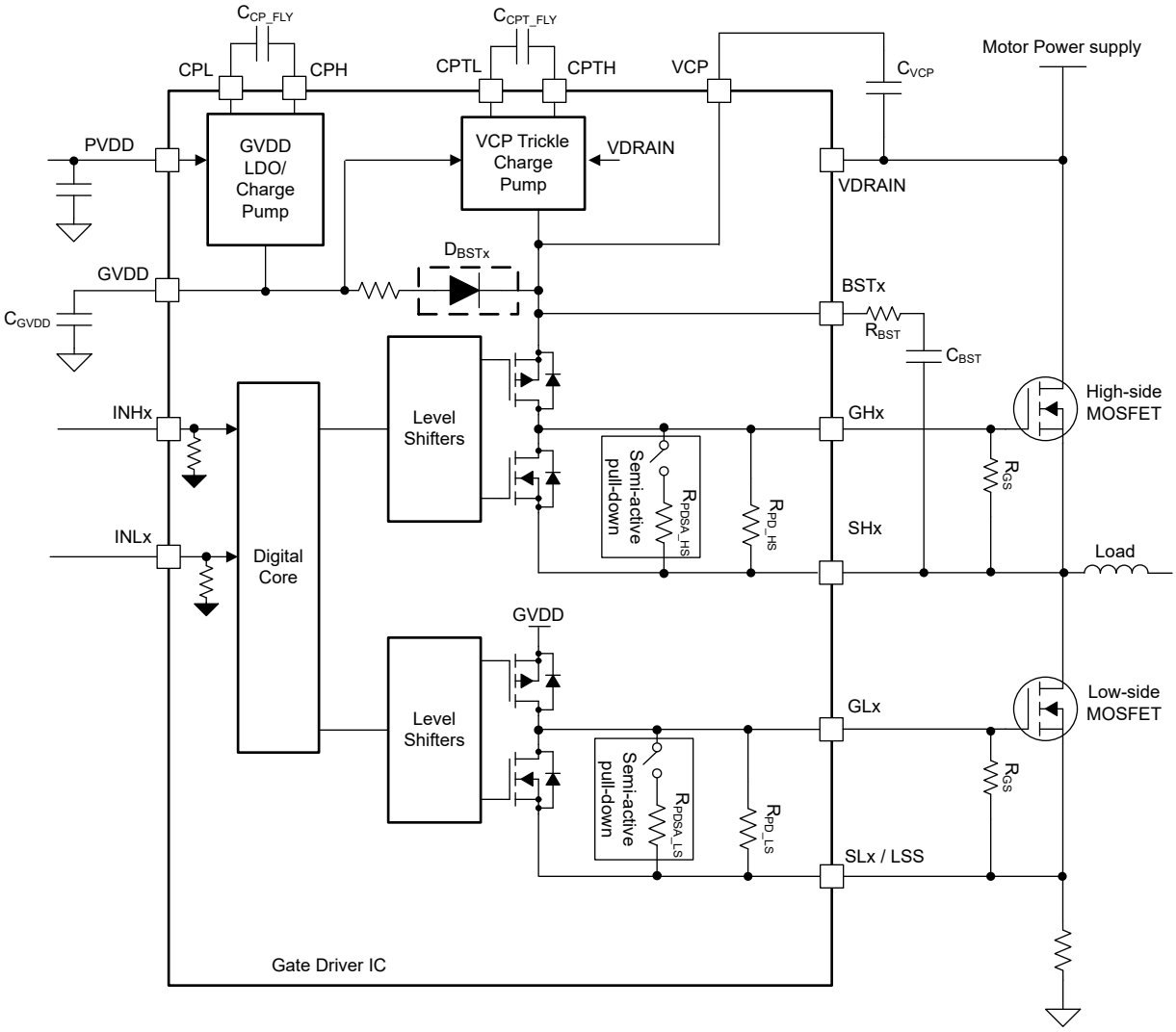

Figure 6-5. Gate Driver Architecture

6.3.1.2.5 Passive and Semi-active pull-down resistor

Each gate driver has a passive pull down between the gate and source to keep the external MOSFETs turned off in unpowered conditions. In addition a semi-active pull down circuit of low-side gate driver reduces the gate impedance during SLEEP mode.

6.3.1.2.6 TDRIVE Gate Drive Timing Control

The device integrates TDRIVE gate drive timing control to prevent parasitic dV/dt gate turn on of external MOSFETs. Strong pull-down I_{STRONG} current is enabled on the opposite MOSFET gate whenever a MOSFET is switching. The strong pulldown lasts for the TDRIVE duration. This feature helps to remove parasitic charge that couples into the MOSFET gate when the half-bridge switch-node voltage slews rapidly.

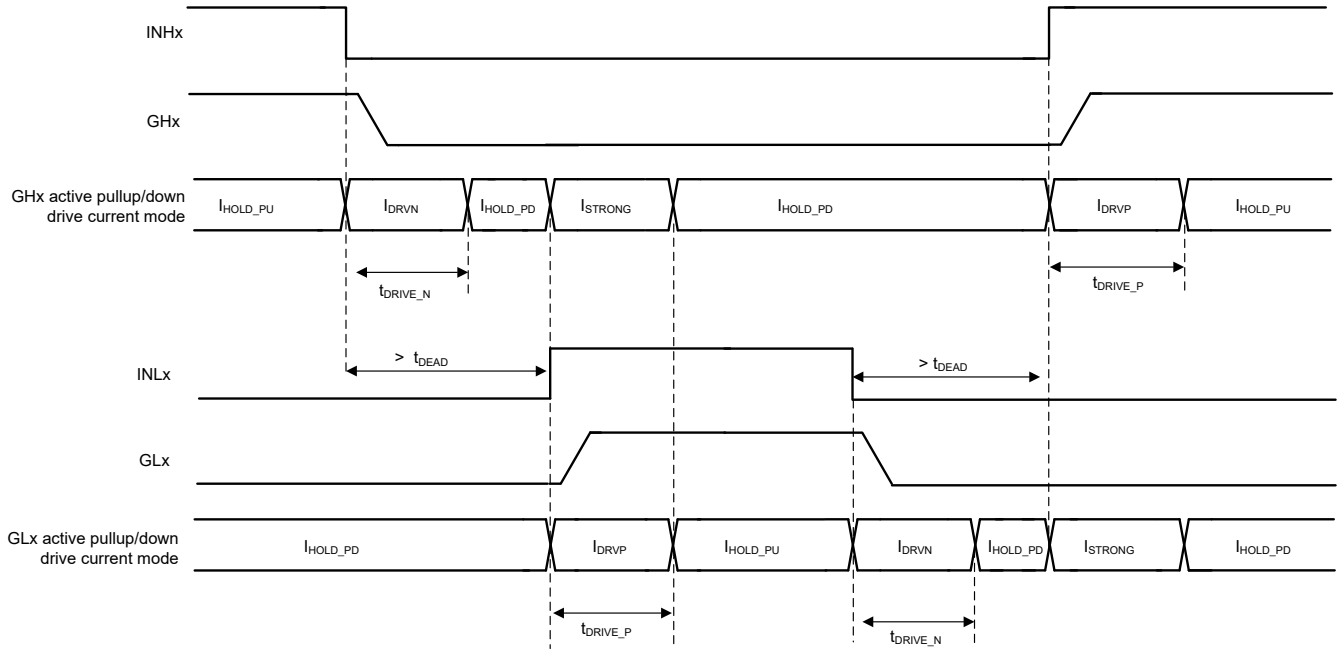

Figure 6-6. TDRIVE Gate Drive Timing Control (DEADT_MODE = 0b)

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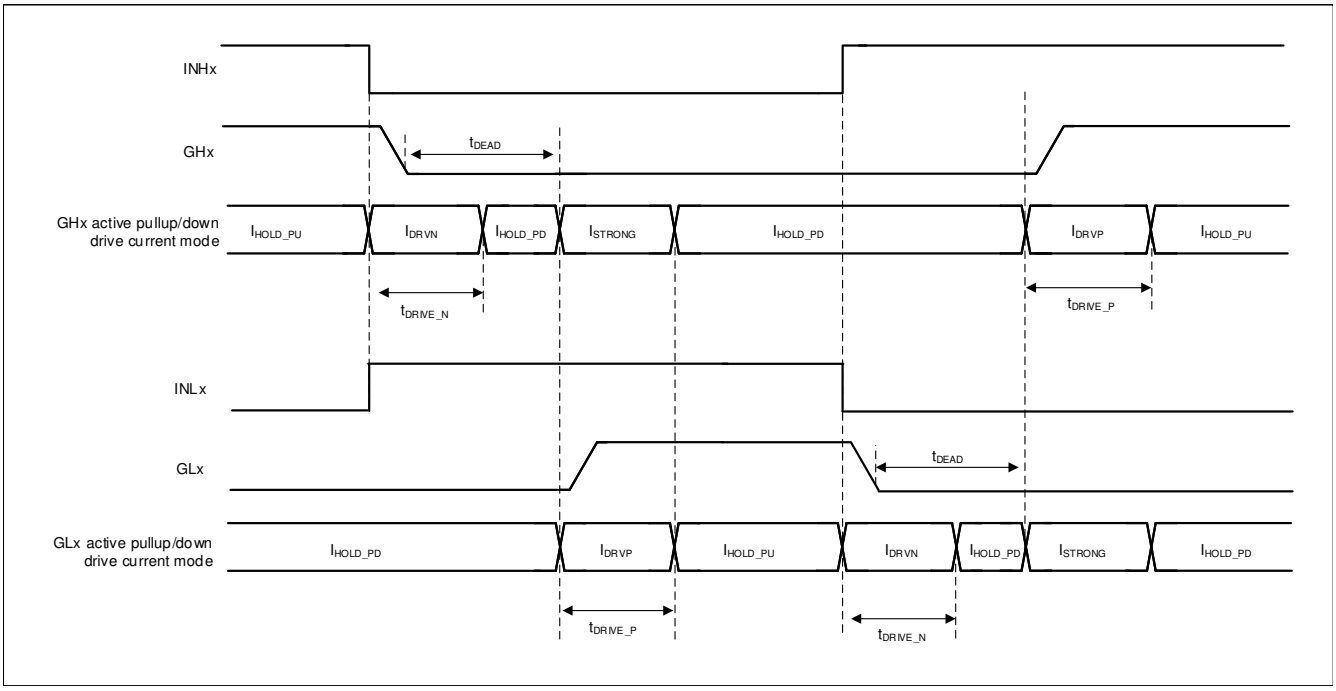

Figure 6-7. TDRIVE Gate Drive Timing Control (DEADT_MODE = 1b)

6.3.1.2.7 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to a detected output change. This time has two parts consisting of the digital propagation delay, and the delay through the analog gate drivers.

To support multiple control modes and dead time insertion, a small digital delay is added as the input command propagates through the device. Lastly, the analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

6.3.1.2.8 Deadtime and Cross-Conduction Prevention

In 6xPWM mode of DRV8334, high-side INHx and low-side INLx inputs operate independently, with an exception to prevent cross conduction when the high and low side of the same half-bridge are turned ON at same time. The device pulls high- and low- side gate outputs low to prevent shoot through condition of power stage and a fault STP_FLT is reported when high- and low-side inputs are logic high at the same time.

In 6xPWM mode, if SPI register bit DEADT_MODE is 0b and DEADT_MODE_6X is 00b, the device monitors INHx and INLx and inserts dead time if the period of INHx=INLx=low is shorter than t_{DEAD}. Other than 6xPWM mode, dead time is always inserted regardless of the configuration.

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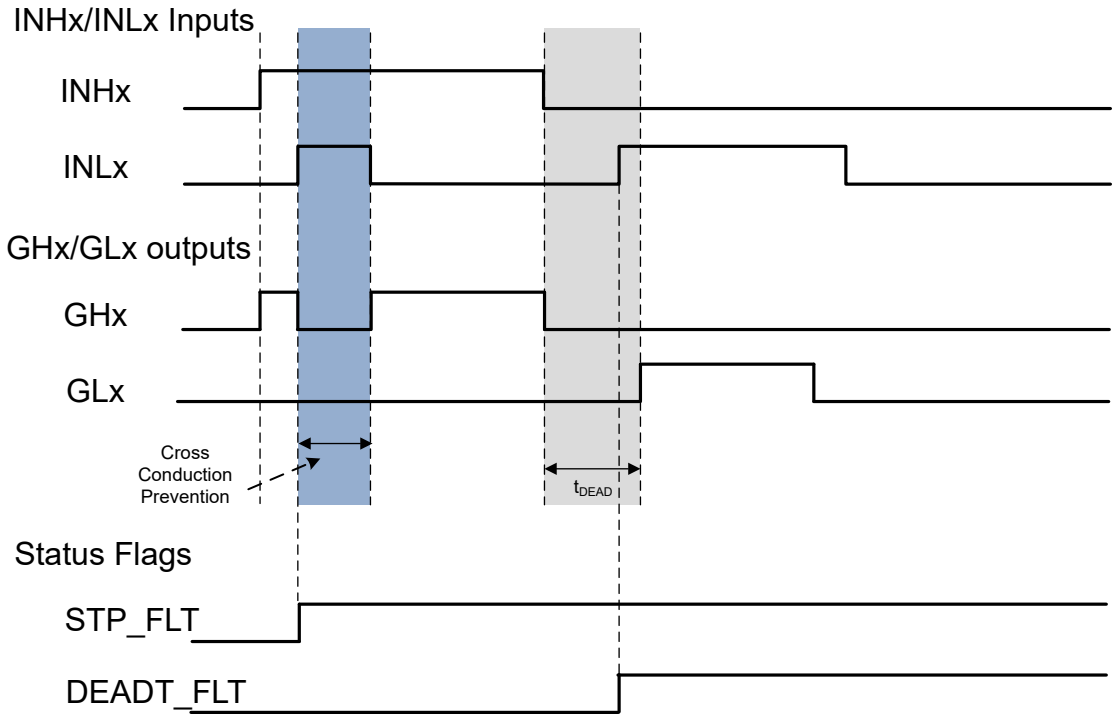

Figure 6-8. Cross Conduction Prevention and Dead time Insertion

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6.3.2 Low-Side Current Sense Amplifiers

The DRV8334 devices integrate high-performance low-side current sense amplifier for current measurements using low-side shunt resistors. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless DC commutation with the external controller. The current sense amplifiers feature nine configurable gain settings between 5 and 40V/V, which can be configured through SPI commands. The CSA output is referenced to the external voltage reference pin (VREF). The CSA output offset can be configured between 1/2 xVREF or 1/8 xVREF to support bidirectional or unidirectional current sensing as needed.

Note

By default, CSA output is disabled. CSA output can be enabled in SPI register IC_CTRL2. After CSA is enabled, the external MCU must wait 100us before sampling CSA output signals.

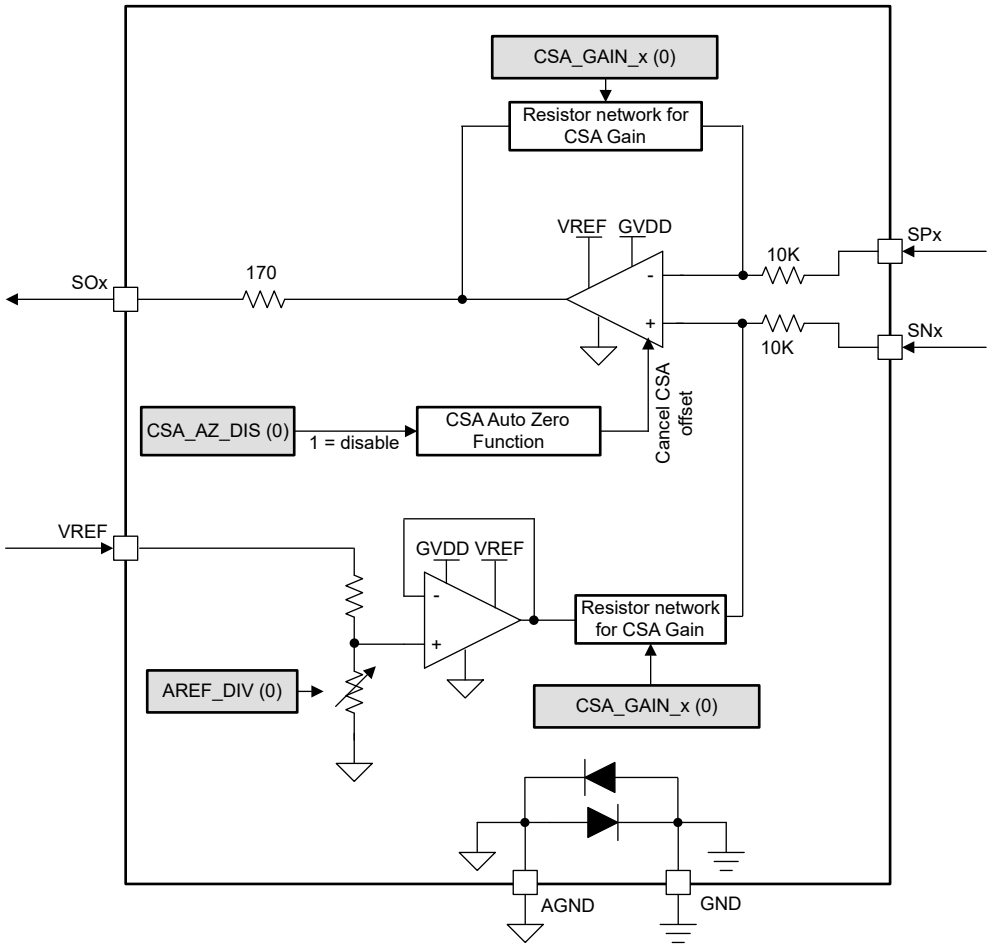

Figure 6-9. Current-Sense Amplifier Diagram

6.3.2.1 Unidirectional Current Sense Operation

The DRV8334 internally generates a common mode voltage of 1/8 x VREF to obtain maximum resolution for current measurement. The current sense amplifier operates in a unidirectional mode and the SO pin outputs an analog voltage equal to the voltage across the SP and SN pins multiplied by the gain setting (G_{CSA}).

Use Equation 1 to calculate the current through the shunt resistor.

$$I = \frac{V_{SOx} - V_{VREF}/8}{G_{CSA} \times R_{SENSE}} \quad (1)$$

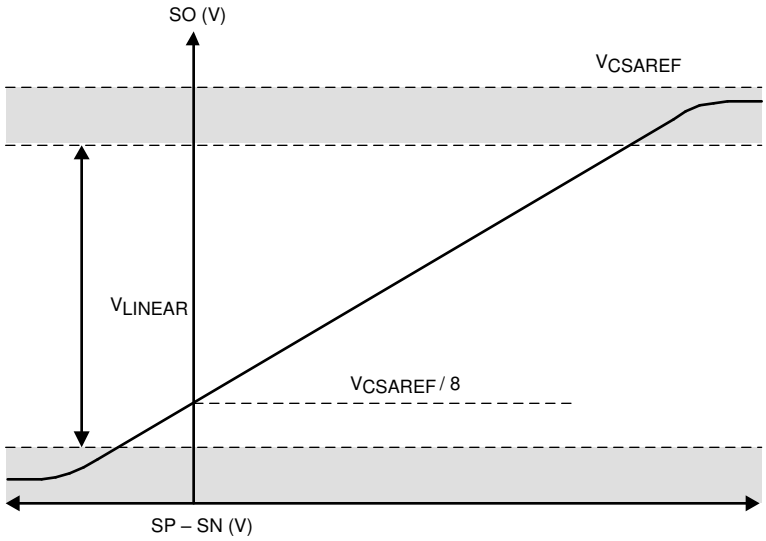

Figure 6-10. Unidirectional Current-Sense Output

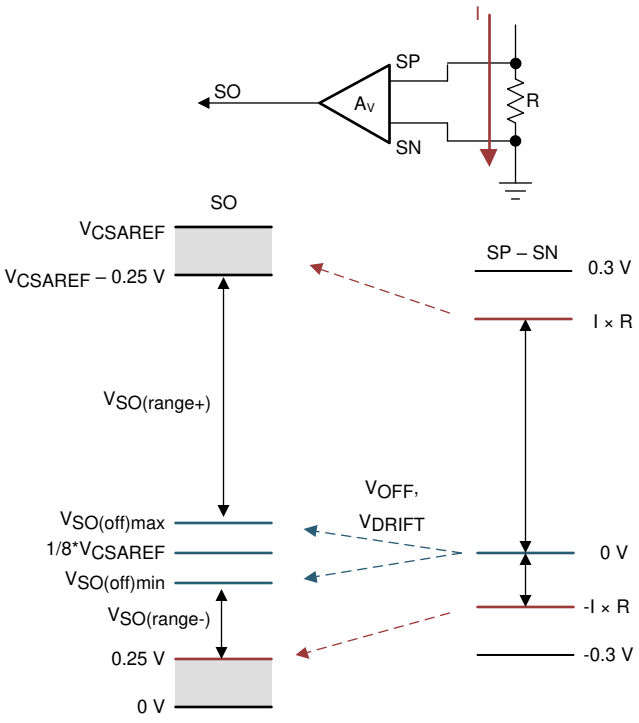

Figure 6-11. Unidirectional Current-Sense Regions

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6.3.2.2 Bidirectional Current Sense Operation

In this mode, DRV8334 internally generates a common mode voltage of ½ x VREF to enable bidirectional current measurement. The current sense amplifier operates in a bidirectional mode and the SO pin outputs an analog voltage equal to the voltage across the SP and SN pins multiplied by the gain setting (G_{CSA}).

Use Equation 2 to calculate the current through the shunt resistor (AREF_DIV = VREF / 2 case) .

$$I = \frac{V_{SOx} - \frac{V_{VREF}}{2}}{G_{CSA} \times R_{SENSE}} \quad (2)$$

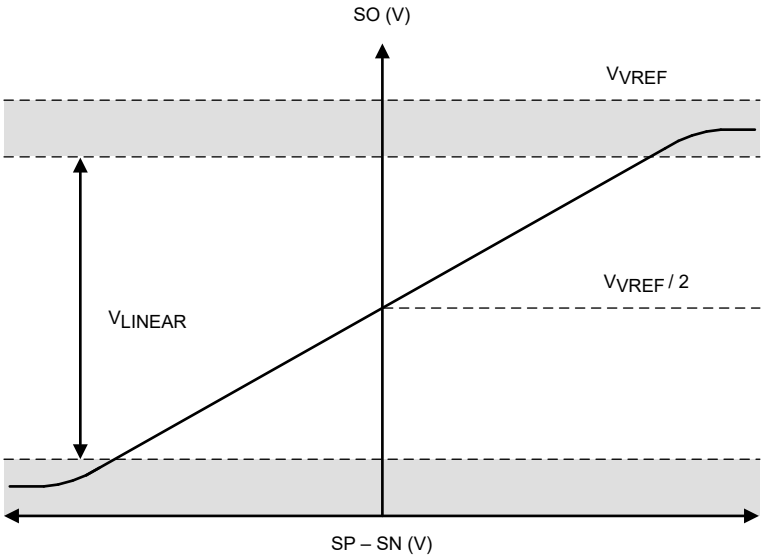

Figure 6-12. Bidirectional Current Sense Output

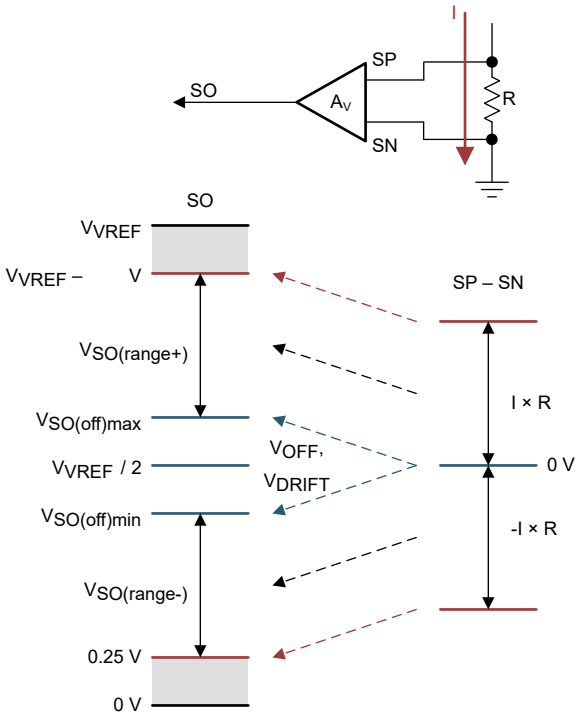

Figure 6-13. Bidirectional Current Sense Regions

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6.3.3 Gate Driver Shutdown

If a fault condition is detected or DRVOFF pin is driven by system, the device takes an action of gate driver shutdown. The high-side and low-side gate driver outputs are pulled down to turn off external MOSFETs.

6.3.3.1 DRVOFF Gate Driver Shutdown

When DRVOFF is driven high, the gate driver goes into shutdown mode, overriding signals on inputs pins INHx and INLx. DRVOFF bypasses the internal digital logic and is connected directly to the predriver. This pin provides a mechanism for externally monitored faults to disable the gate driver directly bypassing the external controller. When the DRVOFF pin is driven high, the device disables the gate driver and triggers the shutdown sequence.

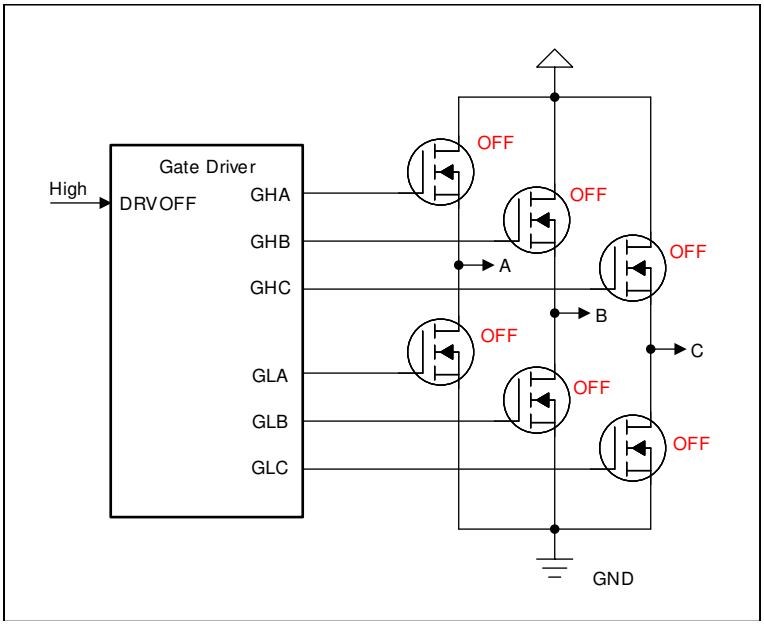

Figure 6-14. DRVOFF Gate Driver Output State

6.3.3.2 Gate Driver Shutdown Timing Sequence

The device initiates gate driver shutdown sequence as shown in figure. The shutdown drive current can be programmed with SPI register IDRVN_SD. The gate driver uses I_{DRVN_SDD} for t_{DRVN_SDD} time to discharge gate of MOSFET. The shutdown current changes to I_{DRVN_SD} current and is hold until end of t_{DRVN_SD} time. After completion of shutdown sequence, gate driver outputs are in semi-active pull-down mode.

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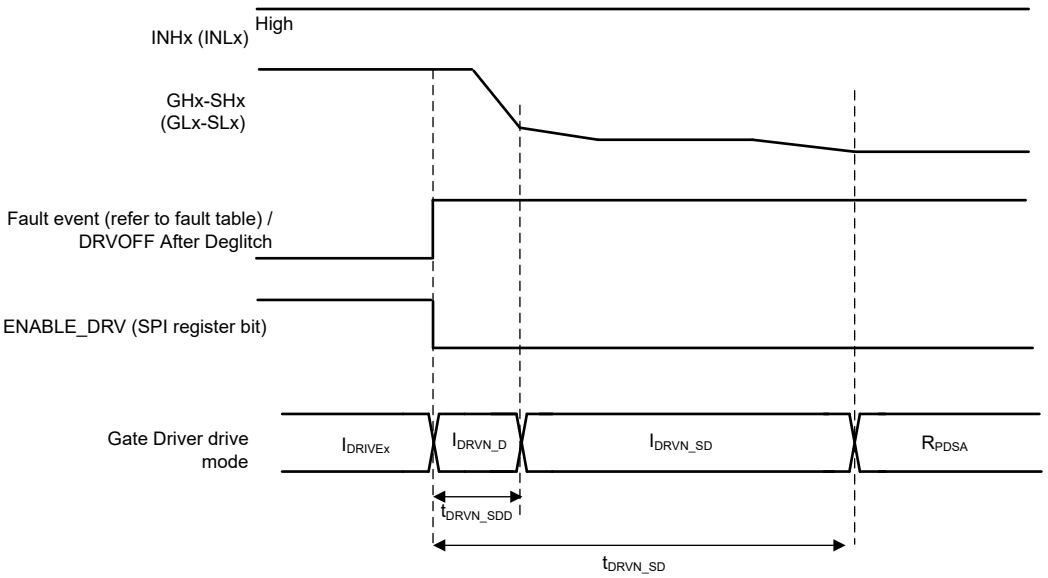

Figure 6-15. Gate Drive Shutdown Sequence

6.3.4 Gate Driver Protective Circuits

6.3.4.1 PVDD Supply Undervoltage Warning (PVDD_UVW)

If at any time the power supply voltage on the PVDD pin falls below the V_{PVDD_UVW} threshold for longer than the $t_{PVDD_UVW_DG}$ time, the DRV8334 detects a PVDD undervoltage warning event. After detecting the undervoltage condition, the device asserts a warning in accordance with the WARN_MODE bit. The V_{PVDD_UVW} threshold is adjustable through the SPI register bit PVDD_UVW_LVL.

6.3.4.2 PVDD Supply Undervoltage Lockout (PVDD_UV)

If at any time the power supply voltage on the PVDD pin falls below the V_{PVDD_UV} threshold for longer than the $t_{PVDD_UV_DG}$ time, the DRV8334 detects a PVDD undervoltage event. After detecting the undervoltage condition, the gate driver disabled, charge pump disabled and nFAULT pin is driven low. After PVDD_UV condition is cleared, the fault state remains latched and can be cleared through an SPI command.

6.3.4.3 PVDD Supply Overvoltage Fault (PVDD_OV)

If at any time the power supply voltage on the PVDD pin exceeds the V_{PVDD_OV} threshold for longer than the $t_{PVDD_OV_DG}$ time, the DRV8334 detects a PVDD overvoltage event. After detecting the overvoltage condition, the gate driver is disabled, charge pump is disabled, and nFAULT pin is driven low. After PVDD_OV condition is cleared, the fault state remains latched and can be cleared through an SPI command. The PVDD_OV threshold is adjustable through the SPI register field PVDD_OV_LVL. The PVDD OV threshold is adjustable through the SPI register field PVDD_OV_LVL, with settings available for 28V, 33V, or 50V.

6.3.4.4 GVDD Undervoltage Lockout (GVDD_UV)

If at any time the voltage on the GVDD pin falls lower than the V_{GVDD_UV} threshold voltage for longer than the $t_{GVDD_UV_DG}$ time, the device detects a GVDD undervoltage event. After detecting the GVDD_UV undervoltage event, the gate driver is disabled, VCP charge pump is disabled and nFAULT pin is driven low if the GVDD_UV_MODE bit is 1b. After GVDD_UV condition is cleared, the fault state remains latched and can be cleared through an SPI command.

6.3.4.5 GVDD Overvoltage Fault (GVDD_OV)

If at any time the power supply voltage on the GVDD pin exceeds the V_{GVDD_OV} threshold for longer than the $t_{GVDD_OV_DG}$ time, the DRV8334 detects a GVDD overvoltage event. After detecting the overvoltage condition, the gate driver is disabled, charge pump is disabled, and nFAULT pin is driven low. After PVDD_OV condition is cleared, the fault state remains latched and can be cleared through an SPI command.

6.3.4.6 BST Undervoltage Lockout (BST_UV)

If at any time the voltage across BTSx and SHx pins falls lower than the V_{BST_UV} threshold voltage for longer than the $t_{BST_UV_DG}$ time, the device detects a BST undervoltage event. After detecting the BST_UV undervoltage event, the high-side gate driver is disabled and nFAULT pin is driven low if the BST_UV_MODE register bit is 1b. The low-side gate driver remains active during BST_UV event. After the BST_UV condition is cleared, the fault state remains latched if BST_UV_LATCH register bit is 1b, and the flag can be cleared through an SPI command.

6.3.4.7 BST Overvoltage Fault (BST_OV)

If at any time the power supply voltage on one of the BSTx pins exceeds the V_{BST_OV} threshold for longer than the $t_{BST_OV_DG}$ time, the DRV8334 detects a BST overvoltage event. After detecting the overvoltage condition, the gate driver is disabled, charge pump is disabled, and nFAULT pin is driven low. After BST_OV condition is cleared, the fault state remains latched and can be cleared through an SPI command.

6.3.4.8 VCP Undervoltage Fault (CP_OV)

If at any time the voltage between the VCP and VDRAIN pins falls below the V_{CP_UV} threshold for longer than the $t_{CP_UV_DG}$ time, the DRV8334 detects a VCP undervoltage event. After detecting the undervoltage condition, the gate driver is disabled, charge pump is disabled, and nFAULT pin is driven low. After the VCP_UV condition is cleared, the fault state remains latched and can be cleared through an SPI command.

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6.3.4.9 VCP Overvoltage Fault (CP_OV)

If at any time the between the VCP and VDRAIN pins exceeds the V_{CP_OV} threshold for longer than the $t_{CP_OV_DG}$ time, the DRV8334 detects a VCP overvoltage event. After detecting the overvoltage condition, the gate driver is disabled, charge pump is disabled, and nFAULT pin is driven low. After VCP_OV condition is cleared, the fault state remains latched and can be cleared through an SPI command.

6.3.4.10 VDRAIN Undervoltage Fault (VDRAIN_UV)

If at any time the supply voltage on the VDRAIN pins falls below the V_{DRAIN_UV} threshold for longer than the $t_{vdrain_uv_dg}$ time, the DRV8334 detects a VDRAIN undervoltage event. After detecting the undervoltage condition, the gate driver is disabled, charge pump is disabled, and nFAULT pin is driven low. After the VDARIN_UV condition is cleared, the fault state remains latched and can be cleared through an SPI command.

6.3.4.11 VDRAIN Overvoltage Fault (VDRAIN_OV)

If at any time the power supply voltage on the VDRAIN pin exceeds the V_{DRFAIN_OV} threshold for longer than the $t_{VDRAIN_OV_DG}$ time, the DRV8334 detects a VDRAIN overvoltage event. After detecting the overvoltage condition, the gate driver is disabled, charge pump is disabled, and nFAULT pin is driven low. After the VDRAIN_OV condition is cleared, the fault state remains latched and can be cleared through an SPI command. The VDRAIN_OV threshold can be adjusted based on expected supply range using the VDRAIN_OV_LVL register field.

6.3.4.12 MOSFET VGS Monitoring Protection

The DRV8334 utilizes integrated gate to source voltage (VGS) monitors to monitor the state of the external MOSFETs. When the output state of the MOSFETs is commanded OFF (INxx = low), the monitor provides that the output stays turned off. If at any point the VGS voltage exceeds the VGS threshold for a duration longer than tvgs_dg, the nFAULT pin is driven low and the VGS_XX flag is set for the corresponding output channel. When the output state of the MOSFETs is commanded ON (INxx = high), the monitor verifies that the output turns on and the MOSFETs are driven with sufficient VGS to be strongly enhanced. If at any point the VGS drops below the VGS threshold for a duration longer than tvgs_dg, the nFAULT pin is driven low and the VGS_XX flag is set for the corresponding output channel. The VGS monitor blanking time can be adjusted through the VGS_BLK register field. TI recommends to set this value based on the expected switching time for the external MOSFETs. The VGS monitor deglitch time can be adjusted through the VGS_DEG register field. The deglitch timer does not start until after the VGS blanking time has elapsed following a rising/falling PWM signal. TI recommends to set this value based on the system noise level and acceptable fault tolerance timing.

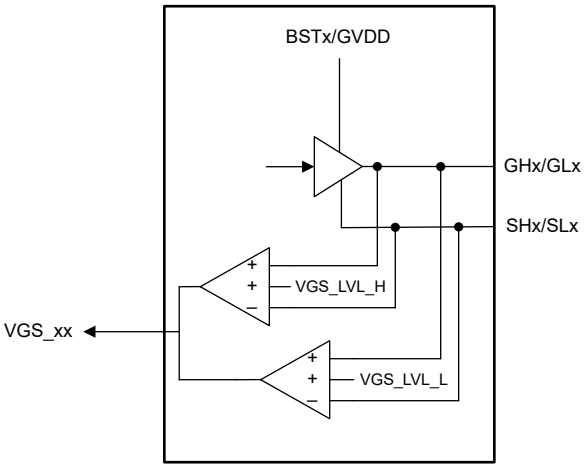

Figure 6-16. DRV8334 V_{GS} Monitors

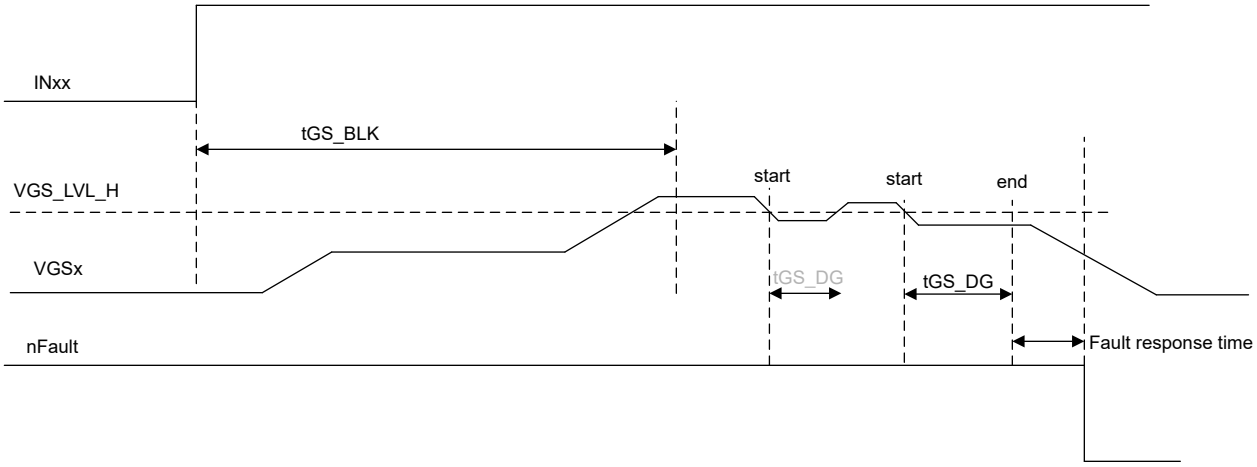

Figure 6-17. DRV8334 V_{GS} Monitor Timing (Output High)

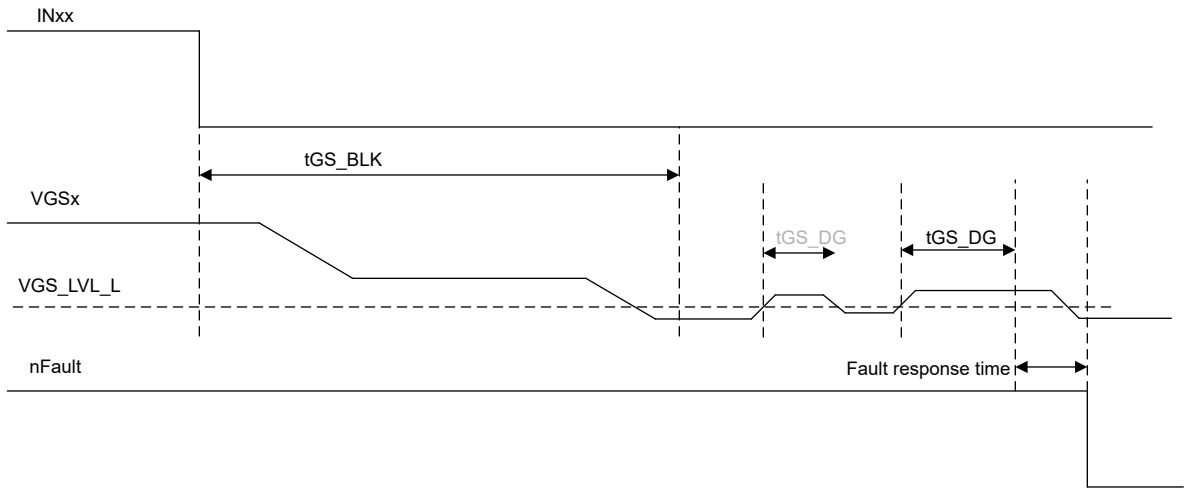

Figure 6-18. DRV8334 V_{GS} Monitor Timing (Output Low)

6.3.4.13 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

The device has adjustable V_{DS} voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. A MOSFET overcurrent event is sensed by monitoring the V_{DS} voltage drop across the external MOSFET $R_{DS(on)}$. The high-side VDS monitors measure between the VDRAIN and SHx pins and the low-side VDS monitors measure between the SHx and SLx pins. If the voltage across external MOSFET exceeds the V_{DS_LVL} threshold for longer than the t_{DS_DG} deglitch time, a VDS_OCP event is recognized. After detecting the VDS overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low. VDS level and deglitch time are programmable.

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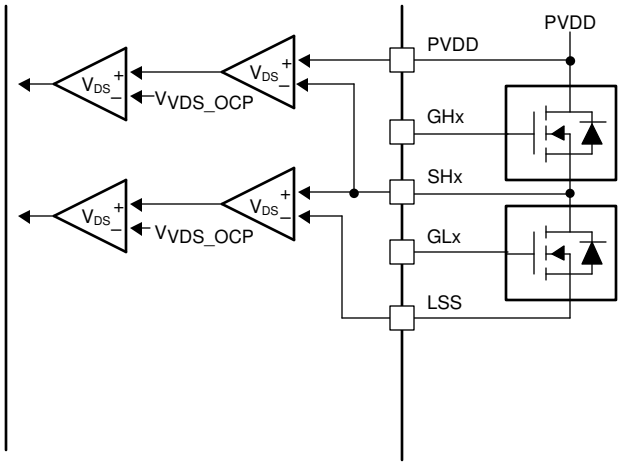

Figure 6-19. DRV8334 V_{DS} Monitors

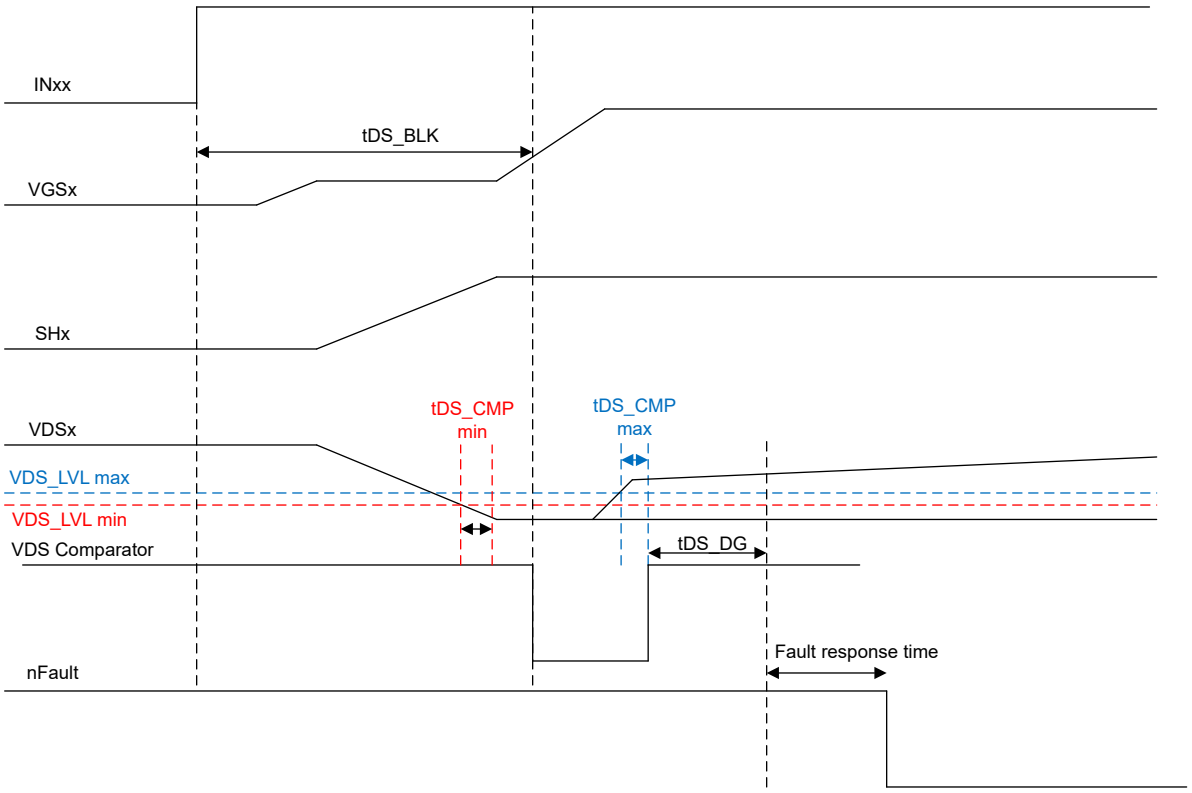

Figure 6-20. DRV8334 V_{DS} Monitor Timing

6.3.4.14 V_{SENSE} Overcurrent Protection (SEN_OCP)

Overcurrent is also monitored by sensing the voltage drop across the external current sense resistor between SPx and SNx pin. If at any time the difference voltage of SPx-SNx exceeds the V_{SEN_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a SEN_OCP event is recognized. After detecting the SEN_OCP over current event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low. The V_{SENSE} threshold and deglitch time are programmable. After SEN_OCP condition is cleared, the fault state remains latched and can be cleared through SPI command.

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6.3.4.15 Phase Comparators

The device has three integrated phase comparators, each of which monitors the voltage at the SHx pin against the voltage on the VDRAIN pin. The phase comparators can be used to monitor the voltage of the SHx pin for motor commutation control, measurement of the time from input to output, or for diagnostics of the drivers, external MOSFETs, and external load.

The phase comparator thresholds are created with a resistor divider between the VDRAIN and GND pins. The threshold voltage is sent to the phase comparator and compared against the SHx voltage with respect to GND.

The device can be configured to enable three push-pull digital outputs on INLA, INLB and INLC pins. The outputs indicate the status of each phase comparator output. When INLx are used for phase comparator outputs, SPI register bit PWM_MODE must be configured to 010b (3xPWM mode with SPIN enable control) to control low-side gate drivers.

The device integrates a logic to compare the digital inputs INHx and the phase comparator outputs. If a mis-compare is detected, the fault is reported on SPI register bits PHCx_FLT.

6.3.4.16 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), OTSD event is recognized. After detecting the OTSD overtemperature event, if OTSD_MODE is Fault mode, all of the gate driver outputs are driven low to disable the external MOSFETs, charge pump and current sense are disabled, and nFAULT pin is driven low. After OTSD condition is cleared, the fault state remains latched and can be cleared through an SPI command (CLR_FLT). The OTSD_MODE is Fault mode by default. If OTSD condition is detected during device power up, nFAULT stays low and charge pump and current sense remain disabled until OTSD condition is removed and SPI command (CLR_FLT) is sent by MCU.

6.3.4.17 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OTW bit is set in the registers of SPI devices. The device performs no additional action and continues to function. After the die temperature falls lower than the hysteresis point of the thermal warning, the OTW bit remains latched and can be cleared through an SPI command CLR_FLT. If OTW bit is 1b, nFAULT remains high.

6.3.4.18 OTP CRC

After each power up, the device performs an OTP CRC check. If the calculated CRC8 checksum does not match the CRC8 checksum stored in the internal OTP memory, the OTP_CRC failed flag is set.

6.3.4.19 SPI Watchdog Timer

The device integrates a programmable window-type SPI watchdog timer to verify that the external controller is operating. The SPI watchdog timer can be enabled by writing a 1 to WDT_EN SPI register bit. The watchdog timer is disabled by default. When the watchdog timer is enabled, an internal timer starts to count up. A valid SPI access resets the timer. This valid SPI access must be issued between the lower window time and the upper window time. If a watchdog timer fault is detected, the WDT_FLT status bit is set to 1b and nFAULT pin is asserted low.

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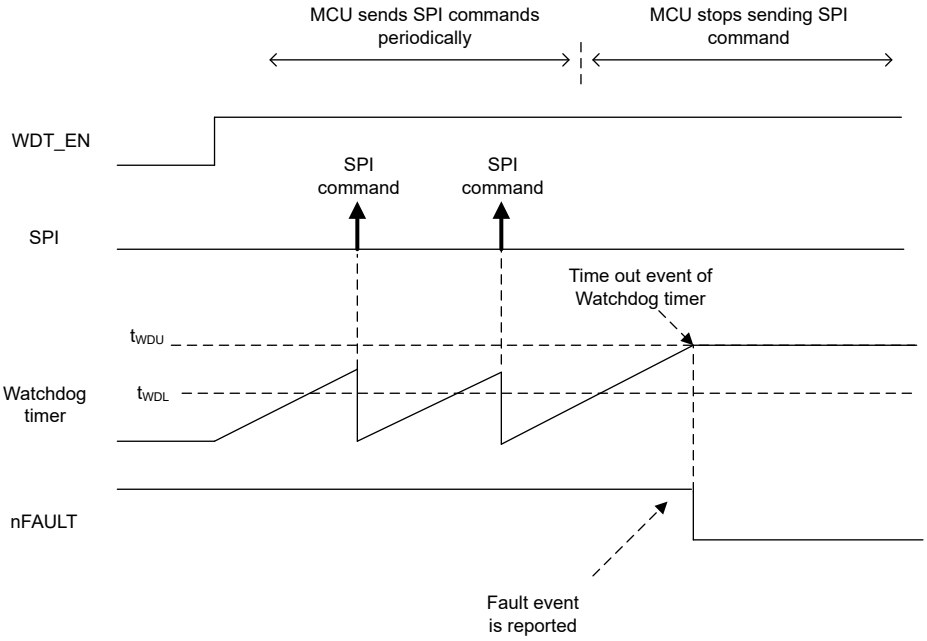

Figure 6-21. SPI Watchdog Timer timing diagram

6.3.4.20 Phase Diagnostic

The device integrates a current source and a switch between VDRAIN and SHx device pins and between SHx device pin and the device ground for each channel. The switches can be individually enabled and disabled via SPI register bits PHDEN_Hx and PHDEN_Lx. If PHDEN_Hx is 1b, the source current I_{PHD_SRC} of SHx pin is enabled. If PHDEN_Lx is 1b, the sink current I_{PHD_SNK} of SHx pin is enabled. When any of PHDEN_Hx and PHDEN_Lx register bits are set to 1, the VDS overcurrent detection flags, VDS_Hx and VDS_Lx, change from the fault detection flag to the status flag of VDS comparators. The combination of the integrated current sources and VDS status flags can be used for the phase diagnostics such as an open fault detection of motor load, without activating external MOSFETs.

By default, the gate drivers are disabled when PHDEN_x register bits are 1b. If PHDEN_DRV register bit is 1b, the gate driver outptus can be controlled by INHx and INLx input pins while PHDEN_x register bits are 1b, and the external MOSFETs can be turned ON during the phase diagnostic.

If PDHEN_x register bits are 1b, VCP charge pump stays enabled but the charging path from VCP to the bootstrap capacitor is disabled. After phase diagnostic, the bootstrap capacitor needs to be pre-charged before PWM operation.

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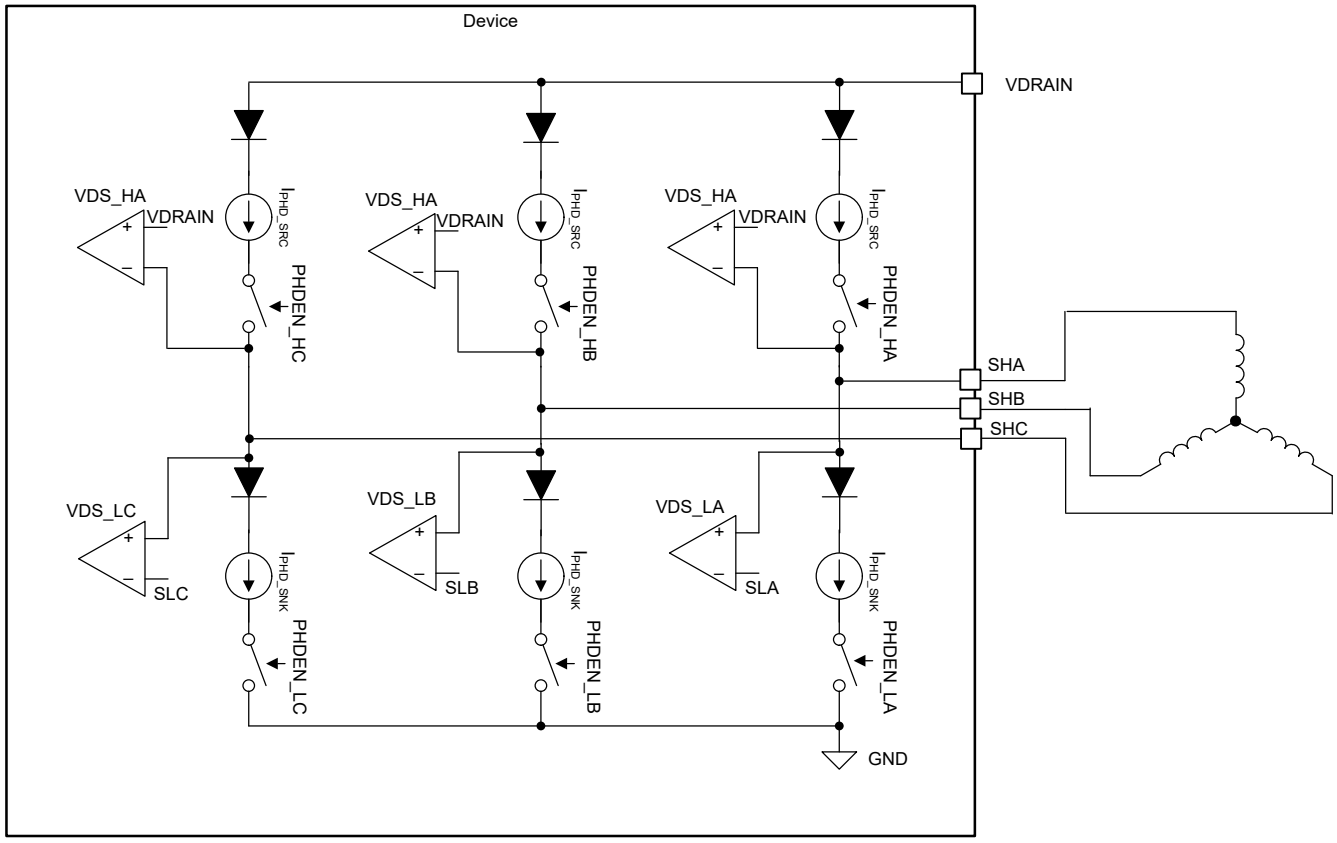

Figure 6-22. Phase Diagnostic (Preview only)

6.4 Device Functional Modes

6.4.1 Gate Driver Functional Modes

6.4.1.1 Sleep Mode

The nSLEEP pin manages the state of the DRV8334. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all gate drivers are disabled, sense amplifiers are disabled, all external MOSFETs are disabled, and the GVDD regulator is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

6.4.1.2 Operating Mode

When the nSLEEP pin is high and the V_{PVDD} voltage is greater than the V_{UVLO} voltage, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the GVDD regulator and AVDD regulator are active

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6.4.2 Device Power Up Sequence

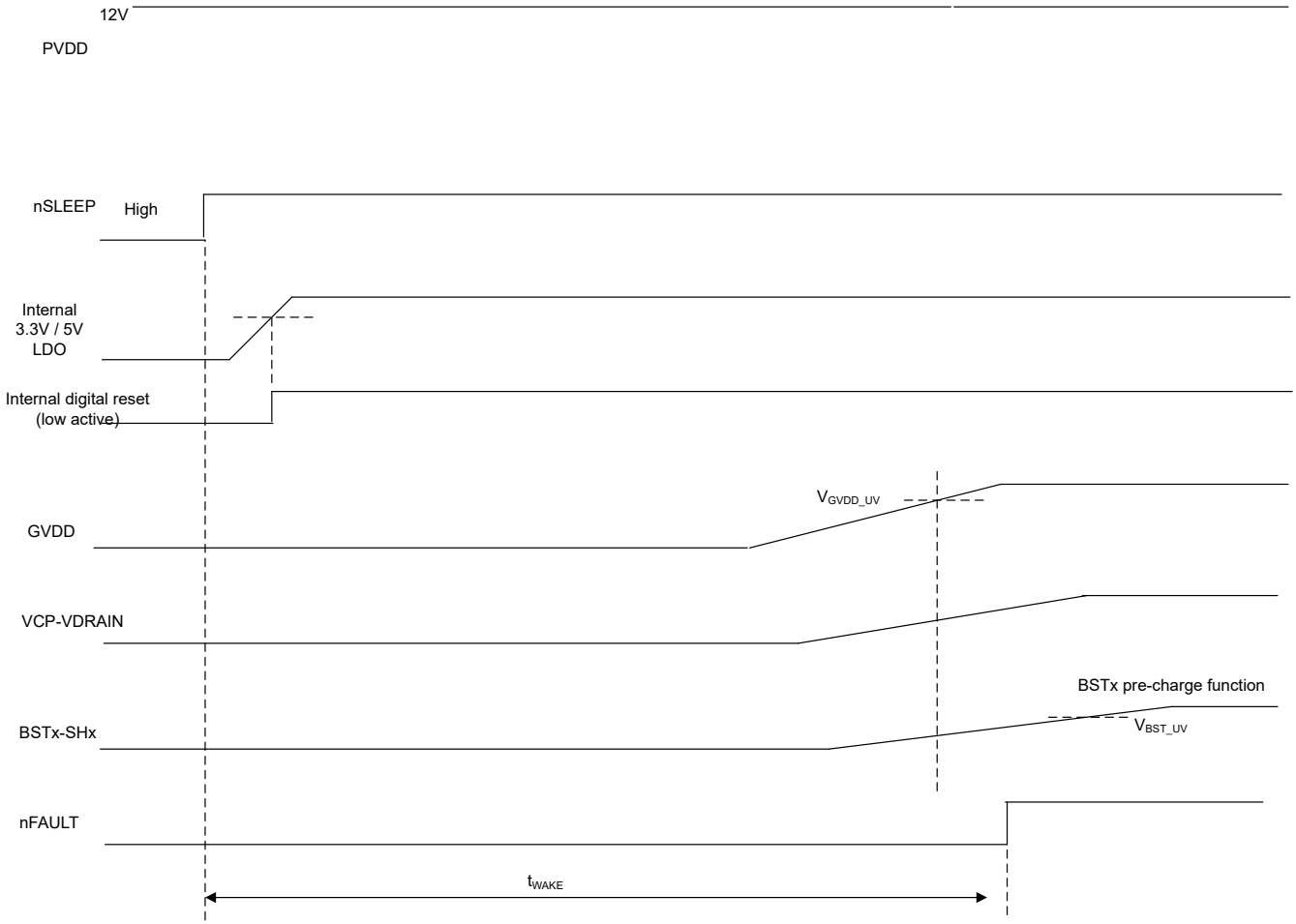

Figure 6-23. Device Power Up Sequence and t_{WAKE}

Figure 6-23 explains the device power up sequence including the device internal information. As described in Section 6.4, if the nSLEEP pin is driven high, the device starts the power up sequence to enable the internal LDOs, GVDD and VCP charge pump. The nFAULT output is low when the device completes the power up sequence and enters the Operating Mode. The external MCU may additonaly wait for the pre-charge of bootstrap capacitors before toggling the high-side gate drivers, and the SPI status flag BST_UVx can be used to check the status of pre-charge operation.

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6.5 Programming

6.5.1 SPI

The device uses a serial peripheral interface (SPI) bus to set device configurations, operating parameters, and read out diagnostic information. The device SPI operates in slave mode and connects to a master external controller. If SPI CRC (SPI_CRC_EN = 1b) is enabled, the SPI input data (SDI) word consists of a 32 bit word, with an 8 bit command, 16 bits of data, and 8 bit CRC (initial value 0xFF, polynomial 0x2F). The SPI output data (SDO) word consists of a 32 bit word, with an 8-bit status data, 16 bits of register data and 8bit CRC (initial value 0xFF, polynomial 0x2F). If SPI CRC is disabled (SPI_CRC_EN = 0b), the SPI data word consists of 24 bit word, where 8 bit CRC is excluded.

Note

CRC is enabled by default. To disable CRC, transmit "0x0009" to register 0x1C with CRC value "0x6E" (full SPI frame is "0x3800096E") after device power-up.

A valid frame must meet the following conditions:

- The SCLK pin is low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin is pulled high for at least 450ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is set Hi-Z.
- Data is captured on the falling edge of SCLK and data is propagated on the rising edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 32 (or 24) SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is not 32 (or 24) bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8 bit command data.
- The SDO pin is a push-pull type output.
- The SPI fault is confirmed at the rising edge of nSCS.

6.5.2 SPI Format

The SDI input data word is 32 (or 24) bits long and consists of the following format:

- 7 address bits, A6-A0
- 1 read or write bit, W0. W0 = 0b for write command and W0 = 1b for read command.
- 16 data bits, D15-D0
- 8-bit CRC if SPI_CRC_EN = 1b.

The SDO output data word is 32 (or 24) bits long and consists of the following format.

- 1 fault status bit, F. This bit is identical to IC_STAT1 FAULT register bit.
- 7 read back bits, A6-A0. This is the read back of incoming 7 address bits of SDI in the same SPI frame. The device captures SDI at the rising edge of SCLK and pushes it out on falling edge of SCLK.
- 16 data bits, D15-D0. This is read data of the addressed register. For write command, it is the data previously stored in the addressed register.
- 8-bit CRC if SPI_CRC_EN = 1b.

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6.5.3 SPI Format Diagrams

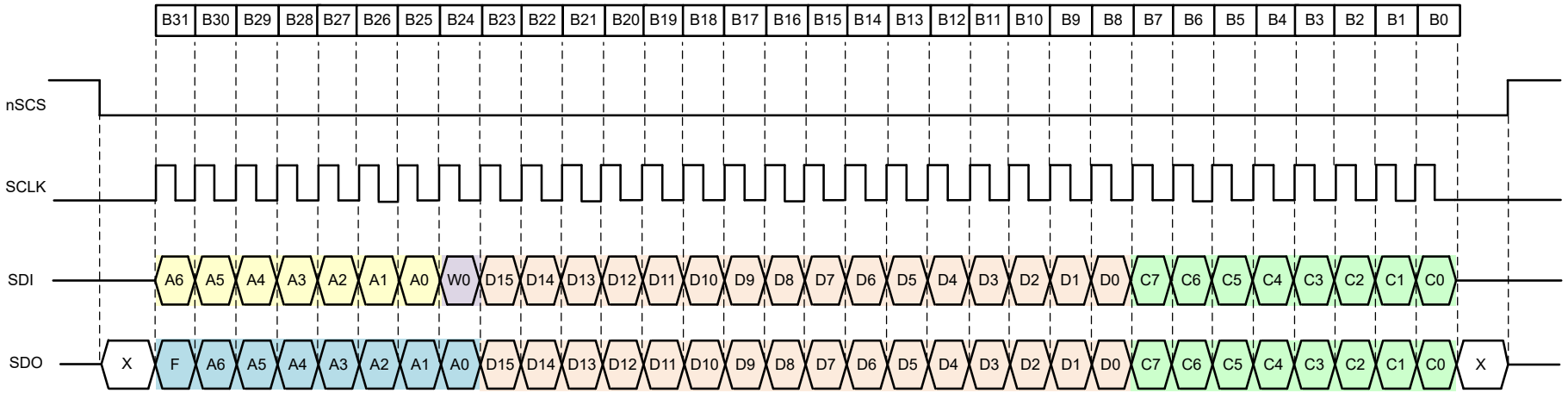

Figure 6-24. SPI Format - 32-bit frame (SPI_CRC_EN = 1b)

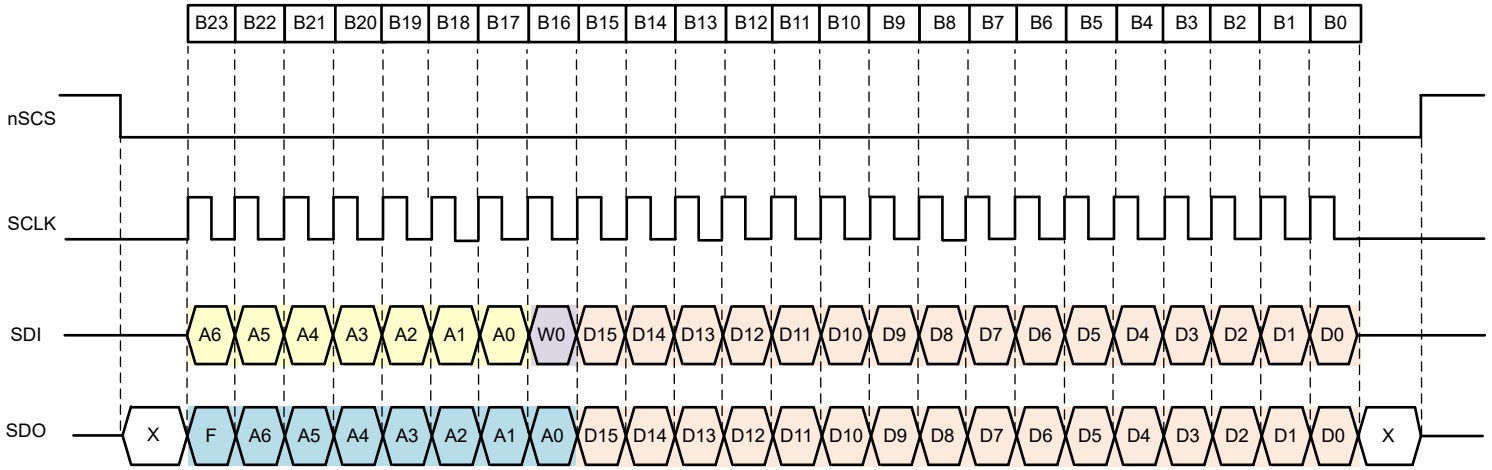

Figure 6-25. SPI Format - 24-bit frame (SPI_CRC_EN = 0b)

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7 Register Maps

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7.1 STATUS Registers

Table 7-1 lists the memory-mapped registers for the STATUS registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. STATUS Registers

Address	Acronym	Register Name	Section
0h	IC_STAT1	IC Status Register 1	Section 7.1.1
1h	IC_STAT2	IC Status Register 2	Section 7.1.2
2h	IC_STAT3	IC Status Register 3	Section 7.1.3
3h	IC_STAT4	IC Status Register 4	Section 7.1.4
4h	IC_STAT5	IC Status Register 5	Section 7.1.5
5h	IC_STAT6	IC Status Register 6	Section 7.1.6

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 IC_STAT1 Register (Address = 0h) [Reset = 8000h]

IC_STAT1 is shown in Table 7-3.

Return to the Summary Table.

Table 7-3. IC_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SPI_OK	R	1b	No SPI Fault is detected 0b = SPI Fault is detected 1b = No fault
14	FAULT	R	0b	Logic OR of FAULT status registers. Mirrors nFAULT pin. 0b = nFAULT status logic-low 1b = nFAULT status logic-high. One or multiple fault events detected.
13	WARN	R	0b	Logic OR of WARN status, except OTW 0b = No warning event detected 1b = One or multiple warning event detected
12	VDS	R	0b	Logic OR of VDS overcurrent detection 0b = No VDS events detected. 1b = One or multiple VDS events detected.
11	VGS	R	0b	Logic OR of VGS detection 0b = No VGS events detected. 1b = One or multiple VGS events detected.
10	SNS_OCP	R	0b	Logic OR of Sense overcurrent detection 0b = No sense overcurrent events detected. 1b = One or multiple sense overcurrent events detected.
9	OV	R	0b	Logic OR of supply voltage overvoltage detection 0b = No overvoltage events detected. 1b = One or more overvoltage events detected.

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Table 7-3. IC_STAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	UV	R	0b	Logic OR of supply voltage undervoltage detection 0b = No undervoltage events detected. 1b = One or more undervoltage events detected.
7-2	RESERVED	R	0b	Reserved
1	OTW	R	0b	Overtemperature Warning Status Bit 0b = No event is detected 1b = Overtemperature warning event detected
0	DRV_STAT	R	0b	Indicates Driver Enable Status. Mirrors ENABLE_DRV register bit

7.1.2 IC_STAT2 Register (Address = 1h) [Reset = 0000h]

IC_STAT2 is shown in Table 7-4.

Return to the Summary Table.

Table 7-4. IC_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CBC_ST	R	0b	VDS and SNS_OCP monitor Cycle By Cycle (CBC) counter activity status. If CBC is enabled (CBC is 1b), CBC counter is incremented when VDS or SNS_OCP condition is detected. CBC_ST is 1 if CBC counter is not 0 (CBC counter > 0) to indicate one or multiple VDS or SNS_OCP conditions have been detected. 0b = CBC counter is 0 1b = CBC counter is not 0 if CBC is enabled.
14-11	RESERVED	R	0b	Reserved
10	SNS_OCP_A	R	0b	Overcurrent on External Sense Resistor Status Bit on phase A
9	SNS_OCP_B	R	0b	Overcurrent on External Sense Resistor Status Bit on phase B
8	SNS_OCP_C	R	0b	Overcurrent on External Sense Resistor Status Bit on phase C
7-6	RESERVED	R	0b	Reserved
5	VDS_HA	R	0b	VDS Overcurrent Status on the A High-side MOSFET
4	VDS_LA	R	0b	VDS Overcurrent Status on the A Low-side MOSFET
3	VDS_HB	R	0b	VDS Overcurrent Status on the B High-side MOSFET
2	VDS_LB	R	0b	VDS Overcurrent Status on the B Low-side MOSFET
1	VDS_HC	R	0b	VDS Overcurrent Status on the C High-side MOSFET
0	VDS_LC	R	0b	VDS Overcurrent Status on the C Low-side MOSFET

7.1.3 IC_STAT3 Register (Address = 2h) [Reset = 0000h]

IC_STAT3 is shown in Table 7-5.

Return to the Summary Table.

Table 7-5. IC_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0b	Reserved
5	VGS_HA	R	0b	Gate driver fault status on the A High-side MOSFET.
4	VGS_LA	R	0b	Gate driver fault status on the A Low-side MOSFET.
3	VGS_HB	R	0b	Gate driver fault status on the B High-side MOSFET.
2	VGS_LB	R	0b	Gate driver fault status on the B Low-side MOSFET.
1	VGS_HC	R	0b	Gate driver fault status on the C High-side MOSFET.
0	VGS_LC	R	0b	Gate driver fault status on the C Low-side MOSFET.

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7.1.4 IC_STAT4 Register (Address = 3h) [Reset = 0000h]

IC_STAT4 is shown in Table 7-6.

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Table 7-6. IC_STAT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PVDD_OV	R	0b	PVDD overvoltage status
14	PVDD_UV	R	0b	PVDD undervoltage status
13	VDRAIN_OV	R	0b	VDRAIN overvoltage status
12	VDRAIN_UV	R	0b	VDRAIN undervoltage status
11	VCP_OV	R	0b	VCP overvoltage status
10	VCP_UV	R	0b	VCP undervoltage status
9	GVDD_OV	R	0b	GVDD overvoltage status
8	GVDD_UV	R	0b	GVDD undervoltage status
7	RESERVED	R	0b	Reserved
6	RESERVED	R	0b	Reserved
5	BSTA_OV	R	0b	BST overvoltage on the A High-side MOSFET
4	BSTA_UV	R	0b	BST undervoltage on the A High-side MOSFET
3	BSTB_OV	R	0b	BST overvoltage on the B High-side MOSFET
2	BSTB_UV	R	0b	BST undervoltage on the B High-side MOSFET
1	BSTC_OV	R	0b	BST overvoltage on the C High-side MOSFET
0	BSTC_UV	R	0b	BST undervoltage on the C High-side MOSFET

7.1.5 IC_STAT5 Register (Address = 4h) [Reset = 0000h]

IC_STAT5 is shown in Table 7-7.

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Table 7-7. IC_STAT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved
14	PVDD_UVW	R	0b	PVDD undervoltage warning status
13-11	RESERVED	R	0b	Reserved
10	GVDD_CP_LDO	R	0b	GVDD operating mode status 0b = Charge pump 1b = LDO mode
9	OTSD	R	0b	
8	WDT_FLT	R	0b	Watch dog timer fault bit
7	SPI_CRC_FLT	R	0b	SPI CRC fault bit
6	SPI_ADDR_FLT	R	0b	SPI Address fault bit
5	SPI_CLK_FLT	R	0b	SPI Clock Framing fault bit. For 32-bit frame (SPI_CRC_EN is 1), the SPI_CLK_FLT is set to 1 if the number of SPI clock of one SPI frame is 1 to 31, 33 or higher. The SPI_CLK_FLT is 0 if the number of SPI clocks is 0 or 32. For 24-bit frame (SPI_CRC_EN is 0b), the SPI_CLK_FLT is 0 if the number of SPI clocks is 0 or 24. For 96-bit frame, the SPI_CLK_FLT is 0 if the number of SPI clocks is 0 or 96. Otherwise, SPI_CLK_FLT is set to 1.
4	OTP_CRC_FLT	R	0b	OTP CRC fault bit. A fault of OTP memory used for device production has been detected.

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Table 7-7. IC_STAT5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OTP_USR_CRC_FLT	R	0b	USER OTP CRC fault. A fault of OTP memory used for user configuration has been detected. The OTP_USR_CRC_FLT will always be set to 1b if USER OTP is not used (programmed), and the flag must be cleared at power up. The OTP_USR_CRC_FLT doesn't affect nFAULT or Gate Drivers.
2	RESERVED	R	0b	Reserved
1	STP_FLT	R	0b	Shoot Through Protection violation
0	DEADT_FLT	R	0b	Dead time violation

7.1.6 IC_STAT6 Register (Address = 5h) [Reset = 0000h]

IC_STAT6 is shown in Table 7-8.

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Table 7-8. IC_STAT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PHCA_FLT	R	0b	Indicates phase comparator fault of PHCA
14	PHCB_FLT	R	0b	Indicates phase comparator fault of PHCB
13	PHCC_FLT	R	0b	Indicates phase comparator fault of PHCC
12	RESERVED	R	0b	Reserved
11	VREF_OV	R	0b	VREF input overvoltage status
10	VREF_UV	R	0b	VREF input undervoltage status
9	VDDSDO_UV	R	0b	Device internal regulator VDDSDO regulator undervoltage status
8	RESERVED	R	0b	Reserved
7	DVDD_OV	R	0b	DVDD overvoltage status
6-5	RESERVED	R	0b	Reserved
4	ABIST_FLT	R	0b	Analog BIST fault status
3	DEV_MODE_FLT	R	0b	Device mode fault status
2-1	RESERVED	R	0b	Reserved
0	CLK_MON_FLT	R	0b	Clock monitor fault status

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7.2 CONTROL Registers

Table 7-9 lists the memory-mapped registers for the CONTROL registers. All register offset addresses not listed in Table 7-9 are considered as reserved locations and the register contents are not to be modified.

Table 7-9. CONTROL Registers

Address	Acronym	Register Name	Section
1Ah	IC_CTRL1	IC Control Register 1	Section 7.2.1
1Bh	IC_CTRL2	IC Control Register 2	Section 7.2.2
1Ch	IC_CTRL3	IC Control Register 3	Section 7.2.3
1Eh	GD_CTRL1	Gate Drive Control Register 1	Section 7.2.4
1Fh	GD_CTRL2	Gate Drive Control Register 2	Section 7.2.5
21h	GD_CTRL3	Gate Drive Control Register 3	Section 7.2.6
22h	GD_CTRL3B	Gate Drive Control Register 3B	Section 7.2.7
23h	GD_CTRL4	Gate Drive Control Register 4	Section 7.2.8
24h	GD_CTRL5	Gate Drive Control Register 5	Section 7.2.9
25h	GD_CTRL6	Gate Drive Control Register 6	Section 7.2.10
26h	GD_CTRL7	Gate Drive Control Register 7	Section 7.2.11
29h	CSA_CTRL	CSA Control Register	Section 7.2.12
2Bh	MON_CTRL1	Monitor Control Register 1	Section 7.2.13
2Ch	MON_CTRL2	Monitor Control Register 2	Section 7.2.14
2Dh	MON_CTRL3	Monitor Control Register 3	Section 7.2.15
2Eh	MON_CTRL4	Monitor Control Register 4	Section 7.2.16
2Fh	MON_CTRL5	Monitor Control Register 5	Section 7.2.17
30h	MON_CTRL6	Monitor Control Register 6	Section 7.2.18
33h	DIAG_CTRL1	Diagnostic Control Register1	Section 7.2.19
36h	SPI_TEST	SPI Test Register	Section 7.2.20
48h	OTP_USR	OTP User control	Section 7.2.21

Complex bit access types are encoded to fit into small table cells. Table 7-10 shows the codes that are used for access types in this section.

Table 7-10. CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.2.1 IC_CTRL1 Register (Address = 1Ah) [Reset = 0000h]

IC_CTRL1 is shown in Table 7-11.

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Table 7-11. IC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0b	Reserved
0	VDDSDO_SEL	R/W	0b	VDDSDO regulator output selection bit. The bit determines VOH level of SDO and PHCx between 3.3V mode or 5V mode. The VIH/VIL of input buffers are not affected by VDDSDO_SEL bit. Before VDDSDO_SEL is set, VDDSDO_MON_LVL needs to be correctly configured. 0b = SDO/PHCx 3.3V mode 1b = SDO/PHCx 5V mode

7.2.2 IC_CTRL2 Register (Address = 1Bh) [Reset = 0006h]

IC_CTRL2 is shown in Table 7-12.

Return to the Summary Table.

Table 7-12. IC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ENABLE_DRV	R/W	0b	Enable predriver bit. The bit is cleared to 0b if one or multiple predriver shutdown conditions are detected and fault flags are set to 1b and if ALL_CH is 1b, or if DRVOFF is driven high. The ENABLE_DRV bit is forced to 0b by device while the fault condition exists or while DRVOFF is high. At power up, write access to ENABLE_DRV is ignored and the bit cannot be set to 1 until nFAULT goes high. After nFAULT goes high, wait 5us and set ENABLE_DRV to 1b. During initial setup, it's recommended to set the gate drive current IDRVx settings before ENABLE_DRV is set to 1b. 0b = INHx and INLx digital inputs are ignored and the gate driver outputs are pulled low (active pull down) by default. 1b = Gate driver outputs are controlled by INHx and INL digital inputs. If IDRVP or IDRVN register values is modified while ENABLE_DRV is 1b, the one PWM cycle delay is expected to get the gate driver current updated.
14	MODE_NSLEEP	R/W	0b	nSLEEP Mode. 0b = nSLEEP is active low and device enters sleep mode when nSLEEP is driven low. 1b = nSLEEP is active low and device enters DRVOFF shutdown mode when nSLEEP is driven low. Internal regulators including GVDD charge pump and TCP/VCP charge pumps are active. If WDT_FLT is detected, the device enters sleep mode when nSLEEP is low regardless of MODE_NSLEEP bit.
13	CFG_CRC_EN	R/W	0b	Enable configuration data CRC function 0b = Configuration DATA CRC function is disabled. 1b = Configuration Data CRC function is enabled.
12	CLKMON_EN	R/W	0b	Clock monitor enable 0b = Clock monitor is disabled. 1b = Clock monitor is enabled.
11	CSA_EN	R/W	0b	Current Sense Amplifier Enable. If GVDD_UV_MODE is 0b (Warning mode), MCU must maintain GVDD_UV flag is 0b before CSA_EN bit is set to 1b. If GVDD_UV_MODE is 1b (Fault mode), IC disables CSA amplifier when GVDD_UV is detected. 0b = CSA is disabled. SOx are HiZ state. 1b = CSA is enabled.
10	CSA_AZ_DIS	R/W	0b	Current Sense Amplifier Auto Zero function disable 0b = CSA Auto Zero function is enabled. This bit is 0b during normal PWM/CSA operation. 1b = CSA Auto Zero function is disabled. The purpose of this bit is to disable switching activity of current sense amplifier for auto zero function. Refer to timing requirements if this bit is used.

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Table 7-12. IC_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	DIS_GVDD_SS	R/W	0b	**Note** TI recommends users to set DIS_GVDD_SS to 1b after power up for the prototype samples. The final production sample plans to remove this function Disable GVDD Charge pump soft start 0b = GVDD output load capability does not meet the spec when PVDD input voltage is lower than 7.2V. 1b = For prototype samples, TI recommends users to set the bit to 1 after power up for prototype samples.
8	GVDD_MODE	R/W	0b	GVDD Charge pump LDO mode control 0b = Normal GVDD operation. Charge pump mode and LDO mode are controlled by device. 1b = LDO mode. GVDD charge pump clock is disabled. (charge pump switching operation is disabled).
7-6	VCP_MODE	R/W	00b	VCP/TCP mode control 00b = Normal VCP/TCP operation. VCP/TCP is enabled at power up. TCP SW is enabled when SPI ENABLE_DRV is 0. When DRVOFF is high and if system expects the device to keep BST cap stay charged, VCP_MODE must be 00b. 01b = VCP/CPTH-SHx switch is disabled. VCP/TCP charge pump clock is active. This bit is valid regardless of SPI ENABLE_DRV. 10b = VCP/TCP shutdown. Both VCP/CPTH-SHx switch and VCP/TCP charge pump clock are disabled. This bit is valid regardless of SPI ENABLE_DRV. 11b = Normal VCP/TCP operation. VCP/TCP is enabled at power up. TCP SW is disabled when SPI ENABLE_DRV is 0.
5-4	RESERVED	R	0b	Reserved
3-1	LOCK	R/W	011b	Lock and unlock the register setting Bit settings not listed have no effect. 011b = Unlock all the registers 110b = Lock the settings by ignoring further register writes except to these bits.
0	CLR_FLT	R/W	0b	Clear fault. After fault event is detected and fault flag is set, TI recommends to issue CLR_FLT command first, then ENABLE_DRV command next in a separate SPI frame. If CLR_FLT and ENABLE_DRV commands are issued in the same SPI frame, CLR_FLT is higher priority and ENABLE_DRV is not set if fault flag is already latched and the device is waiting CLR_FLT. 0b = No action 1b = Clear faults. Self-clear to 0b.

7.2.3 IC_CTRL3 Register (Address = 1Ch) [Reset = 8009h]

IC_CTRL3 is shown in Table 7-13.

Return to the Summary Table.

Table 7-13. IC_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SPI_CRC_EN	R/W	1b	SPI CRC Enable 0b = SPI CRC is disabled. One SPI frame is 8-bit command, 16-bit data. 1b = SPI CRC is enabled. One SPI frame is 8-bit command, 16-bit data, and 8-bit CRC.

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Table 7-13. IC_CTRL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	WARN_MODE	R/W	0b	Warning nFAULT mode; Control nFAULT response for warning events 0b = No nFAULT reporting for warning response. Status flags are set. 1b = nFAULT is driven low for warning response. Status flags are set.
13	RESERVED	R	0b	Reserved
12	DIS_SSC	R/W	0b	TI Internal design parameter: No change is required unless notified by TI. The bit disables Spread Spectrum Clocking feature of the device internal oscillator 0b = Normal operation. Spread Spectrum Clocking feature is enabled. 1b = Spread Spectrum Clock feature is disabled for TI debug purpose.
11	RESERVED	R	0b	Reserved
10	TCP_EN_DLY	R/W	0b	Delay time to activate trickle charge pump after the device detects PWM inactive (INHx=INLx=Low) 0b = 100us (typ) 1b = 250us (typ)
9	DRVOFF_PDSEL_HS	R/W	0b	DROVFF Pull-down select for high-side gate driver 0b = High-side gate driver outputs GHx are semi active pull-down (RPDSA_HS) if DRVOFF is high. 1b = High-side gate driver outputs GHx are passive pull-down (RPD_HS) if DRVOFF is high.
8	DRVOFF_PDSEL_LS	R/W	0b	DROVFF Pull-down select for low-side gate driver 0b = Low-side gate driver outputs GLx are semi active pull-down (RPDSA_LS) if DRVOFF is high. 1b = Low-side gate driver outputs GLx are passive pull-down (RPD_LS) if DRVOFF is high.
7-4	RESERVED	R	0b	Reserved
3	OT_LVL	R/W	1b	Overtemperature shutdown threshold selection 0b = Grade 1 mode 1b = Grade 0 mode
2	RESERVED	R	0b	Reserved
1-0	OTSD_MODE	R/W	01b	Overtemperature shutdown mode 00b = Warning mode 01b = Fault (shutdown) mode 10b = No report. No shutdown. 11b = No report. No shutdown

7.2.4 GD_CTRL1 Register (Address = 1Eh) [Reset = 0138h]

GD_CTRL1 is shown in Table 7-14.

Return to the Summary Table.

Table 7-14. GD_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved

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Table 7-14. GD_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	PWM_MODE	R/W	000b	PWM mode. 000b = 6x PWM mode (INHx/INLx) 001b = 3x PWM mode with INLx enable control 010b = 3x PWM mode with SPI enable control (DRVEN_x). INLx don't affect PWM control. MCU must use this mode to generate PWM if PHC_OUTEN is 1b. 011b = 1x PWM mode (INHx/INLx) 100b = Reserved. 101b = SPI Gate Drive Mode. DRV_GHx and DRV_GLx register bits are valid. 110b = 6x PWM mode (INHx/INLx) 111b = 6x PWM mode (INHx/INLx)
11	RESERVED	R	0b	Reserved
10-9	SGD_MODE	R/W	00b	Smart Gate Drive mode 00b = Smart Gate Drive with fixed peak current control. TDRVN_D is not valid and ignored. 01b = Smart Gate Drive with dynamic peak current control. TDRVN_D is enabled.
8	SGD_TMP_EN	R/W	1b	Enable dynamic temperature control of Smart Gate Drive. 0b = SGD temperature control is disabled. IDRVP and IDRVN are constant. 1b = SGD temperature control is enabled. IDRVP (300mA or higher) and IDRVN (600mA or higher) are adjusted based on DIE_TEMP information. The IDRIVx adjustment takes place every 9ms by the device or when the SGD_TMP_EN bit changes from 0b to 1b.
7	STP_MODE	R/W	0b	Shoot-through protection report mode **Note** Other than PWM_MODE 000b, STP_MODE shall be set to 1b, otherwise a false STP_FLT flag is reported. 0b = Shoot-through protection is enabled. The gate driver outputs are forced low during a shoot-through condition. The SPI fault flag is set and the nFAULT pin is driven low when the condition is detected. Set STP_MODE to 0b only for PWM_MODE 000b (6xPWM mode). 1b = Shoot-through protection is enabled but no reporting is performed. The gate driver outputs are forced low during a shoot-through condition. No SPI fault flag is set, and the nFAULT pin stays high when the condition is detected. Other than PWM_MODE 000b, STP_MODE shall be set to 1b not to report a false STP_FLT flag.
6	RESERVED	R	0b	Reserved
5-3	DEADT	R/W	111b	Gate driver dead time 000b = 70ns 001b = 200ns 010b = 300ns 011b = 500ns 100b = 750ns 101b = 1000ns 110b = 1500ns 111b = 2000ns
2	DEADT_MODE	R/W	0b	Dead Time Insertion Mode. 0b = Dead time is inserted when device input (INHx or INLx) goes low. 1b = Dead time is inserted by monitoring gate driver outputs (GHx or GLx).

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Table 7-14. GD_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	DEADT_MODE_6X	R/W	00b	Dead Time Violation Response Mode for 6 PWM mode only. NOTE: Other than 6 PWM mode, dead time is always inserted regardless of the DEADT_MODE bit and no fault is reported to the MCU. 00b = Dead-time protection is enabled. The gate driver control signals are enforced low during the dead time period. The SPI fault flag is set and the nFAULT pin is driven low when the dead time condition is detected. 01b = Dead-time protection is enabled but no reporting is performed. The gate driver outputs are forced low during the dead time period. The SPI fault flag is never set and the nFAULT pin stays high when the dead time condition is detected 10b = Dead-time protection is disabled. No dead time is inserted. No SPI fault flag is set and the nFAULT1 pin stays high. This is applied to both the cases when DEADT_MODE is 0b (monitoring INH or INL) and 1b (monitoring GHx or GLx). 11b = Dead-time protection is enabled and SPI fault is set but no nFAULT reporting is performed. The gate driver outputs are forced low during the dead time period. The nFAULT pin stays high when the dead time condition is detected.

7.2.5 GD_CTRL2 Register (Address = 1Fh) [Reset = 0717h]

GD_CTRL2 is shown in Table 7-15.

Return to the Summary Table.

Table 7-15. GD_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0b	Reserved
11-8	TDRVP	R/W	0111b	Peak source pull up drive timing 0000b = 0.143us 0001b = 0.179us 0010b = 0.321us 0011b = 0.464us 0100b = 0.607us 0101b = 0.750us 0110b = 0.893us 0111b = 1.036us 1000b = 1.321us 1001b = 1.607us 1010b = 1.893us 1011b = 2.179us 1100b = 2.536us 1101b = 2.964us 1110b = 3.393us 1111b = 3.821us

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Table 7-15. GD_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	TDRVN_D	R/W	0001b	Peak sink pull down pre-discharge timing 0000b = 70ns 0001b = 140ns 0010b = 211ns 0011b = 281ns 0100b = 351ns 0101b = 421ns 0110b = 491ns 0111b = 561ns 1000b = 632ns 1001b = 702ns 1010b = 772ns 1011b = 842ns 1100b = 912ns 1101b = 982ns 1110b = 1053ns 1111b = 1123ns
3-0	TDRVN	R/W	0111b	Peak sink pull down drive timing. Refer to TDRVP

7.2.6 GD_CTRL3 Register (Address = 21h) [Reset = 0700h]

GD_CTRL3 is shown in Table 7-16.

Return to the Summary Table.

Table 7-16. GD_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0b	Reserved
11-8	TDRVN_SDD	R/W	0111b	Smart shutdown discharge timing. Refer to TDRVN_D
7-6	RESERVED	R	0b	Reserved
5-0	IDRVN_SD	R/W	000000b	Smart shutdown drive current.

7.2.7 GD_CTRL3B Register (Address = 22h) [Reset = 0000h]

GD_CTRL3B is shown in Table 7-17.

Return to the Summary Table.

Table 7-17. GD_CTRL3B Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0b	Reserved
13-8	IDRVN_D_H	R/W	000000b	Peak sink pull down pre-discharge current for high-side gate driver. Refer to IDRIVE description
7-6	RESERVED	R	0b	Reserved
5-0	IDRVN_D_L	R/W	000000b	Peak sink pull down pre-discharge current for low-side gate driver. Refer to IDRIVE description

7.2.8 GD_CTRL4 Register (Address = 23h) [Reset = 0000h]

GD_CTRL4 is shown in Table 7-18.

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Table 7-18. GD_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PWM1X_COM	R/W	0b	1x PWM Commutation Control 0b = 1x PWM mode uses synchronous rectification 1b = 1x PWM mode uses asynchronous rectification
14	PWM1X_DIR	R/W	0b	1x PWM Direction. In 1x PWM mode this bit is ORed with the INHC (DIR) input
13-12	PWM1X_BRAKE	R/W	00b	1x PWM output configuration 00b = Outputs follow commanded inputs 01b = Turn on all three low-side MOSFETs 10b = Turn on all three high-side MOSFETs 11b = Turn off all six MOSFETs (coast)
11-10	RESERVED	R	0b	Reserved
9	IDRVP_CFG	R/W	0b	IDRVP configuration mode 0b = IDRVP register is not valid and ignored. IDRV_RATIO is used to determine IDRVP parameter if IDRVN is in the range of 000000b (0.7mA) - 100011b (247mA). If IDRVN is 100100b (600mA) - 101100b (2000mA), IDRVP uses the same setting as IDRVN. For example, if IDRVN is set to 100100b (600mA), IDRVP is 100100b (300mA) where pull-up current is typically half of pull-down current. 1b = IDRVP register is used to determine IDRVP parameter. IDRV_RATIO is not valid and is ignored.
8	IHOLD_SEL	R/W	0b	Select IHOLD pull-up and pull-down current. IHOLD_SEL bit must be configured while PWM is inactive (ENABLE_DRV is 0b). 0b = IHOLD pull-up/down 500mA/1000mA (typ) 1b = IHOLD pull-up/down 260mA/260mA (typ)
7-6	RESERVED	R	0b	Reserved
5	DRV_GHA	R/W	0b	Drive GHA by SPI command. PWM_MODE = 101b (SPI gate drive mode) only. This bit is valid when ENABLE_DRV is 1b. 0b = GHA is driven low 1b = GHA is driven high
4	DRV_GHB	R/W	0b	Drive GHB by SPI command. PWM_MODE = 101b (SPI gate drive mode) only. This bit is valid when ENABLE_DRV is 1b. 0b = GHB is driven low 1b = GHB is driven high
3	DRV_GHC	R/W	0b	Drive GHC by SPI command. PWM_MODE = 101b (SPI gate drive mode) only. This bit is valid when ENABLE_DRV is 1b. 0b = GHC is driven low 1b = GHC is driven high
2	DRV_GLA	R/W	0b	Drive GLA by SPI command. PWM_MODE = 101b (SPI gate drive mode) only. This bit is valid when ENABLE_DRV is 1b. 0b = GLA is driven low 1b = GLA is driven high
1	DRV_GLB	R/W	0b	Drive GLB by SPI command. PWM_MODE = 101b (SPI gate drive mode) only. This bit is valid when ENABLE_DRV is 1b. 0b = GLB is driven low 1b = GLB is driven high
0	DRV_GLC	R/W	0b	Drive GLC by SPI command. PWM_MODE = 101b (SPI gate drive mode) only. This bit is valid when ENABLE_DRV is 1b. 0b = GLC is driven low 1b = GLC is driven high

7.2.9 GD_CTRL5 Register (Address = 24h) [Reset = 0007h]

GD_CTRL5 is shown in Table 7-19.

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Table 7-19. GD_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0b	Reserved
2	DRVEN_A	R/W	1b	DRVEN_A = 0 enforces GHA and GLA low with active pull down without shutdown sequence. This bit is valid for any PWM_MODE settings. This bit is valid when ENABLE_DRV is 1b. 0b = GHA and GLA are actively pulled down (low). ENABLE_DRV is not affected by this bit. 1b = No affect. GHA and GLA are controlled normally depending following PWM_MODE setting.
1	DRVEN_B	R/W	1b	DRVEN_B = 0 enforces GHB and GLB low with active pull down without shutdown sequence. This bit is valid for any PWM_MODE settings. This bit is valid when ENABLE_DRV is 1b. 0b = GHB and GLB are actively pulled down (low). ENABLE_DRV is not affected by this bit. 1b = No affect. GHB and GLB are controlled normally depending following PWM_MODE setting.
0	DRVEN_C	R/W	1b	DRVEN_C = 0 enforces GHC and GLC low with active pull down without shutdown sequence. This bit is valid for any PWM_MODE settings. This bit is valid when ENABLE_DRV is 1b. 0b = GHC and GLC are actively pulled down (low). ENABLE_DRV is not affected by this bit. 1b = No affect. GHC and GLC are controlled normally depending following PWM_MODE setting.

7.2.10 GD_CTRL6 Register (Address = 25h) [Reset = 0000h]

GD_CTRL6 is shown in Table 7-20.

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Table 7-20. GD_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0b	Reserved
13-8	IDRVP_H	R/W	000000b	High-side peak source pull up current. IDRVP_H is valid if IDRVP_CFG = 1b. IDRVP_H is not valid and ignored if IDRVP_CFG = 0b.
7-6	RESERVED	R	0b	Reserved
5-0	IDRVP_L	R/W	000000b	Low-side peak source pull up current. IDRVP_L is valid if IDRVP_CFG = 1b. IDRVP_H is not valid and ignored if IDRVP_CFG = 0b.

7.2.11 GD_CTRL7 Register (Address = 26h) [Reset = 0000h]

GD_CTRL7 is shown in Table 7-21.

Return to the Summary Table.

Table 7-21. GD_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	IDRV_RATIO_H	R/W	00b	High-side IDRVP and IDRVN ratio. IDRV_RATIO_H is valid if IDRVP_CFG = 0b and if the range of IDRVN_H is from 00000b (0.7mA) to 100011b (typ 247mA). IDRIVE_RATIO_H doesn't affect gate driver performance if IDRVN_H is 100100b(600mA) or higher setting. If IDRVP_CFG = 1b, IDRV_RATIO_H is not valid and ignored. 00b = IDRVP is IDRVN x 1 01b = IDRVP is IDRVN x 0.75 10b = IDRVP is IDRVN x 0.5 11b = IDRVP is IDRVN x 0.25

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Table 7-21. GD_CTRL7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-8	IDRVN_H	R/W	000000b	High-side peak sink pull down current. Refer to Electrical Characteristics table, IDRVN parameter.
7-6	IDRV_RATIO_L	R/W	00b	Low-side IDRVP and IDRVN ratio. IDRV_RATIO_L is valid if IDRVP_CFG = 0b and if the range of IDRVN_H is from 00000b (0.7mA) to 100011b (typ 247mA). IDRIVE_RATIO_L doesn't affect gate driver performance if IDRVN_H is 100100b(600mA) or higher setting. If IDRVP_CFG = 1b, IDRV_RATIO_L is not valid and ignored. 00b = IDRVP is IDRVN x 1 01b = IDRVP is IDRVN x 0.75 10b = IDRVP is IDRVN x 0.5 11b = IDRVP is IDRVN x 0.25
5-0	IDRVN_L	R/W	000000b	Low-side peak sink pull down current. Refer to Electrical Characteristics table, IDRVN parameter.

7.2.12 CSA_CTRL Register (Address = 29h) [Reset = 0000h]

CSA_CTRL is shown in Table 7-22.

Return to the Summary Table.

Table 7-22. CSA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	AREF_DIV	R/W	0b	VREF dividing ratio 0b = 1/2 1b = 1/8
14-12	RESERVED	R	0b	Reserved
11-8	CSA_GAIN_A	R/W	0000b	CSA Gain of SOA. Gain can be updated during PWM operation. Undefined settings (1001b - 1111b) are 40. 0000b = 5 0001b = 10 0010b = 12 0011b = 16 0100b = 20 0101b = 23 0110b = 25 0111b = 30 1000b = 40
7-4	CSA_GAIN_B	R/W	0000b	CSA Gain of SOB. Gain can be updated during PWM operation. Undefined settings (1001b - 1111b) are 40. 0000b = 5 0001b = 10 0010b = 12 0011b = 16 0100b = 20 0101b = 23 0110b = 25 0111b = 30 1000b = 40

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Table 7-22. CSA_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CSA_GAIN_C	R/W	0000b	CSA Gain of SOC. Gain can be updated during PWM operation. Undefined settings (1001b - 1111b) are 40. 0000b = 5 0001b = 10 0010b = 12 0011b = 16 0100b = 20 0101b = 23 0110b = 25 0111b = 30 1000b = 40

7.2.13 MON_CTRL1 Register (Address = 2Bh) [Reset = 4002h]

MON_CTRL1 is shown in Table 7-23.

Return to the Summary Table.

Table 7-23. MON_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	VDRAIN_OV_LVL	R/W	01b	VDRAIN Overvoltage threshold level 00b = 29.5V (typ) 01b = 34.5V (typ) 10b = 53.5V (typ) 11b = 53.5V (typ)
13	VDRAIN_MON_MODE	R/W	0b	VDRAIN monitor mode for under and over voltage monitors 0b = Warning mode 1b = Fault mode
12	BST_OV_MODE	R/W	0b	BST pin overvoltage monitor mode 0b = Warning mode 1b = Fault mode
11	BST_UV_LATCH	R/W	0b	BST pin undervoltage latch mode 0b = BST_UV is real time monitor. BST_UV is cleared to 0b when VBST exceeds VBST_UV threshold. BST_UV_MODE is ignored. 1b = BST_UV is latched when under voltage condition is detected.
10	BST_UV_MODE	R/W	0b	BST pin monitor mode. If BST_UV_LATCH is 1b, BST_UV_MODE determines Warning mode or Fault mode. Refer to BST_UV_LATCH register bit. 0b = Warning mode 1b = Fault mode
9	BST_UV_LVL	R/W	0b	BST pin undervoltage threshold level V_{BST_UV} 0b = 4.2V (typ) 1b = 7.2V (typ)
8	DVDD_OV_MODE	R/W	0b	DVDD monitor mode of over voltage monitor 0b = Warning mode 1b = Fault mode
7	GVDD_OV_MODE	R/W	0b	GVDD monitor mode of over voltage monitor 0b = Warning mode 1b = Fault mode
6	GVDD_UV_MODE	R/W	0b	GVDD monitor mode of under voltage monitor 0b = Warning mode 1b = Fault mode
5	VCP_OV_MODE	R/W	0b	VCP monitor mode of over voltage monitor 0b = Warning mode 1b = Fault mode
4	VCP_UV_MODE	R/W	0b	VCP monitor mode of under voltage monitor 0b = Warning mode 1b = Fault mode

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Table 7-23. MON_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PVDD_UVW_LVL	R/W	0b	PVDD UV Warning threshold level
2-1	PVDD_OV_LVL	R/W	01b	PVDD OV threshold level
0	PVDD_OV_MODE	R/W	0b	PVDD OV threshold monitor mode 0b = Warning mode 1b = Fault mode

7.2.14 MON_CTRL2 Register (Address = 2Ch) [Reset = 1101h]

MON_CTRL2 is shown in Table 7-24.

Return to the Summary Table.

Table 7-24. MON_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	VDS_MODE	R/W	00b	VDS overcurrent mode 00b = Warning mode. 01b = Fault mode. 10b = Reserved 11b = No report. No shutdown.
13-11	VDS_BLK	R/W	010b	VDS overcurrent blanking time
10-8	VDS_DEG	R/W	001b	VDS overcurrent deglitch time
7-6	VGS_MODE	R/W	00b	VGS monitor mode 00b = Warning mode. 01b = Fault mode. 10b = Reserved 11b = No report. No shutdown.
5-3	VGS_BLK	R/W	000b	VGS monitor blanking time
2-0	VGS_DEG	R/W	001b	VGS monitor deglitch time

7.2.15 MON_CTRL3 Register (Address = 2Dh) [Reset = 003Bh]

MON_CTRL3 is shown in Table 7-25.

Return to the Summary Table.

Table 7-25. MON_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0b	Reserved
8	VGS_LVL	R/W	0b	Gate voltage monitor threshold level when INLx/INHx = High. $V_{GS_LVL_H}$ 0b = 5.7V (typ) 1b = 7.7V (typ)
7-6	SNS_OCP_MODE	R/W	00b	Monitor mode of V_{SENSE} overcurrent protection (Rshunt monitor) 00b = Warning mode. 01b = Fault mode. 10b = Reserved 11b = No report. No shutdown.
5-3	SNS_OCP_LVL	R/W	111b	Threshold voltage of V_{SENSE} overcurrent protection (Rshunt monitor) 000b = 50mV (typ) 001b = 75mV (typ) 010b = 100mV (typ) 011b = 125mV (typ) 100b = 150mV (typ) 101b = 200mV (typ) 110b = 300mV (typ) 111b = 500mV (typ)

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Table 7-25. MON_CTRL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESERVED	R	0b	Reserved
1-0	SNS_OCP_DEG	R/W	11b	Deglitch time of V_{SENSE} overcurrent protection (Rshunt monitor) 00b = 2.0us (typ) 01b = 4.0us (typ) 10b = 6.0us (typ) 11b = 10.0us (typ)

7.2.16 MON_CTRL4 Register (Address = 2Eh) [Reset = 0000h]

MON_CTRL4 is shown in Table 7-26.

Return to the Summary Table.

Table 7-26. MON_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0b	Reserved
5	WDT_FLT_MODE	R/W	0b	Watchdog Time Fault Mode 0b = Report on nFAULT. No gate driver shutdown. 1b = Report on nFAULT. Gate Driver shutdown.
4	WDT_CNT	R/W	0b	Watchdog Time Fault Count 0b = One time WDT fault reports status flag and asserts nFAULT1 pin low. 1b = Three consecutive faults report status flag and assert nFAULT pin low. Internal counter is cleared to 0 after the three consecutive faults are detected. Internal counter can also be cleared if WDT_EN is cleared to 0b.
3	WDT_MODE	R/W	0b	Watchdog Time MODE 0b = Any valid read access reset the watchdog timer 1b = A valid write access to SPI_TEST resets the watchdog timer
2-1	WDT_W	R/W	00b	Watchdog Timer window t_{WDL} (lower window) and t_{WDU} (upper window) 00b = tWDL 0.5ms tWDU 10ms 01b = tWDL 1ms tWDU 20ms 10b = tWDL 2ms tWDU 40ms 11b = tWDL 2ms tWDU 40ms
0	WDT_EN	R/W	0b	Watchdog Time Enable 0b = Watchdog timer disabled 1b = Watchdog timer enabled

7.2.17 MON_CTRL5 Register (Address = 2Fh) [Reset = 0000h]

MON_CTRL5 is shown in Table 7-27.

Return to the Summary Table.

Table 7-27. MON_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0b	Reserved
13	VDDSDO_MON_LVL	R/W	0b	VDDSDO (Power supply of SDO) undervoltage and overvoltage monitor level. The target nominal VDDSDO voltage is either 3.3V or 5V. 0b = 3.3V mode 1b = 5V mode

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Table 7-27. MON_CTRL5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	VREF_MON_LVL	R/W	0b	VREF (CSA reference voltage) undervoltage and overvoltage monitor threshold level. The target nominal VREF voltage is either 3.3V or 5V 0b = Target nominal voltage of VREF is 3.3V. The under voltage monitor threshold is 2.8V (typ) and the overvoltage monitor threshold is 3.8V (typ). 1b = Target nominal voltage of VREF is 5V.The under voltage monitor threshold is 4.2V (typ) and the overvoltage monitor threshold is 5.8V (typ).
11	VREF_MON_MODE	R/W	0b	VREF monitor mode for under and over voltage monitors. 0b = Warning mode 1b = Fault mode
10-5	RESERVED	R	0b	
4	PHC_OUTDG_SEL	R/W	0b	Phase Comparator output (PHCx device pin) deglitch time selection 0b = No deglitch time. The device comparator output is directly routed to device pin (PHCx). 1b = Deglitch 1us (typ) is enabled, and deglitch is added on the phase comparator output.
3	PHC_MON_MODE	R/W	0b	Phase Comparator fault monitor mode 0b = Report to status register bits. No nFAULT1 reporting. No gate driver shutdown 1b = Report to status register bits and nFAULT1 is driven low. No Gate driver shutdown
2	PHC_COMPEN	R/W	0b	Phase Comparator enable 0b = disabled. Phase comparator outputs (device pin or SPI status bit) are not valid. 1b = enabled. System needs to wait 5us after enabled.
1	PHC_OUTEN	R/W	0b	Phase Output buffer enable. This bit can be enabled regardless of PWM_MODE. 0b = disabled. The output is HiZ. 1b = enabled. INLx signals are tied to low in device.
0	PHC_TH	R/W	0b	Phase Comparator threshold 0b = 75% for rising and 25% for falling 1b = 50%

7.2.18 MON_CTRL6 Register (Address = 30h) [Reset = 20BBh]

MON_CTRL6 is shown in Table 7-28.

Return to the Summary Table.

Table 7-28. MON_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0b	Reserved
13	ALL_CH	R/W	1b	All channel shutdown enable 0b = Associated faulty half-bridge is shutdown (active pull down) in response to VDS, VGS and OCP_SNS. nFAULT goes low after all three channels have the faults. ENABLE_DRV bit is NOT cleared by the device. For a recovery sequence to re-start PWM, MCU uses CLR_FLT and clears ENABLE_DRV (can be in one SPI command), then set ENABLE_DRV to 1b. 1b = All three half-bridges are shutdown (semi-active pull down) in response to VDS, VGS and OCP_SNS. nFAULT goes low if one or multiple channels have the faults. ENABLE_DRV bit is cleared to 0b by the device.

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Table 7-28. MON_CTRL6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CBC	R/W	0b	Cycle By Cycle shutdown retry mode enable. This bit is applied to Fault mode of VDS and SNS_OCP detection. One counter is implemented internally for each phase. 0b = Cycle By Cycle retry mode is disabled 1b = Cycle By Cycle retry mode is enabled. When gate driver is shutdown when VDS or SNS_OCP fault is detected (fault mode), PWM outputs are automatically retried when a new PWM input (either rising or falling edge of INLx/INHx) is given. The status flag is latched. If nFAULT reporting is enabled, nFAULT is asserted (low) when CBC count reaches at CBC_CNT + 1b.
11	CBC_CNT	R/W	0b	Cycle By Cycle shutdown retry count selection. The CBC retry finishes after the retry count reaches at CBC_CNT (after CBC_CNT + 1 faults are detected). If ALL_CH = 1b, ENABLE_DRV is cleared after CBC retry finishes. After ENABLE_DRV is cleared, the CBC_CNT is reset to 0 when ENABLE_DRV is set to 1. If CBC_CNT is cleared when CLR_FLT is set 1. 0b = CBC retry is repeated 3 times. CBC retry finishes at 4th fault. 1b = CBC retry is repeated 10 times. CBC retry finishes at 11th fault.
10-8	RESERVED	R	0b	Reserved
7-4	VDS_LVL_HS	R/W	1011b	VDS overcurrent threshold for high-side MOSFETs
3-0	VDS_LVL_LS	R/W	1011b	VDS overcurrent threshold for low-side MOSFETs. The threshold setting is identical to VDS_LVL_HS

7.2.19 DIAG_CTRL1 Register (Address = 33h) [Reset = 0000h]

DIAG_CTRL1 is shown in Table 7-29.

Return to the Summary Table.

Table 7-29. DIAG_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0b	Reserved
5	PHDEN_HA	R/W	0b	Phase Diagnostic switch enable on high-side channel A (VDRAIN-SHA) 0b = No effect 1b = Phase Diagnostic switch is enabled. VDS_Hx and VDS_Lx flags change from the fault detection to the real monitor status. If all PHDEN_x bits are cleared to all 0s, VDS_xx flags are cleared by device.
4	PHDEN_LA	R/W	0b	Phase Diagnostic switch enable on low-side channel A (SHA-GND) 0b = No effect 1b = Phase Diagnostic switch is enabled. VDS_LA bit is real monitor status of SHA-SLA voltage
3	PHDEN_HB	R/W	0b	Phase Diagnostic switch enable on high-side channel B (VDRAIN-SHB) 0b = No effect 1b = Phase Diagnostic switch is enabled. VDS_Hx and VDS_Lx flags change from the fault detection to the real monitor status.
2	PHDEN_LB	R/W	0b	Phase Diagnostic switch enable on low-side channel B (SHB-GND) 0b = No effect 1b = Phase Diagnostic switch is enabled. VDS_LB bit is real monitor status of SHB-SLB voltage
1	PHDEN_HC	R/W	0b	Phase Diagnostic switch enable on high-side channel C (VDRAIN-SHC) 0b = No effect 1b = Phase Diagnostic switch is enabled. VDS_Hx and VDS_Lx flags change from the fault detection to the real monitor status.

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Table 7-29. DIAG_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PHDEN_LC	R/W	0b	Phase Diagnostic switch enable on low-side channel C (SHC-GND) 0b = No effect 1b = Phase Diagnostic switch is enabled. VDS_LC bit is real monitor status of SHC-SLC voltage

7.2.20 SPI_TEST Register (Address = 36h) [Reset = 0000h]

SPI_TEST is shown in Table 7-30.

Return to the Summary Table.

Table 7-30. SPI_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SPI_TEST	R/W	0000000000000000b	SPI Test register. Write access to this register has no effect on device operation.

7.2.21 OTP_USR Register (Address = 48h) [Reset = 0000h]

OTP_USR is shown in Table 7-31.

Return to the Summary Table.

Table 7-31. OTP_USR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0b	Reserved
4	OTP_USR_P_VER	R/W	0b	Enables memory verification of User OTP Program. The bit is used after user OTP is programmed by user. MCU waits until the bit is cleared to 0 by the device, and then MCU must check OTP_USR_CRC_FLT for the verification result. OTP_USR_PRG and OTP_USR_P_VER shall never be set to 1b at the same time. 0b = User OTP Verification is inactive 1b = User OTP Verification is enabled and is active. The device runs CRC automatically, and OTP_USR_CRC_FLT status bit is set to 1b if User OTP Verification is failing.
3-1	OTP_USR_P_ACC	R/W	000b	Access control of User OTP Program and User OTP Verification. The write access of OTP_USR_PRG bit is not available unless the following value is written in sequence; 0x2, 0x1, 0x4. Any other undefined values are ignored and the reset the internal sequence logic. The device returns read 0x7 if the sequence values are accepted. After the sequence is accepted by device (read =0x7), any write access (including 0x2, 0x1, 0x4) to this register resets the sequence logic (read = 0x0). 000b = Read returned data if sequence logic is reset. 001b = The 2nd data to be entered in the sequence 010b = The 1st data to be entered in the sequence 100b = The 3rd data to be entered in the sequence 111b = Read returned data if the sequence commands are accepted by device and write access to OTP_USR_PRG is allowed.
0	OTP_USR_PRG	W	0b	Program User OTP. MCU sets the bit to 1 to enable OTP program. MCU waits until the bit is cleared to 0 by the device. OTP_USR_PRG and OTP_USR_P_VER shall never be set to 1b at the same time. When OTP_USR_PRG is set to 1, the following SPI register bits shall be configured accordingly; ENABLE_DRV=0, ADC_EN=0, ADC_EN2=0, PWSPI_EN=0, WDT_EN=0, VCP_MODE=11, CLKMON_EN=0, DRVEN_A=0, DRVEN_B=0, DRVEN_C=0, CSA_EN=0, GVDD_MODE=1. 0b = User OTP Program is inactive. 1b = User OTP Program is enabled and is active.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8334 is primarily used in applications for three-phase brushless DC motor control. The design procedures in the *Section 8.2* section highlight how to use and configure the DRV8334 device.

8.2 Typical Application

8.2.1 Typical Application with 48-pin package

Figure shows a typical application diagram of DRV8334 48-pin package.

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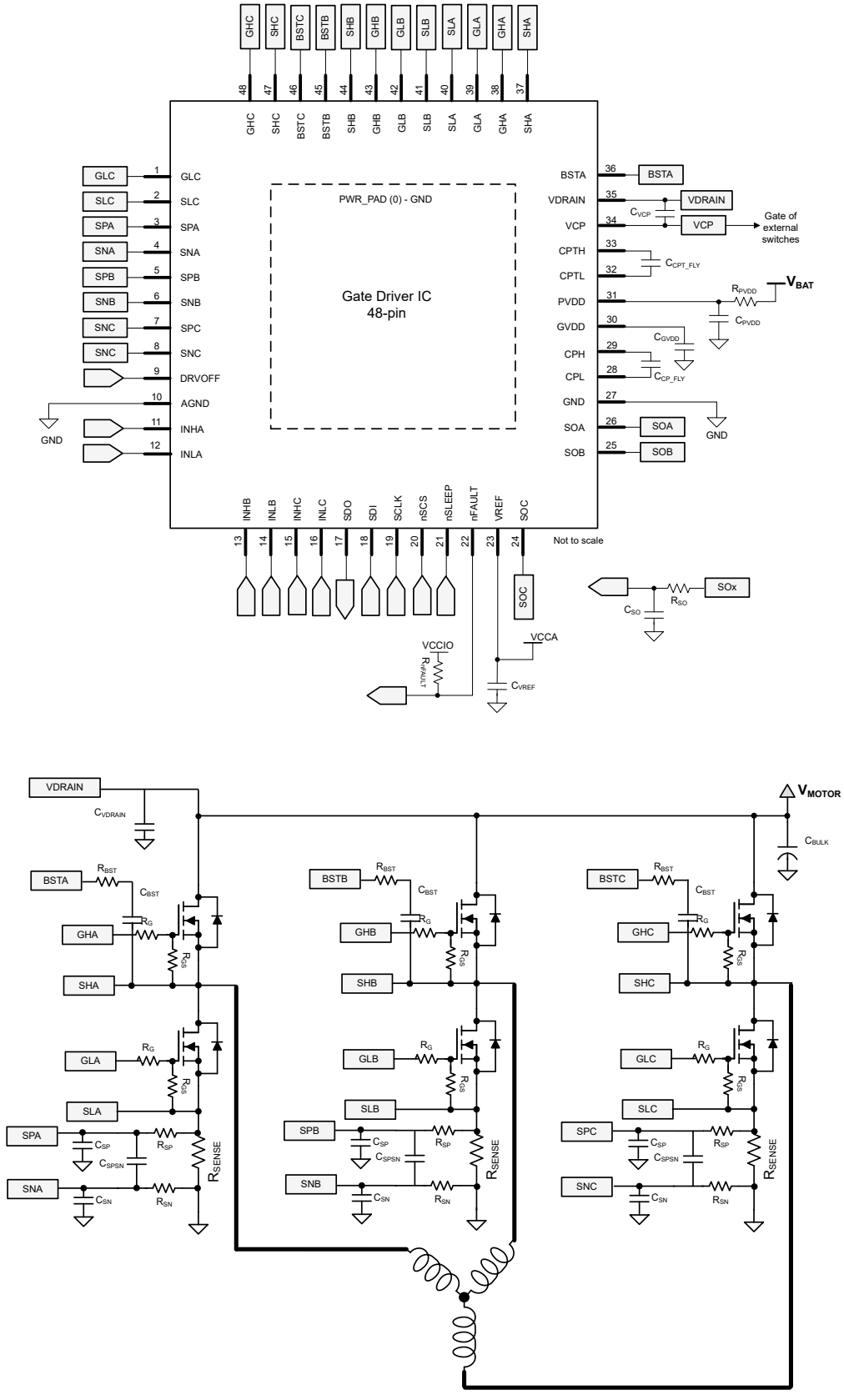

Figure 8-1. DRV8334 Typical Application Schematic

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8.2.1.1 External Components

External components lists the recommended external components. Note that the capacitances below are considered effective capacitances under nominal conditions. Consider the impact of DC derating when selecting these components.

Table 8-1. External Components (48-pin Package)

COMPONENT	PIN1	PIN2	RECOMMENDED
R_{PVDD}	V_{BAT}	PVDD	OPTIONAL: 1Ω (or smaller) series resistor
C_{PVDD}	PVDD	GND	10µF ceramic capacitor rated for PVDD.
C_{GVDD}	GVDD	GND	10µF ceramic capacitor rated for GVDD.
C_{CP_FLY}	CPH	CPL	1.0µF ceramic capacitor rated for GVDD voltage
C_{CPT_FLY}	CPTH	CPTL	1.0µF ceramic capacitor rated for GVDD voltage
C_{VCP}	VCP	VDRAIN	1.0µF ceramic capacitor rated for VCP voltage
R_{nFAULT}	VCCIO	nFAULT	10kΩ pulled up the MCU I/O power supply
C_{VREF}	VREF	GND	0.1µF ceramic capacitor rated for VREF
C_{BULK}	V_{MOTOR}	GND	100µF - 1000µF rated for V_{MOTOR}; Depending on system configuration
C_{VDRAIN}	VDRAIN	GND	1µF rated for VDRAIN
C_{BST}	BSTx	SHx	1.0µF, 20V ceramic capacitor between BSTx and SHx depending on the total gate charge of external MOSFET Q_g. $C_{BST} > 20 \times Q_g / (V_{GHX}-V_{SHx})$
R_{BST}	BSTx	SHx	OPTIONAL: 2Ω series resistor between BSTx and SHx to help prevent C_{BST} from being overcharged if big negative transient voltage is observed on SHx pin.
R_G	GHx, GLx	Gate of external MOSFET	OPTIONAL: 3Ω series resistor between GHx/GLx and Gate of external MOSFET.
R_{GS}	GHx, GLx	Source of external MOSFET	100kΩ pull down resistor between GHx/GLx and Source of external MOSFET.
R_{SENSE}	SPx	SNx	0.5mΩ Shunt resistor for current sense amplifier. System design parameter.
R_{SO}	MCU ADC	SOx	160Ω for current sense amplifier output filter
C_{SO}	MCU ADC	GND	470pF ceramic capacitor rated for AREF for current sense amplifier output filter
R_{SP}, R_{SN}	SPx/SNx	R_{SENSE}	OPTIONAL: 10Ω for current sense amplifier input filter.
C_{SPSN}	SPx	SNx	OPTIONAL: 1nF ceramic capacitor for current sense amplifier input filter.
C_{SP}, C_{SN}	SPx/SNx	GND	OPTIONAL: 1nF ceramic capacitor for current sense amplifier input filter.

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8.2.2 Application Curves

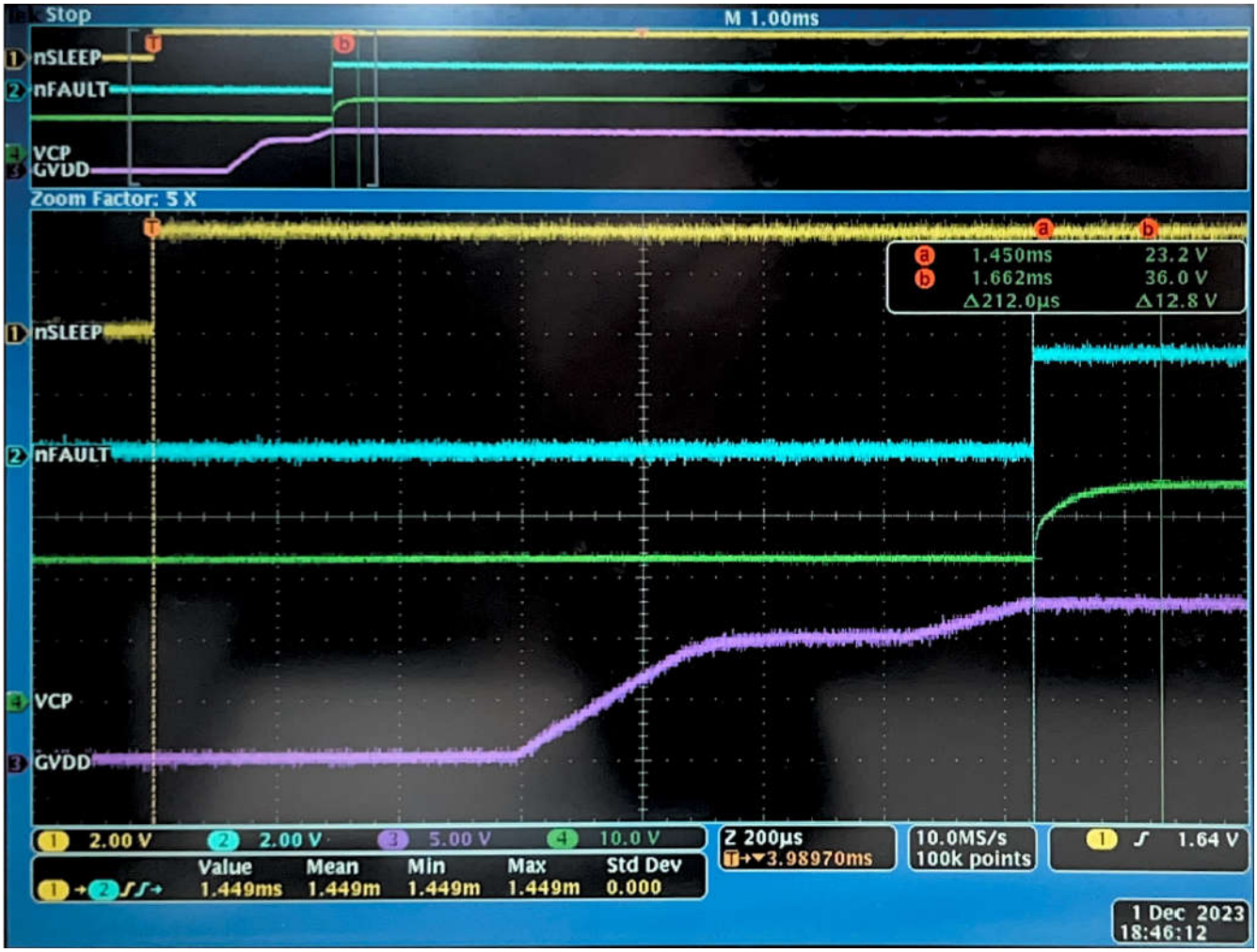

Figure 8-2. Device Powerup

8.3 Layout

8.3.1 Layout Guidelines

- Minimize length and impedance of GHx, SHx, GLx, and SLx traces. Use as few vias as possible to minimize parasitic inductance. TI recommends to increase these trace widths shortly after routing away from the device pin to minimize parasitic resistance.
- Keep BSTx capacitors close to the respective pins
- Keep CPH/CPL flying capacitor as close to the device pins as possible
- Keep PVDD capacitors close to PVDD pin
- Keep VDRAIN capacitor close to VDRAIN pin to supply steady switching current for the charge pump.
- Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance is placed to minimize the length of any high current paths through the external MOSFETs. The connecting metal traces are as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and let the bulk capacitor deliver high current.
- Connect SLx pins to MOSFET source, not directly to GND, for accurate VDS detection.
- Route SNx/SPx pins in parallel from the sense resistor to the device. Place filtering components close to the device pins to minimize post-filter noise coupling. Maintain that SNx/SPx stays separated from GND plane to achieve best CSA accuracy. The bypass capacitor across VREF and GND is placed closer to the device pin.

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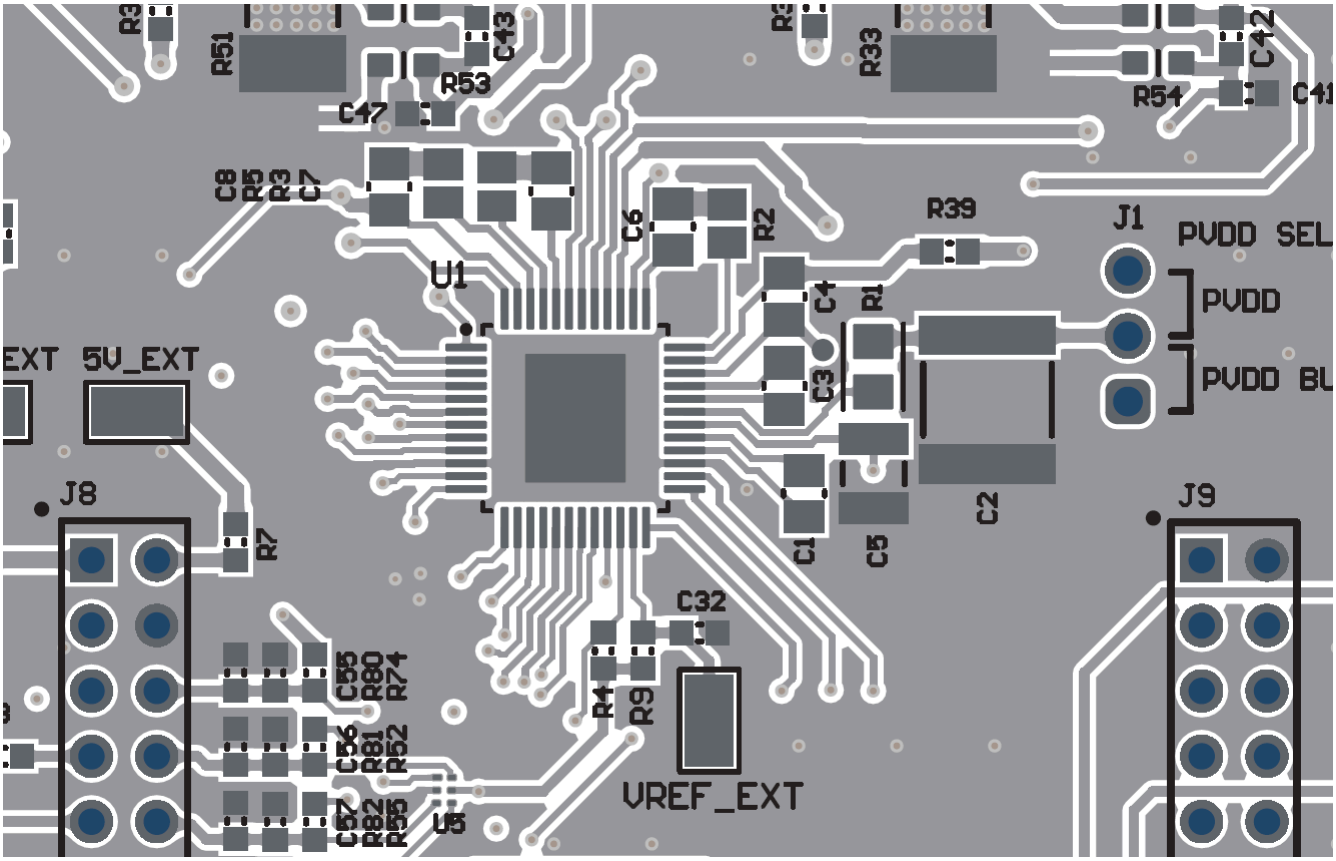
- The exposed pad is used for thermal dissipation, not electrical grounding, and has a high-impedance connection to the GND/AGND pins. Therefore, TI recommends to connect the exposed pad to the best thermal GND, and to connect the GND/AGND pins to the MCU-reference GND.

8.3.2 Layout Example



9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments,*Understanding Smart Gate Drive (Rev. D)* application report
- Texas Instruments, *Brushless-DC Motor Driver Considerations and Selection Guide (Rev. A) application report*
- Texas Instruments, *Designing High-Side and 3-Phase Isolator MOSFET Circuits in Motor Apps* application note
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers (Rev. B)* application note
- Texas Instruments,*PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments,*PowerPAD™ Made Easy* application report
- Texas Instruments,*Sensored 3-Phase BLDC Motor Control Using MSP430* application report
- Texas Instruments, *Hardware Design Considerations for an Electric Bicycle Using a BLDC Motor* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Community Resources

9.4 Trademarks

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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2023) to Revision A (May 2025)	Page
• Added QFN package to data sheet	1
• Updated the device status for DRV3233EPHP to production data.	1
• Added descriptions for PVDD Supply Undervoltage Warning, PVDD Supply Overvoltage Fault, GVDD Undervoltage Lockout, GVDD Overvoltage Fault, Bootstrap Undervoltage Lockout, Bootstrap Overvoltage Fault, VCP Undervoltage Fault, VCP Overvoltage Fault, VDRAIN Undervoltage Fault, VDRAIN Overvoltage Fault, and MOSFET VGS Monitoring Protection. Added diagrams for MOSFET VDS Overcurrent Protection	36

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8334PHPR	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8334
DRV8334PHPR.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8334
PDRV8334RGZR	Active	Preproduction	VQFN (RGZ) | 48	4000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF DRV8334 :

- Automotive : DRV8334-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

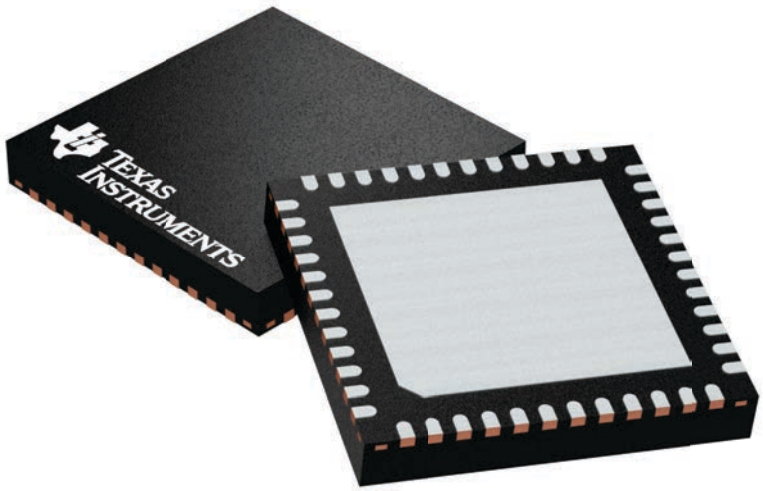
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

GENERIC PACKAGE VIEW

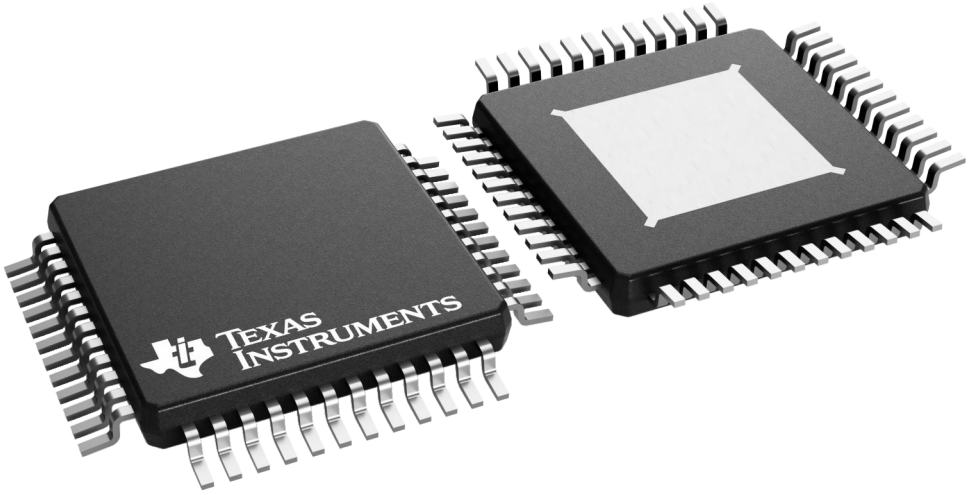
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



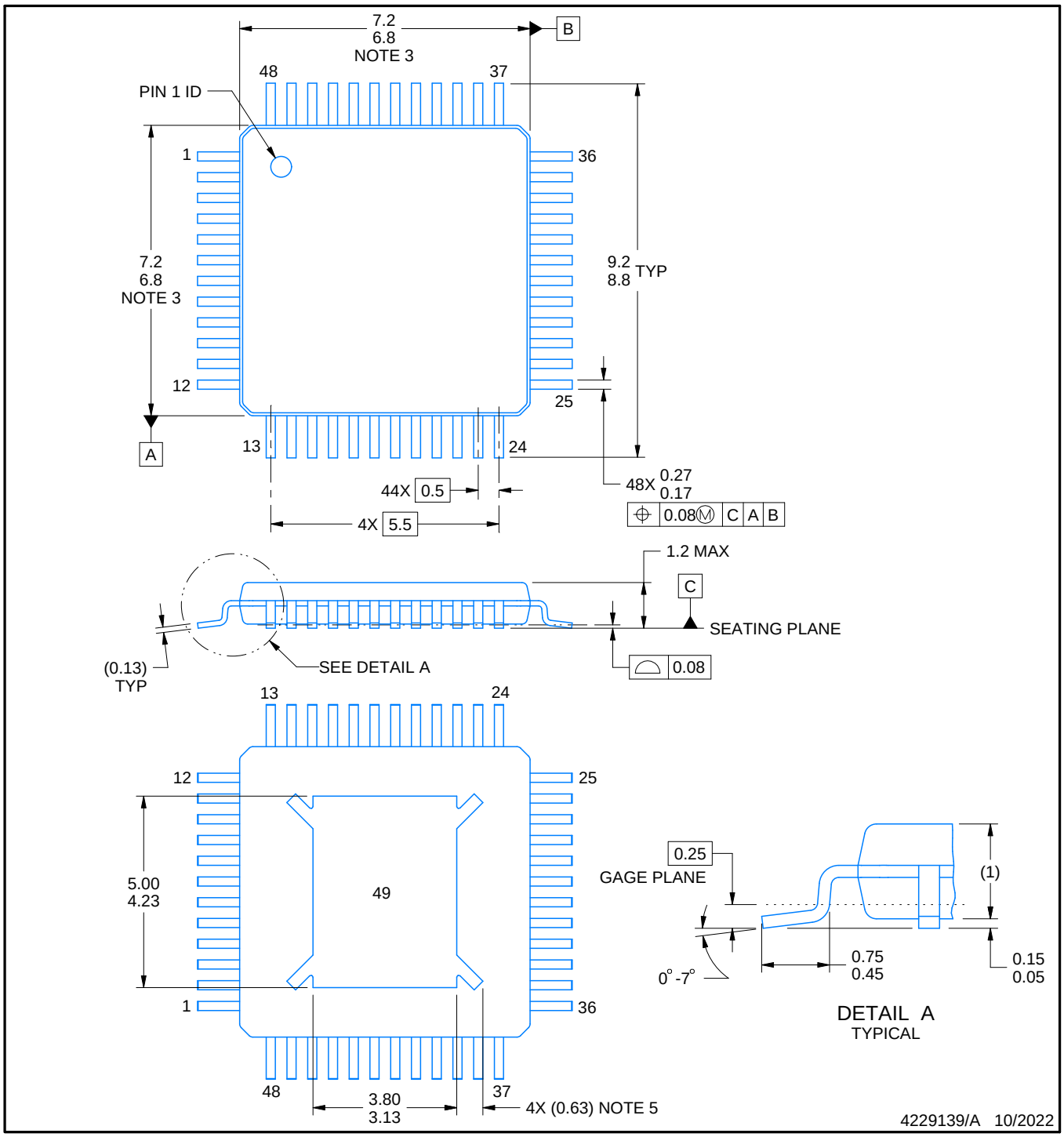
4226443/A

PACKAGE OUTLINE

PHP0048P

PowerPAD™ HTQFP - 1.2 mm max height

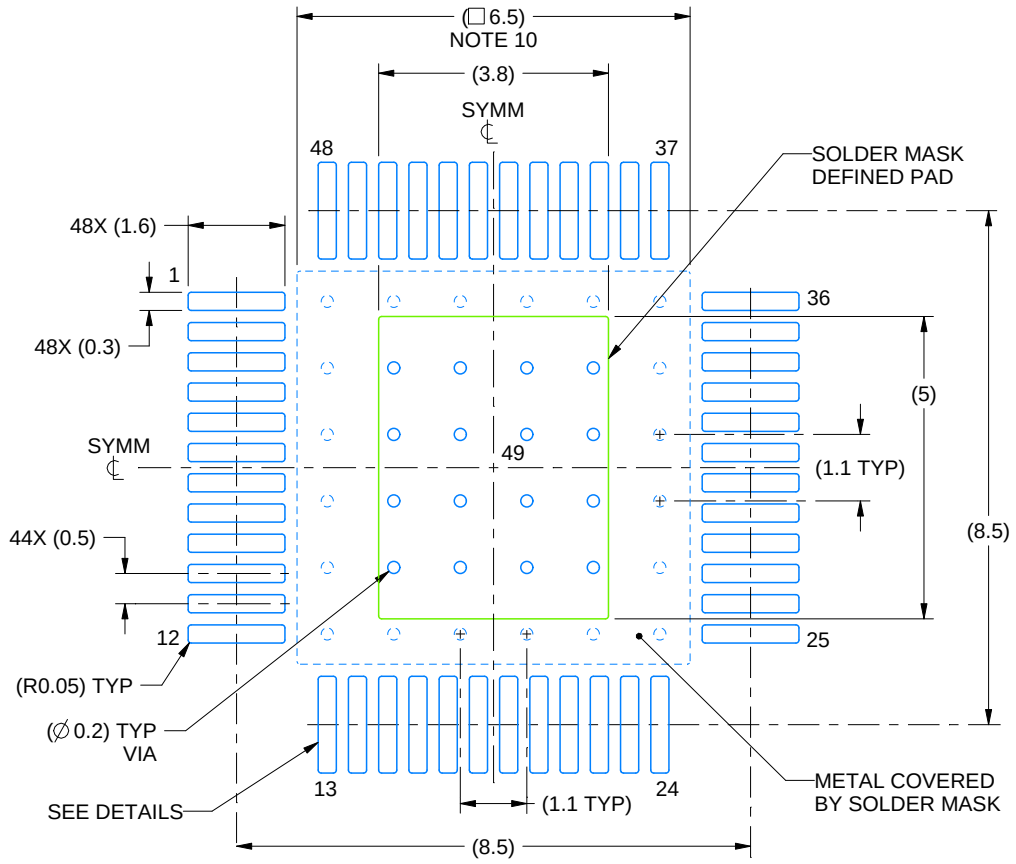
PLASTIC QUAD FLATPACK



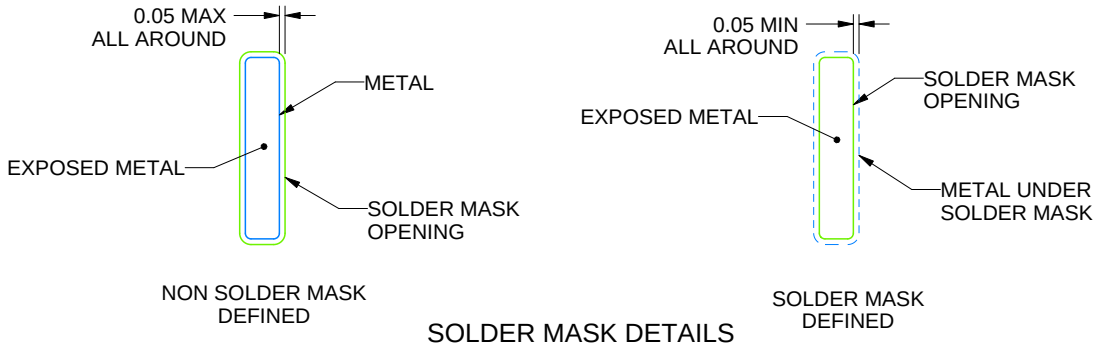
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

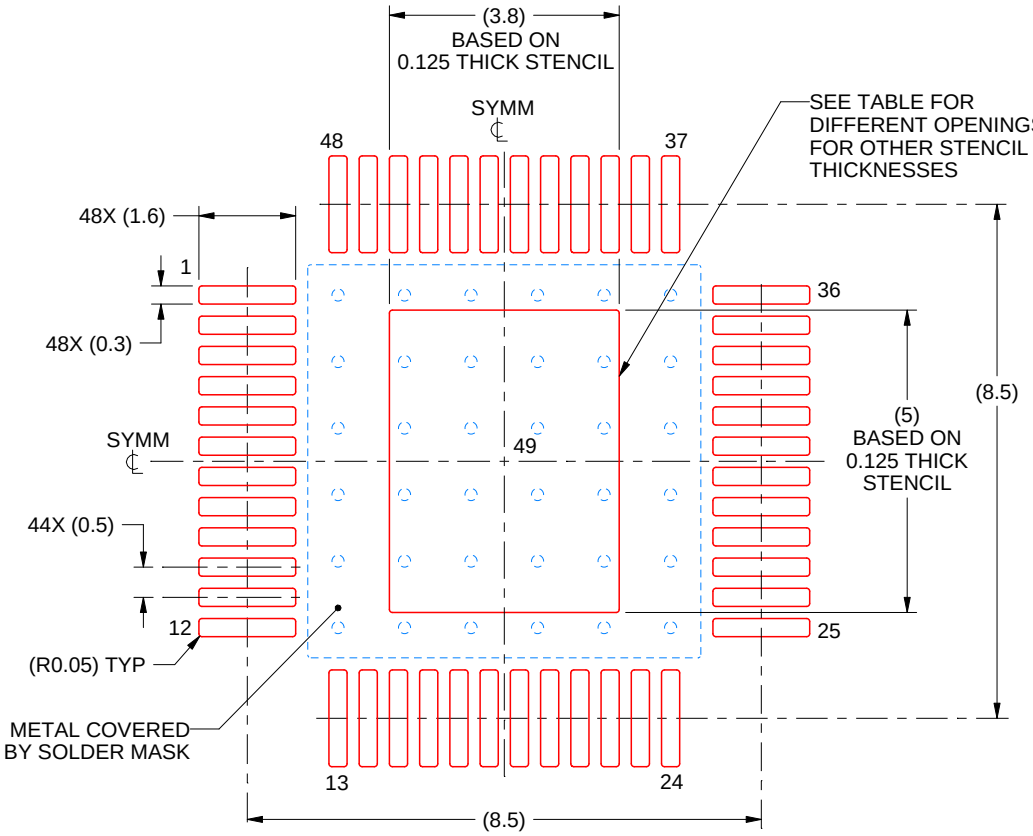


SOLDER MASK DETAILS

4229139/A 10/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.25 X 5.59
0.125	3.80 X 5.00 (SHOWN)
0.150	3.47 X 4.56
0.175	3.21 X 4.23

4229139/A 10/2022

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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